REVERSE VOLTAGE AND OVERVOLTAGE PROTECTION FOR A 5V CMOS TECHNOLOGY

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Key words: semiconductors, IC, integrated circuits, CMOS processes, CMOS technologies, reverse voltage protection, overvoltage protection, integrated protection, protection circuits, control circuits, simulation results, practical implementations

Abstract: In automotive applications the IC must withstand various hostile environments and still guarantee normal operation. One of the requests is the survival of the overvoltage and reverse supply voltage. For that usually a high-voltage process is used. In this paper a protection structure for a 5V CMOS process is presented. The proposed structure protects the internal circuit against up to +26V and down to -16V of the external supply voltage.

Vezje za zaščito pred nasprotno in previsoko napetostjo v 5V CMOS tehnologiji

Ključne besede: polprevodniki, IC vezja integrirana, CMOS procesi, CMOS tehnologije, zaščita pred napetostjo obrnjeno, zaščita pred prenapetostjo, zaščita integrirana, vezja zaščitna, vezja krmilna, rezultati simulacije, izvedbe praktične

Izvleček: Integrirana vezja, ki se uporabljajo v avtomobilskih aplikacijah, morajo biti odporna na razne sovražne vpliva okolja, kjer delujejo. Ena od takih zahtev je odpornost na previsoke napetosti in nasprotne napetosti na napajalnih priključkih. Za doseganje teh zahtev se ponavadi uporabi visoko-napetostna tehnologija in s tem elementi, ki so odporni na te napetosti. V članku je opisana zaščitna struktura v 5V CMOS procesu. Predlagana zaščita ščiti notranje napajanje integriranega vezja pred zunanjimi napetostmi v območju od -16V do +26V.

1. Introduction

The complexity and quantity of the embedded electronics in today's automotive products is steadily rising. It is expected that the value of the built in electronics will grow up to 5-10% of the total manufacturing cost of the car. Due to the large series of production the automotive electronics is usually integrated in a chip or chipset. Due to the safety and reliability requirements the IC must withstand hostile environments. The most common failures originate from various wiring problems. The most common wiring problems are shorted and disconnected lines. The IC must sense these problems, survive and signalise the existence of the problem. The IC usually operates with a regulated low-voltage supply (5V), but the supply lines can be shorted to the automotive car battery or reversed. In this article a standard CMOS technology protection structure against these overvoltage and reverse supply voltages is presented. A high-voltage CMOS technology is usually used in such applications, but the standard CMOS technology offers an advantage in the IC manufacturing cost.

2. Supply protection circuit

The supply protection circuit is made from two blocks. The first one is the actual protection structure made from four PMOS transistors, the gate controlling high-voltage NMOS transistors and from poly resistors. The second block is the control block, which monitors the supply voltage and controls the behaviour of the protection block. Each block is designed in such a way that it can also tolerate reverse supply voltages.

2.1 The PMOS protection structure

The supply protection structure is constructed from four PMOS transistors in series (the topology is presented in Figure 1.). Each gate of these PMOS transistors is controlled by a high-voltage NMOS pull-down transistor, which can tolerate drain voltages up to 35V. The series PMOS transistors are thereby switched on and off with the signal *con*, which is generated by the control circuit. In normal operation conditions the *con* signal is high, then the PMOS gates are pulled down and thereby the transistors are opened. The W/L ratio must be high and depends on the supply current of the IC. In this application the supply current is in the range of 5-10mA. The series resistance is approximately 20Ω. Because the IC also incorporates digital logic the internal supply is decoupled with a low-ohmic capacitor.

If the external supply voltage exceeds the allowed 7V, then the *con* signal goes low and the PMOS transistors are closed. The internal supply is shorted to the supply ground. The complete external supply voltage is divided between the four PMOS transistors. Because the maximum allowed PMOS drain-source voltage is 8V and the maximum expected external supply voltage is +26V four transistors have been used. If the supply voltage would stay below +24V only three transistors would be sufficient. With the use of series transistors the excessive voltage is divided between a number of devices and therefore preventing various break-

downs (gate, drain-source, diffusion to substrate ...) due to large voltages. The protection structure is made from devices available in standard CMOS processes (this also includes the high-voltage NMOS transistor).

If the IC is exposed to reverse supply voltages the numerous N-diffusion and N-well in the P substrate diodes are opened. The resulting current thermally destroys the IC. In the presented protection circuit all NP diode structures are protected by series poly resistors and thereby limiting the reverse voltage current. Special care was taken in the layout design to prevent the reverse current bipolar effects.

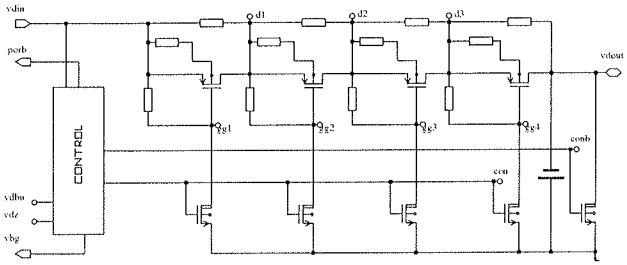

Figure 1: The overvoltage protection structure

2.2 The control circuit

The task of the control circuit is to monitor the supply voltage and detect overvoltage conditions. This is achieved with the comparison of a fraction of the external supply voltage with the reference voltage. The control circuit is made from a band-gap reference voltage source, comparator and the supply protection (Figure 2.). Because the control circuit must operate during the overvoltage condition it has its own supply protection. This protection is made from a series resistor and five transistor thresholds. If the supply voltage exceeds the 5*Vt voltage (which is process and temperature dependent) the transistors begin to conduct and therefore causing a voltage drop on the resistor. So the supply of the control circuit never exceeds the allowed maximum voltage. Because of the high resistance of the series resistor the current consumption of the control circuit must be kept low (in this case 50mA).

The band-gap voltage is compared to the fraction of the supply voltage and if this voltage exceeds the predefined voltage the control circuit outputs (*con* and *conb*) are changed. These signals are also used to set the IC output stage amplifier into a defined error signalising state, which can be detected by the IC readout electronics.

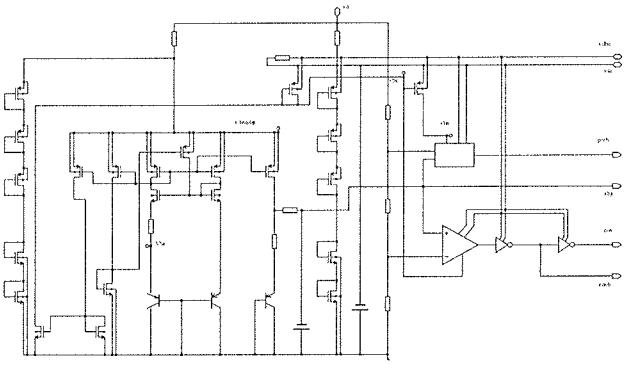

Figure 2: The control circuit

The high resistance of the supply protection resistor is also limiting the reverse voltage current.

2.3 Simulation results

Both conditions have been simulated to verify the various voltages and currents across the circuit to check if there are excessive values which could lead to the IC destruction.

In figure 3. the overvoltage condition simulation results are visible. The supply voltage is swept from 0 to 26V. At 7V the control circuit switches off the PMOS transistors. The voltage distribution across the transistors and the control signal behaviour is visible.

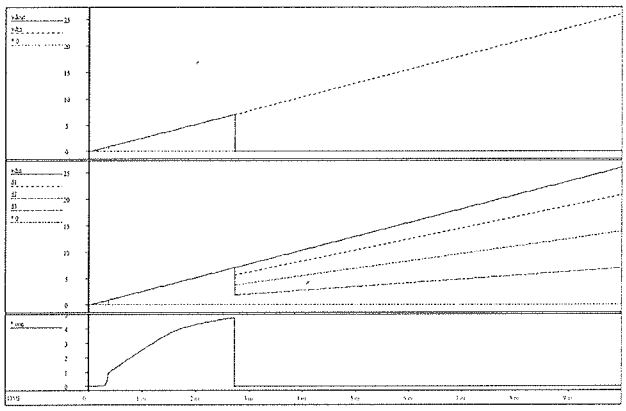

Figure 3: Overvoltage condition; voltage distribution and control signal

The reverse voltage condition simulation can be seen in Figure 4. The reverse voltage is swept from 0 to -16V. The voltages across the protection structure and the reverse current can be seen on the plot. The reverse current is limited to 1.6mA, which is sufficient to prevent damage of the IC.

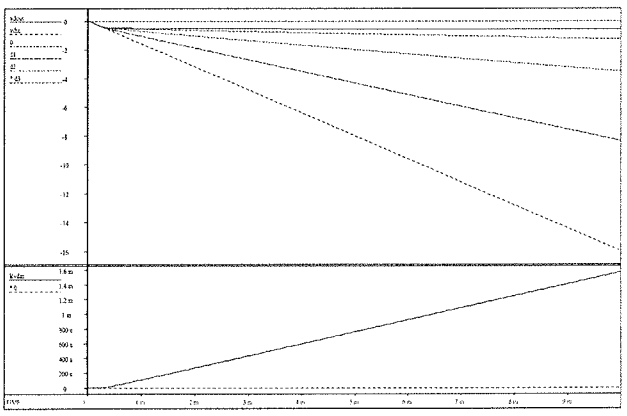

Figure 4: Reverse voltage condition; voltage distribution and reverse current

2.4 Implementation

The proposed protection structure has been implemented in a double-metal, double-poly CMOS 0.8μm technology. A test IC was fabricated to measure the circuit behaviour. The measurements proved the protection capabilities of the structure in both overvoltage and reverse voltage conditions. The layout of the implemented protection structure is in Figure 5. The protection structure is on the upper side of the IC, the control circuit on the lower side.

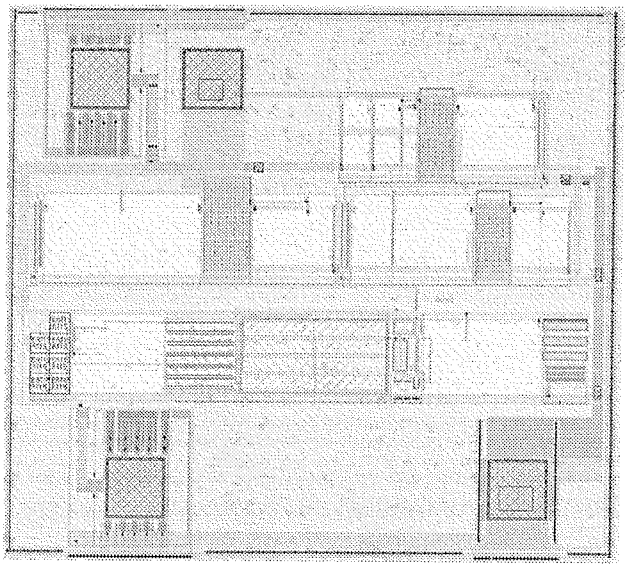

Figure 5: The protection structure test chip layout

3. Conclusion

The design and implementation of a supply protection structure was presented. It was shown that also low voltage (standard) CMOS processes can be used for IC's in applications, where the IC must withstand excessive voltages on the supply lines.

4. References

P. Menniti and S.Storti. "Low drop regulator with overvoltage protection and reset function for automotive environment." IEEE JSSC SC - 19.3 (June 1984): 442-448.

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