RATIOMETRIC-TO-SUPPLY VOLTAGE OUTPUT BUFFER DESIGN

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Key words: ratiometric, transfer function, precision, analog-to-digital, converter, gain control

Abstract: Paper is focused to design the ratiometrical - signal processing gain stage. The stage is a part of complex integrated system and is operating in a narrow frequency band. Its main part is a programmable operational amplifier, having controlled gain, automatic gain tracking with supply voltage and automatic signal ground tracking with supply voltage VDD. The stage cut-off frequency is 100Hz, the control loop -3dB frequency is at 1kHz. Precision of ratiometric control is 0.325%, accuracy is 0.6%. The main topics of present paper is to show ratiometric system behavior by the system description with its transfer function and verification using HSPICE and the MatLab tooling. The circuit is implemented in 0.8um CMOS technology.

Končna ojačevalna stopnja z lastnostmi, nastavljivimi z napajalno napetostjo

Ključne besede: prevajalna funkcija, točnost, AD pretvornik, kontrola ojačanja, sorazmeren napajanju.

Izvleček: V članku je opisana stopnja, katere lastnosti sledijo spremembi pozitivne napajalne napetosti v določenem frakvenčnem pasu. Vezje je zasnovano tako, da sledijo napajalni napetosti - ratiometrično - le lastnosti procesiranega vhodnega signala. Sestavlja ga: DC pretvornik, merilnik napajanja, AD pretvornik, regulacijska zanka za sledenje ojačanja in signalne mase. Cilj članka je opisati vezje s prevajalno funkcijo in jo verificirati s simulacijami (HSPICE), z analizo (MatLab) ter z meritvami na integriranem VLSI vezju. Vezje, kot sestavni del integriranega sistema, je bilo procesirano v 0.8um tehnologiji CMOS.

I. Introduction

The number of different integrated systems have to have output signal proportional to the supply voltage VDD. Such systems require precisely defined power supply rejection outside useful signal pass as well as good definition for signal transfer function. The ratiometric-to-supply feature is a useful function when processed signal besides its main function i.e. follow the supply voltage changes.

The main concept of ratiometry may operate in continuos time or may operate digitally weighted via analog-to-digital converter (ADC) where ratiometric signal ground (RAGND) is generated as continous analog signal with appropriate frequency response. The signal to be processed needs to be converted from system - constant analog ground (AGND) to ratiometric ground (AGND) by processing of the input signal in the level-shift gain stage.

II. Ratiometric signal processing stage

The main system transfer function is expressed as in (1). Rgr is ratiometric-variable resistor with VDD supply. Rg is programmable gain resistor (Fig. 1 in Fig. 2). To complete the function (1) with all the sub-definitions, the transfer function (1) will clearly define the supply voltage dependence, frequency response and temperature stability.

$$T(S) = (1+\frac{R_{gr}}{R_g}) \cdot \frac{1}{1+sR_1C_1} \qquad (1)$$

$$(1+\frac{R_{gr}}{R_g})$$

is the gain of output stage,

and

$$\frac{1}{1+sR_1C_1}$$

is the low-pas filter (100Hz) transfer function.

Gain stage is in non-inverting gain configuration. The gain of the stage is linearly dependent on the VDD supply voltage. Gain is programmable from A=3 to A=12 or 12 in 8 - linear steps by varying the resistor Rg. The resistor Rgr is automatically adjusted with varying of the supply voltage VDD in the range of -5% to +5% from its nominal value (5V) and nominal gain of (3 to 6). Ratiometric-gain-setting precision is 0.325% with worst-case accuracy of 0.6%. Used operational amplifier is class AB stage with open-loop gain of 104dB_min and has input referred noise of 260nV/sqrt(Hz)@ 10Hz to 93nV/sqrt(Hz)@100Hz.

Filter is placed in signal path, having no influence on supply voltage-dependent analog ground (RAGND) and vice-

versa. That principle guarantees good common-mode rejection of the output buffer and therefore no distorts the output signal. Filter in supply voltage (Vd generation) influences therefore only on output stage-gain with its low-pass characteristic. Ratiometric block is shown in Fig. 1, the simplified block diagram is on Fig. 2.

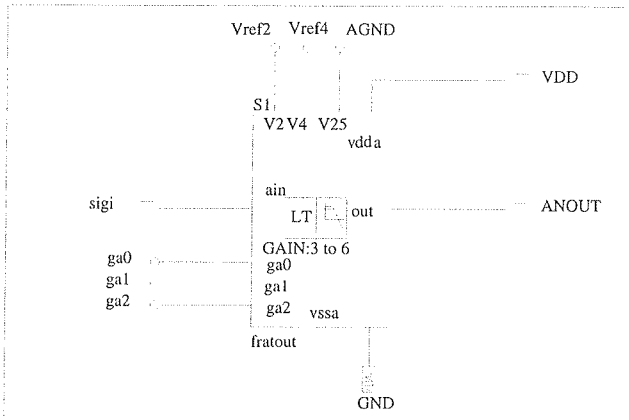

Fig. 1: Ratiometric output gain stage: sigi *is input signal, referred to AGND,* ANOUT *is the gained output signal, referred to ratiometric RAGND.*

A. Ratiometric gain

The feedback network resistor *Rgr* is controlled to follow the supply voltage variations *VDD*, and is included in *Vd*:

$$R_{gr} = R_{nf}[184 + \frac{40V_d}{V_{ref4}} - 4]$$

Rnf is a unit resistor,

$$i = \frac{40V_d}{V_{ref4}} - 4$$

the *i* is a digital code from flash ADC converter, converting the *Vd* voltage which is proportional to *VDD* supply. The accuracy of the code is defined by INL and switching point, which mainly depends on resistors matching and comparators offset voltage.

B. Ratiometric analog voltage Vd

$$V_d = (\lambda \cdot \frac{0.8x}{2x} \cdot VDD - V_{ref2}) \cdot (1 + \frac{R_{df}}{R_{da}}) + V_{ref2} \qquad (3)$$

Vd voltage depends on supply voltage *VDD* and is used for ratiometric gain tracking (1), (2). λ is voltage coefficient of the implanted well resistors. The cutoff frequency of voltage *Vd* is close to 1kHz and is expressed by:

$$Vd(j\omega) = (VDD \cdot \frac{R_3 \,\|\, \frac{1}{j\omega C_2}}{R_0 + \frac{1}{j\omega C_3} \,\|\, (R_2 + R_3 \,\|\, \frac{1}{j\omega C_2})} - V_{ref2}) \cdot \left[1 + \frac{R_{df}}{R_{da}}\right] \qquad (4)$$

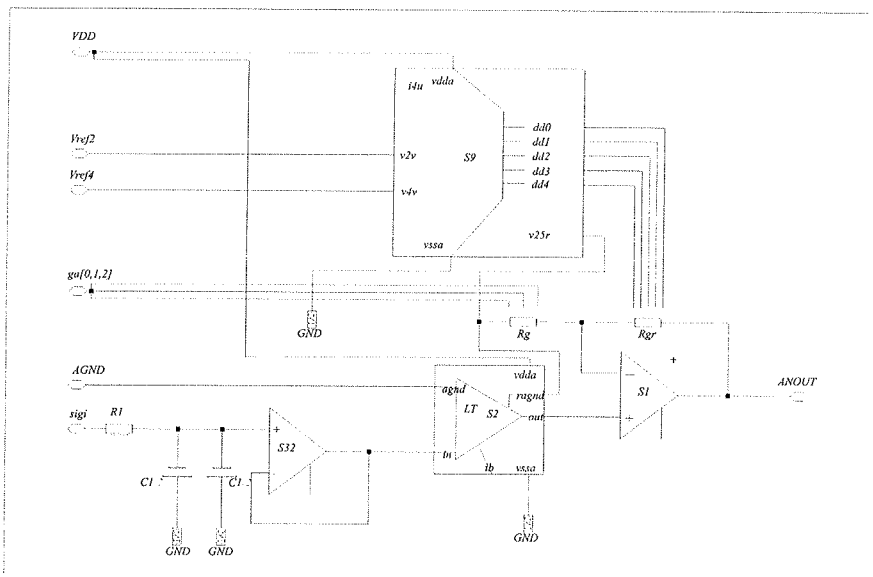

Fig. 2: Ratiometric gain stage, consists of the ratiometric signal ground generation, ratiometric gain control by measuring the supply voltage VDD with gain-control stage via 5 bit AD converter (S9), signal converter (S32), active low-pass filter, and programmable and supply voltage controlled gain - class AB operational amplifier (S1). Signal converter frequency response is also described. It acts as a common mode signal on the input terminals of the output amplifier (s1). The output amplifier has a wide frequency range (BW=9MHz) and has high input common-mode-rejection. RAGND in signal converter is therefore omitted from Transfer function (1), it is included in term Rgr.

C. AD converter

The 5 bit flash AD converter based on resistors string, array of 32 comparators and decoding logic to convert thermometer code to 5 bit binary code. The switching point of the comparator is:

$$V_{sw} = V_{refi} + V_{off}$$

where *Vrefi* is the voltage on the i-th tab of the AD resistor string, supplied by the reference voltage *Vref4* and is:

$$V_{refi} = \frac{V_{ref4}}{40R_n} \cdot (i+4)R_n + \frac{V_{ref4}}{2^5} \cdot \sum_{k=1}^{i} \frac{\Delta R_{nk}}{R_n}$$

$$V_{refi} = V_{ref4} \cdot [\frac{i+4}{40} + \frac{1}{2^5} \cdot \sum_{k=1}^{i} \frac{\Delta R_{nk}}{R_n}]$$

The digital output code is generated when the voltage on i-th tab equals to the analog voltage *Vd*, including comparator offset voltage *Voff*:

$$V_d = V_{sw}$$

From here the digital code i can be found:

$$i = \frac{40V_d}{V_{ref4}} - 4 - \frac{40}{2^5} \cdot \sum_{k=1}^{i} \frac{\Delta R_{ni}}{R_n} \qquad (5)$$

If we assume ideal resistors matching, the last term can be omitted, else the term should be taken too. The maximum accuracy errors may occur in the middle of the resistor string and cause the maximum INL error of:

$$|INL|_{\max} = \frac{V_{ref4}}{2} \cdot \frac{\Delta R_{nk}}{R_n}$$

Rn is resistive unit in the string, *ΔRnk* is the value of the resistance error (difference from ideal *Rn*) due the mismatch. Maximum error therefore may happen around nominal supply voltage.

D. Reference voltage Vref4

Reference *Vref4* is a *G1* times magnified voltage, proportional to the bandgap of silicon:

$$V_{ref4} = G_1 \cdot [V_{be}(T) + A \cdot \frac{k}{q} \cdot T \cdot \ln\left\langle \frac{J2}{J1} \right\rangle] \qquad (6)$$

Vbe is voltage of the forward biased base-emitter junction of the vertical bipolar device, *kT/q* is thermal voltage and is 26mV at 300K, J2/J1 is emitter-current density ratio. *Vref4* is constant with temperature and may vary for 20 ppm/C from its nominal value of 4V.

E. Reference voltage Vref2

Reference *Vref2* is reference voltage based on silicon-bandgap (*Vbgr=1.206V*):

$$V_{ref2} = G_2 \cdot [V_{be}(T) + A \cdot \frac{k}{q} \cdot T \cdot \ln\left\langle \frac{J2}{J1} \right\rangle] \qquad (7)$$

Voltage is stable within 20 ppm/C and has nominal value of 2V.

F. Gain programmability

The gain is adjust via trimming circuit using 3 bits (Fig. 2) which gives eight linear gain steps from nominal gain of 3. Resistors are polysilicon, temperature coefficient is cancelled-out from transfer function (1), also absolute value variations with process is canceled-out due to be fact that amplifier has sufficient open-loop gain and high enough output driving capability:

$$A_{cl} = \frac{A_{ol}}{1 + A_{ol} \cdot \frac{R_g}{R_g + R_{gr}}}$$

Aol is open loop of the class AB differential amplifier and is 104dB.

G. System signal ground

System analog ground voltage (*AGND*) is gained bandgap voltage *Vbgr* of 1.206V:

$$AGND = (1 + G_3) \cdot V_{bgr}$$

and is stable (20 ppm/C) at nominal value of 2,5V.

H. Ratiometric analog ground

The voltage is generated from *VDD* supply as a front-end analog signal to the 5 bit AD converter. The resistor divider network (R0, R2, R3) of (1, 0.2, 0.8 Mohm) and capacitors (C2, C3) of (100pF, 100pF) form a low-pass filter followed by unity gain buffer-driver.

RAGND at ω=0

$$RAGND = VDD \cdot \frac{R_2 + R_3}{R_0 + R_2 + R_3} = \frac{VDD}{2}$$

$$RAGND(j\omega) = VDD \cdot \frac{\frac{1}{j\omega C_3} \| (R_2 + R_3 \| \frac{1}{j\omega C_2})}{R_0 + \frac{1}{j\omega C_3} \| (R_2 + R_3 \| \frac{1}{j\omega C_2})} \qquad (8)$$

and has voltage coefficient due to implanted resistors used.

III. Ratiometric signal tracking with ratiometric analog ground voltage

The signal tracking stage is an inverting gain stage acts as a DC level shift to move the signal-voltage from *AGND* level to ratiometric ground level *RAGND*. Buffer amplifier is a class A stage with open-loop gain (Aol) of 99dB, gain bandwidth of 1.2MHz and input referred noise 88nV/sqrt(Hz)@10Hz to 28nV/sqrt(Hz)@100Hz. Close-loop gain error of the stage with a gain of 0dB is *[Aol/(1+Aol)]* and is negligible. The output voltage of the stage is:

$$V_{rsigi} = RAGND + V_{sigi} = \frac{VDD}{2} + V_{sigi}$$

where is *Vsigi* a signal voltage, relation is valid for ω=0.

IV. Output stage frequency response

The output stage has therefore the frequency response as follows:

$$A[dB] = 10\log[1 + (\frac{\omega_i}{\omega_p})^2]$$

Where ω*i* is a given frequency and ω*p* is the cutoff frequency, defined by low-pas filter constant (1):

$$\omega_p = \frac{1}{R_1 C_1} = \frac{1}{30x\Omega \cdot 2 \cdot 27pF} = 617r/\sec$$

which is close to 100Hz (Fig. 5 and Fig. 6).

All other poles come from level-shift circuit, ratiometric ground, etc, are at much higher frequencies.

Conclusion

The *overall* transfer function which include the frequency behavior, the **VDD** influence, the temperature and the elements matching influence described in the equations (2), (3), (4), (5), (6), ((7), (8)) can be verified by replacing appropriate variables in equation (1). The circuit has been simulated using HSPICE and transfer function verified in MatLab. Results are shown in Fig. 3, Fig. 4, and Fig. 5 -to- Fig. 9. On Fig. 5 is *overall* transfer function (1) included *Rgr(f)*.

References:

/1/ Arthur B. Williams, "ELECTRONIC FILTER DESIGN HANDBOOK", McGraw-Hill Book Company, 1981

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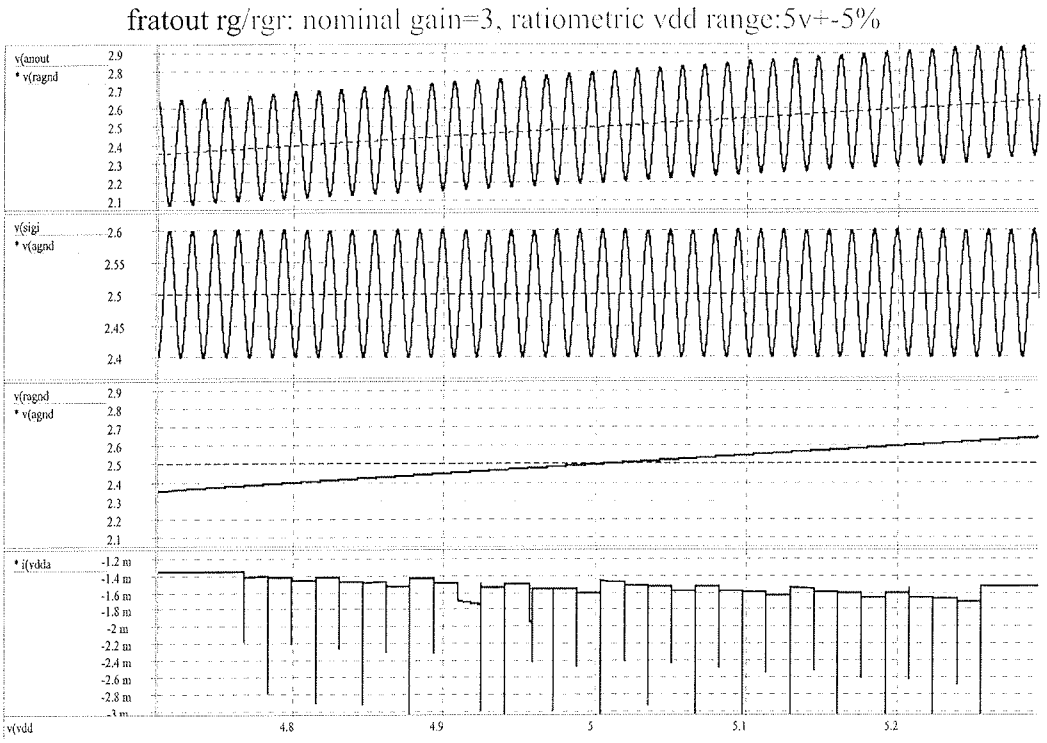

Fig. 3: Ratiometric range is limited to 5V (+-5%). Output DC level and output AC signal amplitude (ANOUT) follow the supply voltage VDD.

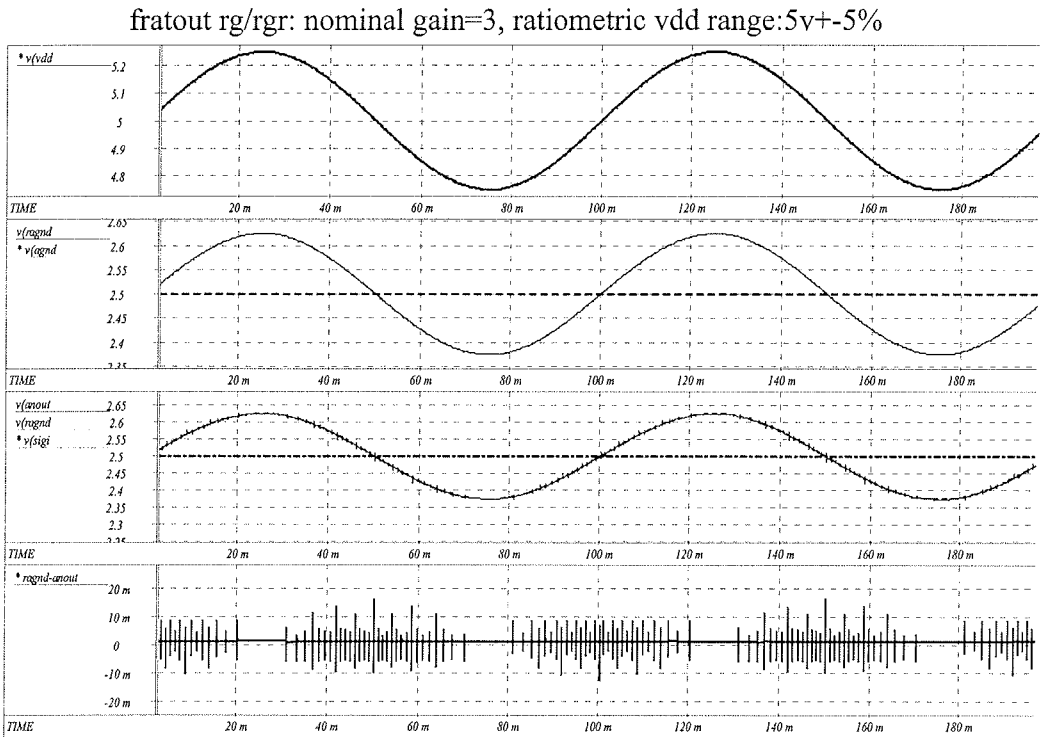

Fig. 4: Ratiometric signal ground (RAGND) follow the supply voltage without significant delay (VDD changes with 10Hz). Output at zero input signal (sigi) follows the ratiometric signal ground, having the same amplitude and frequency response. The low-pass filters have Butterworth filter characteristic, having no overshot and does not have any oscillatory behavior.

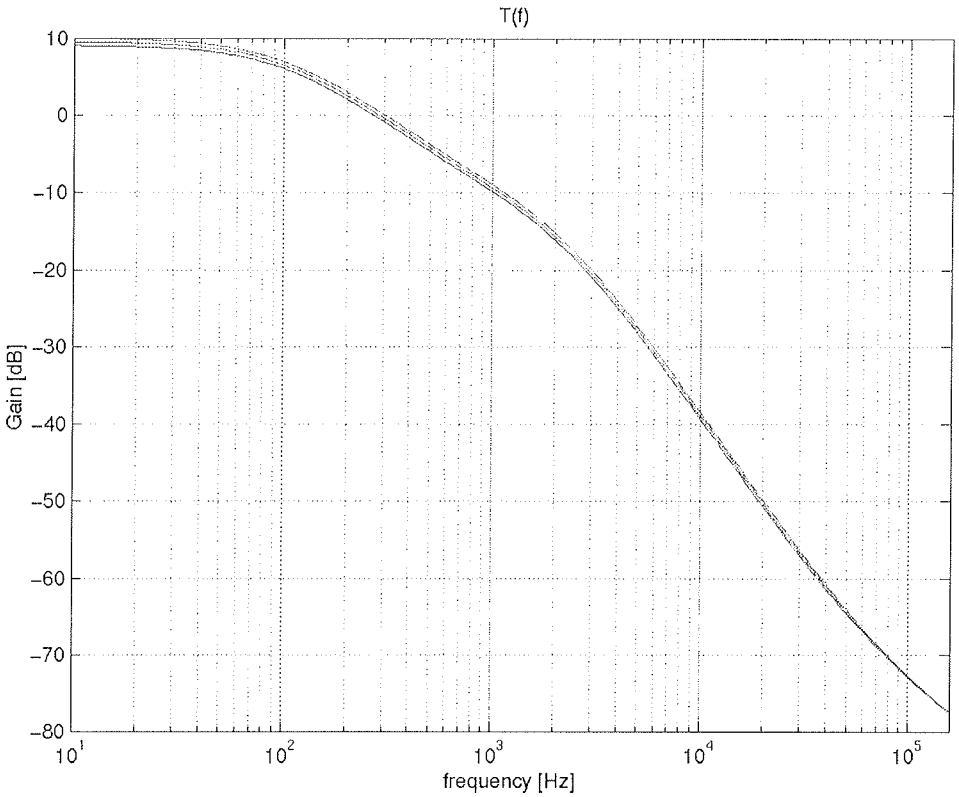

Fig. 5: Gain of "fratout" at nominal setting (g=3) for three different supply voltages (VDD=5V+-5%). Frequency response includes all blocks as is shown from Fig. 2. All equations are combined into equation (1).

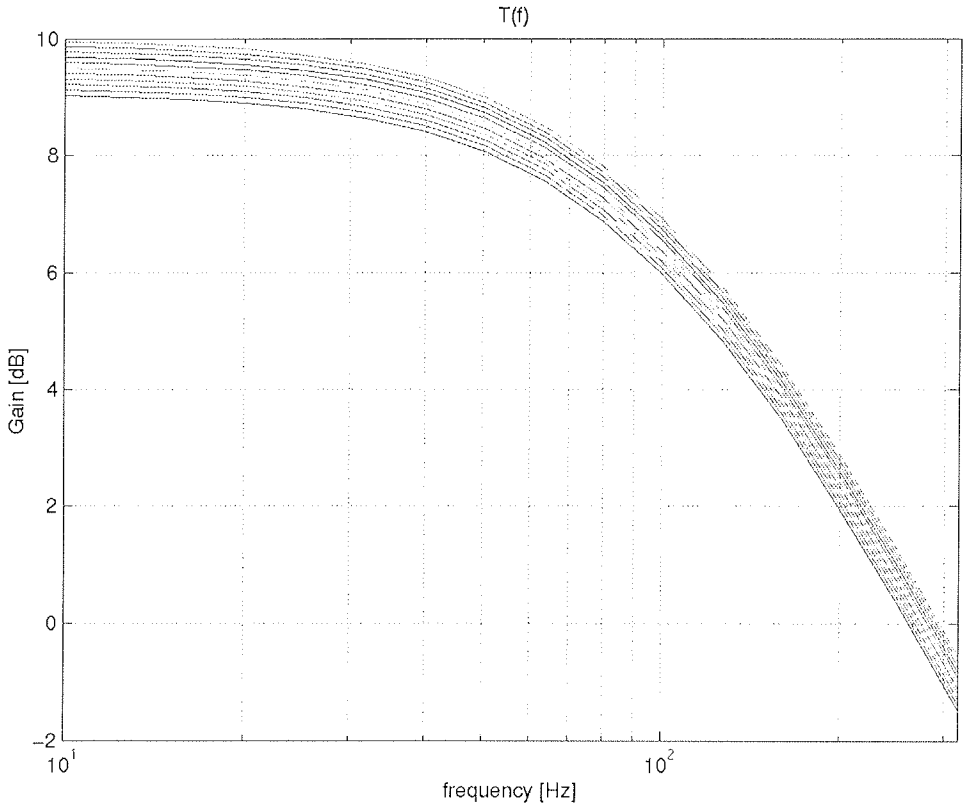

Fig. 6: The "fratout" transfer function with supply voltage VDD from 4.75V to 5.25V.

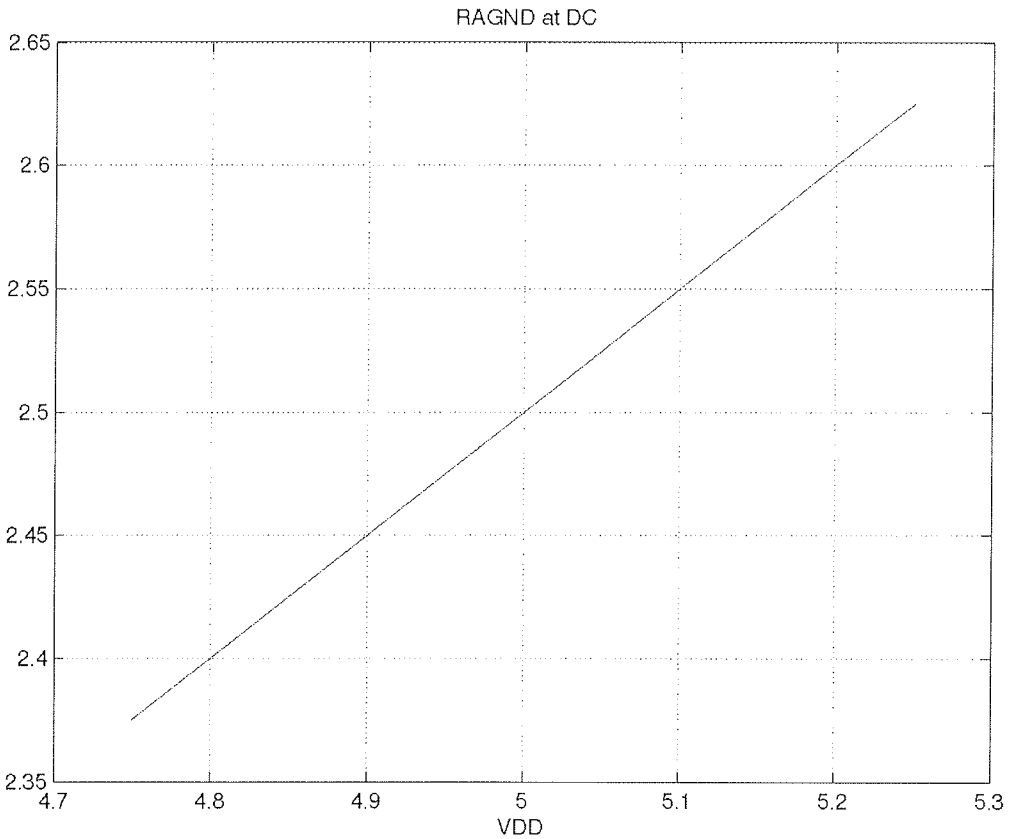

Fig. 7: RAGND variations with VDD. Transfer function is linear.

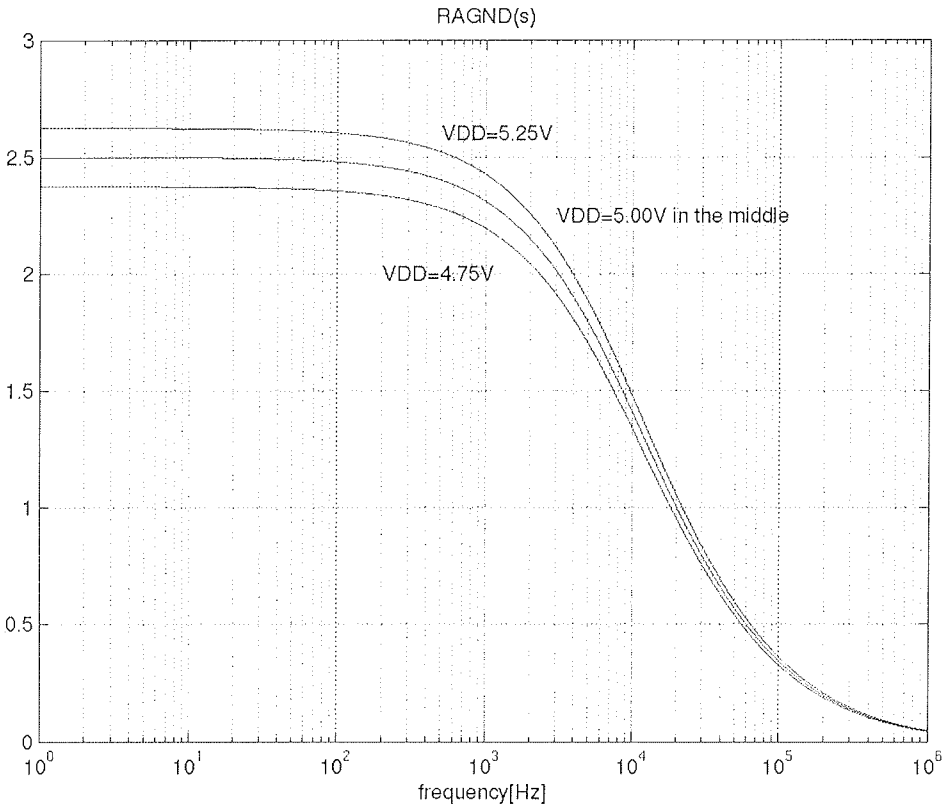

Fig. 8: RAGND frequency response (8) for minimal, nominal and maximal supply voltage.

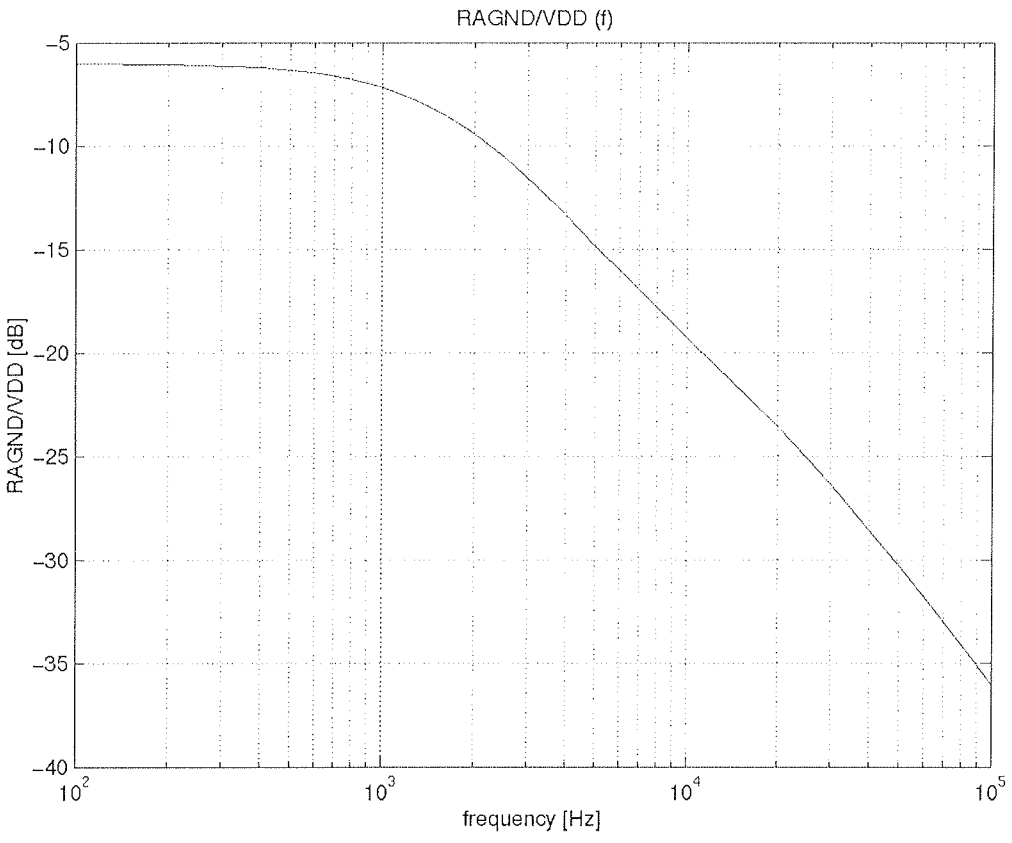

Fig. 9: RAGND/VDD transfer function.