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Computer-Aided Modeling and Simulation of Fabrication Steps in Semiconductor Processes

Računalniško podprto modeliranje in simulacija tehnoloških korakov v polprevodniški tehnologiji

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We present some problems in the modeling and simulation of the metallurgical processes in modern VLSI technologies on silicon. First, basic layers and interfaces as encountered in scaled building blocks of these circuits are presented and their technological applications are briefly described. Next, computer software and hardware implementations of relevant simulation tools are described and certain hardware platforms are evaluated, based on the CPU time for a typical process simulation, where the disk I/O is negligible. Finally, two examples are presented from simple process steps in the unipolar silicon technology.

Key words: microelectronics, process-modeling, technology CAD for silicon

V članku so predstavljeni nekateri problemi modeliranja in simulacije metalurških procesov v modernih tehnologijah VLSI na silicijevi osnovi. Najprej so na kratko predstavljene osnovne plasti in njihovi medsebojni stiki, kot jih srečamo v osnovnih, pomanjšanih gradnikih teh vezij kakor tudi njihova tehnološka uporaba. Nato so opisane računalniške strojne in programske zahteve za posamezna uporabljana simulacijska orodja. Na osnovi časov centralne procesne enote so izvrednotena nekatera tipična strojna okolja, kjer lahko zanemarimo vhodno/izhodne operacije na disku. Na koncu sta prikazana dva primera enostavnih procesnih korakov v unipolarni tehnologiji na siliciju.

Ključne besede: mikroelektronika, modeliranje procesov, računalniško podprto načrtovanje tehnologij na siliciju

1. Introduction

Modern technologies for fabricating discrete and integrated semiconductor devices involve a large number of operations which include the preparation of the base crystalline material (like Si or GaAs) as well as many other steps - like epitaxy, oxidation, ion implantation, dopant diffusion, thin film deposition - which all require dedicated equipment in order to provide the needed environment and/or high temperature.

The basic materials used in semiconductor technology include both inorganic and organic as well as crystalline and non-crystalline substances in both elemental or compound form in order to produce the semiconductor element or circuit and its package. According to this statement one can place this technology in the broad and complex field of material science or even apply the term the *micro-metallurgy* to it.

2. Basic Technologies

The building elements for complex integrated circuits (IC) are in fact very simple (and very small - the minimum feature length is less than 0.5μm) three-dimensional electronic components - like bipolar an unipolar transistors, diodes, resistors and capacitors sharing the same substrate while their interconnections provide the desired digital and/or analog system functions. In order to obtain these elements one needs the following materials and/or layers:

* the electronic-grade base material and wafer preparation
* the semiconducting p- and n-type material
* the multi-level conducting layers with diffusion barriers
* the isolation layers
* other material structures and techniques, as required by the specific technology.

These layers and their respective interfaces are depicted in **Table 1**.

The base material for modern very-large-scale-integration (VLSI) technology are wafers, cut from the already-doped ingots prepared by the Czochralski technique. The relative concentration of all unintentional impurities in EGS silicon must be typically bellow 10^{-9}. Silicon epitaxy, when applied to grow a crystalline film on a crystalline substrate, has several advantages over bulk silicon wafer. The growth rate can be limited by either the surface chemical reaction or by the transport of the reactants across the boundary layer. The electrically-active volumes of an IC must include a certain amount of n- or p-type dopants which are introduced by the means of the ion implantation or by the diffusion from different sources. The impurity distribution has an important influence on the electrical behavior of the device and

procesna plast	kontakti, povezave, difuzijske zapore	izolatorji	polprevodniki
process layer	contacts, interconnect. diffusion barries	isolators	semiconductors
photoresist	(doped) poly-Si	Si_3N_4	crystalline Si
	silicides, nitrides, carbides	(doped) SiO_2	implanted/doped Si
	Al, Al+Cu, Al+Cu+Si	Si_2N_2O	epitaxial Si
	refractory metals		

Table 1. Typical layers and interfaces in advanced silicon IC technology

Tabela 1. Značilne plasti in prehodi med njimi v napredni polprevodniški tehnologiji na siliciju

we must have ways to predict this distribution after all the process steps are performed. This prediction becomes very complex since the diffusion of dopants in silicon must be treated in parallel with the transport of the points defects in silicon[2,3]. The modeling and simulation of the initial distribution after the ion implantation is, for example much simpler even when second-order effects are taken into the consideration[4,5]. The dielectric layers have an important role in the physical structure of the IC. These layers provide the necessary electrical isolation among electrically-active volumes within the IC, they are used as dielectrics in the capacitor structures and they form the isolation layers between the conductive layers, while they are also used as required by the particular process technique (like, for example, in locally oxidized Si (LOCOS) structures). They can grow directly over the silicon - like SiO_2 or Si_3N_4 - or can be deposited in the plasma-assisted environment or by the low-pressure chemical vapor deposition (LPCVD) technique (for poly-Si and Si_3N_4). The formation process does, however, affects the chemical, physical and electrical properties of the layers as well as the distribution of the dopants in the silicon structure. In fact, the diffusion engineering can be performed by the proper choice of the layer above the silicon substrate. The conductive layers provide the necessary interconnects among basic electric elements of the cell of an IC as well as the required interconnects among the cells in order to obtain the desired characteristics of the complete IC. In order to obtain these conductive films we use the evaporation, sputtering and CVD for Al, Mo and W or codeposition (and reaction) for the silicides of Mo, Ta, Ti, W and Co. These techniques do, however, exhibit metallurgical interconnection problems associated with grain-boundary diffusion. The new epitaxial methods in forming silicide and Al layers might improve the contact metallization in ICs.

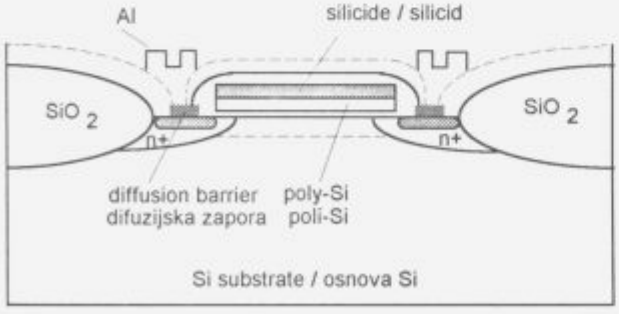

Figure 1. A schematic structure of a unipolar transistor cell

Slika 1. Struktura celice unipolarnega transistorja

Figure 1 shows a typical structure of a unipolar transistor where all metallurgicaly interesting parts are shown. In order to obtain this composition of layers and the required patterns, the photolitographic technique is applied. In the situation when the minimum feature size is comparable with the wavelength of light, a two-dimensional dedicated process simulator can be used in order to study the optical pattern transfer. Similar modeling and computer simulation must be used when the dry (plasma) etching methods are studied since the vertical and horizontal dimensions are comparable.

3. Computer Models and Implementation

The necessary equipment in semiconductor technology is in most cases very complex and expensive because it is dedicated to the volume production of electronic and optical devices. Together with the cost of the dedicated production areas - known as the clean room - the complete technology does not allow many experiments and technology development ecame very computer-oriented even in the past when the computation costs (measured in e.g. USD/MFLOPS) were much higher than at the present[6,7,8]. The second reason for using more powerful computer resources is the need to perform the simulations in two or even three spatial dimensions. Such simulations are needed because of the integration of devices which in turn become smaller and smaller and the role of the lateral dimension becomes comparable to the role of the vertical dimension in the physical structure of the complete device. The basic idea behind these requirements is the possibility of the computer-assisted integration of all software tools needed in the development cycle of a new integrated circuit. The use of such *analog work-stations*[9] (the term describes both the hardware and the software needed to design both the circuit and/or technology for both analog and/or digital ICs) is today possible and can provide the feedback in the design/development/manufacturing cycle, the view-port into micro-space and the repository for accumulated knowledge.

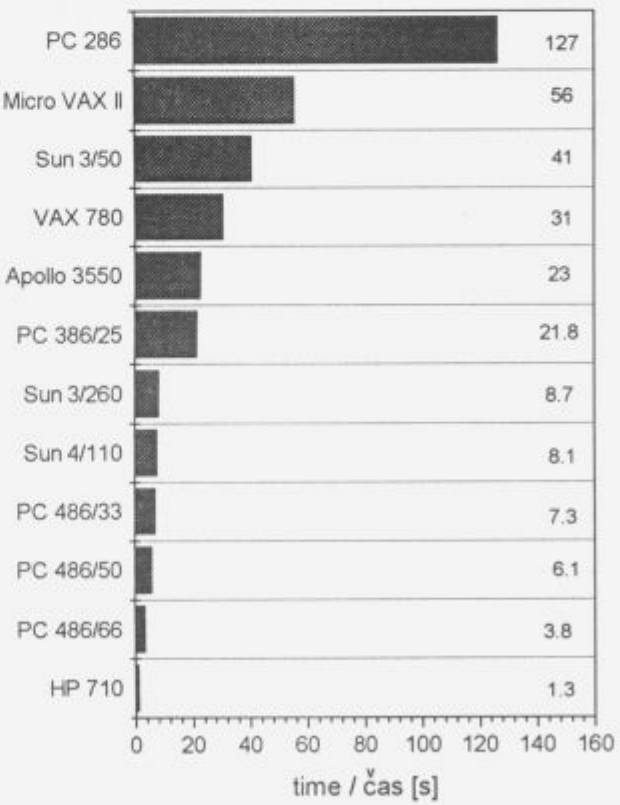

Figure 2. Relative performance of several engineering computer systems for TCAD

Slika 2. Primerjava zmogljivosti nekaterih računalniških sistemov za TCAD

These simulation programs follow the traditional approach, used in the engineering applications. With the front end, the user defines the geometry, materials, initial and boundary conditions. The core solves the relevant transport equations (for e.g. charge carriers or impurities and defects) using a numerical procedure based on finite elements or on finite differences, while the post-processor is used for data presentation and analysis. In order to transfer the data between different programs, a common format for input/output (data and/or graphic) files is used.

Finally, the models and their software implementation must be addressed from the view-point of computer hardware. The comparative results show that today most of the programs can be used on a graphic work-station (using scalar compilers and the X-Windows environment) or on a high-performance personal computer. In our laboratory we are using a high-performance work-station as a server together with high-performance personal computers on a net-work. The performance of some other computer system for TCAD (Technology Computer Aided Design) are presented in **Fig. 2** for the case of 1-dimensional process simulation. Some older computers are included only in order to illustrate the influence of the computer development in the area of the TCAD.

4. Examples

In order to illustrate the TCAD/work-station approach we examine two cases which are common in modern unipolar IC processing. **Figure 3** is a SEM photo of a single transistor cross-section where some of the important metallurgical layers, as depicted in **Figure 1**, can be observed.

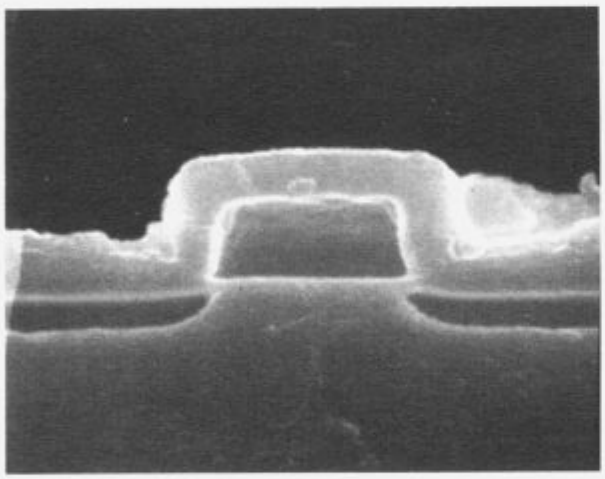

Figure 3. SEM cross-section of a unipolar transistor (the marker shows 1μm)

Slika 3. Presek SEM unipolarnega transistorja (marker: 1μm)

Although it is almost impossible to evaluate the two-dimensional impurity profile in the active volumes of the device, one can at least compare this picture with the simulated impurity profile from **Figure 4** if the metallurgical junction depth is in the question.

The surface topography of the photoresist patterns effects the transfer and the shape of the etched areas and frequently even the electrical characteristics of the integrated cell. **Figure 5** shows a SEM cross-section of a photoresist line over an oxidized poly-Si line.

The standing-wave effect is clearly evident and again simulated with a lithography simulation program, **Figure 6**.

5. Conclusions

The role of computer modeling and simulations in the semiconductor technology is very important because of small physi-

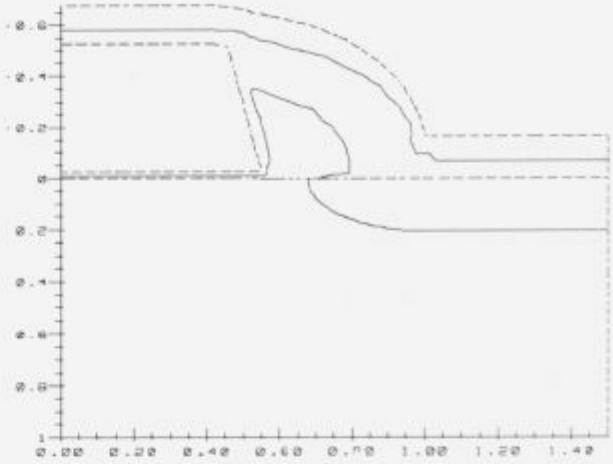

Figure 4. Simulated two-dimensional impurity profile (x- and y-dimensions in μm)

Slika 4. Simulirana dvodimenzionalna struktura (x- in y-dimenzije v μm)

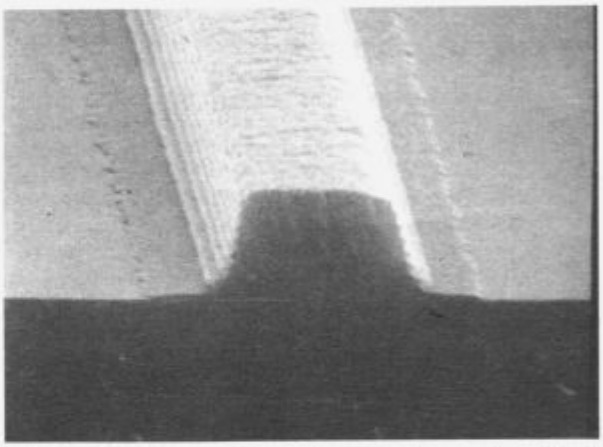

Figure 5. SEM cross-section of a photoresist line over the oxidized poly-Si after the development cycle

Slika 5. Presek SEM fotopolimerne linije na oksidiranem poli-Si

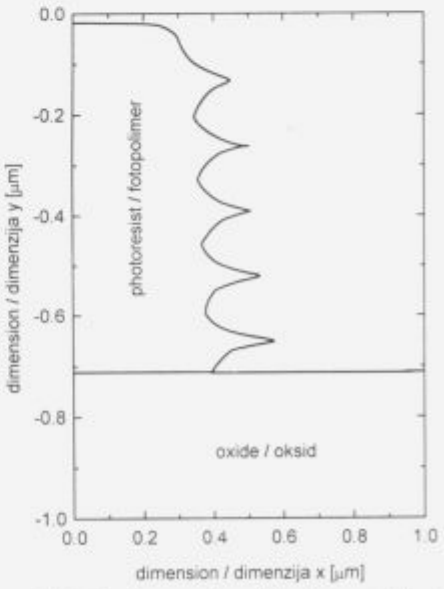

Figure 6. Simulated topography of the photoresist line after the development cycle

Slika 6. Simulirana topografija fotopolimera po razvijanju

cal dimensions and because of complex inter-related physical processes. The adequate feedback from the experiments is necessary. Modern work-station with their high computing throughput offer an excellent hardware platform for these computationally intensive simulations at least in two space dimensions. It is expected that more powerful computers are required when three space dimensions must be considered.

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