SYNTHESIS OF ANALOG INTEGRATED CIRCUITS

Andrej Vodopivec

Faculty of Electrical Engineering, University of Ljubljana, Ljubljana, Slovenia

Key words: analog circuit synthesis, analog circuit, circuit analysis, circuit optimization, topology selection

Abstract: A new approach to synthesis of analog circuits combines circuit rule based topology selection with circuit optimization. With the advent of super fast microprocessors it is possible to choose out the dimensions of devices in an analog circuit which suit best the set of requests using optimization techniques build into modern circuit simulation tools. These tools still basically only analyze a given circuit so an extra layer is needed to select a topology which suits the set of requirements. The selection can be efficiently described for any analog block using programming language OPAN.

Sinteza analognih integriranih vezij

Ključne besede: sinteza analognih integriranih vezij, analogno vezje, analiza vezja, optimizacija vezja, izbira topologije

Izvleček: Nov pristop k sintezi integriranih analognih blokov kombinira na pravilih temelječo izbiro topologije z optimizacijo vezja. Z izboljšavami hitrosti delovanja mikroprocesorjev postaja uporabna izbira dimenzij komponent analognega vezja, ki najbolje izpolnjuje dane zahteve, z uporabo optimizacijskih postopkov vgrajenih v moderna orodja za simulacijo vezij. Ta orodja v osnovi vedno samo analizirajo dano topologijo, zato je za sintezo pomembna izbira ustrezne topologije. Iziro je mogoče učinkovito opisati z jezikom OPAN.

1. Introduction

Accurate and fast circuit simulations of integrated circuits is a critical step in integrated circuit design. Traditional analog circuit simulators like SPICE /1/, RELAX /2/ were slow while new simulation technologies like SPECS /3/ traded accuracy for speed. Both were able to analyze a general analog circuit but were too slow to be used in analog integrated circuit synthesis so device sizing /6/ was used which considerably simplified analysis of specific topologies.

A set of rules /7/ was used to describe changes of properties of the circuit with new sizes of selected devices as well as to guide the selection of new device sizes to ensure requested circuit properties. Circuit modeling /8/ turned out to work fine for operational amplifiers in a tool when used by experienced analog designers. Novice designers were not able to use the synthesis tool because they tend to over-specify the design in so many 'weird' way that the set of rules became unmanageable.

With the advent of super fast microprocessors it is possible to execute hundreds or thousands of circuit analysis required by analog circuit synthesis within a few hours. Building optimization loops in SPICE /4/ turned out very efficient. A number of optimization methods /5/ enable modern implementations of SPICE to choose out optimal device dimensions for a selected set of requirements.

What is left for a synthesis tools (fig. 1) is:

- design of optimization scripts in such a way that a meaningful result is obtained no matter what properties are selected,
- selection of the appropriate topology (e.g. A class) and variation (e.g. micro power), and

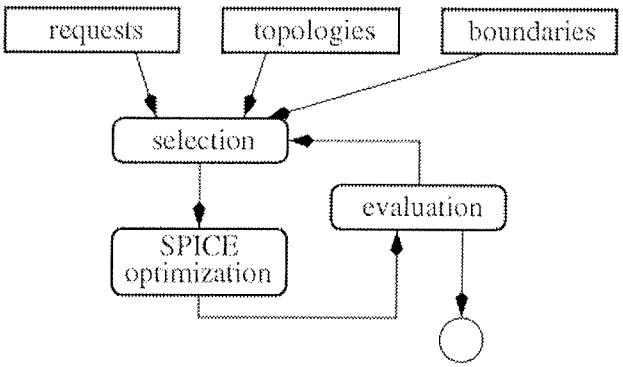

Fig.1: Synthesis of analog circuit

- automation of inter topology boundary selection depending on process parameters used to model devices of the current technology.

2. Describing topology

The topology description consists of:

- circuit netlist
- process parameters
- requested properties
- optimization loop
- corner analysis loop

The description is build modularly so parts of requests and optimization can be omitted to simplify and speed up the optimization process.

The description starts with circuit netlist and process parameters as any other SPICE input file. The netlist is a typical SPICE netlist with the exception of symbolic values

used to denote properties (sizes) of some devices. The sizes of these devices are going to be optimized while others will keep the assigned values. The process parameters are used to pass values to device models of the technology used in the design.

Passing requested properties from the user interface to the optimization script is not straightforward. Since the user is at liberty to select values for the circuit's properties and omit them as well attention must be paid to select default values for certain properties to obtain meaningful result no matter what properties are selected. Some topologies even require properties not available in the user interface to ensure operation.

Since circuit optimization using circuit simulation is a very CPU time consuming operation the optimization loop must be carefully designed. Omission of analysis required by "don't care" properties may result in substantial speed up of the optimization process.

Analysis of the optimized circuit using simulation corners is very important in evaluation of the results of the synthesis. Corner analysis should be placed inside the optimization loop but since this could easily result in prolonging the optimization time by an order of magnitude or more it is more practical to over-specify the circuit's properties a little.

3. Topology selection

Analog block (e.g. operational amplifier) can be build using a databases consisting of tens of topologies (e.g. A class) and variations (e.g. micro power, rail to tail common mode). Optimization of all available topologies for the requested set of block properties and selection of the best final candidate is still a tool CPU time consuming operation. Selection of a small set of topologies to be optimized and evaluated becomes crucial.

Expert knowledge of experienced analog designers is required to set up a good selection procedure. Hard-coding topology selection in C soon turned out to be too complicated for the analog designer so a simple programming language OPAN was used. It consists of assignment statements and control structures. The only control structures needed to describe the topology selection are if-then-else and goto. Despite long formulae the input deck is quite readable since it can be written in TEX.

$$/* \text{ rule } 16 */$$

$$A_0 = A_{0o} * \sqrt{\frac{(\frac{W}{L})_d}{(\frac{W}{L})_{d_o}}} * \sqrt{\frac{I_b}{I_{bo}}} * A_0 t;$$

When a number of topologies or variations meet selection criteria all are evaluated and the final selection is made with a cost function weighting requests and results of all optimized circuits.

4. Adjusting selection to new fab or new minimum feature size

Topology boundaries define the range of requested properties which are optimally synthesized using a given topology. These boundaries vary with the fab or new minimum feature size. Where one topology is best for the given set of request in one process (e.g. AMS 0.8μm) another may be in a different process (e.g. TSMC 0.25μm).

An attempt was made within intensive study of various topologies of operational amplifiers to find general principles which could be used in mapping topology properties from one process to another using process parameters.

As we were not able to find any expressions which could be used in mapping topology boundaries we used optimization capabilities of SPICE building topology boundary tables. A characteristic set of properties was selected for each topology. The topology is then optimized for each property of the set and the optimal values were used in definition of topology boundaries.

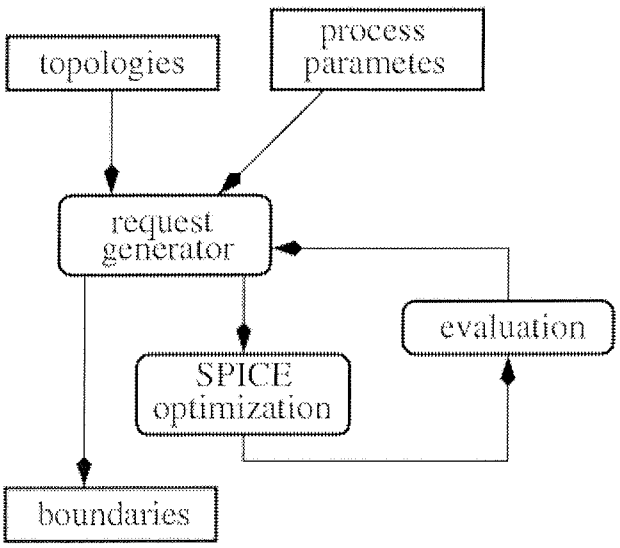

Fig. 2: Topology boundary selection

5. Conclusions

Optimization capabilities build into SPICE make analog synthesis more reliable. What is needed on top of SPICE is good topology selection. This can be accomplished using a rule based programing language OPAN. When applying analog synthesis to real world cases defining topology boundaries becomes a must. SPICE optimization can be used in building topology boundary tables. Computers are still too slow to evaluate corner cases during optimization in real time. As trade offs are always used in design the final request are usually set only when all constraints are evaluated. With this final request one can execute a multi-day corner cases optimization.

References

/1/ L. W. Nagel, "SPICE2: A Computer Program to Simulate Semiconductor Circuits", Elect. Res. Lab. Report ERL-M520, University of California, Berkeley, 1975

/2/ A. R. Newton, A. L. Sangiovanni-Vincentelli, "Relaxation-Based Electrical Simulation", IEEE Trans. Computer-Aided Design, vol. CAD-3, pp 308-330, May 1984

/3/ CC. Visweswariah, R. A. Rohrer, "Piecewise Approximation Circuit Simulation", IEEE Trans. Computer-Aided Design, vol. CAD-10, pp 565-576, May 1991

/4/ J. Puhan, T. Tuma, "Optimization of Analog Circuits with SPICE 3F4", Proc. of the European Conference on Circuit Theory and Design, Budapest, Hungary, pp 177-180, 1997.

/5/ J. Puhan, T. Tuma, I. Fajfar, "Optimization Methods in SPICE, a Comparison", Proc. of the European Conference on Circuit Theory and Design, Stresa, Italy, Vol. 2, pp 1279-1282,1999.

/6/ J. Trontelj, L. Trontelj, A. Pleteršek, A. Vodopivec, G. Shenton, "Synthesis and Layout Compilation Automation of Mixed Analog-Digital ASICs", Proc. Of the IEEE 1990 ISCS, New Orleans pp 816-819, 1990.

/7/ J. Trontelj, L. Trontelj, A. Pleteršek, A. Vodopivec, G. Shenton, "Rule Based CAD Tools for Analog Circuit Synthesis and Layout Compilation", Proc. Of the IEEE 1990 CICC, Boston, pp. 14.8.1-14.8.4, 1990.

/8/ A. Vodopivec, J. Trontelj, "Modeling for Analog Circuit Synthesis", Proc. 1993 MIEL, Bled, pp 61-64, 1993.

Andrej Vodopivec
Faculty of Electrical Engineering, University of Ljubljana, 1000 Ljubljana, Slovenia

Prispelo (Arrived): 06.06.2002 *Sprejeto (Accepted): 25.03.2003*