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APPROXIMATE ANALYTICAL MODELING OF SILICON INTERNAL INDUCTANCE OF VLSI INTERCONNECTS

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Key words: semiconductors, microelectronics, IC, Integrated Circuits, VLSI circuits, Very Large Scale of Integration circuits, interconnects, internal inductance, lossy silicon substrates, analytical modeling, approximate modeling, GREEN'S unctions, electric current, current distribution, eddy current, substrate resistivity

Abstract: In previous work, a closed form expressions for the series line impedance per unit length of a single and multiple coupled interconnects on lossy silicon substrate were presented. In this paper, the induced current density distribution inside silicon substrate and quasi-static Green's function approach were used to derive the frequency-dependent closed-form expression for the internal inductance per unit length accociated with the silicon substrate. With this expression, we can quantitatively determine what percentage of the total inductance per unit length is associated with the internal silicon substrate inductance for a given frequency. The effect of the substrate resistivity on the inductance of on-chip interconnects was examined. It was shown that depending on the frequency, large changes in the inductance can occur due to this effect.

Približno analitično modeliranje notranje induktivnosti VLSI povezav na siliciju

Ključne besede: polprevodniki, mikroelektronika, IC vezja integrirana, VLSI vezja integracije zelo visoke stopnje, povezave medsebojne, induktivnost notranja, substrati silicijevi izgubni, modeliranje analitično, modeliranje približno, GREEN funkcije, tok električni, porazdelitev toka, tok vrtinčni, upornost substrata

Izvleček: V enem od prejšnjih prispevkov smo predstavili zaključen izraz za frekvenčno odvisno vzajemno impedanco povezav na izgubni silicijevi tabletki. Tokrat s pomočjo porazdelitve inducirane tokovne gostote znotraj silicija in s pristopom, ki uporablja kvazi statične Greenove funkcije izpeljemo zaključen izraz za frekvenčno odvisno notranjo induktivnost na enoto dolžine povezano s silicijevim substratom. S pomočjo dobljenega izraza lahko kvantitativno določimo, kakšen del celotne induktivnosti na enoto dolžine odpade na silicijev substrat pri dani frekvenci. Ravno tako smo preučili vpliv substratne upornosti na induktivnost povezav na tabletki. Pokazali smo, da zaradi tega efekta lahko pride do velikih sprememb induktivnosti v odvisnosti od frekvence.

1. Introduction

As the sub-nano second transition time of a signal becomes comparable to its propagation delay on interconnection lines, the transmission line effects on the IC interconnects become extremely important. The IC interconnect transmission line parameters are inherently frequency-dependent because of the silicon substrate effect, the metal skin effect and the proximity effect in the current return paths /1/. In order to accomplish this, it is necessary to analyze and model the broad-band characteristics /2 - 5, 8 - 10/ of the silicon IC interconnects since the signals tend to exhibit both the short rising and falling times. Since the conductive silicon substrate does not act as a perfect ground plane, significant amount of return currents comes back through it. The internal inductance of the silicon semiconducting substrate is governed by the skin effect (i.e. the skin effect associated with the silicon substrate). As a results, it is known qualitatively that at very high frequencies, the total inductance is dominated by the external inductance and the internal inductance (silicon substrate) can be neglected. However, for a given frequency there has not been a way of quantitatively determining how large or small the contribution of the internal silicon inductance is compared to the total inductance of IC interconnects.

In this paper, for the first time, we introduced a closed-form expression for the internal inductance per unit length of the silicon associated with VLSI interconnects. This expression can be used to determine the internal silicon substrate inductance for any given frequency and substrate resistivity. The results presented here illustrate that the resistivity, geometry of the interconnect lines as well as the frequency play a strong role in determining the relative importance of the internal silicon inductance.

2. New closed-form expression for the internal silicon inductance

The new modeling approach is described for a microstrip line on a lossy silicon substrate with conductivity σ, as illustrated in Fig. 1. The silicon substrate and silicon oxide have the thickness h and d, respectively, and the the microstrip conductor is infinitely thin with width w.

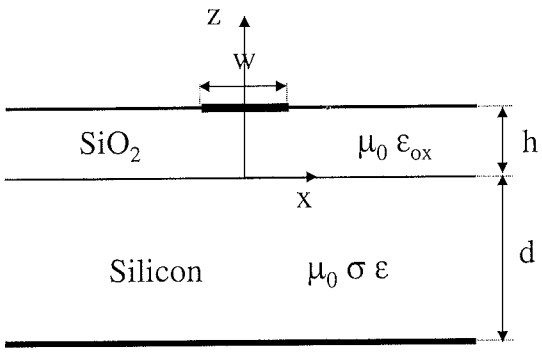

Fig. 1. Cross section of a microstrip interconnect on an oxide-semiconductor substrate.

The internal inductance of the silicon semiconducting substrate is given by

$$L_{si} = \frac{1}{I_{si}^2} \int_V \mathbf{B} \cdot \mathbf{H} dv \qquad (1)$$

where I_{si} is the total current flowing in the silicon substrate and **B** and **H** are magnetic flux density and magnetic field intensity inside the silicon substrate, respectively. For infinitely long interconnect conductor, the fields are uniform in the y direction and the problem is two-dimesional. In general, the magnetic fields inside the lossy silicon have both an x and z component. However, in /6/ it was shown that inside a highly conducting region (VLSI interconnects in CMOS technology) the tangential components of the fields (the x component in this case) dominates the normal component (the z component), and to zero-order, $H_z \approx 0$. (Little generality is lost by considering this quasi-TEM case). By utilizing this fact and assuming that the materilas are nonmagnetic, (1) reduces to

$$L_{si} = \frac{\mu_0}{I_{si}^2} \int_{-d}^{0} \int_{-\infty}^{\infty} H_x^2 dx dz. \qquad (2)$$

It was shown in /6/ that the fields exhibit an exponential decay of $e^{z/\delta}$ (where $\delta = \sqrt{2}/(\omega\mu\sigma)$ is the skin depth) away from the surface of a conducting region. Therefore, by assuming that the magnetic field inside silicon substrate is governed by this same skin depth behaviour, we get

$$H_x = H_{0x}(x) e^{z/\delta} \qquad (3)$$

where H_{0x} is the value of the magnetic field on the surface of the silicon substrate and is function of x. By using the boundary condition for the tangential component of the magnetic field, $\mathbf{a}_n \times \mathbf{H} \mid_{z=0} = J_{si}$, the H_{0x} can be approximated by

$$H_{0x}(x) = J_{si}(x) \qquad (4)$$

where $J_{si}(x)$ is the surface current density of the silicon substrate. Upon substituting (3) and (4) into (2), the z integration can be done explicitly and the expression for internal inductance become

$$L_{si} = \frac{\mu_0 \delta}{2} (1 - e^{-2d/\delta}) \int_{-\infty}^{\infty} [J_{si}(x) / I_{si}]^2 dx. \qquad (5)$$

The surface current density on a semiconducting silicon substrate was derived via a quasistatic Green's function approach /7, 9, 10/ and was shown to be

$$J_{si}(x) = (I_{si} / w\pi)[\tan^{-1}((w - 2x)/2h) + \tan^{-1}((w + 2x)/2h)] \qquad (6)$$

where w and h are defined in Fig. 1. Substituting the surface current density (6) into (5), we get

$$L_{si} = (\mu_o \delta / 2(w\pi)^2)(1 - e^{-2d/\delta}) \int_{-\infty}^{\infty} [\tan^{-1}((w - 2x)/2h) + \tan^{-1}((w + 2x)/2h)]^2 dx. \qquad (7)$$

Using the concepts of complex analysis /11/(the Cauchy Integral Theorem and proper complex contour of integration), the x integration can be evaluated in closed form (the details we leave out) and the internal inductance per unit length of the silicon substrate is given by

$$L_{si} = \frac{\mu_o \delta}{w\pi} (1 - e^{-2d/\delta}) \left\{ \tan^{-1}\left(\frac{w}{2h}\right) - \frac{h}{w} \log\left[1 + \left(\frac{w}{2h}\right)^2\right] \right\} \qquad (8)$$

3. Results and discussions

In this section, two sets of resistivities (low and high resistivity substrate) used commonly in VLSI intergated circuits are analyzed. Fig.2 illustrates the significance of the frequency dependent internal inductance of silicon for single interconnects on a heavily doped CMOS 300 mm substrate (resistivity ρ_{si} =0.01 Ωcm) with a 3 μm oxide layer. The width of zero-thickness conductor is 2 μm. Fig. 2a shows the results of the total inductance ($L_t = L_{ex}+L_{si}$), the external inductance L_{ex}, and the internal silicon substrate

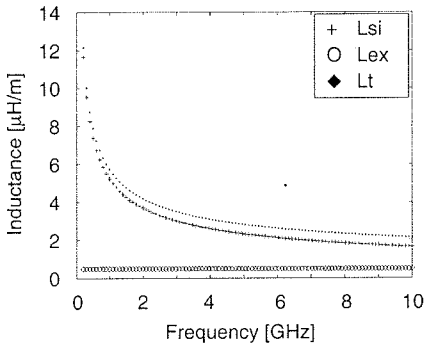

Fig. 2. (a) Total, external, and internal silicon substrate inductance for single interconnects used in silicon-based IC circuits,

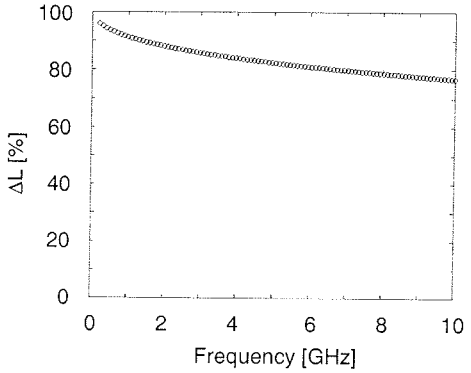

Fig. 2. *(b) The percent of internal silicon substrate inductance compared to total inductance for single interconnects.*

inductance L_{si}. (For computation of total and external inductances of on-chip interconnects we used the proposed methodology in /9, 10/) The external inductance is very small compared to the internal inductance of silicon substrate at low frequencies, but at very high frequencies the differences becomes smaller. This is further illustrated in Fig. 2b, where the percent ΔL of silicon substrate inductance compared to the total inductance L_t is plotted as a function of frequency. For low, medium and high frequencies up to 20GHz internal inductance of silicon substrate have a strong effect on the propagation properties of IC interconnects.

For the case of a microstrip interconnect on a 500-μm high resistivity silicon substrate (resistivity ρ_{si} = 10 Ω-cm) with a 2-μm oxide layer, the internal inductance of silicon as a function of frequency is shown in Fig. 3. The width of microstrip is 4μm. For high resistivity silicon substrate, the total, external and internal silicon inductances becomes frequency-independent (see Fig. 3) and the variation of the magnetic flux penetration into silicon substrate becomes frequency-independent, too. The internal inductance of silicon is comparable to the external inductance, as illustrated Fig. 3. The numerical results presented in this chapter show that the influence of the resistivity of the semiconducting substrate on the frequency-dependent and

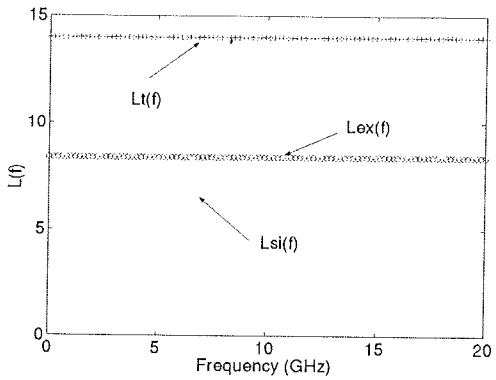

Fig. 3. *Frequency dependence of total, external and internal silicon inductances as a function of frequency for high resistivity silicon substrate.*

transient behaviour of on-chip interconnects is significant and can not be neglected.

4. Conclusion

In this paper, we introduced a closed-form expression for the frequency-dependent internal inductance of silicon of on-chip interconnects. We have investigated the sensitivity of the frequency-dependent inductance per unit length of microstrip interconnect to the substrate resistivity. The results presented here illustrate that the resistivity of the silicon as well as frequency play strong role in determining the relative importance of the silicon substrate inductance (substrate skin effect).

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NAČRTOVANJE NOVIH SREDNJENAPETOSTNIH INDIKATORJEV NAPETOSTI S POMOČJO IZRAČUNA ELEKTRIČNEGA POLJA

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Ključne besede: EES sistem elektroenergetski, napetost električna, napetost srednja, napetost električna 125 kV, naprave stikalne, indikatorji napetosti, enote elektronske, delilniki napetosti kapacitivni, polja električna, izračuni, izolatorji podporni, IEC 61985 standardi, IEC 61243-5 standardi

Izvleček: Indikatorji napetosti se uporabljajo za indikacijo prisotnosti napetosti. Sestavljajo jih običajno trije epoksidni podporni izolatorji, v katere so vgrajeni kapacitivni delilci visoke napetosti in indikatorska elektronska enota. Izolatorji so vgrajeni v stikalnem aparatu ali drugem dovodnem elementu na katerem je prisotna napetost.

Novi IEC standardi so, za indikatorje napetosti, ki v popolnosti zagotavljajo breznapetostno stanje, definirali potrebno kapacitivnost delilca napetosti, ki je nekajkrat večja kot pri dosedanjih izvedbah. To se lahko doseže le s povečanjem površine elektrod kapacitivnega delilca, s tem pa močno naraste električna poljska jakost znotraj in ob izolatorju. S pomočjo izračuna električnega polja so bile izbrane elektrode indikatorjev napetosti, ki zadovoljujejo opisanim zahtevam in sočasno omogočajo najugodnejšo porazdelitev električne poljske jakosti.

Optimizirana je bila modificirana izvedba sedanjega indikatorja napetosti, zasnovana pa je bila tudi nova izvedba.

Izračuni električne poljske jakosti so bili potrjeni na prototipih podpornih izolatorjev.

Design of New Medium Voltage Indicator by Means of Electric Field Calculation

Key words: electrical power system, electrical voltage, medium voltage, electrical voltage 125 kV, switchgears, voltage indicators, electronic units, capacitive voltage dividers, electric fields, calculations, supporting insulators, IEC 61985 standards, IEC 61243-5 standards

Abstract: Voltage indicators are used in medium voltage switchgears for indication of voltage presence. They consist of three epoxy insulators with a capacitive voltage dividers, indicator electronic unit, the input of which is connected to the divider's output, LE diode for indication of the presence of voltage and push-button for checking the correctness of indicator's operation.

For the voltage indicators that entirely ensure conditions without voltage (shielded invisible parts), the new IEC standards define necessary capacitance, which is much higher than in previously made indicators. This is necessary due to the fact, that for a reliable operation of the voltage indicator to have sufficient electric current. The terminals of voltage indicators that fulfil the above described requirements have been selected on the basis of electric field calculations. These calculations have also been used for achieving the most suitable electric field strength distribution. The old version of voltage indicator has been optimised and modified. The concept of a new version has also been developed.

For solving 3D electromagnetic problems using finite element method the program package Electromagnetic Field Analysis Tools (EleFAnT3D) has been used. 3D graphical pre-processor enables inputting of 3D structures, boundary conditions, sources and data on materials used. Data input phase is followed by running the computations and presentation of results in graphical and numerical form.

The results of electric field calculations and optimisation have shown that for the existing layout of supporting insulator's electrodes (Figure 16) the strongest electric field is in the upper part (Figure 12) and oriented towards the outside of insulator (Figure 13). In this part there is also the connection and in the case of voltage increase there is a possibility of a flashover.

In the newly designed concept of supporting insulator's electrodes (Figure 17) the strongest electric field is in the bottom part (Figure 14), where it almost reaches the dielectric strength of air. Nevertheless, this distribution is more suitable since the electric field is oriented towards the inside of the insulator (Figure 15) - dielectric strength of epoxy is ten times higher than the dielectric strength of air.

The calculations of electric field have been verified with measurements on the prototype of the insulators.

1. Uvod

Izolatorji iz epoksidnih smol imajo zelo dobre izolacijske, mehanske in termične lastnosti, ter veliko odpornost na različne kemikalije. Odlikujejo se tudi po malih dimenzijah, zahtevnih oblikah in dolgi življenjski dobi.

V stikalnih napravah so uporabljeni kot izolacijski (električno izoliranje prevodnih delov od ozemljenih) in konstrukcijski (mehansko pritrjevanje elementov stikalnega aparata ali vodnikov) elementi.

Podporne izolatorje uporabljamo tudi za indikacijo napetosti v srednjenapetostnih stikalnih napravah. Pri tem imamo vedno vidno informacijo o prisotni napetosti, kar nam omogoča:

- povečano varnost posluževalcev,
- preprečitev napačne manipulacije in
- povečano zanesljivost delovanja električnih postrojev.

Elektrode indikatorjev napetosti se za srednjenapetostne notranjemontažne naprave običajno vgradijo v podporne izolatorje na stikalnem aparatu ali drugem dovodnem elementu na katerem je prisotna napetost.

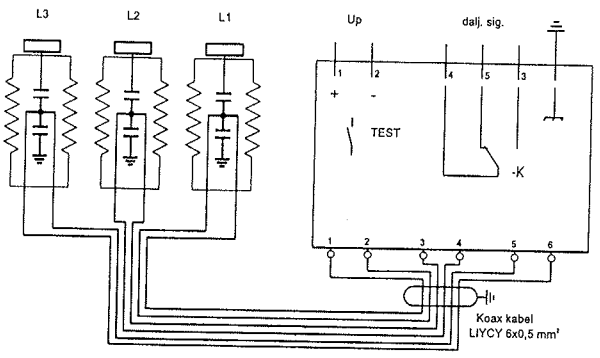
Dosedanji podporni izolatorji z vgrajenimi kapacitivnimi delilci so zgrajeni tako, da imajo majhno kapacitivnost. Do

sedaj ni bilo nobenih omejitev. Nov standard IEC 61985 v osnovni opredelitvi zahteva, da je stikalna naprava zagotovo v breznapetostnem stanju, opredeljenim z indikatorjem napetosti le, če je izdelana v skladu z IEC 61243-5, ki podaja vrednosti zahtevane kapacitivnosti. Proizvajalec mora to posebej navesti. Po zahtevi standarda morajo biti dosežene kapacitivnosti med 74 in 88 pF. Zato je potrebno vse dosedanje delilce napetosti v podpornih izolatorjih konstruirati tako, da so izpolnjene zahteve standarda. To smo izvedli tako, da smo s pomočjo izračuna električnega polja optimizirali elektrode kapacitivnega delilca napetosti, medtem ko ostane zunanjost izolatorja nespremenjena.

2. Indikatorji napetosti

Trifazni indikatorji napetosti zaslonjenih delov pod napetostjo se uporabljajo v srednjenapetostnih stikalnih napravah v katerih so elementi pod napetostjo zakriti s pregradami tako, da jih ni mogoče videti pri normalnem delovanju. To je v vseh kovinsko oklopljenih in kovinsko ali izolacijsko pregrajenih stikalnih celicah in drugih električnih napravah.

V srednjenapetostnih stikalnih celicah indikator sestavljajo trije epoksidni podporni izolatorji standardne oblike, v katerih so vgrajeni kapacitivni delilci visoke napetosti in indikatorska elektronska enota v ohišju (slika 1). Le-ta ima obliko standardnega merilnega instrumenta za vgradnjo. Na čelni plošči enote so svetlobne diode, ki z utripanjem kažejo prisotno napetost vsake faze posebej. Na njej je tudi tipka za testiranje neprekinjenosti povezav indikatorske enote s kapacitivnimi delilci v podpornih izolatorjih in pravilnega delovanja same enote.



Slika 1: Shematski prikaz indikatorja napetosti

V indikatorski elektronski enoti je vgrajen tudi pomožni rele s preklopnim kontaktom, ki služi za daljinsko signalizacijo prisotnosti visoke napetosti. Ko pride do ugasnitve oziroma utripanja diod, rele s časovno zakasnitvijo preklopi, tudi pri testiranju indikatorja, če le-to traja dalj časa. Da se izognemo vplivu visokofrekvenčnih motenj iz pomožnega napetostnega izvora, je izvedeno napajanje indikatorja z, v njegovi enoti vgrajenim, DC/DC pretvornikom. Za preprečevanje motilnih vplivov drugih visokonapetostnih in visokofrekvenčnih polj je potrebno povezati indikatorsko elektronsko enoto s podpornimi izolatorji (delilci napetosti) z oklopljenim vodnikom. Njegova dolžina ne sme biti prevelika, da ne bi prišlo do prevelikega slabljenja koristnega signala.

Druge vrste indikatorjev visoke napetosti so enofazni vtični indikatorji, ki se uporabljajo v kombinaciji s kapacitivnim delilcem napetosti v srednjenapetostnih stikalnih napravah. Ne potrebujejo pomožnega napajanja, so enostavnejši in zato cenejši. Za izvor svetlobe je uporabljena tlivka. V stikalno celico je potrebno vgraditi le ustrezne podporne izolatorje z vgrajenimi kapacitivnimi delilci in namestiti na vrata nizkonapetostne krmilne omarice tri enofazne vtičnice ter jih s koaksialnim kablom medsebojno povezati. Vtičnice so v normalnem obratovanju kratko spojene s kratkostičniki. Pri ugotavljanju prisotne napetosti je potrebno kratkostičnike izvleči iz vtičnic in na njihovo mesto vtakniti indikator.

3. Izračun elektromagnetnega polja

Elektromagnetno polje opišemo z osnovnimi Maxwellovimi enačbami:

$$\begin{aligned} \nabla \times \mathbf{H} &= \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \\ \nabla \times \mathbf{E} &= -\frac{\partial \mathbf{B}}{\partial t} \\ \nabla \cdot \mathbf{B} &= 0 \\ \nabla \cdot \mathbf{D} &= \rho \ , \end{aligned} \qquad (1)$$

kjer pomeni:
H - vektor magnetne poljske jakosti,
J - vektor gostote električnega toka,
D -vektor gostote električnega pretoka,
B - vektor gostote magnetega pretoka,
E - vektor električne poljske jakosti,
ρ - prostorninska gostota naboja.

V poljubnem prostorskem področju Ω, ki ga omejuje rob Γ (slika 2) opisujejo stacionarno električno polje naslednje enačbe:

$$\begin{aligned} \mathbf{D} &= \varepsilon\, \mathbf{E} \\ \nabla \cdot \mathbf{D} &= \rho \\ \nabla \times \mathbf{E} &= \mathbf{0} \end{aligned} \qquad (2)$$

Na robnih ploskvah lahko uporabimo Dirichletove (Γ_1), ali Neumannove (Γ_2) robne pogoje, odvisno od reševalnega primera:

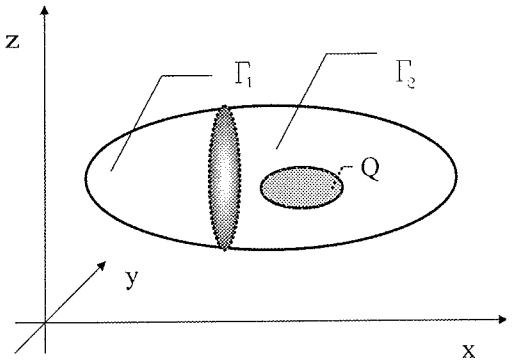
- na delu roba Γ_1, ki omejuje območje Ω velja za tangencialno komponento *E*:

$$\mathbf{E} \times \mathbf{n} = 0 \qquad (3)$$

- na robu Γ_2, območja Ω pa velja za normalno komponento gostote električnega pretoka:

$$\mathbf{D} \cdot \mathbf{n} = 0 \ . \qquad (4)$$

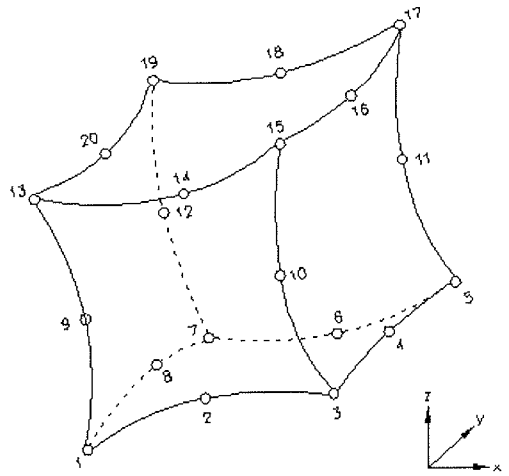
Območje Q predstavlja področje električnih izvorov.



Slika 2: Opazovano področje z danimi izvori in robnimi vrednostmi

Tako postavljeni problem rešujemo z metodo končnih elementov (MKE). V praksi uporabljamo za reševanje tridimenzionalnih problemov tetrahedralne in heksahedralne elemente. V našem primeru smo za predstavitev 3D geometrije modela uporabili končne elemente drugega reda, z dvajsetimi vozlišči. Ti elementi omogočajo tudi modeliranje ukrivljenih struktur.

Slika 3 predstavlja tak element z oštevilčenimi vozlišči.



Slika 3: 20-vozliščni heksaedralni element v globalnem koordinatnem sistemu

4. Optimiranje elektrod kapacitivnega delilca napetosti s pomočjo izračuna električnega polja

Elektrode kapacitivnega delilca, nameščene znotraj podpornega izolatorja, običajno tvorijo kovinski vložki za pritrjevanje na obeh straneh izolatorja in cilindrična elektroda, izdelana iz kovinske mrežice ali pločevine. Kovinski vložki lahko imajo tudi privarjene elektrode posebnih oblik.

Konkretni primer smo računsko reševali s programskim paketom **Ele**ctromagnetic **F**ield **An**alysis **T**ools, ki so ga razvili na IGTE, TU Graz (EleFAnT3D). Program je namenjen reševanju tridimenzionalnih problemov elektromagnetnega polja z uporabo metode končnih elementov.

Program omogoča reševanje:

- *stacionarnih* (elektrostatična, tokovna, magnetna polja) in
- *časovno odvisnih* (vrtinčni tokovi, toplotna polja) elektromagnetnih in toplotnih polj.

3D grafični predprocesor omogoča vnos vrste in geometrije problema, robnih pogojev, materialov in izvorov.

Glavni program - t.i. *solver* omogoča različne matematično-numerične možnosti izračuna (skalarni potencial, vektorski potencial, T-Ω...), odvisno od vrste in oblike problema. Tako lahko iščemo rešitve v posameznih vozliščih končnih elementov ali pa po robovih, kjer uporabljamo robovne elemente, kot posebni primer Whitney-evih elementov. Zadnje pride posebej v poštev pri reševanju problemov magnetnega polja.

Postprocesor omogoča tako numerični kot 3D grafični prikaz skalarnih in vektorskih veličin reševanega problema v celoti ali delno. Dodatno postporocesiranje v konkretnem primeru omogoča izračun volumskega integrala danega problema in s tem velikost nakopičene energije v izbranem materialu. Na osnovi le-te lahko izračunamo kapacitivnost, ki jo v našem primeru iščemo, s pomočjo enačb:

$$C = \frac{Q}{U} \tag{5}$$

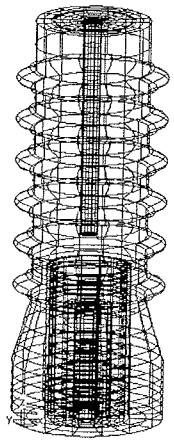
$$C = \frac{2W}{U^2} \tag{6}$$

pri čemer pomeni:
C - kapacitivnost,
Q - el. naboj,
U - napetost,
W - električna energija.

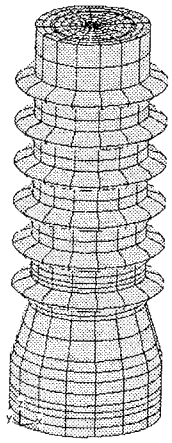
5. Prikaz rezultatov

Vsi izračuni električnega polja so narejeni pri preskusni napetosti 125 kV. Na slikah, ki prikazujejo električno polje, je velikost tega označena na desni strani. Povsod kjer je polje večje od te vrednosti je izolacijski material bele barve.

Zgornja meja polja, ki je še dovoljena, da ne pride do preboja ali preskoka se imenuje prebojna ali preskočna trdnost. Prebojna trdnost epoksidne izolacije znaša 30 MV/m in ni bila nikjer presežena. Največje vrednosti polja v epoksidni izolaciji so se pojavljale med elektrodo povezano s kovinskim vložkom in mrežico. Vzrok je relativno majhna razdalja med tema dvema elementoma in velika potencialna razlika. Problemi so se pojavili tudi na prehodu polja iz epoksidne izolacije v zrak (prebojna trdnost zraka je 3 MV/m) zaradi velike vrednosti električne poljske jakosti na koncu mrežice.



Slika 4: *Struktura kon. elem. podpornega izolatorja*



Slika 5. *Struktura z mrežo in vidnimi materiali*

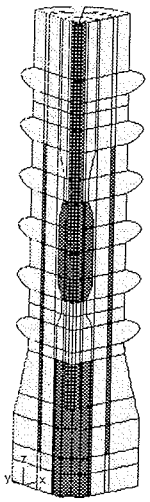
Na sliki 4 je prikazana struktura končnih elementov na sliki 5 pa struktura z mrežo in vidnimi materiali podpornega izolatorja. Zaradi osne simetrije izolatorja, boljšega pregleda rezultatov in enostavnosti izračuna, bodo v nadaljevanju vsi izračuni električnega polja opravljeni za 1/4 podpornega izolatorja.

Optimizacija z izračuni električnega polja bo prikazana za dva tipa podpornih izolatorjev in sicer:

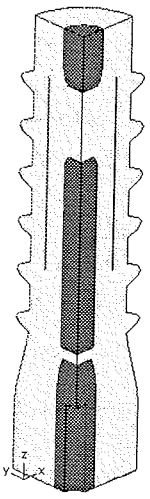
- modificirana izvedba sedanjih elektrod in
- nova izvedba elektrod.

Na sliki 6 je prikazan sedanji 24 kV podporni izolator za indikacijo visoke napetosti. Zgornja elektroda (in hkrati priključek) je na potencialu 125 kV, mrežica pa na potencialu 0 V.

Slika 7 prikazuje novo konstruiran podporni izolator, ki ima elektrodo na potencialu 0 V, medtem ko je na mrežici in zgornjem priključku potencial 125 kV



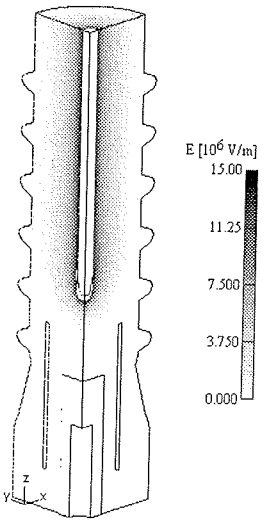
Slika 6: *Modificirana strukt. sedanjega izolatorja*



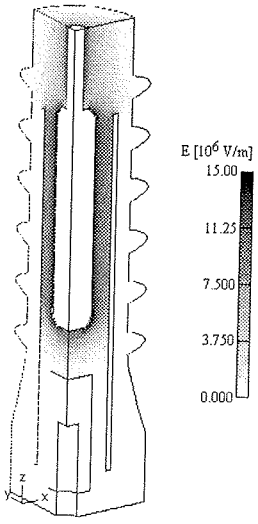
Slika 7: *Izvedba novih elektrod izolatorja*

Podporni izolatorji z elektrodami dosedanje izvedbe

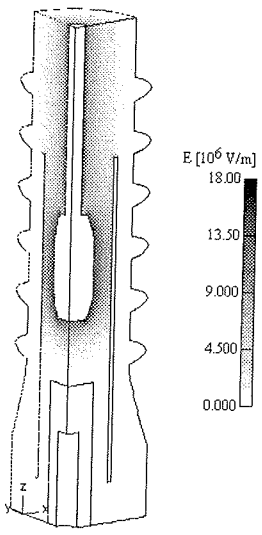
Na sliki 8 je prikazana električna poljska jakost podpornih izolatorjev z dosedanjo izvedbo elektrod. Vidimo, da v epoksidni izolaciji ni presežena prebojna trdnost 30 MV/m, kakor tudi ne v zraku 3 MV/m. Problem je kapacitivnost, ki znaša za to obliko 12 pF, po IEC 61243-5 pa se zahteva od 74 do 88 pF. Zato bo v nadaljevanju sledil prvi primer optimizacije tega podpornega izolatorja; mrežica se dvakrat podaljša, zgornja elektroda pa se odebeli na dvakratno vrednost po skoraj celotni dolžini. Vrednost električne poljske jakosti je prikazana na sliki 9. V epoksidni izolaciji vrednosti ne presegajo 20 MV/m, v zraku pa ni polje večje kot 1.5 MV/m. Vrednost kapacitivnosti še vedno ni v zahtevanih mejah.



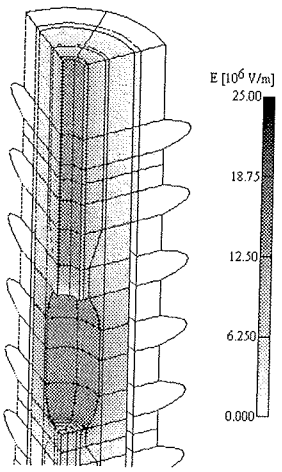
Slika 8: *Električna poljska jakost sedanjega podpornega izolatorja*



Slika 9: *Električna poljska jakost podpornega izolatorja z odebeljeno elektrodo*



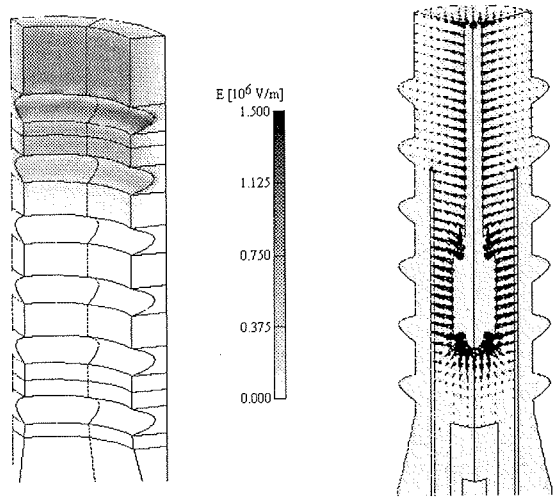
Slika 10: *Električna poljska jakost izolatorja, ki odgovarja zahtevam IEC*



Slika 11: *Prikaz električne poljske jakosti brez kovinskih materialov*

Naslednji korak optimizacije je bil skrajšanje odebeljenega konca elektrode samo na spodnji del in 20 odstotno povečanje premera. Kapacitivnost se je povečala na 83 pF, kar je dovolj glede na zahteve IEC. Električno poljsko jakost celotnega podpornega izolatorja prikazuje slika 10, na sliki 11 pa je prikazano polje v notranjosti epoksidne izolacije (brez kovinskih materialov). Vrednosti električne poljske jakosti niso nikjer presegle prebojnih trdnosti.

Tudi v 1 cm debeli plasti zraka okoli podpornega izolatorja (slika 12) električna poljska jakost ne presega prebojnih trdnosti. Na sliki 13 pa je vektorski prikaz električne poljske jakosti



Slika 12: Električna poljska jakost v zraku okoli zgornjega dela izolatorja

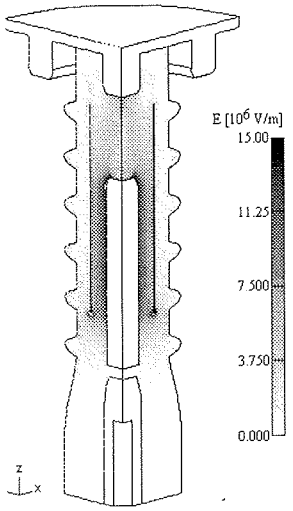
Slika 13: Vektorski prikaz električne poljske jakosti

Podporni izolatorji z novo izvedbo elektrod

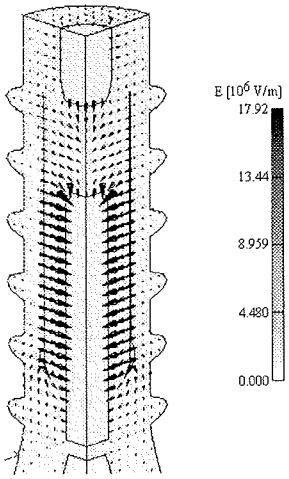
Iz izračunov polja v dosedanjih primerih vidimo, da je zunanjost izolatorja zgoraj bolj obremenjena (večji E). Čeprav električna poljska jakost nikjer ne presega prebojne trdnosti, se pojavljajo največje vrednosti polja na vrhu mrežice. Dodatno se še lahko pojavijo problemi s prebojno trdnostjo, ker je na zgornji strani tudi priključek in bi prišlo še prej do preboja. Zato bi bilo za obratovanje ugodneje, če bi se večja vrednost električne poljske jakosti prenesla v spodnji del izolatorja.

V nadaljevanju je prikazan podporni izolator z novo razporeditvijo elektrod, ki bo imel zgornji priključek in mrežico na potencialu 125 kV, posebej oblikovano elektrodo in spodnji priključek pa na 0 V.

Optimizacijo smo izvajali na podoben način kot v prvem primeru. Spremenljivke so bile dolžina in premer mrežice ter premer in dolžina srednje elektrode. V najugodnejšem primeru smo dosegli kapacitivnost 82 pF, kar odgovarja standardu IEC. Prikaz električne poljske jakosti za ta optimalni primer prikazujeta sliki 14 in 15. Slika 14 prikazuje električno poljsko jakost podpornega izolatorja, ko smo na zgornjem delu dodali priključek (približek dejanskemu stanju). Vidimo, da priključek (na potencialu 125 kV) ugodno vpliva na razporeditev električne poljske jakosti zunaj izolatorja. Prebojna trdnost je na spodnjem delu mrežice na prehodu v zrak na mejni vrednosti 3 MV/m in ni bila presežena

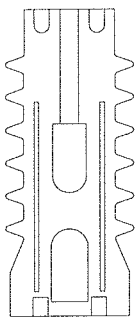


Slika 14: Električna poljska jakost v zgornjem delu podpornega izolatorja

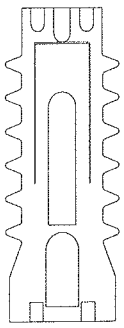


Slika 15: Vektorski prikaz električne poljske jakosti izolatorja z novimi elektr.

Sliki 16 in 17 prikazujeta načrt podpornega izolatorja v prerezu po optimizaciji. Na sliki 16 je modificirana oblika elektrod dosedanjega indikatorja napetosti (podpornega izolatorja), ki odgovarja zahtevam standarda IEC. Slika 17 pa prikazuje primer razporeditve elektrod novo zasnovanega indikatorja napetosti v skladu s standardom IEC.



Slika 16: Optimizirana oblika 24 kV izolatorja z modif. sedanjimi elektrodami



Slika 17: Optimizirana oblika 24 kV izolatorja z novimi elektrodami

6. Sklep

Iz poteka optimiziranja obeh tipov podpornih izolatorjev vidimo, da se je dolžina mrežice povečala, prav tako pa se je povečala debelina zgornje elektrode. S tem so se zmanjšale razdalje med posameznimi elementi, povečala pa se je vrednost električne poljske jakosti. Vendar so izračuni električnega polja pokazali, da električna poljska jakost ni nikjer presegla prebojnih trdnosti in sicer za epoksidno izolacijo 30 MV/m in za zrak 3 MV/m.

Rezultati izračuna električnega polja in optimiranja so pokazali, da je pri sedanji razporeditvi elektrod podpornega izolatorja (slika 16) polje največje v zgornjem delu izolatorja (na koncu mrežice - slika 12 in je usmerjeno navzven (slika 13). Poleg tega je na tem delu tudi priključek in bi pri povečani napetosti lahko prišlo do preboja.

Na podpornem izolatorju z novo zasnovanimi elektrodami (slika 17) je polje največje v spodnjem delu izolatorja (konec mrežice - slika 14) in je na meji prebojne trdnosti. Vendar je ta razporeditev ugodnejša, ker je polje usmerjeno navznoter (slika 15) - prebojna trdnost epoksida je desetkrat večja od prebojne trdnosti zraka.

Po opravljenih izračunih so bili v tovarni TSN Maribor izdelani prototipi podpornih izolatorjev z elektrodami kapacitivnih delilcev. Posamezni izolatorji so bili že testirani, potrebno pa je opraviti še preskuse znotraj stikalne celice.

7. Zahvala

Avtorji se zahvaljujemo TSN Tovarni stikalnih naprav Maribor za sodelovanje pri nalogi in za izdelavo prototipov epoksidnih izolatorjev.

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TESTING OF LEAD-FREE SOLDER PASTES FOR COMPONENT SOLDERING ON PRINTED AND HYBRID CIRCUITS

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Key words: electronics industry, printed circuits, hybrid circuits, electronic components, soldering, lead-free solder pastes, wettability, viscosity, solder balls, soldering flux residues, soldering technologies, testings, functional reliability

Abstract: The basic properties of the investigated lead-free solder pastes such, as viscosity, solder ball, wetting, were tested in laboratories for printed-circuit and hybrid-circuit technology development.The influence of flux residues on the reliable functioning of electronic circuits was tested by measuring the ionic contents in the solder pastes and by copper corrosion tests after humidity conditioning.

On the basis of the results from incoming tests on new, lead-free solder pastes the most suitable solder paste for component soldering on printed and hybrid circuits was selected for reliability testing in a humidity chamber.

Preizkusi pastoznih spajk brez svinca za spajkanje elektronskih komponent na tiskana in hibridna vezja

Ključne besede: industrija elektronike, vezja tiskana, vezja hibridna, deli sestavni elektronski, spajkanje, spajke pastozne brez svinca, omočljivost, viskoznost, kroglice spajk, ostanki fluksov spajkalnih, tehnologije spajkanja, preskušanja, zanesljivost delovanja

Izvleček: V laboratoriju za razvoj tiskanih in debeloplastnih hibridnih vezij smo izmerili osnovne lastnosti pastoznih spajk brez svinca. Opazovali smo pojav kroglic po pretaljevanju, omočljivost in izmerili viskoznost pastoznih spajk. Vpliv ostankov fluksa na zanesljivost delovanja elektronskih vezij smo ugotavljali z meritvijo vsebine ionskih ostankov v pastozni spajki in s pregledom pojave korozije na bakreni ploščici po staranju v vlagi. Na temelju rezultatov preizkusov, smo izbrali primerne pastozne spajke brez svinca za nadaljnje meritve zanesljivosti elektronskih vezij s pritrjenimi komponentami po staranju v vlažni komori.

1. Introduction

The worldwide electronics industry is faced with a ban on the use of lead, which is planned to come into force in January 2007. A number of lead-free alloys are currently being offered as replacements for use in hand soldering (solder wires), wave soldering (bars) and reflow soldering (solder pastes). Most of these alloys are based on a high tin content with the addition of various other elements (silver, copper, indium, bismuth antimony), which lead to higher melting temperatures than standard solder materials that contain lead. /1/, /2/

Some of these alloys offer advantages over conventional tin-lead solders, such as higher joint strengths, better fatigue resistance, improved high-temperature life times and harder solder joints. However, not all of these benefits are found with all the various lead-free alloys. Although many of the lead-free alloys have demonstrated more-than-adequate reliability, it is still necessary to carefully evaluate new solder pastes. /3/ In this paper we present the results of incoming tests on new, lead-free solder pastes for soldering miniature electronic components on hybrid and printed circuits. The solder pastes of various producers were compared after solder-ball, wetting, and copper corrosion tests and ionic content measurements in flux residues after reflow soldering. Also, viscosity measurements on fresh samples and on stored samples were compared for all the solder pastes tested. On the basis of the test results the best solder pastes were selected for a reliability test: a surface insulation resistance (SIR) test; and a test of the shear strength of the soldered joint between the component and the substrate before and after temperature cycling.

2. Experimental and results

2.1 Soldering paste tested

The main characteristics of the lead-free soldering pastes produced by Ecorel, Alpha Metals, Heraeus , Microbond, Multicore and Interflux, are presented in Table 1.

All the tested solder pastes are prepared for fine-pitch printing (small grain sizes) with no-clean fluxes.

The viscosities of the as-received solder pastes were measured, and the test samples for the ionic content measurement were printed with a 150 µm-thick stainless-steel stencil. During printing the samples were handled with gloves.

For the solder-ball testing, the wetting test and the copper corrosion test the samples were printed manually.

Solder paste	E808.3	OM 310	F817	NCD 8010-9	CR39	IF 9002 JAC
Alloy	Sn96 Ag4	Sn95.5 Ag 4 Cu0.5	Sn95.5 Ag4 Cu0.5	Sn95.2 Ag2.5Cu 0.8Sb0.5	Sn96.5 Ag3.5 Cu0.5	Sn95.5 Ag3.8 Cu0.7
Metal content [%]	-	89	89	-	-	88
Powder type	-	3	3	3	3	3
Powder size [µm]	-	25-45	325/500 mesh	325/500 mesh	325/500 mesh	25-45
Density [g/cm^3]	-	4.4	4.7	-	-	4.3
Melting temp. [°C]	221	217	217-219	219	219	217
Peak of reflow temp. [°C]	240-250	235-240	232-245	232-240	232-245	232-245

Table 1: The main characteristics of lead-free soldering pastes

2.2 Viscosity measurement

The viscosities of the pastes were determined with a cone-and-plate Haake VT700 viscometer at the J.Stefan Insitute (IJS), Ljubljana. The following parameters were determined:

-Viscosity versus shear speed (Fig.1, Fig.2, Fig.3 and Fig.4), measured on solder pastes from various producers on both a fresh sample and a sample that had been stored in a refrigerator for 4 months.

Fig. 1 shows the viscosity of the F817 solder paste, Fig.2 is for CR39, Fig.3 is for NCD 8010-9 and Fig.4 is for IF9002 JAC

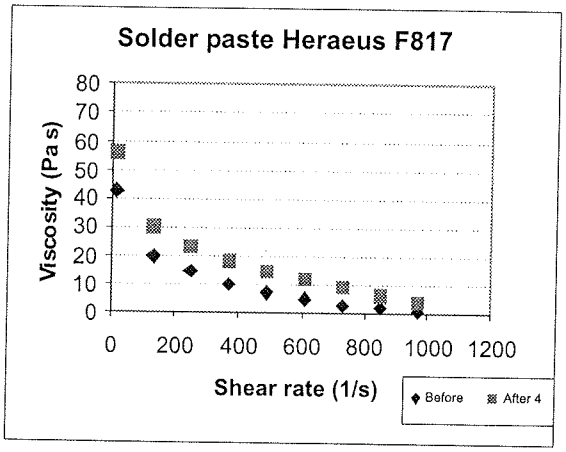


Fig. 1

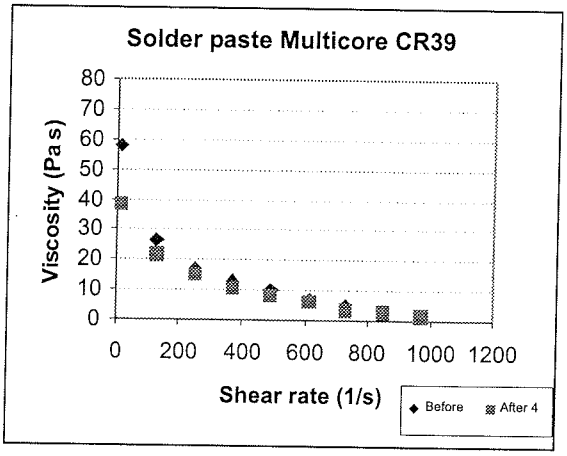


Fig. 2

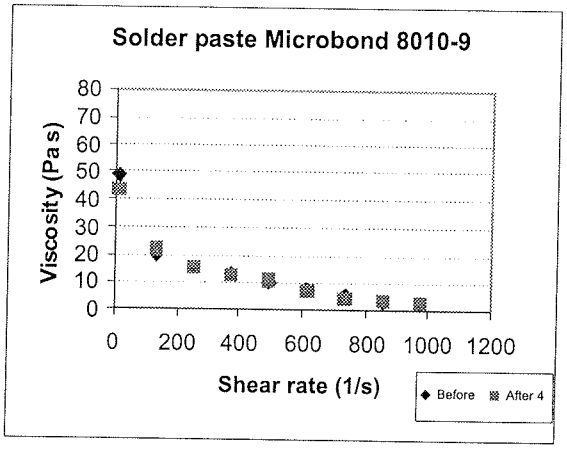


Fig. 3

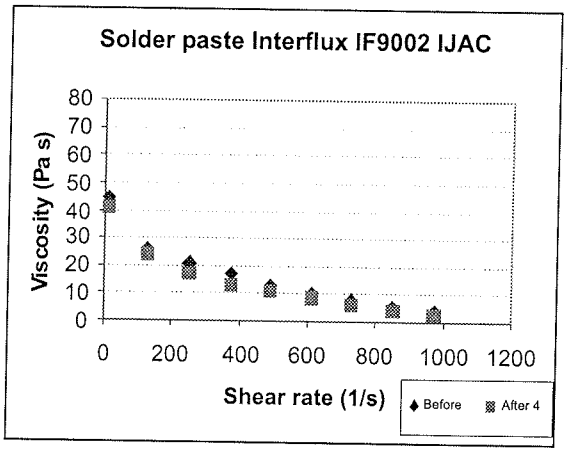


Fig. 4

2.3 Ionic contamination measurement

The ionic contamination measurement of the solder paste after soldering was made with a conductometer at Iskra-emeco according to the MIL-P-28805A Standard.

The test samples were prepared at the IJS on 2x2-inch ceramic substrates using thick-film conductors soldered

with following lead-free solder pastes:E 808.3, OM310, F817, NCD 8010-9, CR39 and IF 9002 JAC. The samples were not cleaned before the measurements and during preparation they were handled with gloves.

The results of ionic content measurements after reflow soldering of the samples on a hotplate at 240°C are given in Table 2.

Paste name	Ionic Content ($\mu gNaCl/cm^2$) Measured at Iskraemeco
E 808.3	0.2
OM 310	0.1
F817	0.25
NCD 8010-9	0.1
CR39	0.2
IF9002JAC	0.1

Table 2: Ionic contamination test results on a ceramic substrate for solder pastes printed using a fine-pitch stencil.

2.4 Solder-ball testing

The solder-ball test was used to determine the reflow properties of the solder pastes. These tests were carried out using ceramic substrates. The paste was deposited through a 0.2-mm-thick stainless-steel stencil with a 6-mm hole diameter. After 1 h of conditioning in the laboratory atmosphere the samples were soldered with a reflow peak temperature at 240 °C for 20 s. The samples were reflow soldered in three different furnaces: at the IJS, at Iskratel Electronics and at HIPOT-HYB.

The degree of coalescence was determined by comparing with the criteria given in the ANSI Standard for tin-lead solder paste /4/. According to the test criteria, when a paste forms a single sphere without small balls after soldering (criteria 1) or if in addition to one big sphere up to five small spheres are formed (criteria 2). Our test results are presented in Table 3 (according to test criteria /4/) and in Fig.6.

Fig.5 shows a reflow-soldering temperature profile in the production furnace at Iskratel Electronics.

The time-temperature reflow-soldering profile was selected according to the suggestions of the different producers of the tested solder pastes. The peak temperature was set at a minimum value of 235°C for the reflow soldering of both solder pastes with composition SnAg and SnAgCu. The selected profile was identical for all the tested solder pastes, however, for some solder pastes will have to be optimized later. The aim of the solder pastes testing on solder balls and wetting, after reflow soldering in different furnaces was, to observe the influence of the time-temperature profile on the test result.

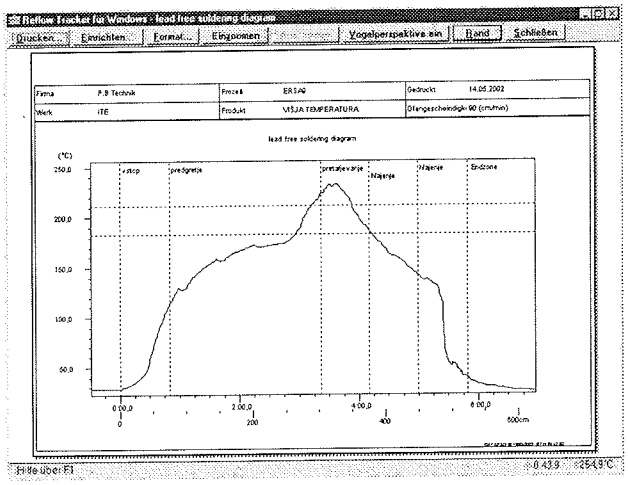


Fig.5: Reflow-soldering profile of the furnace at Iskratel Electronics for lead-free solder pastes (peak temperature higher than for SnPb solder pastes)

The similar reflow-soldering temperature profile was obtained in the production furnace at HIPOT-HYB, only the peak temperature was higher, 245°C in comparison with 235°C obtained in the furnace at Iskratel Electronics. The temperature profile for the small reflow-soldering furnace at the IJS is not shown, because this furnace has only a two-zone profile, and it was not possible to have a profile like in Fig.5, however, the peak temperature was 240°C for 20 s.

Solder paste	Reflow temperature profile IJS	Reflow temperature profile HIPOT	Reflow temperature Profile Iskra
	Criteria	Criteria	Criteria
E 808.3	A	A	A-B
OM 310	B	C	C
F 817	A-B	A	B
NCD 8010-9	A	B	B
CR39	A	B	B
IF9002 JAC	B	C	B-C

Table 3: The results of the solder-ball testing according to ANSI Standard (criteria A,B,C or D), tested at the IJS , HIPOT-HYB and Iskratel Electronics

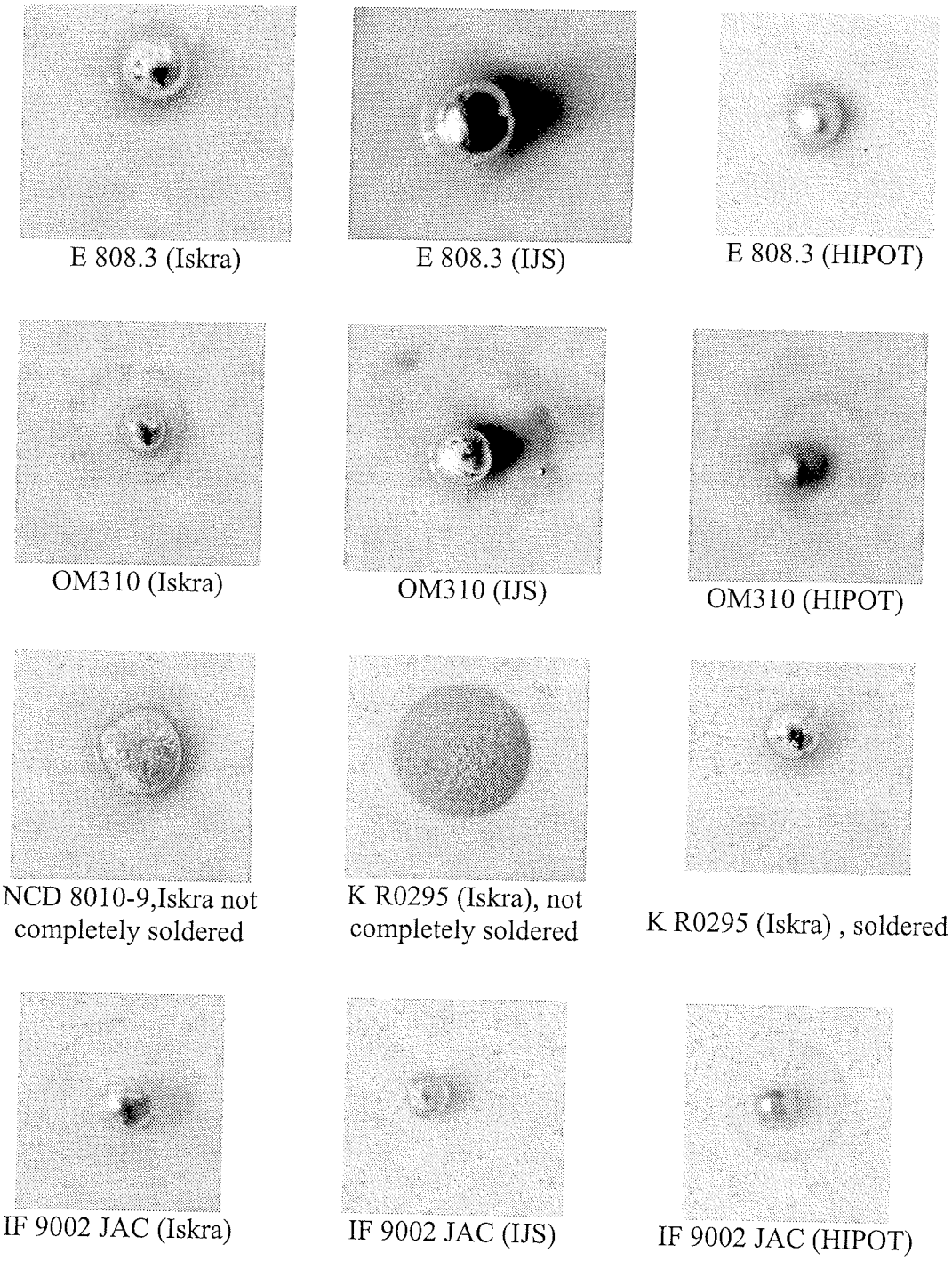


Fig.6: The results after solder-ball testing

Fig 6 shows the results of the solder-ball testing after reflow soldering of solder pastes E 808.3, OM310, NCD 8010-9 and IF 9002JAC. Also, the results of the solder-ball test for the solder paste K R0295, reflow soldered in the furnace at Iskratel Electronics are presented for various test samples.

2.5 Wetting test

The wetting properties of the solder paste were tested according to the ANSI Standard /5/. The paste was deposited by means of a stencil, on a cleaned, double-copper-clad laminate FR 4, with a thickness of 1.5 mm. Immediately after printing the paste was reflowed in the production furnace at Iskratel Electronics, in the production furnace at HIPOT-HYB and in the laboratory furnace at the IJS. The samples for the wetting test at the IJS were prepared on both copper-clad laminate and on the ceramic substrate with a AgPd thick-film conductor. The results are presented in Table 4 and in Fig.7.

Solder paste	Reflow-soldering profile Iskra	Reflow soldering profile HIPOT	Reflow-soldering profile IJS 240°C, 20s	
			Cu substrate	AgPd conductor
E 808.3	A-B	B-C	A	B
OM 310	C	C	B-C	B
F 817	B-C	C	B	A
NCD 8010-9	B-C	B-C	B	A
CR 39	B-C	C	B	A-B
IF9002 JAC	C	C	B	B

Table 4: The results of the wetting test according to ANSI Standard (criteria A, B,C or D) for samples prepared at Iskratel Electronics , HIPOT-HYB and the IJS

Fig.7 shows the results of the wetting tests when the solder pastes E 808.3, OM310 , NCD 8010-9 and IF 9002 JAC were reflow-soldered in the laboratory furnace at the IJS or in the production furnaces at Iskratel Electronics and HIPOT-HYB.

2.6 Copper corrosion test

The samples for the copper corrosion test were prepared on 0.05-mm-thick Cu foil according to ANSI Standard IPC-TM-650, 2.6.15. /6/ The foil was carefully cleaned before the solder paste deposition. A circular depression was formed in the foil, into the middle of which 1 g of solder for test was placed. The solder paste was reflowed on the hotplate at 240°C and placed vertically in a humidity chamber at 40°C, 93%RH for 10 days. After the exposure period the samples were examined at 20X magnification with

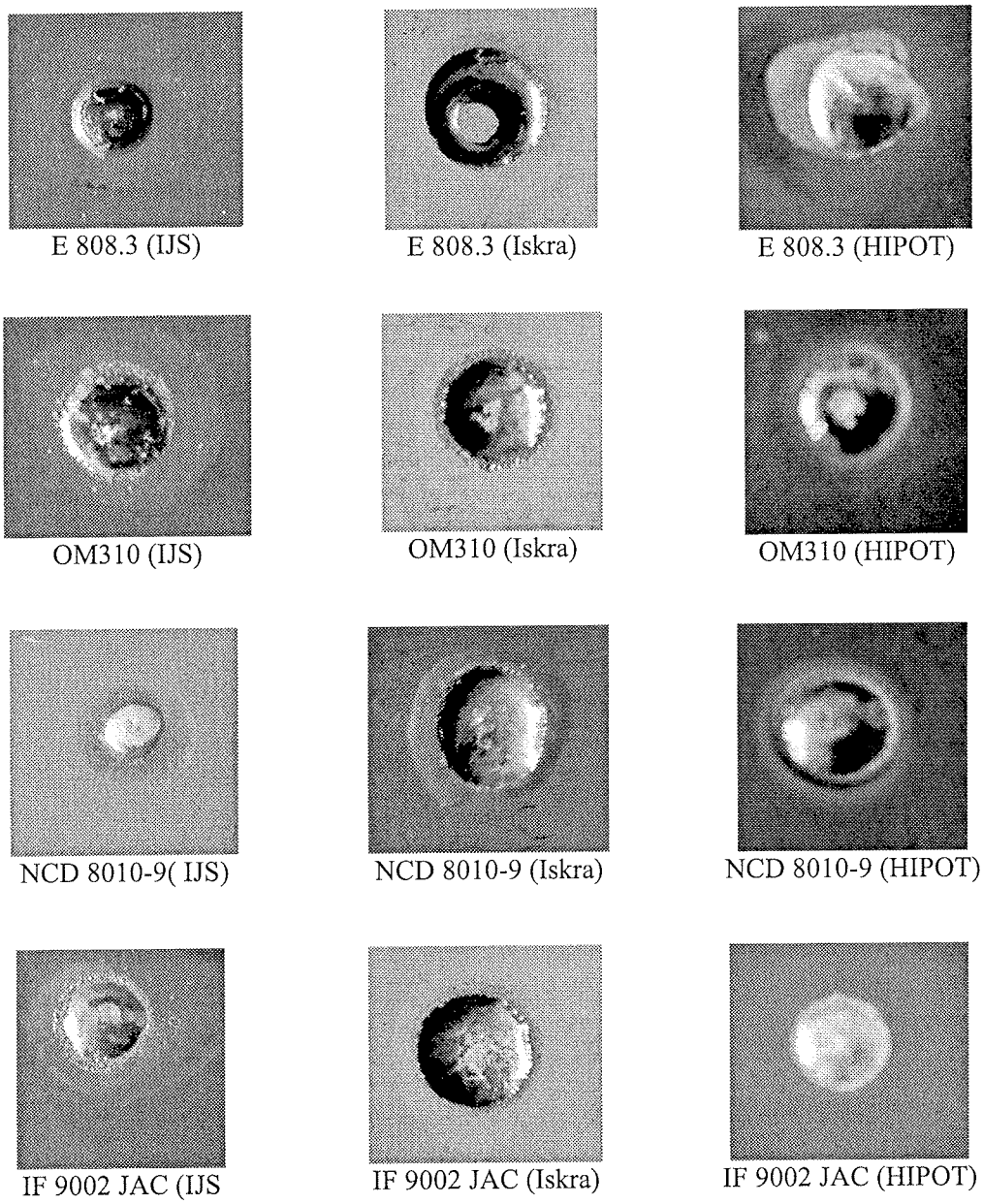
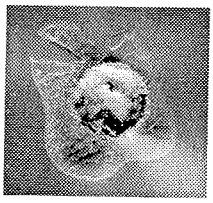
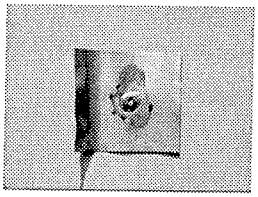


Fig.7: The results of wetting test

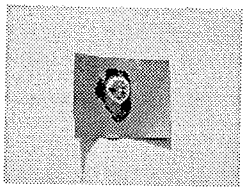
a microscope and the results for all the solder pastes are given in Table 5. Fig.9 are photographs taken after testing for the solder pastes E 808.3, IF9002 JAC, F817 and OM310.



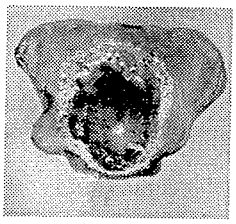
E 808.3



IF9002 JAC



F817



OM310

Fig.9: Results of copper corrosion test for solder pastes

Solder paste	Reflow-soldering profile IJS 240°C, 20s VISUAL ANALYSIS
E 808.3	No green residues
OM 310	Green residue
F 817	Olive green residue
NCD 8010-9	Olive green residue
CR 39	Olive green residue
IF9002 JAC	Green residues

Table 5: The results of copper corrosion test (10 days in humidity chamber at 40°C, 93%RH)

3. Discussion of results

The majority of the pastes measured with the Haake viscometer show a stable viscosity after 4 months of storage in the refrigerator. Only the solder pastes OM310, F369 and F817 show a slightly higher viscosity after storage. The solder paste IF 9002 JAC showed higher viscosity for the fresh sample than for the sample stored for 4 months in refrigerator for lower shear rates.

The results of the measurements of the ionic content in the flux residues after soldering (Table 1) show a very low ionic content from 0.1 to 0.25 μgNaCl/cm^2 for all the measured solder pastes, which is lower than allowed according to Standard MIL-P-28809A (1 μgNaCl/cm^2).

The results of the solder-ball testing presented in Fig.6 and Table 3 show, that all the investigated solder pastes passed this test (criteria A and B) except for the solder pastes IF 9002 JAC and OM310 (criteria C). The best result was obtained on samples with E 808.3 solder paste, with or without a very small number of small balls around the melted ball. In the samples with solder pastes IF 9002 JAC and OM310 around the melted ball were a large number of small balls, which is not acceptable.

No big influence on the test results was observed when the samples were reflow soldered in the three furnaces with somewhat different temperature-time profiles.

The biggest difference was obtained on samples with OM310 and IF9002 JAC solder pastes, when soldered in the furnace at IJS, the result was positive (B criteria) and when soldered in production furnaces at Iskratel Electronics and HIPOT-HYB, the result was negative (C criteria).

When the test samples were reflow-soldered in the production furnace at Iskratel Electronics, on some samples the solder paste was not completely melted, which means that the peak temperature of 235°C is not sufficient for soldering. In Fig.6 some examples of non-melted solder pastes (M 8010-9 and K R2095) are presented.

When the samples were reflow soldered in the production furnace at HIPOT-HYB, with a peak temperature 245°C, on all the samples the solder paste was melted.

The results of the wetting test given in Fig.7 and Table 4 for all the solder pastes tested show non-wetting (criteria B) or dewetting (criteria C), when reflow soldered on a Cu plate. When the solder pastes were tested on AgPd thick-film conductors, all the solder pastes showed better or similar results as tested on Cu printed circuit.

The test result of non-wetting or dewetting after reflow soldering in the furnaces was obtained when the samples were soldered in production furnaces. In some cases (solder pastes F817, NCD 8010-9 and CR39), when the samples were soldered in the laboratory furnace at the IJS, the solder pastes printed on the thick-film conductor completely wetted the AgPd surface.

A small difference in the test results was observed when the solder pastes CR39 and IF9002 IJAC were soldered in the Iskratel Electronics and the HIPOT-HYB production furnaces, but in both case the copper surface of the printed circuit substrate was not completely wetted.

The results of the copper corrosion test after conditioning in a humid atmosphere, given in Fig.9 and Table 5, show that the solder pastes OM310 and IF9002 IJAC have green residues. This means the flux residue after soldering contains some corrosive components.

The best results after the corrosion test was obtained for samples with solder paste E 808.3, which had no sign of corrosion. All the other solder pastes, after humidity testing, showed olive green residues, which is not a sign of a corrosive process.

4. Conclusion

All of the investigated pastes, measured with the Haake viscometer, demonstrate relatively stable viscosities after 4 months of storage in a refrigerator. This means that during the printing of 4-month-old solder paste the difference in the precision of dimensions of small printed pads for component soldering cannot be noticed.

The results of ionic content in flux residues after soldering show, for all the measured solder pastes, a very low ionic content from 0.1 to 0.25 $\mu gNaCl/cm^2$.

The results of copper corrosion test after conditioning in humid atmosphere show that solder pastes OM310 and IF9002 IJAC have green residues, which means the flux residue after soldering contains some corrosive components.

We did not observe a big difference in the results of the solder-ball and wetting tests after the samples were soldered in two production furnaces and in a laboratory furnace with not exactly recommended temperature profiles, but with recommended peak temperature from the producers of the solder pastes.

The peak temperature of 235°C is not sufficient for reflow soldering of solder pastes without lead.

From our results of the preliminary tests on lead-free solder pastes, it is clear that solder pastes tested do not wet the Cu-printed circuit surface well after melting. A little better wetting after soldering was observed when the solder pastes were printed on the AgPd thick-film conductor.

For the reliability testing of measurements the surface insulation resistance (SIR) between the soldered lines after humidity conditioning, will be selected the solder pastes E808.3, F817, NCD8010-9 and CR39, where the incoming test results were rather good, and also solder paste OM 310, because of the interest of the producer of this solder paste.

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/5/ American National Standard J-STD-005, IPC-TM-650, 2.4.45,

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MODERN DEVELOPMENT TRENDS IN HIGH-PERFORMANCE SOFT FERRITES

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Key words: electronics, magnetic ceramic, soft ferrites, development trends, high-performance, Mn-Zn ferrites, magnetic properties, electrical properties, microstructures, grain boundaries

Abstract: This paper considers the current MnZn-ferrite development trends in high-performance soft ferrites. Today, soft MnZn ferrites play the dominant role in magnetic materials. They are produced in large quantities and are used in a wide variety of applications. As a result, research and development in both industry and research centres has made great efforts to develop new classes of soft-ferrite materials.

Novi trendi priprave visokokvalitetnih mehkih feritov

Ključne besede: elektronika, keramika magnetna, feriti mehki, trendi razvoja, zmogljivost visoka, Mn-Zn feriti, lastnosti magnetne, lastnosti električne, mikrostrukture, meje med zrni

Izvleček: V članku so podane različne razvojne smeri priprave kakovostnih MnZn-feritnih materialov. Danes predstavljajo mehki feriti pomembne magnetne materiale, ki se proizvajajo v velikih količinah in za različne uporabe. Rezultat razvojnih dejavnosti v industriji in na raziskovalnih inštitutih so nove kvalitete mehko magnetnih feritnih materialov.

1. Introduction

Ferromagnetic ceramic materials, which are mainly composed of ferric oxide, have a lower saturation magnetisation than ferromagnetic alloys, however in spite of this, ceramics have the advantage of being usable at higher frequencies because of their higher electrical resistance, higher corrosion resistance, better heat resistance and lower price.

Applications using ferrites began about 30 years after the commercialisation of the ferromagnetic soft Fe-Si alloy. The commercial ferrites did not attract much attention because their magnetic properties were considerably inferior to those of ferromagnetic alloys. However, the importance of ferrites became clear during the 1950s, as a result of new applications such as radio, television, telephones, computer and microwave devices which were rapidly expanding at that time. At the same time, physicists and electronic engineers became very interested in the magnetism and the expanded high-frequency applications of ferrites. Research scientists in chemistry, ceramics and metallurgy also started to study ferrites and become engaged in the development of new ferrites and improved ferrite-manufacturing processes. Manufacturing ferrites is a complicated process that requires more steps than the manufacturing of ferromagnetic alloys. Because ferrites are frequently used as electronics parts, there are strict requirements in terms of the accuracy of their dimensions and the uniformity of their properties. Consequently, extremely good quality control is necessary during their manufacture.

Ferrites are mistakenly believed to be fully developed in all fields of science, technology and applications. Ferrite materials are now being recognised and crucial to the further development of electronics and it is believed that the production levels of ferrites will increase year by year as their applications become more diverse. Reviewing the history of ferrites and accurately analysing their present situation will help with further development in the future.

The electromagnetic properties of ferrites depend on the method of production and the resulting micro- and nanostructures. MnZn ferrite is designed to have a high permeability and to be used in power application. A high initial permeability over 15 000 at 10 kHz was recently achieved by using pure spray-roasted iron oxide. However, hand low power losses are also of prime importance for power applications. Control of the grain-boundary chemistry and the grain size by the appropriate selection of additives and firing conditions is required to achieve low power losses at high frequencies.

The magnetic characteristics of ferrites are sensitive to chemical composition, impurities, firing conditions, and so on. Much effort has been devoted to investigating these parameters in order to achieve the best properties in the limit of a conventional process. In order to go beyond these limits, attempts involving new processes for ferrite powders have recently been made. Hydrothermal synthesis, which is one of these new processes, is a process under consideration. This process may be particularly useful to producing low-cost high-performance power ferrites for high-frequency switching power supplies.

Finally, the parameters that determine the magnetic losses in MnZn ferrites, such as the purity of the raw materials, the influence of the dopant and the sintering process are considered in terms of their effect on the final magnetic properties.

2. MnZn FERRITES

MnZn ferrites are generally classified into three groups: i) high-permeability materials for wide-band and pulse transformers, ii) low-loss materials for inductors and telecommunications uses and iii) high-saturation-flux-density materials for power applications.

The performance of ferrites is not determined only by the high value of the initial permeability. The other characteristics such as a low loss value, a high saturation flux density, a high sintered density and frequency characteristics are also important. In many cases, these requirements are not satisfied at the same time, so a compromise material has to be selected in such cases.

2.1. High initial permeability materials

The initial permeability of high-permeability materials depends to a large extent on the mobility of the Bloch' s domain walls. To obtain high permeability it is important to lower the anisotropy and the magnetostriction. During the development of high-permeability MnZn ferrites in the past, much effort was devoted to the parameters which govern the bulk properties such as composition, microstructure and porosity /1/. To achieve a high permeability the composition of MnZn ferrite must be selected from a relatively narrow composition range where a zero crystalline anisotropy and a zero average magnetostriction can be expected. Studies of the grain-boundary chemistry in combination with grain-boundary structural analyses revealed that the grain boundaries are usually a source originating from

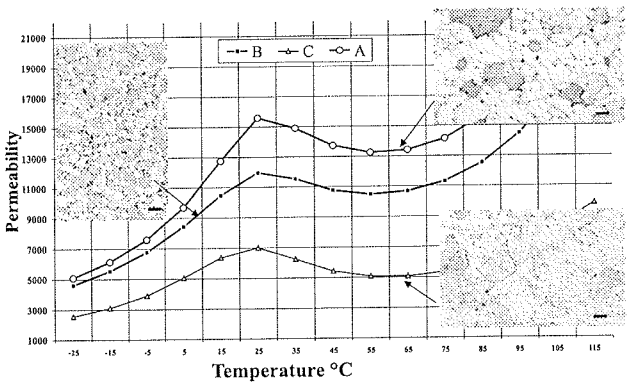


Fig. 1: Effect of liquid-phase-forming additives on the μ - T characteristics of sintered MnZn ferrites; A - doped with Bi_2O_3, SiO_2 > 200 ppm; B- doped with Bi_2O_3, SiO_2 < 200 ppm and C - doped with Bi_2O_3, SiO_2 < 500 ppm . The micron marker is 30μ m.

ZnO evaporation and the presence of a glassy phase at the grain boundary and the segregation of aliovalent ions /2/. Firing conditions and additives are also important for achieving good properties, Fig.2. However, the most important microstructural parameter when it comes to achieving a high magnetic permeability is large and inclusion-free ferrite grains.

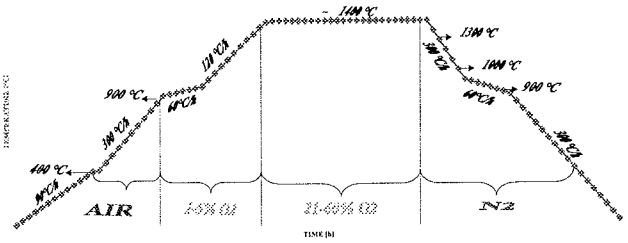


Fig.2: Typical firing program used for sintering of high performance high permeability ferrites

In order to increase the average grain size in MnZn ferrites the mobility of the grain boundaries must be promoted by using a proper additions that form a liquid phase during sintering such as Bi_2O_3 or SiO_2. In order to take the advantage of the presence of the liquid phase in ferrites during sintering, solid-state diffusion must be the prime mechanism at a constant amount of liquid phases until the total grain-boundary surface area decreases to such an extent that a liquid-phase film of a critical thickness d_0 is formed and solution-reprecipitation starts /3/.

The coarse grains in samples C, with intragranular porosity can be easily attained by discontinuous grain growth when the critical liquid-phase film is achieved at an early state of sintering when the average grain size is relatively small. Pores in large grains make no contribution to the magnetisation and decrease the free path length of domain walls during magnetic polarisation thus decreasing the magnetic pemeability.

Continous grain growth in the samples B is a key to achieving a relatively high permeability due to the intergranular porosity and the formation of grains free of non-magnetic inclusions. However, the average grain size obtained after just the solid-state sintering is usually about 30 μ m unless long sintering times are used. Long sintering times increases the average grain size but are detrimental to the permeability due to the evaporation of ZnO (4). Here, sample B contains an insufficient amount of liquid-phase-forming impurities or additions that would otherwise induce a liquid-phase film to provoke the anomalous grain growth.

In sample A the formation of a critical liquid-phase film was delayed as long as possible and the solution-reprecipitation processes started at a time when the total surface grain-boundary area decreases during solid-state sintering, accompanied by a grain size increase to about 30 μm. Here, during this sintering step the driving force is already "exhausted" and the pore size has increased and he pores were more resistant to being entrapped during the exag-

gerated grain growth. This all leads to a microstructure with larger average grain size and pore-to-pore distance and consequently to a higher magnetic permeability.

2.2. Low-loss Power Ferrites

Power ferrites should have low-power- loss characteristics under driving conditions. Low-power- loss MnZn ferrites should have uniformly sized fine grains and a high fired density. Thus far, the power-loss characteristics of ferrites were improved mainly by additives and a suitable sintering profile. Additives and impurities responsible for the grain-boundary chemistry have a remarkable effect on the grain boundaries properties, particularly on the grain-boundary resistance /5/. In order to obtain a sintered body with uniformly sized fine grains, which would be suitable for achieving low power losses, grain growth should be suppressed especially in the initial stage of sintering.

The average grain size during sintering can be decreased when a suitable sintering profile is applied, Fig. 3. This program is a combination of an initially high oxygen concentration and then, above 900°C, a low oxygen concentration /6/. At an oxygen concentration of above 20 vol % the microstructural development in MnZn ferrites is dominated by exaggerated pore growth /7/, while at a lower oxygen concentrations, below about 20 vol % the grain-boundary mobility in MnZn ferrites during sintering is promoted because of the increase in the concentration of oxygen vacancies which are the slowest moving species and hence promote volume diffusion. On the other hand, grain growth in ceramics is largely determined by the attachment or separation of pores from grain boundaries, which depends on the ratio of pore size to grain /7/. Thus, a combination of an intial high oxygen partial pressure, which promotes exaggerated pore growth, and a subsequent low oxygen partial pressure, which enhances volume diffusion, can inhibit grain growth and consequently decrease the average grain size in MnZn ferrites and increase the final sintered density.

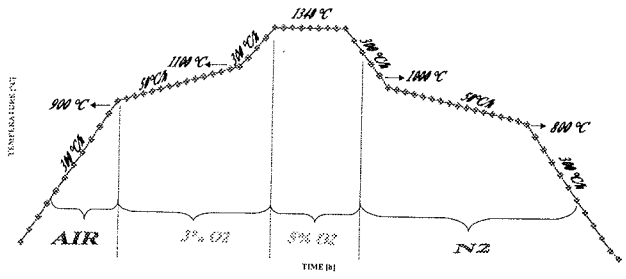


Fig. 3: Typical firing scheme for of high-performance power ferrite

The selection of high-grade raw materials with low level of impurities is of special importance in the production of MnZn ferrites with optimised microstructural properties. Ca and Si are well known to control the microstructural properties. This means that the raw materials have to be checked for existing levels of Ca and Si impurities. Both ions strongly influence the microstructure of MnZn ferrites. Furthermore, the total resistance of MnZn ferrites increases due to the precipitation of silicate phases at the grain boundaries. This has the advantage that CaO and SiO_2 are doped in a defined amount in the ferrite mixture and their effect can be optimised without being influenced by further impurities. In addition to the concentration of impurities, the reactivity of raw materials is a fundamental parameter when optimising the production process /9/.

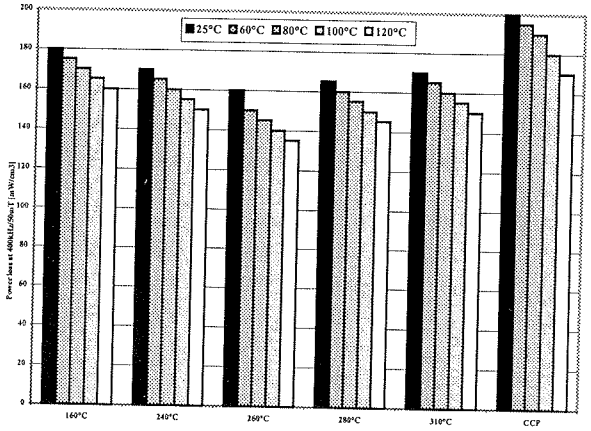


Fig. 4: Temperature dependence of the power loss of samples prepared by hydrothermal synthesis at various temperatures and a time of 10h versus a conventional ceramic processing; labeled as CPP.

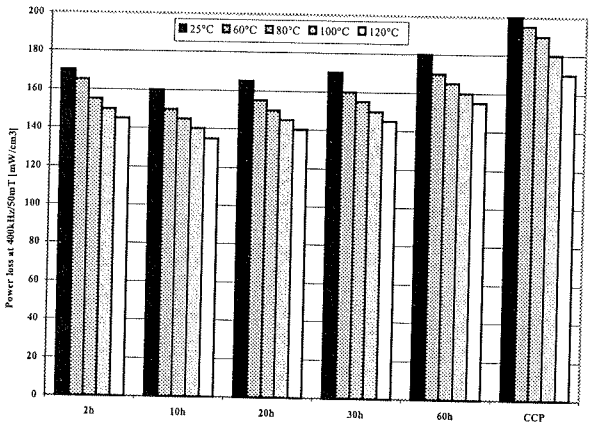
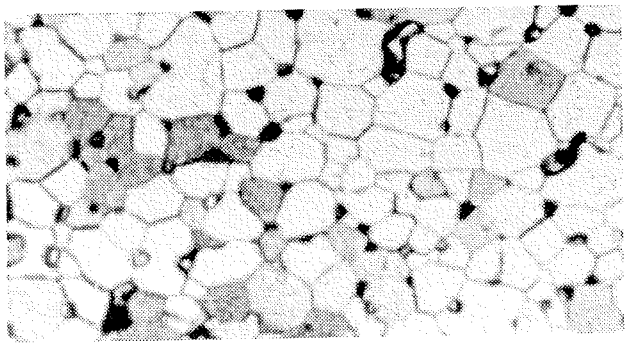


Fig. 5: Temperature dependence of the power loss of samples prepared by a hydrothermal synthesis under the same temperature conditions 260°C and different times versus a conventional ceramic processing, labeled as CPP.

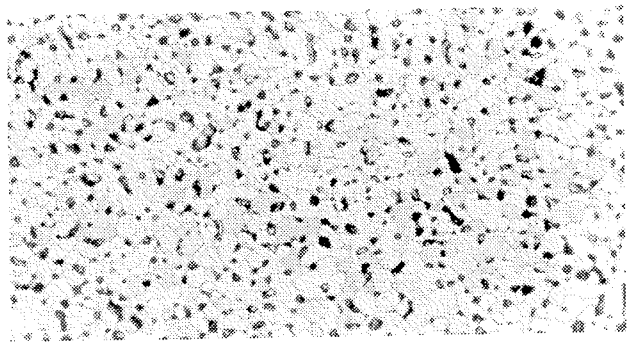
The power loss of samples prepared by the hydrothermal processing method is shown in Fig.4 and Fig.5. Samples synthesised at 260°C and 10 ^{h} exhibit the lowest power losses.

The large-scale production of MnZn-ferrite ceramic materials is based on ceramic technology involving pre-sintering of a homogenized mixture of appropriate starting oxides at temperatures around 900 - 1000 ^{0}C in air. The pre-sintered material is subsequently milled to produce the ferrite powder. The pre-sintering step has the following effects on the ferrite powder (i) oxides are partially transformed into various spinel phases, (ii) the variations in reactivity of the individual starting oxides are reduced and (iii) the starting mixture is homogenized.

An alternative method involves the preparation of ferrite powders by the hydrothermal treatment of starting oxides /10,11/. During the hydrothermal treatment, chemical reactions between oxides occur in an autoclave at elevated temperatures around 260 ^{0}C under a high pressure, normally at an equilibrium water pressure. As a result of the hydrothermal treatment, a homogeneous mixture of some residual reactants (Fe_2O_3, Mn_3O_4) and ferrite spinel products $Zn(Mn)Fe_2O_4$ is obtained. Hydrothermally derived powders are much finer and more homogenous than conventionally prepared powders using pre-sintering.



a



b

Fig. 5: Typical microstructures of samples; a) prepared by a conventional ceramic process, and b) by a hydrothermal process.

Raw-material quality is a very critical factor in ferrite processing. Other factors to be taken into account are reactivity, particle size distribution, chemical homogeneity, impurity content, impurity distribution and consistency between lots. In conventional processing the raw materials are mixed, pelletized, calcined and then milled to break up agglomerates. The disadvantages of this form of processing are poor homogeneity, a wide particle size distribution and the introduction of impurities during milling. The hydrothermal process eliminates the pelletizing, calcining and milling steps of the conventional process and leads to the formation of a fine, homogeneous powder with good reactivity.

3. Future Prospects for Ferrites

As described at the beginning, no-one doubts that the amount of ferrite produced will continue to increase each year. If researchers and engineers who work on MnZn ferrites take a closer look at the future prospects for MnZn ferrites and focus on important areas, of great value, the future for ferrites will be bright.

Most researchers who have studied the basic science of ferrites are now woking in other areas. The reason for this is that when we want to prepare ferrites with better properties or to find a new application, we may find that there is insufficient knowledge available from basic research. For example, when we want to achieve a value as close as possible the theoretical value for the magnetic or poweloss characteristics of MnZn ferrites by changing the heatreatment conditions, we would need a more precise understanding of the equilibrium between the phase and oxygen partial pressure, as well as the oxidation and the reduction kinetics of the ferrites.

It is not easy to develop novel, exiting new ferrite materials. At present, however, some promising materials are under investigation and their future development is anticipated.

The demand for soft ferrites has been growing and ferrites will expand considerably in both quantity and extent of application as the need for ferrites of higher quality increases. Raw materials and the improvement of technology, of which iron oxide is a major constituent, plays a decisive role in improving the quality as well as lowering the costs of ferrites. With a combination of improved raw materials, compositional and processing improvements, a new class of soft ferrite will be developed.

Furthermore, new applications of ferrites such as toners for photocopier application, new microwave ferrite material at a frequency of several tens of GHz and biomedical applications will be developed as a new research category.

Research on the application of ferrites for protecting the natural environment is being actively investigated. Applications include a washer disposal method for factory drains and the transformation of solar energy into hydrogen energy using ferrites as catalysts. We hope that some of these studies will become practical application in the near future /12/.

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ENLARGEMENT OF THE ROTATIONAL FIELD HOMOGENITY AREA IN A TWO-PHASE ROUND ROTATIONAL SINGLE SHEET TESTER

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Key words: magnetic devices, magnetic sheet, measurement, alternating magnetic fields, R.R.S.S.T., Round Rotational Single Sheet Testers, 3D modeling, three-dimensional modeling, calculations, numerical methods, FEM, Finite Element Method, experimental results

Abstract: Round rotational single sheet tester (R.R.S.S.T.) is used for the measurement of magnetic properties in rotational and alternating magnetic fields. The influence of the shields on the field homogeneity of the magnetic field distribution in the sample in the case of rotational magnetic field is investigated with finite element calculation. The aim of the calculation is to define optimal position of both side shields in order to expand the rotational field homogeneity area.

Povečanje področja homogenosti rotacijskega polja v dvofaznem rotacijskem merilniku magnetne pločevine

Ključne besede: naprave magnetne, pločevina magnetna, merjenje, polja magnetna izmenična, R.R.S.S.T. merilniki okrogli rotacijsko lastnosti pločevine magnetne enoslojne, modeliranje 3D tridimenzionalno, izračuni, metode numerične, FEM metoda elementov končnih, rezultati eksperimentalni

Izvleček: Okrogli merilec lastnosti magnetne pločevine se uporablja za merjenje lastnosti magnetne pločevine v rotacijskih in alternirajočih magnetnih poljih. Z izračuni, ki temeljijo na metodi končnih elementov, je proučevan vpliv ščitov na obliko rotacijskega polja v vzorcu okroglega merilca magnetne pločevine. Cilj izračunov je definiranje optimalne pozicije obojestranskih ščitov z namenom povečanja homogenega področja rotacijskega magnetnega polja.

1. Introduction

Two phase round rotational single sheet tester (R.R.S.S.T.) is used for the measurement of magnetic properties in rotational and alternating magnetic fields. Photo of the R.R.S.S.T. is shown in Fig. 1.

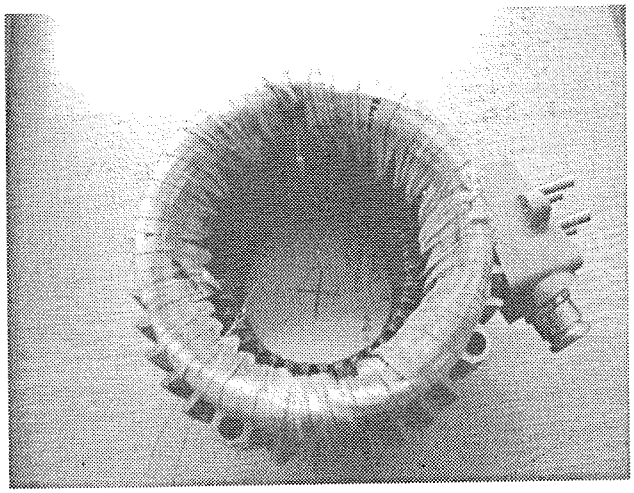

Fig. 1. Photo of the R.R.S.S.T.

The two phase winding is placed in the stator package of the induction motor and it produces rotational or alternating magnetic field. Measuring coils have to be placed in the homogeneous field. The excitation coils are longer than the sample thickness, which causes z-component of magnetic density ***B*** at the edges of the sample. The aim of the calculation is to define the optimal position of both side shields. The position of the shields can make the area of the homogeneous rotational field smaller or bigger than in the case with no shields by influencing the z-component of ***B*** /1/.

2. Modelling and calculation

R.R.S.S.T. is modelled as a 3D problem. The calculation is based on the use of the magnetic vector potential ***A*** and electric scalar potential *V* in the conducting area and only magnetic vector potential ***A*** in the nonconducting area (***A***, *V*-***A*** formulation /2/, /3/).

In the conducting area the differential Equations (1) and (2) have to be solved.

$$\nabla \times \frac{1}{\mu} \nabla \times \boldsymbol{A} - \nabla \frac{1}{\mu} \nabla \cdot \boldsymbol{A} + \sigma \frac{\partial \boldsymbol{A}}{\partial t} + \sigma \nabla V = 0 \qquad (1)$$

$$\nabla \cdot \left(-\sigma \frac{\partial \boldsymbol{A}}{\partial t} - \sigma \nabla V \right) = 0 \qquad (2)$$

In the nonconducting area the Equation (3) can be written.

$$\nabla \times \frac{1}{\mu} \nabla \times A - \nabla \frac{1}{\mu} \nabla \cdot A = J_s \qquad (3)$$

σ is the conductivity of the material, μ is the permeability of the material and J_s is the excitation current.

The calculation is made as a nonlinear transient calculation (T.C.) /4/. Magnetic material is defined with magnetisation curve. Anisotropy of the material is not taken into account in the calculation.

Euler's method is used for the time integration. Potentials at the time instant $n+1$ are calculated as in (4).

$$\left(\mathbf{S} + \frac{\mathbf{T}}{\Delta t}\right) \cdot A^{(n+1)} = R^{(n+1)} + \frac{\mathbf{T}}{\Delta t} \cdot A^{(n)} \qquad (4)$$

From (4) it is noticed that the potentials $A^{(n+1)}$ depend on the potentials from the previous time instant $A^{(n)}$. Euler's integration method is the first order integration method.

Cross sections of R.R.S.S.T. in the planes z=0 (horizontal plane) and x=0 (vertical plane) are shown in Fig. 2. and Fig. 3. separately. The length of the package is 86 mm. In Fig. 3. it can be seen, that d is the distance between the sample and the shield.

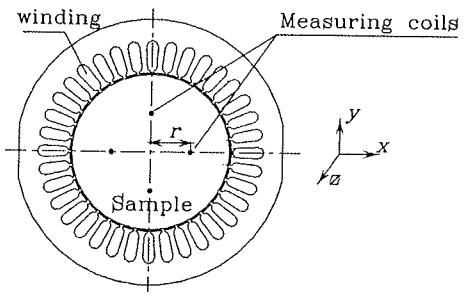

Fig. 2. R.R.S.S.T. in the plane z=0 (horizontal plane)

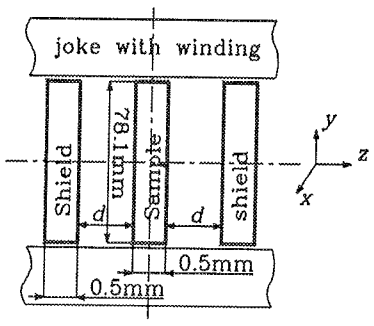

Fig. 3. R.R.S.S.T. in the plane x=0 (vertical plane)

Finite elements of the first order are used, which means that the approximation inside the element is linear. The elements are prisms. The two dimensional mesh of triangles in the horizontal plane is shown in Fig. 4. It is extracted into the three dimensional mesh of the prisms.

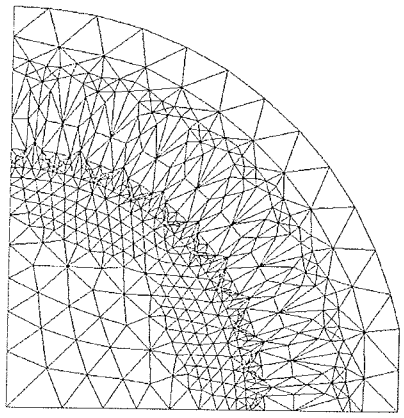

Fig. 4. Quarter of the 2D mesh in the horizontal plane

The problem is symmetrical. Only a half of the problem (from the centre z=0 to the end of the problem z=43 mm) is modelled and appropriate boundary conditions are set. The endings of the windings are not taken into account.

3. Results

The nonlinear characteristic of the material of the sample causes that the area of the homogeneous field is different for different $\boldsymbol{B}$ in the sample. If $\boldsymbol{B}$ in the centre of the sample is the same for all calculations, the nonlinearity of the material does not influence the result. Results are shown for magnetic density $\boldsymbol{B}$ = 1.43 T in the centre of the sample. The same can be concluded about the shields position influence on the field homogeneity for all amplitudes of $\boldsymbol{B}$. To get the same $\boldsymbol{B}$ in the centre of the sample algorithm from Fig. 5. is used.

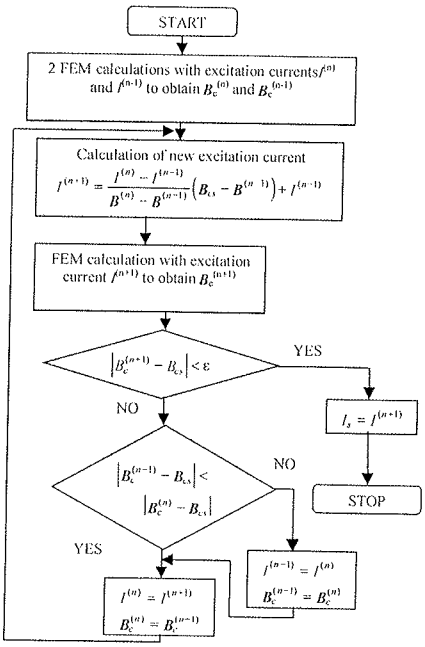

Fig. 5. Algorithm to get the same **B** *in the center of the sample.* B_{cs} *is* **B** *which we want to get in the center of the sample.* n-1, n, n+1 *are successive iterative calculation steps.*

The results obtained by use of both side shields are shown in Fig. 6. The procentual deviation of average value of $|\boldsymbol{B}|$ (averaging is made over the area enclosed by measuring coils) from value of $|\boldsymbol{B}|$ in the centre of the sample dependant on the radius of the measuring coils is shown.

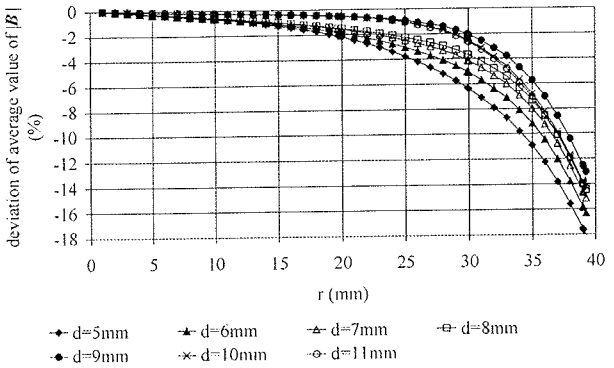

Fig. 6. Deviation of average value of $|\mathbf{B}|$ *from the value of* $|\mathbf{B}|$ *in the centre of the sample dependant on the radius of the measuring coils*

In Fig. 7., Fig. 8. and Fig. 9. magnetic flux density in the sample for the R.R.S.S.T. without the shields, for the R.R.S.S.T. with the shields which are in the distance of d = 5 mm from the sample and for the R.R.S.S.T. with the shields which are in the distance of d = 9 mm from the sample as in Fig. 3. is shown.

Z-component of $\boldsymbol{B}$ in the vertical plane for the R.R.S.S.T. without the shields, for the R.R.S.S.T. with the shields which are in the distance of d = 5 mm from the sample as in Fig. 3. and for the R.R.S.S.T. with the shields which are in the distance of d = 9 mm from the sample is shown in Fig. 10., Fig. 11., and Fig. 12. separately.

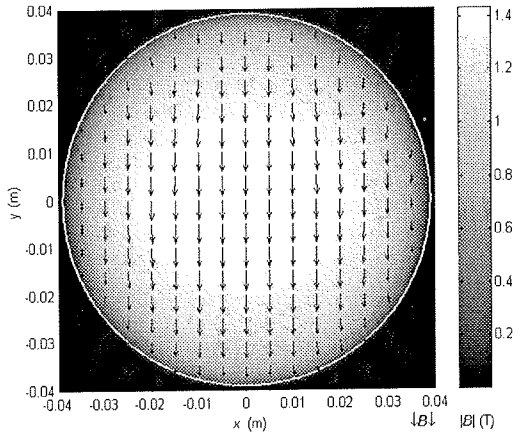

Fig. 7. **B** *as arrows and as shading in the sample in the plane z = 0 for the rotational magnetisation direction at 270⁰ of 50 Hz T.C. for R.R.S.S.T. without the shields*

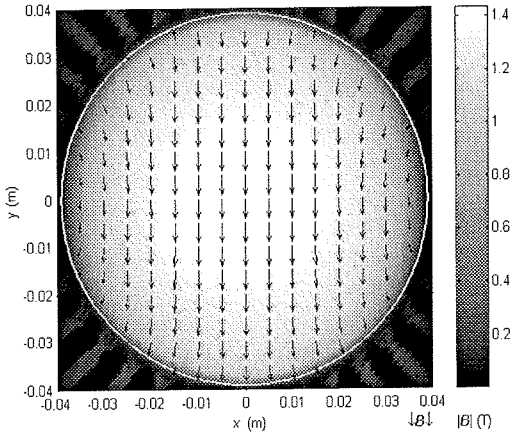

Fig. 8. **B** *as arrows and as shading in the sample (z = 0) for the rotational magnetisation direction at 270⁰ of 50 Hz T.C. for R.R.S.S.T. with the shields (d = 5 mm)*

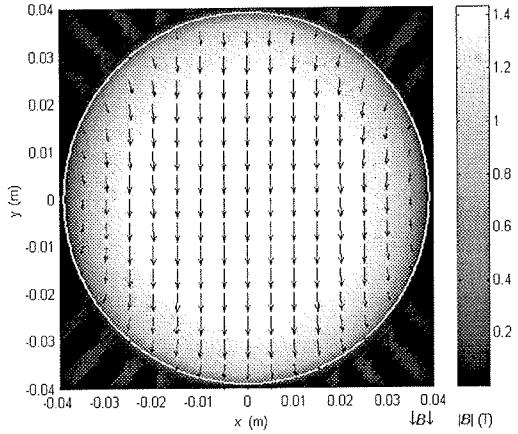

Fig. 9. **B** *as arrows and as shading in the sample (z = 0) for the rotational magnetisation direction at 270⁰ of 50 Hz T.C. for R.R.S.S.T. with the shields (d = 9 mm)*

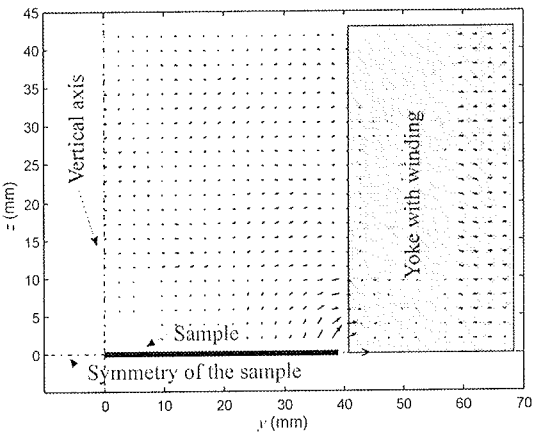

Fig. 10. **B** *in the vertical plane for the rotational magnetisation direction at 270⁰ of 50 Hz T.C. for R.R.S.S.T. without the shields*

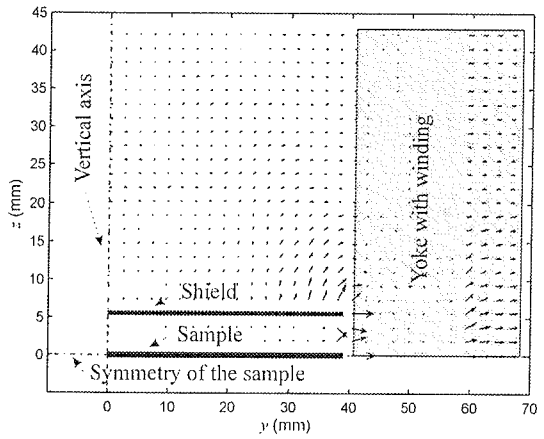

Fig. 11. **B** *in the vertical plane for the rotational magnetization direction at 270^0 of 50 Hz T.C. for R.R.S.S.T. with the shields* (d = 5 *mm)*

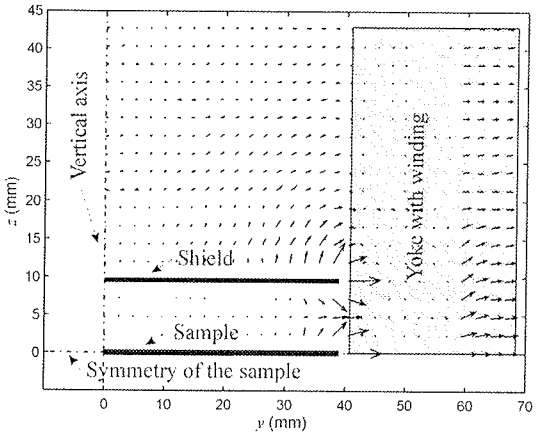

Fig. 12. **B** *in the vertical plane for the rotational magnetisation direction at 270^0 of 50 Hz T.C. for R.R.S.S.T. with the shields* (d = 9 *mm)*

In the case of T.C., the eddy currents appear at the edge of the sample and eddy currents cause that the direction of ***B*** in the sample does not coincide with the rotational magnetization direction. It can be seen from Fig. 13.

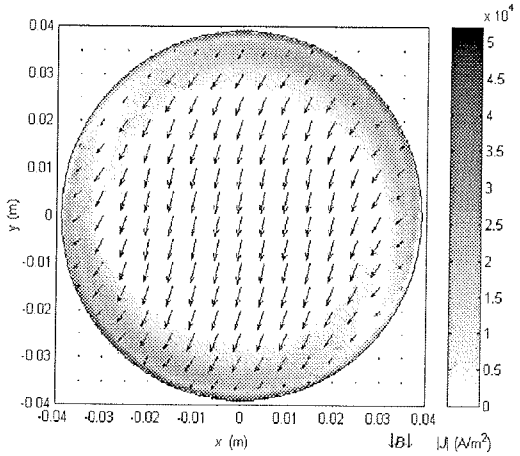

Fig. 13. **B** *as arrows and* |**J**| *as shading in the sample in the plane z=0 for the rotational magnetization direction at 270^0 of 500 Hz T.C.*

Fig. 14. shows changing of the direction of ***B*** depending on radius *r* of measuring coils for static calculation (S.C.), 50Hz transient calculation (T.C.) and 500Hz transient calculation. From Fig. 14. it can be seen that eddy currents in the case of 500Hz T.C. causes a big change of direction of ***B*** in the sample from the rotational magnetization direction. Shields improve only the amplitude of ***B*** but they do not influence the direction of ***B***. This is the reason why they are useful only for the frequencies in the rank of 50Hz.

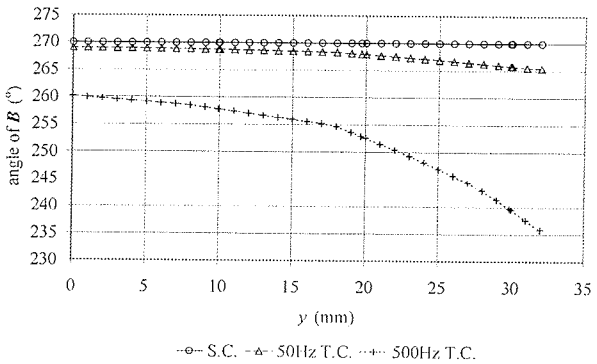

Fig. 14. Angle of **B** *along* y *axis for rotational magnetization direction at 270^0 of S.C., 50Hz T.C. and 500Hz T.C.*

Excitation currents obtained from the measurement on the N.O. 3% FeSi steel sample are used in the calculation. Procentual deviation between the 50Hz T.C. and measurement in the case where no shields are used for the rotational magnetization direction from 180^0 (*t* = 0 s) till 360^0 (*t* = 0.01 s) is shown in Fig. 15. Deviation is less than 9%. Deviation can be explained by the fact that anisotropy of the material and hysteresis effects are not taken into account in the calculation.

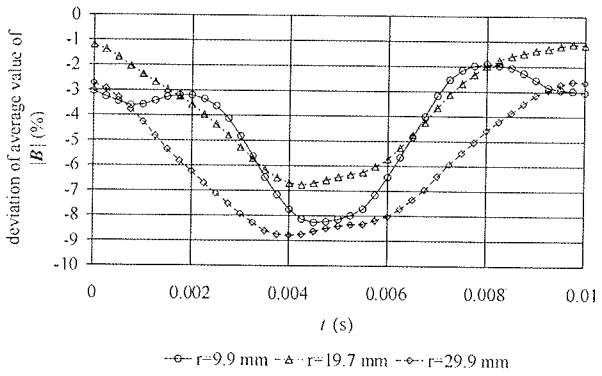

Fig. 15. Deviation of average value of |**B**| *for different* r *of measuring coils of 50Hz T.C. for R.R.S.S.T. without the shields from measurement*

4. Conclusions

The comparison of the best result for R.R.S.S.T. with both side shields and d = 9 mm, the result for R.R.S.S.T. with both side shields and d = 5 mm and result for R.R.S.S.T. with no shields is shown in Fig. 16. From Fig. 16. it can be seen that incorrect position of the shields can make the area of the homogeneous rotational filed smaller than in the case with no shields. The best result of all cases is obtained when both side shields are used and d = 9 mm.

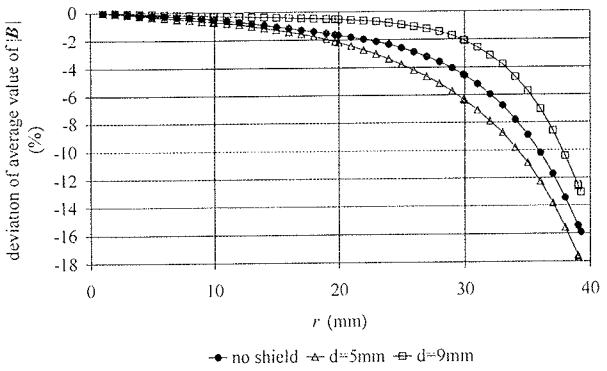

Fig. 16. Deviation of average value of |**B**| *from the value of* |**B**| *in the centre of the sample dependant on the radius of the measuring coils*

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ENOFAZNO TRIFAZNI NAPETOSTNI PRETVORNIK

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Ključne besede: elektronika energetska, pretvorniki napetosti, AC-DC-AC pretvorniki napetosti enofazne v trifazno, PARK transformacija, transformatorji električni, rezultati teoretični, rezultati eksperimentalni, rezultati praktični

Izvleček: V prispevku bo opisana pretvorba enofaznega napetostnega sistema v trifazni napetostni sistem. Ta pretvorba je bila zasnovana na uporabi Parkove transformacije. Parkova transformacija se je opravila na trifaznem transformatorju, ki je bil del pretvorniškega vezja. Pretvorniško vezje, ki napaja navitje srednjega stebra transformatorja, mora zagotoviti za p/2 zakasnjeno napajalno napetost glede na enofazno napetost, ki jo priključimo na navitja stranskih stebrov. Teoritične domneve so na koncu potrjene z laboratorijskim eksperimentom.

Single Phase to Three Phase System Conversion

Key words: power electronics, tension converters, AC-DC-AC single phase to three phase voltage converters, PARK transformation, electrical transformers, theoretical results, experimental results, practical results

Abstract: The single-phase to three-phase converter based on using of Park transformation is developed. The transformer, which is the main part of the whole system, has been supplied from grid and from the inverter which provides the p/2 delayed voltages, for central column of the transformer, according to the mains. In this paper the theoretical analysis and experimental verification is presented in this paper.

1. Uvod

Trifazni sistemi in pripadajoča trifazna oprema imata nekaj prednosti pred enofaznimi sistemi in enofazno opremo. Trifazno napajanje omogoča uporabo enostavnih zvezda-trikot zagonov za zmanjševanje zagonskih tokov. Trifazni motorji imajo večje zagonske navore in manjšo valovitost navora, kot jo imajo primerljivi enofazni motorji. Trifazna usmerniška vezja povzročajo manjše popačitve omrežnih tokov, kot to povzročajo enofazni usmerniki pri pretoku iste količine moči /1/. Slabost trifaznih sistemov pa je, da so pogosto ekonomsko neizvedljivi na nekaterih krajih, kot so npr. visokogorske kmetije, planinske koče, otoki ali več sto kilometrov oddaljeni industrijski obrati. Če zagotovimo relativno poceni pretvorbo napetosti iz enofaznega v trifazni sistem, se le-ta kasneje obrestuje.

Za takšno pretvorbo potrebujemo pretvorniška vezja, ki vsebujejo veliko ektronskih komponent, tako v močnostnem kot v krmilnem delu, in so zaradi tega zelo draga. Uporaba Parkove transformacije pri takšni pretvorbi pa zmanjša število elektronskih komponent, poenostavi regulacijo ter zmanjša toplotne izgube in višje harmonike v napajanju /2/, /3/.

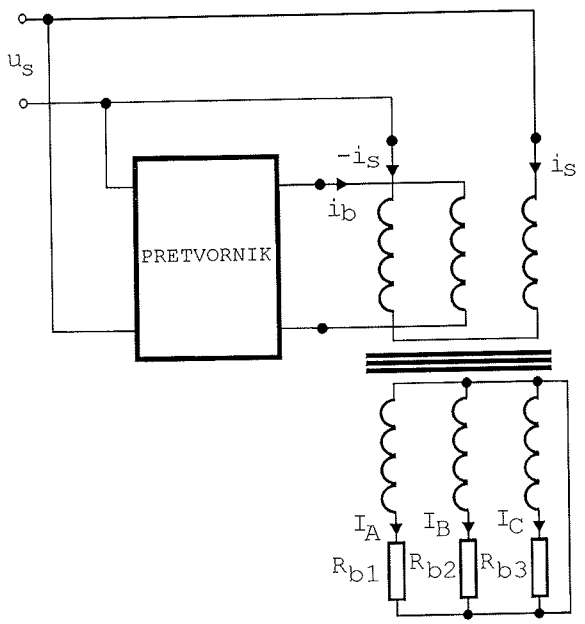
V tem prispevku bomo pokazali izvedbo pretvornika enofaznega napetostnega sistema napetosti v trifazni napetostni sistem /4/. Parkova transformacija se bo opravila v jedru transformatorja. Transformator je na primarni strani vzbujan z dvema tokoma, ki sta med seboj fazno premaknjena za $\pi/2$. Podali bomo teoretične predpostavke in nato z eksperimentom pokazali, da so teoretične domneve pravilne.

2. Teoretične osnove

Parkova transformacija je trifazno-dvofazna transformacija, ki nam preslika sistem trifaznih veličin v sistem dvofaznih veličin. Zapleteno impedančno matriko modela trifaznega stroja, ki zaradi treh navitij in njihovih medsebojnih induktivnosti vsebuje devet členov, pretvori v ekvivalenten dvofazni model. Impedančna matrika modela dvofaznega stroja, pri katerem zagotovimo pogoje, da ni induktivnih sklopov (navitji sta prostorsko premaknjeni za $\pi/2$, kakor tudi magnetilna tokova), pa vsebuje samo lastne induktivnosti in je diagonalna. Parkova transformacija nam za lažjo in hitrejšo matematično analizo trifaznih strojev pretvori model trifaznega stroja v ekvivalenten model dvofaznega stroja. Pri pretvorbi, ki bo opisana v nadaljevanju, bodo uporabljena spoznanja te transformacije. Osnova pretvornika je trifazni transformator, navit na skupnem jedru. V transformatorju poteka dvofazno-trifazna transformacija.

2.1 Tokovne razmere

Prvi fazni tok i_s teče neposredno iz omrežja, ta pa magneti navitja, navita na dveh stranskih stebrih. Drugi fazni tok i_b magneti navitje srednjega stebra, generira pa ga usmerniško-razsmerniško vezje, kot je to prikazano na sliki 1. Vrednosti in fazne razmere teh tokov nam bo pokazala nasled-



Slika 1: Pretvornik enofaznega napetostnega sistema v trifazni napetostni sistem

nja analiza. Sistem primarnih faznih tokov lahko ponazorimo kot vektor, ki je enak vsoti posameznih vektorskih komponent tokov v smeri osi *d* in v smeri osi *q*:

$$\overrightarrow{i_{ABC}(t)} = \overrightarrow{i_d(t)} + \overrightarrow{i_q(t)} \tag{1}$$

kjer za komponenti i_d in i_q velja:

$$\begin{aligned} i_d(t) &= f_1(i_A(t), i_B(t), i_C(t)) \\ i_q(t) &= f_2(i_A(t), i_B(t), i_C(t)) \end{aligned} \tag{2}$$

oziroma:

$$\begin{aligned} i_d(\omega t) &= \hat{I}_s \sin(\omega t) \\ i_q(\omega t) &= \hat{I}_s \cos(\omega t) \end{aligned} \tag{3}$$

kjer $\hat{I}_s$ predstavlja amplitudo toka v *d-q* koordinantnem sistemu, ω pa krožno frekvenco. Naslednji izraz opisuje Parkovo dvofazno trifazno transformacijo /3/:

$$\overrightarrow{i_{ABC}(t)} = \mathbf{B}_1\mathbf{B}_2\mathbf{B}_3\overrightarrow{i_{dq0}(t)} \tag{4}$$

kjer je $\overrightarrow{i_{ABC}(t)} = [i_A\ i_B\ i_C]^T$ in $\overrightarrow{i_{dq0}(t)} = [i_d\ i_q\ i_0]^T$. Prva matrika $\mathbf{B}_1$ je matrika simetričnih komponent. Ta matrika vsebuje devet členov zaradi treh navitij in njihovih medsebojnih povezav, kot je to prikazano v (4):

$$\mathbf{B}_1 = \frac{1}{\sqrt{3}}\begin{bmatrix} 1 & 1 & 1 \\ e^{j\frac{4\pi}{3}} & e^{j\frac{2\pi}{3}} & 1 \\ e^{j\frac{2\pi}{3}} & e^{j\frac{4\pi}{3}} & 1 \end{bmatrix} \tag{5}$$

Druga matrika $\mathbf{B}_2$ je enostavnejša, saj opisuje ekvivalenten dvofazni sistem, kjer ni induktivnih sklopov; navitja so prostorsko premaknjena za $\pi/2$, kar zagotovi enako fazno premaknitev magnetilnih tokov:

$$\mathbf{B}_2 = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & j & 0 \\ 1 & -j & 0 \\ 0 & 0 & \sqrt{2} \end{bmatrix} \tag{6}$$

Tretja matrika $\mathbf{B}_3$ pa pri transformaciji zagotovi še za kot Θ zasukan prostorski koordinatni sistem:

$$\mathbf{B}_3 = \begin{bmatrix} e^{j\Theta} & 0 & 0 \\ 0 & e^{j\Theta} & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{7}$$

Ob predpostavki, da je Θ=0 in ob vstavitvi izrazov (4)-(6) v (3) za trifazni sistem tokov, velja nasednji zapis:

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \frac{1}{\sqrt{6}}\begin{bmatrix} 2 & 0 & \sqrt{2} \\ -1 & \sqrt{3} & \sqrt{2} \\ -1 & \sqrt{3} & \sqrt{2} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \tag{8}$$

Toki i_A, i_B in i_C v bistvu ne tečejo skozi primarna navitja, saj tega pretvorniško vezje ne omogoča (slika 1). Enačbo (8) je treba izpisati po komponentah:

$$\begin{aligned} i_A &= \frac{1}{\sqrt{6}}\left(2i_d + \sqrt{2}i_0\right) \\ i_B &= \frac{1}{\sqrt{6}}\left(-i_d + \sqrt{3}i_q + \sqrt{2}i_0\right) \\ i_C &= \frac{1}{\sqrt{6}}\left(-i_d - \sqrt{3}i_q + \sqrt{2}i_0\right) \end{aligned} \tag{9}$$

Ker sistem nima ničelnega voda, velja, da je i_0=0. Ob vstavitvi izraza (3) v (9) sledi:

$$\begin{aligned} i_A &= \frac{1}{\sqrt{6}}2\hat{I}_s \sin(\omega t) \\ i_B &= \frac{1}{\sqrt{6}}\left(-\hat{I}_s \sin(\omega t) + \sqrt{3}\hat{I}_s \cos(\omega t)\right) \\ i_C &= \frac{1}{\sqrt{6}}\left(-\hat{I}_s \sin(\omega t) - \sqrt{3}\hat{I}_s \cos(\omega t)\right) \end{aligned} \tag{10}$$

Po krajšem računanju iz (10) in /5/ izhaja:

$$\begin{aligned} i_A(\omega t) &= \frac{1}{\sqrt{6}}2\hat{I}_s \sin(\omega t) \\ i_B(\omega t) &= \frac{1}{\sqrt{6}}2\hat{I}_s \sin\left(\omega t + \frac{2\pi}{3}\right) \\ i_C(\omega t) &= \frac{1}{\sqrt{6}}2\hat{I}_s \sin\left(\omega t + \frac{4\pi}{3}\right) \end{aligned} \tag{11}$$

Trifazni sistem tokov (11) se navidezno pojavi na primarju transformatorja (v primeru Y vezave primarja transformatorja). Tako vzbujan transformator pa preko transformacijskega razmerja generira ustrezne sekundarne toke, ki na trifaznem bremenu povzročijo sistem trifaznih napetosti. Način za vzbujanje primarnih navitij je razviden iz (9). Tok i_A teče navidezno skozi navitje prvega stebra transformatorja, toka i_B in i_C pa skozi preostali dve navitji. Zaradi predlagane transformatorske vezave je treba izračunati toka, ki bosta v transformatorju generirala tako zastavljene trifazne razmere. Iz sistema enačb (9) dobimo odgovore na naslednji način:

$$i_B = \underbrace{-\frac{1}{\sqrt{6}}\hat{I}_s \sin(\omega t)}_{i_S} + \underbrace{\frac{1}{\sqrt{6}}\sqrt{3}\hat{I}_s \cos(\omega t)}_{i_b} \tag{12}$$

$$i_C = -\left(\underbrace{\frac{1}{\sqrt{6}}\hat{I}_s \sin(\omega t)}_{-i_S} + \underbrace{\frac{1}{\sqrt{6}}\sqrt{3}\hat{I}_s \cos(\omega t)}_{i_b} \right) \tag{13}$$

iz (12) in (13) vidimo, da dobimo trifazni sistem tokov i_A, i_B in i_C, če vzbujamo transformator z dvema tokoma, in sicer:

$$\begin{aligned} i_s(\omega t) &= -\frac{1}{\sqrt{6}}\hat{I}_s \sin(\omega t) \\ i_b(\omega t) &= \frac{1}{\sqrt{6}}\sqrt{3}\hat{I}_s \cos(\omega t) \end{aligned} \tag{14}$$

Iz (14) je razvidno razmerje med omrežnim tokom i_s, ki magneti stranska stebra transformatorja, in tokom, ki ga mora za magnetenje srednjega stebra zagotoviti razsmernik. Pri tem vidimo, da mora biti tok navitja na srednjem stebru za $\sqrt{3}$-krat večji od toka, ki teče skozi primarna stranska navitja transformatorja in je fazno premaknjen za $\pi/2$. Če bo tem pogojem zadoščeno, se na sekundarni strani transformatorja pojavi trifazni sistem tokov in posledično trifazni sistem napetosti. Napetostne razmere pa vidimo iz kazalčnega diagrama na sliki 2.

2.2 Napetostne razmere

Podobno, kot je bila uporabljena Parkova transformacija pri analizi tokovnih razmer, se lahko ta transformacija uporabi tudi pri analizi napetostnih razmer. Trifazni napetostni sistem se lahko dobi z ustrezno transformacijo dveh dvofaznih napetosti, zapisanih v *d-q* prostoru, in sicer:

$$\begin{aligned} u_d(\omega t) &= \hat{U}\sin(\omega t) \\ u_q(\omega t) &= \hat{U}\cos(\omega t) \end{aligned} \tag{15}$$

kjer $\hat{U}$ predstavlja amplitudo napetosti v *d-q* koordinantnem sistemu. Po uporabi enačb (5)-(7) sledi:

$$\begin{bmatrix} u_{AC} \\ u_{CB} \\ u_{BA} \end{bmatrix} = \frac{1}{\sqrt{6}} \begin{bmatrix} 2 & 0 & \sqrt{2} \\ -1 & \sqrt{3} & \sqrt{2} \\ -1 & \sqrt{3} & \sqrt{2} \end{bmatrix} \begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} \tag{16}$$

in nato ob predpostavkah, da je u_q=0, dobimo za napetosti u_{AC}, u_{CB} in u_{BA} izraze:

$$\begin{aligned} u_{AC}(\omega t) &= \frac{1}{\sqrt{6}} 2\hat{U}\sin(\omega t) \\ u_{CB}(\omega t) &= \frac{1}{\sqrt{6}}\left(-\hat{U}\sin(\omega t) + \sqrt{3}\hat{U}\cos(\omega t)\right) \\ u_{BA}(\omega t) &= \frac{1}{\sqrt{6}}\left(-\hat{U}\sin(\omega t) - \sqrt{3}\hat{U}\cos(\omega t)\right) \end{aligned} \tag{17}$$

kar po krajši analizi pripelje do znanega sistema trifaznih napetosti:

$$\begin{aligned} u_{AC}(\omega t) &= \sqrt{\frac{2}{3}}\hat{U}\sin(\omega t) \\ u_{CB}(\omega t) &= \sqrt{\frac{2}{3}}\hat{U}\sin\left(\omega t + \frac{2\pi}{3}\right) \\ u_{BA}(\omega t) &= \sqrt{\frac{2}{3}}\hat{U}\sin\left(\omega t + \frac{4\pi}{3}\right) \end{aligned} \tag{18}$$

V izrazih (17) so prikazane dejanske razmere, ki jih je treba zagotoviti na treh navitjih transformatorja in posledično za generiranje trifaznih napetosti na sekundarni strani:

$$u_{AC}(\omega t) = \underbrace{\frac{1}{\sqrt{6}} 2\hat{U}\sin(\omega t)}_{-u_S} \tag{19}$$

$$u_{CB}(\omega t) = \underbrace{-\frac{1}{\sqrt{6}}\hat{U}\sin(\omega t)}_{\frac{u_S}{2}} + \underbrace{\frac{1}{\sqrt{6}}\sqrt{3}\hat{U}\cos(\omega t)}_{u_b} \tag{20}$$

$$u_{BA}(\omega t) = -\underbrace{\left(\frac{1}{\sqrt{6}}\hat{U}\sin(\omega t) + \frac{1}{\sqrt{6}}\sqrt{3}\hat{U}\cos(\omega t)\right)}_{-\frac{u_S}{2}} \qquad \underbrace{\qquad\qquad}_{u_b} \tag{21}$$

Iz enačb (19)-(21) je razvidno, kako se primarna navitja transformatorja priključijo na omrežno napetost; in sicer se na navitja skrajnih stebrov transformatorja priključi omrežna napetost u_s, na navitje srednjega stebra pa se priključi napetost u_b, ki mora imeti za $\sqrt{3}$-krat večjo amplitudo, kot je amplituda omrežne napetosti, in fazno zamaknitev za $\pi/2$. Te razmere so razvidne iz (22):

$$\begin{aligned} u_s(\omega t) &= \frac{1}{\sqrt{6}} 2\hat{U}\sin(\omega t) = U_s\sqrt{2}\sin(\omega t) \\ u_b(\omega t) &= \frac{1}{\sqrt{6}}\sqrt{3}\hat{U}\cos(\omega t) = U_b\sqrt{2}\sin(\omega t) \end{aligned} \tag{22}$$

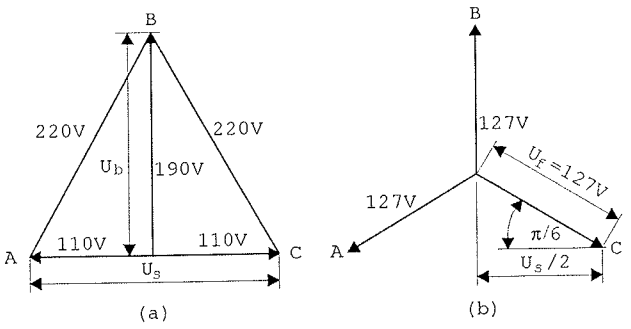
kjer U_s predstavlja efektivno vrednost napajalne napetosti in U_b predstavlja efektivno vrednost izhodne napetosti pretvornika. V primeru pretvornika na sliki 3 sta bili izbrani vrednosti omrežne in napetost na izhodu pretvornika:

$$U_s = 220V,\ U_b = (U_s/2)\sqrt{3} = 190$$

Na navitja stranskih stebrov je treba priključiti omrežni napetosti, ki sta fazno premaknjeni za π, kar je preprosto rešeno z zaporedno vezavo le-teh, kot je to razvidno s slike 3. Na sliki 2 sta prikazana kazalčna diagrama. Kazalčni diagram na sliki 2(a) prikazuje dejanske napetostne razmere na primarnih navitjih transformatorja. Napetost srednjega stebra prehiteva napetost C-stebra za kot $\pi/2$ in zaostaja za napetostjo stebra A za enak iznos. Vrednost amplitude napetosti srednjega stebra je mogoče dobiti iz (22), saj je za $\sqrt{3}$ -krat večja od napetosti, priključene na stransko navitje. Fazne napetosti na posameznih navitjih primarja transformatorja je mogoče izračunati s pomočjo geometrijskih razmer s slike 2(a). Ker imajo medfazne napetosti enake amplitude, se lahko v kazalčnem diagramu ponazorijo z enakostraničnim trikotnikom (slika 2(a)). Navidezna efektivna vrednost ene fazne napetosti primarnega navitja transformatorja U_f se izračuna z naslednjim izrazom:

$$U_f = \frac{U_s}{2}\sin\left(\frac{\pi}{6}\right) = 127V \qquad (23)$$

Izraz (23) omogoča izračun prestavnega razmerja transformatorja. S pomočjo (23) so tako podani vsi potrebni parametri, potrebni za projektiranje transformatorja.

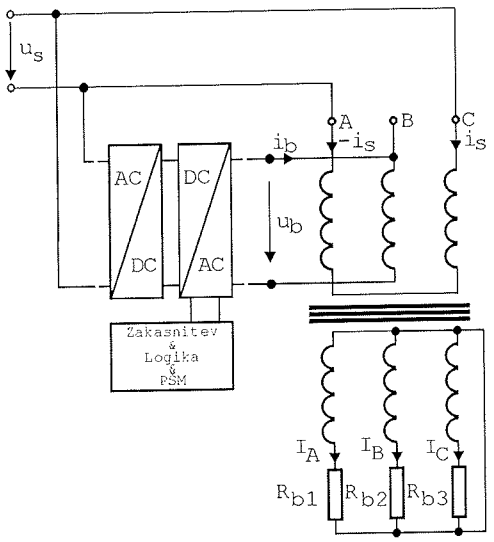


Slika 2: Kazalčni diagram

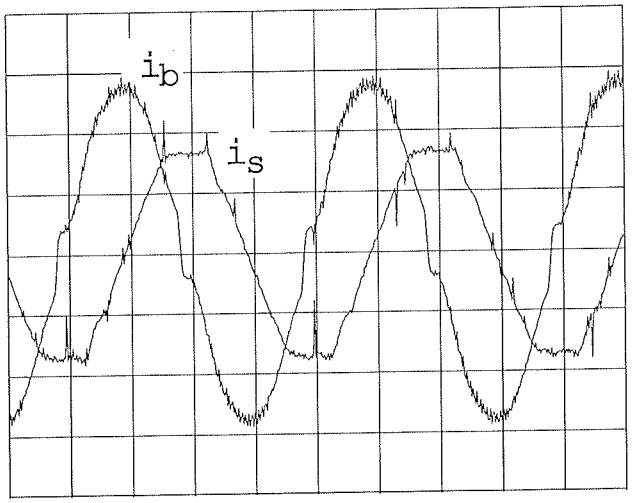
3. Praktična izvedba pretvornika

Iz pravkar opravljene matematične analize lahko povzamemo naslednje zahteve za projektiranje pretvornika:

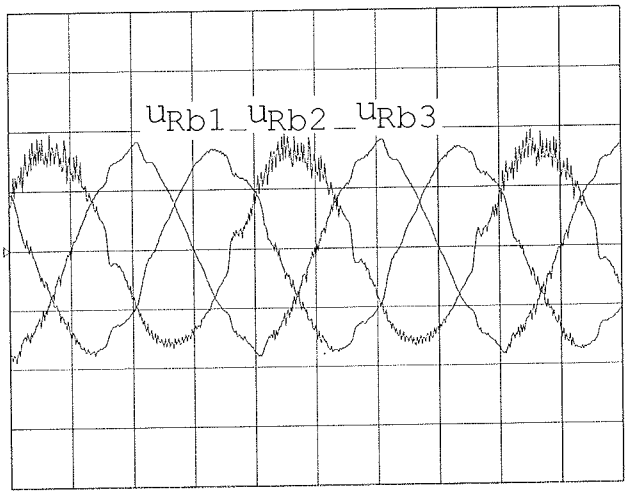
- Navitja stranskih dveh stebrov transformatorja je potrebno vezati protifazno.
- Navitje srednjega stebra transformatorja je potrebno magnetiti s tokom i_b, ki je premaknjen za kot $\pi/2$, glede na tok i_s, ki teče po navitjih na stranskih dveh stebrih.
- Zagotoviti je potrebno, da bo tok i_b, ki teče po navitju srednjega stebra, imel za $\sqrt{3}$ -krat večjo amplitudo, kot jo ima tok i_s, ki teče po navitjih na stranskih dveh stebrih.



Slika 3: Zasnova pretvornika



Slika 4: Primarna tokova: x-os 5ms/div; y-os 200V/div



Slika 5: Sekundarne napetosti: x-os 5ms/div; y-os 200V/div

Pretvornik, ki nam zagotavlja transformacijo iz enofaznega sistema v trifazni sistem, je sestavljen iz diodnega usmerniškega vezja in mostičnga razsmerniškega vezja /1/. Razsmernik je bil zgrajen z MOS-FET-i. Krmilna elektronika zagotovi ustrezna tokovna in napetostna razmerja na srednjem transformatorskem stebru. S pomočjo integratorskega vezja dobimo referenčni cosinusni signal, ki ga še ustrezno skaliramo, tako, da je bila amplituda osnovnega harmonika izhodne napetosti pretvornika (pred navitjem srednjega stebra transformatorja je bil vgrajen NP filter) za $\sqrt{3}$-krat večja, kot je bila amplituda omrežne napetosti u_s. Kot modulator je bil uporabljen standardni pulzno širinski modulator, izveden v enem čipu.

Natančnejši opis krmilne elektronike je podan v /4/. Na sliki 3 je podana blokovna shema celotnega sistema.

4. Eksprimentalni rezultati

Za zgoraj opisani pretvornik smo zgradili eksperimentalni model, s pomočjo katerega smo verificirali prikazano teorijo. Dobljeni rezultati so se zelo dobro ujemali s teoretičnimi predpostavkami. Na sliki 4 vidimo, da tok i_b, ki teče po navitju srednjega stebra, prehiteva za kot $\pi/2$ tok i_s, ki teče po navitjih stranskih stebrov transformatorja. Toka se razlikujeta tudi po amplitudi. Tok i_b je za $\sqrt{3}$-krat večji, kot je tok i_s. Ti rezultati torej potrjujejo izraz (15), ki smo ga dobili pri matematični analizi procesa.

Na sliki 5 so prikazane tri sekundarne napetosti, ki so med seboj premaknjene za $2\pi/3$. Zaradi nizke stikalne frekvence in neprilagojenega izhodnega filtra vsebuje napetost U_{rb2} stikalni šum. Napetosti U_{rb1} in U_{rb3} pa sta popačeni zaradi popačene omrežne napetosti. Izkoristek takšnega pretvornika se je v odvisnosti od obremenitve gibal od 77% do 86%.

Zanimiv je bil tudi eksperiment, pri katerem je bila preverjena občutljivost pretvornika na nesimetrično obremenitev. Pri polovični razbremenitvi enega sekundarnega navitja so izhodne napetosti med seboj odstopale za največ 10%. Pri popolni razbremenitvi enega sekundarnega navitja je bilo odstopanje večje od 10% le v primeru razbremenitve sekundarnega navitja srednjega stebra transformatorja. V tabelah 1 in 2 so prikazani rezultati teh meritev. V tabeli 2 so prikazani rezultati eksperimenta pri popolnem odklapljanju bremenskih uporov.

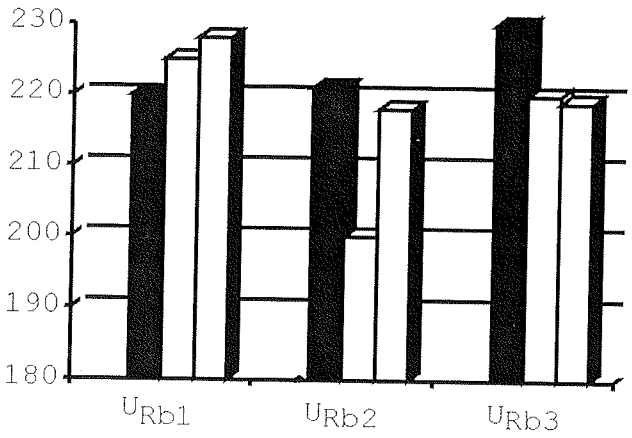
5. Zaključek

Pri pretvorbi enofaznega napetostnega sistema v trifazni napetostni sistem je bila uporabljena Parkova transformacija. Pretvorba je bila izvedena v transformatorskem jedru. Zaradi tega je bilo število elektronskih komponent, tako v energetskem, kakor tudi v krmilnem delu, zelo zmanjšano glede na klasični način pretvorbe. Klasični tovrstni pretvornik vsebuje usmerniško vezje, enosmerni povezovalni krog (velik elektrolitski kondenzator) in trifazni razsmernik.

Pretvornik je pokazal tudi veliko mero neobčutljivosti na spreminjanje obremenitve na izhodu, kakor tudi na nesimetrično obremenitev trifaznega izhoda.

Tabela 1: Zmanjšanje bremenske upornosti iz 500Ω na 250Ω

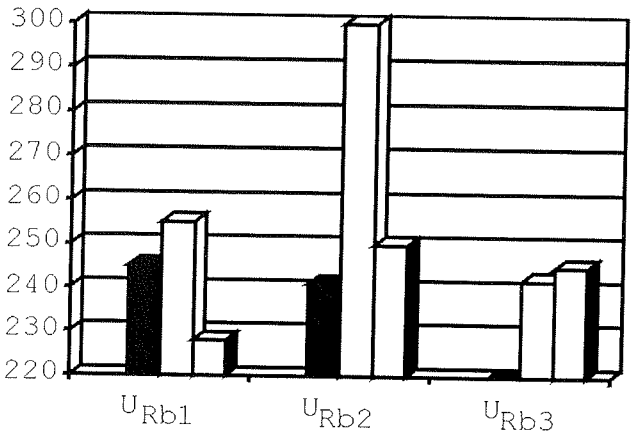
	U_{Rb1}	U_{Rb2}	U_{Rb3}
R_{B1} iz 500Ω na 250Ω	220	221	230
R_{B2} iz 500Ω na 250Ω	225	200	220
R_{B3} iz 500Ω na 250Ω	228	218	219



Slika 6: Grafični prikaz rezultatov iz tabele 1

Tabela 2: Razbremenitev posamezne faze pri $R_B = 500\Omega$

	U_{Rb1}	U_{Rb2}	U_{Rb3}
R_{B1} iz 500Ω na ∞	245	241	218
R_{B2} iz 500Ω na ∞	255	>300	242
R_{B3} iz 500Ω na ∞	228	250	245



Slika 7: Grafični prikaz rezultatov iz tabele 2

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HITRA KALIBRACIJA FLIKERMETRA ZA PRAVILNO OCENO KAKOVOSTI NAPETOSTI PO EN 50160

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Ključne besede: elektrotehnika, energija električna, EES sistem elektroenergetski, kakovost napetosti električne, merjenje kakovosti, flikermetri, kalibriranje, ocena kakovosti, IEC 60868-0 standardi ,EN 61000-4-15 standardi, EN 50160 standardi

Izvleček: Skladno z našo regulativo je SIQ pooblaščena organizacija za izdajanje certifikatov o ustreznosti merilne opreme. To nalogo večinoma tudi uspešno opravlja, za nekatere redke meritve pa ji manjka zelo draga preskusna oprema. V teh primerih bi morali spremeniti naše zakone in dovoliti SIQ-u nostrifikacijo certifikatov tujih pooblaščenih zavodov - predvsem tistih iz EU. Eden takšnih preskusov je preverjanje delovanja flikermetra skladno z IEC 60868-0 in EN 61000-4-15.

Ko smo v Laboratoriju za energetiko UM FERI zaznali razhajanje merilnih rezultatov paralelno priključenih flikermetrov (večina je pokazala prevelike vrednosti), smo sestavili generator s standardom zahtevanih sprememb napetosti in kalibrirali instrument, ki ima certifikat nemškega pooblaščenega laboratorija Forschungemeinschaft für Hochspanungs- und Hochstromtechnik E.V. Pri nivoju P_{ST} = 1, ni bilo razhajanja med v standardu zahtevano in dejansko izmerjeno vrednostjo. Tako lahko sklepamo, da imamo v našem omrežju, glede na flikerje, boljšo kakovost napetosti, kot jo izmerijo instrumenti, ki so na trgu v Sloveniji.

Quick Flickermeter Calibration for the Estimation of Voltage Quality by En 50160

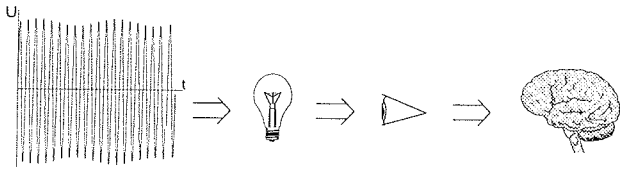
Key words: electrotechnics, electric energy, electrical power system, quality of electrical tension, quality measurement, flicker meters, calibration, quality estimation, IEC 60868-0 standards, EN 61000-4-15 standards, EN 50160 standards

Abstract: SIQ is, regarding technical regulations in Slovenia, authorized organization for certification of accordance of measuring devices. This is pretentious task and SIQ is performing it fairly well, although there are some instances that require special equipment, which is too expensive for SIQ to afford it. Such cases indicate that we should amend the law in question and allow SIQ to nostrificate the certificates of the foreign authorized institutions - at least the EU ones. One of such test is proof of flickermeter functionality in accordance to IEC 60868-0 and EN 61000-4-15 standards.

In Power engineering laboratory at University of Maribor, FERI, we have made some comparative analysis of flickermeter measuring equipment and became aware of noticeable deviation of measuring results. Tests were performed with parallel connected equipment and most of instruments indicate somewhat too high values, therefore we generate series of voltage fluctuation as demand by standard and calibrated the instrument, which has certificate of the German authorized laboratory "Forschungemeinschaft für Hochspanungs- und Hochstromtechnik E.V." We have checked the level of flicker P_{st} = 1 and found that the measured values are in accordance with the ones prescribed with the standards. This leads us to conclusion that, regarding to flicker levels in Slovenian network, we have better voltage quality than measured by instruments, attainable in Slovenia.

1 Uvod

Fliker je subjektivni občutek, ki ga povzročajo spremembe svetlosti v vidnem polju opazovalca. Večinoma povzroča takšne spremembe kolebanje napetosti, saj so nanj žarnice zelo občutljive. Meritev flikerja temelji na človeških psiho-vizualnih občutkih, ki jih je treba ovrednotiti. Osnovna ideja za merjenje flikerjev je simulacija verige: žarnica-oči-možgani (slika 1) z merilnikom (flikermetrom), katerega vhodni signal je nihajoča napetost sistema v priključni točki. Izhodni signal je veličina, ki pomeni občutek neugodja večine ljudi zaradi migotanja svetlobnega toka.



Slika1: Simulacija verige: omrežje-žarnica-oči-možgani

2 Razlog za primerjalni test in njegova izvedba

Osnovni pogoj za kakovostno meritev je dobra merilna naprava. Kvaliteto merilne naprave navede že proizvajalec, potrdi jo pa kalibracija. Takšno pot smo poizkusili narediti tudi z našim flikermetrom. Razvil ga je prof. dr. Manfred Sakulin (Institut für elektrische Anlagen, TU Graz), ki zagotavlja, da je naprava v skladu z DIN VDE 0846 T2, kar potrjuje poročilo nemškega neodvisnega akreditiranega laboratorija Forschungemeinschaft für Hochspanungs- und Hochstromtechnik E.V./8/.

Žal takšno potrdilo pri nas ne velja, čeprav je slovenski standard SIST EN 61000-3-2:1997 omenjenemu standardu DIN enak, saj oba izhajata iz IEC 1000-3-2:1995. Zakon o meroslovju priznava le slovenske ateste. Zato smo poizkusili dobiti atest pri Slovenskem inštitutu za kakovost. Tam so umerjanje opravili, vendar v opombah poročila napisali: "Negotovost merilne metode je bila enakega velikostnega razreda ali večja kot je relativni mejni pogrešek

merila. Zato je v nekaterih primerih relativni pogrešek merila večji kot je relativni mejni pogrešek."

To torej pomeni, da SIQ nima primerne opreme za kalibracijo flikermetrov /9/.

V zadnjih nekaj letih se je na našem tržišču pojavilo kar nekaj različnih flikermetrov, ki seveda nimajo slovenskega atesta, zato smo se odločili, da naredimo primerjalno meritev.

Od različnih trgovcev in proizvajalcev smo dobili še šest med seboj različnih flikermetov. Priključili smo jih na 0,4kV zbiralke v transformatorski postaji 10/0,4 kV št. 337 Tehniških fakultet v Mariboru.

Meritev smo izvedli med 19. 6. in 26. 6. 2000, kar je sicer čas poletnih počitnic, vendar je bilo omrežje kljub temu dovolj nemirno, da smo izmerili nivo kratkotrajnega flikerja $P_{ST,95} \approx 0,6$.

3 Rezultati primerjalne meritve

Že pri zagonu instrumentov so se pojavile prve težave. Eden od izposojenih flikermetrov ni bil popoln. Manjkal je osebni računalnik, kar bi se še dalo urediti, vendar je bil brez ustrezne programske opreme. Kljub dogovarjanju s proizvajalcem, ga nismo uspeli usposobiti za celotedensko meritev. Ostalih šest je začelo meritev brez večjih problemov in tudi trenutni rezultati (trenutne vrednosti P_{st}) so bili v pričakovanih mejah.

Po enem tednu, kolikor takšna meritev traja po standardu SIST EN 50160, smo morali rezultate zaradi obdelave in analize prenesti na osebni računalnik. Pri tej operaciji je izpadel še en flikermeter, saj izmerjenih rezultatov nismo mogli prenesti in pripraviti za obdelavo.

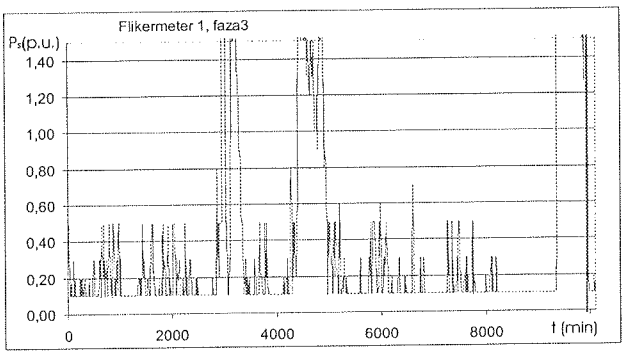
Tabelarični izpis rezultatov je zahteval nove "žrtve". En flikermeter je v vseh treh fazah in za celotni čas meritve zabeležil enake vrednosti. Drugi je v dveh fazah sicer nekaj izmeril, vendar samo na eno decimalno mesto natančno, v tretji fazi pa vedno shranil enako (negativno!) vrednost. Tako so rezultati slednjega ostali le pogojno uporabni.

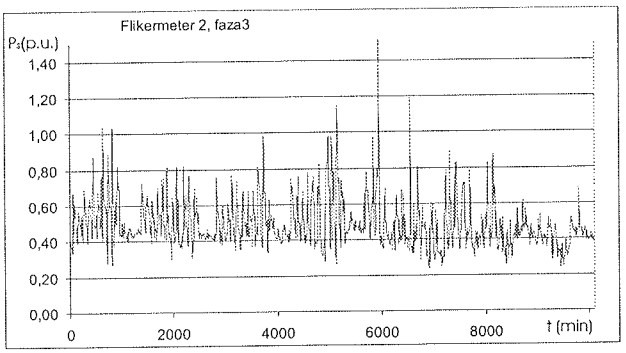
Iz preostalih treh, vključno z našim, smo uspeli dobiti smiselne rezultate. Časovni potek P_{st} kaže, da so flikermetri zaznali kolebanje napetosti v enakih obdobjih, le različno so jih ovrednotili (slika 2). Še lepše je to razvidno iz urejenega diagrama (slika 3). Najpomembnejše so vrednosti v 95 in 99% časa, ki znašajo:

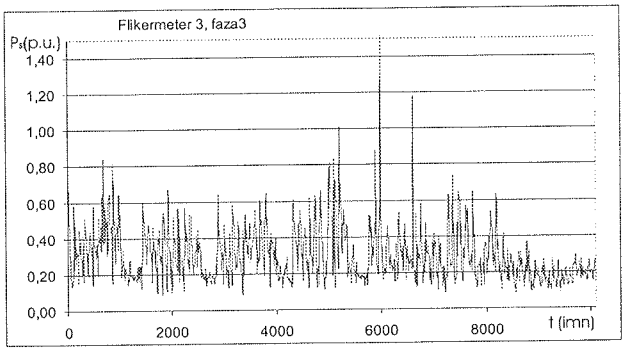
Preglednica 1: Vrednosti P_{st} za 95 in 99% časa

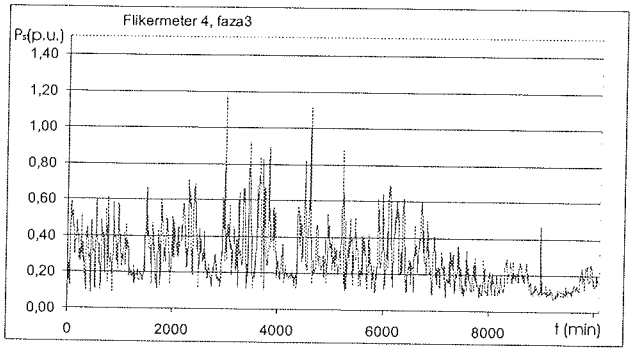
	FM 1	FM 2	FM 3	FM 4
$P_{st,95}$ (faza L1)	0,70	0,54	0,55	-
$P_{st,95}$ (faza L2)	0,77	0,58	0,56	0,3
$P_{st,95}$ (faza L3)	0,76	0,58	0,59	0,2
$P_{st,99}$ (faza L1)	0,91	0,80	0,73	-
$P_{st,99}$ (faza L2)	0,92	0,72	0,72	0,5
$P_{st,99}$ (faza L3)	0,94	0,73	0,72	4,1

Ugotovimo lahko, da se rezultati meritev dveh flikermetrov lepo ujemajo, dočim rezultati meritev drugih dveh močno odstopajo. Žal so štirje oz. trije rezultati premalo, da bi lahko naredili Gaussovo porazdelitev in ocenili najverjetnejšo vrednost, zato smo se odločili, da sami preverimo delovanje našega flikermetra skladno s publikacijo UIE (Union International for Electro-heat): Flicker Measurement and Evaluation, ki jo je prevzel tudi IEC v svoji publikaciji IEC 868, s hitro, poenostavljeno kontrolno meritvijo.

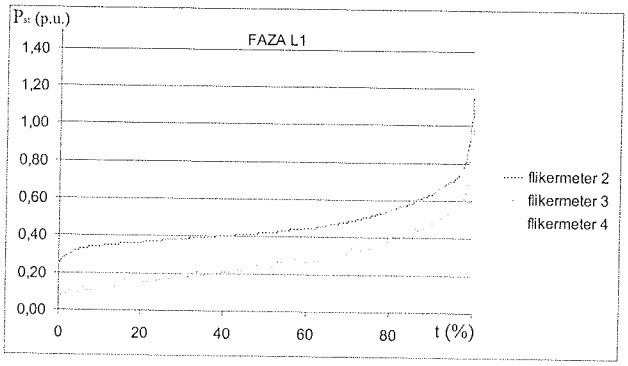


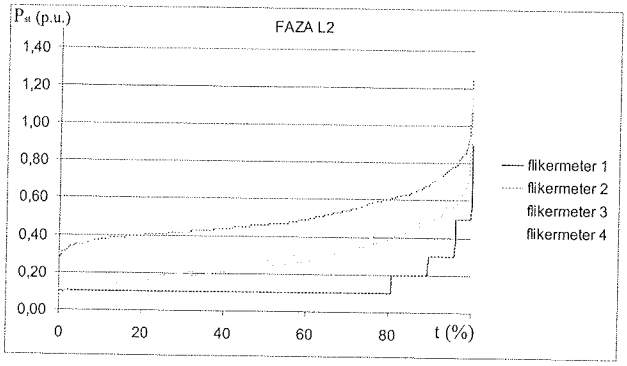


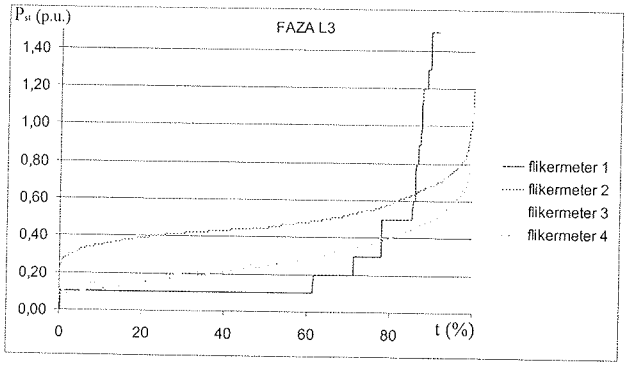




Slika 2: Časovni diagrami poteka P_{st} za različne flikermetre v fazi L3





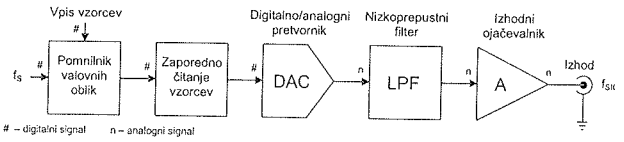


Slika 3: Urejeni diagrami poteka P_{st} za različne flikermetre v vseh treh fazah

4 Kontrola delovanja flikermetra

Območje efektivnih vhodnih napetosti flikermetra je običajno 40 do 480 V. Generator, sposoben generirati testni signal amplitude, večje od 40 V, nam ni bil dostopen. Od proizvajalca smo izvedeli, da ima flikermeter skladno s standardom na vhodu uporovni napetostni delilnik, ki prilagodi vhodno napetost na nivo 0 do ±5V. Za ta napetostni obseg smo realizirali generator testnega signala. Izhodno napetost generatorja smo nato prilagodili nizkonapetostnemu vhodu merilnika.

Zaradi zahtev, ki jo mora tak izvor signala izpolnjevati, smo uporabili generator zgrajen na osnovi delovanja generatorja poljubnih valovnih oblik (AWG - Arbitrary Waveform Generator). Blokovni diagram merilnega sistema prikazuje slika 4.



Slika 4: Generator poljubnih valovnih oblik

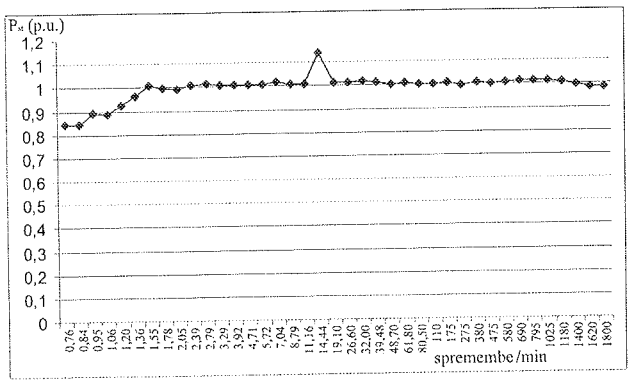
V bistvu je AWG prefinjen sistem za ponovno generacijo različnih valovnih oblik na osnovi shranjenih digitalnih podatkov oziroma vzorcev, ki opisujejo nenehno spreminjanje nivoja signala. Vzorce bi tako lahko dobili iz osciloskopa z digitalnim vzorčenjem na katerega je priključen primeren signal ali pa s pomočjo grafičnih in matematičnih operacij in tehnik. Uporabili smo slednjo metodo, ker so testni signali za P_{ST}=1 po IEC 868 že sami po sebi matematično določeni. Izračun valovnih oblik je potekal z 32-bitno natančnostjo, končni rezultat pa zaokrožen na 16 bitov kolikor jih ima uporabljen D/A pretvornik. Vertikalna ločljivost izraža napetostno negotovost vzorcev in je za 16-bitni AWG, ki nudi 65536 nivojev napetosti prek celega napetostnega področja, reda 0,002% (ξ = 96 dB). Tako prekaša vsak analogni izvor sinusnega signala glede harmonične popačitve ter stabilnosti napetosti, frekvence in faze.

Mnogo višja frekvenca vzorčenja (f_S = 8 kHz) od testnega signala (f_{SIG} = 50 Hz) nam omogoča vernejšo rekonstrukcijo testnega signala še pred nizkopasovnim filtranjem na izhodu. Vsako periodo testnega signala tako opisuje 160 vzorcev. Potrebna globina pomnilnika AWG je sorazmerno velika, saj period signala ne ponavljamo, kot je to pri AWG običajno, temveč izračunamo testni signal v celotni dolžini. Za simuliranje nižjih frekvenc kolebanja tako uporabljamo signal dolžine 30-tih minut, kar pomeni 14,4 milijona vzorcev. Korist, ki jo imamo od tega, je odprava mejnih točk. Te bi namreč privedle do neizogibnih napak, ki bi nastale pri prehodu, te pa močno vplivajo na meritev. Skupni čas vseh 45-tih testnih signalov tako znaša 13 ur in 15 minut (381,6 milijona vzorcev), kar je zato tudi čas popolne „hitre" kalibracije flikermetra. Za v bodoče bi mogoče kazalo

uporabiti še kakšen „bolj strog" test s pomočjo namenoma popačenega osnovnega signala, kar smo v tem primeru izpustili iz objektivnih razlogov.

Parametre testnih signalov navaja standard IEC 60868-0. Testni signal je sinusna napetost frekvence 50 Hz, ki je amplitudno modulirana z napetostjo sinusne ali pravokotne oblike. Standard navaja amplitude in frekvence superponiranih napetosti. Za vsak testni signal mora flikermeter izmeriti vrednost P_{st} = 1(±10%).

Slika 5 prikazuje, da je pogrešek flikermetra le pri zelo nizkih frekvencah (do 1 spremembe na minuto) večji od dopustnih 10%.



Slika 5: Odziv našega flikermetra na testni signal

5 Sklep

Flikermeter je merilni instrument, s katerim želimo ovrednotiti dve nelinearni fiziološki funkciji; občutljivost človeških oči in odziv možganov na sprejeto informacijo. Merimo spreminjanje - kolebanje napetosti, vgrajeni filtri in statistika, ki simulirajo naše psiho-fiziološke odzive in občutke, pa so narejeni z računalniškimi programi.

Kot rezultat primerjalnih meritev ocenjujemo, da so vsi flikermetri pravilno izmerili efektivno napetost, programska oprema večine instrumentov pa se je pokazala kot nezanesljiva.

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POVEZAVA MERILNIH SIGNALOV IN MATLABA PREKO PROCESNEGA STREŽNIKA

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Ključne besede: okolja industrijska, okolja raziskovalna, procesi proizvodni, avtomatizacija, signali merilni, strežniki procesni, PLC krmilniki logični programirljivi, povezave, MATLAB oprema programska simulacijska, SCADA krmiljenje nadzorno in zajemanje podatkov, merjenje, optimiranje, komunikacije v času realnem, OLE vgraditev in povezava objektov, OPC OLE krmiljenja procesov

Izvleček: Sodobni sistemi za avtomatizacijo proizvodnih procesov uporabljajo industrijsko testirane, na tržišču dostopne ter uveljavljene proizvode kot so senzorji, aktuatorji, krmilniki (PLC - Programmable Logic Controller) in SCADA (Supervisory Control and Data Acquisition) sistemi. Le-ti zagotavljajo zanesljivo in varno delovanje proizvodnega procesa. Takšni sistemi so zelo omejeni glede na možnosti raziskav, optimizacije, testiranja in simulacije, kar pa omogočajo sistemi, znani iz raziskovalnega okolja. Povezava takega industrijskega okolja s prožnim, a nestabilnim raziskovalnim okoljem je osnovni cilj predstavljenega dela. Za povezavo industrijskega sistema z Matlab/Simulink programom je bila uporabljena OPC tehnologija, ki je pogosto sestavni del sistemov industrijske avtomatizacije in je tam že dobro uveljavljena. OPC je okrajšava za OLE for Process Control, kjer je OLE oznaka za Microsoftovo tehnologijo Object Linking and Embedding. Uporaba Matlab simulacijskega programa in njegovih orodij omogoča veliko prožnost pri raziskavah, analizah in optimizaciji, kar v današnjih SCADA sistemih ni zagotovljeno. V testnem sistemu je strežnik zajemal podatke iz krmilnika, preveril kvaliteto in morebitno spremembo vrednosti podatkov ter jih posredoval odjemalcu, ki jih je po obdelavi poslal nazaj po isti poti. Za namene "worst case" testiranj se je uporabilo sinhrono branje, kjer se je vsak podatek vsakič spremenil, na istem računalniku pa so tekli en strežnik, dva odjemalca, SCADA ter Matlab program. Bistvena prednost predstavljene rešitve je integracija računskih, simulacijskih ter grafičnih zmogljivosti Matlaba z robustnostjo industrijskega sistema. Rešitev je univerzalna, omogoča sprotno obdelavo podatkov in dostop do podatkov drugim programskim orodjem, ne da bi pri tem fizično posegali v industrijski sistem za avtomatizacijo.

Connection Between Measurement Signals and MATLAB Using Process Server

Key words: industrial environments, research environments, fabrication processes, automation, measurement signals, process servers, PLC, Programmable Logic Controllers, connections, MATLAB simulation software , MATrix LABoratory simulation software, SCADA, Supervisory Control And Data Acquisition, measurements, optimization, real-time communications, OLE, Object Linking and Embedding, OPC, OLE for Process Control, Object Linking and Embedding for Process Control

Abstract: The automation of processes has reached the point where one cannot go without applying sensors, actuators, PLC (Programmable Logic Controllers) and SCADA (Supervisory Control and Data Acquisition) systems that enable acquisition of large quantities of data. The process automation is particularly important in isolated rooms where physical presence of humans is undesirable, as for example in the production of electronic components or in the pharmaceutical industry. Such manufacturing systems operate with various degrees of success and are not modified very often. Every alternation of any industrial process is followed by extensive documenting, testing and validating of the new system. Quite often the production must be stopped which gives a rise to substantial costs for entire operation. On the other hand there are a number of research laboratories where various approaches are constantly a subject to change, development and testing in order to bring about improvements. The research work often implements mathematical and simulation software such as Matlab (Matrix Laboratory) which enables solving of complex mathematical operations, simulations, optimisations, etc. However, their main disadvantage is that they are substantially limited in their connectivity to other systems and applications. Manufacturing processes include many procedures where large amounts of data could be processed, examined and optimised: regulation loops, optimal production structuring, calculation of illumination in various points, etc. The equipment that is used in the industry, such as PLC and SCADA, is not suitable for performing such data processing. Instead, Matlab would be much better if only it were possible to feed it with real-time data from the manufacturing process. By applying this technology a wide spectrum of possibilities for testing and analysis emerges which can contribute to the improvement of the process. The system can also be upgraded to perform a real-time parallel optimisation procedure. In this configuration the manufacturing process would be running independently whereas Matlab would be performing in parallel all the necessary mathematical operations, the results of which would be fed back into the process. There are two difficulties in implementing such real-time connections: the problem of connectivity and the difficulty of presenting a universal solution enough that would not require altering our existent manufacturing systems, especially when new research requires updating or changing our existing configurations. One possible solution would be to use the OPC standard and the associated technology. OPC means OLE for Process Control (OLE - Object Linking and Embedding) and represents an international industrial standard (Specifications v.1.0a) that is based on the Microsoft's OLE/COM/DCOM technology. It provides a unified communication interface based on Plug&Play between various devices of process control. The OPC interface thus belongs to one of the new technologies applied to connecting and interfacing systems of process control which is based on the component technology. The main properties of the component technology can be summarised by the properties of OLE automation which enable that one application can contain objects from other applications, the linking of both applications results in data being simultaneously updated in both, and non-native objects can be executed or changed inside the application where they are embedded. In the usual systems of process control each SCADA software has to have its own piece of software code in order to be able to communicate with the kernel of the I/O driver or with any other part of the software code that is used to communicate with the I/O unit. In other words: each SCADA system needs drivers in order to be able to communicate with other devices and each device connected to the system must have its own driver. If a system is connected to another SCADA system then this system needs its own drivers again for all the devices that will communicate with it and that are connected to it. The number of required drivers can be calculated by multiplying the number of I/O units with the number of SCADA packets. The result is a very high number and thus an inelegant solution. As a solution, the OPC creates a 'software bus' where applications only need to be aware on how to access data on the OPC. Testing system consisted of an OPC server which captured data from the

controller, it checked the data's quality, evaluated it for a change of state, and then forwarded it to the OPC client who returned it along the same route once it was processed. For the 'worst case' scenario synchronous reading was used where each piece of data was changed every time and the same computer ran a server, two clients, as well as the SCADA and Matlab software. The measurements performed show that due to the fixed dead time the worst results are obtained when transferring a single piece of data only. The results show a rate of approximately 1000 pieces of data per second can be expected with large quantities of data. The process data is available to Matlab virtually at the same time as to the SCADA system which makes the application suitable for industrial environments. The proposed solution is especially suitable for manufacturing processes with slower rates of change since here it can also be used for process control. Main advantages of proposed solution are the integration of the numerical, computational and graphical powers of MATLAB® with the robustness of industrial system, universality, on-line data processing and accessibility to other software programs, without any physical connection or disturbance of the manufacture automation system.

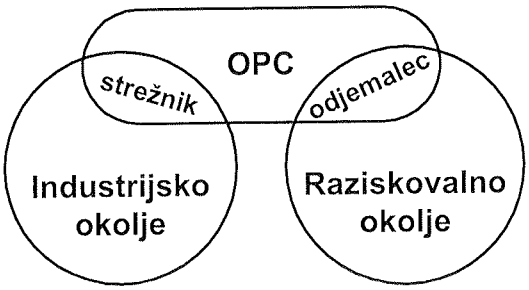
1. Uvod

Proizvodnja je dandanes avtomatizirana do te mere, da si je več ne znamo predstavljati brez obilice senzorjev, aktuatorjev, krmilnikov (PLC - Programmable Logic Controller) ter SCADA (Supervisory Control and Data Acqusition) sistemov /12/, ki omogočajo veliko število informacij. Prav posebej visok nivo avtomatizacije je v procesih, ki potekajo v t.i. čistih prostorih, v katerih je fizična prisotnost ljudi nezaželjena, kot je to primer pri proizvodnji elektronskih komponent /21/ ali zdravil. Ti sistemi v proizvodnih procesih bolj ali manj uspešno delujejo in se predvsem ne spreminjajo prepogosto /19/. Vsak poseg v proizvodni proces je namreč povezan vsaj z obširnim dokumentiranjem, testiranjem ter validiranjem, tudi s strani certifikacijskih organizacij, kot sta npr. ISO (International Standard Organization) ter FDA (Food and Drug Administration), če ne tudi z zaustavitvijo proizvodnje, kar ima za posledico velike skupne stroške posega /20/.

Na drugi strani pa je svet raziskovalnih laboratorijev, ki je podvržen nenehnim spremembam, razvoju ter testiranjem različnih pristopov v smeri izboljšav. V raziskovalno okolje so velikokrat vključeni tudi matematični in simulacijski programi kot je Matlab (Matrix Laboratory), ki omogoča reševanje zahtevnih matematičnih operacij, simulacije, optimizacije itd., vendar imajo omejene možnosti povezovanja /18/.

V proizvodnem procesu je veliko postopkov s podatki, ki so zanimivi za obdelavo, raziskave ter morebitno optimiranje: od regulacijskih zank, optimalnega razvrščanja proizvodnje pa do npr. izračunavanja osvetlitve v posameznih točkah. Zaradi velike matematične zahtevnosti omenjenega že instalirana oprema (krmilniki in SCADA) za tovrstne operacije ni primerna, primeren pa je Matlab /10/, v katerega je potrebno sprotno prenašati podatke iz proizvodnega procesa. Z uporabo takšne rešitve se kaže širok spekter možnosti testiranj ter analiz v smeri izboljšanja delovanja procesa, kar se lahko nadgradi tudi s sprotnim paralelnim optimizacijskim postopkom, kjer industrijski proces teče samostojno, hkrati pa se paralelno v Matlabu izvajajo potrebne matematične operacije, katerih rezultati se sporočajo nazaj v proces. Pri implementiranju On-line povezave je zraven problema povezljivosti prisotna tudi problematika univerzalnosti rešitve ter predvsem nespreminjanja obstoječega industrijskega sistema tudi v primeru morebitnih dopolnitev ali sprememb na raziskovalnem nivoju.

Možna rešitev je uporaba OPC standarda /22/ in tehnologije, ki je s tem povezana. OPC je okrajšava za OLE for Process Control, kjer je OLE oznaka za Microsoftovo tehnologijo Object Linking and Embedding.V članku je predstavljena rešitev, v kateri se znotraj okolja Matlab uporabi OPC odjemalec, ki izmenjuje podatke z že obstoječim OPC strežnikom na nivoju povezave PLC-SCADA, kar je prikazano na sliki 1. OPC se zmeraj bolj uporablja v sistemih industrijske avtomatizacije /12/ /14//1//3//2/, prav razširjenost uporabe pa daje rešitvi potrebno univerzalnost.



Slika 1: Uporaba OPC za povezavo industrijskega in raziskovalnega okolja

V naslednjih poglavjih bo predstavljeno nekaj pogosteje uporabljanih tehnik za On-line matematično analizo procesnih podatkov, povzete glavne lastnosti OPC in predstavljena zasnova in izvedba povezave Matlaba z industrijskim krmilnikom, skupaj z rezultati eksperimenta. V zaključku je podana analiza z povzetkom glavnih lastnosti takega pristopa, podane pa so tudi smernice za nadaljevanje dela.

2. Nekaj do sedaj uporabljanih rešitev za On-line matematično analizo procesnih podatkov

Uporaba možnosti vključevanja lastnih programov v enem višjih programskih jezikov, kar ponuja večina SCADA programov, je na prvi pogled enostavna rešitev za dodatno matematično obdelavo. Težave se lahko pojavijo pri programiranju zahtevnih matematičnih operacij.

Ena pogosteje uporabljanih rešitev za zajem realnih podatkov v Matlab je uporaba posebnih PC I/O modulov /4/, /9/, ki jih podpira Matlab (npr. Burr-Brown ali National Instruments). Prednost takšne povezave je zraven produktne usklajenosti predvsem hitrost operiranja z podatki, ki je lahko manjša od 1 ms/podatek. Vendar pa gre za tipično laboratorijsko opremo, ki se jo v proizvodnih procesih sreča

le redko, kar pomeni zraven nakupa strojne opreme še težave pri implementiranju le-te v sam proizvodni proces. Takšno kartico je potrebno fizično povezati na obstoječo senzoriko in sicer vzporedno ali zaporedno s krmilniško opremo, kar pomeni že omenjene težave v povezavi s stroški zaustavitve proizvodnje, dokumentiranjem ter validiranjem. Poudariti je potrebno, da je težav z izvedbo takšnega posega ni, ko so cilji ter rezultati posodobitve natančno definirani, do česar pa je zopet težko priti brez Online testiranj ter prezentiranja rezultatov na dotičnem procesu. Podobna je rešitev z uporabo merilnih instrumentov z možnostjo GPIB ali VISA komunikacije, ki jo podpira tudi Matlab.

V Matlabu je omogočen dostop do serijskega vodila, kar ponuja možnost izdelave lastnega API (Application Programming Interface), ki »prisluškuje« prometu po mreži krmilnikov in po potrebi tudi pošilja podatke. Prednost takšne ideje je, da ne poseže direktno v proces. Pomanjkljivost je časovno zahtevna izdelava vmesnika za industrijsko vodilo ter neuniverzalnost rešitve /10/.

Za obravnavano problematiko so se rešitve zmeraj bolj nagibale proti programskim rešitvam, ki ponujajo bolj izmenjavo podatkov kot pa dodatno zajemanje podatkov, saj se meritve tako ali tako kontinuirano opravljajo za potrebe krmilnikov in SCADA in zato ni potrebno podvajanje. Najenostavnejša izmenjava podatkov je mogoča preko ASCII datoteke, v katero vpisujeta oba, SCADA in Matlab. Rešitev je v omejenem obsegu univerzalna, vendar so potrebni posegi v SCADA program, pa tudi prenos ni hiter.

S pomočjo OLE (Object Linking and Embedding) je mogoča povezava Matlaba z MS Excelom, kar omogoča standardni Matlabov Toolbox Excel Link. Excel podpira DDE (Dynamic Data Exchange), ki ga podpirajo tudi SCADA sistemi, kar ponuja možnost povezave, ki je med bolj univerzalnimi, vendar se DDE na področju procesnega vodenja nikoli ni povsem uveljavil zaradi neučinkovitosti in nezanesljivosti pri prenašanju velikih količin podatkov /5/. Dodatna težava omenjenega pristopa je potreben poseg v SCADA sistem, iz katerega je potrebno pošiljati DDE podatke (ob predpostavki, da SCADA ne bazira na DDE). Tak poseg pomeni spremembo funkcionalnosti in s tem potrebo po validacijskem postopku.

Uporaba OPC (OLE for Process Control) za izmenjavo podatkov med Matlabom in industrijskim procesom predstavlja logično nadaljevanje predstavljenih tehnik in je opisana v nadaljevanju.

3. OPC

3.1. Uvod

Za kratico OPC se skriva ime OLE for Process Control (OLE - Object Linking and Embedding) in predstavlja mednarodni industrijski standard (specifikacija v1.0a), ki temelji na Microsoftovi OLE/COM/DCOM tehnologiji in zagotavlja skupen komunikacijski plug&play vmesnik med različnimi napravami na področju procesnega vodenja. OPC vmesnik je ena izmed novih tehnologij pri povezovanju in komunikaciji v sistemih procesnega vodenja, ki temelji na komponentni tehnologiji. Osnovna načela komponentne tehnologije se lahko opišejo s principi OLE avtomatizacije, ki določajo možnost, da ena aplikacija vsebuje objekt iz druge aplikacije, da preko povezovanja prihaja do osveževanja podatkov med njima ter da je možno objekte spreminjati in poganjati znotraj aplikacije, ki jih vsebuje.

3.2. Problem povezljivosti v sistemih procesnega vodenja

V običajnih sistemih procesnega vodenja potrebuje vsaka SCADA programska oprema lasten kos programske kode za komunikacijo z jedrom I/O gonilnika oz. tistim delom programske kode, ki zna komunicirati z I/O enoto /14/. Če se poenostavi: vsak SCADA sistem potrebuje za komunikacijo z napravami gonilnike, ki jih je toliko, kot je naprav priključenih na sistem. Če se sistem povezuje z drugim SCADA sistemom, potrebuje ta sistem zopet svoje gonilnike za vse naprave s katerimi bo komuniciral in ki so priključene na ta sistem. Izračuna se lahko, koliko različnih gonilnikov je potrebno, tako da se pomnoži število I/O enot s številom SCADA paketov; rezultat pa je zelo visoka številka ter nepraktična rešitev. Tovrste povezave SCADA sistemov v celoto se zato izvedejo večinoma le znotraj istih proizvajalcev procesne in programske opreme (Siemens, GE, Omron...).

OPC vmesnik se v kos programske kode za komunikacijo z jedrom I/O gonilnikov ne poglablja, saj se z njimi v večini primerov ukvarjajo protokoli na nižjem nivoju kot so FieldBus, DeviceNet, Profibus, LonWorks /11/. Problem je, da vsak gonilnik uporablja svoj vmesnik za komunikacijo s periferno napravo oziroma aplikacijo, kar onemogoči več aplikacijam hkrati komunicirati z isto periferno napravo. OPC pa v nasprotju z opisanim ustvari t.i. programsko vodilo (»software bus«), kjer morajo aplikacije, oz. programerji aplikacij, vedeti samo kako dostopati do podatkov na OPC programskem vodilu, ki jih posredujejo periferne naprave. Aplikacije so tako preprostejše, manjše in enostavnejše za uporabo. Gonilniki perifernih naprav (OPC strežniki) morajo tako samo znati prenašati informacije iz perifernih naprav na OPC vodilo v določenem formatu.

Vendar univerzalnost prenosa podatkov ni edina prednost, ki jo ponuja OPC vmesnik. Prvotno namenjen reševanju problematike I/O gonilnikov, se je OPC vmesnik izkazal dovolj fleksibilen, da se poleg povezovanja perifernih naprav s SCADA sistemi uporablja tudi pri povezovanju z aplikacijami »višje navzgor« vse do sistemov poslovnega odločanja.

3.3. Tehnologija OPC vmesnika

Povezovanje z OPC vmesnikom se vrši s pomočjo programskih vmesnikov, ki temeljijo na COM (Component Object

Model) tehnologiji, različna vodila, kot sta Fieldbus in Profibus, pa se ukvarjajo s fizično in mrežno povezavo. COM je Microsoftova osnova za pisanje API-jev (Aplication Programming Interface). Ob upoštevanju, da je zelo široko uporabljena, omogoča tudi zelo dobro navpično povezovanje, kjer je potrebno povezati OPC strežnik ter OPC odjemalec, ki je običajno že integriran v samem SCADA sistemu. To vključuje tudi DCOM tehnologija (Distribuirani COM), ki omogoča ustvarjanje aplikacij, ki temeljijo na mrežnem povezovanju. Še najbližje takšni strukturi prenosa podatkov se je približal DDE vmesnik, vendar se na področju procesnega vodenja nikoli ni povsem uveljavil zaradi neučinkovitosti in nezanesljivosti pri prenašanju velikih količin podatkov. Mnogi proizvajalci programske opreme so raje uporabljali lastne API-je, kot pa DDE vmesnik za prenos procesnih podatkov iz periferne enote v programsko opremo ali iz ene v drugo programsko opremo.

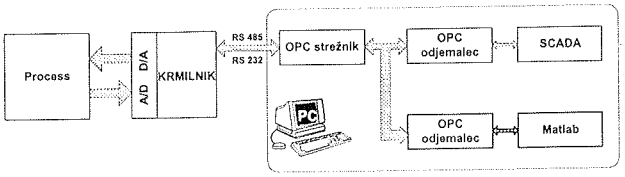
OPC je dovolj fleksibilen za delovanje v različnih plasteh sistemov, kot tudi dovolj dober za uporabo preko mreže. Učinkovitost OPC vmesnika je zagotovljena, saj lahko le-ta prenaša na stotine in tisoče podatkov z eno transakcijo, kar DDE ne omogoča. Vsaka transakcija lahko vključuje še mnogo različnih spremenljivk. Tako je vsaka transakcija OPC vmesnika sestavljena iz podatka, časovne znamke podatka ter informacije o kvaliteti podatka. Z DDE vmesnikom bi se za to potrebovale tri transakcije. OPC strežniki so lahko integrirani v samem procesu, lahko so lokalni (Local) ali pa so daljinski (Remote). Glede na učinkovitost prenosa podatkov je zelo pomembno kje se nahaja OPC strežnik, saj omogoča v prvem primeru (v procesu) milijon transakcij na sekundo, v drugem (Local) okoli tisoč in v tretjem (Remote) okoli sto.

Ponujena je tudi možnost, da lahko proizvajalci oz. programerji ustvarijo in/ali nadgradijo enostaven in učinkovit gonilnik, ki podpira delovanje s perifernimi napravami ne glede na proizvajalca. S tem je omogočeno, da OPC strežnik univerzalno prenaša real-time podatke procesnih spremenljivk kot so temperatura, tlak, pretok, pozicija, hitrost, itd. Zajem podatkov je možno še poenostaviti, saj OPC aplikacija dovoljuje definiranje ene ali več »skupin« (Groups), v katerih se potem nadzirajo posamezne želene spremenljivke. OPC odjemalec, ki je odjemalec podatkov iz OPC vodila in posrednik podatkov v SCADA sistem lahko potem izvaja sinhrono ali asinhrono branje podatkov želenih spremenljivk v skupini.

Poudarjene funkcije pri povezovanju in komunikaciji z OPC vmesnikom so zraven on-line dostopa do podatkov (On-line Data Access) še upravljanje z alarmi in dogodki (Alarm and Event Handling), beleženje podatkov (Historical Data Access), zaščita dostopa (Security) in prenos podatkov pri šaržnih procesih (Batch). Zadnji dve specifikaciji sta še v fazi dogovorov, razvoja in standardizacije, v fazi zaključnih dogovorov pa so specifikacije za področje OPC XML ter nova specifikacija OPC Data Access 3.0 /23/.

4. Izveden eksperiment

Z matematičnim orodjem Matlab smo v okolju Simulink zgradili testno okolje za eksperiment, katerega cilj je bil realizirati On-line prenos procesnih podatkov v Matlab iz klasičnega industrijskega krmilnika (slika 2). Zajem podatkov v Matlab je sicer mogoč s pomočjo posebnih I/O računalniških kartic, kar pa je rešitev, ki večinoma v realnih industrijskih sistemih ni mogoča. Razlogi tičijo v že instalirani opremi, (ne)robustnosti, internih standardih, itd. V tovarniškem okolju je uporaba industrijskega krmilnika in SCADA sistema največkrat edina možnost. Po drugi strani pa je programski paket Matlab s Simulinkom zelo močno matematično orodje, ki omogoča boljšo matematično obdelavo podatkov kot katerikoli SCADA sistem. Zato je smiselno, da se ga vključi v sisteme procesnega vodenja.



Slika 2: Testno okolje za eksperiment

Kot tipičen predstavnik industrijskih krmilnikov je bil porabljen krmilnik S7-414-2DP proizvajalca Siemens. Namen predstavljene rešitve je branje in vpisovanje on-line procesnih podatkov iz krmilnika v Matlab. Za programiranje krmilnika je bil uporabljen programski paket Simatic STEP7, povezava z računalnikom pa je potekala preko vmesnika MPI/RS 232 (Multi Point Interface), kjer je bila hitrost omejena na 19 200 bps. Še boljše rezultate pri prenosu podatkov bi se lahko doseglo z uporabo Profibus vodila, kjer je hitrost prenosa bistveno višja.

Za programsko zajemanje podatkov je bil uporabljen program KEPServerEX OPC strežnik neodvisnega proizvajalca KepWare. Potrebno je bilo ustvariti kanal po katerem poteka komunikacija, izbrati napravo s katere se zajema podatke ter določiti skupino spremenljivk, ki se jih naj nadzoruje. S programom OPC Quick Client istega proizvajalca je možno preklopiti OPC strežnik v monitoring način in tako vnaprej preveriti, če OPC povezava oziroma komunikacija deluje.

Za OPC odjemalec je bil uporabljen OPC Client for Matlab, ki omogoča komunikacijo med OPC in Matlab-om. Gre za nekaj dodatnih ukazov, ki so na razpolago v okolju Matlab in omogočajo povezavo na katerikoli OPC strežnik. Za konfiguracijo tega programa je potrebno vpisati določene ukaze v komandno okno programa Matlab, kot je prikazano na sliki 3 za primer komunikacije z enim vhodom in enim izhodom.

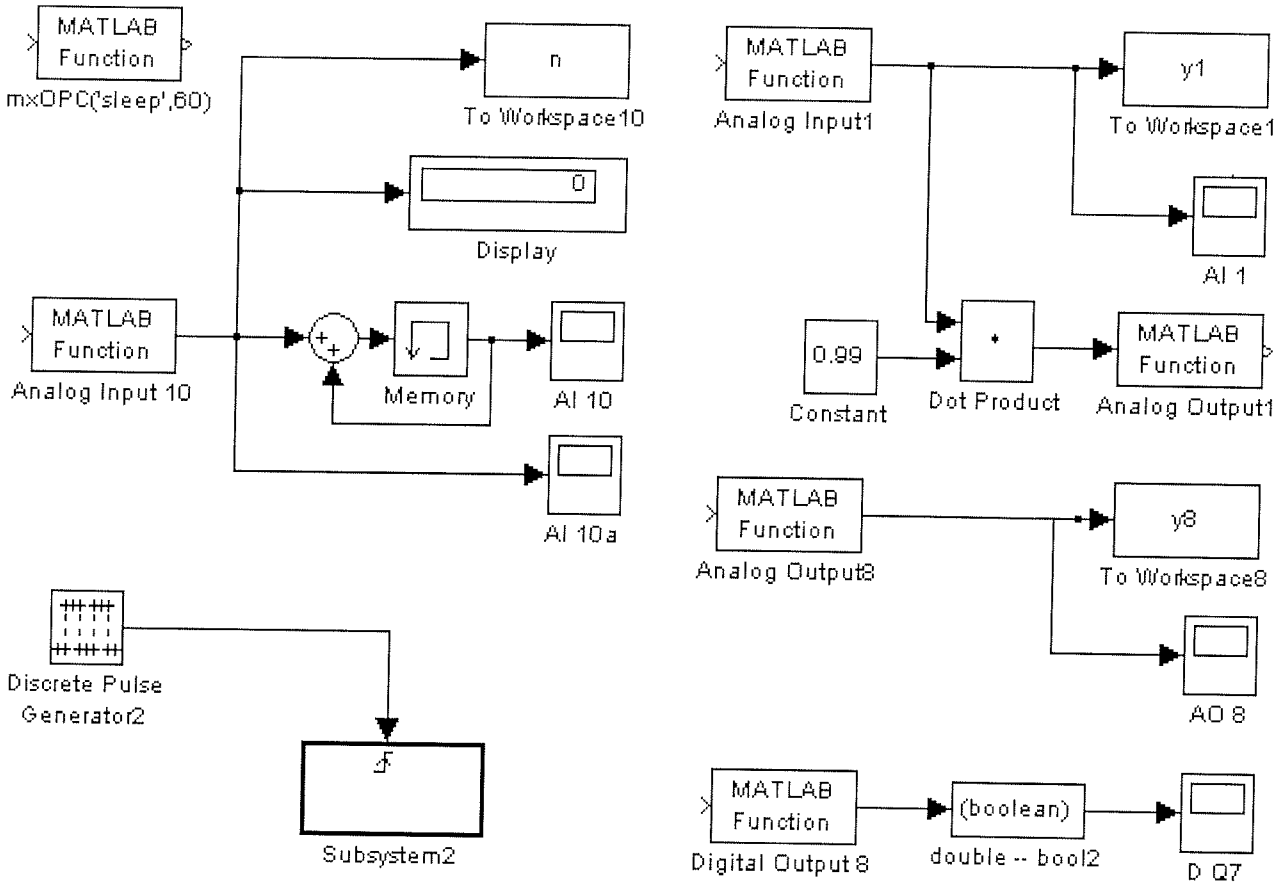
```
i=0;
while(i==0);
hr=mxOPC('open','KEPware.KEPServerEx.V4','localhost',10);
mode=mxOPC('readmode','cache');
hr=mxOPC('setdoublecache','Channel1.Device1.Group1.analog_vh1',1,0);
hr=mxOPC('setdoublecache','Channel1.Device1.Group1.analog_izh1',1,0);
hr=mxOPC('Startdoublenotify','Channel1.Device1.Group1.analog_vh1');
hr=mxOPC('Startdoublenotify','Channel1.Device1.Group1.analog_izh1');
hr=mxOPC('readcache');
hr=mxOPC('writecache');
i=i+1;
end
```

Slika 3: Primer programa v Matlabu za komunikacijo z enim vhodom in enim izhodom

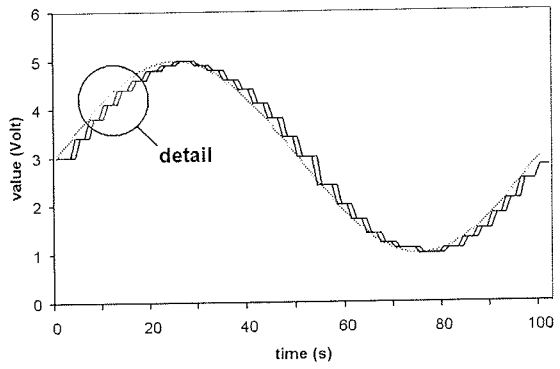
Matlabovo okolje je možno sinhronizirati s procesom. S startno notifikacijo ('startnotification') in čakalnimi ukazi ('wait') je možno ustaviti Matlabovo okolje vse dokler podatek ni poslan na OPC strežnik. Druga pot za sinhonizacijo Matlabovega okolja je možna z uporabo sleep ukazov, kar je uporabljeno za testiranje hitrosti komunikacije in je prikazano na sliki 4.

Za testiranje hitrosti prenosa podatkov iz realnega sveta v Matlab je bil uporabljen zvezen sinusni signal, prikazan na sliki 5 iz katere je razvidna diskretizacija kot posledica tipanja. Testiranja oziroma meritve smo izvajali v za sistem najbolj neugodnih razmerah, saj so se le tako lahko pridobili podatki o mejnih zmogljivostih. Strežnik je zajemal podatke iz krmilnika, preveril kvaliteto in morebitno spremembo vrednosti podatkov ter jih posredoval odjemalcu, ki jih je po obdelavi poslal nazaj po isti poti. Za namene "worst case" testiranj se je uporabilo sinhrono branje, kjer se je vsak podatek vsakič spremenil, na istem računalniku pa so tekli en strežnik, dva odjemalca, SCADA ter Matlab program. Na sliki 6 je prikazan detajl signalov, kjer je z *a* označen sinusni signal, z *b* podatki na strežniku ter s *c* podaki na odjemalcu. Skupen čas prenosa je označen s t_3, osnovo oziroma fiksni del časa prenosa predstavlja konstanta t_1 = 300 ms, kar je najmanjši čas kontinuiranega osveževanja uporabljenega OPC strežnika, razlika do izmerjenega časa pa je posledica obremenitve strežnika, ki je znašala povprečno t_2 = 11 ms za 11 signalov, torej okrog 1000 podatkov/s (vse na sliki 6). Omenjeni rezultati so v skladu s specifikacijami OPC standarda ter tudi skladni z opažanji drugih raziskovalcev /3//15//23/, ki so izvajali testiranja na industrijskih SCADA sistemih.

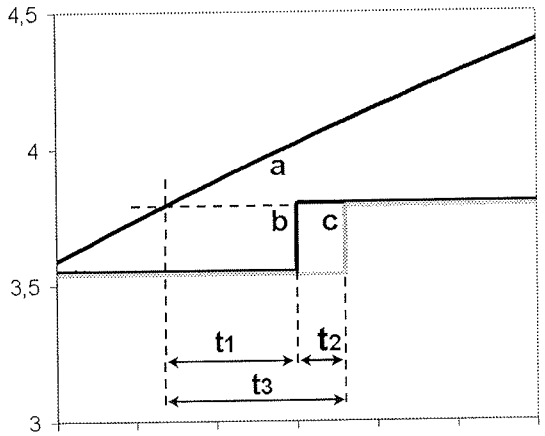
Drugi del testiranja se je nanašal na zanesljivost komunikacije. Opazovali smo razmerje med uspešno in neuspešno poslanimi podatki. Testiranje smo izvajali v zaprti zanki krmilnik-Matlab-krmilnik, ob čemer smo spreminjali tako čas "sleep" v Matlabu kot tudi obremenitev računalnika z drugimi opravili. Za kot najbolj neugodno se je izkazala manipulacija s slikami. V Matlabu smo v fiksnih časovnih intervalih prožili cikle obdelave podatkov ter spremljali razmerje izvršenih ter neizvršenih ciklov. Če se cikel ni izvršil in je bil posledično prenos podatka neuspešen, smo sklepali na



Slika 4: Del testnega okolja v Matlabu



Slika 5: Signali za testiranje prenosov podatkov



Slika 6: Detajl signalov

zasedenost računalnika z drugimi opravili ter s tem na preobremenjenost. Ob tem naj poudarimo, da tudi klasični sistemi industrijske avtomatizacije nimajo 100% zanesljive komunikacije, ampak se izpadi podatkov pojavljajo tudi med normalnim delovanjem, kar se rešuje s ponovitnijo zahteve po prenosu izpadlega podatka (retry).

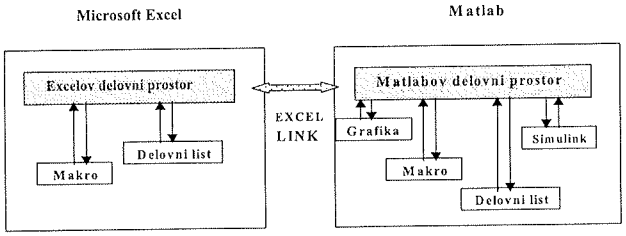
Testiranje smo izvedli pri časih proženja Matlabovih ciklov 20 ms in 60 ms pri različnih obremenitvah operacijskega sistema (OS), ter pri obdelavi enajstih realnih podatkov iz procesa. Rezultati so prikazani v tabeli 1, kažejo pa, da je pri časih izvrševanja 60 ms in več poraste zanesljivost na sprejemljivo vrednost tudi za industrijske razmere. Nekoliko zmanjšana hitrost ne predstavlja posebnih težav, saj je v industrijskih procesih večina prenosov podatkov do PC računalnika razreda sekund.

	Pročenje cikla v Matlabu	
	20 ms	60 ms
Neobremenjen OS	0,12 %	0,02 %
Obremenjen OS	1,69 %	0,61 %

Tabela 1: Rezultati testiranja izvajanja Matlab aplikacije - procent neizvršenih ciklov

Tretji del testiranja smo izvedli podobno kot v drugem primeru ob zaprti zanki krmilnik-Matlab-krmilnik, pri čemer smo ob znani hitrosti delovanja Matlaba merili skupen čas prenosa (t_3 na sliki 6), ki je povprečno znašal 720 ms, kar je še znotraj sprejemljivih mej za nadzor industrijskih procesov. Omenjen čas prenosa običajno ni sprejemljiv za vodenje procesov, čemur pa ne SCADA, ne opisana aplikacija nista namenjena, saj za to skrbijo krmilniki.

V četrtem delu smo poskušali poiskati alternativno pot za prenos industrijskih podatkov v Matlab. Obstaja možnost, da se podatki preko izbranega KEPServerEx vmesnika prenašajo v Microsoft Excel, kjer se da do njih on-line dostopati tudi iz Matlaba s pomočjo Excel linka, ki je podobno kot OPC odjemalec skupek nekaj dodatnih funkcij za Matlab. Sestavljena je bila aplikacija kot na sliki 7, izmerjene pa so bile hitrosti oziroma časi potrebni za prenos podatkov.



slika 7: Povezava Matlaba in Excela

Razvidno je bilo, da podatek prihaja iz krmilnika v Matlab hitreje, kot pa se izpisuje iz Matlaba na krmilnik. Razlog je v makru, ki vpisuje podatek na OPC strežnik oziroma na krmilnik. Opisana povezava je zelo občutljiva na obremenitev računalnika, saj so bili časi prenosa podatkov od 600 do 1200 ms, pri čemer naj omenimo, da je bil od obremenitve bolj odvisen čas branja podatkov v Matlab, kot pa čas vpisovanja podatkov v PLC.

Kot zadnje smo izvedli še test v pogojih, ki jim je predlagana rešitev najbolj namenjena. To je prenos procesnih podatkov v Matlab za namene simulacije, optimizacije in testiranj in sicer podatkov, ki jih tako ali tako že zajema SCADA sistem (slika 2). Uporabljena je bila torej standardna struktura sistema industrijske avtomatizacije, ki smo ji dodali povezavo do Matlaba. Pomembno je, da pri predstavljeni rešitvi ne prihaja do časovnih zakasnitev med podatki v Matlabu in tistimi v SCADA sistemu, saj sta oba priključena na isti OPC strežnik. Tudi morebitnih zakasnitev delovanja celotnega sistema zaradi dodatnega OPC Clienta ni bilo zaznati. Na procesih, ki imajo časovno konstanto večjo od ene minute ponuja predlagana rešitev tudi možnost vodenja brez omejitev, saj je v tem primeru čas tipanja 100 krat večji od časovne konstante in se lahko signal obravnava kot zvezen signal. Ta možnost se lahko izkoristi v učne, eksperimentalne ali raziskovalne namene, ob čemer ohranja vse prednosti uporabe zanesljivih in preverjenih industrijskih rešitev.

5. Zaključek

Namen OPC standarda je zagotoviti možnost medsebojnega povezovanja različne procesne opreme in programskih paketov različnih proizvajalcev ter s tem preprečiti, da bi bila programska oprema odvisna od strojne opreme proizvajalcev. Ugotovljeno je bilo, da prinaša uporaba te tehnologije številne prednosti, ki jih lahko strnemo v boljši povezljivosti z različnimi sistemi in procesnimi napravami ter boljši funkcionalnosti, ki jo OPC v povezavi s SCADA sistemi ponuja. Dogajanja na trgu SCADA programske opreme kažejo, da je praktična uporaba omenjene tehnologije dejansko trend razvoja na tem področju. SCADA sistema, kot sta iFIX ter InTouch, že temeljita na komponentni arhitekturi ter OPC in s tem tudi pričata, da je uporaba OPC realnost. Pri avtomatizaciji proizvodnje pomeni odločitev za OPC ne samo trenutno prednost zaradi primerljivosti različnih ponudb izvajalcev, ampak tudi ali pa predvsem odprtost sistema za nadaljno širitev saj so enkrat zajeti podatki resnično na voljo ostalim programom brez morebitnih posegov v SCADA sistem. Razvoj OPC tako ni samo pripomogel k večji izbiri proizvodov in konkurenčnosti, pač pa tudi k vedno večji uporabnosti in funkcionalnosti sistemov procesnega vodenja v industriji vse do sistemov poslovnega odločanja. Tudi na področju OPC gre razvoj v smeri povezovanja z Internetom, kjer so v fazi zaključnih dogovorov specifikacije za področje OPC XML ter nova specifikacija OPC Data Access 3.0.

Predlagana je rešitev, ki preko OPC uspešno poveže že obstoječ sistem industrijske avtomatizacije z okoljem Matlab, kar lahko služi za on-line spremljanje procesnih podatkov proizvodnje z namenom analize ali optimizacije proizvodnega postopka, zgodnje detekcije napak, ali pa zgolj prenosu procesnih podatkov v Matlab za nadaljnjo obdelavo ali shranjevanje. Omenjena rešitev pokaže svojo uporabnost še posebej v pogojih, ko se proizvodnega postopka ne sme spreminjati ali zaustaviti, kot je to primer v farmacevtski industriji ali v proizvodnji mikroelektronike, ko je tudi sama prisotnost ljudi v proizvodnji nezaželena. V testnem sistemu je OPC strežnik zajemal podatke iz krmilnika, preveril kvaliteto in morebitno spremembo vrednosti podatkov ter jih posredoval OPC odjemalcu, ki jih je po obdelavi poslal nazaj po isti poti. Za namene "worst case" testiranj se je uporabilo sinhrono branje, kjer se je vsak podatek vsakič spremenil, na istem računalniku pa so tekli en strežnik, dva odjemalca, SCADA ter Matlab program. Opravljene meritve kažejo, da so zaradi fiksnega mrtvega časa zmogljivosti najslabše pri prenosu enega samega podatka, pri velikem številu podatkov pa se lahko računa na hitrosti okrog 1000 podatkov/s. Procesni podatki so Matlabu na razpolago praktično istočasno kot SCADA sistemu, kar potrjuje uporabnost v industrijskih sistemih. Predlagana rešitev je še posebej primerna za počasi se spreminjajoče industrijske procese, kjer ponuja tudi možnost vodenja.

Možnosti nadaljnjih raziskav se kažejo v raziskavi uporabe OPC strežnikov z manjšimi časi prenosov podatkov v povezavi z opcijo "prenos podatka le ob spremembi" (exception based), kar pomeni v povprečju sicer krajši, vendar nedeterminističen čas prenosa. OPC omogoča tudi "time stamping", kjer se v hitrem krmilniku pripne podatku zraven njegove vrednosti še časovna znamka nastanka podatka. Ob prenosu takih podatkov v Matlab bi se le-ti lahko uskladili z ostalimi on-line podatki, kar prinaša nove izzive na področju vodenja procesov s spremenljivimi mrtvimi časi.

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IEEE 1149.1 STANDARD: A WIDELY SUPPORTED DESIGN FOR TESTABILITY TECHNIQUE

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Key words: electronics, electronic circuits, PCB, Printed Circuit Boards, IC, Integrated Circuits, electronic systems, testing, debuggers, debugging, design for testability, in-circuit test, boundary-scan test, JTAG, Joint Test Action Group, IEEE 1149.4 standards, TAP, Test Access Port, mixed-signal test buses, EDA, Electronic Design Automation, ATPG, Automated Test Pattern Generation, IEEE 1532 standards, in-system configurations, IEEE 1500 standards, embedded core tests

Abstract: This paper is a short introduction to the implementation and application of IEEE 1149.1 boundary-scan test techniques, which are key to efficient design test and debug in increasingly complex electronic circuits. Following a short description of IEEE 1149.1 compliant devices, the paper focuses on the actual benefits of using boundary-scan test infrastructure on chip, board and system levels. Main features of currently available boundary-scan test design and application tools are briefly presented. A survey on IEEE 1149.1 standard extensions and recent developments of related standards is also included, which confirms the importance for designers to be familiar with boundary-scan techniques. The main goal of the paper is therefore to promote the use of IEEE 1149.1 and other standardized design for testability techniques amongst developers and designers in our national electronic industry.

IEEE 1149.1 standard: dobro podprta tehnika načrtovanja zmožnosti testiranja vezij

Ključne besede: elektronika, vezja elektronska, PCB plošče vezja tiskanega, IC vezja integrirana, sistemi elektronski, preskušanje, iskalniki in odstranjevalniki napak, iskanje in odstranjevanje napak, snovanje za preskusljivost, preskušanje v vezju, linija preskusna robna, JTAG skupina delovna za preskušanje spojev, IEEE 1149.4 standardi, TAP vrata dostopa preskusa, vodila preskusna s signali mešanimi, EDA avtomatizacija snovanja elektronike, ATPG generiranje vzorcev preskusnih avtomatizirano, IEEE 1532 standardi, konfiguracije v sistemu, IEEE 1500 standardi, preskušanje jeder vgrajenih

Izvleček: Članek predstavlja kratek uvod v načrtovanje in uporabo tehnike IEEE 1149.1 robne testne linije, ki je ključnega pomena za učinkovito testiranje in razhroščevanje čedalje bolj kompleksnih elektronskih vezij. Kratkemu opisu strukture IEEE 1149.1 združljivih komponent sledi predstavitev dejanskih koristi, ki sledijo iz vgradnje infrastrukture robne testne linije v integrirano ali tiskano vezje oziroma elektronski sistem. Na kratko so predstavljene poglavitne lastnosti trenutno razpoložljivih orodij za načrtovanje vezij in testnih postopkov z uporabo robne testne linije. Pregled razširitev standarda IEEE 1149.1 ter trenutnega razvoja sorodnih standardov dodatno potrjuje potrebo načrtovalcev vezij po poznavanju tehnik robne testne linije. Cilj prispevka je tako predvsem spodbujanje uporabe IEEE 1149.1 in drugih standardiziranih postopkov načrtovanja zmožnosti testiranja med razvijalci in načrtovalci v domači elektronski industriji.

1. Introduction

Miniaturization and increasing density of modern electronic devices has brought to increased problems in the production testing of loaded printed circuit boards (PCBs). The production test is essentially an attempt to detect possible defects, such as net-to-net shorts, solder opens or missing components in the assembly of integrated circuits (ICs) and other components on the board. In-circuit test (ICT) has been the industry leading technique for board level testing since mid-1970s due to a number of benefits compared to various functional ("edge connector") testing methods /1/. ICT relies on physical probing of internal PCB interconnections through a "bed-of-nails" fixture (Figure 1) in order to improve fault detection and simplify component level diagnosis.

As high density ICs with smaller pin-to-pin spacing evolved, distance between PCB interconnections has decreased and test lands, which are laid onto copper interconnections to allow ICT probe application, have shrinked as well. This made ICT bed-of-nails fixtures difficult and costly to build. Furthermore, use of multichip modules (MCMs), complex System-on-Chip (SoC) devices and multi-layer boards made physical access to internal nodes virtually impossible /2/.

During the 1980s several companies tackled the problem of limited access board testing, developing the so-called boundary-scan principle. They built their concept on ICT techniques, but with physical nails being substituted by an on-chip serial shift register placed around the IC core boundary i.e. a boundary-scan register. In 1985 representatives from several European and North American companies formed the Joint Test Action Group (JTAG), which converted the boundary-scan idea into an international standard. The IEEE 1149.1 standard was first published in 1990.

During the past decade boundary-scan became a mature Design for Testability (DfT) technique /3/, widely supported by both catalog IC manufacturers and by electronic design automation (EDA) tool vendors /4, 5, 6/. Nevertheless many electronics manufacturers still ignore the benefits of providing their PCB designs with IEEE 1149.1 infrastructure. This paper wants to briefly illustrate these ben-

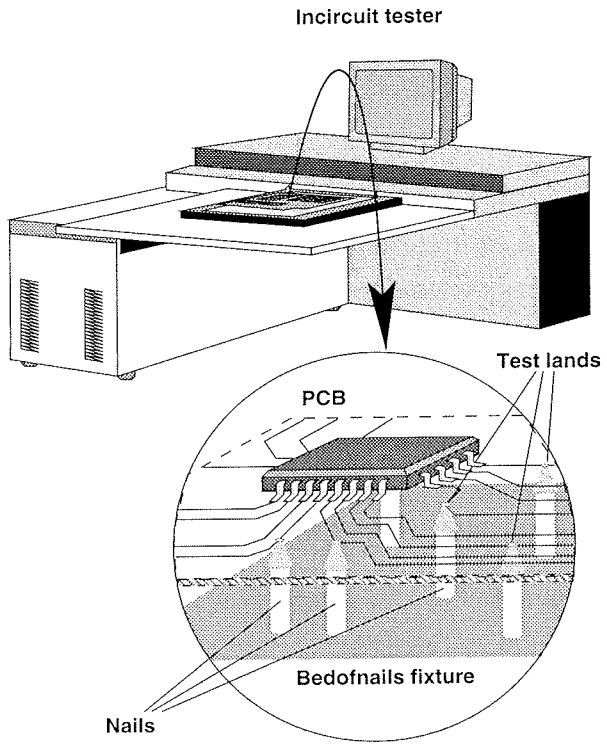

Figure 1: In-circuit test technique

efits and direct the interested reader to more detailed sources of information on boundary-scan infrastructure design, its use and the available tools.

2. The IEEE 1149.1 standard test access port and boundary-scan architecture

A boundary-scan device features multi-purpose memory elements called boundary-scan cells (BSCs), which are interposed between each primary input or output and the appropriate core logic terminal, and a minimal Test Access Port (TAP) interface (Figure 2). The BSCs are serially concatenated into a parallel-in parallel-out shift register, which is accessed through two TAP pins, namely Test Data Input (TDI) and Test Data Output (TDO). Control structures, which are required to select between normal and test operation modes, comprise a finite state machine (TAP controller) that operates synchronously to a Test Clock (TCK) and under the control of a Test Mode Select (TMS) signal. Additional test structures include a single instruction register that controls the test modes and any number of test data registers (including the boundary-scan register) that can be selected by specific instructions. An optional Test Reset (TRST) pin can be also included into the TAP.

The IEEE 1149.1 standard does not prescribe actual hardware implementation of the test infrastructure described above but only defines required components (4-port TAP, boundary, instruction and bypass registers) and their functional properties, as well as the minimum test instruction

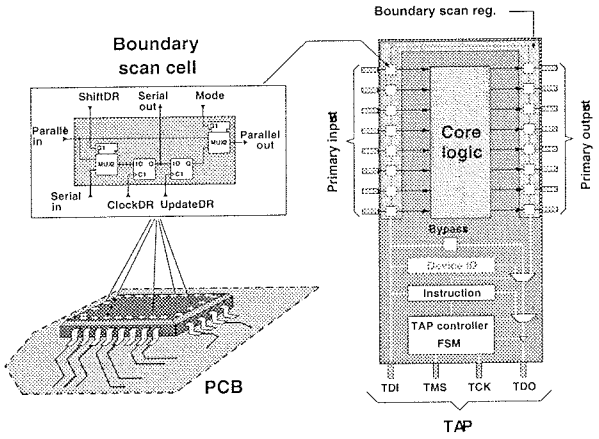

Figure 2: Structure of a boundary-scan device

set that any compliant device must support /7/. Furthermore, the standard allows for optional and proprietary test instructions, and for additional test data registers to be implemented on-chip. A later supplement to the standard defines the Boundary-Scan Description Language (BSDL) syntax. BSDL is used for describing the boundary-scan device pin-out and the specific implementation of its test infrastructure (such as boundary register, optional registers, instruction set and opcodes). BSDL files are readily available from manufacturers of IEEE 1149.1 compliant devices.

2.1 Use of boundary-scan at chip level

The on-chip boundary-scan test infrastructure does not contribute to the basic functionality of the device. Nevertheless it can provide substantial benefit at chip level with its provision for a standard test access method (TAP), which can be used to access chip-internal test facilities, such as internal scan path, built-in self-test (BIST) or built-in emulation and debug.

Internal scan paths are implemented by substituting normal storage elements (latches, flip-flops) within the core logic with scannable ones, which can be serially interconnected to form a shift register structure (Figure 3). The primary reason to adopt this technique is the inability of sequential automatic test pattern generation (ATPG) algorithms to provide adequate fault coverage for core logic test. By dividing core logic into smaller sequential blocks (partial-scan), or plain combinatorial blocks (full-scan) that are accessible from the internal scan path, better fault coverage can be achieved with existing ATPG algorithms /8/.

IEEE 1149.1 architecture allows the definition and use of proprietary instructions therefore the internal scan path register can be easily integrated with other 1149.1 test data registers. Consequently, static device test requirements can be reduced to the TAP interface, since both boundary and internal scan registers are accessible through TDI/TDO. Furthermore, internal scan path can be accessed through the same interface for chip debug and failure diagnosis.

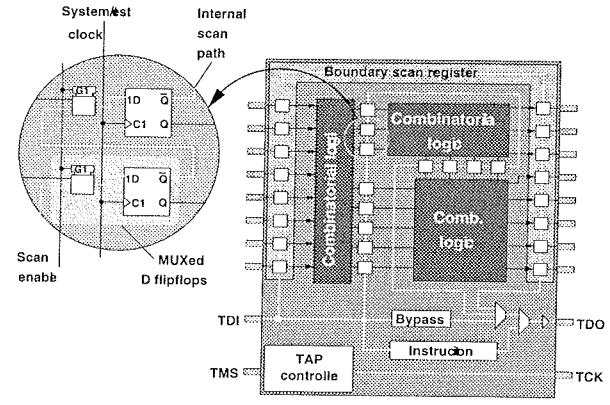

Figure 3: Device with internal scan path

The main benefit of BIST techniques is that test vectors are generated and test responses are monitored on-chip thus eliminating the need for external generation and application of large sets of test vectors via the chip primary inputs/outputs. This is usually achieved by means of pseudo-random pattern generators and signature analyzers implemented as linear-feedback shift registers (LFSRs). IEEE 1149.1 provides for easy integration with on-chip BIST through the implementation of the optional *runbist* test instruction. When implemented, *RUNBIST* can provide for quick functional testing of a PCB mounted device.

2.2 Use of boundary-scan at board level

Board-level test has been the primary concern of the IEEE 1149.1 standard developers. Boundary-scan cells replace ICT physical nails by providing electrical access to circuit-internal nodes through device primary inputs/outputs and are therefore often referred to as "virtual nails" or "silicon nails". At the board level, boundary-scan devices are usually daisy-chained (TDO to TDI, Figure 4) to form a single boundary-scan path.

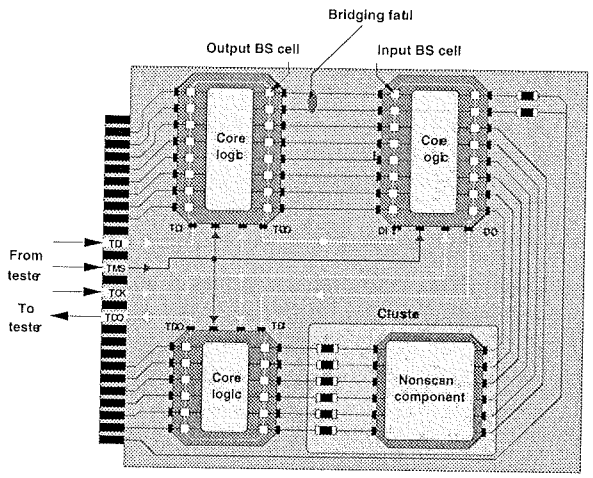

Figure 4: Board-level boundary-scan path implementation

For boards, which are entirely populated by IEEE 1149.1 compliant devices, opens/shorts tests with 100% fault coverage can be generated fully automatically by ATPG software and inexpensive four-wire boundary-scan testers can be used to perform the board test. Furthermore, faults can be automatically isolated to the interconnection (for shorts) or to the node (for opens). The task of generating board-level fault tests is greatly simplified. Since each device input pin can be sampled and each output pin can be driven from the appropriate BSC, no knowledge of the device core logic is required for fault testing the board. For a group of PCB interconnections between two boundary-scan devices, a single test vector is required to test all interconnections for stuck-at-one faults. To provide stimulus, an all-zeros test vector is shifted into output BSCs via TDI to drive the interconnections low. Interconnection values are then sampled into input BSCs and shifted out via TDO for comparison with the expected value. Similarly, stuck-at-zero faults test requires a single test vector of all-ones. Bridging faults can be isolated using a binary search algorithm: a group of 8 interconnections requires only 3 test vectors for a complete bridging fault test, as shown in Table 1.

	Interconnection							
	1	2	3	4	5	6	7	8
Vector 1	0	1	0	1	0	1	0	1
Vector 2	0	0	1	1	0	0	1	1
Vector 3	0	0	0	0	1	1	1	1

Table 1: Test vectors for 100% bridging fault coverage (number of interconnections = 8)

Altogether, a board with N interconnections between distinct BSCs, would require a total of (log N / log 2) + 2 test vectors for full bridging and stuck-at fault test (i.e. 5 test vectors for 8 nets). Consider now fault testing a non-IEEE 1149.1 board with ICT probes. In contrast with BSCs, bed-of-nails fixtures usually provide a single access point to any interconnection, therefore stimulus is applied to interconnections at device inputs and response is sampled on interconnections at device outputs. A plain combinatorial device would require 2^N test vectors for a full test (i.e. 256 vectors for 8 interconnections). Although the number might be significantly reduced by studying the device functionality, this requires adequate functional models and test development tools. In case of a sequential device the problem would become even more complex, since several set-up vectors might be required to condition a device to test an input and several vectors might be required to propagate the fault to an output for observation.

On the other hand, even if the board comprises only a few IEEE 1149.1 devices, the test development can be substantially simplified and fault coverage improved. When clusters of non-scan devices and other components are surrounded by boundary-scan devices, BSCs in surrounding devices can be used to stimulate the cluster and observe its responses. In this case a suitable test vector set targeting interconnection faults within the cluster must be prepared. When such approach is not sufficient in terms of fault coverage, the boundary-scan infrastructure can be

combined with ICT physical nails to access cluster-internal interconnections.

2.3 Use of boundary-scan at system level

Chip and board-level IEEE 1149.1 based tests can be reused at system level e.g. for system BIST, field service, remote diagnostics or hardware debug. The main benefit is that the physical test access can be limited to the simple TAP interface and use of complex test hardware can be avoided. Moreover, by implementing backplane bus interfaces on single PCB modules and on the backplane PCB with scannable devices, the backplane connectivity and integrity test can be performed and the system can be partitioned along modules boundaries for easier diagnostics.

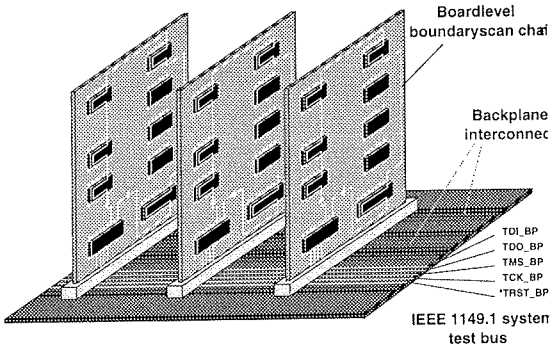

Figure 5: Multidrop system IEEE 1149.1 architecture

While a single boundary-scan chain is usually used to connect IEEE 1149.1 devices on a PCB (Figure 4), the same approach is not adequate for integrating boards into the backplane architecture (Figure 5). If the backplane is designed such that board-level scan chains are daisy-chained into a single system wide chain, then removing any board from the system will break the boundary-scan chain. Furthermore, boards must be located in specific slots in order to preserve a known test infrastructure and a fault in the chain of one board would leave the entire system untestable. To avoid such problems the standard proposes a multidrop star configuration in which the TDI and TDO pins are bussed. However to prevent simultaneous scanning of multiple boards onto the same TDI/TDO bus, multiple TMS signals are required (one for each slot) and the number of backplane channels increases proportionally. An alternative solution, which does not require multiple TMS lines, is a multidrop scheme using addressable IEEE 1149.1 devices.

3. Boundary-scan development tools and testers

In order to benefit from the IEEE 1149.1 standard, the designer should specify the use of boundary-scan infrastructure in custom ASICs and place scannable catalog devices on board wherever possible. Nowadays a number of IC vendors provide a variety of IEEE 1149.1 compliant devices, including standard components (bus interfaces, microprocessors, DSPs, memory ICs, ...), user field-programmable devices and ASICs (gate-arrays, standard cells, ...). Various support devices (test bus controllers, scan path bridges/linkers/selectors, multidrop addressable test ports) are readily available to facilitate the implementation of board or system level boundary-scan infrastructure.

Another very important issue for a designer is the availability of EDA tools supporting boundary-scan. Most major EDA vendors offer boundary-scan insertion tools as well as tools for boundary-scan ATPG.

Finally, some means of boundary-scan test application is also required, which can come either in the form of large production in-circuit or functional testers with integrated boundary-scan capabilities or as inexpensive, PC-based standalone boundary-scan testers.

3.1 Design of IEEE 1149.1 compliant devices

Boundary-scan insertion tools provide for a more or less automated design of IEEE 1149.1 compliant ASICs, which is often combined with insertion of other on-chip test structures, such as internal scan or BIST. These tools usually operate on RTL or gate-level descriptions of the ASIC design and on existing libraries of boundary-scan building blocks. Better tools provide for a more flexible configuration of the building blocks (e.g. implementation of proprietary test instructions, integration with internal scan / BIST) as well as for the generation of test patterns for use with on-chip test structures. The tool output usually consists of a device netlist and the appropriate BSDL device description (see Figure 6).

3.2 Boundary-scan test development

Boundary-scan ATPG tools automatically generate prototype or manufacturing tests to be applied to the circuit under test (CUT) using the board level TAP. ATPG tools usually consist of various software modules, which can be combined to suite the chosen test strategy. Modules include access analysis, boundary in-circuit test, virtual interconnects test, virtual component/cluster test, boundary functional test as well as test generators for BSDL validation and TAP/scan-path integrity testing. Access analysis tools are typically used before layout of mixed scan/non-scan circuits to identify interconnections, which do not require physical test access. Boundary in-circuit test generators combine physical probing and boundary-scan devices to reduce test complexity. Virtual interconnect test modules generate patterns to test interconnections using only the virtual access provided by the boundary-scan path while virtual component/cluster test modules use boundary-scan access to detect open and stuck-at faults on the leads of non-scan devices/clusters, eliminating the need for physical access. Some tools also support multiple boundary-scan paths on a single board. ATPG tools usually operate

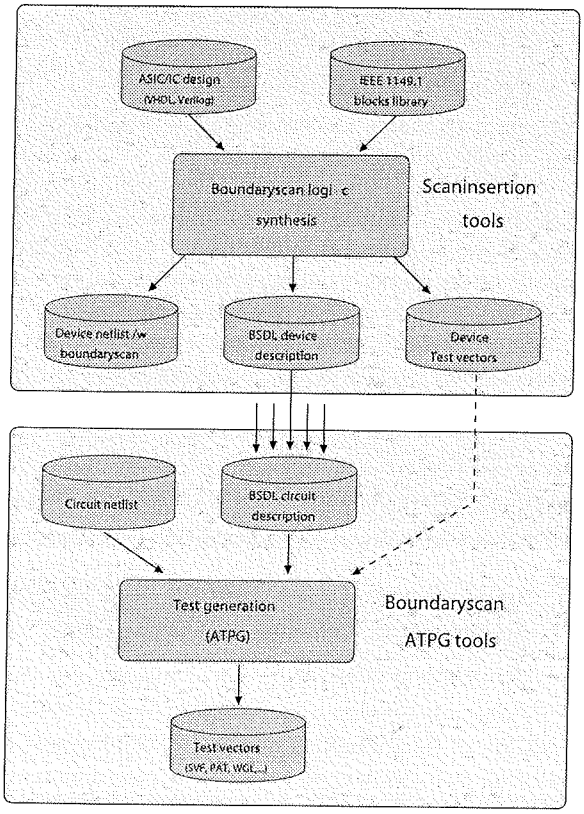

Figure 6: Boundary-scan development process

on given circuit netlist and BSDL description (see Figure 6), producing test patterns in standard automatic test equipment formats, such as the Serial Vector Format (SVF).

3.3 Boundary-scan testers

We can roughly divide commercially available boundary-scan testers into two groups. The first one includes large production in-circuit and functional testers with integrated boundary-scan support, which are designed to achieve the highest possible fault coverage within only one production step. This is reflected by high complexity and elevate costs of such testers. The second group includes so-called stand-alone boundary-scan testers. These usually consist of a host PC and a relatively inexpensive adapter, which controls the IEEE 1149.1 test bus and possibly features some additional parallel I/Os to control/observe CUT edge connectors. A variety of internal and external PC adapters are available on the market for many standard buses, such as ISA, PCI, VXI, PXI, PC-CARD, PIO, RS-232, USB or GPIB.

The minimum requirement for any boundary-scan tester is the ability to exercise the board-level TAPs under the control of a simple test description (e.g. a SVF file), however an interactive boundary-scan test and debug environment is preferred to simplify the use of the test system. Most boundary-scan testers provide software tools that allow interactive view and control of only those portions of the board (pin, register, bus, user-defined signal group) that

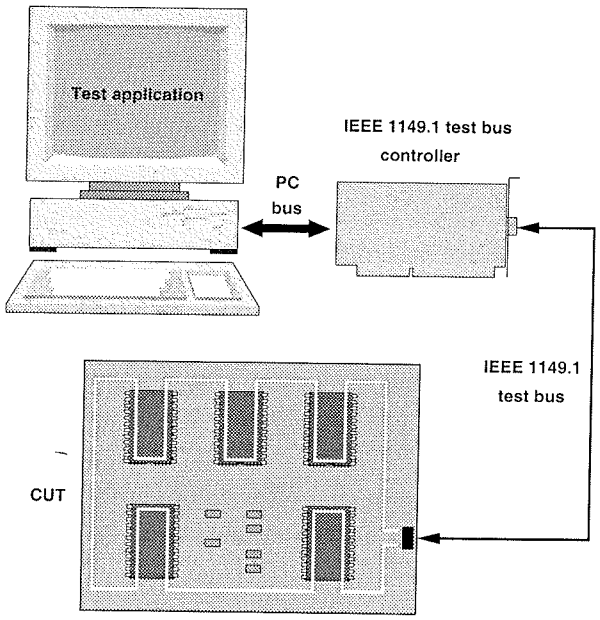

Figure 7: Stand-alone boundary-scan tester

are of interest. The benefit of such tools is that complexity of TAP protocol and boundary-scan chain are hidden from the user and test stimuli/responses are presented as waveform and state diagram displays. The tools usually support various test vector generation methods including interactive creation and EDA or boundary-scan ATPG generated test sets. They also allow the user to describe the boundary-scan test infrastructure using standard formats such as BSDL and EDIF (Electronic Design Interchange Format).

4. IEEE 1149.1 related standards

During the existence of IEEE 1149.1 several related standards have emerged, which extended the use of the boundary-scan techniques and its infrastructure to new areas such as testing of mixed-signal circuits or in-system configuration (ISC) of programmable devices, while a standard concerning testing of System-on-Chip (SoC) devices is currently in project phase. The original standard itself has seen two additional supplements: IEEE 1149.1a-1993 and IEEE 1149.1b-1994 (BSDL). The IEEE 1149.1-1993 supplement brought some clarifications and new optional boundary-scan test commands to the original standard. Furthermore it addressed the issue of integration of IEEE 1149.1 with other test access methods such as the Level Sensitive Scan Design (LSSD), which is frequently used to access internal scan paths. The supplement described a simple mechanism for converting a component from conformance to IEEE 1149.1 to conformance to a different standard. The three publications were finally merged into the latest standard publication - IEEE 1149.1-2001.

4.1 IEEE standard for a mixed-signal test bus (1149.4-1999)

The IEEE 1149.4 standard extended the boundary-scan principle into the domain of mixed analog-digital circuits with the introduction of new elements to the existing IEEE 1149.1 test infrastructure. The standard defines analog boundary modules (ABMs), which are interposed between primary analog functional pins and appropriate analog core terminals. The TAP is expanded with analog pins AT1 (Analog Test 1) and AT2, which are internally connected to each ABM via the Test Bus Interface Circuit (TBIC) and a two-wire on-chip analog bus AB1/AB2 (Figure 8). At the board level, all IEEE 1149.4 devices are connected to a two-wire analog bus through AT1 and AT2 pins /9/.

This additional infrastructure allows analog stimulus from external generators to be routed from AT1 pin to an output ABM and on to connected analog components. Analog responses arriving at an input ABM can be routed to AT2 pin and on to an external measurement unit. In this way, parametric measurements of on-board analog components can be performed.

Although IEEE 1149.4 compliant catalog devices are currently unavailable, first steps are being done by IC manufactures towards the implementation of such devices /10/ and feasibility studies on experimental ICs have already shown a number of possible benefits in designing mixed-signal ICs with IEEE 1149.4 infrastructure /11, 12, 13/.

4.2 IEEE standard for in-system configuration of programmable devices (1532-2000)

In-system configuration of programmable devices has become a major new application of the IEEE 1149.1 standard. Programmable logic imposes several problems (lack of device models, test preparation delays) to ICT board testing methods, therefore IEEE 1149.1 infrastructure is included in the majority of programmable devices. The manufacturers soon realized that they could also use the TAP interface and the boundary-scan serial protocol for ISC of the device. The result of a standardization effort between various manufacturers is the IEEE 1532 standard, which defines additional data registers to assist configuration programming, along with new mandatory and optional instructions compatible with the IEEE 1149.1 physical and logical protocols /14, 15/.

4.3 IEEE Standard Testability Method for Embedded Core-based Integrated circuits (P1500)

Test development currently represents a major problem in the design of complex SoC devices, which include embedded cores originating from different core providers. The P1500 working group was established in 1995 with the goal to develop a standard DfT method for such devices. The standard will define a test wrapper architecture and a language for the description of test related information for

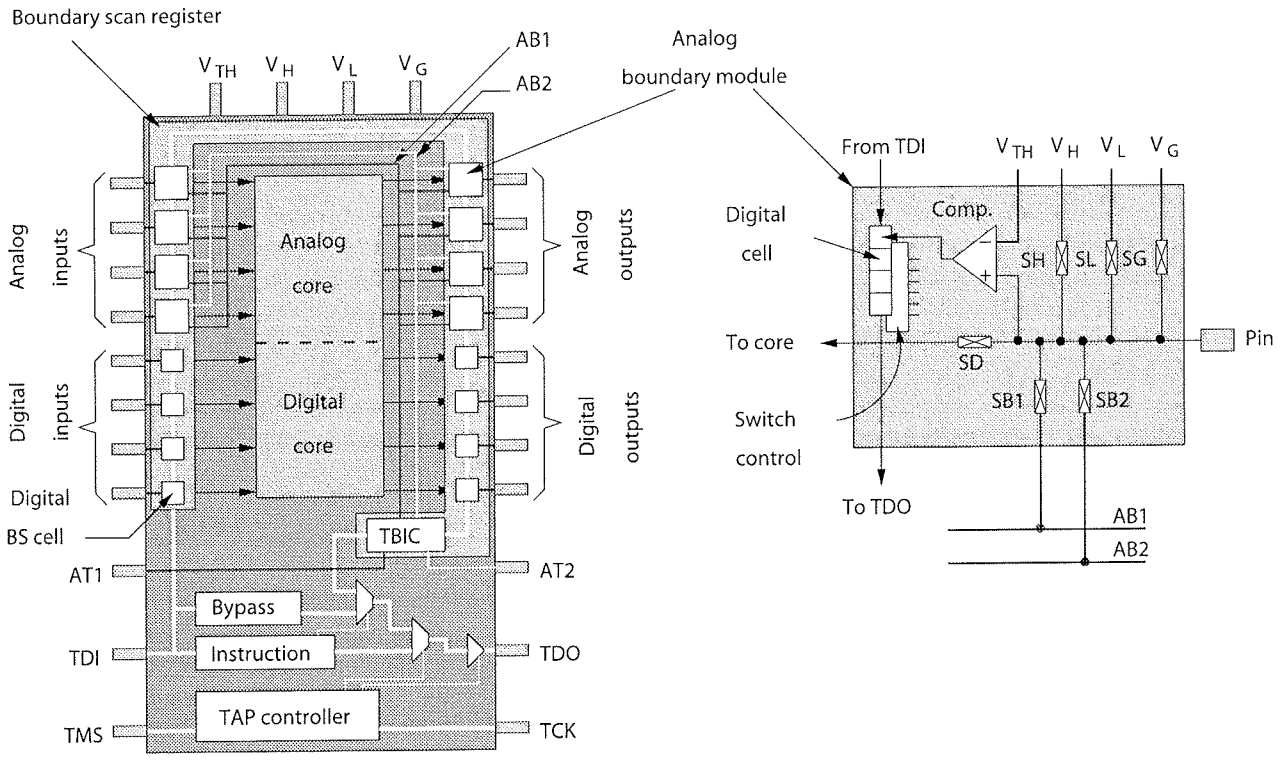

Figure 8: IEEE 1149.4 compliant mixed-signal device structure

the cores (e.g. processor cores, memory blocks, ...) embedded in the SoC /16/, /17/.

In practice, many embedded cores might already include IEEE 1149.1 or another test access mechanism. Hence we may expect the P1500 standard (or a related document) to present some solution for the integration of different test access standards with the proposed wrapper architecture. As mentioned above, similar issues concerning IEEE 1149.1 were addressed by a later supplement to the original standard.

5. Conclusion

In the early years from its publication, the IEEE 1149.1 standard was often criticized for elevating silicon costs and increasing design time. Many designers failed to see how the standard can benefit them, often being confused by the requirements for complex sequencing of the TAP signals. However the declining silicon costs, the growing list of IEEE 1149.1 compliant catalog devices, and the increasing availability of EDA tools that automate boundary-scan test insertion, generation and application have resulted in boundary-scan becoming a widely accepted DfT technique.

Although IEEE 1149.1 is a very efficient answer to the complex problem of testing boards and systems for various manufacturing defects and performing other design debug tasks, many designers still seem to lack basic knowledge about its potentials. In this paper we briefly introduced the reader to the standard, the main benefits of its use at chip, board or system level, and the most important features of available EDA tools. We presented some recent standardization efforts related to the IEEE 1149.1 standard, demonstrating the importance for designers to be familiar with boundary-scan techniques, which will keep an important role in the design of increasingly complex electronic devices. Readers looking for further details on boundary-scan are therefore encouraged to consult referenced literature.

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APPLICATION ARTICLE

CHARACTERISTICS OF POWER SEMICONDUCTORS

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ABSTRACT

This paper aims to give a brief overview of the essential characteristics of power semiconductors, and to provide a guide in their selection for particular applications.

It considers the characteristics of various power components when operating like a switch - either blocking current or voltage, or conducting with a small voltage drop.

Their behaviour is examined in terms of:

(i) Typical current and voltage ratings (switchable power) permanent current - short overcurrent;

(ii) The switching behaviour: switching speed and switching losses;

(iii) Drive requirements.

Advantages and disadvantages are summarised, and the relative cost of each solution indicated.

Currently, the main types of power semiconductors are the Power Diode, the power Bipolar Junction Transistor (BJT), the Thyristor (Triacs and SCRs), the Gate Turn-off Thyristor (GTO), the Power MOSFET, and the Insulated Gate Bipolar Transistor (IGBT).

2 THE POWER DIODE see figure 1.

2.1 Current

The physical parameter which limits current is the maximum junction temperature; the temperature at which destruction of the device occurs. Hence the maximum current in a diode depends essentially on the cooling; in practical terms on the thermal resistance (for DC operation), and on the thermal impedance (for short duration surge currents).

2.2 Voltage

The device is destroyed if the electric field across the N region of the diode becomes strong enough to cause breakdown - hence the voltage ratings of the transistor (forward, V_F and reverse, V_{DRM}) depend upon the thickness of this region.

2.3 Switching

Power PN diodes have a "memory" effect due to the storage of minority carriers. If the voltage across a diode which has been conducting in the forward direction is suddenly

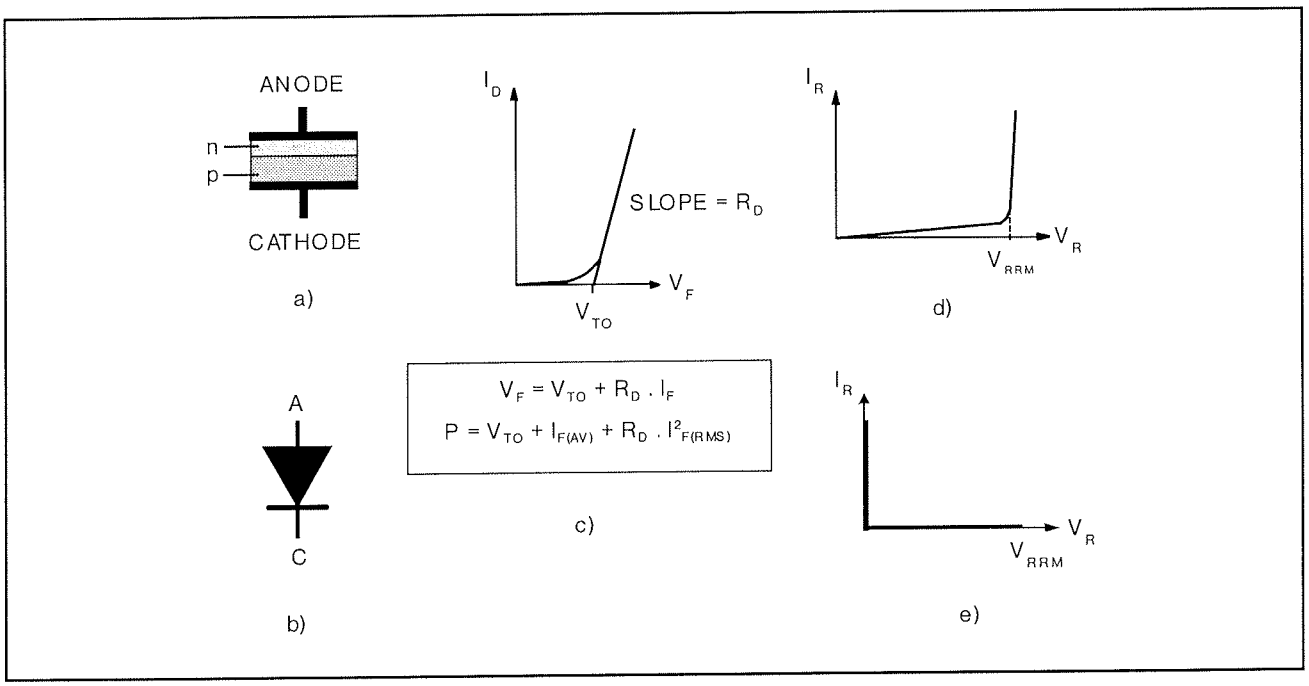

Figure 1. Power Diode: a) Simplified structure b) Circuit symbol c) Current limits d) Voltage limits e) Safe Operating Area

reversed, the p and n regions of the diode are still full of minority carriers, which can cause the diode to behave like a short circuit for a short period of time until the minority carrier density falls. The reverse current due to this effect can cause problems: current spikes, noise, overvoltages, and supplementary switching losses.

Figure 2 shows the turn-off behaviour. The main parameter is the reverse current, I_{RM}, and in some case the recovery charge Qr. The reverse current increases with dI_R/dt (slope of decreasing current before turn-off) and with junction temperature.

A fast PN diode is a diode made with a reduced minority-carrier lifetime, which leads to a reduction in the diffusion length (ie the average distance travelled by a minority carrier before recombination).

If the diffusion length is shorter than the thickness of the silicon N region, the diode's on-resistance increases drastically. However the maximum voltages that the diode can withstand depend upon the thickness of this region. The design of a fast diode is therefore the result of a trade-off between maximum voltage V_{DRM}, forward voltage drop V_F and speed (t_{rr}) - see figure 3.

Figure 4 shows losses introduced by a frewheel diode. Using a faster diode reduces these losses, but it is not always possible to have an ultra fast diode with a high voltage rating. Instead it could be possible to use several low voltage ultra-fast diodes in series - see reference /3/.

When the diode switches off in series with an inductance L, a supplementary energy $L \cdot I^2_{RM}$ is dissipated in the circuit. For this reason the choice of circuit configuration is very important (figure 5).

2.4 Schottky Power Diodes

Schottky power diodes, which use only majority carriers, have a different behaviour; they have a smaller voltage drop and no recovery charge, and are many times faster than PN diodes. However, they have the disadvantages of a limited voltage range (60 to 100V) and a very high internal capacitance. The leakage current is also large, and becomes larger at high temperatures.

3 THE BIPOLAR TRANSISTOR

see figure 6.

3.1 Current

The current capability is defined by:

$V_{CE(sat)} < 1.5V$@ If $I_C = I_{C(sat)}$ If $I_B = I_{B(sat)}$

If $I_C < I_{C(sat)}$, the voltage drop V_{CE} is proportional to it, and can be very small.

If $I_C > I_{C(sat)}$, V_{CE} remains relatively constant with changing I_C, and so the transistor can be considered as a current source.

The bipolar transistor has no overcurrent capability (I_C cannot exceed $I_{C(max)}$), and this maximum operating current is defined by the gain, not by thermal considerations.

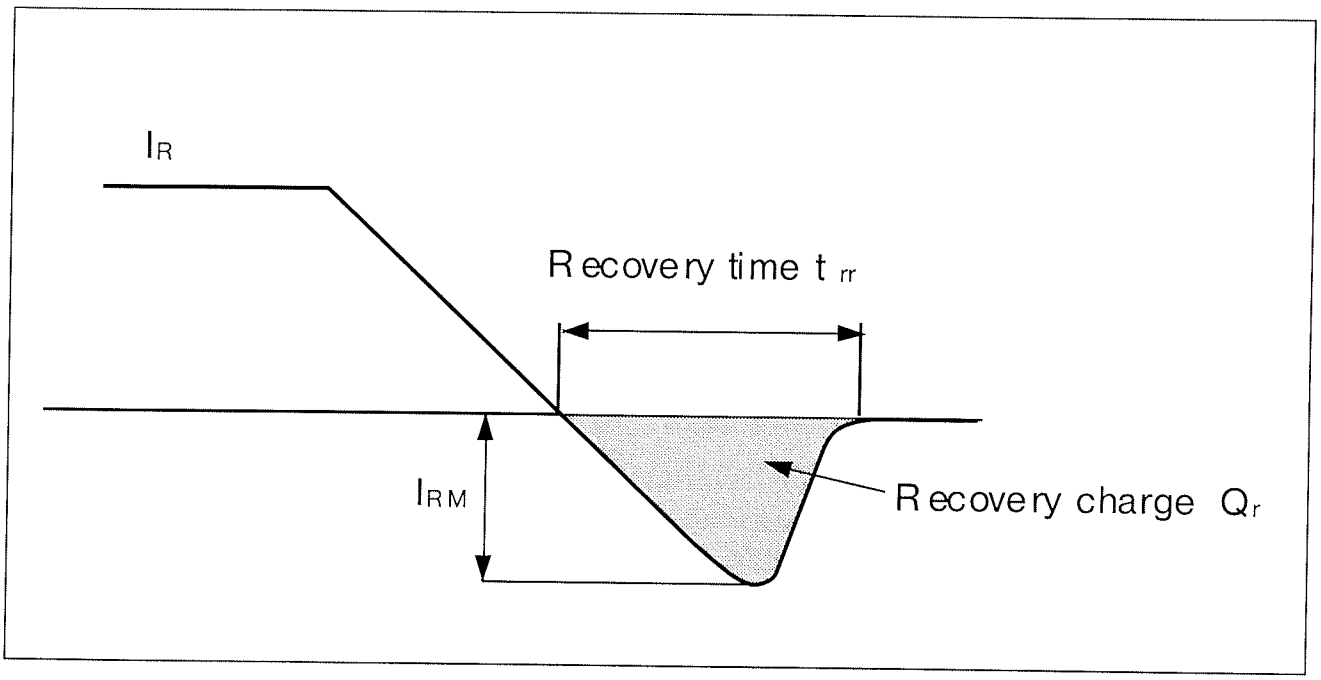

Figure 2. Diode turn-off behaviour

	BYW81	BYT12-400	BYT12-800	BYT12-1000
V_{DRM}	200	400	800	1000
V_F @ 12V	0.85V	1.4V	1.8V	1.8V
I_{RM} (A)	1.8	3.7	6.0	7.8

T_j = 100°C

dI/dt = -50A/µs

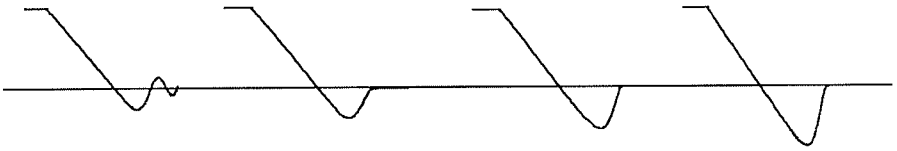

Figure 3. Speed versus VDRM

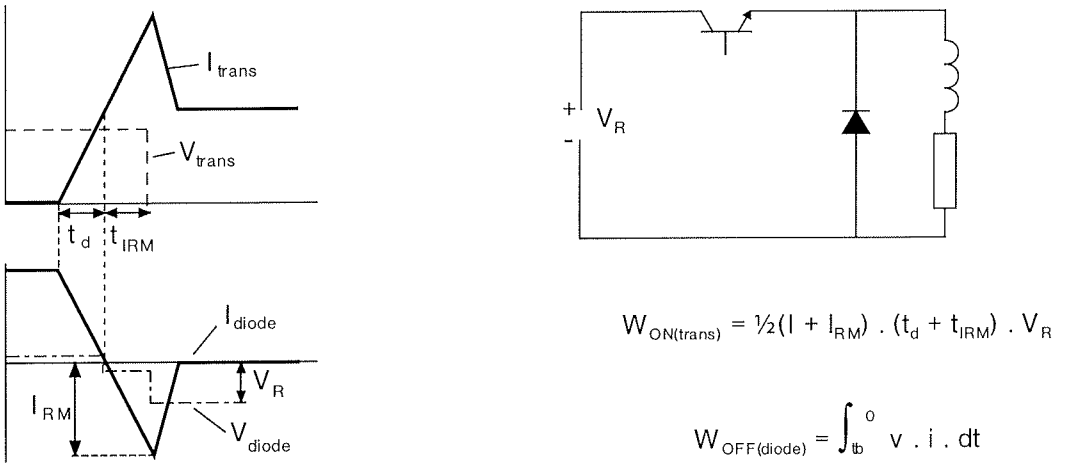

Figure 4. Freewheel diode losses

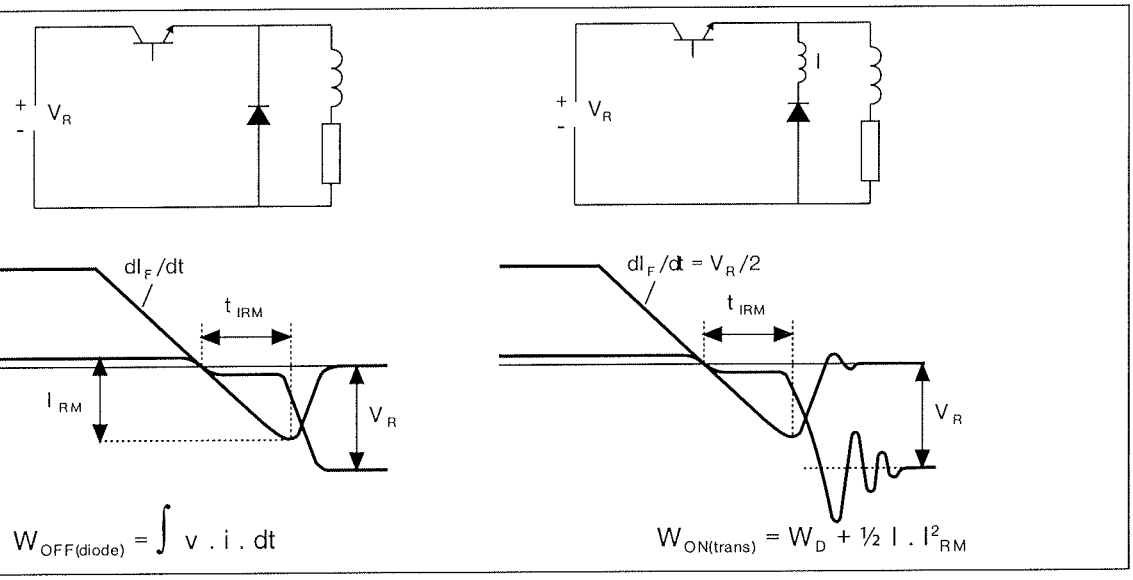

Figure 5. Effect of circuit topology on diode behaviour

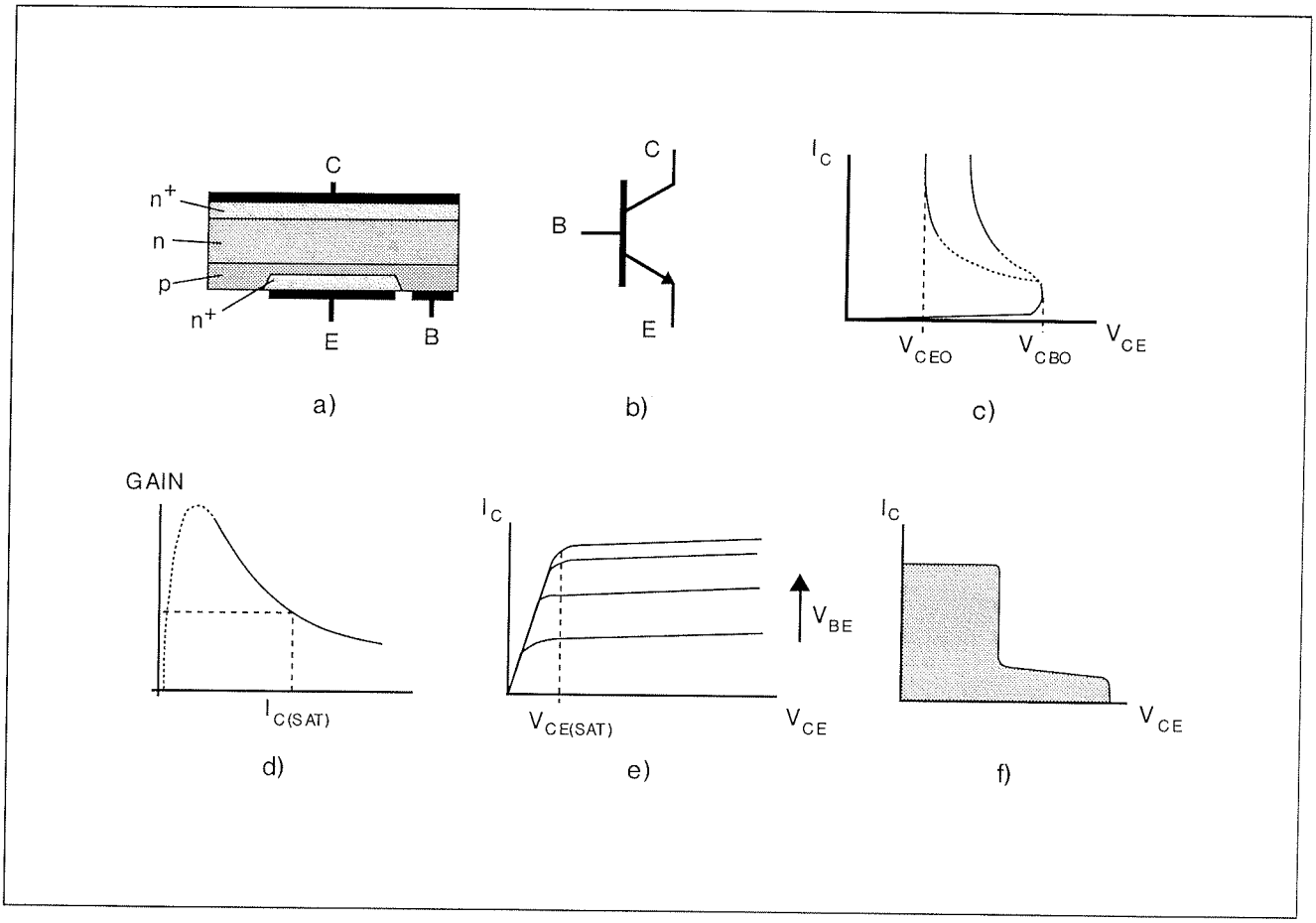

Figure 6. The Bipolar Transistor: a) Simplified structure
b) Circuit symbol
c) Gain characteristics
d) Output characteristics
e) Forward breakdown characteristics
f)Forward-bias safe operating area (FBSOA)

3.2 Voltage

Two parameters define bipolar transistor voltage capability:

- V_{CEV}, the maximum voltage with the base emitter junction blocked (V_{CEV} = V_{CBO}, the maximum collector-base voltage).
- V_{CEO}, the maximum voltage with base open.

For switching applications, voltage limits are defined by the Safe Operating Area (SOA). (V_{CEW}, the working voltage at high current, is often equal to V_{CEO}).

Maximum capabilities for the early 1990s

	V_{CEO}	V_{CEV}	$I_{C(sat)}$
Fast transistors	800V	1300V	60A
Slow transistors	1000V	1400V	400A

Voltage drop: If $I_C < I_{C(sat)}$ the voltage drop (with optimised drive) is very low.

$$V_{CE} = \frac{I_C}{I_{C(sat)} \cdot V_{CE(sat)}}$$

3.3 Drive requirements

See figure 7.

The BJT is a current-driven device: during the conducting phase its necessary to deliver a base current

$$I_{B1} = \frac{I_C}{ß} \qquad ß = \text{gain}$$

At nominal current the gain specified for low voltage transistors (V_{CEO} < 250V) is around 10, and for high voltage transistors is around 5, near $I_{C(sat)}$ as defined in the data sheets.

The following empirical relation can be used to estimate gain at other current levels.

$$ß\ @\ I_C = [ß\ @\ I_{C(sat)}] \cdot \frac{I_C}{I_{C(sat)}}$$

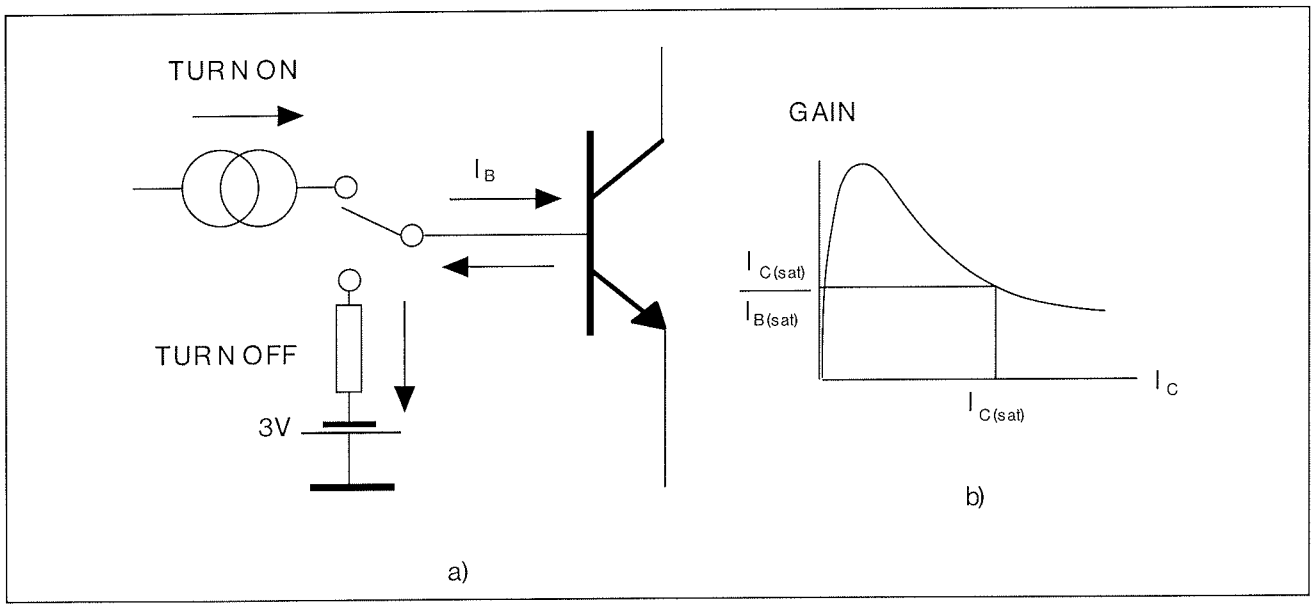

Figure 7. Driving a bipolar transistor: a) Driving circuit b) Choosing the base drive current

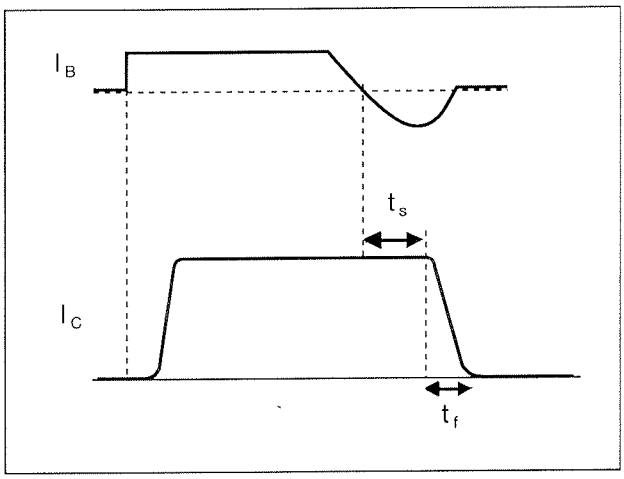

Figure 8. Bipolar transistor switching times

3.4 Switching times

The total turn-off time toff is the sum of two components (see figure 8):

- The storage time t_s. This is a "memory" effect, due to the storage of minority carriers in the base. (1s for V_{CEO} = 100V, 3s for V_{CEO} = 400V).
- The fall time t_f. The majority of switching losses are due to the fall time (but modern transistors using cellular technology have very small fall times).

To ensure fast turn-off, it is necessary to force a negative current I_{B2} in the base to increase the rate of recombination of minority carriers.

3.5 The Darlington

This is a structure which behaves like two bipolar transistors connected, as shown in figure 9: the first acting as a driver, and the second as a power stage.

The Darlington offers higher gain than a conventional BJT, and the ability to operate at higher current density (because the gain of the power stage can be very high), but these advantages are offset by a higher voltage drop:

$$V_{CE(sat)}\ \text{Darlington} = 0.8V + V_{CE(sat)}\ \text{BJT}$$

and also the increased turn-off time - the power stage transistor can only begin to turn off after the driver has turned off.

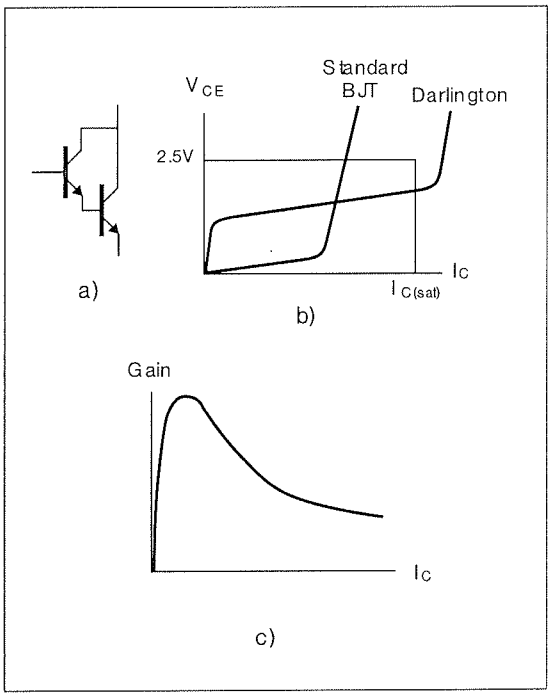

Figure 9. Darlington Transistor characteristics
a) Equivalent structure
b) Output characteristics
c) Gain characteristics

4. THE THYRISTOR

»Thyristor« is a generic term for a semiconductor device having four or more layers. The two main members of the family are the Silicon Controlled Rectifier, or SCR (often simply called a thyristor) and the TRIAC (derived from TRIode for Alternating Current). Both share similar current and voltage characteristics. The structure and characteristics of the SCR are shown in figure 10.

The thyristor operates using positive feedback - once the device is turned on or "fired" by applying the current pulse to the gate, it continues to conduct until the current through it falls below a certain small fixed value, known as the holding current. This effect occurs because, as shown in figure 10b, the SCR behaves like two bipolar transistors connected back to back, which once fired effectively provide their own base drive current.

4.1 Current

The maximum operating current is defined, like the power diode, by the rate at which the device is cooled. The thyristor can withstand very high surge currents (within the capabilities of the cooling arrangements).

4.2 Voltage

The blocking voltage can be very high - up to 5kV. Its voltage drop is around 0.8V at low current, rising to 1.2V at nominal current.

4.3 Drive requirements - see figure 11.

Because of the positive feedback, the thyristor needs only a very low current for a short time at turn-on (firing). In practice a small "holding current" is required to maintain the device in conduction. However it has the disadvantage that the device cannot be turned off by controlling the gate current - instead the anode current must be forced to zero, by forcing the anode-cathode voltage to zero. In switching or AC circuits this can be achieved using a resonant LC circuit connected in series or parallel.

4.4 Switching times

When the anode current is forced to zero, the thyristor turns off. However, it is necessary to wait for a time tq (the turn-off time, like the fall time of a bipolar device) before the anode voltage is reapplied - otherwise the device will continue to conduct.

4.5 The TRIAC

The TRIAC is effectively two SCRs connected in anti-parallel, with a single gate - see figure 12. This device can conduct current in both directions (ie from A1 to A2 and from A2 to A1) and so can be used to control the flow of AC currents - the current through the device will fall below the holding current every half cycle, and at this point the device will turn off automatically unless it is refired. Hence for continuous conduction the device must be refired at twice the frequency of the current it is conducting.

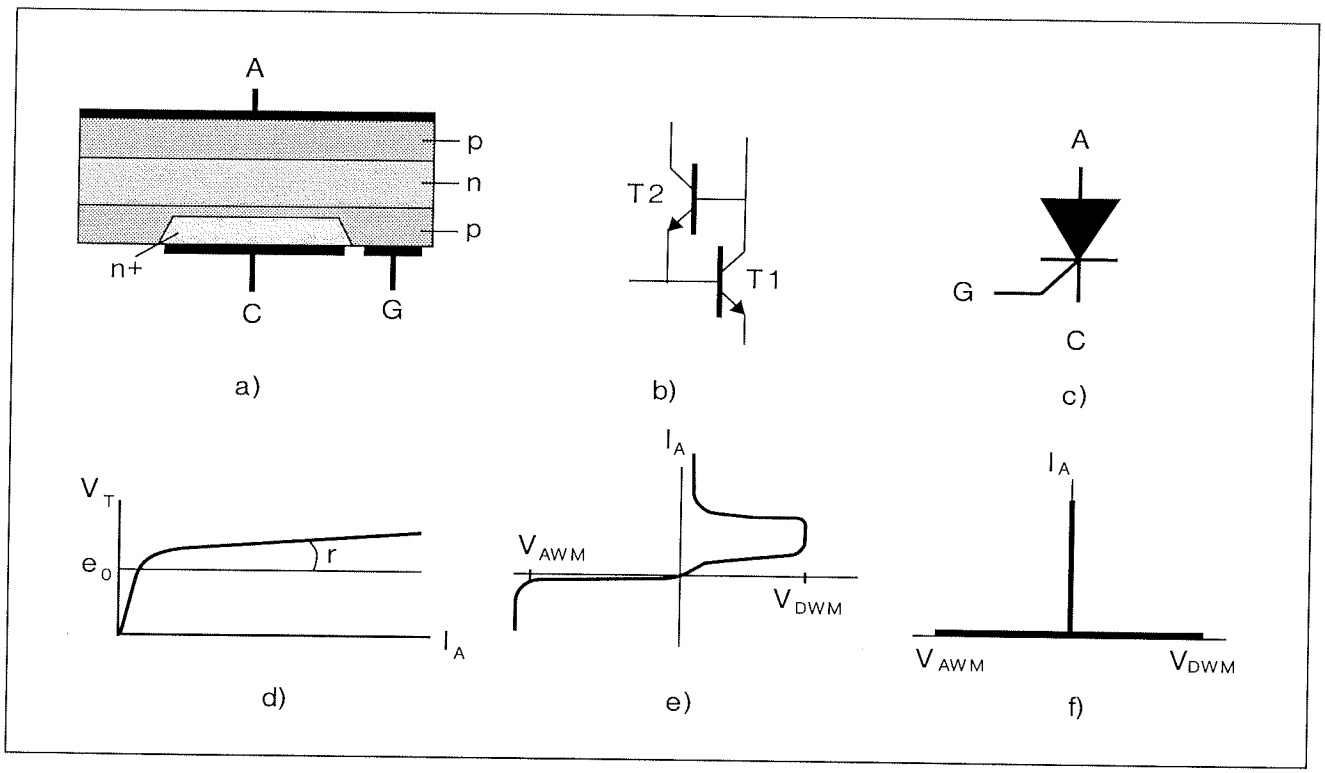

Figure 10. The SCR: a) Simplified structure b) Equivalent circuit c) Circuit symbol d) Current limits e) Voltage limits f) Switching Safe Operating Area

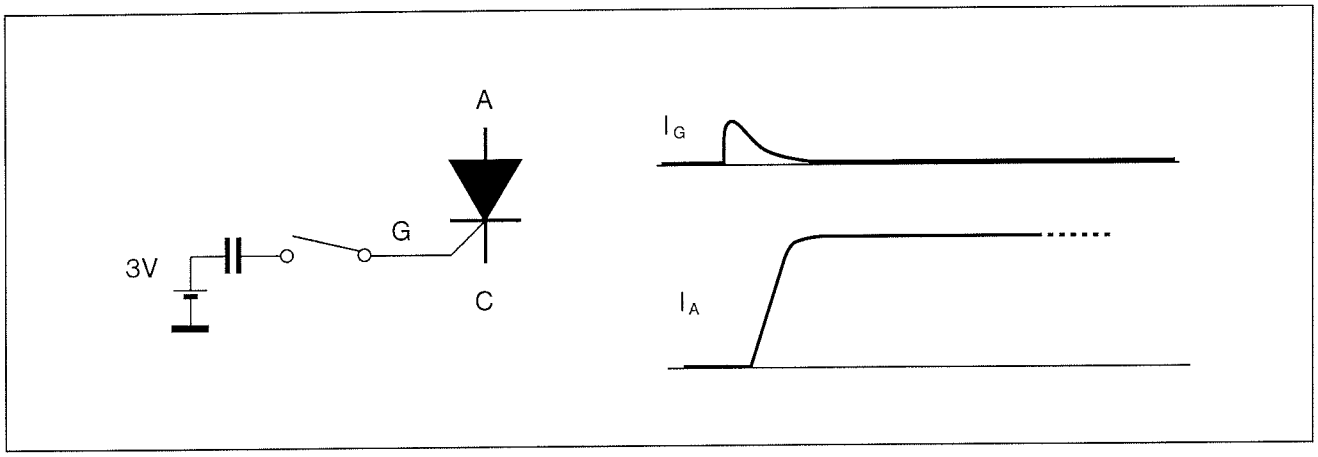

Figure 11. Thyristor drive requirements

As shown in figure 13, the TRIAC can operate in one of two ways:

a) The device is fired on only for a certain proportion of AC half waves, or

b) The firing of the device can be delayed such that only a portion of each half wave is allowed through. This is known as phase control.

Operating in the first way, the device can be used as a simple on-off AC switch, while used in the second way, the device can be used to control AC power - for example as a speed control for an AC motor.

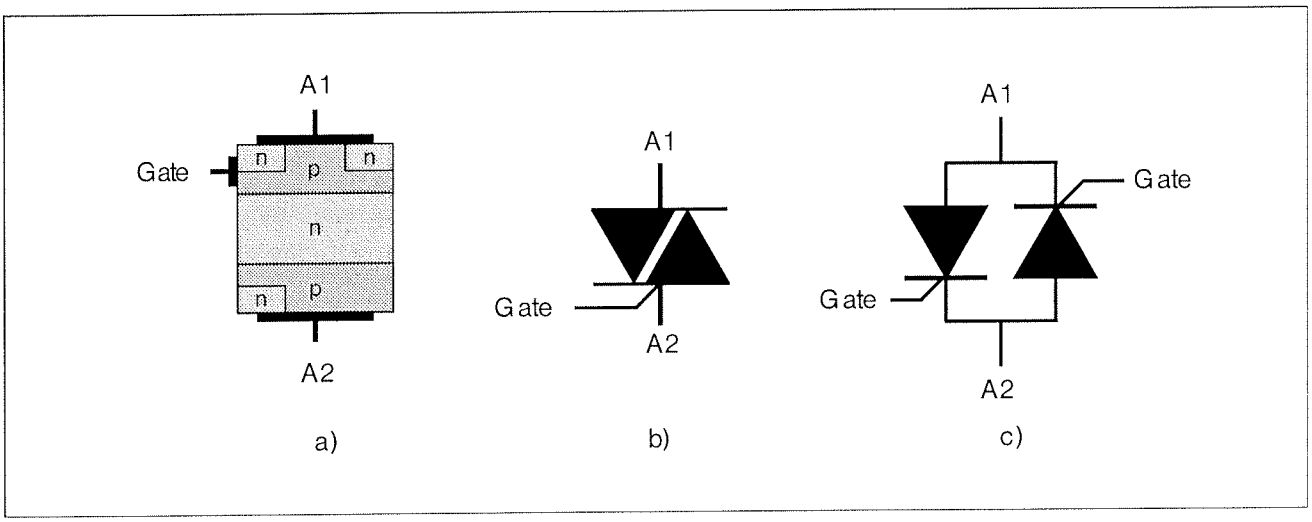

Figure 12. The TRIAC a) Simplified structure b) Circuit symbol c) Equivalent circuit

5 THE GTO see figure14.

The GTO is another "positive feedback" component and is similar to the thyristor, but it has an interdigitated structure, as shown in figure 14. Consequently it has similar characteristics to the thyristor, but it can be blocked like a transistor.

5.1 Voltage

GTOs can support up to around 4kV with a maximum rated current of 1kA. During turn-off the maximum voltage is defined by the SOA. The GTO has a poor S.O.A. when operating at high currents. Its voltage drop is marginally higher than that of the thyristor.

5.2 Drive requirements see figure 15.

The GTO requires a very high negative gate current to turn-off quickly; its has a gain of only 3 which means it requires a sophisticated and expensive gate drive if it is to be run at any speed. This means that it is often impractical to use a charge extracting drive circuit, and so the device has a "tail effect" whereby the device still conducts while the minority carriers combine naturally.

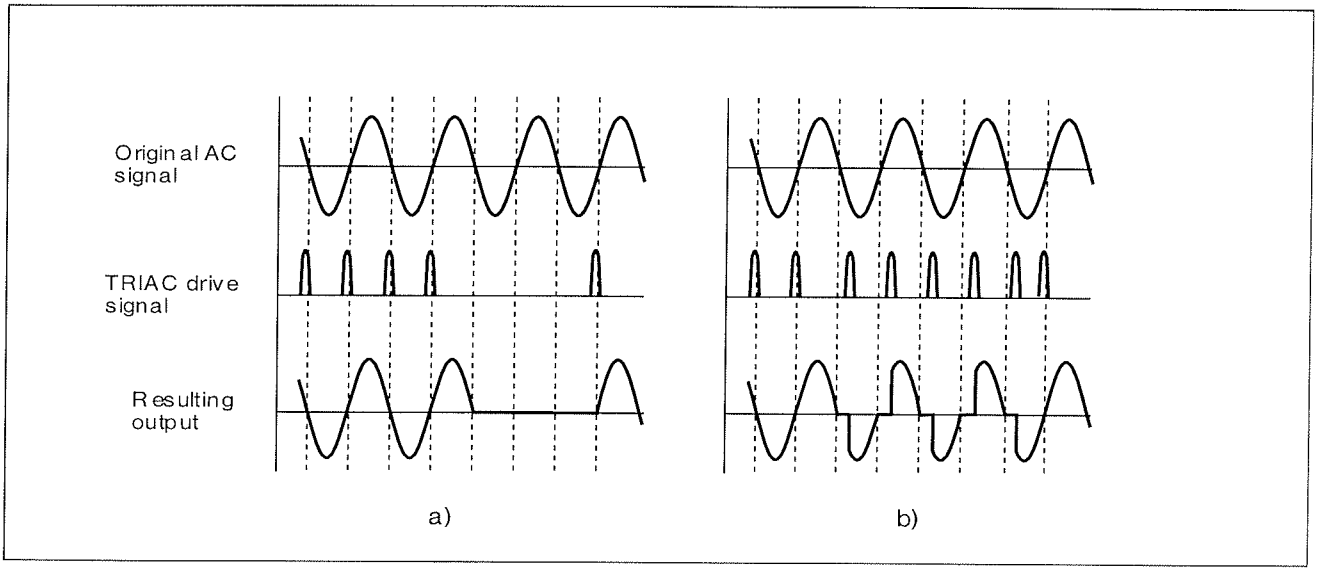

Figure 13. Driving a TRIAC: a) Using as an on-off switch b) Phase control

5.3 Switching times - see figure 16

Like the bipolar transistor the GTO has a storage time, and during the fall time its tail effect considerably increases the turn-off losses.

6 THE POWER MOSFET see figure 17.

This component uses only majority carriers in conduction, which accounts for its specific behaviour.

The majority carriers flow into the component due to the influence of gate voltage; the current cannot be limited by a "gain phenomenon". Hence the voltage drop depends only on the resistance of the silicon path between the drain and source, $R_{DS(ON)}$.

6.1 Current

The maximum operating current is defined, as for a diode, by the rate at which it is cooled. Its surge current capabil-

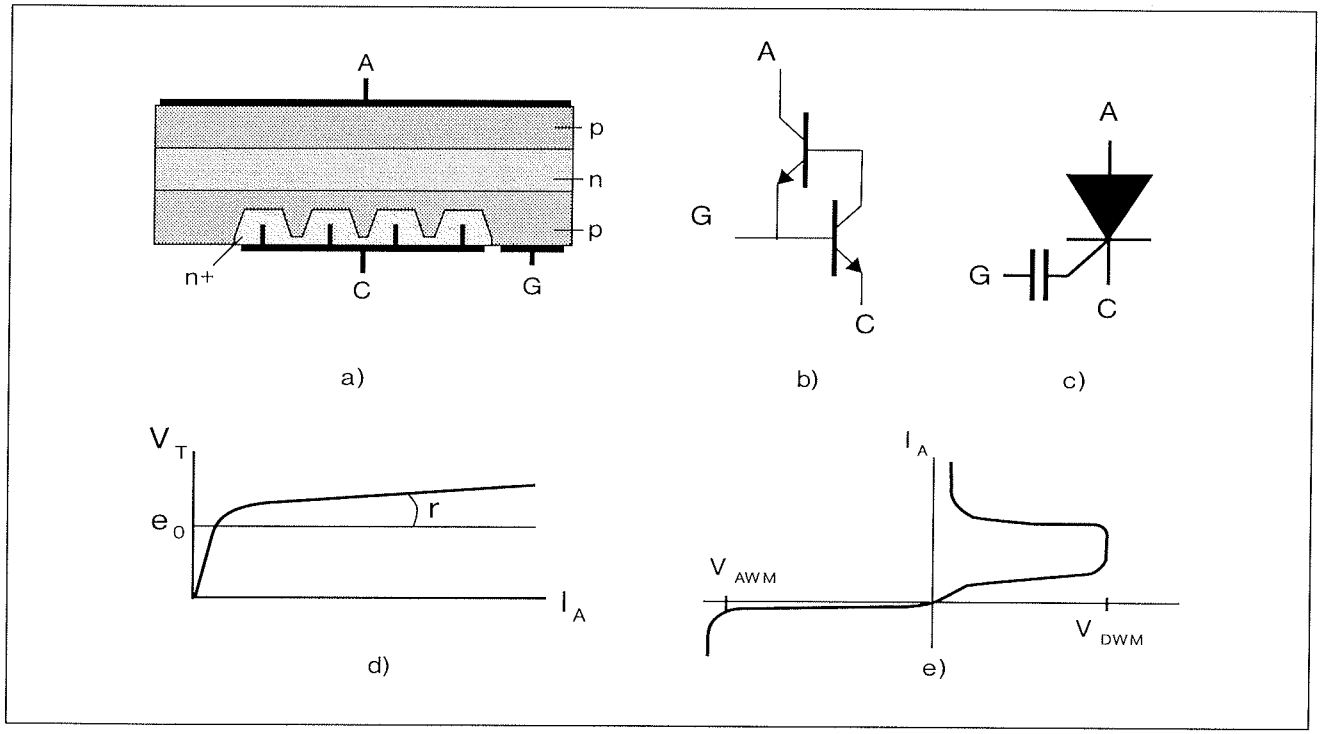

Figure 14. The Gate Turn-Off Thyristor: a) Simplified structure b) Equivalent circuit c) Circuit symbol d) Current limits e) Voltage limits

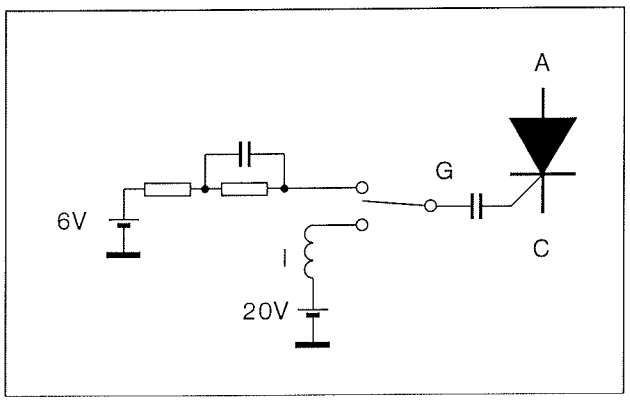

Figure 15. Driving a GTO

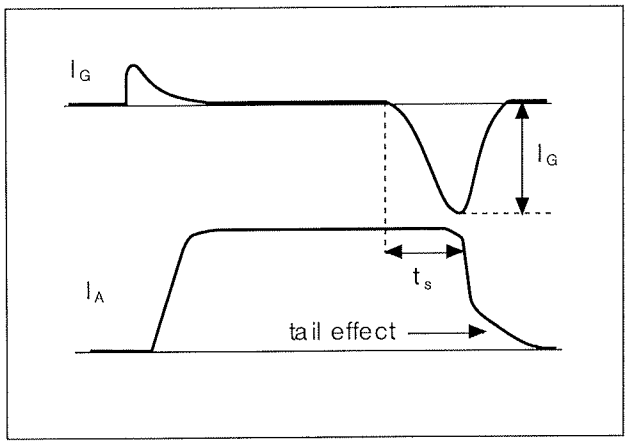

Figure 16. GTO switching times

ities are defined by the thermal time constant of cooling arrangements (figure 18).

6.2 Voltage

Because the area of silicon used and hence $R_{DS(ON)}$ increase considerably with the maximum rated voltage, this voltage is currently limited to around 1000V.

The MOSFET has a large S.O.A, as it is able to sustain its maximum rated voltage during turn-off.

Present technology current ratings are governed by the following $R_{DS(ON)}$ (25°C) values for the relevant voltage ranges.

$R_{DS(ON)}$ @ 25°C (mW)	Max. rated voltage (V)
77	100
850	500
3500	1000

It is frequently said that the MOSFET has a very high voltage drop, but this is not correct. The MOSFET voltage drop,

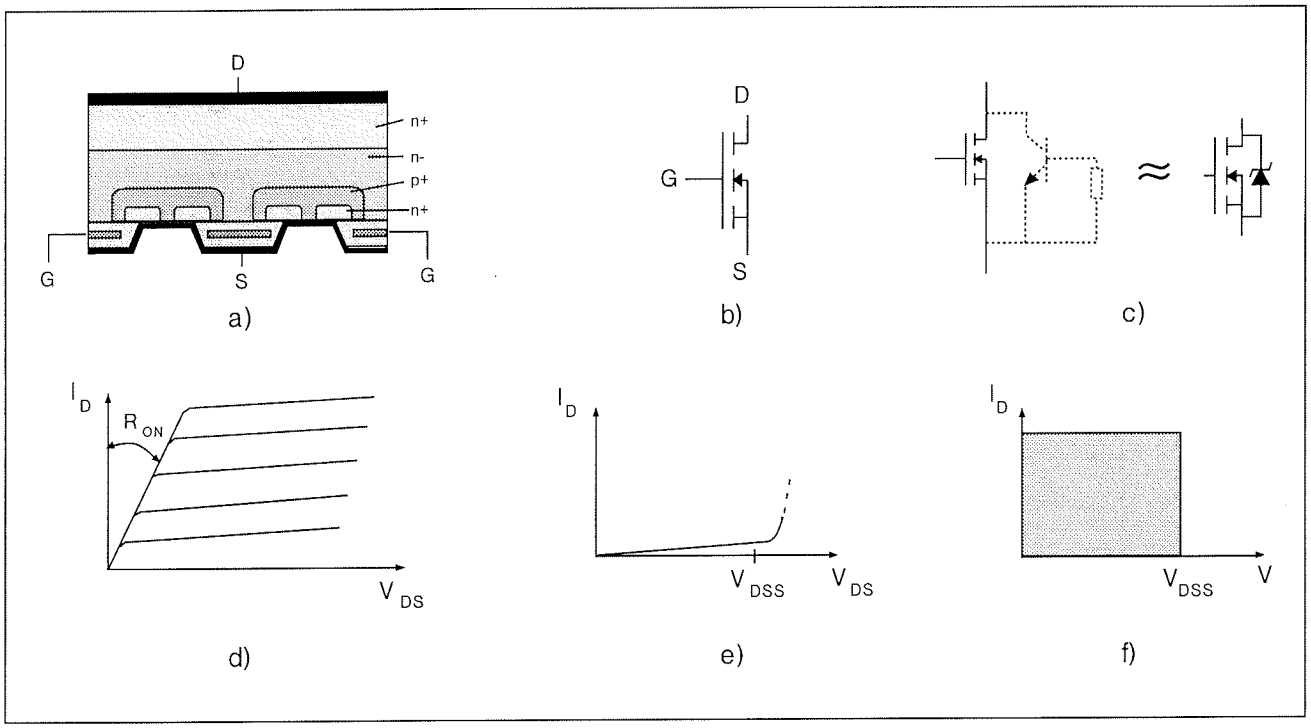

Figure 17. The Power MOSFET: a) Simplified structure
b) Circuit symbol
c) Equivalent circuit
d) Output characteristics
e)Forward breakdown characteristics
f) Switching Safe Operating Area

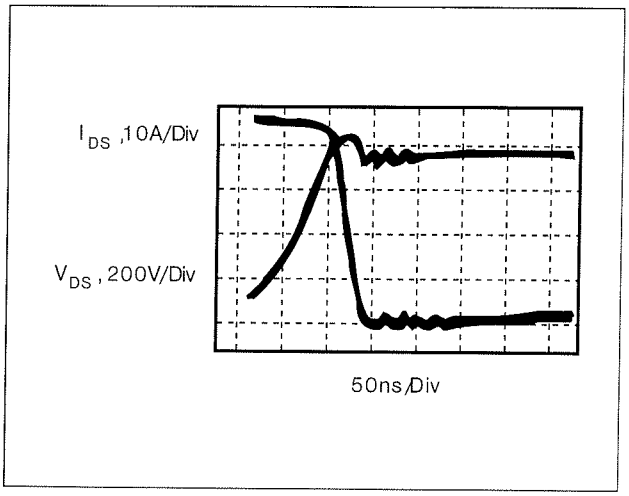

Figure 18. Turnoff with high current

$R_{DS(ON)}$.I, can be very low at a low current density, though that would be compensated by the need for a large silicon surface area.

The $R_{DS(ON)}$ is (unfortunately) specified in manufacturers datasheets at 25°C. At a more realistic operating temperature:

$$R_{DS(ON)} @ 100°C \approx 1.7 \times R_{DS(ON)} @ 25°C$$

6.3 Drive requirements

During conduction the gate requires only a voltage (approximately 15V) without any significant energy consumption - see figure 19.

MOSFETs turn off very quickly when the gate-source voltage falls to zero. However, the prescence of a capacitance between the gate and source means that to switch the device, charge must be supplied or removed to make the gate voltage rise or fall.

The designer must consider losses due to the charge/ discharge of this capacitance at each turn-on/off.

6.4 Switching times

The MOSFET, a majority carrier device, has no storage time. This is very important for many applications. Fall time (depending on drive) can be very small, but for a rated voltage higher than 300V, it is approximately the same for both fast bipolar and MOSFET devices.

7 THE IGBT see figure 20.

The IGBT can be considered as a pseudo-Darlington with a MOSFET as driver and a bipolar transistor as the power stage.

7.1 Current

The maximum current is generally limited by cooling. It has over-current capability.

7.2 Voltage

At present, the maximum rated voltage is 1.2kV. This limit is rapidly increasing towards 1800V and a maximum rated current of 500A. The SOA is approximately rectangular.

The voltage drop across the IGBT is relatively constant with respect to the current. This means that at high current levels, conduction losses are lower than those of a MOSFET, but at low current levels they are considerably higher. This causes a limit to the efficiency of IGBT circuits.

7.3 Drive requirements

Similar to the MOSFET drive (figure 21).

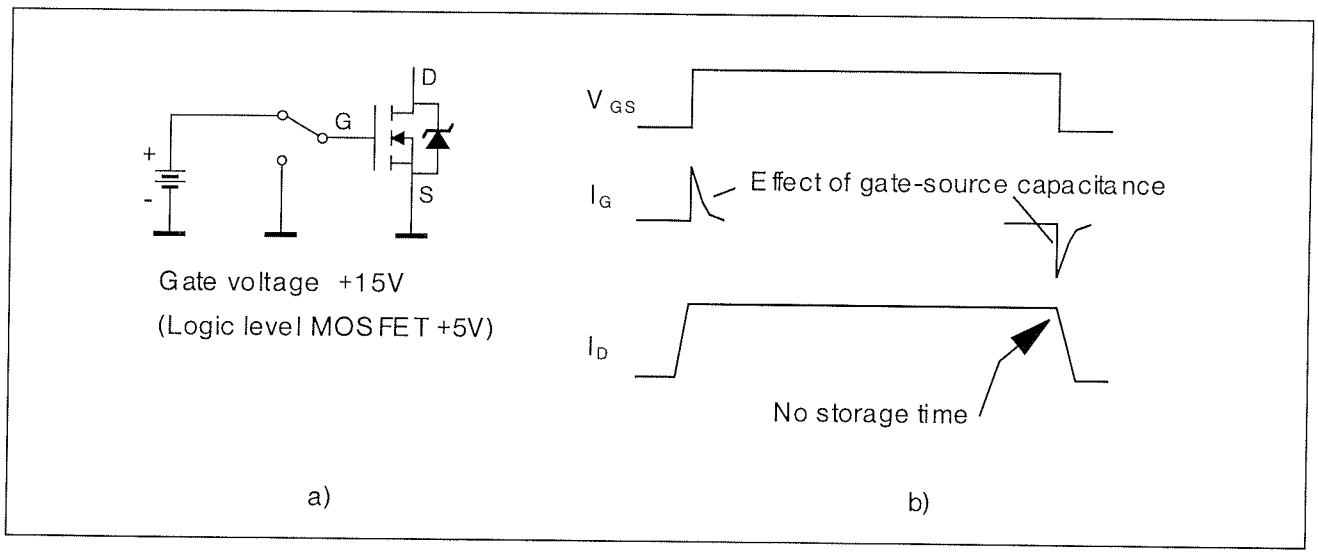

Figure 19: a) Driving a Power MOSFET b) MOSFET switching waveforms

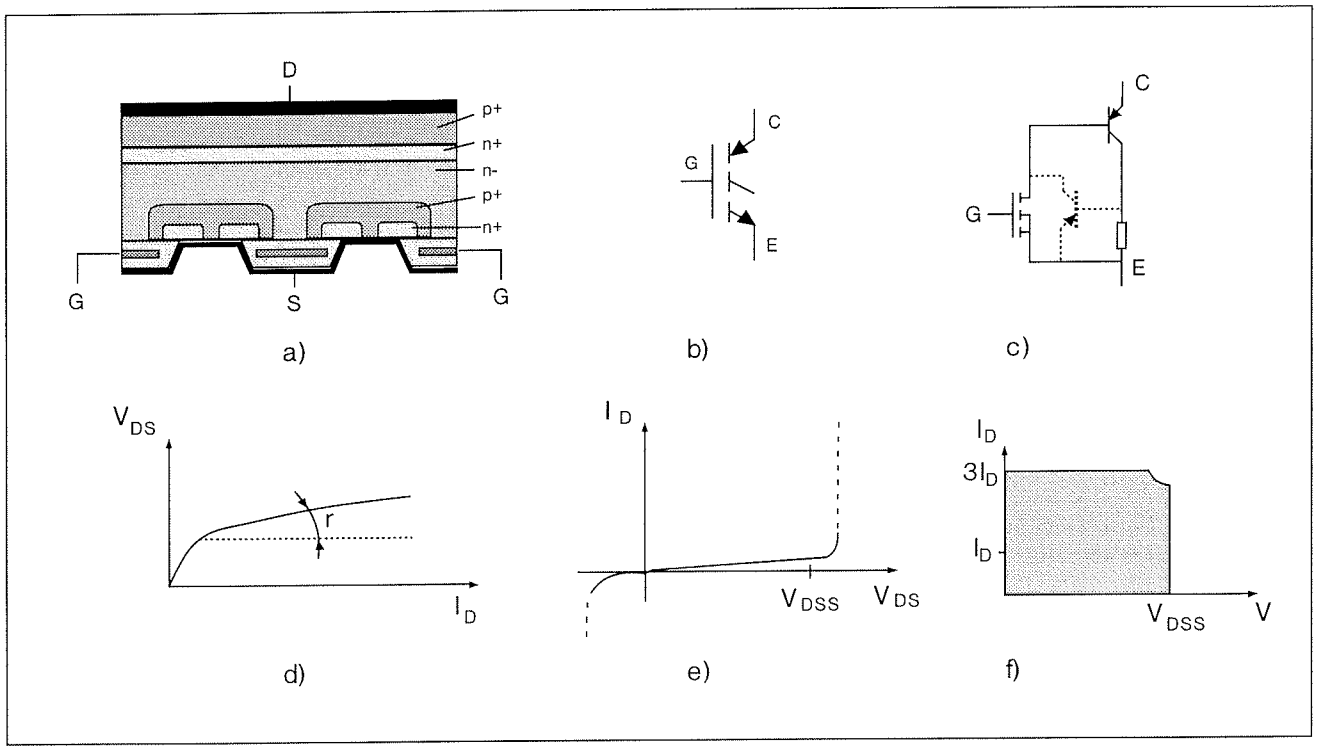

Figure 20. The IGBT: *a) Simplified structure*
b) Circuit symbol
c) Equivalent circuit
d) Output characteristics
e) Forward breakdown characteristics
f) Switching Safe Operating Area

7.4 Switching times

The MOSFET stage has practically no storage time, but the bipolar section causes a tail current like that in the GTO, where the device continues to conduct due to the prescence of residual minority carriers in the base. As the base section of the device cannot be accessed externally to remove these charges, this tail current persists until the carriers recombine naturally. This current causes switching losses, which increase with operating frequency.

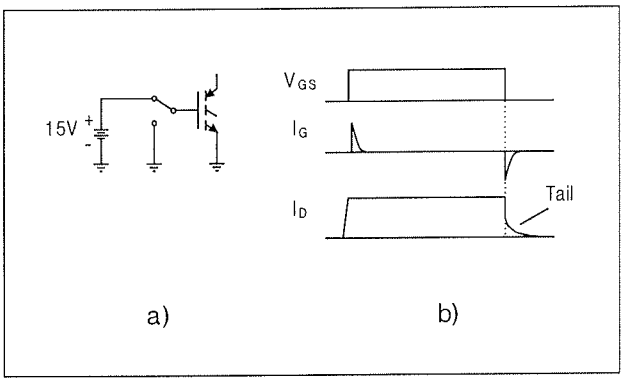

Figure 21. Driving an IGBT.
a) Driving circuit
b) Switching waveforms

8. LIMITS AND MAXIMUM RATINGS

The absolute maximum ratings are defined by the semi conductor manufacturer. These ratings must not be exceeded under any circumstances - to do so risks destroying the component. Examples of maximum ratings are the maximum junction temperature $T_{j(max)}$, the maximum current and the maximum blocking voltage.

It should be noted that the user cannot measure these parameters, as the device will probably be destroyed in the attempt. Characteristics which may be measured are for example the collector-emitter saturation voltage $V_{CE(sat)}$, and the switching times.

The manufacturer specifies a maximum and/or minimum value, depending on the parameter. In the design of circuits it is important to take into account the "worst case" value of the component, and to verify that the circuit operates correctly with the spread of all parameters.

9. CHOOSING THE RIGHT SEMICONDUCTOR

When selecting the type of semiconductor device to use in a particular application, the designer must take into account a number of factors, such as:

i) The cost of the device, and the cost constraints on the application.

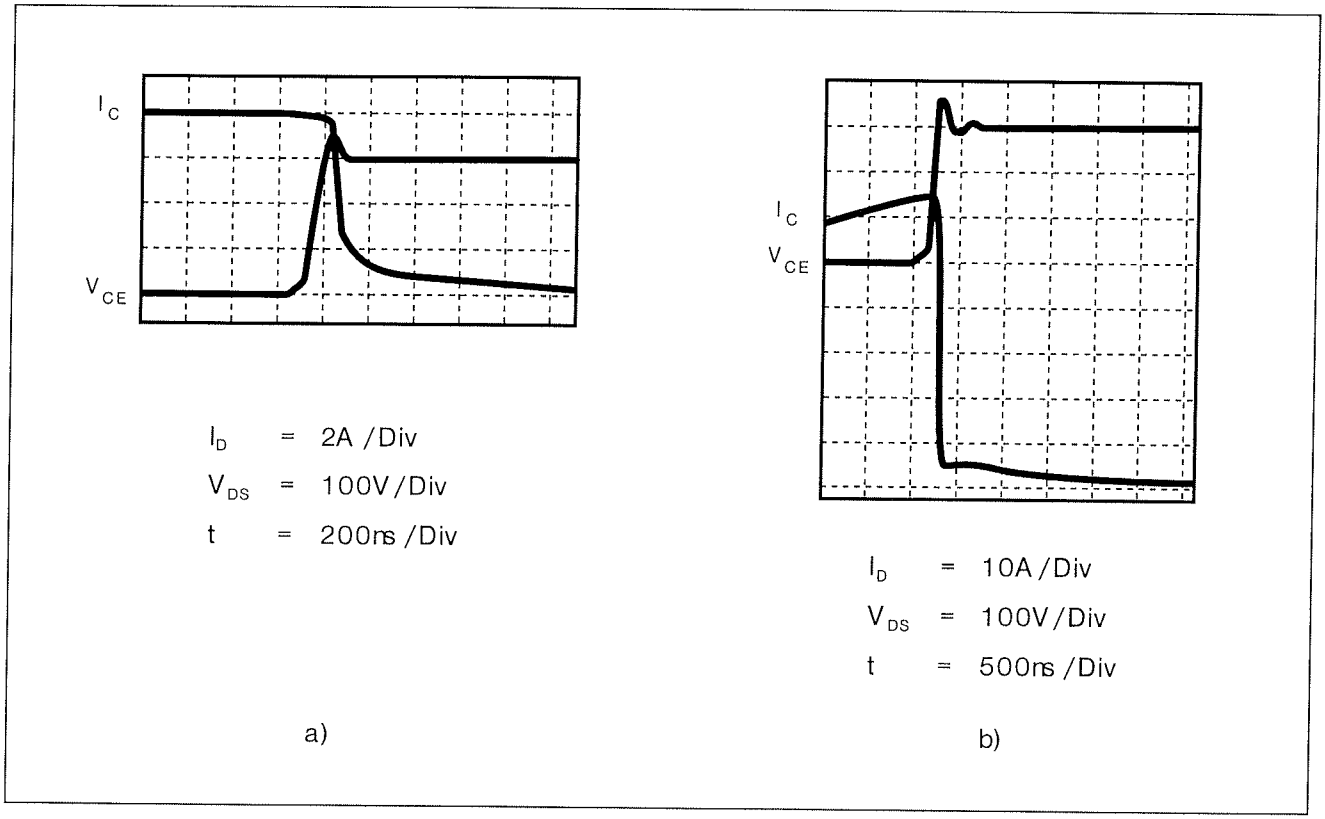

Figure 22. IGBT Switch-off behaviour: a) Normal current b) Very high surge current

ii) The magnitude of voltages and currents encountered.

iii) The drive requirements of the device - the need for a complex drive circuit can increase design time and the cost of the circuit.

iv) The frequency at which the device will switch.

9.1 Typical applications of each type

9.1.1 Bipolar transistors

In general terms bipolar transistors compete with Power MOSFETs and IGBTs. Their main advantage over these types is the lower cost, particularly for high voltage devices, while their main disadvantages are the cost of the drive circuit and the limit on their switching speed imposed by the storage and fall times. The applications in which they are used are typically characterised by low to medium operating frequency and high voltage, where they result in a cheaper solution than the equivalent MOSFET or IGBT. Examples are in electronic lamp ballasts, automotive ignition switches, and horizontal deflection circuits in TVs and monitors.

9.1.2 Power MOSFETs

The main advantages of Power MOSFETs are their minimal drive requirements and ability to operate at high frequencies. In power supplies, operation at high frequencies allows the size of circuit magnetics to be reduced, decreasing the circuit cost. In compact fluorescent lamp ballasts (such as those used in domestic environments) operating at high frequencies leads to smaller overall dimensions. The low currents and relatively low voltages in this application means that in this case the Power MOSFET leads to a cheaper solution than the power bipolar.

Power MOSFETs are also frequently used as power actuators (solid-state relays) in automotive circuits, because of the low voltages involved means that they are inexpensive, and types are available which can be driven directly from a microprocessor, which are increasingly being used to control automotive systems.

9.1.3 IGBTs

The main applications of IGBTs are in motor control and automotive ignition - again these are characterised by high voltages and relatively low operating frequencies. In these applications they compete with bipolars. Although the basic device is more expensive than a bipolar transistor, the minimal drive requirements can lead to a cheaper overall solution, particularly where there is a need to interface with a microprocessor. Its main disadvantage is the unavoidable losses caused by the tail current (which become more significant at high frequencies),

9.1.4 GTOs

GTOs are used in conditions of very high voltage and very high current, and low switching frequencies. An example of their use is in electric trains.

9.1.5 Thyristors

This component is very cheap, but its use is limited by the difficulty of turning it off. It can be used to control devices which can be fed with half-wave rectified AC current, for example DC motors (when it will turn off automatically every half cycle, like the TRIAC), and also to protect other devices, for example in power supplies.

9.1.6 TRIACs

TRIACs are unique in their ability to conduct and control current in both directions. They are the cheapest way of controlling AC currents, for example in AC motor speed controls or lamp dimmers.

11. CONCLUSION

"Power MOSFET has very high voltage drop"

"Bipolar ... an old technology"

"Epitaxial is better..."

This type of commercial jargon does not help the designer to produce optimal circuits. At the present time the designer has a choice between a lot of components. Which is the best solution? The answer is, there is no best solution - this is the field of technical design, not scientific research.

For some applications, for example 1MHz Switch Mode Power Supplies, only one solution (MOSFET) is possible. For most applications, there are always several solutions. The designer's job is to optimize the "switching function"after thorough analysis. Experience shows that the quality of this analysis, and the work done by the designer (drive, protection, etc.) play a bigger role in the total cost than the actual price of the component.

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/2/ Power Transistor application manual SGS-THOMSON 1989

/3/ Parallel Operation of Fast Rectifiers SGS-THOMSON Application Note

Posvet o senzorjih v Zavodu TC SEMTO dne 15. 03. 2002
Workshop on Sensors within Zavod TC SEMTO on March 15th, 2002

Igor Pompe, Zavod TC SEMTO, Ljubljana, Slovenija

Ključne besede: posvet o senzorjih, sensorji, senzorski sistemi, kooperacija

Povzetek - 15. 03. 2002 je Zavod TC SEMTO v prostorih Fakultete za elektrotehniko, Univerze v Ljubljani organiziral posvet o senzorjih. Na posvet so bili vabljeni tudi nečlani, zastopniki industrije, ki je aktivna na tem področju. Profesorji Fakultete za elektrotehniko so imeli uvodne referate, na katerih so pregledno predstavili problematiko senzorjev in njihovo vgradnjo v elektronske sisteme. Zastopniki industrije so predstavili svojo aktivnost na tem področju in ponudili svoje sodelovanje.

Keywords: conference on sensors, sensors, sensor system, cooperation

Abstract - On March 15th Zavod TC SEMTO has organised Conference - Information on Sensors in the premises of Faculty for Electrical Engineering, University of Ljubljana. We have invited also non-members, the representatives of the industry, active in this field. The professors of the Faculty gave the introductory lectures in which the sensors problematic and their implementation in the electronic systems has been clearly introduced. The representatives of the industry have presented their activity in this field and offered their cooperation.

Zavod TC SEMTO (Tehnološki center za sklope, elemente, materiale, tehnologije in opremo za elektrotehniko , Stegne 25, Ljubljana) ima nalogo svoje člane seznanjati z novostmi na njihovem področju delovanja ter z aktivnostmi in razpoložljivostjo znanja pri posameznih članih. Tako za člane organizira delavnice in posvete, na katerih vabljeni strokovnjaki vodijo razgovore o temah, zanimivih za več članov in posamezni člani postavljajo vprašanja ter seznanijo druge s svojimi dosežki, možnostmi sodelovanja ali potrebami po razvojnem sodelovanju na obravnavanem področju.

Tako je v tem letu Zavod TC SEMTO že organiziral delavnico za pripravo poslovnih načrtov in razvojnih projektov in posvet o senzorjih. Povzetke prispevkov nekaterih avtorjev na posvetu priobčamo v tej številki revije Informacije Midem. Upamo, da bo ta objava spodbudila tudi uporabnike senzorjev, ki se posveta niso udeležili, k navezavi stikov s proizvajalci senzorjev ali imetniki tehnologij, potrebnih za proizvodnjo senzorjev. Proizvajalcem senzorjev bodo pogledi uporabnikov zelo dragoceni.

V okviru tehnološkega centra je možno organizirati razvojno-raziskovalne projekte na temah, zanimivih za več uporabnikov.

Seznam predstavljenih referatov z izvlečki (OPOMBA : referati bodo v celoti objavljeni v eni izmed naslednjih številk revije Informacije MIDEM) :

S.Amon, D.Vrtačnik, D.Resnik, U.Aljančič, M.Možek

Laboratorij za mikrosenzorske strukture - LMS FE UL, Ljubljana, Slovenia

Osnovne značilnosti senzorjev

IZVLEČEK: Uvodoma bodo predstavljene nekatere osnovne definicije s področja senzorjev in pomembnejši ključi razdelitve senzorskih družin. Podrobneje bodo razložene izbrane senzorske lastnosti kot so npr. prenosna funkcija, občutljivost, točnost, ločljivost, selektivnost, šum, nelinearnost in drugo. Shematsko bo predstavljen tudi princip zajemanja podatkov na osebnem računalniku. V nadaljevanju prispevka bo predstavljena raziskovalno - razvojna dejavnost na področju mikrosenzorskih struktur v LMS. Poudarek bo na predstavitvi postopkov mikroobdelave in aplikacijah, ki so bile v Laboratoriju zasnovane. Na koncu bomo podali pregled lastnosti inteligentnih senzorjev, ki predstavljajo eno izmed glavnih smernic razvoja modernih senzorskih struktur.

Leopold Knez,

Iskra Feriti, Ljubljana, Slovenija:

Induktivni senzorji

IZVLEČEK: Induktivni senzorji so gradniki nekontaktnih stikal. Uporabljamo jih v avtomatiki in profesionalni elektroniki za merjenje razdalj, razpoznavanje kovin in krmiljenje aktuatorjev. Za zanesljivo delovanje je treba izbrati primeren feritni material, ki ima majhen izgubni faktor $\tan\delta/\mu_i$ in čim manjši temperaturni koeficient permeabilnosti α_F. V članku opisujemo princip delovanja induktivnega senzorja, induktivnega stikala, pojasnjujemo nekatere parametre in sklenemo s praktičnim izračunom senzorske tuljavice. Izračunu dodajamo še meritve induktivnega senzorja L14 za primerjavo.

Janez Holc[1], Marija Kosec[1], Franck Levassort[2], Louis Pascal Tran-Huu-Hue[2] in Marc Lethiecq[2]

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[2]LUSSI/GIP Ultrasons, EIVL, François Rabelais University, Blois cedex, Francija

Integrirani ultrazvočni piezoelektrični pretvorniki za uporabo v medicini

IZVLEČEK: Za izdelavo medicinskih visokofrekvenčnih ultrazvočnih pretvornikov je potrebna zelo tanka piezoelektrična keramika, debeline nekaj 10 mm. Navadno se izdeluje piezoelektrične elemente z rezanjem in tanjšanjem kosa keramike. Zaradi majhne debeline elementa lahko nastane pri lepljenju na podporni dušilec (backing) krušenje in lomljenje. Problem smo rešili tako, da smo na primeren nosilec, ki je imel tudi vlogo dušilca z debeloplastno tehnologijo nanesli piezoelektrično plast. Pretvornik smo izdelali na pozlačenem poroznem nosilcu $Pb(Zr,Ti)O_3$ (PZT). Debelina piezoelektrične PZT-plasti je okoli 40 μm. Zaradi velikega dušenje poroznega PZT- nosilca, njegove primerljive akustične impendance in plasti, ima izdelan modelni pretvornik ustrezno frekvenčno karakteristiko. Zaradi podobne kemijske sestave nosilca in plasti je minimalna tudi kemijska in fizikalna interakcija med plastjo in podlago, kot sta na primer difuzija zaradi podobne sestave in dobro ujemanje termičnih raztezkov.

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Mikrosistemi z integriranimi kapacitivnimi, magnetnimi in optičnimi senzorji

IZVLEČEK: Članek obravnava mikrosisteme z integriranimi senzorji za merjenje fizikalnih veličin kot so pospešek, električni tok in gibanje. Za vsako veličino je predstavljen integrirani mikrosistem, ki je sestavljen iz senzorjev in obdelovalne elektronike, ki sta integrirani na istem silicijevem substratu. Poudarek članka je na predstavitvi integriranih senzorjev.

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Elektronika na poti od detektorja do osrednjega dela sistema

IZVLEČEK: Senzorski sistem smo razčlenili na elektronska vezja, ki jih srečamo na poti od detektorja do osrednjega dela. Opredelili smo najpomembnejše osnovne gradnike in izvedbe ojačevalnikov ter opisali način in realizacijo odjema upornosti, napetosti, toka in naboja. Podali smo zgled delovanja optoelektronskega detektorskega polja. Pri prenosu signalov smo se posvetili zmanjševanju vpliva motilnih signalov s tokovno zanko.

F.Koplan,

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ABS-senzorji na osnovi AlNiCo-magnetov

IZVLEČEK: Predstavljamo fizikalne osnove in princip delovanja ABS-sistema, zahteve za vgrajene AlNiCo-magnete, ki so ključni element senzorja. Ilustriramo izdelavo samega ABS-senzorja, najpomembnejše značilne elektromagnetne lastnosti senzorja kot osnovo za nadaljnji razvoj elektronskega krmilnega modula ali alternativnih rešitev ter sprememb samega senzorja. Predstavljena je tudi možnost podjetja, da ponudi proizvode z večjo stopnjo integracije za nove potrebe trga ter izsledke razvojno raziskovalnega dela na področju razvoja opreme za kontroliranje in preskušanje magnetov za potrebe drugih področij raziskovalnega dela, proizvodnje elektronskih komponent ter izdelovanja magnetnih sistemov.

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Debeloplastna tehnologija za senzorske aplikacije

IZVLEČEK: Kljub pospešenemu razvoju mikrosistemske tehnike, ki je integracija številnih področij, kot so: senzorika, aktorika, mikroperiferika, mikromehanika, integrirana optika itd., so prevladujoče tehnologije za izdelavo senzorjev in pripadajoče elektronike še vedno monolitne polprevodniške tehnologije ter tankoplastna in debeloplastna tehnologija. Debeloplastna tehnologija lahko pri izdelavi senzorjev nastopa v dveh vlogah. Prva je izdelava debeloplastnega senzorskega elementa. Druga pa je integriranje senzorskega elementa, ki navadno ni debeloplasten, s kompenzacijskimi elementi in elektroniko za obdelavo električnega signala. V prispevku so prikazane predvsem nekatere aplikacije na področju senzorjev mehanskih veličin (senzorji tlaka in sile), kjer je uporabljena debeloplastna tehnologija v eni ali obeh naštetih vlogah.

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Senzorji tlaka za medicinsko in industrijsko uporabo

IZVLEČEK: Družba HIPOT-HYB že vrsto let proizvaja, poleg hibridnih debeloplastnih vezij, tudi senzorje tlaka za medicinsko in industrijsko uporabo. Razvoj tehnologije in zahteve trga usmerjajo tudi razvojno dejavnost. V prispevku bo predstavljena raziskovalno-razvojna dejavnost na področju senzorjev tlaka. Njeni dosežki na tem področju bodo ilustrirani z nekaterimi značilnimi primeri, njene usmeritve pa bodo prikazana na primeru pametnega senzorja tlaka.

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Vloga senzorjev v sistemih vodenja procesov

IZVLEČEK : Pri načrtovanju in vzdrževanju sistemov vodenja v industriji igrajo senzorji odločilno vlogo. Inženirji avtomatike morajo namreč upoštevati dejstvo, da je nemogoče regulirati, če ni na razpolago ustrezno natančnih meritev. Pri tem je pomembna tudi njihova izvedba, saj morajo biti prilagojeni okolju, v katerem delujejo, tako po zgradbi kot tudi v smislu dinamičnih lastnosti. Zato je izbira, vgradnja in vzdrževanje merilnih sistemov kompleksen postopek, ki je odločilen za uspešno delovanje obravnavanega procesa.

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Strokovna revija za mikroelektroniko, elektronske sestavine dele in materiale

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