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Dear Reader,

This issue brings three invited papers of distinguished lecturers at the 50th International Conference on Microelectronics, Devices and Materials – MIDEM 2014 that took place in Ljubljana, Slovenia in Oct 2014. They provide insights to the state-of-the-art achievements in three important areas of electronics: integrated sensors, embedded and cyber-physical systems and reliability of electron devices. The MIDEM 2014 conference was a big success and we expose the golden (50th) conference on the front cover page and with an opening speech at the Celebration Academy MIDEM-50.

An Editorial of the last issue should reveal some statistics. In 2014 we have received more than 150 manuscripts, out of which 36 have already been accepted for publication (4 review scientific papers, 26 original scientific papers and 6 Professional Articles), whereas more than 90 were rejected and the remaining ones are still under review. Despite a well defined title of our journal and on-line instructions for authors we receive each year a few manuscripts that are out of our journal's scope. The success rate of 30% in 2014 reflects a good foundation for the long-term quality growth of the journal. I would like to sincerely thank all reviewers for their valuable contribution to the journal quality and growing reputation. Commitment of Editorial Board Members to high quality review process paths a way toward a better profiling of our journal.

Institutional support for our journal has been decreasing in the last two years. To cover publishing costs and to secure continuation of quality growth we need to introduce page charges for papers published in the journal. We will continue to provide a free electronic access to all papers published in *Informacije MIDEM* –Journal of Microelectronics, Electronics Components and Materials (since 1986).

Let the last December days bring festive atmosphere, joy and peace in each home, office or research laboratory. It is the time to look back, but also to look ahead ambitiously and make plans for the coming year. This brings me to editorial wishes for 2015. As a part of your success we look forward to receiving your next manuscript(s) in our inbox (editor@midem-drustvo.si).

Merry Christmas and a Happy and Prosperous New Year!

Prof. Marko Topič
Editor-in-Chief

P.S.
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Review scientific paper

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Integrated Hall Magnetic Angle Sensors

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Abstract: A magnetic angle sensor is a matched combination of a permanent magnet, affixed to a rotating shaft, and a magnetic field sensor. The magnet part of the angle sensors is configured so as to create either a magnetic field with an angle-dependent component perpendicular to the chip surface; or two angle-dependent components parallel with the chip surface. The magnetic field component perpendicular to the sensor dice is measured by planar Hall devices. The two in-plane magnetic field components are measured either by a combination of planar Hall devices and an integrated magnetic flux concentrator (IMC-Hall), or by vertical Hall devices. The IMC-Hall is the most used technology for implementing a compass in mobile telephones. The circular vertical Hall device is most suitable for high-speed rotation angle sensing. The major performance-limiting factors of magnetic angle sensors are non-uniformity of magnets, imperfections in the integrated magnetic sensor IC, and thermal drift. The magnetic sensing part of contemporary magnetic angle sensors is a CMOS IC, incorporating Hall devices, biasing circuit, amplifiers and other analog signal conditioning circuits, analog-to-digital convertors, and digital circuits for angle retrieval and correction of errors.

Keywords: magnetic angle sensor, Hall device, compass

Integriran Hallov magnetni senzor kota

Izvleček: Magnetni senzor kota je kombinacija trajnega magneta, nameščenega na rotirajoč držaj, in senzorja magnetnega polja. Magnetni dela senzorja kota je konfiguriran tako, da ali ustvarja magnetno polje s kotno komponento pravokotno na površino čipa ali dve kotno odvisni komponenti vzporedni s površino čipa. Magnetno polje v normali s površino čipa se meri s planarno Hallovo napravo. Dve planarni komponenti magnetnega polja se merita lahko s kombinacijo planarnega Hallovega senzorja in integriranega koncentratorja magnetnega pretoka (IMC-Hall) ali pa z dvema vertikalnima Hallovima senzorjema. IMC-Hall je najbolj uporabljena tehnologija za izdelavo kompasa v mobilnih telefonih. Rotirajoča vertikalna Hallova naprava je bolj primerna za zaznavanje rotirajočih kotov z veliko hitrostjo. Največje omejitve lastnosti magnetnih kotnih senzorjev je nehomogenost magneta, nehomogenost integriranega magnetnega senzorja in temperaturne spremembe. Magnetni senzorski del kotnega senzorja je CMOS integrirano vezje, ki vključuje Hallove senzorje, usmerniško vezje, ojačevalec in ostala analogna vezja, analogno digitalne pretvornike in digitalno vezje za kompenzacijo in popravljanje napak.

Ključne besede: magnetni senzor kota, Hallov sensor, kompas

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1 Introduction

An angle sensor converts the angular position of a rotating mechanical part into a corresponding electronic signal. The oldest known angle sensors were based on the sliding-contact resistor potentiometer. Modern angle sensors are contactless and consequently much more reliable. Contactless angle sensors may be based on various operating principles, including optical, capacitive, inductive, and magnetic. Optical angle sensors, better known as optical (angle) encoders, have the best performance, but they are also the most expensive. In a large application area requiring accuracy up to 0.1°, magnetic angle sensors have by far the best performance – price ratio. By analogy with optical encoders, magnetic angle sensors are also called magnetic angle encoders, particularly if they have a digital output signal.

A magnetic angle sensor consists of a combination of a permanent magnet and an adequate magnetic sensor, as shown in Figure 1. The magnet is typically mounted on a rotating shaft so that the magnetic field sensed by the magnetic sensor also rotates. The angular position of the magnet, and so also of the shaft, can be then retrieved from the output signals of the magnetic sensor. The structure shown in Figure 1 is called end-of-shaft configuration. If the end of a shaft is not available, then the shaft may be inserted into a hole in the magnet, and the magnetic sensor is positioned off-axis, near the magnet. This configuration is known as trough-shaft or side-shaft magnetic angle sensor.

The notion of angle is closely related with the notion of direction. Since direction is the basic property of a

vector, a magnetic vector sensor can be readily used as an angle sensor. But in most cases, the form of the magnetic field in the magnetic angle sensor is such that the associated magnetic sensor needs to measure only two, and in some cases even only one component of the magnetic field.

A compass can be also considered as a kind of magnetic angle sensor, in which the role of the magnet plays Earth. But a good electronic compass has to measure all three components of the Earth's magnetic field, that is, it should be a magnetic vector sensor.

Magnetic angle sensors provide contactless measurement, can work in harsh environments, and are inexpensive. Good magnetic angle sensors have measurement range from 0° to 360°, without a dead angle, and absolute accuracy up to 0.1°.

Magnetic angle sensors are typically applied as contactless potentiometers, valve position sensors, single- and two-axis joysticks, motor shaft angle sensors, compasses, etc. They are widely used in industrial, automotive, and consumer products.

The maximum rotation velocity in most magnetic sensor applications do not exceed a few thousands rotations per minute (rpm). But in order to insure a low delay between an instantaneous angular position and the related output signal of the angle sensor, it is often necessary that the angle sensor's bandwidth is several tens of kHz. Moreover, there are applications where a much higher sensor's bandwidth is required, for example: high performance hard disc drives rotate at 15 000 rpm, the fastest gas turbine engines reach 165 000 rpm, electromechanical batteries can reach 200 000 rpm, to mention but a few.

The magnetic sensors applied in magnetic angle sensors may be Hall devices [1] or ferromagnetic magneto-resistors, i.e., AMRs [2] and GMRs [3, 4]. Hall devices have a great advantage of being fully compatible with IC technologies, which allows for making a Hall magnetic sensor as an application-specific integrated circuit (ASIC). Accordingly, a modern magnetic sensor typically incorporates a single Hall magnetic sensor IC chip, containing Hall elements, biasing and signal conditional electronics, and means for angle retrieval.

In this paper I will review the most successful contemporary concepts of magnetic angle sensors based on integrated Hall magnetic sensors. This is an updated version of an earlier review [5]. In the present paper I will also briefly discuss the magnets for magnetic angle sensors.

2 Angle sensors based on classical hall devices

A classical Hall device is a plate-like structure with 4 contacts, also called a Hall plate [1]. When implemented by using integrated circuit technology, a Hall plate is positioned "horizontally" (in parallel) with respect to the surface of the IC dice. For this reason, a classical Hall device is sometimes referred to as a horizontal Hall device. A Hall plate responds to a magnetic field that is perpendicular to its plane. Therefore, the magnets of the first Hall magnetic angle sensors were designed so as to provide a convenient angular dependence of the component of the magnet's field perpendicular to the Hall sensor chip. One concept of such magnetic angle sensors, which is still much used, is illustrated in Figure 1.

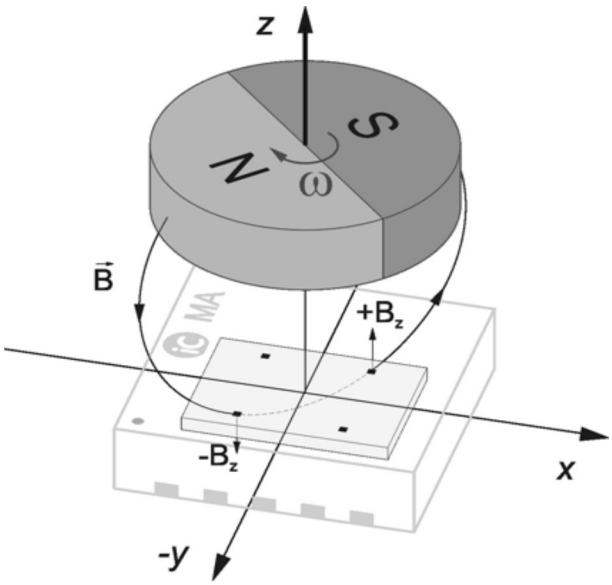

Figure 1: A magnetic angle sensor based on an integrated array of Hall plates.

Figure 1 illustrates a magnetic angle sensor based on an integrated array of Hall plates [6, 7]. In this concept, several "horizontal" Hall plates measure the local vertical components of the magnetic field carried by a radially polarized magnet, which is fixed on the end of a shaft. In the Hall sensor chip, the difference of the magnetic fields "seen" by the diametrically positioned Hall plates (for example, +Bz – (–Bz) in Figure 1) is built. As the magnet turns, this difference varies as the sinus or cosine of the rotation angle. The rotation angle can be retrieved from the output signals of at least two pairs of the Hall devices in several ways – see Section 6.

A sensor like that in Figure 1 can measure angles at end-of-shaft over the whole range 0° to 360°. Thanks to the differential measurement, several parasitic effects cancel, including the matched parts of the offsets

of the diametrically positioned Hall plates and the external magnetic fields. An unpleasant feature of this concept is that, for good performance at a reasonable distance magnet – chip, it requires the Hall elements to be positioned on a circle of a relatively large diameter, typically ≥ 2mm. Therefore, the IC-chip of such an angle sensor can be neither very small nor very inexpensive. Moreover, this concept is not convenient for trough-shaft angle sensors.

3 Angle sensors based on hall sensors with magnetoconcentrator

If combined with a "soft" ferromagnetic plate, in the way illustrated in Figure 2, a group of horizontal Hall device can be converted into a magnetic sensor that responds to all tree components of magnetic field [8]. The ferromagnetic plate functions as a magnetic flux concentrator. An integrated combination Hall plates – magnetic flux concentrator (in short: integrated magneto-concentrator or IMC) can be used to build a two-axis or three-axis Hall magnetic field sensor.

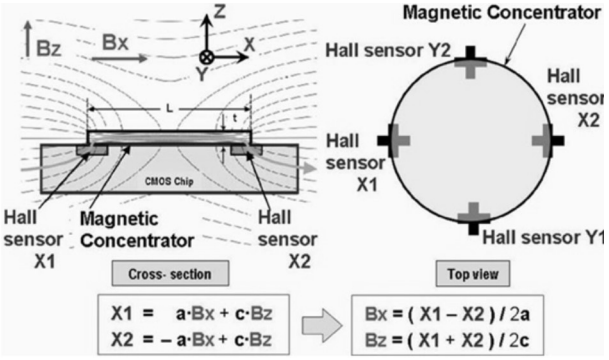

Figure 2: The principle of the IMC-Hall two-axis or three-axis magnetic field sensor (figure from [9]).

In Figure 2, the IMC has the form of a thin disk. The Hall elements are positioned under the periphery of the disk. For each horizontal sensing axis (X and Y) there are two Hall elements placed at the two opposite ends of the disk diameter parallel with the corresponding axis. The concentration of the magnetic flux lines by IMC produces (locally, near the Hall plates) the perpendicular components of a magnetic field B. The difference of the output signals of the Hall plates X1 and X2 is proportional to the parallel field component Bx. The By component is measured in the analogous way. The Bz component is the sum of all Hall signals.

A two-axis (X and Y) version of an IMC-Hall magnetic sensor, combined with a permanent magnet like that in Figure 1, gives a magnetic angle sensor. As the in-chip-plane component of the magnetic field of the magnet rotates for an angle α, the difference of the Hall voltages of the two non-neighboring Hall elements vary as cosα and sinα. The angular position of the magnet can be found from these two signals - see Section 6. This device provides, without any calibration, accuracy better that 0.5° over the measurement range of 360° [8].

The main advantages of an angle sensor based on the IMC-Hall combination are robustness and scalability. For the in-chip-plane component of the magnetic field, the IMC provides a magnetic gain, which is illustrated by the high density of the magnetic flux lines penetrating the Hall plates in Figure 2. This leads to a good signal to noise ratio of the sensor, even when the magnet is small or is placed at a relatively large distance from the IMC-Hall chip. For these reasons, an IMC-Hall angle sensor is very immune to the variations of the shape, strength, and the position of the applied permanent magnet. The magnetic field sensing area of an IMC-Hall sensor typically occupies very small portion of the sensor IC chip area, and does not hamper miniaturization of the chip. The IMC-Hall technology enabled development and successful commercialization of a number of IC for magnetic angle sensors and some other products [10]. An IMC-Hall IC for magnetic angle sensors is suitable also for the implementation of through-shaft angle sensors [11]

But the IMC-Hall technology brings about also some secondary effects that limit the range of the magnetic fields in which an IMC-Hall angle sensor functions well. At high magnetic fields the magnetic saturation of the magnetic flux concentrator produces nonlinearity error [12]. In some commercially-available IMC-Hall angle sensor ICs, the saturation starts when the external flux density reaches 60mT. At low magnetic fields, two other effects may deteriorate angle measurement accuracy. One is perming – a remnant magnetization of the IMC, which may produce in the Hall elements an unpredictable offset field of some micro-tesla. The other is the influence of external magnetic field, which is also amplified by IMC, and cannot be distinguished from the local field carried by the rotating magnet.

The deposition and structuring of the IMC requires post-processing of the Hall IC wafers. Therefore, at the same other circumstances, an IMC-Hall sensor has to be more expensive than a "bare" Hall sensor.

4 Angle sensors based on vertical hall devices

In a vertical Hall device [13] the region that plays the role of the Hall plate is made to be perpendicular to the

chip plane (therefore the attribute "vertical"). A merged combination of two mutually orthogonal vertical Hall devices gives a good magnetic sensor for the simultaneous sensing of the two in-plane components of a magnetic field. Based on this device a magnetic angle sensor was demonstrated [14]. But this first two-axis vertical Hall device was fabricated in a specific process, which is not compatible with modern IC technologies. Later, we developed also integrated vertical Hall devices: we applied a high-voltage CMOS technology, and used the deep n-well for the active region of the vertical Hall device. An integrated magnetic angle sensor based on such integrated vertical Hall devices [15] has similar performance as the one based on the IMC-Hall technology.

The most recently developed magnetic angle sensors are based on the circular vertical Hall device (CVHD) [16, 17]. The CVHD is illustrated in Figure 3. The active region of this device is a deep N-well ring, on whose surface are positioned several equally spaced N+ contacts. Any adjacent 5 contacts and the corresponding segment of the N-well make a vertical Hall device. The contacts can be connected to a current source and/or to an amplifier via an array of CMOS switches. By activating the appropriate switches, the active 5-contact-portion of the ring can be moved, step by step, around the ring. This is equivalent with moving a vertical Hall device around the ring. At each instant, the magnetic sensitivity vector of the device is collinear with the radius vector of the central contact of the currently active vertical Hall device. That means that the magnetic sensitivity vector of the CVHD rotates. The Hall voltage of a Hall device is given by the scalar product

$$Vh \approx \mathbf{S} * \mathbf{B} \quad (1)$$

where **S** denotes the magnetic sensitivity vector of the Hall device and **B** denotes the magnetic flux density vector. If the **S** - vector rotates so fast that **B** could be considered stationary, then the output voltage of a CVHD is given by

$$Vh \approx S \; B_{||} \cos(\omega t + \alpha) \quad (2)$$

where S denotes the magnitude of the magnetic sensitivity vector of the Hall device, $B_{||}$ - the in-chip-plane component of the magnetic flux density vector, ω – the angular velocity of the magnetic sensitivity vector of the CVHD, t – the time, and α – the instantaneous in-plain angle (azimuth) of the $B_{||}$ - vector with respect to a reference axis. Therefore, the phase shift of the CVHD output signal directly gives the angle α of the in-plane magnetic field. This means that a CVHD-based magnetic angle sensor does not need any additional angle-retrieving calculation or other procedure, which makes it very suitable for high-speed rotation angle sensing.

Another version of such magnetic angle sensor is based on two miniaturized 8-contact CVHDs (8CVHD) whose sensitivity vectors rotate in opposite directions, Figure 4 [18, 19]. The output voltages of the two 8CVHDs are separately processed in two channels and act as a reference one to another. Therefore there is no need for the reference signal as in [17]. The output of the sensor is a pulse-width modulated signal whose width is proportional to twice the angle enclosed between the in-plane magnetic field vector and the reference axis. The use of two devices doubles the sensitivity of the sensor, though at the expense of reduced angular measurement range. Logic circuit, driven by an on-chip clock controls the switches. The dimensions of the chip are about 2 x 2 mm.

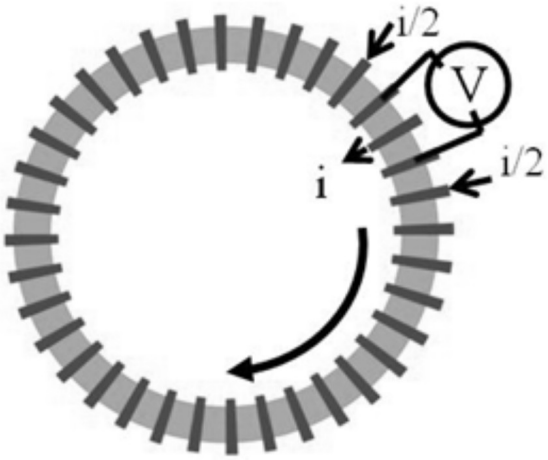

Figure 3: Principle of the circular vertical Hall device (CVHD). The ring represents a narrow n-well region, and the radial bars are the N+ contacts. An array of integrated CMOS switches (not shown) connects sequentially a set of 5 contacts, so that the 5-contact vertical Hall device virtually moves along the ring.

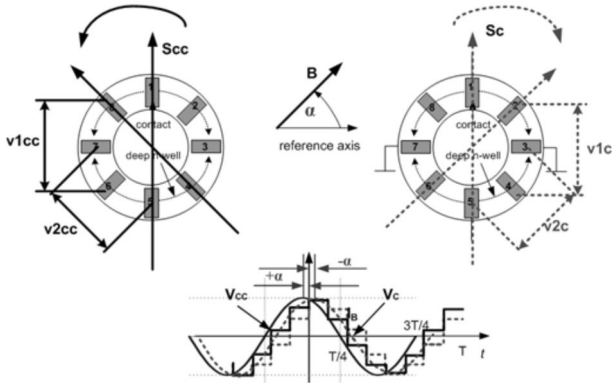

Figure 4: Biasing and sensing of the Hall voltages of the two 8CVHDs. Low-middle figure: clockwise (dashed line), counter clockwise (full line) and the band-pass fil-

tered signals for the DC magnetic field enclosing the angle α with the reference axis.

The angle sensors based on the vertical Hall technology are even more robust than those based on the IMC-Hall technology. A vertical Hall device responds to a strictly in-chip-plane component of a magnetic field with negligible non-linearity. In particular, in vertical Hall technology the problems of perming and magnetic saturation do not exist. On the other hand, integrated vertical Hall devices tend to have higher equivalent offset field and noise than the IMC-Hall devices. Therefore, in angle sensors based on the vertical Hall technology it is beneficial to apply stronger magnets.

5 Compass and other magnetic direction sensors

The magnitude of the magnetic field at the Earth's surface ranges from 25 to 65 micro-tesla. This had been long considered a too week field to be measured by integrated Hall magnetic sensors. Moreover, an electronic compass should measure all three components of the Earth's magnetic field, whereas a classical Hall plate is a single-axis magnetic sensor. But the advent of the IMC-Hall technology has changed the circumstances: an IMC provides a magnetic gain for the two in-chip-plane components of the measured magnetic field; and the combination IMC-Hall allows for sensing all three components of a magnetic field on a single chip: see Figure 2. Thanks to these facts, the IMC-Hall is currently the dominant technology used in electronic compass ICs, particularly in mobile telephones [9], [20].

An integrated three-axis magnetic sensor, a magnetic vector sensor, can be also realized by combining at least two vertical Hall devices, one horizontal Hall device, and signal conditioning electronics on a same chip [21]. The latest improvement in the magnetic resolution of the integrated vertical Hall devices [22] opens the way for the realization of the integrated magnetic vector sensors with nearly as high resolution as that of an IMC-Hall 3-axis magnetic senor, but without the shortcomings of the IMC (perming, saturation, cost).

A high resolution, high magnetic range, and low-cost magnetic vector sensor would be a key component of a 3D position and/or direction sensor [23].

6 The magnet and its position

The magnetic signal that is measured by any of the magnetic sensors described so far is provided by a moving magnet, which is a part of an angle or direction sensor system. The optimal shape of the magnet's field depends on the type of the employed magnetic sensor. Tolerances in the distribution and the angular dependence of the magnet's field with respect to the "normal" (assumed) values may deteriorate the performance of the magnetic angle sensor.

By way of example, consider a magnetic angle sensor with a magnetic field sensor that responds to the in-plane component of the magnetic field, such as that based on IMC-Hall or vertical Hall technology. Then the rotation angle of the in-chip-plane component of the magnet's field vector should be the same as the rotation angle of the shaft. This is the case if the magnetic field is homogeneous. Since real magnets are subject to manufacturing tolerances, it is often necessary to measure the homogeneity of its magnetic field over an area of interest. Figure 5 [24] shows the result of such a measurement.

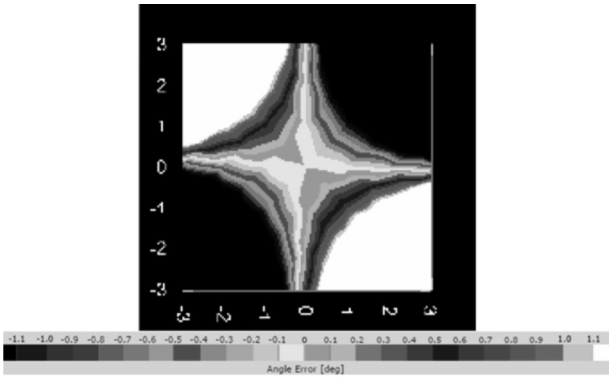

Figure 5: Measured distribution of the homogeneity error of a ferrite disc-shaped magnet, diameter 10mm. The measurement was performed by a precise 3D magnetic field mapper [25].

The quality of the magnet and the accuracy of the positioning of the magnet and the magnetic sensor IC may be the dominant factors that determine the accuracy of a magnetic angle sensor.

6 Signal conditioning

All integrated Hall magnetic sensors described above include biasing and signal conditional electronics. The signal conditioning includes amplification, reduction of offset, noise, and influence of temperature, analog to digital conversion, and retrieval of the angle of the magnetic field vector.

In contemporary integrated Hall magnetic sensors the crud offset is reduced by orthogonally coupling of 2 or more integrated Hall elements, and the residual offset

and 1/f noise are further reduced by the spinning current method [1].

The temperature dependence of the magnetic sensitivity per se is not a problem in most of the magnetic angle or direction sensors, since the retrieved angle depends on the ratio of two signals. However, the effective temperature coefficients of apparently equal devices may depend on their position on the chip. This comes about mostly because of the "co-operation" of the thermo-mechanical stress in the chip and the piezo-resistive, piezo-Hall, and piezo-junction effects. These effects are also the origin of offset and gain instability and miss-match of different signal processing channels. This problem can be alleviated by passing all sensor signals as much as possible through a same processing channel.

After A-D conversion of the Hall signals, the rotation angle can be retrieved in several ways, including the application of CORDIC algorithm (COrdinate Rotation DIgital Computer) [25], calculation of tangent and finding arc tangent from a look-up table, and by interpolation of the signals from an array of several Hall devices positioned around a circle.

In the CVHDs, the result of angle measurement appears as the phase shift between two ac signals, which can be measured by a phase detection circuit. Then the sensor output signal can be a pulse-width modulated signal, or a digital signal – the number of the clock periods within the pulse-width.

The accuracy of a magnetic angle sensor can be much improved by calibration. To this and, the sensor system should incorporate a temperature sensor, memory, and an adequate information processing. The calibration procedure might look like that used in an advanced 3-axis teslameter [27]. The efficiency of calibration is ultimately limited by noise and instability phenomena.

7 Conclusions

A magnetic angle sensor incorporates a magnet and a magnetic field sensor. The magnetic field sensor is usually an integrated sensor based on classical planar Hall devices, an integrated combination of Hall plates and magnetic flux concentrators (IMC-Hall), or vertical Hall devices.

The IMC-Hall technology provides magnetic gain and 3-axis magnetic sensing. The majority of compass chips in contemporary mobile telephones are based on the IMC-Hall. A magnetic angle sensor based on the IMC-Hall can work with smaller or more distant magnets. However, an IMC-Hall saturates at about 60mT; and at low magnetic fields, it suffers from perming and external disturbances.

In the sensors based on the vertical Hall technology the problems of perming and magnetic saturation do not exist; but the vertical Hall sensors have higher offset and noise than IMC-Hall sensors, and therefore require stronger magnets.

The magnetic angle sensor based on the circular vertical Hall device provides the measured angle very quickly; therefore they are very suitable for high-speed rotation angle sensing.

The dominant sources of errors in a magnetic angle sensor are related to the inhomogeneity of the magnet and the temperature drifts. Most of the errors can be corrected by calibration, but the ultimate limit of accuracy comes from noise and instability phenomena.

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Heterogeneous MPSoC Technology for Modern Cyber-physical Systems

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Abstract: Spectacular progress in microelectronics and information technology created a big stimulus towards development of advanced embedded and cyber-physical systems, but also introduced unusual silicon and system complexity and heterogeneity. Moreover, many modern cyber-physical applications demand guaranteed (ultra-)high performance and/or (ultra-)low energy consumption, as well as high dependability, safety and security. This all combined results in numerous serious system development challenges. To overcome these challenges a substantial system and design methodology adaptation is necessary. This paper focuses on the system technology for the modern highly-demanding cyber-physical systems. After brief introduction to modern cyber-physical systems and consideration of several serious challenges of their design, the paper discusses the heterogeneous MPSoC technology needed to implement those systems. This MPSoC technology exploits heterogeneous computation and communication resources involving application-specific instruction-set processors, hardware accelerators, distributed parallel memories and hierarchical communication structures.

Keywords: cyber-physical systems, MPSoC technology, design

Heterogena MPSoC tehnologija za moderne kibernetno-fizikalne sisteme

Izvleček: Izreden razvoj v mikroelektroniki in informatiki je ustvaril veliko vzpodbud v smeri razvoja naprednih vgrajenih in kibernetni-fizikalnih sistemih. Hkrati je vpeljal neobičajen silicij in kompleksnost in heterogenost sistemov. Nadalje, moderne kibernetno-fizikalne zagotavljajo (zelo) visoko učinkovitost in/ali (izredno) nizko porabo energije, kakor tudi visoko zanesljivost in varnost. Vse to se odraža v številnih resnih razvojnih izzivih. Za premagovanje teh izzivov je potrebna nadomestna metodologija sistema in načrtovanja. Članek se osredotoča na sistemsko tehnologijo modernih visoko zahtevnih kibernetno-fizikalnih sistemov. Po kratkem uvodu v moderne kibernetno-fizikalne sisteme in opisu izzivov pri načrtovanju, članek opisuje heterogeno MPSoC tehnologijo, ki je potrebna za implementacijo teh sistemov. MPSoC tehnologija izkorišča heterogen računski in komunikacijski vir z vključevanjem izbranih procesorjev, pospeševalnikov, distribuiranega vzporednega pomnilnika in hiearhične komunikacijske strukture.

Ključne besede: kibernetno-fizikalni sistemi, MOSoC tehnologija, načrtovanje

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1 Introduction

The recent nano-dimension semiconductor technology nodes enabled implementation of a very complex multi-processor system on a single chip (MPSoC) that may involve hundreds processors and realize much increased performance. This facilitated a further rapid progress in mobile and autonomous computing, global networking and wire-less communication which, combined with progress in sensor and actuator technologies, created new important opportunities. Many traditional applications can now be served much better, but what is more important, numerous new sorts of mobile and autonomous cyber-physical systems became technologically feasible and economically justified. Specifically, a big stimulus has been created towards development of high-performance embedded and cyber-physical systems. Various systems performing monitoring, control, diagnostics, communication, visualization or combination of these tasks, and representing (parts of) different mobile, remote or poorly accessible objects, installations, machines, vehicles or devices, or even being wearable or implantable in human or animal bodies can serve as examples. A new wave of information technology revolution arrived that started to create much more coherent and fit to use modern cyber-physical systems.

However, these new opportunities come with a price. On the one hand, unusual complexity has been introduced: *silicon complexity* (i.e. an extremely high number, diversity, small dimensions and huge density of devices and interconnects; huge length of interconnects, etc.), and *system complexity* (i.e. huge number of possible system states, large number and diversity of subsystems, extremely complex interactions and interrelations between the subsystems etc.). On the other hand, for numerous new highly-demanding embedded and cyber-physical applications in several fields (e.g. consumer, medical, well-being, communication, automotive, monitoring, control, etc.) the straight-forward software solutions are not satisfactory. Many of these applications require a guaranteed high performance and/or (ultra-)low energy consumption. Moreover, many of the new embedded and cyber-physical applications combine different kinds of signal and information processing involving algorithms with various characteristics. They are from their very nature complex, heterogeneous and highly-demanding. To adequately serve these applications, heterogeneous architectures have to be exploited. They require application-specific heterogeneous MPSoCs to perform their divergent real-time computations to extremely tight schedules, while satisfying their stringent energy, area and other requirements. Furthermore, due to the rapid evolution of many modern applications towards newer improved versions and due to the high and growing costs of application specific circuit realization in new technology nodes, adaptable hardware solutions are needed, as provided by (re-)configurable and programmable hardware. Finally, the gap between the nano-electronic technology capability and the system designers' productivity increases rapidly.

The combination of the high system and silicon complexity with the applications' stringent and partly contradictive requirements results in numerous serious system development challenges, such as: ability to satisfy the stringent requirements and ensuring high-quality of the complex systems, accounting in design for more aspects and changed relationships among aspects (e.g. increased influence of interconnects on major physical system characteristics, increased leakage power, etc.), adequately addressing the need of energy reduction, accounting for the dominating influence of interconnects and communication on major system characteristics, complex multi-objective system optimization, resolution of numerous complex design tradeoffs, reduction of the system development time and costs without compromising the system quality, etc.

To overcome these challenges sophisticated system and design technologies are needed. When considering the system and design methodology adaptation to the above briefly characterized situation in the field of the modern embedded and cyber-physical systems, we have first to ask: what general system approach and design approach seem to be adequate to address the listed problems and resolve the challenges? Predicting the current situation based on the commonly known Moore's law and own observations of rapid developments in embedded systems, more than 15 years ago I proposed such system paradigm and design paradigm that effectively address these challenges, namely, the paradigms of: *life-inspired systems* [1, 2, 3], and *quality-driven system design* [4 5, 6, 7], as well as, the *methodology of quality-driven model-based system design* based on them [6, 7, 8, 9]. From that time our research team, as well as, our industrial and academic collaborators are researching and applying this methodology to the multi-objective automatic architecture exploration and synthesis of MPSoCs for real-time embedded applications. The research confirmed the adequacy of this methodology.

This paper focuses on the modern highly-demanding embedded and cyber-physical systems, and heterogeneous MPSoC technology needed to implement those systems. The paper starts with introduction to cyber-physical systems. Subsequently, it briefly introduces the paradigm of life-inspired systems, and discusses the issues and challenges of the modern cyber-physical system design. Finally, the paper discusses the heterogeneous MPSoC technology needed to implement the highly-demanding embedded and cyber-physical systems. This MPSoC technology exploits heterogeneous computation and communication resources involving general purpose processors (GPPs), as well as, application-specific instruction-set processors (ASIPs), HW accelerators, distributed parallel memories and hierarchical communication structures, and it is a specific practical realization of the paradigm of life-inspired systems.

2 Modern cyber-physical systems

There is much ambiguity and misunderstanding in the research area of cyber-physical systems, and specifically, many various (sometimes strange or logically incorrect) definitions of a cyber-physical system were proposed in recent years. Therefore, this section starts with several definitions and explanations, with the aim to order the background and increase the understanding.

A **system** is a complex whole composed of interrelated, interdependent and interacting components (elements or larger parts of a system) that are so intimately

composed together that they appear and operate as a single unit in relation to the external world (to other systems).

Regarding to the increasing level of organization, all known systems can be sub-divided into the following three categories:
- *unorganized systems* – representing a mechanical unsystematic conglomerates of objects (e.g. a dune, being a conglomerate of sand grains);
- *organized systems* – being systematic and law-governed compositions of parts, which properties cannot be reduced to the properties of their parts, but involve some new emerging properties resulting from complex composition of the parts' properties (e.g. a molecule, crystal, circuit, computer); and
- *organic systems* - formed not as a composition of some pre-existing parts, but being an integral whole with distinguishable parts that originate and develop together with the whole (e.g. life organisms); two characteristic features of the organic systems that distinguish them from all other systems are the self-development and self-reproduction.

In this paper organized and life systems will be considered.

Cyber systems (information technology systems) are the information collecting, processing and communicating systems. They are actually (parts of) control systems of other cyber, physical, biological or social systems.

Cyber systems either:
- *collect information* using various sensors and other (distant) communication inputs, or
- *process the collected information* to compute some conclusions representing some control decisions or serving for preparation of such control decisions, or
- *communicate the results of information processing in time* using various memories or *in space* using different (distant) communication means and actuators, or
- *implement all these functions* realizing a *complete control system*, or
- *implement a sub-set of these functions* realizing e.g. a *monitoring* or *diagnostic system*.

For acquisition and communication of signals from physical and biological systems, the cyber systems use various sensors and (distant) communication means. For communication of control decisions to and actuation of controlled systems, the cyber systems use divergent (distant) communication means and actuators. Sometimes we even do not realize that particular systems or we personally are controlled or monitored by certain cyber systems. For instance, if we work in a feedback loop with a computer play: we controll the computer play, but the computer play also controls us. Similarly, when we watch TV, the TV system controls us to some degree.

Physical systems are systems in which matter or energy acquisition, processing and communication (transportation, transmission or storage) take place according to the lows of physics.

Life systems (biological organic systems, i.e. life organisms or organism populations) are compound systems performing matter and energy acquisition, processing and communication, as well as, information acquisition, processing and communication. They can be considered as natural cyber-physical systems (contrary to the engineered once).

An **embedded system** (unlike a stand-alone computer) is an inseparable part of a certain larger system (e.g. product or infrastructure). It serves a specific aim (e.g. monitoring, control etc.) in this larger system through (repeatedly) executing specific computation and communication processes required by its application. It is application-specific. It has to be especially designed or adopted to adequately serve the execution of these specific computation processes, and satisfy the application's requirements related to such attributes as functional behaviour, reaction speed or throughput, energy consumption, geometrical dimensions, price, reliability, safety, security, etc. Typically, embedded systems are (reactive) real-time systems, include sensing, interfacing, processing and/or actuating sub-systems, and involve in their implementation various mixtures of digital and analog hardware, and embedded software. In brief, embedded systems are cyber systems that are tightly coupled with (embedded in) the systems that they control, supervise, monitor or diagnose.

Pervasive computing (ubiquitous computing) is a paradigm of a seamless integration of information processing and communication into objects and environments. A **pervasive system** is in fact an "ideally" integrated embedded system.

As mentioned above, many various definitions of a cyber-physical system were proposed in recent years. Below, two cyber-physical system definitions will be introduced. The first one defines cyber-physical system in the broad sense, and the second one in the narrow sense of the "ideal" future cyber-physical system.

Cyber-physical systems (CPS) are compound systems engineered through close integration of cyber and physical sub-systems or components and/or pre-existing component cyber-physical systems, so that they appear and operate as a single unit in relation to the external world (to other systems). The sub-system integration involves both an appropriate spatial arrangement of the sub-systems, as well as, an adequate interconnection, communication and collaboration of the sub-systems.

Due to numerous reasons, of which discussion is out of the scope of this brief paper, much more effective and efficient infrastructure and products are required to be build in the future. In parallel to static system optimization at design time, highly effective and efficient dynamic control of the functional behaviour and resources consumption (e.g. energy consumption) of the future systems is essential to deliver these future much higher levels of system quality. Therefore, next generations of embedded systems are expected to be more intimately integrated and seamlessly orchestrated with the physical systems observed or controlled by them, and much more intelligent, autonomous, dynamic and adaptive to create higher synergy among the cyber and physical sub-systems, better combine the dynamics of the cyber and physical processes, and to result in highly effective, efficient and robust cyber-physical systems with coherent combined real-time behaviour of the collaborating cyber and physical sub-systems. They are expected to be smarter in the sense of a better use of more information and more precise information about various important features and laws of the part of the world observed by them, and in the sense of being more dynamic, predictive, adaptive and precise in controlling the physical part and of itself, to at the same time increase the effectiveness and efficiency. Additionally, more and more cyber-physical systems are becoming safety-critical. In addition to more systems in applications traditionally known as safety-critical (e.g. transportation, industrial and infrastructure automation, security control, medical and emergency management systems, etc.) many new applications become safety-critical [1, 3]. Such systems must be safe, secure and dependable, and have to guarantee adequate real-time operation. Therefore, the following more demanding narrower definition probably better reflects the character of the future advanced cyber-physical systems.

Cyber-physical systems (CPS) are smart compound systems engineered through seamless integration of cyber and physical sub-systems or components and/or pre-existing component cyber-physical systems, so that they appear and operate as a coherent single unit in relation to the external world (to other systems). The sub-system integration involves both an optimized spatial arrangement of the sub-systems, as well as, a seamless interconnection, and guaranteed real-time communication and collaboration of the sub-systems.

As cyber-physical systems may involve other cyber-physical systems as their sub-systems, the above definition also covers systems involving biological sub-systems, including human beings, or even social systems. Various medical CPS systems and a health-care system can serve here as a good example. For instance, an implanted pace-maker or another medical control/monitoring/diagnostic system forms a cyber-physical system together with the controlled/monitored/diagnosed (part-of) a human. It can be connected and can communicate with another CPS system being (a part of) a certain health-system (social system) forming together a higher-level CPS system.

The above example shows that cyber-physical systems can communicate and collaborate with other cyber systems and cyber-physical systems (including human beings). They can be very complex: together with some other CPS systems they can form cyber-physical (hierarchical) systems-of-systems. They can communicate using various multimodal machine-machine or human-machine interfaces, and private or shared communication media and channels, including internet and intranet communication networks, and heterogeneous short and long distance wireless communication. Cyber-physical systems connected through various combinations of heterogeneous interfaces and communication media to the global Internet are starting to form the so called Internet of Things (IoT). This way they can use globally available data and services (e.g. cloud data-bases and cloud computing services) for tasks impossible or difficult to perform when only using local resources.

The vision of "smart" systems collaborating on various scales, including the global scale, is not a science-fiction anymore, but is quickly becoming an actual reality. Examples of the new systems include various modern monitoring, diagnostic, control, multi-media and communication systems that can be put on or embedded in: mobile, remote, poorly accessible or dangerous objects, installations, devices, machines or vehicles; hospital, office, home or personal equipment; or even implanted in human or animal body. Embedded and cyber-physical systems already now play an extremely remarkable role in our life. Example application sectors of these systems include: *infrastructure* (e.g. smart homes, buildings, towns, etc.), *transportation* (e.g. smart transportation monitoring, communication and control systems, aerospace systems; traffic control and collision avoidance, assisted driving, autonomous com-

municating cars, etc.), *energy and information acquisition, storage and delivery* (e.g. smart power grids, data centres, etc.), *military* (smart monitoring equipment, tele-operation equipment, arms etc.), *environment* (e.g. smart environmental monitoring and control, rapid environmental intervention, environment exploration, etc.), *extension or replacement of human capabilities* (e.g. smart operation in remote, poorly accessible or dangerous environments (tele-robotics and robotic surgery, fire-fighting, search and rescue, military applications, sea and space exploration...), artificial limbs and implants, etc.), *personal assistance* (e.g. in well being, sport, monitoring, distant communication and control etc.), *social systems* (e.g. smart health-care, assisted leaving, etc.), etc. The term "modern cyber-physical systems" will be used by us to designate all kinds of "smart" infrastructure, things and objects, as briefly discussed above.

In the future, embedded and cyber-physical systems will be used even more and more commonly in virtually all fields of human activity, in various sorts of technical, social and biological systems, in more and more important and demanding applications. Our life is and will be to a higher and higher degree dependent on their adequate operation. Therefore, the individual and society expectations regarding their quality grow rapidly. Future research and development in cyber-physical systems will have to satisfy these growing expectations though enabling systems that will be much more effective, efficient, responsive, robust, safe and dependable than the today's systems. Current focus of the research and development in cyber-physical systems is mainly on:

- *holistic system quality assurance and heterogeneity in system design*, which treats cyber, physical, and biological (e.g. human) parts and sub-systems as integral components of a compound CPS system to create coherent highly optimized CPS, and addresses a. o. such aspects as intimate coupling, seamless orchestration, co-modelling, co-design, co-simulation and co-validation of the heterogeneous information-processing and physical subsystems; multi-objective multi-domain system optimization; effective and efficient dynamic, predictive and adaptive control of the system functional behaviour and resources consumption; and smart use of more information and more precise information for system control;
- *safety, security and dependability* of CPS;
- *generic high-performance, low-power, robust and acceptable-cost architectures, architecture templates and platforms* for complex collaborating CPS enabling guaranteed robust real-time performance and synchronization in complex networked CPS, low-energy consumption, predictability, adaptability, reusability, interoperability, scalability, composability, (semi-)automatic system integration, etc.;
- *miniaturized sensors and actuators* easy to integrate with cyber and physical system parts;
- *packaging technologies and smart materials* seamlessly integrating miniaturized sensors, actuators, processors, memories and their interconnections;
- *design methodology and design automation* of (platform-based) CPS;
- *systems-of-systems and Internet-of-Things*.

As the future much more effective and efficient "smart" cyber-physical systems will have important applications in virtually all economic and social segments, their potential economic and societal impact will be enormous. Consequently, major investments are being made worldwide both by private enterprises (from large multi-nationals, as e.g. Intel, Qualcomm, Google, etc., to small start-up SMEs) and by country governments to develop the CPS technology. As Europe has an approximately 30% share in the global market of embedded and CPS systems (being especially strong in the automotive, aerospace, medical, consumer and several other sectors) the development of CPS technology is of crucial importance for Europe.

A very important subclass of cyber-physical systems is this of **mobile and autonomous CPS** that can have inherent mobility or can be transported by other cyber-physical or biological systems, including humans and/or are autonomous regarding their functioning and energy sources. Some of these systems work fully independently, but most of them collaborate with other cyber or cyber-physical systems, when they require information or resources that are locally not available, or they deliver some information or services to the external systems. Examples of such systems include mobile robots, wireless sensor systems, mobile equipment transported by humans or animals, wearable systems, implantable systems etc. Perhaps the most popular and broadly known of these mobile and autonomous CPS is smartphone. Smartphone is actually a quite complex CPS, including: significant heterogeneous information processing resources (several different general purpose and application-specific processors with their local and global memories, and communication structures); several different long and short distance communication sub-systems (3G or 4G mobile cellular, WiFi, Bluetooth, etc.) to communicate with mobile cellular telecommunication network, Internet or other devices; and several sensors and actuators (touch screen, microphone, speaker, camera(s), light sensor, proximity sensor, GPS, etc.) that enable various cyber-physical applications.

Two essential characteristics of the mobile and autonomous CPS are:

- the requirement of ***(ultra-)low energy consumption***, often combined with the requirement of ***high performance***, and
- ***heterogeneity*** in the sense of ***convergence and combination of various earlier separated applications, systems and technologies*** of different sorts in one system, or even in a single chip or package.

In the first generation of the mobile and autonomous CPS: computing, communication and media were combined, resulting a. o. in smartphones and tablets and creating a huge market. The global smartphones market is expected to rapidly grow from $85.1 billion in 2010 to as much as $258.9 billion in 2015 (MarketsandMarkets), and the smartphone shipments forecast for years 2014-2018 is roughly 8 billion units (Gartner, Sept. 2013). The tablet shipments are expected to rise to 315 million units in 2014 (65% of the mobile PC market), and to 455 million by 2017 (75% of the global PC market) (NPD, Feb.2014). In years 2014-2018 the smartphone and tablet shipments are expected to exceed all other consumer system shipments in which modern processors are used, as PCs, TVs, cameras, video and audio systems, media players and adapters, game consoles, vehicles etc. (Gartner, Sept. 2013).

In the next generations of the new CPS systems more sensors/actuators and more divergent sensors/actuators will be integrated together with computing, communication and media, and the cyber sub-systems will be tighter coupled or even concurrently co-designed with the physical sub-systems to better support various modern cyber-physical applications. Early versions of such products, called "convergence products", are already in the market for some time, as e.g. iPhone-based ECG, smartphone-based USG or smartphone-based glucose monitor.

In the near future, a rapidly growing market will be this of smart wearable or implantable systems, for which miniaturized (multi-)sensors/actuators, ultra-low energy consumption, small size and appropriate form are of paramount importance. **Smart wearables** (often just referred to as wearables) are intelligent and often communicating (via Bluetooth) dresses, accessories and other wearable devices equipped with multiple sensors and/or actuators (e.g. screens; cameras; microphones; speakers; hart-rate, pressure, temperature, light, proximity and other sensors, GPS, etc.) that constitute a sub-class of the mobile and autonomous CPS. Examples of them are: light, sound or physically reactive dresses, smart heated clothes, connected T-shirt, monitoring T-shirt, Bluetooth jewellery, Apple Watch, personal locator watch, and other smart watches, activity tracker band, sun-exposure monitoring band, identity bracelet, smart glasses, vision-enhancement glasses, Google glass motorcycle helmet, jet fighter pilot helmets, hearing aids, wireless EEG headset, wireless ECG monitor, wireless glucose monitor, eButton (wearable health and activity monitoring system), etc. Many wearables are devoted to wireless health, personal assistance, well-being or sport applications, enabling (distant) in-action monitoring, treatment and/or communication. The application area of wearables is however much broader and includes many segments: from fashion and glamour, life-style computing and personal communication, through sport, well-being, medical and business, to safety, security and military. In 2015 wearable devices shipments are expected to exceed 90 million units and account for almost $20 billion revenue. This market is expected to further grow at almost 40% a year over the next six years, to surpass 340 million units and account for nearly $57 billion in revenue by the end of 2020 (SNS Research, August 2014). The rapidly growing market of more and more complex and sophisticated wearables will create a strong market pull for miniaturized sensors and actuators. Since the number of sensors in the future wearables will be higher than in the today's once (in 2019 an average wearable device will include 4.1 sensors compared to 1.4 sensors in 2013) the market of sensors for wearables will grow even faster than the wearables market. From 67 million units in 2013 it is expected to grow to about 85 million units in 2014, 175 million units in 2015, and 466 million units in 2019 (IHS Technology). So, an exponential growth of the miniaturized sensors is expected by factor seven in six years.

A related sub-class of the mobile and autonomous CPS, but with even more stringent ultra-low energy consumption requirements, is this of **smart miniaturized implants** (e.g. miniaturized pace-makers, neuro-stimulators, implantable defibrillators, ophthalmic implants, ear cochlear implants, drug-delivery pumps, etc.) and **pill-size medical devices** (e.g. endoscopic devices with sub-mm cameras). Finally, body area networks (BAN), representing somewhat more complex CPS involving several implanted or worn externally sensing, processing and communicating devices, can remotely monitor several vital bio-signals and communicate them wirelessly. It is predicted that over the period 2011-2016 the global market for microelectronic medical implants will grow at an 8.9% compound annual growth rate (CAGR), from $15.1 billion in 2011 to $23.1 billion in 2016. The fastest-growing segments will be: ear implants (18.2%), neuro-stimulators (10.5%) and implantable drug pumps (10.5%) (BCC Research, May 2011).

In parallel to the (ultra-)low energy and high-performance demands, for wearable and implantable systems very important issues are these of geometrical dimensions and form, as well as, integration of the miniaturized sensors and actuators with information processing and communication sub-systems on one chip or in one package.

CPS connected through various combinations of heterogeneous interfaces and communication media to the global Internet are forming the so called Internet of Things (IoT). Due to a large-scale and rapidly growing invention of new modern CPS systems, the Internet of Things started an explosive growth. In 2013 there were approximately 12.1 billion internet-connected devices, and their number is expected to more than quadruple to nearly 50 billion devices by 2025. While in 2013, more than 87% of the internet-connected devices were in communications, computers, and consumer electronics, this share is expected to decline to about 59% during the next 12 years, as the industrial market is expected to become the fastest growing market (specifically, its manufacturing, medical, automotive, military and aerospace sectors), followed by the consumer market (IHS Technology, Q1 2014).

The huge and rapidly developing markets of the modern CPS systems represent great opportunities both for private enterprises (from large multi-nationals, as e.g. Intel, Qualcomm, Google, etc., to small start-up SMEs) and country economies, including social systems.

Summing up, the spectacular advances in microelectronics and information technology created unusual new opportunities briefly discussed above. However, at the same time they introduced **unusual complexity**:

- ***Silicon Complexity***, in the sense of extremely high number, diversity, small dimensions and huge density of devices and interconnects, huge length of interconnects, increased number of serious issues and changed relationships among the issues; and
- ***System Complexity***, in the sense of a huge number of possible system states, large number and diversity of subsystems, and extremely complex interactions and interrelations between the subsystems.

Additionally, most of the modern "smart" CPS are highly demanding in the sense of requiring (ultra-)low energy consumption and guaranteed real-time high performance, as well as, high safety, security and dependability. The above discussed and some additional factors cause that the gap between the nano-electronic technology capability and the system designers' productivity increases rapidly.

This all results in serious system development challenges, such as:

- guaranteeing the real-time high performance, while at the same time satisfying the requirements of (ultra-)low energy consumption, and high safety, security and dependability;
- accounting in design for more aspects and changed relationships among aspects (e.g. leakage power, negligible in the past, is a very serious issue now; increased influence of interconnects on major physical system characteristics);
- complex multi-objective MPSoC optimization;
- adequate resolution of numerous complex design tradeoffs;
- reduction of the design productivity gap for the increasingly complex and sophisticated systems;
- reduction of the time-to market and development costs without compromising the system quality, etc.

These challenges cannot be overcome without a substantial system and design methodology adaptation.

Already more than 20 years ago I predicted the current situation and started research that aimed at answering the question: what system technology and design technology will be adequate to serve the development of the future complex and highly demanding embedded and cyber-physical systems?

When considering the system and design methodology adaptation to the situation in the field of the modern complex and highly-demanding systems, we have first to ask: what general system approach and design approach seem to be adequate to address the above mentioned problems and resolve the challenges?

More than 15 years ago I proposed such system paradigm and design paradigm, namely, the **paradigms** of: ***life-inspired systems*** [1, 2, 3], and ***quality-driven design*** [4, 5, 6, 7]. Based on them, I developed the **methodology of quality-driven model-based system design** [6, 7, 8, 9]. From that time my research team and our industrial and academic collaborators are researching and applying this methodology to the multi-objective (semi-)automatic architecture exploration and synthesis for real-time embedded MPSoCs [9-29], and this research confirms the adequacy of this methodology.

What are the life-inspired systems?

3 Life-inspired systems

The paradigm of life-inspired systems originated from my observation that:

- the complexity, operation domains and roles of the microelectronic-based systems
- more and more resemble
- the complexity, operation domains and roles of the (intelligent) life organisms or organized populations of such organisms.

Based on this parallel, I formulated the **hypothesis** that: ***the future microelectronic-based systems should have characteristics that resemble the characteristics of the (intelligent) life organisms or their populations***. Consequently, ***the basic concepts, principles, functional and structural organization etc. of the microelectronic-based systems should resemble these of the (intelligent) life organisms***. Similarly to a real brain, a life-inspired system should effectively and efficiently solve complex problems, take and implement difficult decisions, adapt to changing conditions, learn, etc., also in relation to itself.

To achieve these diverse aims effectively and efficiently in relation to complex applications and in the light of changing, noisy, or unreliable environment and own interior, a life-inspired system must be largely autonomous, self-contained, dynamic and robust, and it has to include adequate self-organization, adaptation and regulation mechanisms. Like a real organism or brain, a life-inspired system should be highly decentralized and composed of largely autonomous, diverse, having their own particular aims and optimized for these aims sub-systems (organs or centres). To form a coherent system the autonomous sub-systems have to be adequately (hierarchically) organized, interconnected with an appropriate network of effective and efficient communication channels, properly coordinated and adequately collaborating with each other, to synergistically achieve the global system aims.

To achieve a high performance and energy efficiency of the system processing and communication:
- information and intelligence, and in consequence computation, storage and communication resources, of the life-inspired system should be properly distributed over all its sub-systems;
- effective application-specific computing and storage should be implemented in the sub-systems, and efficient application-specific communication should be provided inside and between the sub-systems; and
- application parallelism should be extensively exploited, so that all kinds of application parallelism will be adequately supported both by hardware and software.

Realization of such life-inspired system, having the basic characteristics and organized according to the basic principles as sketched above, **requires**:
- autonomous heterogeneous sub-systems, implemented using multiple clock and/or power domains, and asynchronous or GALS techniques;
- local distributed application-specific memories for the sub-systems, enabling effective and efficient parallelism exploitation at the system and sub-system levels: multi-port, multi-bank and/or vector memories;
- (more) global (multi-port, multi-bank) memories for sharing data and for communication between the sub-systems;
- memory-centric processing for massive data - computations must come to data;
- adequate application-specific mixture of effective and efficient application-specific communication schemes and mechanisms of all kinds (i.e. NoCs, busses, switches, point to point communication, etc.);
- (massively) parallel application-specific processing sub-systems efficiently exploiting all kinds of application parallelism and involving in hardware implemented application-specific computation operators; and
- (re-)configurable hardware to realize the flexibility often required and implement the application-specific processing and communication schemes effectively and efficiently.

Specifically, **(re-)configuration** plays a very important role and serves numerous purposes:
- computation speedup and energy usage reduction in comparison to standard software solutions, due to computing platform specialization involving (massively) parallel application-specific processing, as well as, effective implementation of application-specific operations and (massively parallel) computation patterns directly in the (re-) configurable hardware;
- product differentiation and adaptability in relation to applications and standards;
- adaptability to changing operation conditions (e.g. adaptive control, filtering, interfacing, etc., but also self-diagnosis and fault-tolerance);
- design reuse and computational resource sharing;
- development and fabrication effort re-use that results in reducing the design productivity gap, reducing the design costs and shortening the time-to-market.

In particular, **generic system solutions**, and specifically, generic system platforms and architecture templates serve the above purposes, and additionally, enable an efficient (semi-)automatic system architecture synthesis. Through adequate instantiation and/or extension,

generic system platforms and architecture templates can be reused and adapted to (better) suit a particular application. The general form of a generic solution constrains the solution search space to such a degree that the construction of particular system solution instances for a particular application can efficiently be performed (semi-)automatically. The (semi-)automatic system construction can be performed through an appropriate instantiation and/or extension of the generic architecture platform or template, and computation process scheduling and mapping on the constructed this way instance of the platform or template. Observe, that the concept of *generic system solution* is strictly parallel to *genotype* in the life organisms: genotype is mutated to better fit to particular conditions, while generic solution is adequately instantiated to better serve a particular application. The *system (re-)configuration* is strictly parallel to the *adaptation* in life organisms.

Summing up: **the paradigm of life-inspired systems specifies**:

- basic principles, characteristics, as well as, functional and structural organization of embedded and CPS systems through analogy to the (intelligent) life organisms, and
- basic mechanisms and architectural solutions of systems that are necessary to implement the principles, characteristics and organization.

More information on the paradigm of life-inspired systems can be found in [1, 8].

The heterogeneous MPSoC technology needed to implement the highly-demanding embedded and cyber-physical systems, and based on configurable and extensible application-specific instruction-set processors (ASIPs) and HW accelerators is a specific practical realization of several architectural solutions and mechanisms proposed by the paradigm of life-inspired systems.

4 Issues and challenges of the modern cyber-physical system design

As explained in Section 2, many of the modern embedded and cyber-physical applications impose difficult to satisfy ultra-high demands. **Applications involving big instant data generated/consumed by video sensors/actuators and other multi-sensors/actuators *demand (ultra-)high performance in computing and communication***. Examples of such applications include: video sensing and monitoring, computer vision, augmented reality, ultra HDTV, image and multi-sensor processing (e.g. in some wireless-health or automotive applications), etc. (see Fig. 1). For instance, the 4G communication requires as high as 1Gbps throughput, while various HDTV standards require as high throughputs as 1 - 6 Gbps. **Applications providing continuous autonomous service in a long time *demand (ultra-)low energy consumption*** (e.g. continuous monitoring, communication or control in remote or poorly accessible places). For instance, various modern mobile communication, multimedia and medical applications require power consumption close to or below 1 W. Many of the modern applications require not only high computing power and low energy consumption, but high security, safety and reliability as well. For wearable and implantable systems, geometrical size and form play also a very important role. The remaining part of the paper focuses on explaining which kind of cyber technology is needed to implement the embedded and cyber-physical applications that impose demands of (ultra-)high performance and/or (ultra-) low energy consumption.

Figure 1: Demands of ultra-high performance and ultra-low energy consumption.

The modern very complex applications, that require very high throughput and ultra-low energy consumption, usually include numerous different algorithms involving various kinds of massive parallelism: data parallelism, and task-level, instruction-level and operation-level functional parallelism. They are from their very nature heterogeneous. To adequately serve these applications ***heterogeneous computation platforms*** have to be exploited. To adequately exploit the coarse task and data parallelism of applications, application-specific processing engines with ***parallel multi-processor macro-architectures*** have to be constructed. Multiple identical or different processors, each operating on a (partly) different data subset, have to work concurrently to realize the ultra-high throughput and/or ultra-low energy consumption. The different parts of the complex applications involving different kinds of information processing (e.g. different parallel processing structures) should be implemented using different application-part specific hardware architectures well supporting the different required kinds of process-

ing. However, the contemporary multi-core general purpose processors (GPP) are homogeneous. They involve several identical cores. Therefore, no contemporary standard general purpose processor (μP, μC, DSP, GPGPU) and no network of such processors is able to satisfy the ultra-high demands of applications that require the ultra-high throughput (e.g. in the range of several Gbps) or ultra-low power consumption (e.g. close to or below 1 W). Moreover, to realize the so high throughput they would require the clock-speed in the range of hundreds GHz and this would result in an extremely high (impossible to realize) power dissipation. To satisfy the (ultra-)high application demands, highly-optimized application-specific heterogeneous multi-processor systems-on-a-chip (MPSoCs) are required, often involving hardware multi-processors to execute the critical computations. The stringent requirements of the highly-demanding applications can only be addressed by highly effective and efficient application-specific heterogeneous HW/SW and HW solutions, such as application-specific heterogeneous MPSoCs based on adaptable (massively) parallel ASIPs and/or hardware processors (accelerators) (see Fig.2).

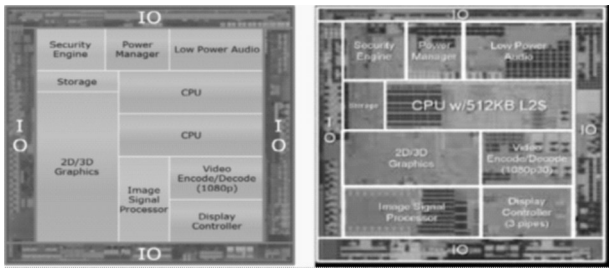

Figure 2: Intel ASIPs in heterogeneous MPSoCs at 32 nm (by courtesy of Intel Benelux)

Moreover, many of the highly-demanding applications involve complex algorithms with data parallelism and multi-input multi-output (MIMO) operations. To satisfy their stringent throughput and energy requirements ***data, operation and instruction parallelism, as well as, custom hardware implementation have to be exploited in the micro-architectures of processors*** for these applications. Thus, ***the application's parallelism has to be explored and exploited at two architecture levels in combination: macro-architecture and micro-architecture level***. Observe that similar performances can be achieved with fewer processors, each being more parallel and better targeted to a particular part of an application, as with more processors, each being less parallel or less application-specific. However, each of the alternatives can have different physical and economic characteristics, such as power consumption or circuit area. This results in the ***necessity to explore and decide various possible tradeoffs between the micro-architecture and macro-architecture design***. Moreover, each micro-/macro- architecture combination requires different compatible parallel memory and communication architectures. Exploitation of data parallelism in a computing unit micro-architecture usually demands getting the data in parallel for processing. This requires simultaneous access to parallel memories and simultaneous data transmission. Furthermore, in multi-processors for ultra-high-performance applications, parallelism has to be exploited on a massive scale [22-25]. However, due to the stringent energy consumption and area requirements, ***partially parallel architectures have usually to be used, which are much more complex to design than the fully parallel architectures*** exploiting the application's maximum available parallelism in a straightforward way.

5 Heterogeneous MPSoC technology for highly-demanding CPS applications

To satisfy the demands of modern highly-demanding embedded and CPS applications, highly-optimized application-specific heterogeneous multi-processor systems-on-a-chip (MPSoCs) are required. For the ultra-high throughput and/or ultra-low energy consumption massively parallel application-specific hardware multi-processors have to be used. For less stringent throughput and/or energy requirements programmable (massively) parallel application-specific multi-ASIP systems can be applied. In many cases, for complex applications involving parts of different character, the mixed ASIP and accelerator based systems can provide the best solution. In those application-specific heterogeneous MPSoCs, the application's parallelism has to be exploited at two architecture levels in combination: macro-architecture and micro-architecture level. The coarse task and data parallelism is exploited through constructing application-specific parallel multi-processor macro-architectures, while the fine grain data, operation and instruction parallelism is exploited through constructing the application-specific parallel micro-architectures of particular processors (see Fig. 4). Also various possible tradeoffs have to be resolved between the micro-architecture and macro-architecture designs, as well as, among the processor, memory and communication architectures. Below the low-density parity-check code [30] (LDPC) decoding will be used as an example application to further explain the application-specific heterogeneous MPSoC technology.

Example: ***heterogeneous massively parallel multi-processors for LDPC decoding***

The LDPC decoding is used as an advanced error-correcting scheme in the newest wired/wireless com-

munication standards, like IEEE 802.11n, 802.16e/m, 802.15.3c, 802.3an, etc. [31]. Some of these standards, for instance the IEEE 802.15.3c, specify as high as 5–6 Gbps throughputs [31]. The ultra-high performance demands in the Gbps range and other high demands of these applications cannot be satisfied by systems implemented using general purpose processors. For instance, an implementation of LDPC decoders on the famous Texas Instruments TMS320C64xx DSP processor running at 600 MHz delivers a throughput of only 5 Mbps [32]. Similarly, implementations of LDPC decoders on the general-purpose multi-cores result in throughputs of only 1–2 Mbps, and range from 40 Mbps on the GPUs to nearly 70 Mbps on the CELL Broadband Engine (CELL/B.E), as reported in [33]. For the realization of the so high throughput as several Gbps massively parallel application-specific hardware multi-processors are indispensable.

A systematic LDPC encoder encodes a message of k bits into a codeword of length n with k message bits followed by m parity checks. Each parity check is computed based on a sub-set of the message bits. To define an LDPC code, a parity check matrix (PCM) of size m×n is used. In Fig. 3 an example PCM for a (7,4) LDPC code is given. Each PCM can be represented by its corresponding task graph, referred to as Tanner graph. The Tanner graph corresponding to an (n,k) LDPC code consists of n variable nodes (VN) and m = n - k check nodes (CN), connected with each other through edges, as shown in Fig. 3. Each row in the parity check matrix represents a parity check equation c_i and each column represents a code bit v_j. An edge exists between a CN_i and VN_j, if the corresponding value $PCM_{i,j}$ is non-zero, what means that v_j is involved in the parity check equation c_i.

Usually, iterative Message Passing algorithms (MAP) are used for decoding of the LDPC codes [34]. The algorithm starts with the so-called intrinsic log-likelihood ratios (LLRs) of the received symbols based on the channel observations. During decoding specific messages are exchanged among the check nodes and variable nodes along the edges of the corresponding Tanner graph for a number of iterations. The variable and check node processors (VNP, CNP) corresponding to the VN and CN computations, iteratively update each other data, until all the parity checks are satisfied or the maximum number of iterations is reached. Since Tanner graphs of practical LDPC codes involve hundreds nodes and even more edges, the LDPC decoding represents a massive complex computation and communication task.

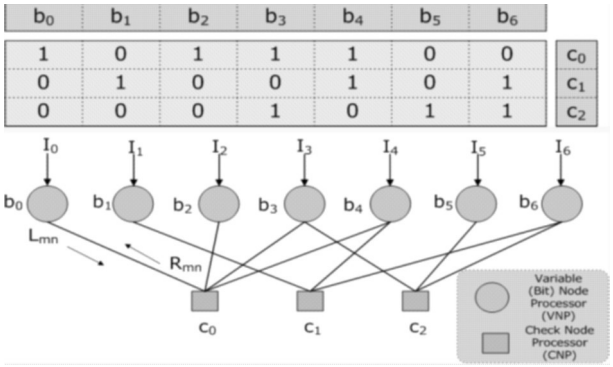

Figure 3: An example PCM for a (7, 4) LDPC code and its corresponding Tanner graph

Since each node receives several inputs and computes several outputs, the operations performed in nodes are multi-input multi-output (MIMO) operations. The micro-architecture level exploration is related here to the more or less parallel realization of various RTL-level MIMO operations. For example, the IEEE 802.15.3c standard specifies four different LDPC codes with variable nodes from a single input/output to maximally 4 inputs/outputs and the check nodes from minimally 5 inputs/outputs to as many as 32 inputs/outputs. The implementation spectrum of the corresponding micro-architectures spans from the fully-serial to the fully-parallel, with numerous partially-parallel micro-architectures in between. The fully-parallel implementation (resulting in a long critical path delay and large hardware) or fully-serial implementation (resulting in a high number of computation cycles) of MIMO operations may not be satisfactory for different stringent design constraints and objectives, which necessitates a careful exploration of partially-parallel architectures at the micro-architecture level (see Fig. 4). Due to the massive data parallelism at the macro-level and task-level functional parallelism, multiple such partially-parallel processors have to be considered at the macro-architecture level to satisfy the ultra-high throughput requirements (see Fig. 4). For example, the rate-1/2 672-bit IEEE 802.15.3c LDPC code consist of 672 variable nodes and 336 check nodes that correspond to maximally the same number of variable and check node processors, respectively, in the macro-architecture level design. Consequently, depending on the actual performance requirements, different massively-parallel multi-processors have to be build of the elementary processors to satisfy the requirements, with micro-architectures of the elementary processors spanning the full spectrum from serial, through partially-parallel, to fully parallel. This results in a very high number of possible macro-architecture/micro-architecture combinations, as well as, related compatible memory and communication structures, and task (node) and data mappings, defining a huge design space of various possible multi-processor

architectures with different characteristics (see Fig. 4). Therefore, construction of the optimal massively-parallel heterogeneous multi-processor architectures is a very difficult and time-consuming task. Fortunately, this task can be automated to a high degree [22, 25].

End of Example.

More information on architectures and designing of massively parallel application-specific hardware multi-processors for highly-demanding embedded and CPS applications, as well as, on distributed parallel memories and hierarchical communication structures can be found in our recent papers [22, 23].

However, in parallel to hardware (multi-)processors implementing the most demanding tasks, an application-specific heterogeneous MPSoC includes several different programmable processors to realize the design reuse and computational resource sharing, as well as, flexibility required for product differentiation, adaptability to changing applications and standards, and accommodation of the late design changes. In general, the heterogeneous MPSoC technology exploits heterogeneous (application-specific) computation and communication resources involving: general- purpose processors (GPPs), application-specific instruction-set processors (ASIPs), HW (multi-)processors, distributed parallel memories and hierarchical communication structures. Usually, the general-purpose processors of a heterogeneous MPSoC perform some low-performance control, synchronization and communication tasks, ASIPs perform the main high-performance tasks, and application-specific HW (multi-)processors the most critical ultra-high performance tasks. Although usually the ASIPs and HW processors occupy only a few times larger area on an MPSoC than the GPPs (see Fig. 2), due to the effective and efficient implementation of the application parallelism with their application-specific parallel hardware they can deliver more than hundred times higher processing power than the GPPs.

In the recently finished research project ASAM [27] (http://www.asam-project.org/) of the European Industrial Research Program in Embedded Systems ARTEMIS, we developed automated architecture synthesis and application mapping technology for heterogeneous MPSoCs based on adaptable ASIPs customizable to a particular application through instantiation and extension. Only a few companies in the world possess such a heterogeneous MPSoCs technology based on adaptable ASIPs: one of them is Intel Benelux - one of the main industrial partners of ASAM.

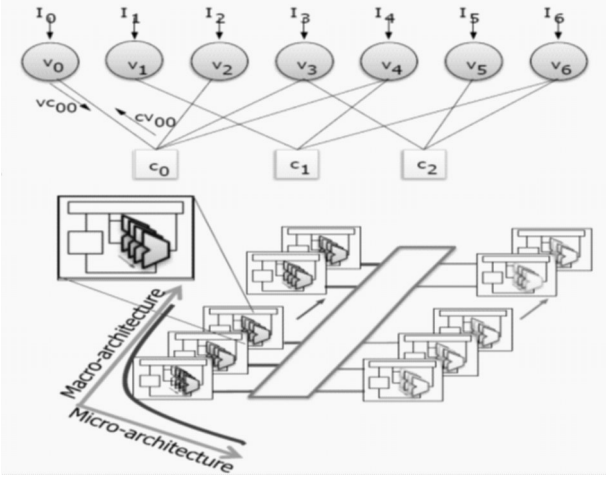

Figure 4: Massively-parallel multi-processors with parallel processor micro-architectures

The architecture platform targeted in the ASAM project was the heterogeneous multi-ASIP MPSoC platform of Intel Benelux (previously Silicon Hive), which can be instantiated and extended for specific applications. Each ASIP of the platform is a VLIW processor capable of executing parallel software with a single thread of control. The generic ASIP architecture of the targeted MPSoC platform is graphically represented in Fig. 5. It includes a processor core (core) performing the actual data processing, and core I/O (coreio) implementing the local memories and I/O subsystem enabling the communication of the ASIP with the rest of the system. The ASIP core includes a VLIW datapath controlled by a sequencer that uses status and control registers, and executes programs from the local program memory. The datapath contains scalar and/or vector function units organized in several parallel issue slots. The issue slots are connected via programmable input and output interconnections to registers organized in several register files. The function units perform computations on intermediate data stored in the register files. Both SIMD and MIMD processing can be realized. The coreio, implementing the local memories and I/O subsystem, enables an easy integration of the ASIP in any larger system. Any other processors or devices of the MPSoC can access the devices in coreio via master and slave interfaces.

Numerous divergent application-specific ASIP instances can be created through configuration and extension of the generic ASIP architecture. The parameters to be explored and set to create an ASIP instance include: the number and type of issue slots and (scalar or vector) instructions inside the issue slots, the number and type of issue slot clusters to optimize parallelism exploitation and communication between the issue slots, the number and size of register files, the type, data width, and

size of local memories, the architecture and the parameters of the local communication structure, the scheduling and mapping of the application part assigned to the ASIP onto the ASIP parallel issue slots and their data onto the local memories; etc. In particular, ASIPs can be constructed that contain both the scalar issue slots and vector issue slots with different vector lengths, as well as, different scalar and vector memories.

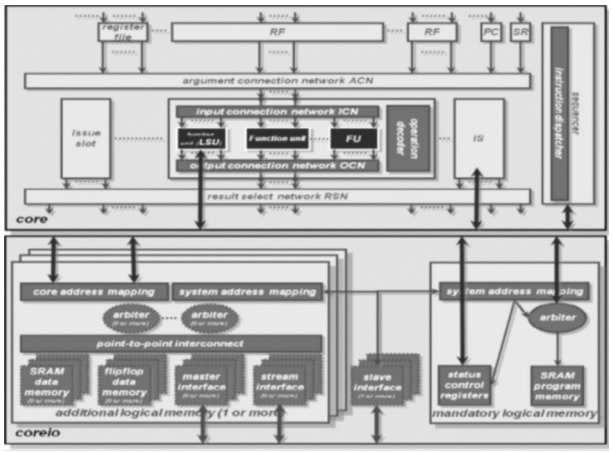

Figure 5: Generic VLIW ASIP architecture (by courtesy of Intel Benelux)

Several different ASIPs, each customized for a particular part of a complex application, can be interconnected via direct buffered connections, busses or a Network-on-Chip (NoC) including shared memories and DMAs to form and MPSoC (see Fig. 2). The parameters to be explored and set at the MPSoC system-level include: the number and types of ASIPs; the number, type and size of shared memories; the scheduling and mapping of the application parts onto the ASIPs and their data onto the memories; and the architecture and parameters of the global communication structure.

The potential of the ASIP-based MPSoC can be illustrated as follows. Several ASIPs with approximately 100 issue slots in total, each for 64-way vector processing, can be placed on a single chip implemented in the currently exploited 22 nm CMOS technology. When operated at only 400–600 MHz, these ASIPs can deliver more than 1 Tops/s, with power consumption far below the upper limit of mobile devices. Such ASIP-based heterogeneous MPSoC platforms enable efficient exploitation of various kinds of parallelism: the multiple ASIPs enable the coarse-grain data and task parallelism exploitation, while the ASIP's parallel issue slots and vector instructions enable the fine-grain data, instruction and operation parallelism exploitation. This adaptable ASIP-based MPSoC technology addresses several fundamental challenges for the development of the highly-demanding embedded and CPS applications:

- it is able to deliver high performance, high flexibility and low energy consumption at the same time;
- it is relevant for a very broad range of application domains;
- it is applicable to several implementation technologies, e.g.: semi-custom SOC or ASIC, structured ASIC, and FPGA.

Provided that an effective and efficient highly automated customization technology will become available, it will become possible to build adaptable ASIP-based MPSoCs at substantially lower costs and with shorter time to market than for the hardwired ASICs or processors build from scratch. This was the primary target of the ASAM project.

With the state of the art in the design technology before the ASAM project:
- the architecture, software, and hardware of the customizable ASIP-based systems had to be designed by experts supported by only some point tools;
- these experts have to possess deep knowledge of the application analysis and restructuring, target technology, ASIP and multi-ASIP system architecture design, as well as, software mapping and compilation processes;
- even for an expert the application analysis and construction of a high-quality software structure and corresponding hardware platform for a complex application constitute a very complex, time-consuming and error-prone task;
- the difficulty and complexity of this task dramatically reduced the abilities of a high-quality systematic exploration of the system, hardware and software design spaces and resulted in a low productivity and/or decreased design quality.

In the ASAM project we developed an effective automated design technology that efficiently performs the HW/SW MPSoC architecture exploration and synthesis both at the ASIP and system level, and implemented the prototype EDA tools of this technology. More information on the architecture of heterogeneous ASIP-based MPSoCs and automated HW/SW co-design technology for the MPSoCs can be found in our recently published papers [17-20][26-29] and on the ASAM project website: http://www.asam-project.org/ .

By comparing information on the application-specific heterogeneous MPSoC technology presented in this section with information on the paradigm of life-inspired systems presented in Section 3, one can easily conclude that the heterogeneous MPSoC technology is a specific practical realization of several architectural

solutions and mechanisms proposed by the paradigm of life-inspired systems.

6 Conclusion

Spectacular advances in microelectronics and information technology created unusual opportunities, and particularly, big stimulus towards development of various kinds of high-performance embedded and cyber-physical systems. However, they also introduced unusual complexity and heterogeneity. Moreover, many modern embedded and cyber-physical applications are not only complex and heterogeneous, but highly-demanding as well. This all combined results in numerous serious system development challenges briefly discussed in this paper.

To overcome these challenges a substantial system and design methodology adaptation was necessary. This included development of the paradigms of life-inspired systems and quality-driven design, as well as, of new system and design technologies implementing them. The new system and design technologies replaced several concepts by the required new once, as e.g.: sequential computing by highly parallel computing, homogeneous architectures by heterogeneous architectures, simple flat architectures by complex hierarchical architectures, separate HW and SW design by actual coherent HW/SW co-design, separate processing, memory and communication design by their co-design, separate macro- and micro-architecture design by their co-design, simple optimization by complex multi-objective optimization and trade-off exploration, etc. In our former projects and in the recently finalized ASAM project we performed a substantial pioneer R&D work towards an adequate system and design technology for the modern highly-demanding embedded and cyber-physical systems. Nevertheless, much R&D work is still needed in this revolutionary developing area being of primary importance for individuals, societies, industries and countries.

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Measurement of NBTI Degradation in p-channel Power VDMOSFETs

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Abstract: In this paper we report on the use of a cost-effective stress and measurement setup for investigations of NBTI in commercial p-channel power VDMOS transistors IRF9520. The effects of stress voltage and temperature under both static and pulsed bias stress conditions are briefly discussed, and dynamic recovery effects are evaluated by varying the duty cycle and frequency of the pulsed stress voltage applied. Less significant degradation of threshold voltage found after pulsed bias stressing is ascribed to the dynamic recovery, and its tendency to further decrease with lowering the duty cycle and/or increasing the frequency of the pulsed voltage used for stressing is explained in terms of the enhanced dynamic recovery effects.

Keywords: Measurement, NBTI, VDMOSFET, Threshold voltage

Meritev NBTI degradacije v p-kanalu močnostnega VDMOSFETa

Izvleček: Članek opisuje stroškovno učinkovito uporabo merilne in testne opreme za preučevanje NBTI v komercialnih p-kanalnih VDMOS IRF9520 tranzistorjih. Opisani so vplivi bremenske napetosti in temperature na statične in pulzne razmere. Obravnavani so dinamični efekti okrevanja s spreminjanjem delovnega cikla in frekvence pri pulzni bremenski napetosti. Ugotovljena je bila manj pomembna degradacija pragovne napetosti pri pulznem vzbujanju je vzrok dinamičnega okrevanja. V okviru dinamičnega okrevanja je razložen je trend nadaljnje degradacije pri manjšem delovne ciklu i/ali višji frekvenci pulznega signala.

Ključne besede: Meritve, NBTI, VDMOSFET, pragovna napetost

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1 Introduction

Negative bias temperature instability (NBTI) has been found to occur mostly in p-channel MOSFETs operated at elevated temperatures (100 – 250 °C) under negative gate oxide fields in the range 2 – 6 MV/cm [1–8]. NBTI is manifested as the decrease in device transconductance (g_m) and absolute drain current (I_{Dsat}) and the increase in device threshold voltage (V_T) and absolute "off" current (I_{off}) [3]. The phenomenon had been known for many years, but has only recently been recognized as serious reliability issue in state-of-the-art MOS integrated circuits with ultra-thin gate oxide devices. Several factors associated with device scaling have contributed to bringing NBTI to the attention of device and circuit designers: first, operating voltages have not been reduced as rapidly as gate oxide thickness, resulting in higher fields and increased chip temperatures, which both enhance NBTI; second, threshold voltage scaling has not kept pace with operating voltage, which has resulted in larger percentage degradation of drain current for the same ΔV_T; and third, the addition of nitrogen into the thinned gate oxides for leakage reduction has had the side effect of increasing NBTI [2].

Regarding device electrical parameters, NBT stress-induced threshold voltage shifts are most critical and can put serious limit to a lifetime of p-channel devices with gate oxide thinner than 3.5 nm [5]. Several models of microscopic mechanisms responsible for the observed V_T shifts have been proposed [1–8], but these are beyond the scope of this paper and will not be discussed. However, it is important to offer a brief answers to a couple of basic questions that could arise so far, such as: (*i*) Why the NBTI is of greater concern in p-channel devices compared to n-channel ones? (*ii*) Why the negative bias causes more considerable degradation than positive bias? The bias temperature stress-induced V_T shifts are generally known to be the consequence

of underlying buildup of interface traps and oxide-trapped charge due to stress-initiated electrochemical processes involving oxide and interface defects, holes and/or electrons, and variety of species associated with presence of hydrogen as the most common impurity in MOS devices. An interface trap is a trivalent silicon atom with an unsaturated (unpaired) valence electron at the SiO_2/Si interface. Unsaturated Si atoms are additionally found in SiO_2 itself, along with other oxide defects, the most important being the oxygen vacancies. Both oxygen vacancies and unsaturated Si atoms in the oxide are concentrated mostly near the interface and they both act as the trapping centres responsible for buildup of oxide-trapped charge. Interface traps readily exchange charge (electrons or holes) with the substrate and they introduce either positive or negative net charge at interface, which depends on gate bias: the net charge in interface traps is negative in n-channel devices, which are normally biased with positive gate voltage, but is positive in p-channel devices as they require negative gate bias to be turned on. On the other hand, the charge found trapped in the centers in the oxide is generally positive in both n- and p- channel MOS transistors and cannot be quickly removed by altering the gate bias polarity [9]. Therefore, absolute values of V_T shifts due to stress-induced oxide-trapped charge and interface traps in n- and p-channel MOS transistors, respectively, can be expressed as [9–11]:

$$\Delta V_{Tn} = \frac{q\Delta N_{otn}}{C_{ox}} - \frac{q\Delta N_{itn}}{C_{ox}} \quad (1)$$

$$\Delta V_{Tp} = \frac{q\Delta N_{otp}}{C_{ox}} + \frac{q\Delta N_{itp}}{C_{ox}} \quad (2)$$

where q denotes elementary charge, C_{ox} is gate oxide capacitance per unit area, while ΔN_{ot} and ΔN_{it} are area densities of oxide-trapped charge and interface traps, respectively. Similar amounts of oxide-trapped charge and interface traps are generated in both n- and p-channel devices [2], but above consideration clearly shows that the net effect on threshold voltage, ΔV_T, must be greater for p-channel devices, because in this case the positive oxide charge and positive interface charge are additive. As for the question (*ii*), it seems well established that holes are necessary for BTI degradation [1–8], which provides a straight answer since only negative gate bias can provide holes at the SiO_2/Si interface. This is also an additional reason why the greatest impact of NBTI occurs in p-channel transistors since only those devices experience a uniform negative gate bias condition during typical CMOS circuit operation.

In spite of continuous tendency in nanometre scale technologies to have the gate oxide thinned down, the interest in ultra-thick oxides has remained owing to widespread use of MOS technologies for realisation of power devices. Vertical double-diffused MOSFET (VD-MOSFET) is an attractive power device for application in high-frequency switching power supplies owing to its superior switching characteristics, which enable operation in a megahertz frequency range [12, 13]. High-frequency operation allows the use of small passive components (transformers, coils, capacitors) and thus enables the reduction of overall weight and volume, making the power VDMOSFETs especially suited for application in power supply units for communication satellites. Also, power VDMOSFETs are widely used as the fast switching devices in home appliances and automotive, industrial and military electronics [14]. Degradation of power MOS devices under various stresses (irradiation, high field, temperature, and even hot carrier injection) has been subject of extensive research (see, for example, [15] and references listed therein), but only few research groups seem to have addressed the NBTI in these devices [14, 16–26]. However, increased electric fields and elevated chip temperatures are frequently approached during the routine operation of power devices in automotive and industrial applications [14], so the investigations of NBTI in power MOSFETs are of importance as well.

Several new measurement techniques have recently been developed in order to get better insight into the microscopic mechanisms of NBTI [27–31]. In this paper we will describe a measurement technique that is particularly suitable for NBTI measurements on power VDMOS transistors. Few experimental results for both static and pulsed NBT stress conditions of investigated devices will be discussed as well.

2 Stress and measurement setup

Threshold voltage shift in the NBTI tests is determined by using various measurement techniques [27–31], including the one based on current–voltage (*I–V*) characteristics. The stress voltage, either static (dc) or dynamic (ac) [32], is removed from the device to perform the measurement, and the threshold voltage is determined from the measured *I–V* characteristic. In order to minimize the dynamic recovery effects on threshold voltage value, the measurement must be completed as fast as possible. Once the measurement has been done, the stress voltage is switched back to the device. Recent developments in measurement technology have made possible fast and on-the-fly (when the stress is even not being interrupted) NBTI techniques with the measurement times reduced down to 1 μs [33–39] or even lower [28]. Measurements are spot, utilizing one or a few points on the transfer *I–V* characteristic [34], so a compromise between accuracy and speed is achieved.

This is fully applicable to thin gate oxide transistors in CMOS technology, where the stress voltage magnitudes are comparable to the operating gate voltage of the device. However, stress voltages required for NBTI investigations in VDMOS transistors, whose gate oxides are much thicker than those in CMOS devices, are several times larger than their typical operating voltage, so separate circuits for providing the stress voltage and performing the NBTI measurements are needed. The tests should be realized by switching back and forth between the circuits.

This paper is focused on the application of the recently developed measurement technique, which is based on cost-effective switching circuit and is suitable for NBTI measurements on VDMOS transistors [25]. Devices used in this study were commercial p-channel power VDMOSFETs IRF9520 with current/voltage ratings of 6.8 A/100 V, encapsulated in TO-220 plastic cases [40]. The devices were built in standard Si-gate technology with gate oxide thickness of 100 nm, and had the initial threshold voltage, V_{T0}, about −3.6 V. As already mentioned, owing to the thick gate oxide, accelerated NBT stressing of these devices requires negative gate voltage amplitudes even over 40 V, which exceed capabilities of commonly used signal voltage sources [41, 42]. Therefore, an external amplifier or a booster is required between the source unit providing the stress voltage and the device under test (DUT), as illustrated by a block diagram shown in Fig. 1. Full scheme and detailed explanation of the system developed for NBT stress and measurements on power VDMOSFETs are given in [25], and here we only provide short description. Reed relays S1 and S2 are used as switches to separate the high-voltage stress circuit from the low-voltage measurement circuit. In the stress mode, source and drain of DUT are tied to ground, whereas gate stress voltage is obtained by boosting a signal from Tektronix AFG3102 function generator to a required magnitude. The booster circuit is based on power VDMOS transistor in a simple switching configuration, which enables to perform either dc stress (function generator output is kept at 0 V) or ac stress (function generator output is used to provide pulses). The booster circuit includes the appropriate drain and gate resistors, which are required to maintain acceptable shape of the switching waveform [43] and prevent possible parasitic oscillations. In the measurement mode, two source-measure units from Agilent 4156C precision semiconductor parameter analyzer are used: one solely to provide sweeping gate voltage to the DUT and the

second one to provide constant drain voltage and to measure drain current of DUT. As already mentioned, switching between stress and measurement circuits is accomplished by using reed relays S1 and S2, but one more relay (not shown in Fig. 1) is additionally used to switch the drain voltage sense circuit of 4156C analyzer, so the voltage drop on the external leads is properly compensated.

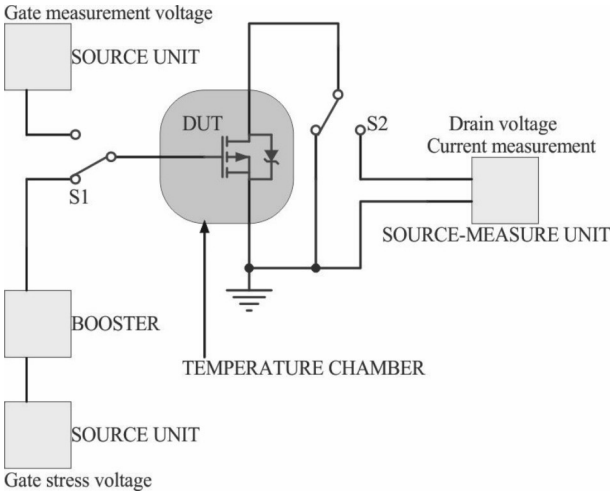

Figure 1: Block diagram of NBT stress and measurement setup for p-channel power VDMOSFETs [25].

All instruments shown in Fig. 1, and the temperature inside the chamber as well, are computer controlled over the IEEE-488 (GPIB) bus. Multithreading PC application software is developed using .NET technology to allow the NBTI test specification and control through the graphical user interface. Timeline for interim measurements is loaded from the external file. Within the graphical interface, which is shown in Fig. 2, user is allowed to specify gate stress voltage amplitude, frequency and duty cycle, stress type (dc, ac, or combined), measurement condition (linear or saturation), drain voltage, and nested timeline for multiple interim measurements after stress. If a combined stress is used, an arbitrary point on the loaded timeline may be chosen for changing the stress type. Measurements at room temperature before and after the test are also performed automatically. Results for each measurement are saved in a separate file during the test and merged upon the test completion. The overall time required to complete an interim measurement, which includes switching from the stress to measurement circuit, measurement of the full *I–V* characteristic while sweeping the gate voltage from −2 to −4.75 V with 50 mV steps, and switching back to the stress circuit, is found to be about 235 ms and cannot be further reduced due to the speed limitations of the reed relays and instrumentation used [25].

3 Results and discussion

The system has been verified by series of NBTI tests on several devices. As an example, Fig. 3 shows measured transfer *I–V* characteristics for one device subjected to

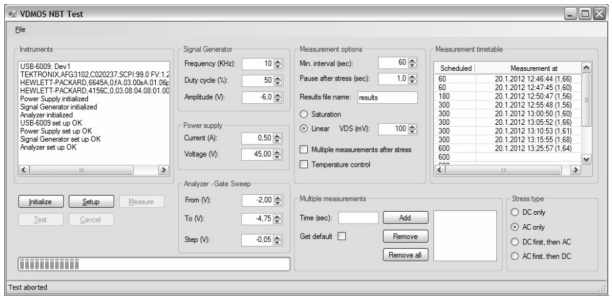

Figure 2: Graphical user interface of the software application for NBT stress and measurement.

12 hours of the pulsed bias stress followed by 24 hours of static stress under the specified conditions. During the 36 h test, the total of 48 interim measurements were performed according to the predefined timeline, but for simplicity, only the initial (before stress) and final (after stress) characteristics at room (27 °C) and stress (175 °C) temperatures are shown. As can be seen, the characteristics are shifted along the gate voltage axis toward the higher voltage values, while their slope slightly decreases, which all points to generation of oxide trapped charge and interface traps induced by NBT stress. The overall NBT stress-induced degradation is considered to include hole trapping in the oxide and creation of interface and oxide traps through the reactions involving hydrogen species and their subsequent diffusion away from the interface (reaction–diffusion component) [44]. The holes trapped near the interface are quickly released once the NBT stress is ceased, and thus make the 'fast' component of degradation, whereas the reaction–diffusion component, whose recovery depends on hydrogen back-diffusion, is the 'slow' component and may even be partially non-recoverable. It should be noted, however, that the time constants associated with hole trapping–detrapping increase about exponentially with distance from the interface [44], and in the case of ultra-thick oxides typical for VDMOS devices may span over many decades in time, which means that hole trapping in this case may contribute to both slow and fast degradation components. Moreover, some recent studies have strongly suggested that the hole trapping could give major contribution to the degradation in thin gate oxides as well [8, 45], and these findings have led to the development of the new charge-trapping models, which link the NBTI degradation with the creation of switching oxide traps and are more consistent with the post-stress recovery data showing dispersion over a wide range of time [45].

Due to the limitations in measurement speed of 4156C [27, 30, 35, 36], the fast component of NBT stress-induced degradation cannot be captured by the proposed setup. However, the setup was optimized to start the measurement immediately (within the instrument's limits) after completing the stress, and it was shown that an approximate evaluation of the dynamic recovery effects in power VDMOS devices still might be possible [25]. Actually, the setup may be of help to alleviate the dynamic recovery effect in NBTI characterization as it seems to offer measurements short enough to capture the faster part of the slow degradation component, which should be sufficient for rather reliable prediction of device lifetime considering the finding that even a 60 s long delay in measurements does not cause significant overestimation of NBTI lifetime [46]. In addition, this method provides the full range *I–V* characteristics that can be used to determine not only threshold voltage but also to extract and/or calculate some other important device parameters, such as transconductance and channel carrier mobility, which may provide better insight into the effects of NBTI.

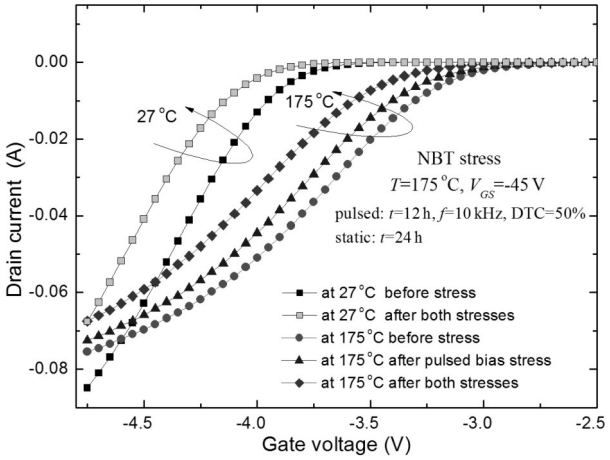

Figure 3: Measured transfer *I–V* characteristics before and after the NBTI test.

Herewith we will present and discuss in more details the results of the experiment in which the two sets of p-channel power VDMOS devices were stressed for 36 hours under the static and pulsed NBT stress conditions, respectively. For the static NBT stress, negative dc voltages in the range 35 – 45 V were applied to the gate, whereas the drain and source terminals were grounded. For the pulsed stress, negative gate voltage pulses (with frequency f = 10 kHz and duty cycle DTC = 50%) of the same magnitudes were used instead. Stressing under both static and pulsed conditions was performed at temperatures ranging from 125 to 175 °C. Threshold voltage values were calculated from the measured *I–V* characteristics by the second derivative method [47].

Two characteristic sets of data (for different stress voltages at 175 °C and for different temperatures at the stress voltage of –45 V) for the stress-induced threshold voltage shifts during the static and pulsed NBT stressing of IRF9520 p-channel VDMOSFETs are shown in Fig. 4. As can be seen, NBT stressing under both static and pulsed bias conditions was found to cause signifi-

cant threshold voltage shifts, which were more pronounced at higher voltages and/or temperatures. The threshold voltage shifts caused by pulsed NBT stress appeared with rather significant delay (30-60 minutes after the start of stressing), which was found to depend on stress temperature and pulse magnitude. In addition, the pulsed voltage stressing caused generally lower shifts as compared to static stressing performed at the same temperature with equal stress voltage magnitude.

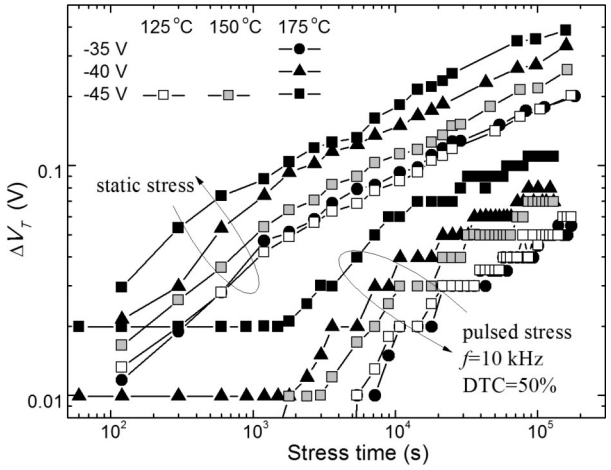

Figure 4: Threshold voltage shifts in p-channel VD-MOSFETs during the static and pulsed (f = 10 kHz, DTC = 50%) NBT stressing.

The reason for the observed delay and lower shifts in the case of the pulsed NBT stress can be explained by two factors associated with the nature of pulsed stressing itself. The first factor is assessed by taking into account that "stress time" in Fig. 4 refers to the total time, which includes fractions of the periods corresponding to both "high" and "low" levels of the pulsed gate voltage applied. However, the devices are stressed only during the fraction of period corresponding to the "high" voltage level (on-time), so the actual or net stress time is significantly shorter (and the resulting stress-induced threshold voltage shifts appear both slower and lower) in the cases of pulsed stress than in the case of static one. The other factor could be a partial recovery of threshold voltage during the period fractions corresponding to the "low" level of the pulsed stress voltage (off-time), which also contributes to the smaller shifts observed in the cases of pulsed bias stress. The partially recovered degradation is restored again on arrival of each new stress voltage pulse, so the phenomenon is referred to as dynamic recovery [48].

To evaluate dynamic recovery effects during the pulsed bias stressing it is necessary to alleviate the first factor mentioned above, which could be done by plotting the threshold voltage shift versus the net stress time rather than the total time. The results of stressing with three different duty cycle pulses (75%, 50%, and 25%) at 10 kHz and those of static stress are shown in Fig. 5, where the net stress time in the cases of pulsed stressing was calculated by multiplying the total stress time with corresponding duty cycle value for each specific case. The overall net stress time was 6 h in all cases, and all devices were stressed with the same gate voltage magnitude (–45 V) at 175 °C. As can be seen, the NBT stress-induced threshold voltage shifts are most significant in the case of the static stress and clearly decrease with lowering the duty cycle in the cases of the pulsed bias stress. This is clear indication that dynamic recovery effects become more pronounced with lowering the duty cycle of the gate voltage applied. However, it should be noted that frequency remains constant, so variations in duty cycle change the ratio between the pulse and no-pulse fractions of the period: the lower duty cycle actually means shorter pulses and longer breaks in between the pulses, which further means shorter stress time and longer recovery time during each period of pulsed stress voltage applied. Accordingly, there is less time to create degradation during a single period and more time for recovery, so the overall resulting degradation found after stressing for equal net stress times tends to decrease with lowering the duty cycle. Therefore, it can be speculated that overall degradation tends to decrease with duty cycle lowering because of two combined effects: one is creation of lesser degradation because the pulses are getting shorter, and the other is enhanced dynamic recovery because the period fractions between the two pulses are getting longer.

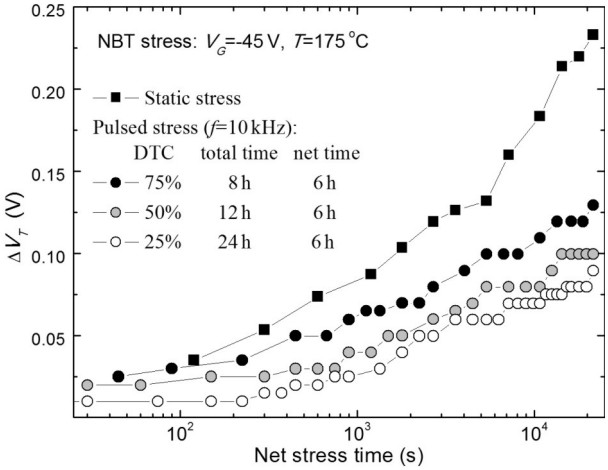

Figure 5: Threshold voltage shifts in p-channel VD-MOSFETs vs. net stress time at various duty cycles (NBT stress: V_G = –45 V, T = 175 °C, f = 10 kHz).

Threshold voltage shifts observed in devices stressed with three different frequency pulses (1, 10 and 100 kHz) in comparison with those obtained by static

stress are shown in Fig. 6. All devices were stressed with the same gate voltage magnitude (–45 V) at 175 °C, and the overall net stress time was 6 h in all cases again. A duty cycle was kept at 50% for the pulsed stressing at all frequencies, so the net stress time in these cases was equal to a half of the total stress time. Again, the stress-induced threshold voltage shifts are most significant in the case of the static stress, and it is interesting to note that they clearly decrease with increasing the frequency in the cases of the pulsed bias stress. So, the dynamic recovery effects seem to become more pronounced with increasing the frequency of the gate voltage applied even though the change of frequency at constant duty cycle practically does not affect the ratio between the pulse and no-pulse fractions of the period at all. However, the increase in frequency means that the pulses and fraction of period between the pulses become both shorter, which further means that there is less time to create degradation and less time for recovery during each period of the pulsed voltage applied. Accordingly, one may expect the resulting degradation would be nearly independent of frequency, as reported in [49, 50], but in our case degradation apparently decreases with increasing the frequency, as reported more recently in [32] (advanced measurement techniques mentioned in previous section have become available rather recently, which might be a reason for inconsistency of the data reported here and in [32] with those found in less recent publications [49, 50]).

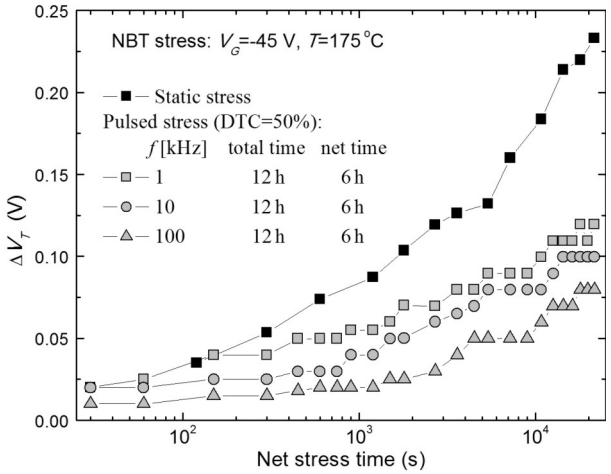

Figure 6: Threshold voltage shifts in p-channel VD-MOSFETs vs. net stress time at various frequencies (NBT stress: V_G=–45 V, T=175°C, DTC=50%).

A possible explanation for why the degradation decreases with increasing the frequency could be as follows. The pulses at low frequencies are long enough to allow for creation of rather significant amount of the slow and/or non-recoverable component of degradation, which is hardly removed in the fraction of period between the pulses. The amount of this component decreases at higher frequencies, while that of the fast component increases, and the latter is more easily removed even though the fraction of period between the pulses becomes shorter. As a result, the dynamic recovery effects become more pronounced and overall degradation tends to decrease with increasing the frequency.

4 Conclusions

A cost-effective stress and measurement setup was used to investigate dynamic recovery effects during the NBTI tests in commercial p-channel VDMOS transistors IRF9520. The effects of NBT stress voltage and temperature under both static and pulsed stress bias conditions were discussed, and dynamic recovery effects were evaluated by varying the duty cycle and frequency of the pulsed stress voltage applied. The stress induced threshold voltage shifts under both static and pulsed bias conditions were found to be larger at higher temperatures and/or stress voltage magnitudes. Less significant degradation of threshold voltage was observed under the pulsed stress bias conditions because of the dynamic recovery. The tendency of overall degradation to decrease with lowering the duty cycle and/or increasing the frequency of the pulsed voltage used for stressing was explained in terms of enhanced dynamic recovery effects.

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Harmonic modeling of full-wave diode rectifier for nonuniform load currents

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Abstract: This paper proposes an equivalent circuit model and formulation for presentation of characteristic harmonic components generated by full wave diode rectifiers for nonuniform load currents. In conventional equivalent circuits, only the uniform current harmonics on AC side of converters are considered. For an exact and general analysis, the proposed model involves both nonuniform current harmonics on AC side and voltage harmonics on DC side of the rectifiers. The obtained expressions are valid for a general load state without simplifying. The proposed model converts the full-wave diode rectifier into a linear circuit with regards to harmonics. The model depends on Fourier series expansion for the load voltage and the source current waveforms. Simulation results and exprerimental results validate the proposed model and the given expressions

Keywords: Equivent circuit, harmonic model, nonuniform load current, rectifier.

Harmonično modeliranje polnovalnega diodnega usmernika za nekonstantne bremenske tokove

Izvleček: Članek predlaga model ekvivalentnega vezja za predstavitev karakterističnih harmonskih komponent, ki jih proizvaja polnovalni diodni usmernik za nekonstantne bremenske tokove. V običajnih ekvivalentnih vezjih so običajno upoštevani le konstantni tokovi na AC strani. Predlagan model, za natančno analizo, vključuje tako nekonstantne tokovne harmonike na AC strani kakor tudi napetostne harmonike na DC strani usmernika. Tako dobljeni izrazi veljajo za splošno breme brez poenostavitev. Predlagan model pretvori polnovalen diodni usmernik v linearno vezje z upoštevanjem harmonikov. Temelji na razvoju Fourierove vrste za bremensko napetost in valovnem vhodnem toku. Simulacijski rezultati in poizkusi potrjujejo predlagan model.

Ključne besede: Nadomestno vezje, harmonski model, nekoonstanten tok, diode

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1 Introduction

The purpose of harmonic studies is to quantify the distortion in voltage and/or current waveforms at various locations in a system. The need for a harmonic study may be indicated by excessive measured distortion in existing systems or by installation of harmonic producing equipment. One important step in harmonic studies is to characterize and to model harmonic-generating sources.

In general, major harmonic sources can be categorized as (1) Devices that generate harmonics during their switching processes. The most commonly seen are power electronic devices, (2) Devices that generate harmonics due to their nonlinear voltage-current characteristics [1-3] such as transformers, reactors, ac arc furnaces; (3) Hybrid devices that include both types of aforementioned devices such as DC arc furnaces and fluorescent lamps with electronic ballasts [4-5]; and (4) Devices such as rotating machines that harmonics are generated because of nonsinusoidal flux distribution in the stator and the harmonic interaction between the stator and field windings [6].

The AC/DC converters are one of the most important harmonic sources in electrical systems. Accurate harmonic analysis of AC/DC converters has got more attention in the last decades. Many harmonic models have been proposed for representing power electronic devices [7-10]. The most common model is in the form of a harmonic current source, which is specified by its magnitude and phase spectrum. Three basic approaches used to build detailed models include developing analytical formulae for the Fourier series as a function of terminal voltage and operating parameters for the harmonic source, developing analytical models for harmonic source operation and solving for its current waveform by a suitable iterative method, and solving for harmonic source steady-state current waveform with time-domain simulation. A more practical approach for the harmonic analysis of an electrical system containing many converters is to use time domain simulation [11]. The interaction between the AC and DC side harmonics in a converter system must be correctly represented.

A time domain sampled-data model method for the computation of the ac current and dc voltage harmonic generated by a capacitor filtered three-phase uncontrolled rectifier is presented in [12]. The approach employs numerical iteration to determine the diode's turn-on and turn-off times and thereby determine the circuit's steady state solution. In [13], harmonic currents of three phase bridge uncontrolled rectifier are analyzed in both continuous domain and discrete domain. Moreover, the further analysis on boundary condition for harmonic current is put forward and generalized. Modeling and simulation of 6-pulse and 12-pulse rectifiers with impacts to input current harmonics are given in [14]-[15]. The paper [16] develops a systematic state-space approach to the modeling of boost type ac–dc converters and reduction of output ripples. The bridge rectifier voltage is modeled as a periodic disturbance whose harmonics have given frequencies but uncertain phases and magnitudes.

A possible alternative to time domain simulation is frequency domain methods [17-19]. Noncharacteristic line current harmonics of AC/DC converters with high dc ripple are investigated by assumption of negligible small commutation in [20]. By means of frequency domain analysis, analytical models are derived based on the first terms of the series expansion of the switching function. A MATLAB-based method to calculate the harmonic amplitudes of rectifier's DC-side output current is given in [21].

In primary investigations of harmonics relating to converters, the current on DC side of the converter systems was assumed uniform that resulted rectangular current in AC side of the converter. In this approach, the order and magnitude of harmonics could be calculated simply. Although considering more details about converter structure and possible practical conditions causes complexity in harmonic analysis, it results in real and accurate converter harmonics spectrum. Therefore, different methods are required to analyze current converter accurately. Using transfer functions or switching function, solving state equations of system, converter models in frequency domain, and solving time domain equations of the converter numerically are samples of these investigations [18, 22-23]. For general and accurate analysis, nonuniform structures of currents on DC and AC sides of converter systems must be considered.

In this study, the exact electrical equivalent circuit and expressions of AC/DC converters with respect to harmonics are introduced. Although the AC/DC converters are switching circuits, the method converts the switching circuit into a linear circuit with regards to harmonics. The paper is organized as follows. First, the conventional equivalent circuits of the rectifiers are pointed out, then a new equivalent circuit with respect to harmonic currents on the AC side and output voltage harmonics on DC side of the rectifiers is proposed. The model and expressions are developed for non-constant valued/nonuniform load currents.

2 Conventional equivalent circuit of full-wave rectifiers

Converters or rectifiers using semiconductor switching devices generate harmonics caused by the behavior of switching. The circuit configuration of a full-wave diode rectifier, of which the equivalent circuit will be described in detail, is shown in Fig.1. The diodes are assumed to be ideal.

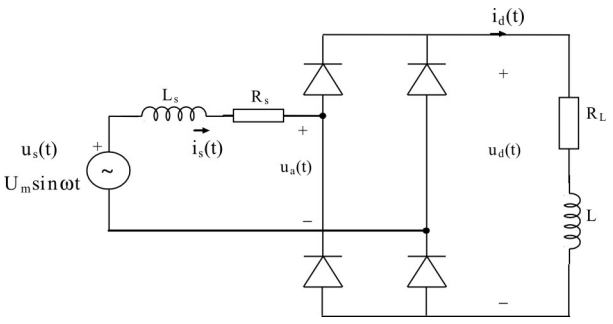


Figure 1: Configuration of a full wave diode rectifier

In a full wave diode rectifier, the output voltage, $u_d(t)$, is not dependent on the load in case that the equivalent serial resistance and inductance of the source are zero. The source current, $i_s(t)$ has a bidirectional form of the

load current, $i_d(t)$. In conventional equivalent circuits, the amplitude of harmonic currents generated by a diode rectifier is considered to be constant by using a smoothing reactor on the DC side. For the condition of constant/uniform load current, in conventional equivalent circuits, the rectifier has been widely considered as an ideal current source for harmonics as follows

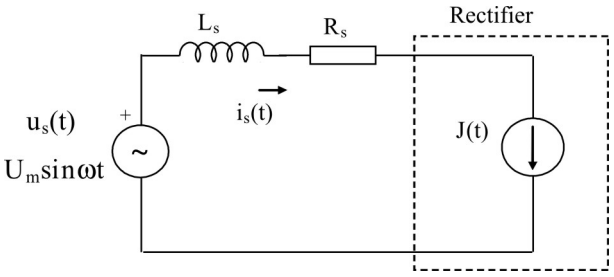
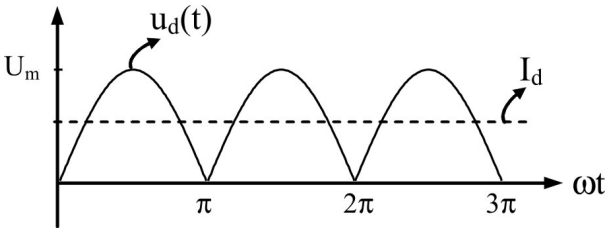
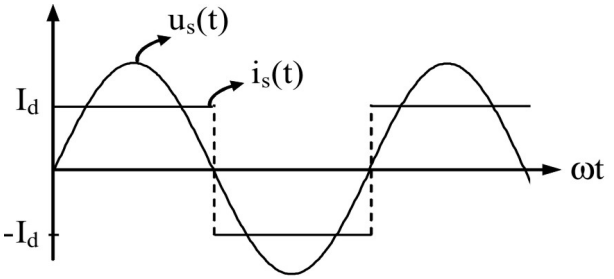


Figure 2: Conventional equivalent circuit to $i_s(t)$ on AC side

With regard to this condition, the load voltage/current and the source voltage/current of Fig.1 are available in many textbooks [24] and also given in Fig.3.



(a) Load voltage and current



(b) Source voltage and current

Figure 3: Waveforms relating to conventional situation

In Fig.1 and Fig.2, the resistor R_s and inductor L_s represent the source internal impedance. Relating to a uniform load current, the average values of the load voltage and load current in Fig. 3 are given as follows.

$$U_d = \frac{2U_m}{\pi} \quad (1.a)$$

$$I_d = \frac{U_d}{R_L} \quad (1.b)$$

3 Proposed equivalent circuit and formulation for nonuniform load currents

In conventional equivalent circuits of rectifiers, for constant valued/uniform load currents, current harmonics on AC side are considered. Whereas, in general situation, load and source currents are not always uniform as shown in Fig.4, in steady state. Moreover, in rectifier circuits, there are both current harmonics on AC side and voltage harmonics on DC side. For an exact and general analysis, it is necessary to deal with both harmonics not having uniform structure. For this purpose, a new equivalent circuit model containing both nonuniform current harmonics and voltage harmonics is proposed. The model depends on Fourier series expansion for the load voltage and the source current waveforms.

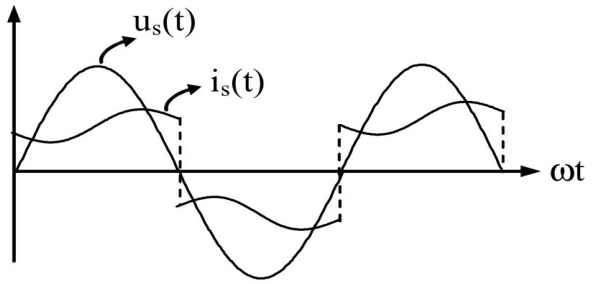


Figure 4: Waveforms relating to nonuniform current situation

First, Let's consider the output voltage harmonics in DC side of the rectifier circuit in Fig.1. In the rectifier circuits, an AC source is processed through a set of switches to create a well-defined waveform. We can represent the combined action of an actual source (AC source) and a set of switches by an equivalent source. The equivalent source provides a very strong advantage: The new circuits are linear, and avoid the nonlinearity and complication of switches. We can use superposition, Laplace transforms, or other techniques from linear network analysis to analyze rectifiers. Based on superposition, a term-by-term for the Fourier series of the current and voltage in the rectifier circuits can be solved. Equivalent voltage source, $u_d(t)$, applied to the load in Fig.1, is presented in Fig.5.

The equivalent voltage source, $u_d(t)$, contains both the fundamental component and harmonic components of the load voltage. The waveform of equivalent source, thereby the output voltage of the rectifier circuit, is given in Fig.3.a. The Fourier series for the voltage $u_d(t)$ can be expressed in trigonometric form as

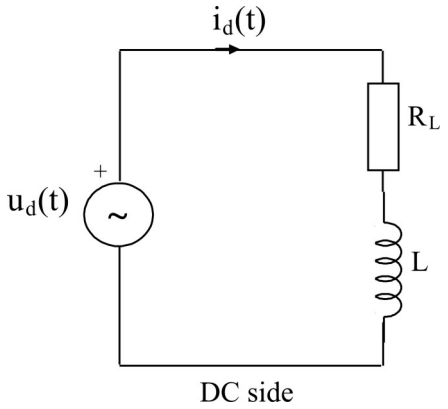


Figure 5: Equivalent voltage source, $u_d(t)$, applied to the load

$$u_d(t) = \frac{2U_m}{\pi} - \sum_{n=2,4,6...}^{\infty} \frac{2U_m}{\pi}\left(\frac{2}{n^2-1}\right)\cos(n\omega t) \qquad (2)$$

Every component of Fourier series corresponds to a voltage source. They are symbolized as U_d, $u_{d2}(t)$, $u_{d4}(t)$, in Fig.6, where U_d is average load voltage as DC source, $u_{d2}(t)$ is a AC source having ω_2 frequency, $u_{d4}(t)$ is a AC source having ω_4 frequency,

Second, Let's deal with the current harmonics on AC side of the rectifier circuit in Fig.1. For this purpose, first, the load current on DC side must be defined. For general situation, the nonuniform load current, $i_d(t)$, is expressed by Fourier series as follows,

$$i_d(t) = \frac{2U_m}{\pi}\left\{\frac{1}{R_L} - \sum_{n=2,4,6...}^{\infty}\left(\frac{2}{n^2-1}\right)\left(\frac{1}{\sqrt{R_L{}^2 + (n\omega L)^2}}\right)\cos(n\omega t - \varphi_n)\right\} \qquad (3)$$

where, $\varphi_n = \tan^{-1}\dfrac{n\omega L}{R_L}$

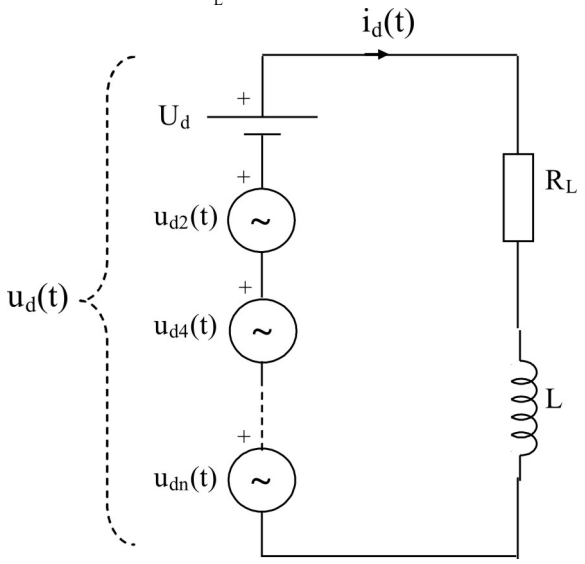


Figure 6: Equivalent voltage sources corresponding to Fourier series

Equation (3) is equal to (1.b) in case that the load current is uniform, inductance L is large enough. Equation (3) relating to the nonuniform load current, $i_d(t)$, can be partitioned as follows

$$i_d(t) = I_d + i_{df}(t) + i_{dh}(t) \qquad (4)$$

Where, I_d is the DC component (average current), i_{df} and i_{dh} represent the fundamental (first) component, the harmonic components of the load current, respectively. Since $i_d(t)$ has even harmonics, $i_{df}(t)$ is equal to 0.

The source current on AC side, $i_s(t)$, is dependent on the load current, $i_d(t)$. Although the current on DC side of the converter is a rectified, accordingly unidirectional current, the current on AC side of the converter is bidirectional as shown in Fig.4. In other words, the source current has a bidirectional form of load current. In order to express the nonuniform source current, first, the DC component of load current, I_d, is converted into bidirectional form as shown in Fig.3b. This rectangular current, $i_{sa}(t)$ is expressed by Fourier series as follows,

$$i_{sa}(t) = \sum_{n=1,3,5,...}^{\infty} \frac{4}{n\pi} I_d \sin(n\omega t) \qquad (5.a)$$

$$i_{sa}(t) = i_{saf}(t) + i_{sah}(t) \qquad (5.b)$$

In (5.a), the current I_d is equal to (1.b). i_{saf} and i_{sah} represent the fundamental component, the harmonic components of current $i_{sa}(t)$, respectively. In order to express the nonuniform source current, second, the harmonic components of load current, $i_{dh}(t)$, are separated from (3).

$$i_{dh}(t) = \frac{2U_m}{\pi} \sum_{n=2,4,6...}^{\infty}\left(\frac{2}{n^2-1}\right)\left(\frac{-1}{\sqrt{R_L{}^2 + (n\omega L)^2}}\right)\cos(n\omega t - \varphi_n) \qquad (6)$$

The exact expression of nonuniform source current, $i_s(t)$ is given in (7). Where, $k = \pm 1$. The load current has a rectified form of source current. The positive portion of $i_s(t)$ is the same as $i_d(t)$ and $k = 1$. On the other hand, although the negative portion of $i_s(t)$ is the inverse of $i_d(t)$, k is taken as –1.

$$i_s(t) = i_{sa}(t) + k \cdot i_{dh}(t)$$

$$i_s(t) = \sum_{n=1,3,5,...}^{\infty} \frac{8U_m}{n\pi^2 R_L}\sin(n\omega t) + k \cdot \frac{2U_m}{\pi} \sum_{n=2,4,6...}^{\infty}\left(\frac{2}{n^2-1}\right)\left(\frac{-1}{\sqrt{R_L{}^2 + (n\omega L)^2}}\right)\cos(n\omega t - \varphi_n) \qquad (7)$$

As seen from (7), the nonuniform source current contains both odd and even harmonics. Now, Let's deal

with the input voltage of converter, $u_a(t)$, in Fig.(1). Since this voltage is dependent on the source current, $i_s(t)$, thereby the load current, it is modeled by a current controlled voltage source, which is controlled with the source current, in Fig.7. Since the load/source current is not uniform, the harmonic voltage source has a nonuniform wave form.

$$u_a(t) = u_s(t) - R_s i_s(t) - L_s \frac{di_s(t)}{dt}$$

$$u_a(t) = u_s(t) - \sum_{n=1,3,5,\ldots}^{\infty} \frac{8U_m}{n\pi^2 R_L} \sqrt{R_s^{\,2} + \frac{L_s^{\,2}}{n^2\omega^2}} \sin(n\omega t + \varphi_a) +$$

$$k \cdot \frac{2U_m}{\pi} \sum_{n=2,4,6\ldots}^{\infty} \left(\frac{2}{n^2 - 1} \right) \left(\frac{1}{\sqrt{R_L^{\,2} + (n\omega L)^2}} \right) \tag{8}$$

$$\sqrt{R_s^{\,2} + \frac{L_s^{\,2}}{n^2\omega^2}} \sin(n\omega t - \varphi_n - \varphi_a)$$

Now, to derive the circuit relating to nonuniform structure containing harmonic currents on AC side and harmonic voltages on DC side of rectifiers, we discuss an equivalent circuit in Fig.8. This model, primarily, is a combination of Fig.5 and Fig.7.

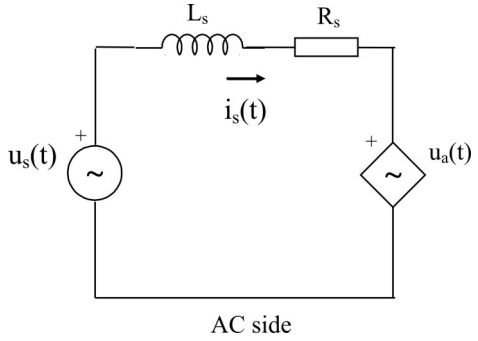


Figure 7: Representation of dependent harmonic voltage source

Since the equivalent circuit shown in Fig.8 contains both AC side and DC side of the rectifier circuit, it meets the need for exact analysis of the rectifier circuit. Owing to this approach, the switching circuit is converted into a linear circuit with regards to harmonics. Thus, any circuit analysis technique can be used to analyze the rectifier circuit.

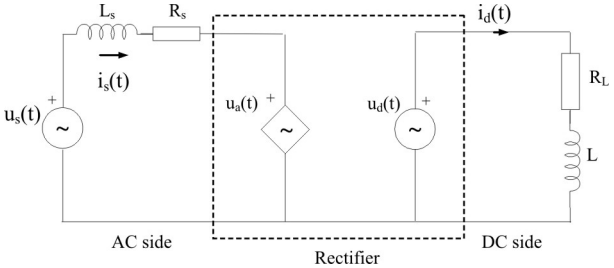


Figure 8: Exact harmonic model of rectifier circuit

From the point of harmonic studies, the equivalent circuit can be divided into two subcircuits: one is an equivalent circuit to the fundamental component and the other is an equivalent circuit to harmonics.

First, the equivalent circuit to the fundamental components on both AC side and DC side of the rectifier is discussed. In this case, the first harmonic components of dependent voltage source, $u_a(t)$, and voltage source $u_d(t)$ in the model are considered: $u_{a1}(t)$, $u_{d1}(t)$. The source voltage, $u_s(t)$ remains unchanged. According to (2), Since $u_d(t)$ has even harmonics, $u_{d1}(t)$ is equal to 0. The equivalent circuit to the fundamental components is obtained as in Fig.9.

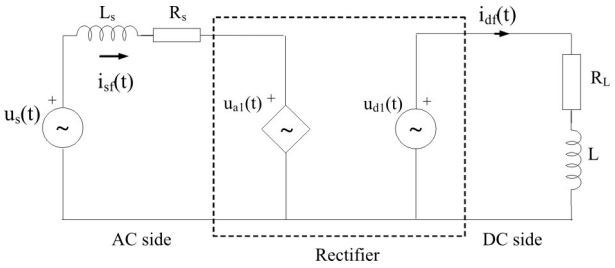


Figure 9: Equivalent circuit to fundamental components

Next, the equivalent circuit to harmonic components on both AC side and DC side of the rectifier is discussed. This equivalent circuit can be obtained under the condition that the source voltage $u_s(t)=0$ and the first component of harmonic voltage source $u_{a1}(t)=0$ in Fig.8. The equivalent circuit to harmonics is shown in Fig.10. $u_{ah}(t)$ and $u_{dh}(t)$ represent the sources relating to harmonic components. By this linear circuit, it can be obtained the desired harmonic components of rectifier as seen in Section IV.

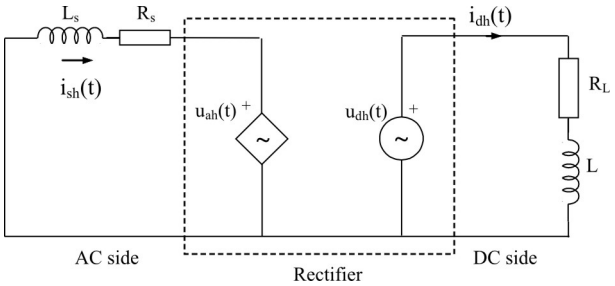


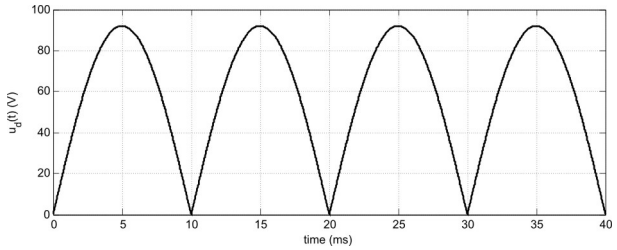
Figure 10: Equivalent circuit to harmonic components

4 Simulation and experimental results

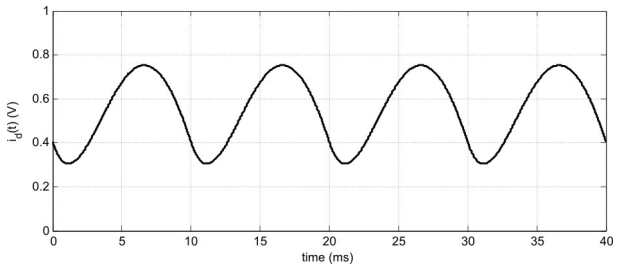
The full wave diode rectifer in Fig.1 is practised experimentally. The internal impedance, R_s and L_s, on AC side of the rectifier are 2Ω, 1mH and the load resistance R_L and load inductance L on DC side are 96Ω and 200mH,

the max. value of the source voltage U_m is 92V and the frequency is 50Hz. The diodes are assumed to be ideal. The measurements are obtained by a power quaility analyzer.

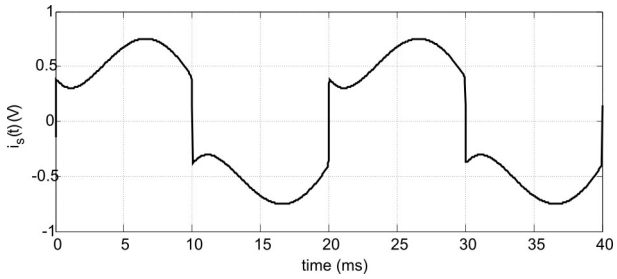
The simulations results and experimental results are given in Fig.11 and Fig.12, respectively. The load voltage, $u_d(t)$, load current, $i_d(t)$ and source current, $i_s(t)$ waveforms relating to the exact equivalent circuit in Fig.8 are given in Fig.11.



(a) Load voltage, $u_d(t)$



(b) Load current, $i_d(t)$

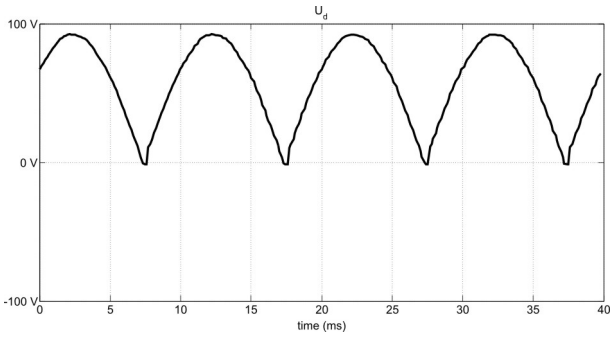


(c) Source current , $i_s(t)$

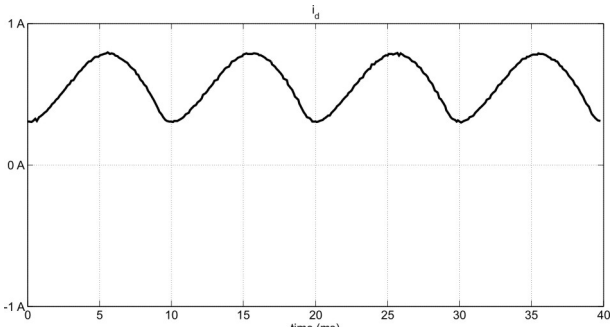
Figure 11: Simulation results relating to the equivalent circuit

The experimental results to load voltage, $u_d(t)$, load current, $i_d(t)$, and source current, $i_s(t)$ are given in Fig.12.

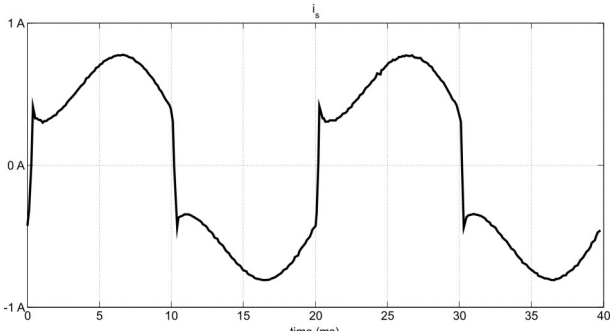
The fundamental component of source current, $i_{sf}(t)$, relating to Fig.9 are given in Fig.13. The desired harmonic components can be easily obtained by the proposed model. The waveform of harmonic components, $i_{sh}(t)$, except the fundamental component, of source current, relating to Fig.10 is given in Fig.14.



(a) Load voltage, $u_d(t)$



(b) Load current, $i_d(t)$



(c) Source current , $i_s(t)$

Figure 12: Experimental results relating to Fig.1

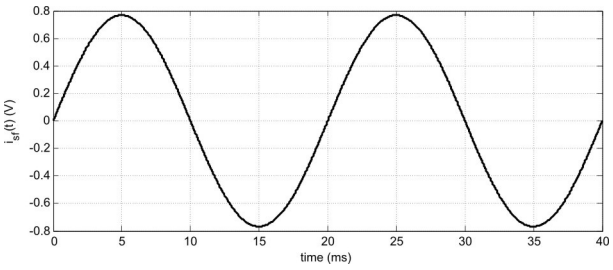


Figure 13: Simulation result relating to fundamental component, $i_{sf}(t)$

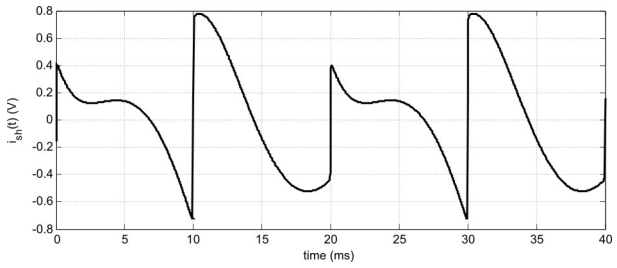


Figure 14: Simulation result relating to harmonic component, $i_{sh}(t)$

5 Conclusion

For an accurate harmonic analysis of converter circuits, the adequate models of harmonic sources are required. For a general analysis, the paper describes the exact equivalent circuit containing nonuniform current harmonics on AC side and voltage harmonics on DC side of rectifiers. The exact formulation relating to the solution and the model is also given. The main contribution of paper is that the circuit model is general because it contains both source/load impedances and nonuniform load currents. By the proposed model, the switching circuit is converted into a linear and non-switched circuit with regards to harmonics. The desired harmonic components are easily obtained by the proposed model. This appraoach can be also applied to other rectifier structures.

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Implementation of Non-periodic Sampling True Random Number Generator on FPGA

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Abstract: Random numbers are essentially required for various cryptographic applications. It is ideal to use nondeterministic random number generators in cryptography field since they are able to generate high-quality random numbers. In this paper, a Ring Oscillator (RO) based True Random Number Generator (TRNG) that can be used in cryptographic applications was developed. In this system, random numbers are generated by non-periodic sampling. Sinusoidal iterator with chaotic behavior was used for generation of non-periodic sampling signals. In TRNG system; three different scenarios, each of which contains three inverters, with 25, 10 and 5 RO circuits were implemented on FPGA environment. Randomness tests of numbers that are generated by TRNG with non-periodic sampling were carried on according to the NIST 800.22 test suit.The results have shown that the proposed system can be used in the cryptographic systems.

Keywords: Non-periodic Sampling, Ring Oscillator, Jitter, Statistical Test

Implementacija neperiodičnega vzorčnega generatorja naključnih števil na FPGA

Izvleček: Naključna števila so izrednega pomena pri številnih kriptografskih aplikacijah. Idealna je uporaba nedeterminističnih generatorjev naključnih števil, saj ti zagotavljajo visoko kvalitetna naključna števila. V članku je predstavljen generator naključnih števil (TRNG) na osnovi obročnega oscilatorja (RO). Naključna števila so v sistemu generirana z neperiodičnim vzorčenjem. Za generiranje neperiodičnih signalov vzorčenja je bil uporabljen sinusoidni iterator s kaotičnim obnašanjem. V TRNG sistemu so uporabljeni trije scenariji s po tremi razsmerniki s 25, 10 in 5 RO vezji v FPGA okolju. Test naključnosti števil je bil izveden na osnovi NIST 800.22 testnega procesa. Rezultati upravičujejo uporabnost predlaganega sistema v kriptografiji.

Ključne besede: neperiodično vzorčenje, obročni oscilator, statistični test

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1 Introduction

Random numbers are expected to have three essential features to be used in computer sciences. Firstly, generated numbers are to be unpredictable. Secondly, generated random numbers are required to have good statistical properties. Lastly, generated number streams should not repeat again. TRNG consists of three main parts as shown in Figure 1.1. These are Noise Source, Digitizer and Post-Processing. To generate random numbers, the first thing to do is to obtain a random signal from noise source. Thermal noise from a diode, jitter from a clock signal, metastability in a signal or mouse movements can be generally used as noise source. Discrete *s/i/* signal is obtained by sampling *n(t)* signal from noise source. When noise source is not ideal, *s/i/* signal does not have good statistical properties. Therefore, post-processing is preferred to improve the shortcoming of noise source or to obtain numbers with good statistical properties. After this stage, numbers are subject to statistical tests so as to determine whether they are random or not.

Generation of key in uncontrolled and unreliable environment negatively affects the system security of cryptographic applications. Thus, it is more appropriate to generate keys on hardware in terms of system security. It is getting more and more popular to generate keys on programmable hardware such as FPGA /1, 2, 3/. One

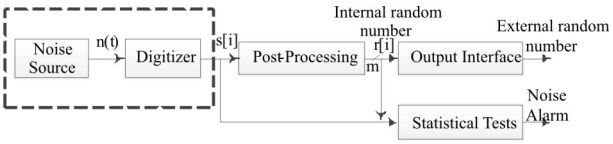

Figure 1.1: TRNG structure

of the most common methods to generate random numbers is to use Ring Oscillator structure achieved by inverters in FPGA /4/. There are 114 ROs and 13 inverters in each RO in TRNG system proposed by /4/. Post-processing is employed to improve statistical properties of generated random numbers. Random numbers were able to be generated at 2.5 Mbps data rate in this system. The drawback of this system is high power consumption. A new RO based structure was proposed by /1/ to overcome this drawback. In this structure, each RO has got a sampling unit. Number of ROs and number of inverters in each RO were decreased to 25 and 3 by using separate sampling units, respectively. This system manages to generate random number with good statistical properties at 100 Mbps since it does not include post-processing unit. It is suggested that post-processing unit is to be used in TRNG systems with cryptographic applications /5/. However, it is not ideal to use the system in /1/ for cryptographic applications since it does not have post-processing unit. In literature, basic processes such as XOR, Von Neumann corrector and LFSR (Linear Feedback Shift Register) Shuffler are used as post-processing /4, 6/. Although post-processing decreases data rate of TRNG, it is to be utilized in cryptographic applications /5/.

In addition to these approaches, random numbers can also be generated by Phase-Locked Loop hardware /6/. Usage of PLL (Phase-Locked Loop) in TRNG systems is rare due to the fact that PLL are limited in FPGA hardware. In another study, Open Loop Structure TRNG was proposed for usage of generated numbers in cryptographic applications /7/. The biggest advantage of this system is that it generates numbers at high data rates and does not require special components such as PLL. In /8/, random numbers could be generated at 20 Mbps by Open Loop Structure on FPGA. Besides, hybrid structures including usage of TRNG and PRNG (Pseudo Random Number Generator) were also proposed in literature /9, 10/. Structures such as Linear Feedback Shift Register (LFSR), chaotic map and cellular automata were used as PRNG /11, 12, 13, 14/. In /15/, the method and design of a pseudo random binary sequence generator operating at 10 Gb/s was implemented. In /16/, a PRNG was designed with usage of logistic map. The system has three logistic maps that are authenticated by different initialization vectors. The proposed system successfully passed statistical tests. Although PRNGs are not utilized in cryptographic applications, the system was analyzed against brute force and differential attacks. After all, the system was proved to be convenient for cryptographic applications. Sequential and parallel hybrid system was proposed by using LFSR structure in /17/. The system was developed on FPGA environment and it obtained successful results against cryptographic attacks.

In this paper, a RO based TRNG system was proposed for random number generation. The proposed system was implemented on FPGA for 3 different scenarios. Jitter, which is obtained from Ring Oscillators on FPGA, was used as noise source. Sampling of jitter was done by usage of non-periodic signals. Sinusoidal iterator, having chaotic behavior, was employed to get non-periodic signal. The system was implemented on FPGA hardware in real time, and statistical tests of generated numbers were conducted according to NIST 800.22 test suit.

Our contribution in this paper can be summarized as below.

It was shown that true random numbers generated by non-periodic sampling instead of periodic sampling can be used in cryptographic applications. A TRNG system that can operate in real time was developed. TRNG system could be turned into a more simple structure as statistical properties of numbers generated in three different scenarios were found to be good. Hence, the proposed TRNG structure is simpler than others in literature.

2 True random number generator

One of the most effective ways to generate random numbers is to use a noise source. Deviations of clock signals, which are generated in noise source, vary from their correct positions. This variability is called as jitter. Jitter, generated by clock signals, can be expressed by the Gaussian distribution as shown in Equation 2.1 /18/.

$$J_{RJ}(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\left(\frac{x^2}{2\sigma^2}\right)} \quad (2.1)$$

Jitter is generally an undesired feature in a system. Due to being random, it is ideal to use jitter in systems such as TRNG. Figure 2.1 shows a jitter occurring in a clock signal.

TRNG systems need to contain two oscillators, one is fast and the other is low, as shown in Figure 2.2. While fast oscillator is obtained from a noise source, low oscillator can be a periodic or non-periodic signal. Clock signal from noise source is sampled in low oscillator by

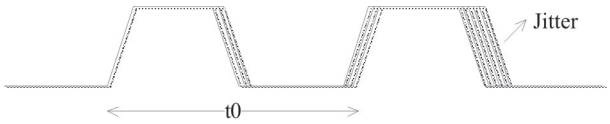

Figure 2.1: Jitter occurring in a clock signal

D flip flop. If the standard deviation in the period of the low oscillator is much greater than the fast oscillator, two consecutive samplings in the oscillator being sampled are regarded as uncorrelated /19/. In other words, numbers generated by sampling are going to be random.

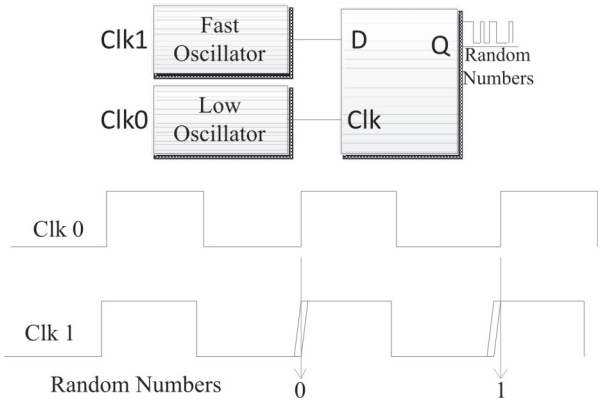

Figure 2.2: Random number generation

Usage of ROs is a classical method in TRNG. Quality of random numbers generated by a RO-based TRNG depends on three parameters below. These are:

- Number of oscillators in system
- Sampling frequency
- Number of inverters in oscillators

Randomness of numbers generated by TRNG is dependent on variability of jitter signal from each RO. Figure 2.3 shows structure of a simple RO.

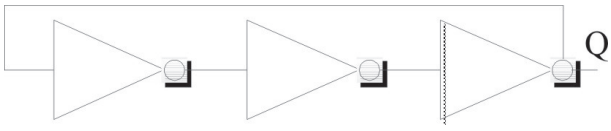

Figure 2.3: Structure of a simple RO

Frequency of signal from RO is as expressed in Equation 2.2. f_s is proportional to number of inverters (n) in system and delay time (t_{inv}) of inverter achieved by LE on FPGA.

$$f_s = \frac{1}{(2nt_{inv})} \tag{2.2}$$

Frequency of low oscillator is to be lower than f_s to be able to generate random numbers by RO-based TRNG.

3 Sinusoidal iterator

Functions with chaotic behaviors can be used as random number generators when given an initial value or seed value. Different number streams can be generated in a fast and easy way by changing initialization condition /20/. One of the functions is sinusoidal iterator given in Equation 3.1.

$$x_{n+1} = ax_n^2 \sin(\pi\, x_n) \tag{3.1}$$

The simplified form of Equation 3.1 for a= 2.3 and seed value x_0=0.7 is as shown in Equation 3.2. Figure 3.1 shows change of random number obtained after 1000 iterations for seed value x_0=0.7.

$$x_{n+1} = \sin(\pi\, x_n) \tag{3.2}$$

Figure 3.1: Change of random numbers obtained by sinusoidal iterator for seed value x_0=0.7

4 Non-periodic sampling TRNG

The TRNG system used in this paper is based on the system proposed by Knut Wold. Knut's system has 25 ring oscillators, each of which has 3 inverters. Instead of using post-processing, output of RO was sampled so that statistical deficiency caused by ROs could be eliminated. However, post-processing unit is advised to be included for cryptography applications. In this paper, non-periodic sampling TRNG system was experimented for three different scenarios. Firstly, non-periodic TRNG structure which includes 25 ROs with 3 inverters each was achieved. Statistical tests of random numbers generated by this structure were successful. In the following configurations, RO number was decreased to 10 and 5 ROs, respectively. Two non-periodic sampling TRNGs were developed on FPGA. Random numbers generated by systems in last two scenarios were also successful in NIST tests.

By this way, TRNG structure was simplified. Each scenario includes XOR post-processing unit. Sinusoidal iterator was used for non-periodic sampling in the system. The reason why Sinusoidal iterator is used instead of simpler structures such as Linear Congruential with chaotic behavior was that sinusoidal iterator has good randomness feature /21/. Figure 4.1 shows implementation of sinusoidal iterator on FPGA.

Random number generation was achieved by sinusoidal iterator, and thus non-periodic sampling signal was also obtained. Multiplication, sinus and comparison modules that can operate with floating point num-

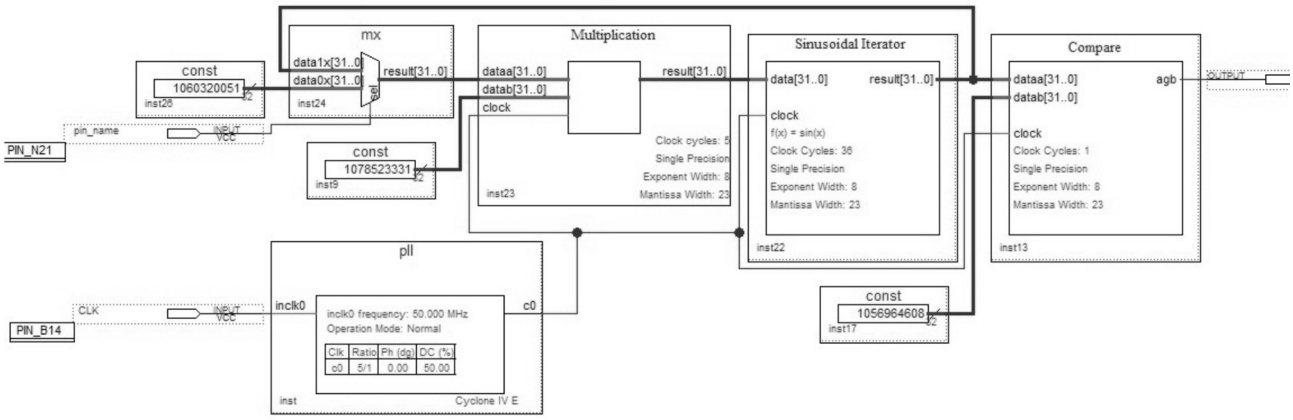

Figure 4.1: Implementation of sinusoidal iterator on FPGA

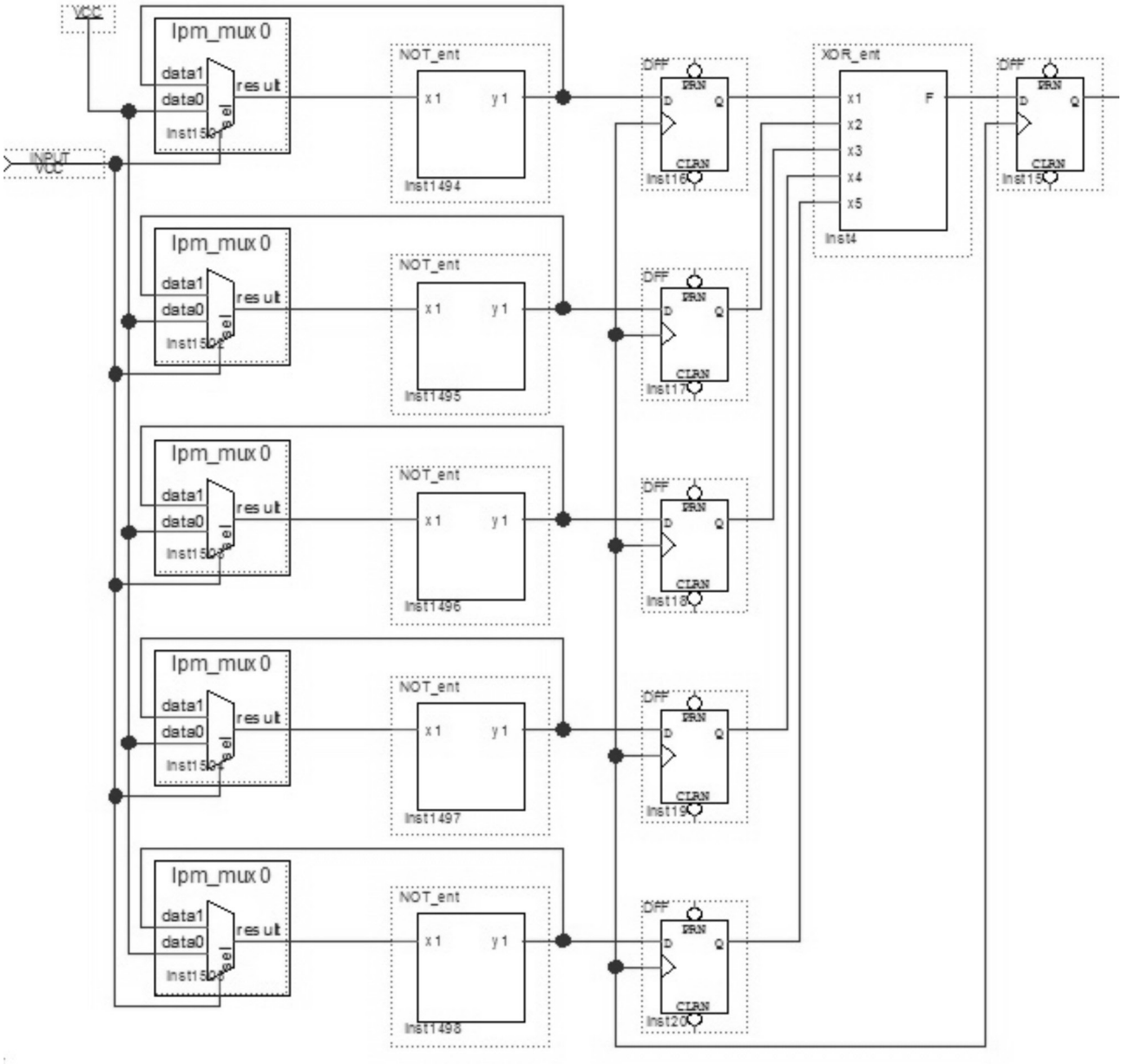

Figure 4.2: Implementation of TRNG with 5 ROs on FPGA

ber were used to achieve sinusoidal iterator. Besides, constant modules were also included so that mux and floating point number could be also used in the system. The value obtained as output, x_n, was provided as input value for the next iteration by mux so that the system could continuously generate random numbers. Initially, the system initialization value (x_0), the seed value in other words, was loaded. Const2 module was loaded by 0.7 or $(3f333333)_H$ in floating number expression. Const1 module was loaded by pi value or $(4048f5c3)_H$ in floating number expression. In order to represent floating point number generated by sinusoidal iterator as 0 and 1, floating number is compared with 0.5 or $(3f000000)_H$ in the output. The clock signal in the system is 200 MHz and the sampling signal obtained by sinusoidal iterator is generated once in 42 clocks. This duration is the sum of the executive times of multiplication (5 clocks), sinus (36 clocks) and comparator (1 clock) hardwares. The generated signal was fed to sampling system of TRNG as input. Figure 4.2 shows TRNG structure which consists of 5 ROs. A separate sampling unit was employed for each RO. Random numbers obtained as a result of sampling were once again sampled in XOR circuit and true random numbers were generated. Lastly, generated numbers were subject to post-processing to improve their statistical properties. In the end, numbers generated in real time were stored in a memory unit so that statistical tests could be applied on them. Figure 4.3 shows the memory unit, where numbers are stored to carry out statistical tests of numbers which are generated by non-periodic sampling TRNG.

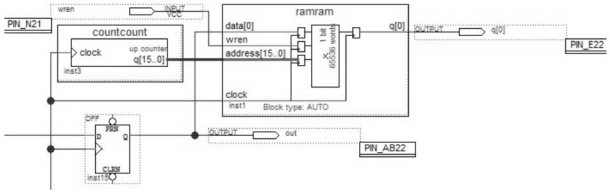

Figure 4.3: The memory unit

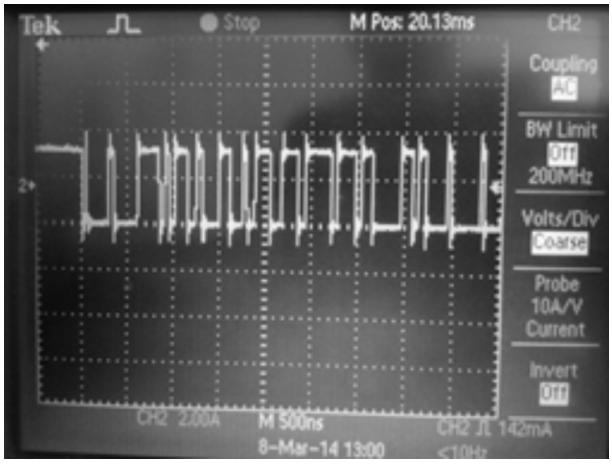

Figure 4.4: Random numbers generated in real time

The proposed structure was implemented in real time on Altera-based Cyclone IV FPGA. The change of random numbers generated by hybrid systemin real time was given in Figure 4.4.

5 Statistical tests and results

Statistical test suites play a very important role in assessing the randomness quality of numbers produced by random number generators. Several tests were developed to analyze randomness of numbers generated by generators. One of these tests is NIST test suit. There are totally 15 tests in NIST test suit, and parameters of each test are mentioned in /22/. The value α is one of the most important parameters used in tests and at the same time it is known as significance level. Determining significance level as 0.01 declares that randomness of numbers to be tested has 99% confidence value. Another parameter is P-value and known as measurement of randomness. If P-value equals to 1, numbers have perfectly random. If P-value equals to 0, then numbers are not random at all. Significance level, α, of numbers to be used in cryptographic applications must be chosen as an appropriate value. A test is assumed to be successful if P-value is equal to or greater than α value. Otherwise, test is considered to be unsuccessful and numbers are not random. Significance level is generally chosen between /0.001, 0.01/. The significance level in this paper was chosen as 0.01. The test was assumed to be successful in case the P-value obtained from each test is greater than 0.01. Results of P-value regarding to numbers generated by the system for 3 scenarios were given in Table 5.1. Numbers generated by the system successfully passed all of the tests as shown in the Table 5.1.

Table 5.1: NIST test results

Tests	P_{Value} (5 RO)	P_{Value} (10 RO)	P_{Value} 25RO
The Frequency (Monobit) Test	0,327	0,356	0,427
Frequency Test within a Block	0.446	0,412	0,598
The Runs Test	0.501	0,853	0,856
Tests for the Longest-Run-of-Ones in a Block,	0.751	0,652	0,840
The Binary Matrix Rank Test	0.398	0,742	0,873
The Discrete Fourier Transform (Spectral) Test	0.644	0,349	0,657
The Non-overlapping Template Matching Test	0.611	0,599	0,819
The Overlapping Template Matching Test	0.763	0,845	0,659

Maurer's "Universal Statistical" Test	0.730	0,945	0,783
The Linear Complexity Test	0.815	0,421	0,594
The Serial Test	0.494	0,584	0,688
The Approximate Entropy Test	0.437	0,746	0,841
The Cumulative Sums (Cusums) Test	0.506	0,355	0,322

Table 5.2 denotes number generation rates and the used ROs numbers of both proposed method and RO based TRNG known in the literature. The number generation rate of the proposed system is 4.77 Mbps and the number of ROs used is 5. According to Table 5.2, when compared our method with other TRNGs, it can be said that the proposed method is a more appropriate design. The number of ROs decreased from 25 to 5 since numbers generated by the system succeed in NIST tests. This is because the system generator numbers by non-periodic sampling and randomness is provided with respect to NIST tests. In spite of the above advantage, the system has a handicap; the power consuming of the system is high because of non-periodic sampling generator. As a remedy to this handicap, we propose the use of a LUT(Lookup Table) based hardware containing signals generated by sinusoidal iterator.

Table 5.2: Compare of both proposed method and RO based TRNG known in the literature.

TRNG	Rate (Mbps)	Number of ROs	Number of inverters in each RO
Multi oscillator rings (Sunar et al. /4/)	2.5	114	13
Multi oscillator rings (Wold et al. /1/)	100	25	3
Multi oscillator rings (Schellenkens at al./23/)	2.5	110	3
The proposed method	4,77	5	3

6 Conclusion

One of the most significant tasks in cryptographic systems is generation of keys in secured environments. Therefore, it is critical to generate keys by a random number generator on hardware such as FPGA. In this paper, non-periodic sampling TRNG system was implemented on FPGA in real time. NIST 800.22 test suit was applied on generated numbers to show that the developed system is suitable for cryptographic applications. Random numbers generated by 3 different scenarios were found out to attain good statistical properties. Another advantage of the proposed system is that the unpredictability of generated number streams was enhanced by non-periodic sampling unit. In other words, the system is more resistance against cryptographic attacks. The disadvantage of the system is that extra logic elements were required to implement sinusoidal iterator and the average data rate was 4.77 Mbps.

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A New Method for Hybrid Pseudo Random Number Generator

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Abstract: Powerful cryptographic systems need qualified random numbers. Qualified random numbers need providing good statistical qualities, not predicting and not re-generating. The numbers generated by raw Pseudo Random Number Generators (PRNG) can be predicted when their seed value are detected or the functions used in the system are not complicated enough. Moreover, the stream generated repeats itself after its period is exhausted. Due to these shortcomings mentioned above, raw PRNGs are not suitable for the cryptographic applications. In order to eliminate these shortcomings, by adding an additional input to the raw PRNG system, a hybrid structure is suggested in this study. In the hybrid system, a chaotic attraction in order to generate pseudo random number and a TRNG system having 5 Ring Oscillator (RO) each of which includes 3 inverters as the additional input were used. The random numbers obtained from the suggested hybrid structure were exposed to the NIST 800.22 statistical tests and it is shown that hybrid system can be used in the cryptographic systems.

Keywords: Random Number Generator, Chaotic Attractor, Additional Input, Hybrid Pseudo Random Number Generator

Nova metoda za hibridne pseudo naključne generatorje števil

Izvleček: Dobra kriptografija potrebuje kvalitetna naključna števila. Kvalitetna naključna števila zahtevajo dobro statistično kvaliteto, ki ni predvidljiva in ponovljiva. Števila generirana s psevdonaključnim generatorjem (PRNG) so lahko predvidljiva, če je odkrito seme in če sistemske funkcije niso dovolj kompleksne. Poleg tega se po preteku periode generiranje števil ponovi, zaradi česar PRNG ni primeren za kriprografijo. Kot rešitev problemov predlagamo uvedbo hibridnega sistema, ki dodaja dodatno vhodno spremenljivko PRNG. V hibridnem sistemu je bil uporabljen TRNG sistem s petimi obročnimi oscilatorji s tremi razsmerniki. Generirana števila so bila podvržena NIST 800.22 testu, ki je pokazal uporabnost hibridnega sistema za kriptografske namene.

Ključne besede: generator naključnih števil, dadaten vhod, hibridni prevdo naključen generator števil

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1 Introduction

The numbers obtained from the random number generators are needed in the statistical samplings, simulations, numerical analysis, entertainment and cryptography. In the various cryptographic applications, especially random numbers are obligatory because cryptography needs random numbers to generate and distribute the keys, to make the initial vector, to generate prime numbers and passwords and in the identity verification authentication protocols. The security of a cryptographic system depends on the true randomness of the numbers obtained. For that reason, the random numbers used in the cryptographic systems have to supply some basic requirements, which are good statistical qualities and not being predicted. As a result, qualified cryptography needs qualified random numbers [1].

In order to obtain random numbers, different random number generators were developed [2-4]. In general, these random number generators are classified as True Random Number Generators (TRNG) and pseudo random number generators (PRNG).

The True Random Number Generators generate random numbers by using the real physical processes which cannot be controlled and predicted as the noise

source. The randomness and the qualities of the random numbers generated by the TRNG depend on the randomness of the physical processes. If there are unpredictable physical processes, the numbers generated cannot be predicted and controlled as well. However, some bit stream generated may have statistical weaknesses. In order to eliminate these weaknesses, the bit stream is exposed to post processing. While post processing applications eliminate the weaknesses, it leads to a decrease in the bit rate. TRNG's disadvantage is that it is slow, costly and depends on the hardware. However, TRNGs were used in a lot of applications in the cryptology as they supplied the qualities of not being predicted, not being re-generated and good statistical qualities which are obligatory qualities for the cryptographic applications [2, 5, 6]. Because of these qualities, TRNGs are used in the hybrid PRNGs as the additional input.

Raw pseudo random number generators cannot generate numbers without having an initial (seed) value. The seed must be chosen randomly. When the specified seed value is used as an input in a certain algorithm, long random number streams are generated. Raw PRNG's advantage is that it is cheap, fast, easily realized and does not need hardware. However, the numbers generated by the raw PRNGs are easily predicted when their seed value is detected or the functions used in the system are not complicated enough. Also, the stream generated repeats itself after its period is exhausted. Due to these shortcoming mentioned above, raw PRNGs are not suitable for the cryptographic applications [2, 7, 8].

Many raw PRNGs are designed as the chaotic system [3, 4]. The most important feature of the chaotic systems is that they depend on the start (initial) condition. These systems show unpredictable behaviours and features which are not periodical [9, 10]. There are different studies performed by using chaotic signs. Some of these studies are double scroll chaotic structure [3, 11], performance scale for the random number generator based on discrete time chaos [4] and oscillator sampling method [5]. Though the discrete time chaotic systems are too simple models, they are insufficient in terms of complicatedness. That's why, more complicated chaotic systems must be used.

Different entropy sources such as jitter and metastable were used in TRNG. Especially the jitter in the ROs was preferred in many TRNG applications. TRNG in the study performed at [6] consist of 114 RO and each RO from 13 inverters. The random signals obtained by RO were combined XOR process. The signals obtained after XOR process was sampled by using D flip-flop. In this method, a random number that has a 2.5 Mbit/s data rate was generated. However, the power consumption is too high due to using too many logic components in the system. The design performed at [12, 6] was obtained by using 110 RO 3 inverters on Xilinx Virtex II Pro FPGA. The output rate obtained 2 Mbps. In [13], a new TRNG is suggested by adding a D flip-flop to the output of a RO in order to increase the randomness quality in the design performed at [6]. In the system, 25 ring oscillators and 3 inverters were used and the output bit streams were not exposed to a post processing. In this system, the output bit rate was obtained as 100 Mbit/s. 25 ROs and 3 inverters used in the study performed at [13] were decreased to 5 ROs and 3 inverters. As a result, the random numbers obtained were observed to pass the NIST statistical test.

In this study, in order to eliminate the shortcomings of the raw PRNGs such as being predicted, being regenerated and not providing good statistical qualities, additional input was supplied to the output function to provide complicatedness to the raw PRNG functions. The additional input increases the security because of bringing the quality of not being predicted and randomness qualities. Also, the PRNG structure used in the study is chaotic attractor with multiple modes. Random numbers were generated by sampling the state variable obtained from the 2+2, 2+4 and 5+4 chaotic attractor. By sampling the numbers obtained, raw random bit stream were obtained. The randomness of the raw bit stream obtained was tested by using the NIST test suit software performed at [14]. In order to eliminate the correlation in the raw random bit stream that have poor negative results, raw bit stream were exposed Von Neumann and XOR post processing. However, 2+4 and 5+4 chaotic attractor were detected not to pass the tests in the last process (post processing). For that reason, in order to increase the security of the system, the complicatedness of the output function and statistical quality, a TRNG generating true random number was added to the output function as the additional input.

The parts of this study were organized as follows. In part 2, pseudorandom number generators and additional input process was mentioned. In part 3, chaotic attractors used in the random number generator, adding an additional input to the raw PRNG system and the statistical test results of the random bit stream obtained by adding an additional input were given. In part 4, the fulfilment of the system by mentioning about the hybrid system proposed. In the last part, the results were assessed.

2 Pseudo random number generator

PRNGs have deterministic architecture and generated numbers by these generators show periodic characteristic [2, 7, 8]. Therefore, generated numbers by PRNGs are not true numbers. Pseudo random number can easily be generated by using a specific algorithm and seed. Although, obtaining a seed from random entropy source make difficult the estimation of the numbers generated by PRNG, it is possible to estimate the numbers.

In the Fig. 1, a general design of the raw PRNG is shown. $s_n \epsilon S$ is the internal state value of the PRNG. Here, the finite sets S and R are named as state space and output space. As seen in the Fig. 1, $\Psi:S\rightarrow R$ output function calculates the next random number r_n from the inner situation value s_n. Then, s_n value is changed with transition function $\phi_H(S_{n+1}=\phi(s_n))$ as s_{n+1}. The first state value s_1 is generated as $s_1=\phi(s_0)$ from the seed value used in the first entry s_0. The important part in the generating phase is that all the situation values $s_1,s_2,....$ and all the generated random numbers $r_1,r_2,\ldots$ depend on the seed value s_0. This poses a risk of exposure of the whole system if the s_0 value is known. That's why, in order to provide the quality of not being predicted, s_0 seed value has to be chosen randomly. Raw PRNG is defined with the stream of variables (S, R, Ψ, ϕ, p_s). Here, p_s is defined as the possibility distribution of the random seed. The generation of the seed is fulfilled outside of the PRNG system. In order to provide a quality of not being predicted, it is usually generated by a TRNG [2].

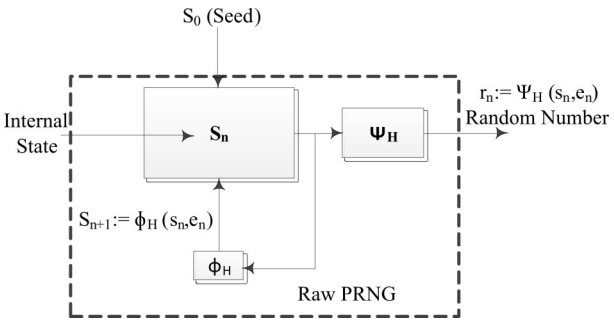


Figure 1: General design of the raw PRNG

The only disadvantage of the PRNG is that the random numbers are determined by the seed and the next random number depends only on the current internal state value. Their advantage is that it is cheaper compared with the other generators and does not need any hardware. In order to provide the feature of being unpredictable, the seed entropy must be large and the transition and exit functions must complicated enough.

In order to eliminate these mentioned shortcomings and to make its functions complicated, an additional input must be provided from $e_n \in E$ which is a finite set as seen in the Fig. 2, which is different from raw PRNG. The additional input increases the security due to its bringing the features of being unpredictable and randomness.

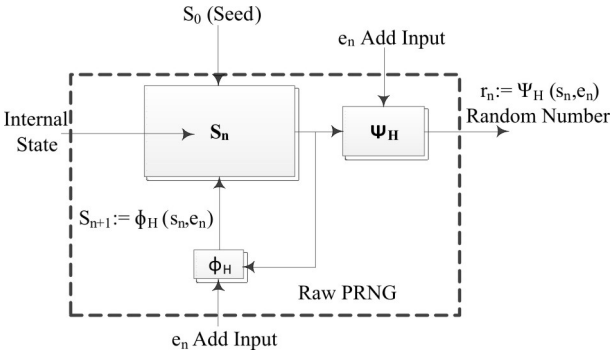


Figure 2: Hybrid design of the raw PRNG

3 Chaotic attractors

Recently, chaos has been started to use a lot in the random number generators [10]. It has been proved that chaotic number stream is easy and fast to generate and store. Only a few functions (chaotic map) and parameters (initial condition) are enough to generate long number streams. Also, too many different number streams can be easily generated by simply changing the condition of start. Thanks to these advantages, chaos has been started to use as the random number generator [10].

In this study, Chua circuit was used whose equations were given in (1), (2), (3) and (4) in order to obtain the chaotic attractor [15].

$$\begin{aligned} \dot{x} &= y + f_1(y) \\ \dot{y} &= z \\ \dot{z} &= -a \cdot x - a \cdot y - a \cdot z + f_2(x) \end{aligned} \tag{1}$$

$$f_1(y) = \sum_{i=1}^{M_1} g_{\frac{(-2i+1)}{2}}(y) + \sum_{i=1}^{N_1} g_{\frac{(2i+1)}{2}}(y) \tag{2}$$

$$f_2(x) = \sum_{i=1}^{M_2} g_{\frac{(-2i+1)}{2}}(x) + \sum_{i=1}^{N_1} g_{\frac{(2i+1)}{2}}(x) \tag{3}$$

$$g_\theta(\alpha) = \begin{cases} 1 & \alpha \geq \theta, \theta > 0 \\ 0 & \alpha < \theta, \theta > 0 \\ 0 & \alpha \geq \theta, \theta < 0 \\ -1 & \alpha < \theta, \theta < 0 \end{cases} \quad (4)$$

In the equation 2 and 3, M_1, N_1, M_2, N_2, i, j, $\in \Re^+$. The effect of $f_1(y)$ on the system is ignored and when a value is taken as 0.4, the system shows a double scroll attractor). $f_1(y)$ and $f_2(x)$ represent the split linear elements with many breakpoints and have the same characteristics. Y state variable affects $f_1(y)$ and x state variable affects $f_2(x)$. These elements show a dynamic structure depending on the M and N parameters. The number of the breakpoints and places are determined with the M and N values.

In the system, chaotic attractors will form along the linear of x and y=-ax+b. Chaotic scrolls under the effect of the $f_2(x)$ form along the axis of x. Chaotic scrolls under the effect of the $f_1(y)$ form along the linear of y=-ax+b. As chaotic attractors form in both directions, this behaviour type is named as the attractor of n+n. The first n value shows the axis of x and the other n value shows the total scrolls formed along the linear of y=-ax+b.

The behaviour of the system was obtained by solving the differential equation given in the equation of (1). Runge-Kutta method with four steps was used by using Matlab program. The start values of the state variables were taken as (x_0, y_0, z_0)=(0.1,0.1,-0.1) and a value was taken as 0.4. In the study performed in the [15], the experimental fulfilment of the attractors and their oscilloscope outputs were given.

The sampling process from X state variable obtained from the 2+2, 2+4 and 5+4 chaotic attractor given in the Fig. 3 was made as shown in Fig. 4. A raw bit stream was obtained by applying the rule shown in the equation 5 with the obtained numbers.

$$S(x) = \begin{cases} 0 & x < 0.5 \\ 1 & x >= 0.5 \end{cases} \quad (5)$$

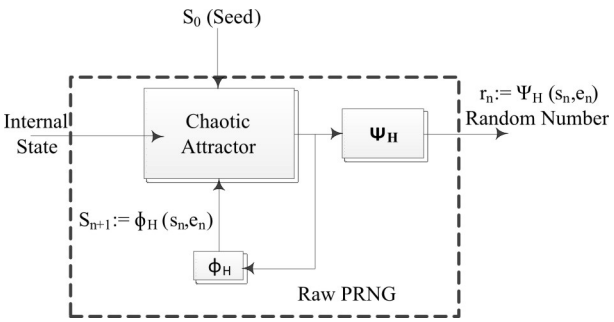


Figure 3: Raw PRNG based chaotic attractor

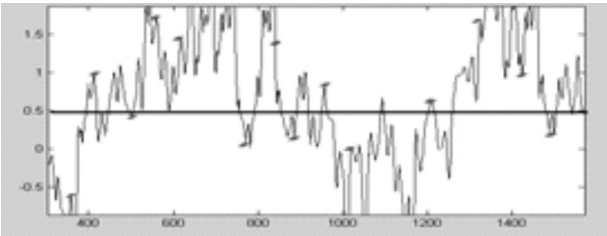
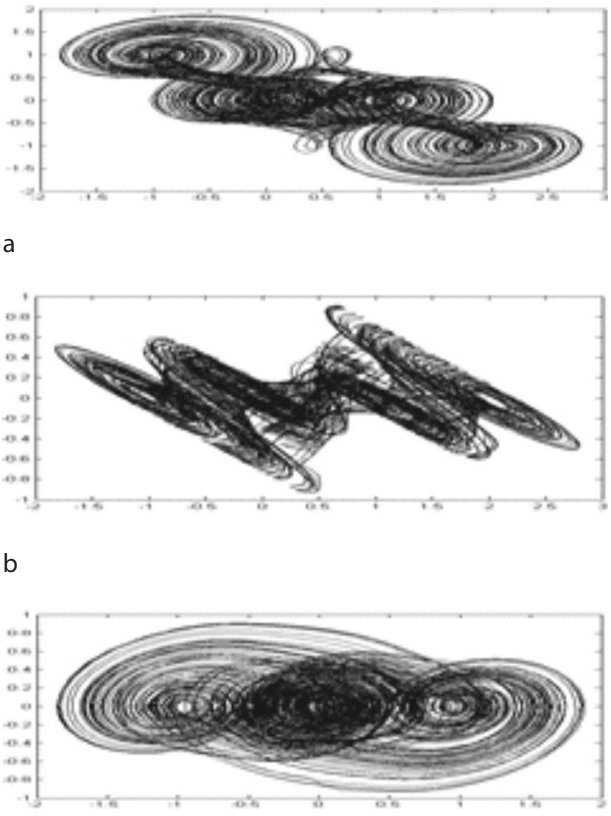


Figure 4: The simulation of a certain area of 2+2 attractor

3.1 Random Number Generation by Obtaining 2+2 Attractor and the Statistical Results

In order to obtain 2+2, M_1=1, N_1=2, M_2=0 and N_2=1 was taken and the changes of x-y, x-z and y-z obtained were shown in the Fig. 5 [15]. In the direction of PRNG design shown in the of Fig. 4, 108418 raw bit stream was obtained by taking a value in every 300 steps as from the first 500 numbers and without exposing to any post processing[16]. The statistical test results of the raw bit stream obtained were shown in Table 1.



a

b

c

Figure 5: 2+2 attractor illustration for M_1=1, N_1=2, M_2=0 and N_2=1 , (a) x-y change (b) x-z change (c)y-z change

Table 1: NIST test results for 2+2 attractor

Test Name	P value	Result
Frequency (Monobit) Test	0.151	Passed
Frequency Test within a Block	0.484	Passed
Runs Test	0.028	Passed
Test for the Longest Run of Ones in a Block	0.069	Passed
Binary Matrix Rank Test	0.675	Passed
Discrete Fourier Transform Test	0.442	Passed
Non-overlapping Template Matching Test	0.086	Passed
Overlapping Template Matching Test	0.778	Passed
Maurer's Universal Statistical Test	0.050	Passed
Linear Complexity Test	0.580	Passed
Serial Test	0.246	Passed
	0.594	
Approximate Entropy Test	0.106	Passed
Cumulative Sums Test	0.085	Passed

3.2 Random Number Generator By Obtaining 2+4 Attractor And The Statistical Results

In order to obtain 2+4 attractor, M_1=2, N_1=2, M_2=0 and N_2=1 and x-y, x-z and y-z obtained were shown in the Fig. 6 [15]. From the X state variable obtained from 2+4 attractor, a value was taken in every 1000 steps from the first 500 numbers and 122807 raw bit stream was obtained. The statistical test results of this obtained raw bit stream and the bit stream obtained after the post processing were shown in the Table 2.

3.3 Random Number Generator By Obtaining 5+4 Attractor And The Statistical Results

In order to obtain 5+4 attractor, M_1=2, N_1=2, M_2=2 and N_2=2 and x-y, x-z and y-z obtained were shown in the Fig. 7 [15]. From the X state variable obtained from 5+4 attractor, a value was taken in every 300 steps from the first 500 numbers and 99062 raw bit stream was obtained. The statistical test results of this obtained raw bit stream and the bit stream obtained after the post processing were shown in the Table 3.

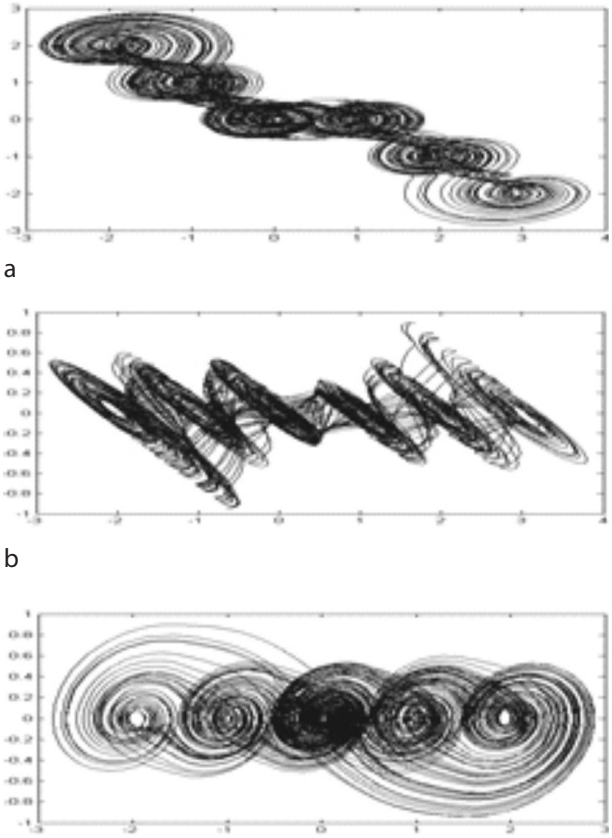
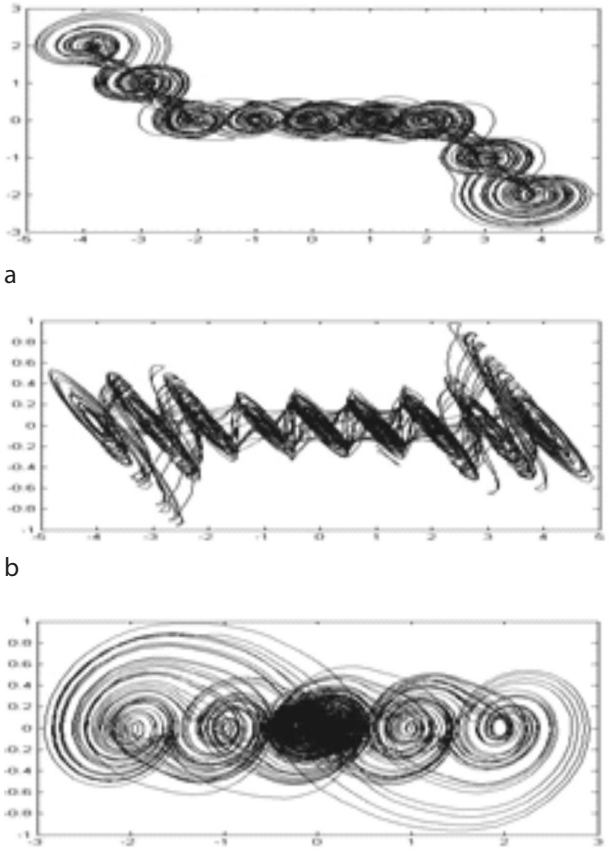


Figure 6: 2+4 attractor illustration for M_1=2, N_1=2, M_2=0 and N_2=1 , (a) x-y change (b) x-z change (c)y-z change

Table 2: NIST test results for 2+4 attractor

The name of the Test	P value 122807 bit	Van Neumann 24061 bit	Xor 61403 bit	Result
Frequency (Monobit) Test	0.786	0.259	-	Unpassed
Frequency Test within a Block	-	0.935	-	Unpassed
Runs Test	-	-	-	Unpassed
Test for the Longest Run of Ones in a Block	-	-	-	Unpassed
Binary Matrix Rank Test	0.343	0.809	0.491	Passed
Discrete Fourier Transform Test	-	0.516	-	Unpassed
Non-overlapping Template Matching Test	-	0.012	-	Unpassed
Overlapping Template Matching Test	-	0.138	-	Unpassed
Maurer's Universal Statistical Test	-	0.078	-	Unpassed
Linear Complexity Test	0.754	0.100	0.859	Passed
Serial Test	-	-	-	Unpassed
	-	0.496	-	
Approximate Entropy Test	-	-	-	Unpassed
Cumulative Sums Test	0.126	0.231	-	Unpassed



a

b

c

Figure 7: 5+4 attractor illustration for M_1=2, N_1=2, M_2=2 and N_2=2 , (a) x-y change (b) x-z change (c)y-z change

4 The proposed hybrid PRNG

In the system of raw PRNG performed by using chaotic attractors, the sampling process used in obtaining random numbers do not always produce good results.

Because, the correct determination of the threshold value shown in the equation 2 is very significant and this affects the quality of the entropy. For instance; 2+2 attractor passes the statistical results without exposing a post processing according to the results in the Table 1; whereas, it is observed that, with and without last processes (post processing), the results of the raw bit stream obtained from 2+4 and 5+4 attractors failed to pass the statistical tests, as seen in the of Table 2 and 3. Therefore, in order to increase the safety and the randomness of the 2+4 and 5+4 chaotic attractors, TRNG system was given as additional input as shown in the Fig. 8. In the system of TRNG, there are 5 RO, each of which contains 3 inverters. Fig. 9 shows the TRNG system used in the hybrid system.

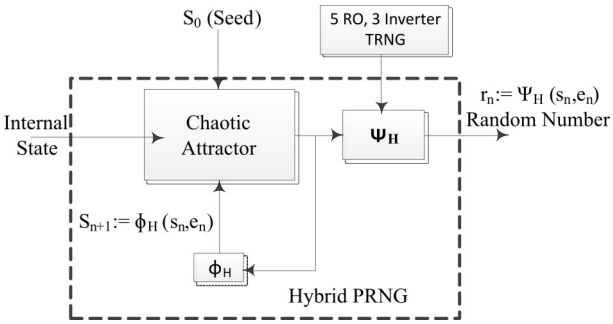


Figure 8: The suggested hybrid system

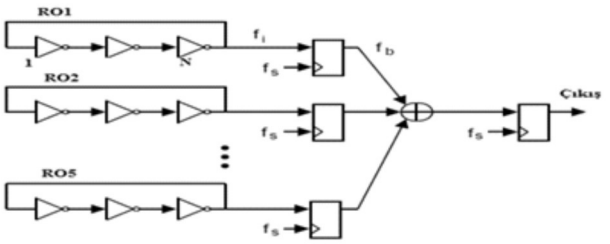


Figure 9: The design of 3 inverter 5RO TRNG

Table 3: NIST test results for 5+4 attractor

The name of the Test	P value 99062 bit	Van Neumann 13505 bit	XOR 49530 bit	Result
Frequency (Monobit) Test	-	0.636	-	Unpassed
Frequency Test within a Block	-	0.973	-	Unpassed
Runs Test	-	-	-	Unpassed
Test for the Longest Run of Ones in a Block	-	-	-	Unpassed
Binary Matrix Rank Test	0.194	0.683	0.414	Passed
Discrete Fourier Transform Test	-	0.022	-	Unpassed
Non-overlapping Template Matching Test	-	-	-	Unpassed
Overlapping Template Matching Test	-	0.142	-	Unpassed
Maurer's Universal Statistical Test	-	0.286	-	Unpassed
Linear Complexity Test	0.529	0.967	0.347	Passed
Serial Test	-	-	-	Unpassed
	-	0.013	-	
Approximate Entropy Test	-	-	-	Unpassed
Cumulative Sums Test	-	0.743	-	Unpassed

Fig. 10 shows RO in the TRNG system performed in FPGA. Each RO used in the system was performed by using data flow and schematic design methods with VHDL language [14].

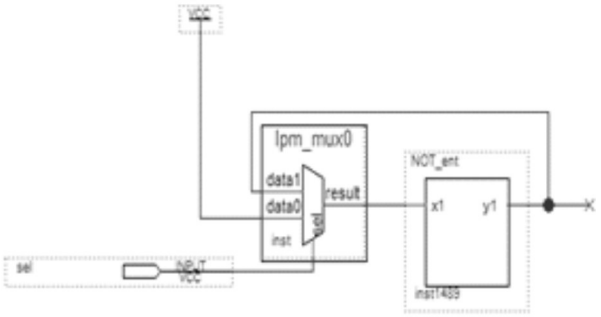
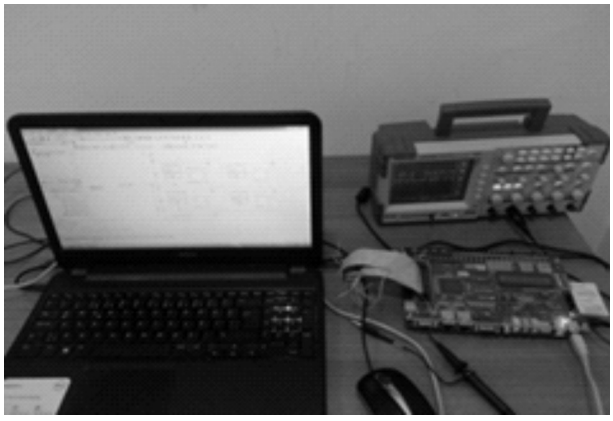


Figure 10: Ring Oscillator

In the Fig. 10, the inverter exit is always at the level of logic 0. In order for RO to obtain a random sign, RO exit (output) is obtained after giving an excitation signal (sel=1) from the physical environment. Random number generation is completed after sampling the random change obtained. Fig. 11 shows the performance of TRNG, used in the hybrid system, in FPGA. In order for the random numbers generated by the TRNG system to perform the statistical tests, the numbers were recorded to a memory unit. Fig. 12.a shows the appearance of the experimental set and Fig. 12.b shows the numbers generated by TRNG in the real time.



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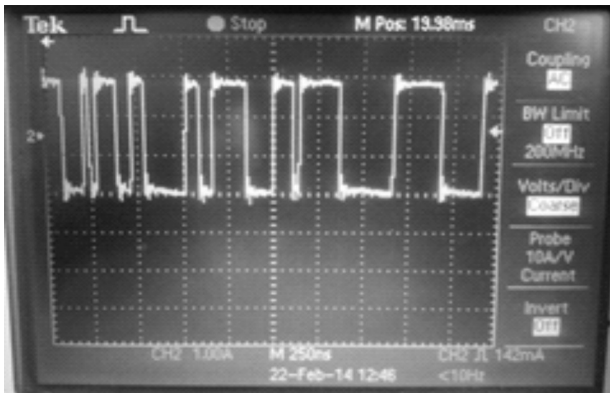

b

Figure 12: (a) The appearance of the experimental set (b)The bits for 5 RO and 3 inverters generated in the real time

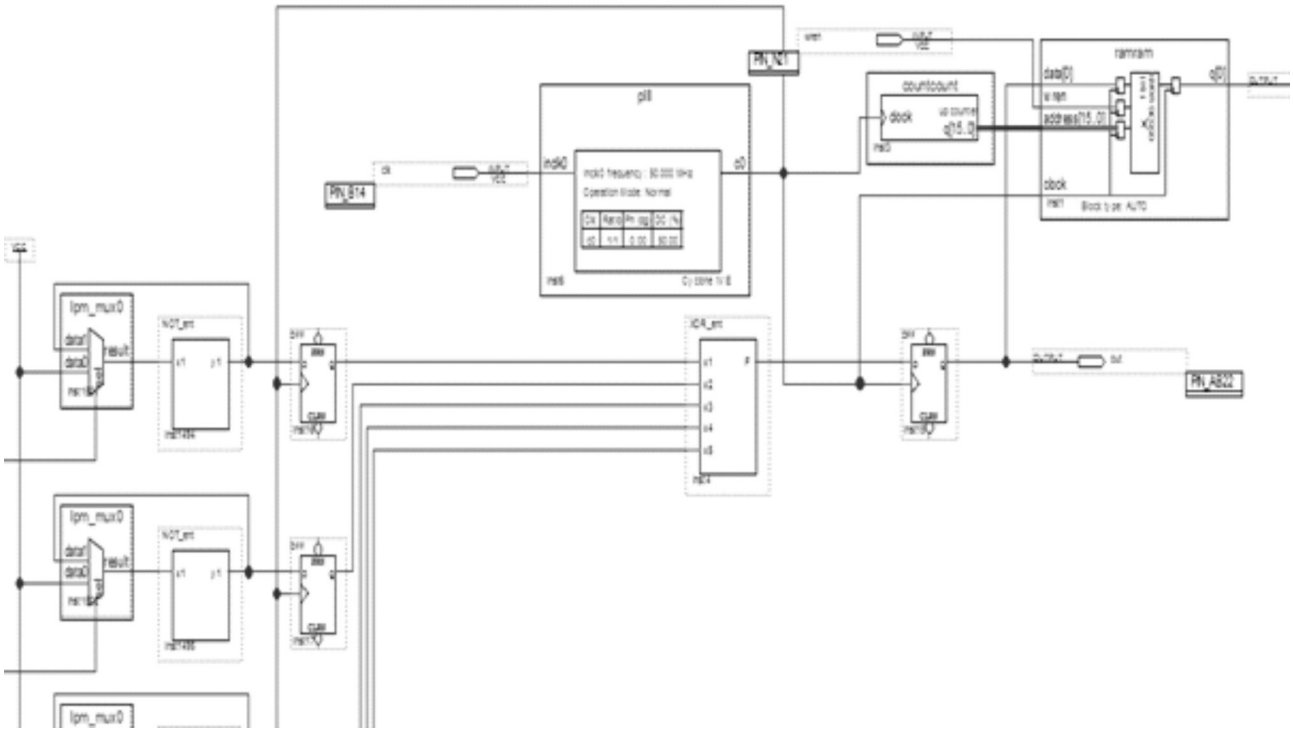

Figure 11: The performance of 5 RO and 3 Inverter TRNG FPGA

As seen in the Fig. 8, an output bit stream was formed by exposing the bit stream obtained from the chaotic attractor and TRNG design to XOR process in the exit function. As a result, the bit stream obtained was exposed to the NIST statistical test whose software was done in [16], without performing a post processing. The results of the suggested hybrid PRNG were given Table 4 and 5. It was observed that the bit stream obtained passed all the statistical tests without performing a post processing.

Table 4: Test result of hybrid PRNG for 2+4 attractor

The name of the Test	P value	Result
Frequency (Monobit) Test	0.506	Passed
Frequency Test within a Block	0.923	Passed
Runs Test	0.638	Passed
Test for the Longest Run of Ones in a Block	0.393	Passed
Binary Matrix Rank Test	0.833	Passed
Discrete Fourier Transform Test	0.029	Passed
Non-overlapping Template Matching Test	0.070	Passed
Overlapping Template Matching Test	0.997	Passed
Maurer's Universal Statistical Test	0.120	Passed
Linear Complexity Test	0.024	Passed
Serial Test	0.641	Passed
	0.210	
Approximate Entropy Test	0.868	Passed
Cumulative Sums Test	0.709	Passed

Table 5: Test result of hybrid PRNG for 5+4 attractor

The name of the Test	P value	Result
Frequency (Monobit) Test	0.656	Passed
Frequency Test within a Block	0.941	Passed
Runs Test	0.714	Passed
Test for the Longest Run of Ones in a Block	0.980	Passed
Binary Matrix Rank Test	0.404	Passed
Discrete Fourier Transform Test	0.016	Passed
Non-overlapping Template Matching Test	0.020	Passed
Overlapping Template Matching Test	0.269	Passed
Maurer's Universal Statistical Test	0.661	Passed
Linear Complexity Test	0.099	Passed
Serial Test	0.458	Passed
	0.584	
Approximate Entropy Test	0.243	Passed
Cumulative Sums Test	0.810	Passed

5 Results

In this study, an additional input was added to the system in order to eliminate the shortcomings of the pseudorandom number generators and increase the complicatedness of the functions used. Random bit stream obtained from the 2+2 chaotic attractor passed the statistical test results without performing a post processing. However, random bit stream obtained from 2+4 and 5+4 chaotic attractors failed to pass the statistical tests with and without post processing. In order to eliminate this disadvantage, TRNG was used as the additional input based on RO. Thus, the randomness and the safety of the system were increased and the random bit stream generated by the hybrid system passed the statistical tests. This result indicates that the hybrid system can be used in the fields of cryptography.

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Low-Kickback-Noise Preamplifier-Latched Comparators Designed for High-Speed & Accurate ADCs

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Abstract: High-resolution high-speed comparators are one of the main cores in the implementation of the high-performance systems, such as ADCs. Two comparators are presented in this paper where both of the structures are suitable for high-speed, low-noise and accurate applications. The comparators are designed, based on the positive feedback structure of two back-to-back inverters. An improved rail-to-rail folded cascode amplifier with an active bias circuit is utilized for the first architecture, in which the structure of the comparator is rearranged appropriate to the running comparison phase. Distinguished by its novel data reception style, a new comparator is proposed in the next circuit. In this structure, the hot n-well concept is considered for the PMOS transistors of the positive feedback latch. Applying the inputs to the bulks of the mentioned PMOS devices, isolates the regenerative outputs from the input signals; hence, a sizable attenuation in the kickback noise value is resulted. Merging the reset, evaluation and latch sequences makes it possible to decrease the comparison duration. Both of the proposed comparators of this paper benefits from this excellence, therefore an intensive increase is observed in their comparison speed. In order to confirm the performance accuracy of the circuits in various terms, multiple simulations are performed in all process corners, using HSPICE (level49) with a standard 0.35µm CMOS process and the power supply of 3.3V. VDD noise of 300mVp-p and alterations in temperature are also included in the simulation conditions. The simulation results confirm recognition of a differential input with 2mV pick-to-pick amplitude at as high a clock frequency as 800MHz with power consumption about 2.6mW for the first circuit and a 1mV differential input with update rate of 1GHz and power consumption about 1.6mW for the low-noise structure of the second comparator. According to the layout pattern, an active area of 55µm × 13µm and 24µm × 15µm is occupied by the improved folded cascode comparator and the proposed novel structure respectively.

Keywords: High Speed Comparator, Kickback Noise, High Speed ADC, High Resolution Comparator.

Visokozmogljiva primerjalnika z nizkim povratnim vplivom na osnovi topologije predojačevalnik-zapah za hitre in natančne analogno-digitalne pretvornike (ADC)

Izvleček: Visokoločljivi in hitri primerjalniki so osnova za izvedbo visokozmogljivih sistemov, kot so analogno-digitalni pretvorniki (ADC). V prispevku sta predstavljena dva primerjalnika, katerih struktura je primerna za hitre, nizkošumne in natančne aplikacije. Primerjalnika sta zasnovana na osnovi dveh povratno vezanih negatorjev. Pri prvem primerjalniku je uporabljen kaskodni ojačevalnik, pri katerem je struktura primerjalnika preurejena glede na tekočo fazo primerjanja. Pri drugem primerjalniku so vhodni signali priključeni na substrat tranzistorja prek diferencialnih tranzistorskih parov. S tem smo zmanjšali vpliv izhoda vezja in vrednost povratnega šuma. Predlagana vezja smo načrtali v 0.35 µm tehnologiji CMOS z napajalno napetostjo 3.3 V in, v postopku simulacije, preverili z uporabo programa HSPICE. Pri tem smo preverili vpliv napetostnih motenj v napajanju in spremembe temperature na delovanje primerjalnikov. Rezultati simulacij potrjujejo zaznavo diferencialne napetosti amplitude 2 mV pri frekvenci ure 800 MHz in porabo moči 2.6 mW za prvi primerjalnik in zaznavo diferencialne napetosti amplitude 1 mV pri frekvenci ure 1 GHz in porabo moči 1.6 mW za drugi primerjalnik. Površina vezja, ki jo zasedata primerjalnika, je 55µm × 13µm in 24µm × 15µm.

Ključne besede: hitri primerjalnik, povratni šum, hitri analogno-digitalni pretvornik, visokoločljivi primerjalnik

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1 Introduction

Although most of the parameters obtained from the nature by different sensors are analog by default, an analog to digital conversion process is required due to the vast improvements in the digital signal processing field. CMOS high-speed analog-to-digital converters (ADCs) are one of the best suited blocks for this purpose where some bottlenecks have to be solved. Precisely comparison of the analog input signal with a reference value and extracting the digital output bit is a great challenge and seems to be the main bottleneck of the process; hence, a high-speed, high-resolution and low-power comparator is needed to keep the overall performance of the system in an acceptable level. The input voltage of the comparators changes continuously which leads to some variations in their outputs at the input clock edges. Based on the comparison, the comparator outputs a High or Low signal.

Depending on their nature, functionality and inputs, comparators are classified into different types such as voltage or current comparators, continuous or discrete time comparators and so on. By another classification, there are two different kinds of comparators: single-stage and multi-stage comparators, [2]. Studding these two kinds, it can be understood that the multi-stage comparators have more power consumption, delay time and die size; however the single-stage ones usually have complicated switches which are required to be controlled accurately via additional controlling signals, [1,2]. Variety of the timing signals might increase the digital coupled noise to the analog section, also generation of these controlling signals requires some extra hardware which again increases the die size and the power consumption of the system. Multi-stage comparators are usually made up of three main stages; pre-amplifier, decision circuit (positive feedback or gain stage) and post-amplifier. The pre-amp stage amplifies the input signal to improve the comparison sensitivity through increasing the minimum detectable input signal by which the comparator can make correct decisions. Meanwhile, it isolates the input of the comparator from the switching noise which is produced by the positive feedback stage like the clock feed through and the kickback noise effect. The gain stage is used to determine which of the input signals is larger and the output buffer amplifies this information and produces a full-range digital data. In the single stage comparators, the three important phases of the comparison, reset, evaluation and latch, are performed via a single block. During the reset phase, the previous data stored in the parasitic capacitors is usually removed using a reset switch that connects the differential output nodes to each other. The second phase is evaluation in which the comparator begins to compare two inputs and decides whether the outputs should be high or low. In the latch phase, the evaluated outputs are separated up to the digital levels. Each of these phases need a certain timeframe, hence it can be concluded that the conversion speed is limited by the decision-making duration of the comparator.

CMOS process variation is the main origin of the offset voltage introduced to the latched comparators, which extremely restricts their comparison accuracy. Coupling a pre-amplifier stage before the output latch attenuates the input-referred offset voltage of the comparator, thus an accurate preamplifier-latch topology is engendered, [6-8], making it possible to utilize the comparator for high-resolution purposes.

Based on the folded cascode structure, a high-speed high-accuracy comparator with preamplifier-latch topology is improved for high-resolution applications. Moreover, another comparator is proposed in which a novel method is utilized for obtaining a high-resolution latched structure. Taking advantage of this circuit, both high speed and high accuracy beside low die size and lessened power consumption is achieved. Rest of the paper is organized in 6 sections. In the next section latched comparators are discussed, the improved folded cascode structure is presented in Section 3, the proposed new comparator circuit is detailed in Section 4, a new readout circuit is presented in Section 5, Section 6 verifies the simulation results, and the final section delivers the conclusion and the comparisons with similar works.

2 Latched Comparators

The threshold voltage of an inverter (V_{th}) is a boundary voltage that determines whether the value of the received signal is High or Low. As depicted in Fig. 1, this voltage is arisen from shorting the input and the output of an inverter. Value of the V_{th} depends on the threshold voltages of NMOS and PMOS transistors (V_{thn} and V_{thp}, respectively).

Threshold voltage for an inverter can be calculated according to (1) and (2).

$$I_{dp} = I_{dn} \tag{1}$$

$$\frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_n (V_{th} - V_{thn})^2 (1 + \lambda V_{th}) = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_p (V_{dd} - V_{th} - V_{thp})^2 (1 + \lambda [V_{dd} - V_{th}]) \tag{2}$$

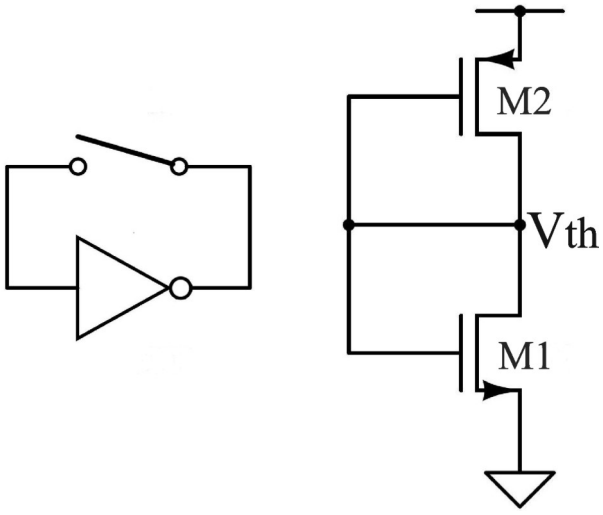

Figure 1: A CMOS Inverter with its Shortened Input and Output.

Ignoring the channel length modulation effect and applying the device sizes as $\mu_n (W/L)_n = \mu_p (W/L)_p$, (3) is obtained:

$$V_{th} = \frac{\left(V_{dd} + V_{thn} - \left|V_{thp}\right|\right)}{2} \quad (3)$$

As it's clear, the value of V_{th} depends on V_{thn} and V_{thp} so it is affected by the process variations, thus its value varies in different process corners. In TT, SS and FF corners V_{thn} is close to V_{thp} in value, so $V_{th} \approx V_{dd} / 2$ but due to inequality in the conductance of NMOS and PMOS devices, in FS and SF corners V_{th} is respectively a little bit greater or lower than $V_{dd} / 2$.

Fig. 2 illustrates two back-to-back inverters besides a reset switch. Variant fabrication process and asymmetrical doping generate two unequal threshold voltages for the inverters. While two output nodes (O_1 and O_2) are shorted by the reset switch, their voltage is equal to a value between two threshold voltages. Following the reset phase, each inverter amplifies the difference between its relevant threshold voltage and this value; due to the regenerative nature of this structure, O_1 and O_2 reach the logic levels.

Applying the input signal, the outputs have to be forced to be separated in desired direction. Because of the positive feedback nature of the system, one must reset the structure to clear the previous data, then evaluate the correct direction according to the inputs and finally ignite the regenerative latch.

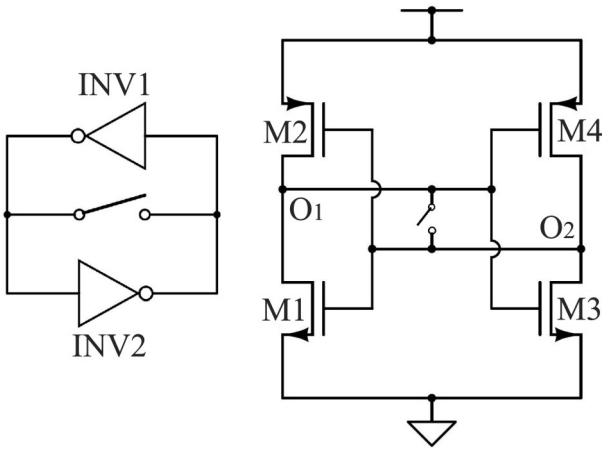

Figure 2: Block Diagram and Circuitry of Two Back-to-Back CMOS Inverters Forming an Intense Positive Feedback Structure.

3 Proposed High-Speed Comparator

Based on the described behavior of the latch block, a rail-to-rail folded cascode amplifier is modified using a positive feedback structure of two back-to-back inverters. Also an NMOS device is utilized as reset switch for removing the previously latched data from the output nodes. The structure is scheduled for performing the consecutive sequences of the comparison process (reset, evaluation and latch). The bias circuit is also an active block which alters the relevant biasing currents of the folded cascode in different operation modes. The proposed comparator structure besides its timing diagram is presented in Fig. 3. Four differential pairs (M_5 – M_{12}) are in connection with the cascode nodes of the amplifier. The analog input signals are applied to these differential pairs. The mentioned back-to-back inverter structure is formed by (M_1 – M_4). Two bias circuits are also observed in Fig. 3. The first section of the bias circuit (M_{21} – M_{23}) prepares the appropriate bias voltages for the current sources of the differential pairs. The next circuit is the active section of the bias block which provides the cascode devices (M_{13} – M_{16}) with variable bias voltage, proportional to the running operation mode.

Considering the timing diagram of Fig. 3, by rising edge of φ_1, two output nodes are shorted through S_1. By the same time the infirm PMOS device M_{25}, enfeebles the positive feedback force of (M_1 – M_4) which facilitates the data removal process. Unlike most of the latched comparators, in the proposed structure of Fig. 3 the reset and evaluation sequences are merged and can be performed simultaneously in separate nodes. While the reset phase is running at the regenerative outputs, the primary evaluation of the input signals is going on at the cascode nodes.

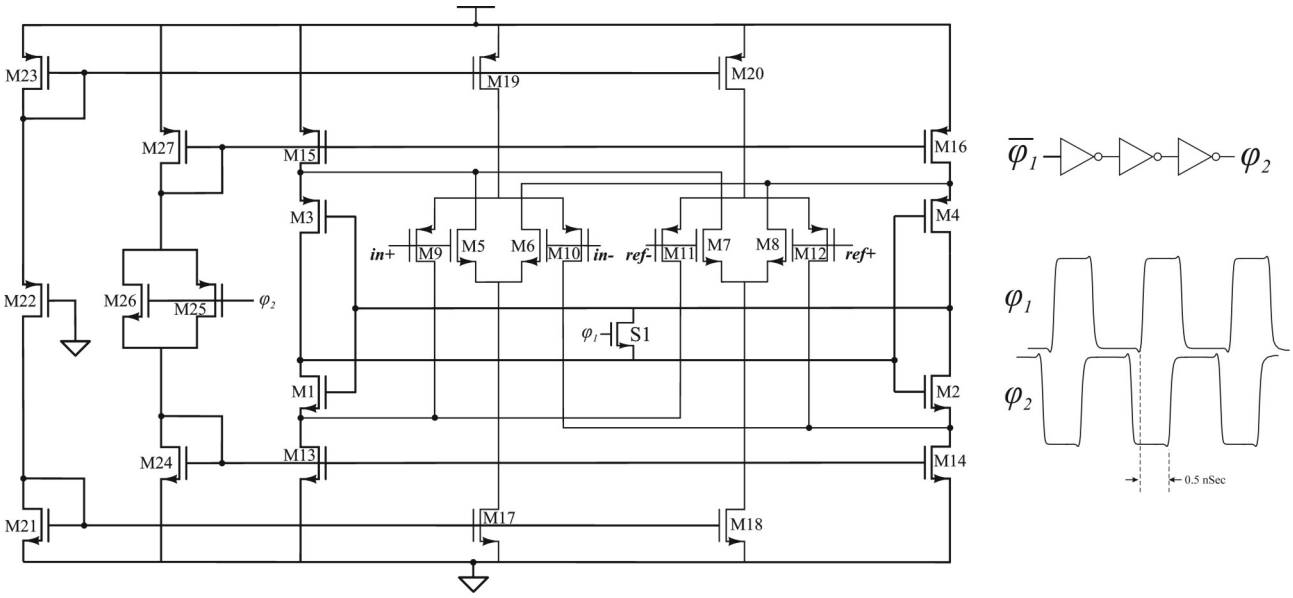

Figure 3: Improved High-Speed Comparator and its Timing Diagram.

After the evaluation, when the voltage difference reaches the detectable range of the positive feedback latch, M_{25} is replaced by M_{26}, at the rising edge of φ_2. So, the strength of the positive feedback is intensified again and the output voltages are separated up to the digital values. From another site of view, the evaluation phase has a separate timing schedule from reset and latch, making it possible to achieve both high speed and accuracy.

Kickback noise is a limiting factor for comparators accuracy [1, 4]. This kind of noise is mainly originated by the regenerative outputs of the positive feedback block. In the proposed comparator of Fig. 3 the current of the positive feedback inverters is limited by the cascode current sources (M_{13} – M_{16}), so rapid variations at the output nodes are avoided and hence the main source of kickback noise is limited.

4 Proposed Low Kickback Noise Comparator

The next proposed comparator is illustrated in Fig. 4. Similar to the comparator of the previous section, this structure also consists of two back-to-back inverters forming an intense positive feedback. What makes the proposed circuit distinguished is its novel data reception style. The input signals are applied to the bulks of the transistors via two differential pairs.

It is necessitous to reverse bias the drain-bulk diode of the transistors to insure their proper work, this affair can be realized in different ways. As it is done in mostly all conventional circuits one can ignore the bulks of the transistors and connect them to VDD and GND respectively for PMOS and NMOS devices. All NMOS transistors on a single die have one common bulk terminal which is the substrate of the chip, it must be connected to the lowest voltage of the circuit (usually GND) to avoid the drain-bulk diode from turning on, so their bulk nodes are not applicable in almost all cases, but in case of PMOS transistors it is not the same. Each PMOS device can be constructed in an individual n-well region so its bulk terminal is also an individual node and can be connected to desirable voltages.

In this paper with aid of the capacitors (C_1 - C_2) and their relevant charging devices (M_9 - M_{10}), voltage level at the bulks of PMOS devices, M_2 and M_4, is kept near VDD insuring the reverse bias of their drain-bulk diodes; also a floating state is established at these bulk nodes which are evaluation nodes of the circuit. The utilized capacitors, C_1 and C_2, are selected as 100fF.

The maximum error arisen for capacitors of this size is about 5% (± 2.5%), if their layout pattern is implemented accurately. With such an error, one of the inputs will have a higher influence, which introduces new offset source to the system; hence, the difference of the capacitors appears as offset voltage at the inputs of the comparator.

Applying the differential inputs alters the voltage level of the mentioned bulks against each other. According to (4), variations in the source-bulk voltage of a transistor directly affects its threshold voltage and consequently the corresponding inverters threshold. Thus the comparison is done by steering the threshold voltages in opposite directions.

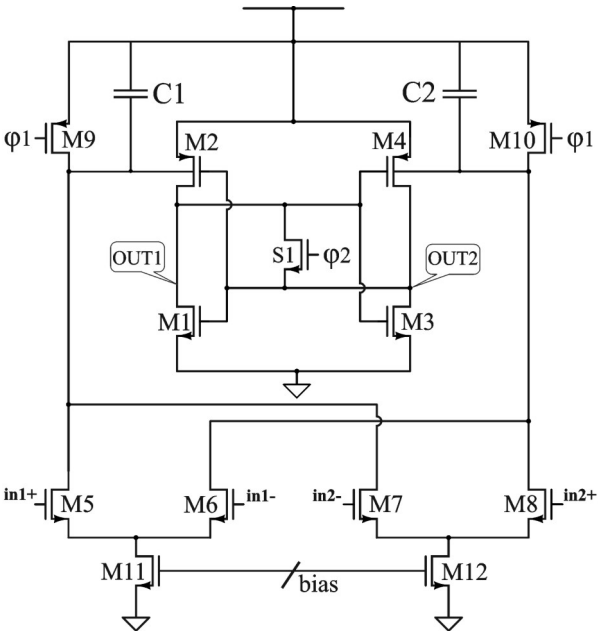

Figure 4: Proposed Low Kickback Noise Comparator.

$$V_{th} = V_{th0} + \gamma\left(\sqrt{\left(V_{SB} + V_{\phi}\right)} - \sqrt{V_{\phi}}\right) \quad (4)$$

Reset, evaluation and latch are three required phases which are performed consecutively in sequential one-stage comparators. This obligation affords delay to the process and limits the speed extremely. In the proposed structure, reset and evaluation sequences are performed simultaneously in separate nodes.

The digital controlling signals are illustrated in the timing diagram of Fig. 5. Reset phase starts at the rising edge of φ_2, concurrently as φ_1 goes low, the capacitors C1 and C2 are approximately charged up to the VDD level; at the rising edge of φ_1, evaluation occurs in the bulk terminals of M_2 and M_4. In pursuit of the output reset, the evaluated data affects the regenerative latch; up to the next rising edge of φ_2, the positive feedback has the opportunity for separating the output voltages. In other words, independence of the evaluation phase from reset and latch phases makes it possible to achieve both high speed and accuracy.

5 Readout Circuit

A simple readout circuit is utilized to hold the latched data. In absence of this circuit, the outputs of the comparator are set to a common mode voltage level after each reset phase and it lasts to reach the desired level once more. Implementing the readout circuit preserves the latched data of the regenerative nodes for one full clock cycle; in fact, it increases the validity period of

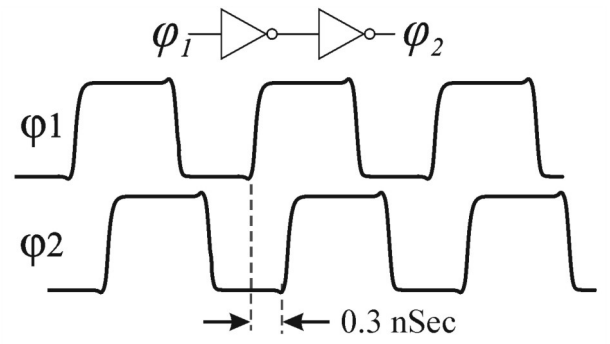

Figure 5: Timing Diagram for the Comparator of Fig.4.

the output signals. The discussed circuit is pictured in Fig. 6. It is made up of a data latch and a pair of NMOS devices. The outputs of the proposed comparators are applied to the gates of the NMOS devices; bit+ and bit- are the outputs of the readout circuit.

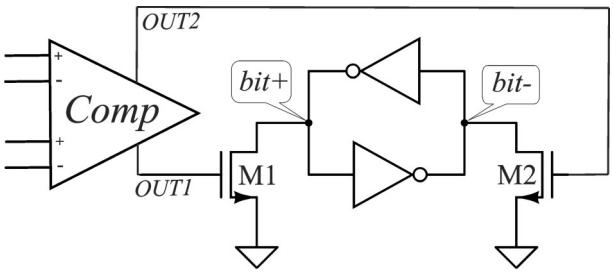

Figure 6: Conventional Readout Circuit.

Cascading the proposed comparator of Section 4 with the readout circuit of Fig. 6 introduces additional capacitance to the output nodes of the comparator hampering the comparison process. As a solution two inverters are implemented as interface between the comparator and the readout circuit. Aiming to reduce the input capacitance of interface circuit, the first inverter of each side has a different structure from the well-known static inverters. The NMOS devices of the first inverters at both sides of the interface circuit are connected to the comparator outputs but their PMOS side is drived by a delayed version of the RESET signal named W. The idea is pictured in Fig. 7.

Reviewing the function of this interface circuit for one side, at falling edge of W, the PMOS device M4 is turned ON for a short time period charging the node K+ and then goes OFF (pre-charge). If the output of the comparator is LOW, the NMOS device M3 will stay in cut-off region and cannot discharge the node K+ so it remains HIGH, but if the comparator output is HIGH, it makes the NMOS transistor to turn ON and discharge K+ (evaluation), hence the comparators output is inverted. K+ is inverted once more by a normal inverter producing the signal D+, this signal is then applied to the pro-

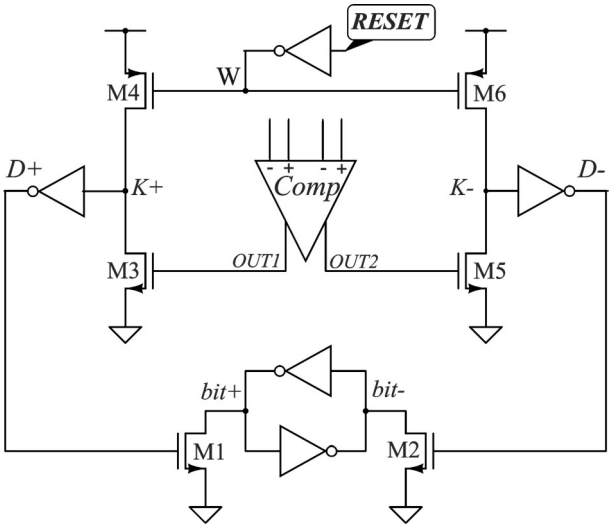

Figure 7: Proposed Readout Circuit.

posed readout circuit. Same story goes on for the next output of the comparator.

By this mean, only a minimum size NMOS device is connected to out1 and out2, so the additional capacitance is dramatically reduced insuring the correct comparison process.

6 Simulation Results

The main cores of the presented comparators beside the readout circuit of Fig. 7 are implemented in 0.35µm CMOS process. As illustrated in Fig. 8, an active area of 715µm^2 and 360µm^2 is occupied by the proposed comparators of Sections 3 and 4. In order to confirm the performance accuracy of the circuits in various terms, multiple simulations are performed in all process corners, using HSPICE (level49) with a standard 0.35µm CMOS process and the power supply of 3.3V. Aiming to generate a none-ideal power supply, some sinusoidal voltage sources are utilized in series with the VDD which leads to a noisy power supply. The simulation results indicate a 300mV p-p noise which is mounted on the VDD source.

In order to examine the capability of erasing the previously latched data, a challenging simulation known as worst case comparison is performed in which the input voltage alters from a large amplitude to a small value in the opposite direction and viceversa.

Precession of the operation is confirmed for both of the proposed structures. As illustrated in Fig. 9, the comparator of the Section 3 has the sufficiency of recognizing a 2mV differential input with 800MHz update rate. On the other hand, Fig. 10 confirms that a 1mV differential input at as high a clock frequency as 1GHz is simply sensible for the proposed comparator of Section 4. The measured power consumption of these two structures is 2.6mW and 1.6mW respectively.

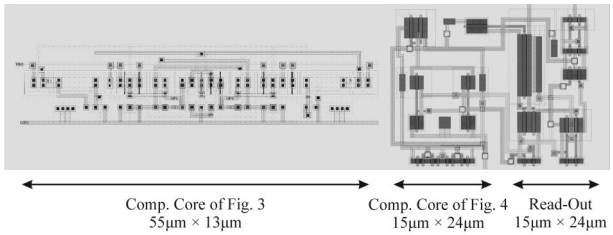

Figure 8: Layout of the Presented Comparators and Readout Circuit.

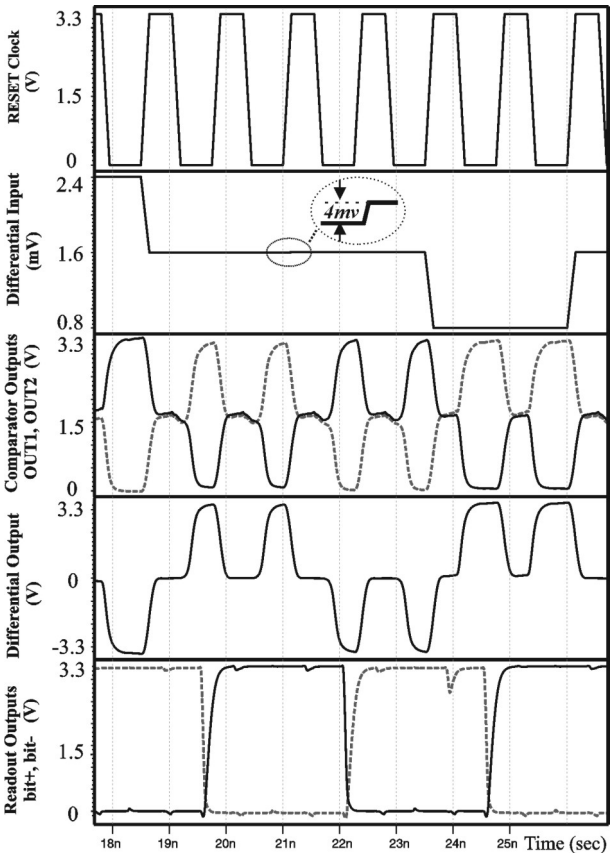

Figure 9: Simulation Results for Comparator of Fig. 3 Consisting the Reset Clock @ 800 MHz, Differential Input, Comparator Outputs, Differential Output and Outputs of the Readout Circuit.

In order to simulate the comparator of Fig. 4 with imbalance capacitors, C_1 and C_2 are selected as 97.5fF and 102.5fF (with ± 2.5% tolerance). A variable ramp source is applied to the comparator as offset voltage source. As depicted in Fig. 11, once the offset cancellation source (ramp voltage source) reaches around the 1.9mVolts, the tolerance of the capacitors is compensated and the improper operation of the comparator is corrected. The issue confirms that any mismatch in the

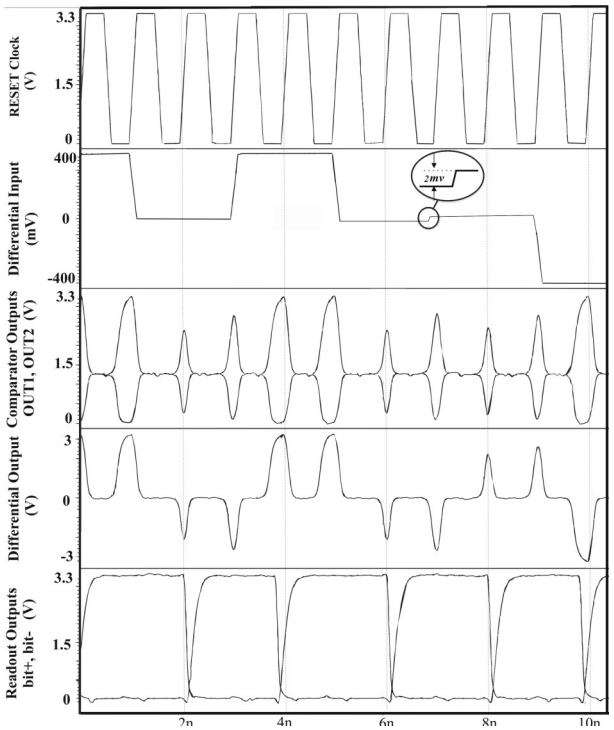

Figure 10: Simulation Results for Comparator of Fig. 4 Consisting the Reset Clock @ 1 GHz, Differential Input, Comparator Outputs, Differential Output and Outputs of the Readout Circuit.

capacitor values, appears as offset voltage at the inputs of the comparator, as well.

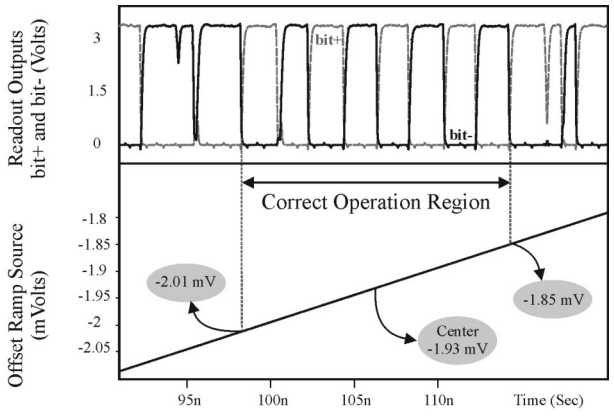

Figure 11: Correcting the Operation of the Comparator of Fig. 4 via a Variable Ramp Source Applied as Offset Voltage Source when C_1 and C_2 are Utilized with ± 2.5% Tolerance.

The originated voltage spikes of the regenerative latch are not able to impress the ideal input voltage source; hence, a resistor string of 10KΩ is used at each end which makes it possible to measure the kickback noise level. According to Fig. 12 and Fig. 13, the maximum amplitude observed is about 1mV and 0.6mV respectively for the comparators presented in Sections 3 and 4.

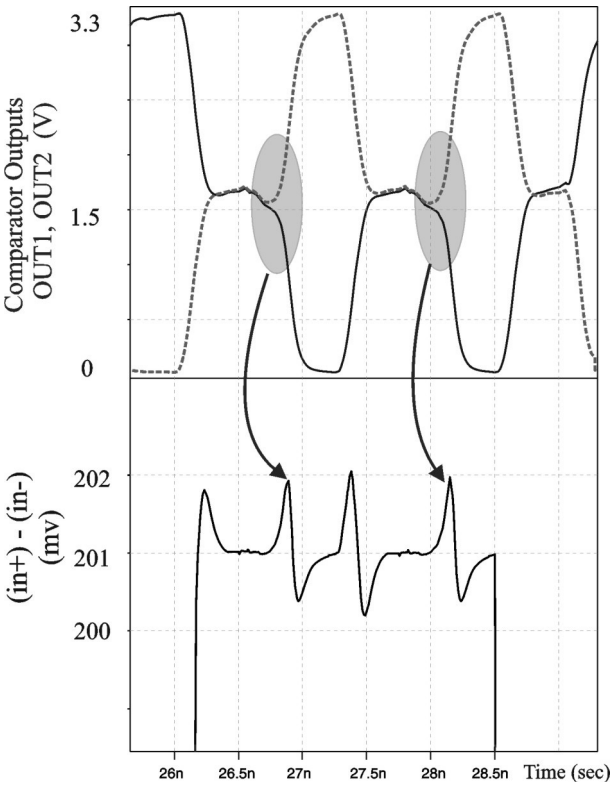

Figure 12: Kickback Noise Simulation for Comparator of Fig. 3.

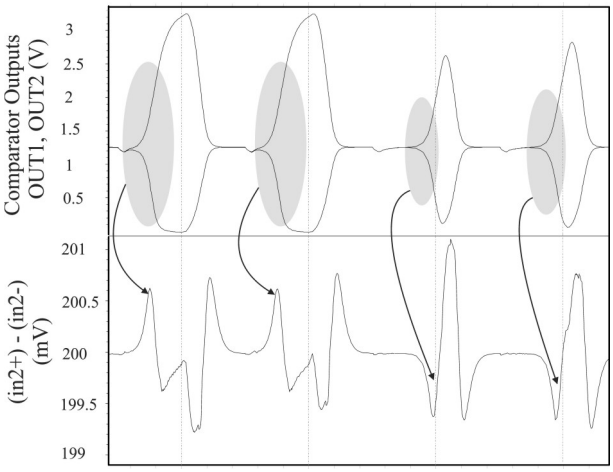

Figure 13: Kickback Noise Simulation for Comparator of Fig. 4.

7 Conclusion

A high performance comparator based on the preamplifier-latch topology was provided by improving the rail-to-rail folded cascode amplifier. Also a novel data reception style was utilized to engender a low-noise structure. Sufficiency of the comparators for high-speed, high-accuracy and low-power applications is confirmed by various simulation results. Table 1 sum-

marizes the performance of the proposed structures and Table 2 compares the proposed circuits with earlier presented similar works.

Table 1: Performance Summary

Process	Standard 0.35µm CMOS Process	
Supply Voltage	3.3Volts	
Power Supply Noise	300mVolts p-p	
Number of Stages	Single Stage	
	Improved High-Speed Comparator	Proposed Low Kickback Noise Comparator
Comparison Rate	800MHz	1GHz
Resolution	2mVolts	1mVolts
Kickback Noise Disturbance	1mVolts	0.6mVolts
Power Consumption	2.6mW	1.6mW
Area	55µm × 13µm	24µm × 15µm

Table 2: Comparison Table

	[1] (2011)	[4] (2010)	[10] (2012)	[11] (2014)	[12] (2011)	[13] (2013)	Proposed Comp. of Fig. 3	Proposed Comp. of Fig. 4
Process	0.35 µm	0.35 µm	45 nm	0.18 µm	0.18 µm	0.18 µm	0.35 µm	0.35 µm
No. Stages	1	1	3	1	1	2	1	1
Comparison Rate (GS/s)	1	0.5	20	2.4	0.5	1.25	0.8	1
Resolution (mV)	10	5	-	-	1	-	2	1
Power Consumption (mW)	1	0.6	0.561	329	0.6uW	0.274uW	2.6	1.6
Area (µm2)	250	300	-	392	-	-	715	360
Kickback Disturbance (mV)	0.4	11.5	-	43 - 13	-	-	1	0.6

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A Counter of Number of Products on the Shelf – Influences on Capacitance of Interdigitated Capacitor with Application in Intelligent Packaging

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Abstract: Products availability on the shelf, in the store, is a very important aspect in order to provide consumer satisfaction. Instead of conducting physical store audit, this paper demonstrates a counter of the exact number of the products on the shelf prototype realization. The complete test platform on Plexiglas has been developed. The proposed principle is based on interdigitated capacitor fabricated using ink-jet technology, where one set of silver electrodes is posted on the platform and another set on the boxes (products). When all products are on the test platform (or shelf) the capacitance has a maximum value. Taking products from the shelf this capacitance decreases and complete hardware solution has been made to transfer measured capacitance into number of products and to show this number on the display and turn on warning messages, if it is necessary. The proposed solution enables early detection of low number of products on the shelf and timely replenishment.
This paper studies performance of interdigitated capacitors printed with ink-jet printing technology on flexible substrate. Focus point of research presented in this paper is influences of different factors (number of capacitors connected in parallel, accurate position of electrodes of one capacitor, frequency range, etc.) on the capacitance of the structure. Main results are in the demonstration of capacitance change due to the influence of position between electrodes. Test platform, using this principle, has been made to demonstrate that it can be used as an effective solution for out-of-shelf problem.

Keywords: flexible substrate, ink-jet printing, intelligent packaging, interdigitated capacitor (IDC), silver ink.

Števec števila izdelkov na policah – Vplivi na kapacitivnost prepletenega kondenzatorja pri pametni embalaži

Izvleček: Za zadovoljstvo stranke je pomembna razpoložljivost izdelka v trgovini. Na mesto fizičnega štetja zaloge članek predstavlja prototipni števec izdelkov na polici. Razvita je bila celotna testna platform na pleksi steklu. Predlagan princip temelji na prepletenemu kondenzatorju v ink-jet tehnologiji, pri katerem je ena srebrna elektroda tiskana na polico, druga na embalažo izdelka. Ko so vsi izdelki na testni polici, je kapacitivnost največja. Ob umiku izdelka s police se kapacitivnost zniža. Izdelana je bila celotna strojna oprema, ki izmeri kapacitivnost, jo pretvori v število izdelkov in pokaže na ekranu. Po potrebi lahko vključi tudi opozorilna sporočila. Predlagana rešitev omogoča pravočasno detektiranje zmanjkovanja izdelkov in posledično njihovo dopolnitev.
Članek opisuje učinkovitost tiskanih kondenzatorjev na gibljivo osnovo. Raziskave se osredotočajo na več faktorjev: število kondenzatorjev vezanih vzporedno, natančno pozicioniranje elektrod, frekvenčno območje itd. Glavni rezultati prikazujejo spremembo kapacitivnosti glede na razdaljo med elektrodama. Testna platform demonstrira učinkovito uporabo pri štetju izdelkov na policah.

Ključne besede: gibljiva osnova, ink-jet tiskanje, pametna embalaža, prepleten kondenzator (IDC), srebrna pasta.

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1 Introduction

The problem of products missing from the shelf (or "out-of-shelf" problem) is still a frequent phenomenon in the grocery retail sector and can lead to lost sales and decreases consumer loyalty [1]. The term "out-of-shelf" (OOS) is used to describe situation where a customer does not find the product (or sufficient number of that product) one wishes to buy on the shelf of a supermarket. The reasons for the OOS are usually ordering problems and replenishing problems. Performing visual and manual inspection by store personnel is slow, expensive, and susceptible to human error. Because of that it is necessary to develop a precise product availability monitoring device or system.

Recently, some published papers suggested solutions of OOS problem through machine-learning technique [1] or classification methods [2, 3] in order to automatically identify products missing from the shelf. Apart from these approaches, there are some other technologies, which can provide product availability monitoring on retail shelves such as: radio frequency identification (RFID) [4, 5, 6], computer vision has developed powerful algorithms for pattern recognition [7], infrared sensors [8], weight-sensitive foam [9], etc.

Polymer or printed electronic is expected to be a promising technology for low-cost and large-area electronic components, circuits and systems [10]. Printed electronics industry has developed a number of processes and substrates materials to print devices at low cost [11]. This area of electronics enables easy processing possibilities with the opportunity to print inks on flexible substrates such as foils, papers, textile, etc. Interdigitated electrode (IDE) capacitors are one of the most used electronic components especially in sensors, transducers, filters, etc. Compared with parallel plates structure, the planar design of IDE is particularly suitable for manufacturing on plastic flexible substrate. Printed and polymer electronics can encourage new opportunities in the field of sensing and electronics. Humidity sensor, inkjet printed on flexible foil, based on interdigitated capacitors to allow ultra-low power consumption has already been reported [12]. Additionally, the same group was developed a differential capacitive sensors with integrated temperature sensor made on polyimide [13] or poly ethylene teraphthalate (PET) [14]. Furthermore, a humidity sensor that employs interdigitated capacitors printed with silver nanoparticle based ink on a flexible PET substrate was fabricated using gravure printing process [15]. Realization of flexible strain sensor that possesses micro scale thick interdigitated capacitors with no residual layer by a simple direct stamping with silver nanoparticles has been demonstrated in [16]. In the paper [17] has been investigated dependence of the capacitance of the interdigitated capacitor as a function of the electrode geometry and the bulk electrical properties of the substrate.

However, these systems were designed to inform personnel when the small number of the products is on the shelf (not exact number) and some of them require a robust installation on the shelves which increases integration costs or with small variation in capacitance (for example, around 50 fF in [18]). In all of these papers both sets of electrodes (fingers) of interdigitated capacitors are fabricated on the same substrate. In addition to this, analysis of influence of different position of fingers on total capacitance has not been performed, up to now.

This paper presents a complete demonstrator - a counter of explicit number of products on the shelf based on flexible/printed electronics. If the quantity of boxes (items on our platform or the shelf) is getting lower, our electronic system prototype informs employees in the store that product should be replenished, through very clear visual and voice messages. The system functionality could be extended by connecting more single product active shelf systems to the network with ability to inform an operator via network central node to take appropriate actions.

This paper also presents comprehensive analysis of influence of various positions of electrodes of interdigitated capacitor (IDC) on its capacitance. IDCs have been fabricated using silver ink on flexible Polyimide substrate, using inkjet technology. One set of electrodes was fabricated on one substrate and another set on the other substrate. In this way, it is possible to change position when one set is incorporated in fixed set of electrodes, as a basis. Consequently, different capacitance values can be achieved. Finally, application of this approach (a complete demonstrator) is presented - a counter of explicit number of products on the shelf based on flexible/printed electronics.

2 Design of interdigitated capacitor

Guideline for selection of dimensions of IDC were dimension of a standard pharmacologist box of children syrup, which are around 5.0 cm x 5.5 cm. Structures are designed in Microsoft Visio® program and exported in .bmp picture format with resolution 1016 dpi x 1016 dpi. Exact dimensions are visible in Figure 1 and they are given in millimetres.

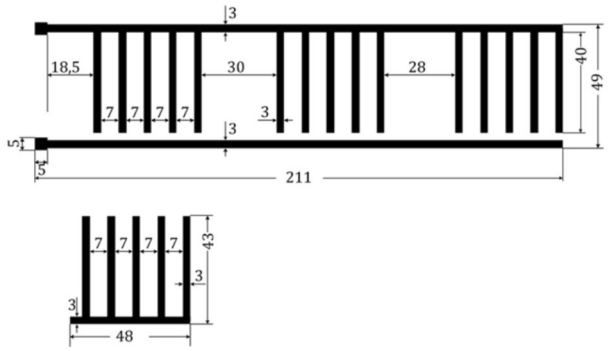

Figure 1: Design of IDC.

When both parts of interdigitated capacitor are in an ideal place (as shown in Figure 2), distance in vertical 10 line set is now 2 mm and gap distance is 3 mm.

Figure 2: Ideal position of electrodes shown for tree IDCs.

The conductive electrodes of the proposed structure of interdigitated capacitor were manufactured using Dimatix® DMP-3000 [18] cartridge based piezo ink jet printing system. Silver nanoparticle (with 20 % concentration) commercial ink (SunTronic® U5603) [19] was used as a conductive material to be printed on polyimide film substrate [20] with the thickness of 50 µm. DMP-3000 printing frequency was set on 4 kHz with nozzle voltage amplitude of 28 V, and drop space resolution of 25 µm. After printing, the structure was sintered in an oven up to 200 ºC for 45 minutes. The polyimide film was selected as a substrate due to its mechanical flexibility, chemical resistant properties and thermal stability. For easier handling one part of the IDC structure is stick to the Plexiglas board (further called fixed part) as shown in Figure 3. Figure 4 shows other electrode of IDC (further called mobile part) printed in the same technology and on the same substrate as the fixed part of IDC. Wires for terminals were glued on the platform with conductive epoxy silver paste and the whole structure was connected to an instrument HP4194A Impedance/Gain Phase Analyzer to conduct measurements. Structures presented in Figure 3 and Figure 4 have identical dimensions like dimensions already depicted in Figure 1.

Figure 5 shows SEM micrograph of the cross-sectional view of the sintered silver layer indicating homogenous structure with thickness approximately 500 nm.

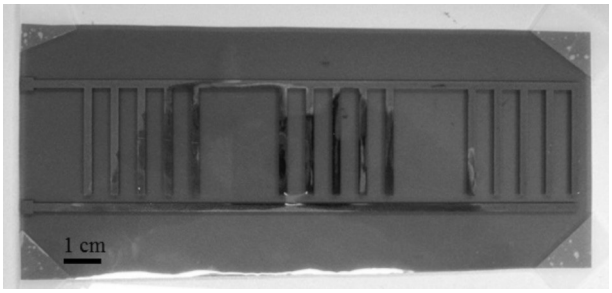

Figure 3: IDC fabricated on the Polyimide film using silver as a conductive material – set of tree half's connected in parallel (fixed part).

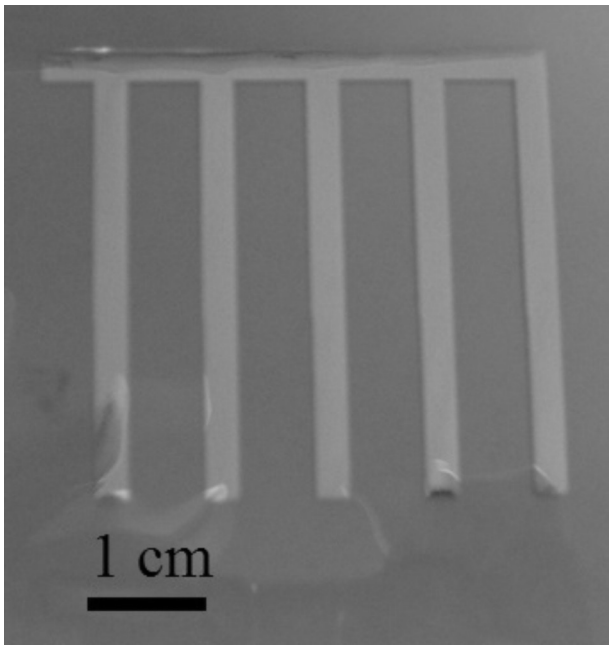

Figure 4: IDC fabricated on the Polyimide film using silver as a conductive material – second half of one IDC (mobile part).

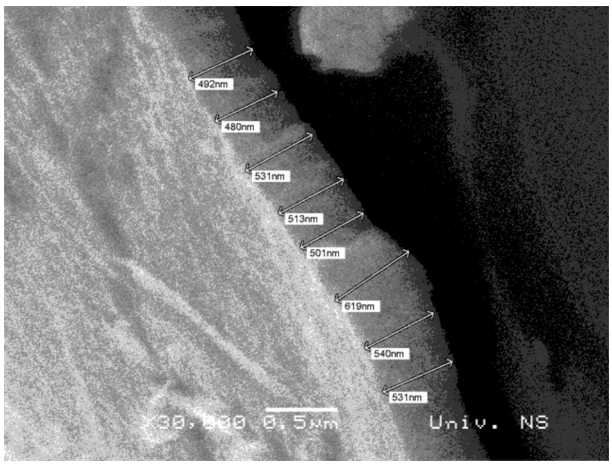

Figure 5: SEM micrograph of silver conductive layer.

3 Description of the electronic part of the system

There are several general approaches in capacitive sensors interfacing applications [21]. For measuring the IDC structure capacitance, a simple capacitance to voltage converter has been implemented. Some variations of this circuit can be found in literature as Mitchell's circuit [22]. It consists of three main blocks shown on the schematics in Figure 6.

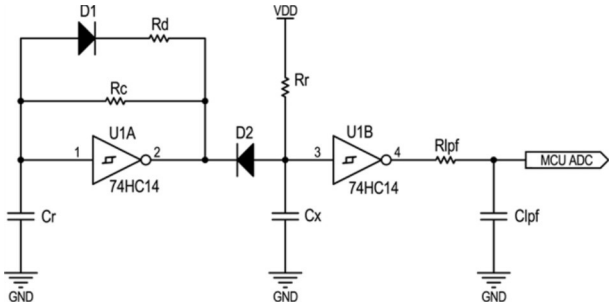

Figure 6: Developed capacitance measurement system schematics.

The implemented circuit can be described as a combination of an oscillator circuit and a charge-time measurement circuit. The first part of the circuit is used to generate appropriate charge/discharge interval using a relaxation oscillator with Schmitt inverter. The Schmitt inverter thresholds are fixed, so the duty cycle of the pulse-width modulation (PWM) on its output is determined by feedback resistors Rc and Rd. A diode at the output of the relaxation oscillator enables the unknown IDC structure capacitor (Cx) to be charged during the high output state of the relaxation oscillator (while the diode D2 is reverse biased). Analogously, during the low output state of relaxation oscillator (while the diode D2 is forward biased) discharging of the Cx capacitor is enabled. The actual values of the capacitor Cr and resistor Rr, which are used as a measurement range selecting components, depend on the desired range. The obvious restriction in the selection of Cr and Rr values is that the charging interval of the Cx capacitor through Rr resistor should be smaller than charging interval of Cr capacitor through Rc resistor, thus allowing the Cx capacitor to be fully charged. The second part of the circuit produces PWM signal at the output of the second Schmitt inverter with average voltage value proportional to unknown IDC structure capacitance. Finally, a passive first order low-pass filter was applied prior to connecting to the microcontroller analog-digital converter (ADC) port.

As a part of the system for measurement data acquisition, calculation and presentation, Atmel's AVR Butterfly microcontroller development kit was used. The AVR Butterfly board is equipped with a fast enough Atmel's ATmega169 low power 8-bit microcontroller as the main part of the system, a LCD, one ADC channel input port, two microcontroller ports connectors, a joystick, a piezo element, etc. The board comes with pre-programmed bootloader firmware allowing very easy microcontroller reprogramming via microcontroller's UART. The measurement data acquisition and presentation firmware was written in C. The main roles of firmware are measurement data acquisitions via microcontroller ADC1 (MCU PortF1) pin and data presentation. The Schmitt inverter thresholds lie within near linear part of capacitor's charge/discharge characteristic – between one and two thirds of the power supply voltage.

4 Building of the test platform

We have developed a prototype on a Plexiglas platform with dimension 45 cm × 20 cm × 10 cm, with 6 interdigitated capacitors (one electrode is on the Plexiglas and another is on the bottom side of the box) in 3 columns and 2 rows (Figure 7). Capacitors are connected in parallel so when the "shelf" in the store is full, the maximum capacitance is obtained and display shows the exact number of the products. In our case, the obtained capacitance was in the range from 20 pF (for six boxes) to 4.45 pF (for an empty shelf). If the quantity of boxes (items on our platform or the shelf) is getting lower, the electronic system prototype informs employees in the store that products should be restocked, through very clear visual and voice messages. The system functionality could be extended by connecting more single product active shelf systems to the network with ability to inform an operator via network central node to take appropriate actions.

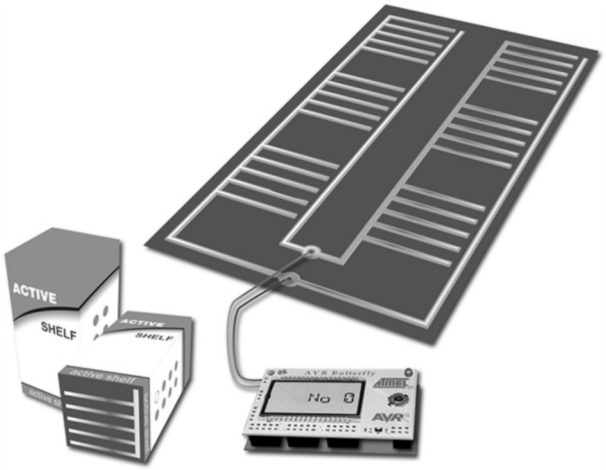

Figure 7: Application of IDC on intelligent packaging.

5 Results and discussion

Two types of influences on the capacitance of the fabricated IDC structure are analysed in this paper:

- Influence of number of capacitors in parallel on the total capacitance,
- Influence of accurate position of mobile part of IDC.
- Measurement of the two other characteristics was made (for an ideal position of the IDCs):
- Frequency dependence of capacitance and
- Values measured on the Atmel AVR ADC for different IDC capacitance values

Positioning of the structures for all cases of measurements is done under the microscope.

5.1 Influence of number of capacitors in parallel on the total capacitance

To demonstrate parallel connection of this type of capacitors and to determine their behaviour, three capacitors were designed. Capacitance of fixed structure exists because both contacts (square parts on the top of Figure 1) are on this part of IDC structure. Realization of complete capacitors occurs when mobile part makes the physical connection with thin line of fixed part (visible in Figure 8). This is the way we achieved free movement of mobile part.

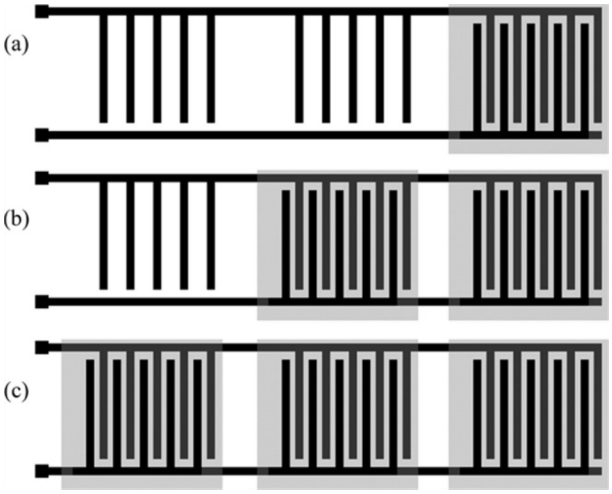

Figure 8: Changing the number of IDCs connected in parallel. (a) one capacitor, (b) two capacitor, (c) three capacitor

Table 1 demonstrates that capacitance rises almost linearly in steps in average of 5.7 pF per addition of one capacitor. Capacitance of fixed part shown in the top of Figure 1 is equal to 4.45 pF. Therefore, by adding mobile parts of capacitors overall capacitance rises in discrete values.

Table 1: Influence of number of capacitors in parallel on the total capacitance

No. of capacitors	Related Figure	Measured capacitance [pF]
0	Figure 1 (top)	4.45
1	Figure 8 (a)	10.19
2	Figure 8 (b)	15.94
3	Figure 8 (c)	21.52

Figure 8 gives an overview of increasing number of IDCs connected in parallel. Gray square marks correspond to Polyimide film of mobile electrodes. Black coloured parts resemble to visible electrodes (looking from the top), gray shadowed parts represents electrodes below the polyimide film.

Further measurement demonstrates that there is no connection between positions of capacitor and capacitance or order of setting and capacitance. Therefore, it is no mater of importance was the left, right or middle capacitor put first on the fixed part; result on full amount of capacitance is the same.

5.2 Influence of accurate position of mobile electrode.

Capacitance of IDC depends of the geometry of electrodes, material of electrodes, substrate and dielectric. In this sub-section, deviation of results of measured capacitance in the case of non-ideal positioning is discussed. The main reason for examination of these cases is a need for determination of differences in capacitance caused by relocation from an ideal position.

Figure 9 summarizes some extreme cases of relocations in four directions: up, down, left and right. This is maximum deviation in movement with which IDC is still working properly (that means that no short circuit is created).

Table 2: Changing position of one capacitor

No. of capacitors	Related Figure	Measured capacitance (pF)
1	Figure 9 (a)	11.94
1	Figure 9 (b)	12.35
1	Figure 9 (c)	12.38
1	Figure 9 (d)	10.68

Measurement results of this deviation are presented in Table 2 In consideration that one capacitor has the measured value of 10.19 pF in an ideal position, calculation evaluates that worst case scenario is when deviation is in up-right direction or in down-left direc-

tion. Hence, that capacitance of the capacitor is 12.35 or 12.38 pF. Thus, capacitance is increased for 2.19 pF maximum. From the results presented in Table 2, it can be concluded that capacitance value is higher in any case of deviation in movement in comparison with the capacitance of one IDC in an ideal position. This is a consequence of closer position of IDC fingers which has effect in increasing capacitance.

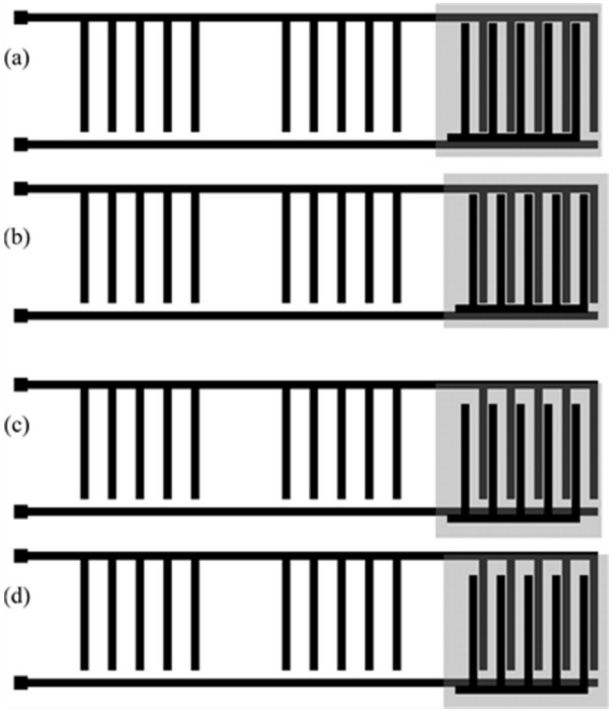

Figure 9: Preview of maximum deviations in movement in four directions (up-down and left-right). Displacement to the up-left corner (a); displacement to the up-right corner (b); displacement to the low-left corner (c) and displacement to the low-right corner (d).

5.3 Frequency dependence of capacitance

The measured results for capacitance as a function of frequency (on an instrument HP4194A Impedance/ Gain Phase Analyzer), for one row of IDC without boxes as well as with one, two or three boxes (this situation is shown in Figure 8) are presented in Figure 10. As can be seen, a very good agreement is achieved between measured and analytical values for capacitance of IDC structure, without boxes on it. It is also worth mentioning that proposed IDC structure can be used in a wide frequency range. Figure 10 reveals that self-resonant frequency is far above 40 MHz, which is the maximum frequency range for the instrument HP4194A. The existence of self resonance results in some increase of capacitance for high frequencies (above 15 MHz), which is characteristic for high values of capacitance (but from practical point of view the range around 20 kHz is of our interest). Contribution in total capacitance is higher with adding each new box, as can be seen from Figure 10, the difference between adjacent curves are higher with increasing number of boxes on the shelf. This is a consequence of lateral and additional fringing capacitances which are pronounced with more number of boxes on the shelf.

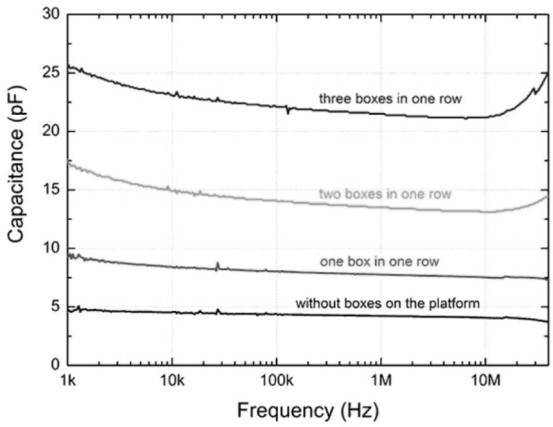

Figure 10: Measured capacitance as a function of frequency for different number of IDC structures formed

In the testing phase, measured values were taken at the circuit's charge/discharge frequency, around 20 kHz.

5.4 Values measured on the Atmel AVR ADC for different IDC capacitance values

Figure 11 shows the values measured at Atmel AVR ADC for different IDC capacitance values, along with its linear fit and adjusted coefficient of determination value of 0.99994. The capacitance meter range components values (Rr and Cr) are chosen to allow measurement in the whole range – around 5 pF for an empty shelf to near 40 pF for all six products on our test shelf platform. This wide capacitance values range is an important advantage of our solution comparing with similar solutions in literature [14]. It can provide a very good resolution and linearity. From the other side, dimensions of whole IDC structure in tens of centimetres range (including the length and width of conductive lines) has a consequence in slightly higher consumption of silver ink during ink-jet printing. However, it is planned that cost-effective cooper ink to be used in the next improvements of presented solution including also optimization of geometry of the IDC structure. Additionally, an important further step will be printing on the box directly, using Pulse Forge machine.

Furthermore, it can be noticed that the system has a small zero bias which is considered in software. Since the removal of the product from the shelf lowers down the equivalent IDC structure capacitance, when

measured capacitance is less than the previous for the amount of threshold (a least single IDC capacitance), firmware decreases the total amount of product on the shelf, and vice versa. For the correct functioning of this approach, it is assumed that initially there is a known quantity of products on the shelf (in the reality this is usually fulfilled).

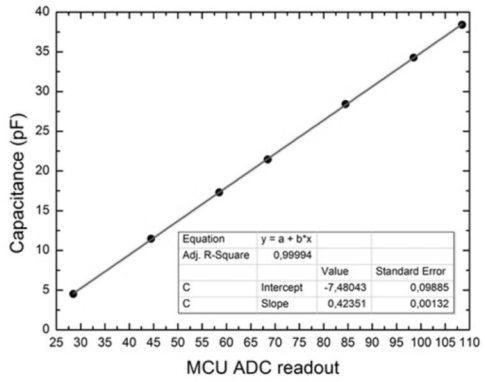

Figure 11: Microcontroller ADC measured values vs. IDC structure capacitances.

Between two successive capacitance readouts, firmware makes a decision upon above described scenario. If the equivalent capacitance is changed, firmware outputs the information of new quantity to the display (LCD) and informs the user of the new total number of products (Figure 12) on the shelf, by emulating the human speech. If the total number of products on the shelf is less or equal to the defined critical amount, system turns on the red LED and informs that the shelf should be replenished with products. Additionally, the text to speech system option is implemented by changing the PWM frequency on the pin connected to the AVR Butterfly piezo element and is implemented for words in English. Entered text strings are broken apart into syllables or phonemes, previously defined in program memory as an array of different PWM frequencies, which are then sent to the piezo element for appropriate syllable emulation. The proposed prototype can be supplied through a small AC/DC converter or using the battery of 9 V. The maximal current is around 20 mA, but in a normal operational mode this consumption is significantly lower.

6 Application

These examination of IDCs printed on flexible substrate are response of demands for smart or intelligent packaging. One of the problems in smart packaging is so called out-of-shelf (OOS) problem. This problem of products missing from the shelf is still a frequent phenomenon in the grocery retail sector and can lead to lost sales and decreases consumer loyalty [15]. The

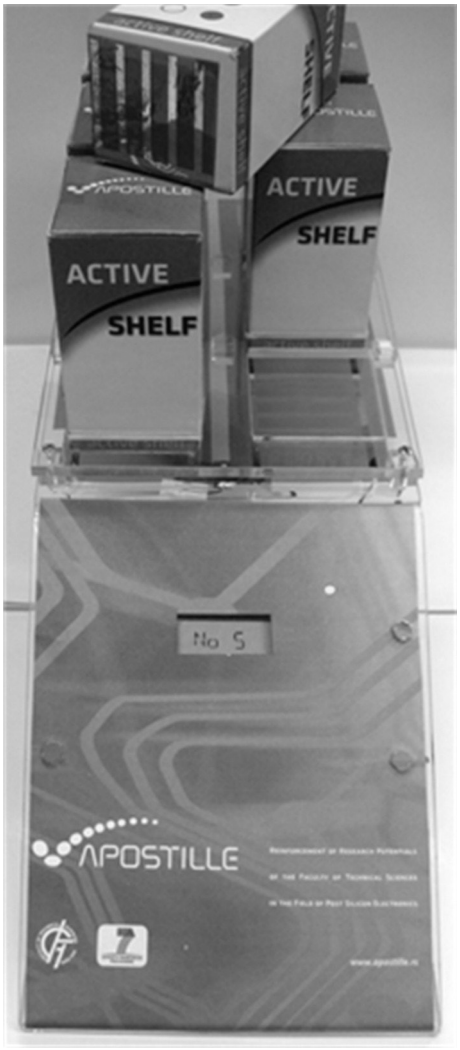

Figure 12: Developed platform of the counter of the number of products on the shelf.

term "out-of-shelf" is used to describe situation where a consumer does not find the product (or sufficient number of that product) one wishes to buy on the shelf of a supermarket, during a shopping tour. It might be that product exists in the store (back-room), but it is not on shelf. The reasons for the OOS are usually ordering problems and replenishing problems. Performing visual and manual inspection by store personnel is slow, expensive, and susceptible to human error. Because of that it is necessary to develop a precise product availability monitoring device or system. Consequently, based in previously described approach we have developed a complete solution, illustrated in Figure 12, intended to solve (or minimize) OOS problem. IDC is connected with AVR system with microcontroller and display for depicting the number of boxes posted on the platform (shelf). As can be seen from Figure 12, the second part of the interdigitated capacitor structure is posted on the bottom side of the boxes (the product in the reality).

Measurements showed almost no difference between capacitance when mobile part is free and when is fixed to the boxes. For this reason we believe that there are no obstacles which consider transition from free mobile part to mobile part fixed to product for further developing of this type of IDCs.

7 Conclusion

This paper has presented one solution for OOS problem. Existing solution is suitable for upgrades in area of wireless connection, advertising and so on.

This paper has presented a structure of interdigitated capacitor printed using ink-jet technology on flexible substrate. The proposed solution of interdigitated capacitor was printed on different substrates where on set of electrodes is fixed to the Plexiglas platform and another set of fingers free (or glued on the box or packaging). The silver electrodes of IDC have been fabricated on flexible Polyimide film by means of ink-jet printer (Dimatix DMP-3000). Mechanical flexibility of Polyimide substrate enables that proposed solution can have a wide range of applications. The total capacitance of IDC decreases with decreasing number of products on the shelf. Influences of: number of IDCs connected in parallel and position of electrodes were examined in detail. The complete electronic system for conversion of measured capacitance range to the number of products (presented on the display) has been developed. If the total number of products on the shelf is less or equal to the defined critical amount, system has visual and oral warnings that shelf should be replenished. The proposed system can accurately anticipate "out-of-shelf" situations and inform the store personnel before this situation occurs.

8 Acknowledgment

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Formation of thick SU-8 mold for the fabrication of UV-LIGA based nickel micro-gyroscope structures

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Abstract: SU-8 is a high contrast, epoxy based negative tone photoresist designed for MEMS and other microelectronic applications, where a thick, chemically and thermally stable image is desired. However, in practice, SU-8 is found to be very sensitive to process parameters variation. This paper reports an optimized process for creating thick SU-8 mold and its application in the fabrication of UV-LIGA based nickel micro-gyroscope structures. Initial experiments are carried out on 4 inch silicon wafers with two different micro-gyroscope structures, a 2-DOF linear micro-gyroscope having minimum feature size of 5 µm and a 4-DOF linear micro-gyroscope having minimum feature size of 3 µm. The patterned SU-8 is examined using scanning electron microscopy (SEM) and is found to be completely resolved having near vertical side walls. Finally, the micro-gyroscope structures are successfully fabricated using SU-8 based UV-LIGA process having 10 µm thick nickel as the key structural layer.

Keywords: SU-8, UV-LIGA, Nickel micro-gyroscope, Electroforming.

Tvorba debelega SU-8 ulitka za proizvodnjo strukture nikljevega mikro žiroskopa na osnovi UV-LIGA

Izvleček: SU-8 je visoko kontrasten negativni fotorezist na osnov epoksija za MEMS in ostale mikroelektronske aplikacije, kjer je potrebna debela in kemijsko in termično stabilna slika. Kakorkoli, SU-8 se je v praksi izkazal zelo občutljiv na spremembo procesnih parametrov. Članek predstavlja optimalen proces za izdelavo debele ulitka in njegovo uporabo pri izdelavi nikljevega mikro žiroskopa. Prvi poskusi so bili izvedeni na 4 inčni silicijevi rezini z dvema različnima strukturama mikro žiroskopa: 2-DOF linearen žiroskop z minimalno velikostjo 5 µm in 4-DOF linearen žiroskop z minimalno velikostjo 3 µm. SU-8 vzorec je bil pregledan s pomočjo elektronske mikroskopije (SEM), ki je pokazala popolnoma vertikalne stranske stene. Končno so bili žiroskopi uspešno izdelan na osnovi UV-LIGA z 10 µm ključno plastjo niklja.

Ključne besede: SU-8, UV-LIGA, nikljev mikro žiroskop, elektroformacija

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1 Introduction

UV-LIGA is an important technology that empowers economic mass production of micro-structures with high aspect ratios for MEMS applications /1/. The core difficulty with this technology is the use of UV or near-UV lithography to form thick micro-molds for electroforming /2/. One of the most employed photoresist for this purpose is SU-8 with properties of high viscosity and low optical absorptions in the near-UV range, which make it an ideal material for generating thick structures for electroforming /3/. However, as feature sizes get smaller and pattern complexity increases, particular difficulties; like planarization defects, film stress and solvent gradients, resist UV absorption, long development times, collapse of structures during rinsing; and a number of material related issues arise and need to be carefully considered /4/.

The micro-gyroscope structure has a perforated proof-mass, suspension system consisting of thin flexible beams which suspend the proof-mass above the substrate and comb-drives with narrow gap between the fingers for electrostatic actuation and capacitive sensing. Hence, the problems mentioned earlier are prominent in creating thick SU-8 mold for micro-gyroscope. Also, there is no published work on SU-8 processing specially for micro-gyroscope structures. In this paper, an optimized process for creating thick SU-8 mold for the fabrication of UV-LIGA based nickel micro-gyroscopes is reported. Two different micro-gyroscope structures are successfully fabricated using the given process.

The rest of the paper is organized as follows. Section 2 describes briefly the structures of proposed micro-gyroscopes. In section 3, lithographic processing of SU-8 and challenges faced are discussed. Section 4 illustrates the complete fabrication process of UV-LIGA based nickel micro-gyroscope and SEM images of fabricated structures.

2 Proposed micro-gyroscope structures

The fundamental operation principle of micro-gyroscope relies on the sinusoidal coriolis force induced due to the combination of vibration of a proof-mass and an orthogonal angular-rate input. The proof-mass is generally suspended above the substrate by a suspension system consisting of thin flexible beams. For exciting the micro-gyroscope, the most common actuation methods are electrostatic, piezoelectric, magnetic and thermal actuation. Most common coriolis response detection techniques include capacitive, piezoelectric, piezoresistive, optical, and magnetic detection. However, electrostatic actuation and capacitive detection are known to offer several benefits compared to other sensing and actuation means /5/. Comb-drives with narrow gap between the fingers are vastly used for electrostatic actuation and capacitive sensing in micro-gyroscope. For our study, we have taken two different micro-gyroscope structures, a 2-DOF linear micro-gyroscope and a 4-DOF linear micro-gyroscope.

Fig. 1 shows the conceptual schematic of proposed structure of 2-DOF linear micro-gyroscope /6/. The design is optimized to be compatible with UV-LIGA process having 10 µm thick nickel as the key structural layer. The device has a perforated proof-mass of 2.56 mm × 2.56 mm. The size of the perforation is 10 µm square with spacing of 10 µm. The width of each of the suspension beam is 6 µm. The gap between comb fingers is kept as 5 µm.

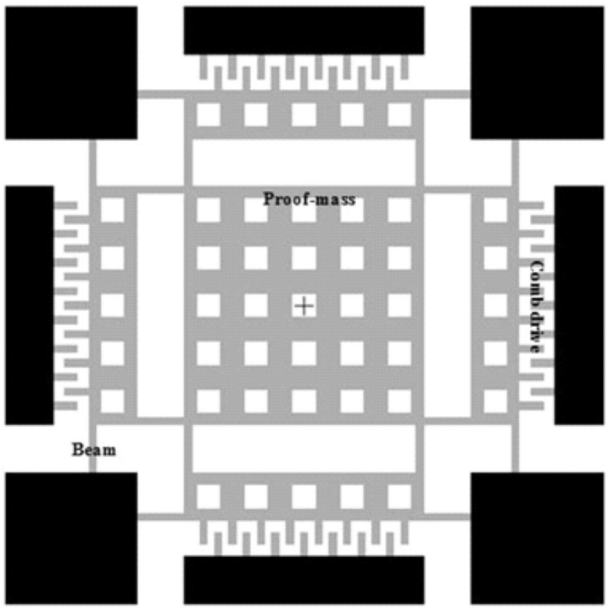

Figure 1: Conceptual schematic of proposed structure of 2-DOF linear micro-gyroscope

Fig. 2 shows the conceptual schematic of proposed 4-DOF linear micro-gyroscope /7/. The first mass m_1 and the combination of the second and third masses (m_2+m_3) form a 2-DOF drive mode oscillator. Whereas, m_2 and m_3 are free to oscillate independently in the sense direction, forming a 2-DOF sense mode oscillator. Mass m_f acts as the decoupling frame. The design is optimized to be compatible with UV-LIGA process having 10 µm thick nickel as the key structural layer. The device has a perforated proof-mass of 4.17 mm × 4.17 mm. The size of the perforation is 8 µm square with spacing of 10 µm. The width of each of the suspension beam is 5 µm. The gap between comb fingers is kept as 3 µm. It is evident from the schematic of Fig. 2 that the pattern complexity is increased in 4-DOF linear micro-gyroscope compared to 2-DOF linear micro-gyroscope.

3. Lithographic processing of SU-8

SU-8 is an acid-catalyzed negative tone photoresist. It is made by dissolving EPON®-SU-8 resin in an organic solvent such as cyclopentanone solvent or GBL (γ-butyrolactone) and adding a photoinitiator. The viscosity, and hence the range of thickness accessible, depends on the ratio of solvent to resin. The EPON resist is a multifunctional, highly branched epoxy derivative that contains bisphenol-A novolak glycidyl ether. On average, a single molecule consists of eight epoxy groups, which explains the "8" in the name SU-8 /8/. In a chemically amplified photoresist like SU-8, one photon produces a photoproduct that in turn causes hundreds of reactions to change the solubility of the film /9/.

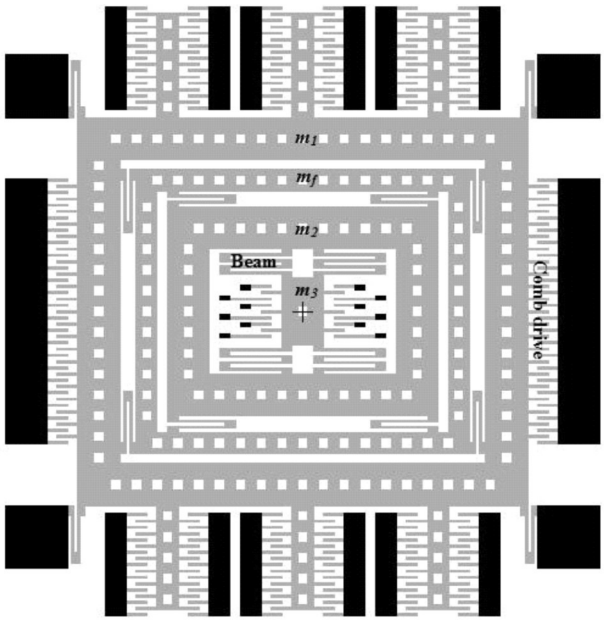

Figure 2: Conceptual schematic of proposed structure of 4-DOF linear micro-gyroscope

Initial experiments for SU-8 processing are carried out on 4 inch silicon wafers with a native oxide layer. Silicon wafers are cleaned by standard degreasing and piranha cleaning. After every cleaning the wafers are rinsed thoroughly in de-ionized water and are then blown dried with filtered compressed nitrogen gas. After that, the wafers are kept in a convection oven at 140 ºC for 30 min to remove any moisture on wafer surface. MCC's Omnicoat is then spin-coated onto the cleaned wafer at 3000 rpm for 30 s. It is recommended by MCC to apply Omnicoat for applications that require electroplating and subsequent removal of SU-8. It also acts as an adhesion promoter /10/. The coated wafers are baked in a convection oven at 140 ºC for 1 hour. After that, MCC's SU-8 2010 is spin-coated onto the wafer at 1500 rpm for 30 s. The wafers are then soft-baked at 65 ºC for 7 min and 95 ºC for 14 min in a convection oven. This step is required to remove the solvent and improve resist-substrate adhesion. However, baking temperature and time has to be selected properly. Higher soft-bake temperatures may initiate thermal cross-linking even if photoactivation has not taken place. On the other hand, lower soft-bake temperatures or shorter soft-bake time leave resist films with a high solvent content which will evaporate and therefore generate high film stress during post-exposure baking. The wafers are cooled down to room temperature after soft-baking. After that, the SU-8 is exposed to 365 nm UV light having an intensity of 30 mW/cm^2 with masks of 2-DOF linear micro-gyroscope and 4-DOF linear micro-gyroscope. We have used multiple exposure technique to achieve near vertical side walls. The exposure time is optimized as two exposures of 1.4 s each with wait time of 10 s between the exposures. Again, exposure time is one of the crucial parameter as overexposure will result in unresolved features and underexposure will result in peeling off of resist during the development step. The wafers are then kept in a convection oven at 65 ºC for 7 min and 95 ºC for 14 min for post-exposure baking. A post-exposure bake increases the cross linking degree in the exposed areas of SU-8 and stabilizes them against the action of solvents during the development step. At the end of the post-exposure bake, the wafers are cooled down to room temperature to release the residual stress. Development is performed by immersing the wafers in MCC's SU-8 developer at room temperature followed by rinsing in isopropanol. The development time is optimized as 50 s. Finally, the wafers are hard-baked at 140 ºC for 1 hour in a convection oven. The hard-baking of photoresist is essential to prevent seepage of plated material under the photoresist during electroforming.

The patterned SU-8 is examined using scanning electron microscopy (SEM). The SU-8 is coated with gold prior to SEM examination. The SEM images of SU-8 molds made for final micro-gyroscope structures are shown in Fig. 3 for 2-DOF linear micro-gyroscope and in Fig. 4 for 4-DOF linear micro-gyroscope. It is evident that pattern is completely resolved having near vertical side walls. The thickness of the mold is measured using surface profiler and it is found to be 11 µm.

4 Micro-gyroscope structure fabrication

The micro-gyroscope structures are fabricated using three mask UV-LIGA process described in Fig. 5. The process starts by growing 1 **µm** thick thermal oxide on 4 inch silicon wafer. Next, a 300/2000 Å thick Ti/Au metallization layer is sputtered and patterned to make contact pads. Again, a 300/2000 Å thick Ti/Au metallization layer is sputtered on the whole wafer surface to act as seed layer. After that, 11 **µm** thick resist MCC's SU8 2010 is patterned and 8 **µm** thick copper sacrificial layer is electroformed on the whole substrate surface except on the anchor regions which are protected by SU-8 resist. Copper is electroformed by using copper sulphate solution at room temperature and by applying optimized current density of 10 mA/cm^2. The rate of copper deposition at this current density is found to be 0.2 µm/min. The negative resist is then stripped from the substrate surface using MCC's Remover PG and CF_4+O_2 plasma chemistry leaving behind the electroformed copper sacrificial layer. Next, once again 11 **µm** thick negative resist SU8 2010 is spin coated and patterned using the key structural layer mask. A 10

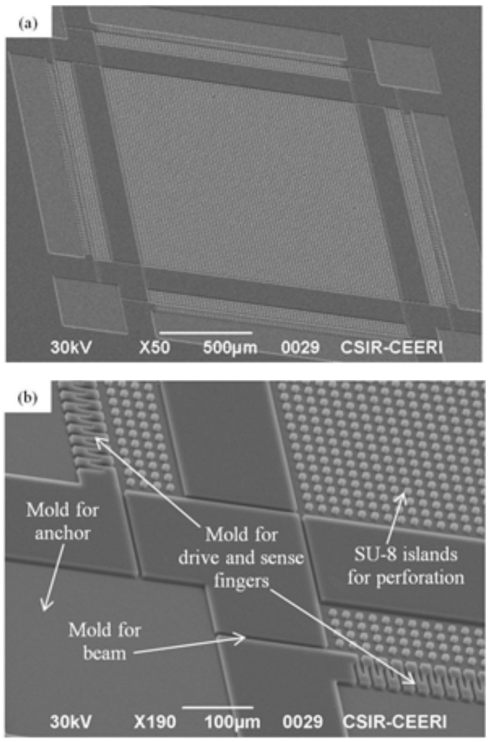

Figure 3: (a) SEM image of SU-8 mold for 2-DOF linear micro-gyroscope structure (b) Closer SEM image of SU-8 mold for anchor, beams, perforations, and fingers

µm thick Nickel is electroformed inside this thick resist mold. Nickel is electroformed by using nickel sulphamate solution at 48 °C and by applying optimized current density of 5 mA/cm^2. The rate of nickel deposition at this current density is found to be 0.067 µm/min. Thereafter, the negative resist is stripped using Remover PG and CF_4+O_2 plasma chemistry. The processed wafers are then diced using mechanical dicing saw. Finally, the copper sacrificial layer and seed layer are etched out selectively.

Fig. 6 shows the SEM images of fabricated 2-DOF linear nickel micro-gyroscope structure. For comparison, the images are taken at the same locations as in Fig. 3. It is clear from closer SEM image in Fig. 6(b) that structure is completely released, beams and other components have vertical side walls, and both drive and sense fingers including perforations in proof-mass are completely resolved.

Fig. 7 shows the SEM images of fabricated 4-DOF linear nickel micro-gyroscope structure. For comparison, the images are taken at the same locations as in Fig. 4. From the SEM image in Fig. 7(b), it is clear that the structure is completely released. Single U-turn and double U-turn beams are resolved with vertical side walls as is evident from Fig. 7(c) and Fig. 7(d). Besides, both drive fingers and sense split-fingers including perforations in proof-mass are also resolved as shown in Fig. 7(b) and Fig. 7(d).

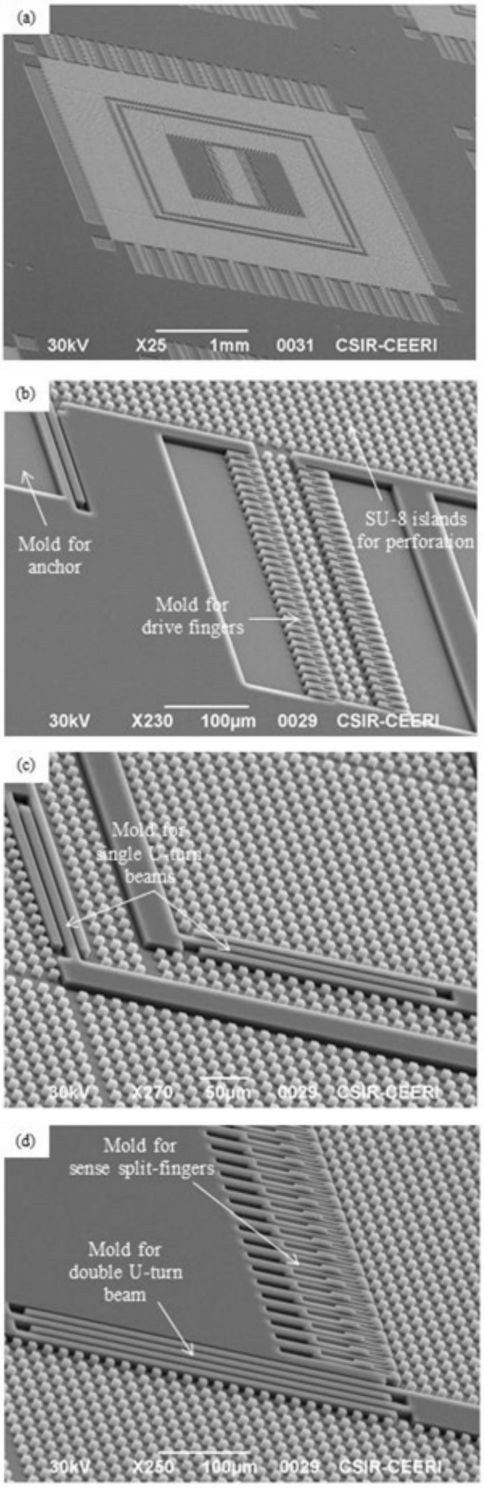

Figure 4: (a) SEM image of SU-8 mold for 4-DOF linear micro-gyroscope structure (b) Closer SEM image of SU-8 mold for anchor, perforations, and drive fingers (c) Closer SEM image of SU-8 mold for single U-turn beams (d) Closer SEM image of SU-8 mold for double U-turn beam and sense split-fingers

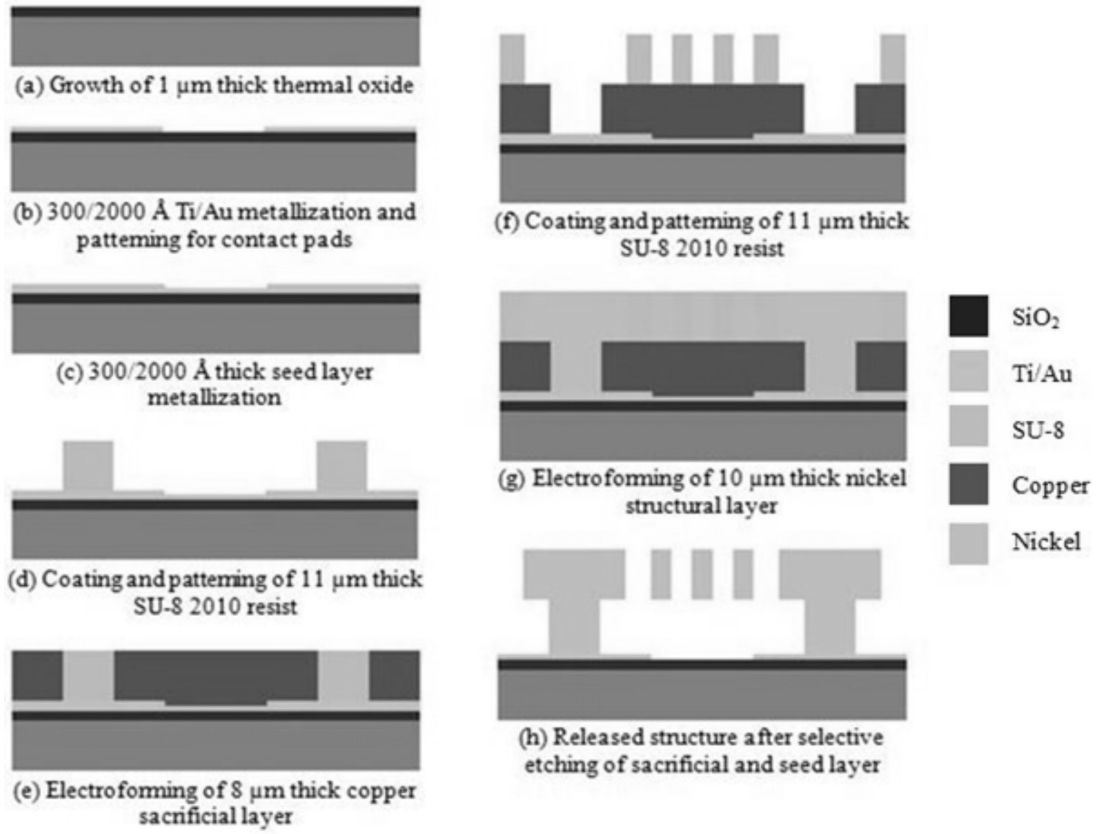

Figure 5: Fabrication steps in three mask UV-LIGA process

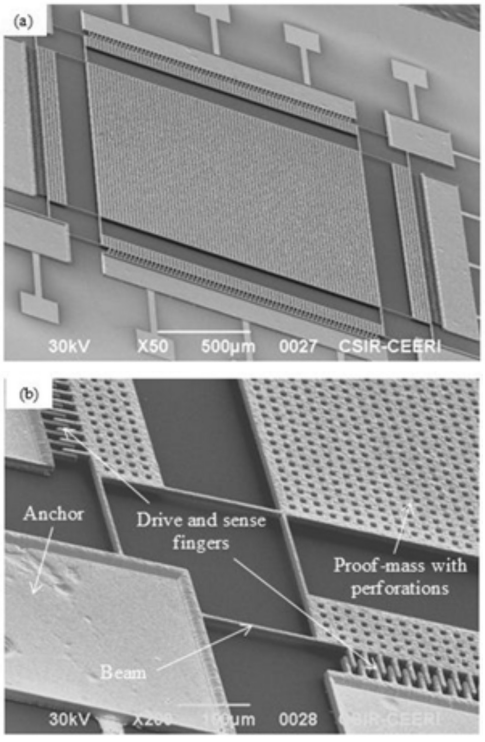

Figure 6: (a) SEM image of fabricated 2-DOF linear nickel micro-gyroscope structure (b) Closer SEM image of anchor, beams, perforations, and fingers of 2-DOF linear nickel micro-gyroscope

5 Conclusion

An optimized process for creating thick SU-8 mold and its application in the fabrication of UV-LIGA based micro-gyroscope structures is reported. Initial experiments are carried out on 4 inch silicon wafers with two different micro-gyroscope structures, a 2-DOF linear micro-gyroscope having minimum feature size of 5 µm and a 4-DOF linear micro-gyroscope having minimum feature size of 3 µm. The patterned SU-8 is examined using scanning electron microscopy (SEM) and is found to be completely resolved having near vertical side walls. Finally, the micro-gyroscope structures are successfully fabricated using SU-8 based UV-LIGA process having 10 µm thick nickel as the key structural layer.

Acknowledgements

This research work was supported by Council of Scientific and Industrial Research (CSIR) under 12th five year plan. The authors would like to thank following members of CSIR-CEERI: Dr. G Eranna and Mr. Ashok Kumar Gupta for providing excellent masks for fabrication; Dr. Jamil Akhtar and Mr. Arvind Kumar Singh for maintaining state-of-the-art gold sputtering facility; Dr. K J Rangra, Dr. Maninder Kaur and Mr. Prem Kumar for SEM

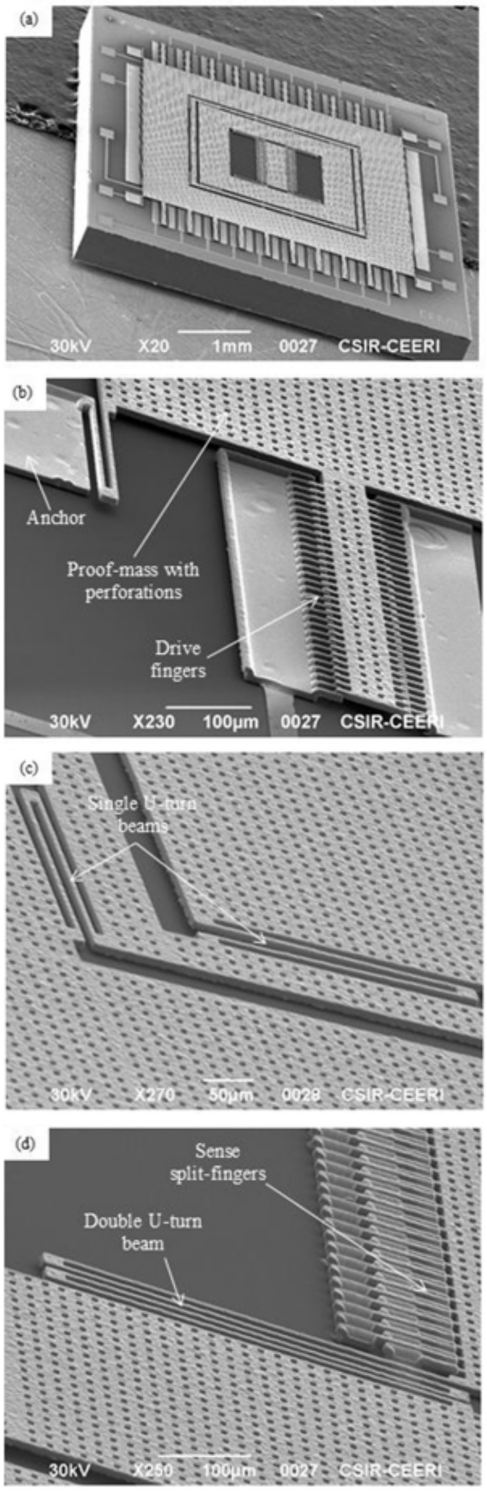

Figure 7: (a) SEM image of fabricated 4-DOF linear nickel micro-gyroscope structure (b) Closer SEM image of anchor, perforations, and drive fingers of 4-DOF linear nickel micro-gyroscope (c) Closer SEM image of single U-turn beams of 4-DOF linear nickel micro-gyroscope (d) Closer SEM image of double U-turn beams and sense split-fingers of 4-DOF linear nickel micro-gyroscope

facility; Ms. Subha Laxmi, Mr. Dhirendra Kumar and Mr. Supriyo Das for their help in fabrication.

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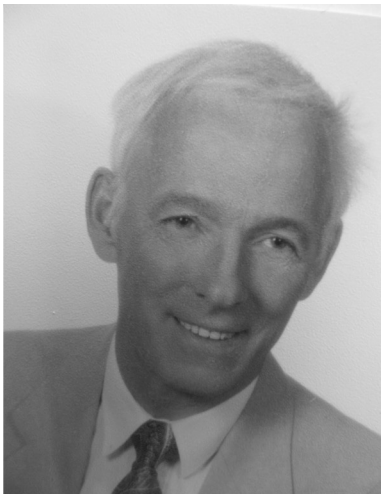
Osemdeset let zaslužnega profesorja Jožeta Furlana

Letos je praznoval osemdesetletnico prof. dr. Jože Furlan, upokojeni redni profesor na Fakulteti za elektrotehniko Univerze v Ljubljani (UL FE). Prof. Furlan velja med kolegi za enega od pionirjev na področju polprevodniških elementov, tranzistorskih in integriranih vezij ter fotovoltaike.



Prof. Furlan je bil rojen v Limbušu pri Mariboru. Že kot gimnazijski dijak se je zapisal področju elektrotehnike. Tako je že v svojih zgodnjih letih pridno obiskoval radioamaterske tečaje in sestavljal radijske sprejemnike ter na ta način prišel v prvi stik z elektroniko, ki se ji je nato zapisal za vse življenje.

Med leti 1952 in 1957 je študiral elektrotehniko na Oddelku za elektrotehniko Tehniške visoke šole v Ljubljani. Po diplomi se je leta 1958 zaposlil kot asistent pri prof.dr. Dušanu Lasiču na Oddelku za šibki tok Fakultete za elektrotehniko in strojništvo Univerze v Ljubljani. Prvo raziskovalno in pedagoško področje prof. Furlana so bile tedaj, v predtranzistorskem obdobju, še vedno zelo aktualne vakuumske elektronke. Pri tem delu je proučeval električna polja in gibanje elektronov v večelektrodnih elektronkah ter raziskoval šum v teh osnovnih elektronskih elementih.

Leta 1960 je bil z ameriško tehnično pomočjo na polletnem akademskem in raziskovalnem izpopolnjevanju v laboratoriju tedaj enega od vodilnih strokovnjakov na področju prihajajočih tranzistorjev, pri prof. Johnu Linvillu na Univerzi Stanford v ZDA, kjer je pridobival vrhunska znanja s področja polprevodniških elementov. Tako se je že v prvi polovici šestdesetih let kot eden prvih slovenskih elektronikov preusmeril od elektronk k tranzistorjem in od tod naprej na področje mikroelektronike. Sredi šestdesetih let je napisal tudi znano knjigo "Elektronika", v kateri je obravnaval nova tranzistorska vezja in jih primerjal z vezji na osnovi elektronk.

V letih 1969/70 je bil na izpopolnjevanju v enem od vodilnih razvojno-raziskovalnih laboratorijev na področju mikroelektronike, pri firmi Hewlett-Packard v ZDA, kjer je raziskoval tranzistorska integrirana vezja. Tu je pridobival najnovejša načrtovalska in tehnološka znanja na področju integriranih vezij. V tem obdobju je za firmo Hewlett-Packard razvil tudi dve zahtevni integrirani vezji za števni merilnik frekvence HP 5345A.

Po povratku v Ljubljano je prof. Furlan napisal prvi knjigi pri nas s področja mikroelektronskih tehnologij in elektronike integriranih vezij. Nato je do sredine sedemdesetih let intenzivno sodeloval pri raziskovalnem in pedagoškem delu v Laboratoriju za mikroelektroniko na Fakulteti za elektrotehniko UL, pri čemer so bile za uspešno delo izredno koristne njegove bogate izkušnje, pridobljene v Ameriki.

V naslednjem obdobju se je raziskovalno delo prof. Furlana usmerilo v študij osnovnih pojavov, lastnosti in aplikacij polprevodniških elementov ter tedaj še razmeroma novih sončnih celic iz monokristalnega in amorfnega silicija. Ustanovil in mnogo let je uspešno vodil Laboratorij za elektronske elemente na FE UL. Iz omenjenega laboratorija sta zaradi povečanega obsega raziskovalnega dela kasneje izšla dva uspešna laboratorija na UL FE, laboratorij LMSE (Laboratorij za mikrosenzorske strukture in elektroniko) in LPVO (Laboratorij za fotovoltaiko in optoelektroniko). Svoje bogate izkušnje je prof. Furlan prispeval v mnogih uspešnih raziskovalnih projektih, tako v povezavi z domačimi in mednarodnimi raziskovalnimi institucijami kot v sodelovanju z industrijskimi organizacijami.

Vsa leta aktivnega delovanja na Fakulteti za elektrotehniko je prof. Furlan tudi zelo zavzeto predaval mnoge predmete s področja elektronskih elementov, integriranih vezij in fotovoltaike. Napisal je večje število izvrstnih knjižnih del in učbenikov s področja elektronike, polprevodniških in drugih elektronskih elementov ter integriranih vezij. Na Fakulteti za elektrotehniko je predaval vrsto predmetov, od osnov elektronike do mikroelektronike, polprevodniških elementov in pasivnih elementov, optoelektronike, sončnih celic, teorije polprevodnikov ter teorije šumov. Predaval je predmete dodiplomskega in podiplomskega študija na Fakulteti za elektrotehniko in Fakulteti za naravoslovje in tehnologijo, UL. Imel je tudi predavanja za izredne študente v centrih Ljubljana, Kranj in Novo mesto.

Prof. Furlan je vsa leta zelo prizadevno, kot izjemno pozoren mentor, vodil tudi raziskovalno delo študentov in

mladih raziskovalcev podiplomskega in doktorskega študija. Rezultati opravljenih raziskav prof. Furlana, v sodelovanju z mlajšimi sodelavci in podiplomskimi študenti, so bili objavljeni v mnogih skupnih publikacijah, ki so izšle v številnih znanstvenih revijah in na konferencah doma in v tujini. Prof. Furlan je avtor ali soavtor številnih znanstvenih člankov v uglednih mednarodnih revijah ter recenziranih prispevkov v zbornikih specializiranih konferenc s področja polprevodnikov, integriranih vezij in fotovoltaike, o čemer priča tudi njegova izredno bogata bibliografija. Prof. Furlan je imel tudi vrsto vabljenih predavanj na uglednih univerzah v Evropi in v ZDA.

Na Fakulteti za elektrotehniko je prof. Furlan med drugim vrsto let vodil Oddelek za elektroniko in bil dolga leta predstojnik Katedre za elektroniko. Bil je tudi prodekan za pedagoško delo in predsednik komisije za podiplomski študij UL FE.

V začetku sedemdesetih let je bil prof. Furlan vodilni, ustanovitveni član Jugoslovanske sekcije mednarodne elektrotehniške organizacije IEEE ter več let njen predsednik. Mnogo let je bila Jugoslovanska sekcija IEEE edina iz skupine vzhodnoevropskih držav, kar je med drugim omogočilo njenim članom v tistih precej hermetičnih časih nemoten dostop do vrhunskih IEEE publikacij ter do raznih drugih članskih ugodnosti.

Za svoje bogato pionirsko, znanstveno-raziskovalno in pedagoško delovanje na področju polprevodnikov, mikroelektronike in fotovoltaike je prof. Furlan prejel številna priznanja in nagrade. Med prvimi učitelji na FE UL je prejel Vidmarjevo nagrado za odlično pedagoško delo. Za raziskave optoelektronskih lastnosti monokristalnega in amorfnega silicija je s sodelavci prejel nagrado Sklada Borisa Kidriča. Za pomembne dosežke v IEEE organizaciji je prejel IEEE Third Millenium Medal. Leta 1990 je za posebne zasluge in uspehe pri delu prejel Red dela z zlatim vencem. Leta 2000 mu je Univerza v Ljubljani podelila naziv zaslužnega profesorja.

Prof. Furlan je kljub formalni upokojitvi l.1999 še danes zelo aktiven in venomer išče odgovore na nova, nerešena vprašanja na področju polprevodniških elementov in fotovoltaike. V sodelovanju z mlajšimi raziskovalci še vedno z njemu lastno energijo, zavzetostjo in pronicljivostjo razčlenjuje in pojasnjuje nove pojave na omenjenih področjih, kar vodi do novih spoznanj ter do znanstvenih objav v mednarodnih publikacijah. Vsi njegovi sodelavci si želimo, da bi bil Joe, kot mu po domače pravimo, še dolgo tako ustvarjalen!

Ljubljana, Nov. 2014

Slavko Amon

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Speech of the MIDEM Society President at the Celebration Academy MIDEM-50

Govor predsednika MIDEM na Slavnostni akademiji MIDEM-50

Dear president of the Slovenian Academy of Sciences and Arts, Academician Professor Tadej Bajd, dear president of the Slovenian Academy of Engineering Professor Stane Pejovnik, dear ladies and gentelmen, dear friends!

This ceremony exceeds the celebration of 50 successful conferences on microelectronics, devices and materials. It exceeds the legacy of the MIDEM Society, which played an important role as an integrator of researchers and developers. We decided that this event should celebrate 50 years of successful research and develepment achievements of Slovenian Electronics academia and industry, as a great engineering heritage which Slovenia should be proud of. I believe pictures in the presentation that follows will speak for themselves, although the naration will be in Slovenian language. To celebrate Slovenian heritage please allow me to continue in slovenian language.

Spoštovani predsednik Slovenske akademije znanosti in umetnosti akad. prof. dr. Tadej Bajd, spoštovani predsednik Inženirske akademije Slovenije prof. dr. Stane Pejovnik, spoštovani visoki gostje, drage članice in člani društva MIDEM!

V veliko čast in ponos mi je, da lahko na današnji slovesnosti ob 50. mednarodni konferenci MIDEM spregovorim nekaj uvodnih besed.

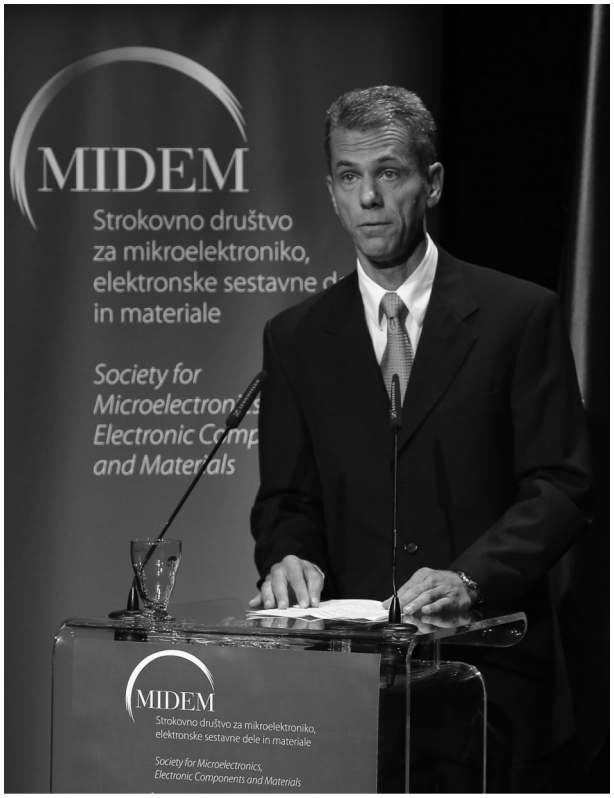
Z velikim veseljem ugotavljam, da je današnja Slavnostna akademija pravi odgovor na častitljivo zlato obletnico naše vsakoletne konference, katere tematska področja že dolgo presegajo področje mikroelektronike, elektronskih sestavnih delov in materialov. V zadnjem desetletju smo priča burnemu razcvetu nanotehnologij, nanoelektronike, na drugi strani pa makroelektronike s fotovoltaiko in optoelektroniko na čelu. Vedno bolj se uveljavlja fotonika, kompozitni in organskih polprevodniški materiali in z njimi novi izzivi, ki bodo v naslednjih desetletjih še bolj zaznamovali področja materialov, elementov, vezij, naprav in sistemov, ki jih v širšem strokovnem smislu naše društvo združuje.

Pred leti je IAS prodrla v medije z konceptom TEHNOLOŠKE AVTOCESTE, ki temelji na celoviti izgradnji infrastrukture in človeškega kapitala za tehnološki razvoj in za usmeritev v družbo znanja. Danes se osredotočamo na PAMETNO SPECIALIZACIJO, in izbiramo področja, kjer naj bi bila Slovenska pamet dosegala kritično maso, ki bi omogočala tehnološke preboje v čim tesnejšem sodelovanju razvojnikov v podjetjih in raziskovalcev na univerzah in institutih.
In kakšna je vloga strokovnih društev? Poleg dvosmernega sodelovanja akademske sfere z industrijo in obratno preko industrijskih projektov vidim strokovna društva v vlogi integratorjev in kot dopolnilni skupni imenovalec pri povezovanju v družbo znanja. Strokovna društva so

- kot krožišča na tehnološki avtocesti,
- kot netehnološka inovacija pri pametni specializaciji,
- kot stičišča človeškega kapitala v drugačni luči. V bolj prijazni, bolj človeški, bolj društveni.

Ocenjujem, da je društvu MIDEM od svoje ustanovitve, leta 1986, torej v minulih 28 letih to dobro uspevalo. Kot bomo lahko videli skozi mozaik raziskovalno razvojnih dosežkov, smo bili z vsakoletno konferenco uspešen integrator raziskovalcev iz akademske sfere in razvojnikov iz podjetij. Ni skrivnost, da se kakovost konferenc vrednoti po kvaliteti predavanj in kvaliteti neformalnega druženja, ki je pogosto bolj pomembno kot pa zgolj poročanje o doseženih rezultatih. Verjetno ste se tudi vi vprašali, ali je sploh možno, da smo imeli vsako leto konferenco in če smo jih res pravilno številčili. Za to se moramo ozreti nazaj in kaj hitro ugotovimo, da je pri konferencah o mikroelektroniki bilo kar nekaj lukenj. Po prvem posvetovanju o mikroelektroniki leta 1965 je bilo potrebno čakati 9 let na 2. posvet o mikroelektroniki. Je pa od leta 1965 potekal vsakoletno simpozij o elektronskih sestavnih delih in materialih z imenom SD. Društva MIDEM je že do osamosvojitve Slovenije v letu 1986 organiziralo oba letna dogodka.

Moja prva udeležba na konferenci MIDEM je bila leta 1992 v Portorožu. Takrat še pod imenom MIEL-SD kot skupek dveh ločenih dogodkov. V Gozdu Martuljku leta



1997 smo oba dogodka združili v enovit dogodek z novim imenom »konferenca MI-DE-M« in prevzeli številčenje konferenc SD (33. v letu 1997).

Da je društvo postalo to, kar je in na kar smo ponosni, pa so bistveno pripomogla vsa dosedanja vodstva, ki so uspešno krmarila v manj ali bolj burnih razmerah. Dr. Rudi Ročak kot prvi in dolgoletni predsednik, prof. dr. Marija Kosec in prof. dr. Slavko Amon. Pri organizaciji konferenc in urednikovanju zbornikov izrekam iskreno zahvalo za izjemno angažiranost dolgoletnemu podpredsedniku društva dr. Iztoku Šorliju, ki je soustvarjal serijo zadnjih 20 konferenc in zbornikov.

V izredno veselje in čast mi je izreči dobrodošlico akademiku prof. dr. Ninoslavu Stojadinoviću iz Srbije, ki se je prijazno odzval našemu povabilu. Kot eden privih podpredsednikov društva MIDEM in dolgoletni predsedujoči sestrske konference MIEL bo morda v svojem nagovoru opisal pričetke delovanja društva v sredini osemdesetih let.

V imenu društva se iskreno zahvaljujem Vam vsem, da ste si vzeli čas in nas počastili z vašo prisotnostjo na Slavnostni akademiji. Iskreno se zahvaljujem vsem članom in vsakemu posamezniku posebej, ki ste s svojimi idejami, dejanji in po svojih močeh prispevali v mozaik aktivnosti društva MIDEM. S ponosom ugotavljam, da je prehojena pot polna uspehov in lepih spominov.

Želim vam prijetno popotovanje skozi mozaik dosežkov in sedanjih aktivnosti slovenske elektronike, ki dokazujejo, da bomo tudi v prihodnje prispevali v družbo znanja na globalnem nivoju. Najlepša hvala!

Prof. dr. Marko Topič
Predsednik društva MIDEM

Ljubljana, 8. oktober 2014

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MIDEM 2015

51st INTERNATIONAL CONFERENCE ON MICROELECTRONICS, DEVICES AND MATERIALS WITH THE WORKSHOP ON TERAHERTZ AND MICROWAVE SYSTEMS

MIDEM

Announcement and Call for Papers

September 23th – 25th, 2015
Brdo pri Kranju (tbc), Slovenia

ORGANIZER: MIDEM Society - Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia

CONFERENCE SPONSORS: Slovenian Research Agency; IMAPS, Slovenian Chapter; IEEE, Slovenian Section; Zavod TC SEMTO.

GENERAL INFORMATION
The 51th International Conference on Microelectronics, Electronic Components and Devices with the Workshop on Terahertz and Microwave Systems continues a successful tradition of the annual international conferences organised by the MIDEM Society, the Society for Microelectronics, Electronic Components and Materials. The conference will be held at Brdo pri Kranju, Slovenia, well-known resort and conference centre, from **SEPTEMBER 23th – 25th, 2015**.

Topics of interest include but are not limited to:
- Novel monolithic and hybrid circuit processing techniques,
- New device and circuit design,
- Process and device modelling,
- Semiconductor physics,
- Sensors and actuators,
- Electromechanical devices, Microsystems and nanosystems,
- Nanoelectronics
- Optoelectronics,
- Photonics,
- Photovoltaic devices,
- New electronic materials and applications,
- Electronic materials science and technology,
- Materials characterization techniques,
- Reliability and failure analysis,
- Education in microelectronics, devices and materials.

ABSTRACT AND PAPER SUBMISSION:
Prospective authors are cordially invited to submit up to 1 page abstract before **May 1st, 2015**. Please, identify the contact author with complete mailing address, phone and fax numbers and e-mail address.
After notification of acceptance (**June 15th, 2015**), the authors are asked to prepare a full paper version of six pages maximum. Papers should be in black and white. Full paper deadline in PDF and DOC electronic format is: **August 31st, 2015.**

IMPORTANT DATES:
- Abstract deadline: **May 1st, 2015** (1 page abstract or full paper)
- Notification of acceptance: **June 15th, 2015**
- Deadline for final version of manuscript: **August 31st, 2015**

Invited and accepted papers will be published in the conference proceedings.

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http://www.midem-drustvo.si/ under Conferences.

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