A SUBSCRIBER LINE INTERFACE CIRCUIT (SLIC) IN A NEW 170V TECHNOLOGY

B. Zojer, R. Koban, R. Petschacher, W. Sereinig
SIEMENS Microelectronic Design Center, Villach

Keywords: electronic linecards, SLIC, Subscriber Line Interface circuits, HV-SLIC, high voltage SLIC, SPTtechnology, Smart Power Technology, SPT170 technology, IC, integrated circuits, internal ringing, output buffers, line current sensors, supply voltage switches, SLICOFI, Subscriber Line Interface and Codec Filter, BiCMOS, Bipolar CMOS circuits, DMOS, Double diffused MOS circuits, CO, electronic Central Offices

Abstract: The presented IC performs the high-voltage functions of an electronic central office subscriber line interface without the need for any transformers or relays. The challenges of SLIC integration stem from the combination of conflicting requirements: low impedance line feeding in a 150V range, current sensing with 0.2% relative accuracy and stability up to 200nF loads, while operating in the harsh environment of the telephone line. The newly developed BiCMOS/DMOS process SPT 170 and circuit techniques that strongly emphasize the physical device properties (e.g. buffers with DMOS outputs, n-type supply voltage switch, accuracy by polyresistors) yielded a very robust 30mm^2 SLIC. All transmission specifications are met without trimming.

Naročniški linijski vmesnik (SLIC) v novi 170V tehnologiji

Ključne besede: kartice linijske elektronske, SLIC vezje vmesniško linije naročniške, HV-SLIC vezje vmesniško linije naročniške visokonapetostno, SPT tehnologija močnostna inteligentna, SPT 170V tehnologija močnostna inteligentna, IC vezja integrirana, zvonenje telefonsko notranje, bufferji izhodni, senzorji toka linijskega, stikala napetosti napajalnih, SLICOFI vezje vmesniško linije naročniške in KODEK filter, BiCMOS CMOS vezja bipolarna, DMOS MOS vezja difundirana dvojno, centrale telefonske

Povzetek: Prikazano integrirano vezje ima visokonapetostne funkcije elektronskega centralnega naročniškega linijskega vmesnika brez uporabe transformatorjev ali relejev. Nasprotujoče zahteve, kot so nizko impedančno napajanje v območju 150V, tokovno zaznavanje z relativno točnostjo 0.2%, relativna točnost in stabilnost s kapacitivnimi bremeni do 200 nF ter delovanje v težavnem okolju telefonske linije so bili izziv za integracijo naročniškega linijskega vmesnika SLIC. Z novo razvito tehnologijo BiCMOS/DMOS SPT 170 ter z načrtovanjem, ki močno poudarja fizikalne lastnosti elementov (n.pr. izhodni krmilniki z DMOS tranzistorji, stikalo tipa n za napajalno napetost, točnost polsilicijevih uporov) je bil izdelan robusten naročniški linijski vmesnik (SLIC) na površini 30 mm^2.
Vse specifikacije prenosa so dosežene brez dodatnega doravnavanja.

Introduction

A complete two chip solution for the analog linecard has been realized, combining a high voltage SLIC with a complex mixed signal IC (SLICOFI) in 1µm - BiCMOS technology /1/. From the functional block diagram of fig.1 the main strategies concerning the system approach can be seen:

- the SLIC provides low impedance DC- and AC-feed of the telephone line; the resulting line current is sensed and fed back for impedance synthesis.
- both AC- and DC-control loops extensively utilize the benefits of digital signal processing (DSP), i. e. high flexibility due to fully programmabe characteristics (receive/transmit gain, impedance matching, trans-hybrid balancing, DC feed characteristics, supervision functions) without the need for external components.
- ringing signals as well as metering pulses (12/16 kHz signals with up to 5 Vrms) are generated on SLICOFI, and amplified and fed to the line by the SLIC
- the chip partitioning follows a simple economic guideline: as many functions as possible are shifted to the digital domain to save external parts, and as few as possible are realized on the high voltage part to save overall chip area.

These features bring about cost advantages in both new access networks and conventional central offices. In spite of its functional simplicity, however, the integration of a SLIC is a difficult task. First of all, driving the two-wire telephone line requires high voltages. Particularly in the ringing state most other electronic solutions disconnect the SLIC, and switch an external ring generator to the line by means of ring relays. A voltage capability of about 70 to 90V then is sufficient for DC line feed and voice signal transmission /2/. In contrast, our system offers internal ringing; however, taking into account a DC-voltage of about 20V for ring trip detection, a 150V supply is needed for exceeding 85V$_{rms}$ differential ("balanced") ring signals. On the other hand, the system's signal transmission specifications (longitudinal balance) demand analog circuits with 0.2% accuracy. Stability over a very wide load range and robustness against overvoltages, lightning surges and power shorts are further essential criterions.

Technology

The key issue is the selection of a proper technological concept. So we started an investigation to compare the possible approaches: dielectric versus junction isolation, bipolar versus BiCMOS. With lower cost than dielectric isolation and better performance than pure bipolar, our starting point has been a 75V Smart-Power-

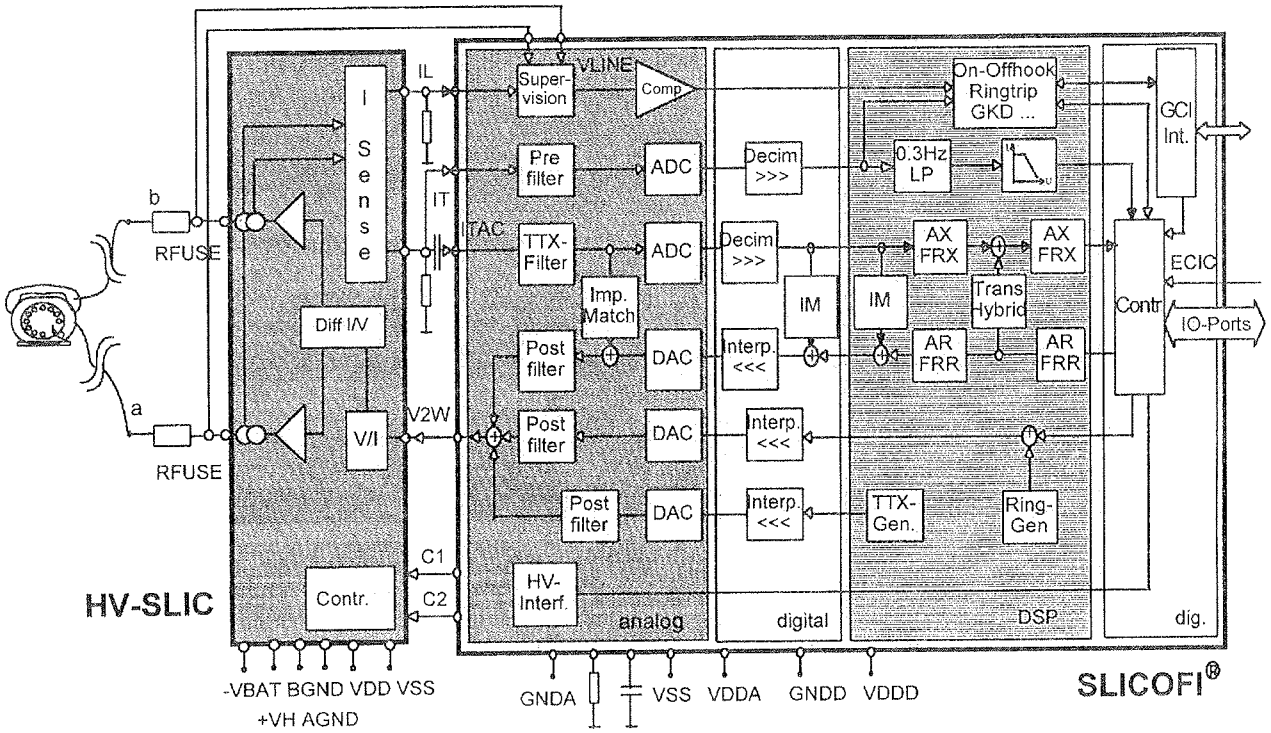

Fig. 1: System Block Diagram

BiCMOS process, SPT75 /3/, with a DMOS- and a lateral PMOS-transistor as the high-voltage (HV-)devices. This basic device concept, completed by high precision poly resistors, base layer resistors, MOS capacitors and Zener diodes, has been maintained in the new SPT170 process (table 1). To achieve the goal of breakdown voltages exceeding 170V, in a first step layer thicknesses and dopings had to be adjusted. Then device layouts had to be optimized with respect to breakdown: as the uppermost principle we regarded, that breakdown should never appear at the surface, but always in the silicon bulk, to significantly enhance destruction power and therefore robustness. Extensive numerical device simulations helped to adequately design surface topology and field plates.

As an example, fig. 2 shows the cross section of a DMOS transistor. The channel length of this high voltage device is defined by the difference in outdiffusion of n^+-source and p-bulk; this allows a relatively small channel of about 1.5 µm. A deep contact hole has to be etched through the source to connect the bulk. The potential distribution in the n^- drain region formed by a 19µm epi layer is essentially influenced by the shape of the poly silicon gate. An additional p^+ layer is introduced to enhance robustness; a well defined planar junction breakdown (bulk/drain) is forced to occur at a lower voltage than any destructive breakdown at the surface.

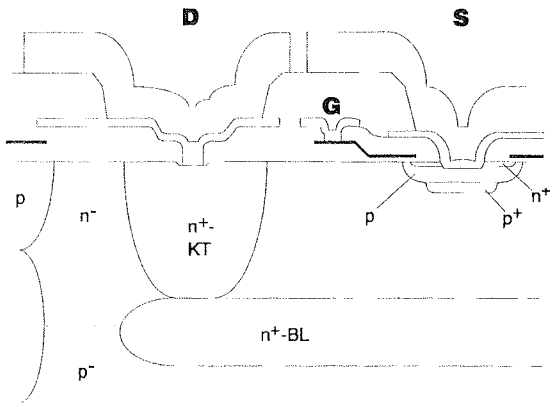

Fig. 2: Cross section of DMOS transistor

Table 1 Active devices in SPT170

		n	p	
	type	DMOS (cell-based)	lat. PMOS with p^- Drain-Extension	
	eff. gatelength	1.5	7.5	µm
	gate-oxide	80	80	nm
HV	max.	170	-170	V
V_{DS}		2	50	Ωmm^2
	spec. on-resist.	bulk	bulk	
	breakdown loc.			
	type	vert. npn	lat. pnp	
	β (0.1mA)	70	100	
	f_T	250	4	MHz
bipolar		70	-20/-100	V
V_{CE0}		110	<-100	V
	V_{CB0}			
	type	NMOS	PMOS	
	min. gatelength	5	6	µm
CMOS	gate-	80	80	nm
oxide		11	30	V
	max. V_{DS}			

Architecture

Fig. 3 gives a block diagram of the HV-SLIC. The main functions are feeding of the telephone line (DC and AC) and sensing of the transversal and lateral line currents. The input voltage V2W contains both the DC- and AC-information; it becomes amplified by 20, phase splitted and related to the internal "high voltage" supplies VBAT' and VH', respectively, to yield the line voltages Va and Vb. Two unity gain buffers then directly drive the TIP- and RING-wire.

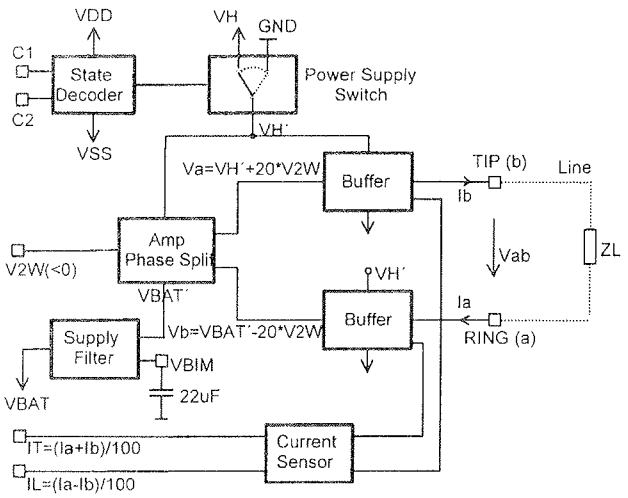

Fig. 3: HV-SLIC Block Diagram

While for normal conversation a single negative supply VBAT of typically -48 to -70V is sufficient (VH' = GND), the transmission of ring signals requires a switchable positive auxiliary voltage VH (up to +80V). These extended supplies are also useful for driving very long lines ("boosted battery" mode). Besides, a ±5V supply system VDD, VSS is available and utilized whenever possible to minimize power dissipation. The state decoder controls the various operating modes, including a "Power Denial" mode with bias currents totally switched off.

In order to achieve sufficient rejection from the power supplies to the signal voltage Vab (= Va - Vb), Vb must not be directly derived from the battery voltage VBAT, but from a filtered supply VBAT'. The g_m/C-type Supply Filter provides the required 40 dB suppression in the voiceband (300 to 3400 Hz).

The current sensor has to scale the line currents Ia and Ib by very precisely the same factor of 100 and to subsequently add and subtract the scaled currents yielding images of the transversal and longitudinal line current IT and IL, respectively. This allows separation of the transversal signals from longitudinal distortions.

Circuit Description

a) Buffer

Obviously, the buffer plays a key role as the actual interface to the telephone line. It must be able to both sink and source line currents up to 100mA, independent of the output voltage. The output voltage itself covers the whole supply range with only a few volts of allowed drop. Stability has to be assured for a very wide range of AC load impedances at any DC-current from zero to ±100mA. To achieve sufficient suppression of longitudinal signals, very low output resistances in the sub-Ω range have to be realized. Efficient current limiting and thermal protection is also required.

We closely investigated possible structures and soon rejected the more common solutions with complementary devices in the output stage, as the HV-devices of our process behave strongly unsymmetrical. So we chose the circuit concept of fig. 4 with its pure DMOS output stage. The combination of two 100-cell DMOS transistors - source follower D2 and common-source transistor D1 operated in a local feedback loop with opamp A - offers a simple solution to a key problem of class A/B amplifiers, the quiescent current control. This current through the output stage at zero line current is crucial for stability of the structure; here it is defined by I1 and the ratio of D2 and D3, as their source potentials are forced to be equal by means of opamp A. However, DMOS-matching is rather poor, so a part of the more critical quiescent current through D1 (~300µA) is determined by HVP2.

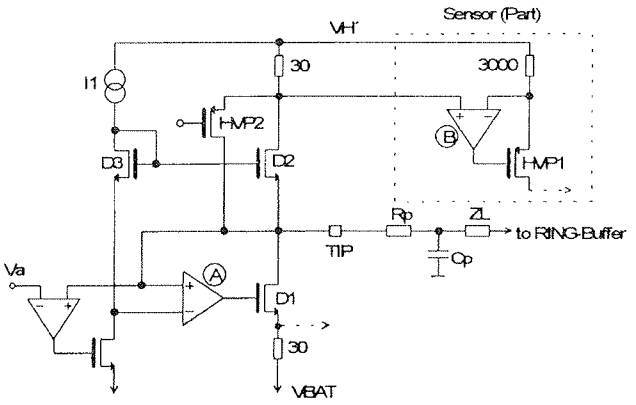

Fig. 4: Buffer Concept and 100:1 Sensor Current Mirror

The question remains, whether this structure can be stabilized for small external Rp (30Ω), protection capacitances Cp in the nF-range and arbitrary line impedance ZL. We succeeded with the structure of opamp A shown in fig. 5. It consists of a HVPMOS input pair, while all other stages (current mirrors, gain stage BN1/P1, emitter follower BN2) employs true BICMOS circuitry with low voltage transistors. An own internal supply voltage 10V above VBAT thus has to be realized using MOS diodes. Due to the large load capacitance, the common pole splitting compensation scheme fails. By returning CC to the emitter of BN3 rather than to the gate of D1, the additional gain of the loop CC, BN3, BN2 and D1 lowers the high frequency output resistance /4/. N4 is included to avoid saturation of BN3. A similar structure is used as the input amplifier. The whole buffer features a unity gain bandwidth of 1 MHz and is stable under all possible operating conditions, provided a minimum Rp and Cp of 30Ω and 100pF, respectively, are used.

Measured output resistances are below 1Ω with a sink/source mismatch below 0.1Ω in the voiceband.

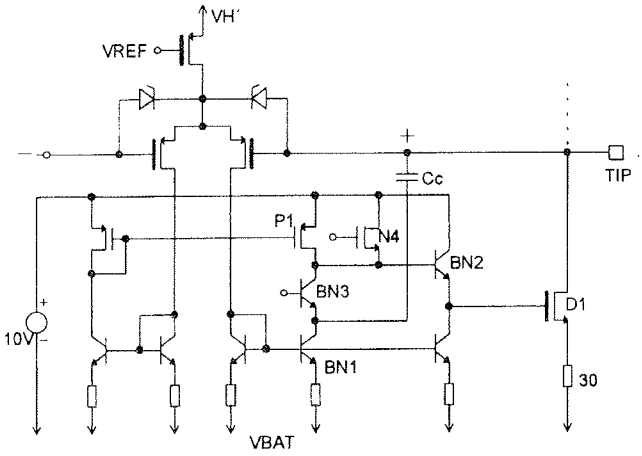

Fig. 5: Buffer Opamp

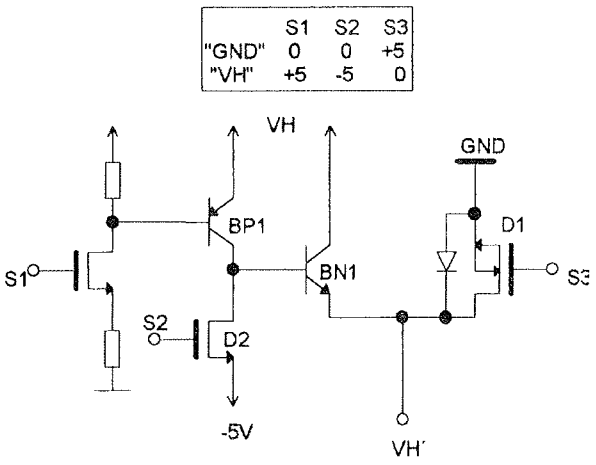

Fig. 6: Supply Voltage Switch

b) Sensor

The demands on longitudinal signal supression requires very accurate current sensing. We aimed to realize the 0.2% matching of the scaling factors without trimming. The only chance to achieve this is to let accuracy be determined by the best matching passive components available. So the sensor and most other accurate circuitry is composed of current mirrors similar to that in fig. 4 (30Ω, 3000Ω, HVP1 and opamp B). Here the current ratio is the inverse resistor ratio, provided that the opamp gain is high enough. The folded cascode structure with npn input stage and PMOS current sources we used, achieves a gain bandwidth product of 8MHz. This corresponds to a gain of several thousands in the voiceband, sufficient for the required overall accuracy.

After having investigated the electrical, mechanical and thermal behaviour of several resistor layers, a phospho-

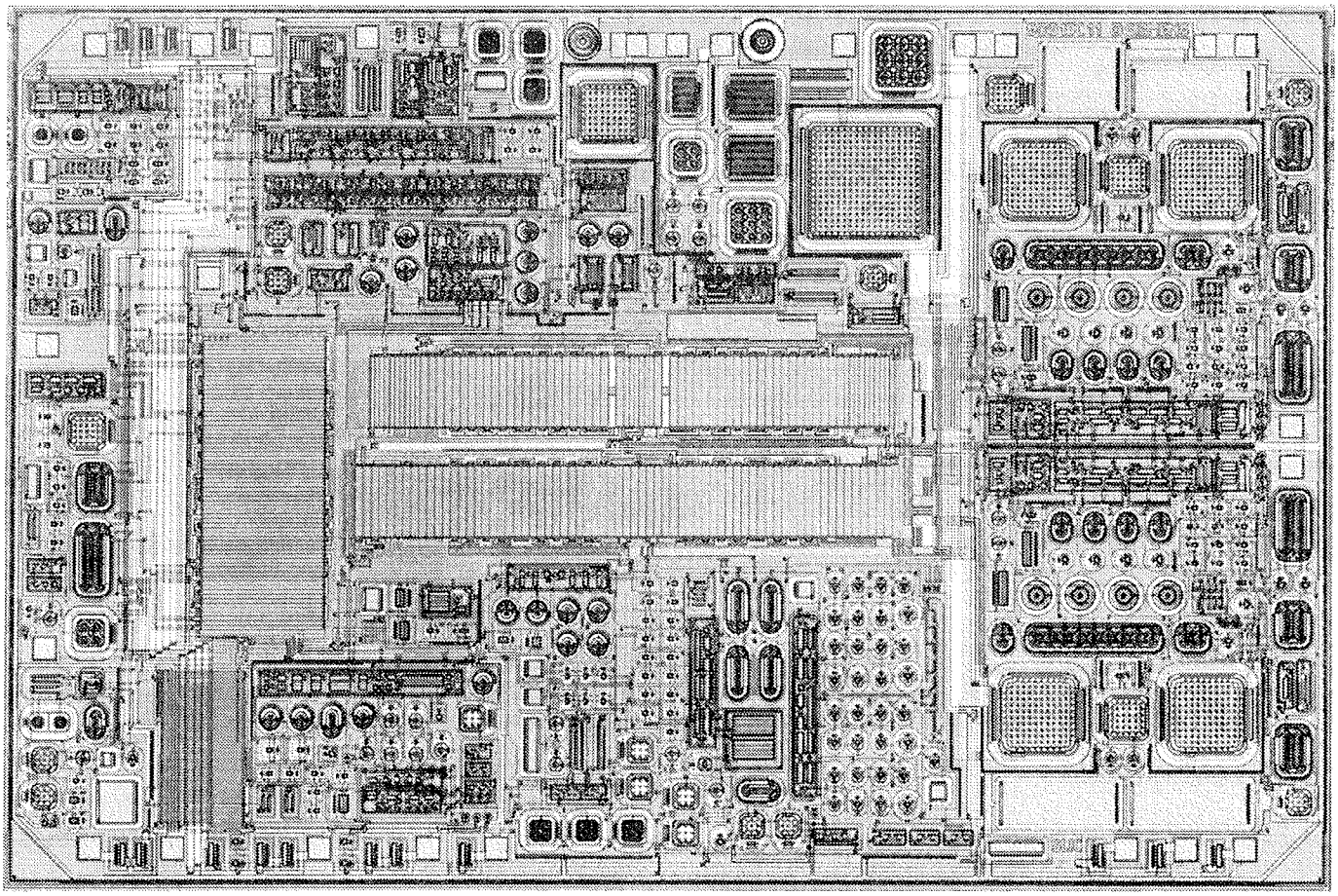

Fig. 7: Chip Microphotograph

rus-doped polysilicon layer of 300nm and 30Ω/square was the best selection; together with a proper resistor arrangement (the 30 and 3000Ω of fig. 4 are composed of identical 300Ω resistors in series or in parallel in a strictly alternating layout) for compensating on-chip temperature and stress gradients, all demands are fulfilled without trimming.

c) Power Supply Switch

A straightforward solution for the supply switch, a p-type transistor to VH and a high voltage diode to GND, has the severe disadvantage of high resistances due to the low doping levels. We once more searched for a pure n-type solution and found that of fig. 6. In position "VH" the operation is evident: npn BN1 forms a very low-resistive path to VH, BP1 delivers the base current; D2 as well as D1, the switching device to GND, are off. When D1 is switched on (S3 to +5V), it is operated inversely, i.e. with VDS 0. Because of the parasitic D/S-diode we must choose D1 large enough to ensure, that this diode will not become forward biased. With 300 cells, the maximum voltage drop is about 300 mV.

The problem remains, that in the SPT170 process VCE0 of BN1 is not sufficiently high to withstand VH. Our solution is to switch the base of BN1 to -5V via D2. Now breakdown of BN1 is governed by VCB, and this breakdown voltage lies beyond 100V.

Realization and Results

The HV-SLIC has been realized on a 6.6 x 4.4mm^2 chip. In the chip micrograph of fig. 7 the two buffers with their four output transistors on the right, beside the switch with its large DMOS, and the precision sensor resistors in the chip center are clearly recognizable. Approximately 1000 devices have been integrated and packaged into a newly developed surface mountable Power-DSO-20 package. The die is attached on a copper-slug for heat spreading purposes; additionally, a heat sink may be used that helps achieving a thermal resistance below 20 K/W (fig. 8).

Our SLIC fully met all transmission specifications in the first design step without any trimming. A typical problem of high-voltage ICs, the drift of parameters due to field induced moving of oxide charges, has been investigated carefully by extensive stress tests; the results indicate sufficient long term stability. None of the further notorious parasitc HV-effects like surface channelling or latch-up appeared, not even at an arbitrary switching sequence of the supply voltages, and the design proved itself to be very rugged against disturbances and transients at the line outputs, including lightning surges. This is mainly due to a consequent observance of some global strategies:

- breakdown always in the bulk, never at the surface to avoid destructive effects at low power
- closed poly guard rings around each device, properly biased, to ensure the absence of surface channels
- strict avoiding of substrate currents and saturation of bipolar transistors to minimize latch-up probability
- consideration and simulation of all kinds of possible distortions (lightning) to guarantee never to exceed destructive power densities

Table 2 is a summary of the most important SLIC characteristics. Meanwhile design and technology could prove themselves to be very well suited for reliable high volume production.

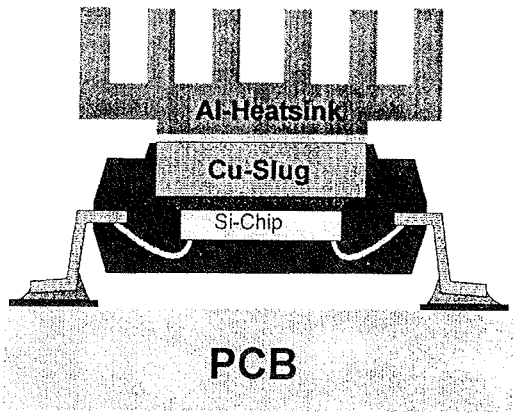

Fig. 8: Power DSO Package

Table 2 SLIC Characteristics

Max. Supply Voltage			150 V
Max. Output Current			100 mA
Power Dissipation	Convers.	(ILoad=0)	250 mW
	Ringing	(ILoad=0)	1300 mW
Gain Flatness (300 Hz.... 3.4 kHz)			0,01 dB
Longitudinal Rejection on		Vab	70 dB
		IT	90 dB
Psoph. Noise on Vab			-80 dBmp
Metering Signal Distortion (5Vrms, 16kHz)			0.02%
PSRR all supply volt. / Vab			> 40 dB
Max. Ringing Voltage			85 Vrms

References

/1/ R. Czetina, B. Astegher, L. Gazsi, T. Linder, H. Zojer, "SLICOFI, a New Approach to an Integrated One Chip Subscriber Line Interface and Codec Filter", Proc. ESSCIRC '94, pp. 136-140

/2/ R. J. Apfel et al, "A Subscriber Line Interface Circuit with an Internal Switching Regulator", Proc. ISSCC83

/3/ H. Zitta, Driver Circuit for an Automotive Smart Power System Chip", Informacije MIDEM 26 No.1, March 96

/4/ R. Castello, F. Lari, M. Siligoni, L. Tomasini, "100V High-Performance Amplifiers in BCD Technology for SLIC Applications", IEEE J. Solid State Circuits, Vol. 27, No. 9, Sept. 92, pp.1255-1263

B. Zojer, R. Koban, R. Petschacher, W. Sereinig
SIEMENS Microelectronic Design Center
Siemensstr. 2, A-9500 Villach
Tel.: +43 4242 305 0
Fax: +43 4242 305 223

Prispelo (Arrived): 21.02.1997 *Sprejeto (Accepted): 25.02.1997*