Oznaka poročila: ARRS-RPROJ-ZP-2011-1/116

ZAKLJUČNO POROČILO
O REZULTATIH RAZISKOVALNEGA PROJEKTA

A. PODATKI O RAZISKOVALNEM PROJEKTU

1. Osnovni podatki o raziskovalnem projektu

Šifra projekta	L2-9304
Naslov projekta	Integrirani sistem za zajemanje in merjenje senzorskih parametrov ter avtomatično kalibracijo merilnih sistemov
Vodja projekta	5648 Andrej Vodopivec
Tip projekta	L Aplikativni projekt
Obseg raziskovalnih ur	2.838
Cenovni razred	D
Trajanje projekta	07.2007 - 06.2010
Nosilna raziskovalna organizacija	2422 IDS integrirani in diskretni sistemi, d.o.o.
Raziskovalne organizacije - soizvajalke	796 Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko
Družbeno-ekonomski cilj	06. Industrijska proizvodnja in tehnologija

1.1. Družbeno-ekonomski cilj[1]

Šifra	06.
Naziv	Industrijska proizvodnja in tehnologija

2. Sofinancerji[2]

1.	Naziv	IDS Integrirani in diskretni sistemi d.o.o.
	Naslov	Sojerjeva 63, 1000 Ljubljana
2.	Naziv	
	Naslov	
3.	Naziv	
	Naslov	

B. REZULTATI IN DOSEŽKI RAZISKOVALNEGA PROJEKTA

3. Poročilo o realizaciji programa raziskovalnega projekta[3]

Razvili smo sistem za atomatično kalibracijo merilnih sistemov (Automatic Sensors' Signals Conditioning), ki so poznani v industriji kot dekodirniki, ki se uporabljajo v merilnih in orodnih strojih (CNC), torej za kontrolo pomika (motion control). Projekt je bil uspešno zaključen meseca junija 2010. Izdelan in integriran sistem predstavlja avtomatično – amplitudno, fazno in ničelno kalibracijo celotnega merilnega sistema, ki vključuje lastnosti zunanjih virov signala, lastnosti zunanjega krmilnika signalnih virov ter kalibracijo parametrov integriranega mikrosistema, ki zajema lastnosti integriranih senzorjev, lastnosti vmesnika med krmilnikom in signalnim virom in neidealne – procesno in temperaturno nestabilne lastnosti integriranih vhodnih ojačevalnikov (AFE). Avtomatično se torej – med normalnim delovanjem, brez kalibracijske faze – merijo parametri in zvezno doravnava celoten merilni sistem brez negativnih vplivov na normalno delovanje sistema. V letu 2009 smo koncentrirali raziskave in razvoj na preverjanje koncepta za vezje, ki naj med samim delovanjem kodirnika samodejno kalibrira merilni sistem glede na fazni premik. V letu zaključka projekta - 2010 smo koncentrirali raziskave in razvoj na merjenje in korekcijo fafe ortogonalnih signalov in delo uspešno zaključili na modelni osnovi. Koncept smo v celoti razvili in preizkusili s simulacijo ter z meritvijo prototipa. Ker na natančnost vpliva tudi hitrost spreminjanja frekvence znotraj kalibracijskega okna, smo v okviru analize proučili tudi vpliv nestabilnosti frekvence. Napravljena je bila tudi analiza najbolj neugodnega primera (Worst case analysis).
Merjenje in korekcijo amplitude, neodvisno od frekvence signalov smo izboljšali na osnovi bliskovne interpolacijske metode, ki smo jo patentirali (algoritem - priložena prva stran podeljenega patenta). Razvit sistem rešuje problem statično tako, da s priključitvijo štirih sinusnih napetostnih virov na simetrični uporovni mostič, zagotovimo monotonost pretvorbe in s tem robustnost in zagotovimo, da ni izgubljenih stanj do frekvence sinusnih signalov 200kHz. Statično delujejo vsi algoritmi, tudi merjenje in korekcija faze.
IZBOLJŠAVE NA RAZVOJU SoC SISTEMA v letu 2010:
Interpolacijski del je jedro A/D pretvornika, ki ga sestavljajo štiri enake uporovne verige Rv, povezane v simetrični uporovni mostič. Napetosti posameznih vhodnih kanalov CHA in CHB so priključene na mostič diagonalno-protifazno (A+, A-), kjer so signali zamaknjeni za 0 in za 180 kotnih stopinj in (B+, B-), kjer sta signala zamaknjena za 90 in za –90 kotnih stopinj v primerjavi s signali prvega kanala CHA. Celoten interpolacijski postopek z znanstvenim ozadjem in rezultati merjenja amplitude je opisan v prejšnjih poročilih in v članku, ki je bil sprejet v objavo v **BENTHAM SCIENCE**. Članek je v prilogi.
Merjenje in korekcijo fazne razlike smo optimirali glede integrabilnosti v letu 2009. in zaključili v letu 2010. Metoda deluje iterativno. V trenutku t=0 je fazna razlika Δfiin med signaloma CH1 in CH2 enaka Δfiout=Δfiin. Če je ta različna od nič (večja ali manjša), generira detektor fazne razlike digitalni signal UP oziroma DOWN. Signal UP/DOWN poveča oziroma zmanjša za 1 bit vsebino digitalnega števca. Izhod digitalnega števca se nato preko 8-bitnega D/A pretvornika pretvori v ustrezno analogno vrednost (Vdelay), ki povzroči zakasnitev kosinusnega signala in s tem zmanjša fazno razliko med CH1 in CH2. S tem je regulacijska zanka sklenjena oziroma končan je prvi cikel (več je v prilogi "APC_PRILOGA-zak-porocilo_2010.pdf").
Raziskovalna skupina v podjetju je v celoti raziskala in razvila sistem za ASSC ortogonalnih signalov ter uvedla sistem za optimalno avtomatično doravnavanje, in je v celoti integrabilen v tehnologiji CMOS. Sodelujoča raziskovalna inštitucija (**FERI v Mariboru**) je raziskala vrsto algoritmov za merjenje in korekcijo faznih razlik ortogonalnih signalov, prav tako neodvisno od frekvence signalov v zahtevanem območju hitrosti merjenj - brez prekinitve delovanja vezja. Integrabilni algoritmi za merjenje in korekcijo faznih razlik so v modelni fazi in v celoti preizkušen; ostali del ASSC je integriran v IDS-jevem prototipnem integriranem vezju EN400B, ki je glede hitrosti in ločljivoti trenutno najboljši integrirani mikrosistem z interpolatorjem na svetu, kjer smo uporabili izsledke raziskav tega programa. Nameravamo le še vgraditi optimiran PCA. Na področju merilnih dekodirnikov, ki uporabljajo sistem za merjenje na osnovi ortogonalnih signalov, je direktna implementacija merjenja in regulacije pri IDS sistemih novost. Takih sistemov ne uporabljajo konkurenčna podjetja (IC-haus, Heidenhain). Zato je podjetje tudi lahko dobilo evropski patent, čeprav je bil kot referenčni patent uporabljen patent podjetja Heidenhain, ki je patentiral svoj - celoten postopek regulacije parametrov vhodnih ortogonalnih signalov.
Seveda je potrebno povdariti, da je nujen nadaljni razvoj novih algoritmov, predvsem prilagajanje le teh na nove – nano-tehnologije in na vedno večje hitrosti merjenja rotacije in pozicije pri robotskih sistemih, pri orodnih strojih itd. Podjetje IDS bo le tako lahko sledilo trendom po vedno večji hitrosti, ločljivosti in prilagajanju na nove – nanosistemske senzorske strukture. Danes uspešno načrtujemo tovrstne integrirane sisteme ASIC v dekodirnikih, predvsem linearnih in rotacijskih magnetnih merilnikih za podjetje RLS d.o.o. iz Ljubljane.

4. Ocena stopnje realizacije zastavljenih raziskovalnih ciljev[4]

Raziskovalna skupina v podjetju IDS je v celoti raziskala in razvila sistem za ASSC ortogonalnih signalov ter uvedla sistem za optimalno avtomatično doravnavanje, in je v celoti integriran v tehnologiji CMOS. Sodelujoča raziskovalna inštitucija (**FERI** v Mariboru) je raziskala vrsto algoritmov za merjenje in korekcijo faznih razlik ortogonalnih signalov, prav tako neodvisno od frekvence signalov v zahtevanem območju hitrosti merjenj - brez prekinitve delovanja vezja. Merjenje in regulacija faze ortogonalnih signalov je bila zaključena v letu 2010, kjer smo zgradili modelno osnovo, s katero smo preizkusili integrabilnost in izbrali le tiste algoritme za fazno korekcijo PCA, ki integrabilnost zagotavljajo. Tako ima podjetje IDS pripravljeno infrastrukturo za vse bodoče aplikacije na področju dekodirnih naprav. IDS-ovo prototipno integrirano vezje EN400B je glede hitrosti in ločljivoti trenutno najboljši integrirani mikrosistem z interpolatorjem na svetu, kjer smo uporabili izsledke raziskav tega programa. Na področju merilnih dekodirnikov, ki uporabljajo sistem za merjenje na osnovi ortogonalnih signalov, je direktna implementacija merjenja in regulacije pri IDS sistemih novost. Takih sistemov ne uporabljajo konkurenčna podjetja (IC-haus, Heidenhain). Podjetje IDS je v letih 2008 do 2010 dogradilo algoritme, ki so bili objavljeni c SLO patentih in je bil v letu 2010 podeljen US in EU patent. Drugi patent s področja avtomatične regulacije je v PCT fazi v EU. Kot referenčni patent je bil uporabljen patent podjetja Heidenhain, ki je patentiral svoj - celoten postopek regulacije parametrov vhodnih ortogonalnih signalov. Seveda je potrebno povdariti, da je nujen nadaljni razvoj novih algoritmov, predvsem prilagajanje le teh na nove – nano-tehnologije in na vedno večje hitrosti merjenja rotacije in pozicije pri robotskih sistemih, pri orodnih strojih itd. Podjetje IDS bo le tako lahko sledilo trendom po vedno večji hitrosti, ločljivosti in prilagajanju na nove – nanosistemske senzorske strukture. Trenutno potekajo v podjetju IDS raziskave integrabilnosti algoritmov v nanometerskih tehnologijah CMOS (65nm). **Realizacija projekta je bila 100%, tudi zato, ker je podjetje IDS vlagalo vpreko 60% vseh sredstev v lasten razvoj v letih 2008 do 2010.**

5. Utemeljitev morebitnih sprememb programa raziskovalnega projekta oziroma sprememb, povečanja ali zmanjšanja sestave projektne skupine[5]

Sprememb cilja ni bilo.

6. Najpomembnejši znanstveni rezultati projektne skupine[6]

	Znanstveni rezultat		
1.	Naslov	*SLO*	Bliskovni interpolator z vgrajenim merilnikom amplitude
		ANG	A flash interpolator ASIC with build-in amplitude measurement circuit
	Opis	*SLO*	Opisano je bliskovno interpolacijsko vezje za pretvorbo analognih sinusnih in ortogonlnih signalov v množico prav tako sinusnih - fazno zamaklnjenih signalov, ki predstavljajo osnovno informacijo za nov algoritem merjenja amplitude. Merjenje je neodvino od frekvence signalov, interpolacijsko število 4 pa zadošča za preciznost merjenja 5.8%. Algoritem je podan in preizkušen v interpolacijskem vezju, ki je bilo procesirano v 0,35um tehnologiji CMOS
		ANG	A flash interpolation circuit converts a pair of periodic and orthogonal sine-signals into a stream of periodic – phase shifted sinusoidal signals, the amplitudes of which can be combined to produce useful information about the peak amplitude of the input sine-signals, independently of the signal's frequency. An interpolation factor of 4 is shown to be sufficient for measuring amplitudes with an accuracy of 5.8 %. The interpolator architecture has been designed, integrated, evaluated and analyzed. The ASIC is designed and processed in 0.35 µm CMOS technology.
	Objavljeno v		PLETERŠEK, Anton, BENKOVIČ, Roman. A flash interpolator ASIC with build-in amplitude measurement circuit, Inf. MIDEM, jun. 2010, letn. 40, št. 2, str. 107-114.
	Tipologija		1.01 Izvirni znanstveni članek
	COBISS.SI-ID		7987796
2.	Naslov	*SLO*	Modeliranje bralne glave optičnega enkoderja in meritev ultra majhnih kotov

		ANG	Optical encoder scanning head modelling and ultra small phase shift measurement
	Opis	*SLO*	Ena izmed nalog vezja za korekcijo vhodnega signala (signal conditioning module) je korekcija faze, ki odstopa od 90 stopinj. Za preverjanje učinkovitosti načrtovanja fazne korekcije, potrebujemo zelo natančno meritev faze, ki se izvaja na nivoju SPICE simulatorja. Izbrali smo meritev faze, ki temelji na meritvi prehoda obeh signalov skozi 0 V in poznavanju hitrosti. S to metodo lahko zasledujemo tudi časovno odvisnost faznega kota. Izvedena je analiza napake, ki nastane pri merjenju kota za neidealne, katerim se spreminja amplituda, frekvenca in enosmerni premik.
		ANG	One of the goals of the signal conditioning module is the elimination of the phase shift that differs from the 90 degrees. For the verification of the design effectiveness the precision phase shift measurement method on the SPICE level is needed. Our second goal was to measure the time-dependent ultra small phase shift in the circuit where the amplitude, frequency and DC offset were also varying with the time. The measurement algorithm should be implemented with the SPICE scripting language.
	Objavljeno v		DOGŠA, Tomaž, ŠALAMON, Matej, JARC, Bojan, SOLAR, Mitja, Inf. MIDEM, sep. 2009, letn. 39, št. 3, str. 162-167
	Tipologija		1.01 Izvirni znanstveni članek
	COBISS.SI-ID		7579988
3.	Naslov	*SLO*	Linearni optični dekodirnik s popačenjem sinusnih signalov pod-63 dB
		ANG	Linear optical encoder system with sinusoidal signal distortion below -60 dB
	Opis	*SLO*	Opisan je sklop, optična glava, ki je grajen kot sistem optičnih detektorjev tako, da omogoča povprečenje vzdolž merilne letve in ima vgrajen nonius sistem, ki dodaja k osnovni 10um periodi še mnogo večjo periodo (Moire efekt). Rezultat je zmanjšanje harmoničnih popačenj ortogonalnih sinusnih signalov pod -60db. Pozicijsko povprečenje pomaga skupaj z predlaganimi posegi v rotacijo indeksnih celic zmanjšati odstopanja amplitud in faznih razlik ter tako omogoči ASSC sistemu avtomatične regulacije parametrov boljšo ločljivost in točnost merjenje in regulacije v sklopu projekta L2-9304.
		ANG	A high precision linear optical scanner is described, combining an averaged optical sensors array with an appropriate 10 μm graduated scales on measurement – fix plate and Vernier sliced parallel scale on a reading plate, where the total distortion of the generated quadrature sinusoidal signals below -60 dB was achieved by distributing and mismatching optical edges over a number of sine wave periods within a number of Vernier scaled periods. All these helps to improve measurement and regulation precision within ASSC system, realized in L2-9304 applied project.
	Objavljeno v		ROZMAN, Jernej, PLETERŠEK, Anton. Linear optical encoder system with sinusoidal signal distortion below -60 dB. IEEE trans. instrum. meas., Jun. 2010, vol. 59, no. 6, str. 1544-1549, ilustr., doi: 10.1109/TIM.2009.2027774.
	Tipologija		1.01 Izvirni znanstveni članek
	COBISS.SI-ID		7747924
4.	Naslov	*SLO*	Metoda interpolacije in frekvenčno neodvisno merjenje amplitude pravokotnih - periodičnih signalov.
		ANG	Interpolation Method and Frequency Independent Peak Amplitude Measurement of Orthogonal – Periodic Signals
	Opis	*SLO*	Opisana je bliskovna interpolacijska metoda z vgrajenim merilnikom amplitude periodičnih in ortogonalnih signalov, ki je inherenten v sistemu in omogoča merjenje s točnostjo 5,5%. To zadošča za večini aplikacij dekodirnikov. Merilni sistem je neodvisen od frekvence delovanja. Izvajanje algoritma ne moti samega delovanja vezja in torej deluje sočasno z normalnim delovanjem. Ssistem je bil realiziran in evaluiran kot SoC v 350nm tehnologiji CMOS.
		ANG	A flash interpolator circuit inherent amplitude measurement algorithm, AMM, is described. The proposed technique of amplitude measurement is suitable for automatic gain control, AGC, and the systems for automatic signal conditioning, where a flash interpolator is already a part of the integrated motion control system.

			The SoC ASIC for incremental optical encoders is designed and processed in 0.35 µm CMOS technology.
	Objavljeno v		PLETERSEK Anton, BENKOVIC Roman, Janez Trontelj, Interpolation Method and Frequency Independent Peak Amplitude Measurement of Orthogonal – Periodic Signals, Recent Patents on Engineering, BENTHAM SCIENCE Publishers, ISSN: 1872-2121 - Volume 5, 3 Issues, 2011 (v prilogi:ANTON-PLETERSEK-MS.pdf); BENKOVIČ Roman je zaposlen v IDS. (Upcoming Article of Recent Patents on Engineering): www.benthamscience.com/eng/UpcomingArticles.htm
	Tipologija		1.01 Izvirni znanstveni članek
	COBISS.SI-ID		2
5.	Naslov	*SLO*	Omejitve pri načrtovanju integriranih sistemov za nizke napajalne napetosti v nanometerskih tehnologijah CMOS
		ANG	Constraints for low voltage - low power integrated systems design for deep sub-micron CMOS technologies
	Opis	*SLO*	Na konferenci je bila predstavljena analiza nanometerskih tehnologij in vpliv skaliranih parametrov na delovanje analognih vezij. S tem smo naredili korak k integraciji prihodnjih dekodirnih sistemov, ki bi delovali z baterijskim napajanjem, vendar bo prej potrebno rešiti probleme, ki jih prinašajo kratki kanali MOS tranzistorjev v tehnologijah pod 350nm. Načrtali smo vrsto ASSC sklopov in jih analizirali v tehnologijah do 65 nm. Predvsem smo analizirali vpliv tokov (leakage) na lastnosti analognih sklopov in predlagali nekaj novih rešitev. Analizo smo delali z analizatorjem Spectre.
		ANG	A design consideration and representative design examples for battery assisted ASIC systems are presented using standard 350 nm technology where ordinary and low threshold devices are available. A number of parts from ASSC has already been analysed. As the low power and low voltage LPLV system design is predominated by low power objectives, the overall leakage has been considered as a dominant issue. To demonstrate the importance of leakage current to ASIC performance, the most representative designs are analyzed with Spectre simulation program.
	Objavljeno v		PLETERŠEK, Anton, KOVAČIČ, Kosta. Constraints for low voltage - low power integrated systems design for deep sub-micron CMOS technologies. Proceedings. Ljubljana: MIDEM - Society for Microelectronics, Electronic Components and Materials, 2010, str. 161-166.
	Tipologija		1.08 Objavljeni znanstveni prispevek na konferenci
	COBISS.SI-ID		7930196

7. Najpomembnejši družbeno-ekonomsko relevantni rezultati projektne skupine[6]

	Družbeno-ekonomsko relevantni rezultat		
1.	Naslov	*SLO*	Postopek za samodejno reguliranje amplitude vhodnih signalov
		ANG	Method for automatically controlling the amplitude of input signals
	Opis	*SLO*	Povsem nov algoritem merjenja amplitude AMM, ki je inherenten v bliskovnem interpolacijskem vezju, kismo ga razvili in patentirali v IDS. Interpolator pretvarja pravokotne vhodne signale v zaporedje fazno zamaknjenih sinusnih signalov, katerih amplitude kombiniramo z AMM algoritmov v efektivno veličino, ki je merilo amplitude vseh vhodnih ortogonalnih signalov.AMM nato kontrolira AGC.
		ANG	A flash interpolator circuit inherent amplitude measurement algorithm, AMM, is described. A flash interpolation circuit converts a pair of periodic and orthogonal sine-signals into a stream of periodic – phase shifted sinusoidal signals, the amplitudes of which can be combined to produce useful information about the peak amplitude of the input sine-signals, independently of the signal's frequency. The proposed technique of amplitude measurement is suitable for automatic gain control, AGC.
	Šifra		F.17 Prenos obstoječih tehnologij, znanj, metod in postopkov v prakso
			A. PLETERŠEK, A. VODOPIVEC, Method for automatically controlling the amplitude of input signals, International publication number WO2008/036053 A1,

	Objavljeno v		PLETERŠEK, Anton, VODOPIVEC, Andrej. Postopek za samodejno reguliranje amplitude vhodnih signalov : patent št. 22403, podeljen z odločbo z dne 5. 5. 2008 : št. prijave P-200600218, Ljubljana: Urad Republike Slovenije za intelektualno lastnino, 2008.
	Tipologija		2.24 Patent
	COBISS.SI-ID		6503764
2.	Naslov	*SLO*	Interpolacijska metoda in vezje za izvajanje metode, ki se uporabljav dekodirnikih z visoko ločljivostjo
		ANG	Interpolation method and a circuit for carrying out said method used in a high-resolution encoder
	Opis	*SLO*	V patentu je opisan algoritem interpolacije (IP=4, točnost 5,8%), ki je bil primerna osnova za nadaljnje raziskovanje merjenja povprečne amplitude več kanalov hkrati in v katerega smo vgradili povsem nov merilnik povprečne amplitude dveh ortogonalnih signalov. Podeljeni patent v ZDA in EU državah uporablja inovativno rešitev merjenja amplitud (v prilogi).
		ANG	A flash interpolation circuit converts a pair of periodic and orthogonal sine-signals into a stream of periodic – phase shifted sinusoidal signals, the amplitudes of which can be combined to produce useful information about the peak amplitude of the input sine-signals, independently of the signal's frequency. An interpolation factor of 4 is shown to be sufficient for measuring amplitudes with an accuracy of 5.8 %.
	Šifra		F.06 Razvoj novega izdelka
	Objavljeno v		PLETERŠEK, Anton, BENKOVIČ, Roman. Interpolation method and a circuit for carrying out said method used in a high-resolution encoder: US 7,777,661 B2, 2010-08-17. [S. l.]: United States Patent and Trademark Office, 2010. LETERŠEK, Anton, BENKOVIČ, Roman. Interpolation method and a circuit for carrying out said method used in a high-resolution encoder: EP 2079 988 B1, European Patent Office, grant of the patent:07-07-2010.
	Tipologija		2.24 Patent
	COBISS.SI-ID		6503508
3.	Naslov	*SLO*	Napetostni primerjalnik
		ANG	Voltage comparator
	Opis	*SLO*	Patentiran je napetostni primerjalnik, ki ga uporabljamo pri vseh integriranih aplikacijah, kjer je potreben hiter prenos podatkov ali hitri digitalni preklopi in majhne zakasnitve. Uporabljamo ga tudi v interpolacijskih vezjih, ki delujejo na bliskovnem principu in so uporabni v merilnikih amplitude iz tega aplikativnega projekta.
		ANG	Voltage comparator where the difference of currents from transistors is converted into voltage, which is amplified and conducted to a gate terminal of the switching transistor. It is usuful part of a systems where a high sped data transmission or very low transit delay is required as is an example in a flash interpolators.
	Šifra		F.06 Razvoj novega izdelka
	Objavljeno v		KUNC, Vinko, VODOPIVEC, Andrej. Voltage comparator : US 7635995 (B2), 2009-12-22. Alexandria: United States Patent and Trademark Office, 2009. 13 str., ilustr. [COBISS.SI-ID 6010964]
	Tipologija		2.24 Patent
	COBISS.SI-ID		6010964
4.	Naslov	*SLO*	Optični merilni sistem dajalnika za merjenje linearnega pomika
		ANG	Optical encoder for linear position measurement
	Opis	*SLO*	Tri diplomska dela so bila realizirana v obdobju trajanja projekta in so direktno povezana z projektom. Eden diplomant se je zaposlil v IDS, kjer dela na doktorski disertaciji, dva sta se zaposlila v RLS. Vsem je bil mentor Anton Pleteršek.
			Three graduate students already completed study with diploma degree under supervision of prof. Pleteršek. All three works thematically matched the contents of the applied project. One engineer is currently employ in IDS and

		ANG	study toward PhD degree, another two are working in RLS, the leading IDS"s customer in motion control field.
	Šifra		D.10 Pedagoško delo
	Objavljeno v		- ROZMAN, Jernej. Optični merilni sistem dajalnika za merjenje linearnega pomika : diplomsko delo. Ljubljana: [J. Rozman], 2007. VI, 47 f., - KORBAR, Tilen. Sistem za avtomatsko testiranje interpolacijskih vezij dajalnikov pozicije : diplomsko delo. Ljubljana: [T. Korbar], 2007. 62 f., - OGRIN, Aljaž. Merilni sistem za verifikacijo in testiranje integriranega vezja SOC za absolutni linearni magnetni senzor : diplomsko delo. Ljubljana: [A. Ogrin], 2009. 50 f.,
	Tipologija		2.11 Diplomsko delo
	COBISS.SI-ID		6081364
5.	Naslov	*SLO*	Načrtovanje integriranih vezij ASIC za avtomobilske aplikacije
		ANG	ASIC design for automotive applications
	Opis	*SLO*	Na konferenci je dr. Pleteršek, soustanovitelj podjetja IDS, predstavil tehnike načrtovanja integriranih sistemov za avtomobilsko elektroniko predvsem z vidika zahtev in strogih predpisov, ki veljajo za avtomobilsko panogo. Tu so pomembne rešitve glede imunosti na motnje (varnost in zanesljivost delovanja) ter zmanjšanje emitiranja motenj (EMI, RFI, in elektromagnetna kopatibilnost EMC). Te zahteve predpisujejo mednarodni standardi in jih upoštevamo pri načrtovanju vseh elektronskih aplikacij, tudi dekodirnih vezjih, ki so prav tako uporabljena v avtomobilih.
		ANG	The following topics have been presented by invited speaker dr. Pletersek: Automotive Systems as they relate to EMI/RFI/ESD, the appropriate Industry Terminology, ASIC solutions for EMI/RFI – ASIC environment, design considerations for EMC, design considerations for Electrostatic Discharge, ESD and regulations covering the listed topics. The presentation have been supported by representative design examples.
	Šifra		B.04 Vabljeno predavanje
	Objavljeno v		Automotivenets Workshop, Trento, Italy, 24th Feb. 2011, PLETERŠEK, Anton, PODRŽAJ, Jurij. ASIC design for automotive applications. [S. l.]: Autoclusters, 2011.
	Tipologija		1.07 Objavljeni strokovni prispevek na konferenci (vabljeno predavanje)
	COBISS.SI-ID		8234580

8. Drugi pomembni rezultati projetne skupine[8]

Vstop na mednarodni trg z IDS produkti, ki jih spremlja vrsta IDS-ovih mednarodnih patentov:
1. Press Release 07. April 2010.
Groundbreaking New IDS Single-Chip RFID Data Logger with Sensor Helps to Reduce Medical, Healthcare and Environmental Safety Concerns.
2. Press Release 12. January 2009.
IDS-SL13A Universal, Affordable Smart Label Chip Named Product of the Year by Electronic Products Magazine.
3. 7. March 2011:
IDS releases its new EPC-based sensory tag chip. The SL900A can automatically track, monitor, time-stamp and record sensory information, which typically include temperature, pressure, humidity and vibration.

IDS-ovi produkti, ki so bili prenešeni v serijsko proizvodnjo v zadnjih treh letih:
(Razvoj RFID infrastrukture, RF in UHF vezij ASIC (ASSP) in raziskave rešitev v IDS, ki so patentirane v 30. mednarodnih patentih s področja RFID. Na področju senzorike dve vezji ASIC za RLS)
To je tudi široko raziskovalno področje za vrsto mladih raziskovalcev v podjetju IDS.]
1. Serija integriranih vezij IDS-R902DRM, izpraševalnik pametnih kartic
za frekvenčno področje UHF - ISO 16000-6C - Gen2, (x-2010)
2. IDS-SL13A je pametha aktivna nalepka z integriranim temperaturnim senzorjem, (2008-2009).
3. IDS-SL900A je čip, ki ima vgrajen protokol EPC Class 3 in senzor, (2009 - 20010).
4. Serija vezij ASIC za Ti (Kapacitivni prenos podatkov preko izolacijske bariere), (x-2010)
5. Integrirani linearni magnetni dekodirnik s 13 bitno ločljivostjo in ASSC, AK_MIS (2009-2010)

6. Integrirani rotacijski magnetni dekodirnik z interpolatorjem in 12 bitno ločljivostjo, KOT6 (2009-2010),
8. Integrirano bipolarno magnetno stikalo AK_LMAB, (2010).
....

9. Pomen raziskovalnih rezultatov projektne skupine[9]

9.1. Pomen za razvoj znanosti[10]

SLO

Cilj raziskave je bil izboljšati kvaliteto senzorskih signalov, s katerimi z nadaljnjo interpolacijo dosežemo večjo ločljivost dekodirnikov. Z novimi algoritmi smo premaknili meje ločljivoeti optičnih dekodirnikov daleč za stanje tehnike, saj se je večina raziskav dosedaj odvijala na zniževanju popačenja signalov dekodirnih glav. Tudi člani IDS so opisal eno takšnih rešitev (članek v IEEE). Predstavljena AMM in fazna korekcija PCA so v smislu izvedljivosti integrabilne in zato omogoćajo veliko robustnost dekodirnih aplikacij - torej večjo zanesljivost, kar je poleg točnosti ključen faktor. Razvitih je bila vrsta integrabilnih algoritmov, ki je privedla do izboljšav, ki smo jih zaščitili z SLO in evropskimi patenti. Doseženi rezultati bodo osnova za nadaljevanje in bodo pospešili raziskave v smislu povečevanja preciznosti meritev znotraj algoritmov, ki zagotavljajo veliko zanesljivost delovanja industrijskih aplikacij in s tem bo znanost uspešno posegla na področje merjenja nanometerskih dimenzij. Naše rešitve puščajo odprto pot tako za raziskave kot za implementacijo algoritmov za avtomatično kontrolo meritev, ki so vezani na sistemske lastnosti samih aplikacij. Opisani in na siliciju implementirani algoritmi so elektronski sklopi (analogni procesorji - AFE), ki ustrezno obdelujejo analogne signale, dobljene iz optičnih merilnih glav ali so v celoti integrirani v IDS-ovih magnetnih dekodirnikih. Prav tako so v teku nadaljnje raziskave novih metod (diplomska dela in doktorati zaposlenih v IDS).

ANG

The target of this work was to improve the quality of the quadrature signals to enable higher interpolation factors and higher encoder resolution. The present progress already moves the selectivity limits far beyond the state-of-the art, the base of which was solutions on optical encoders heads. Also IDS has very encouraging results using Vernier based pitch modulated optical head (Article in IEEE). The proposed solution for AMM and phase correction PCA is much more robust than that using a square circuit to generate DC voltage out of sine and cosine signals, used by competitors. The amplitude measurement described in this paper is an inherently linear process that generates envelope by using the same signal processing path as the interpolator itself. The interpolator monotonicity is guaranteed by the proposed architecture. These are the main advantages over algorithms and products, used by competitors. Present work is an example showing frequency independent and fast measurement of signal amplitude, phase and offset voltage. All achieved results will further accelerate work towards the more sophisticate and more precise measuring algorithms that will be even faster and suitable for use in sub-nanometer measuring applications. Algorithms that automatically control measured parameters depend on applications and will always be developed regarding applications and overall system requirements. The analog front-end electronics that occupies new algorithms is a basis for IDS future magnetic type decoders. Further work is in progress (PhD and Ms degree students in IDS).

9.2. Pomen za razvoj Slovenije[11]

SLO

Rezultat aplikativnega projekta je bil razviti nove, robustne in integrabilne algoritme za avtomatično regulacijo parametrov zajemanja senzorskih signalov, ki temeljijo na ortogonalnosti in so zaradi omenjenih lastnosti tudi cenovno ugodni, kar pomeni, da lahko dosegamo dober izplen in minimalno porabo silicija pri integraciji v sisteme na čipu (SoC). Zato smo razvili novo interpolacijsko vezje, ki mu je bilo potrebno dodati minimalno elektroniko. Sistem merjenja in korekcije jebil integriran v testno vezje EN400B, ki je trenutno najhitrejše tovrstno vezje z najvišjih interpolacijskim številom pri dani hitrosti merjenja. To seveda pomeni konkurenčnost in tržno prednost podjetna IDS tudi na področju merilnih sistemov - v prihodnjih letih in tudi boljše produkte za slovenska podjetja, s katerimi IDS sodeluje (na primer RLS, ki mu IDS uspešno načrtuje integrirane magnetne dekodirne sisteme na siliciju, kjer vgrajujemo integrabilne algoritme, načrtane v sklopu aplikativnega projekta). Novi produkti so prisotni na svetovnem trgu, kar povečuje tehnološki ugled Slovenije.

ANG

The aim of this application research and development was to find a cost-effective and area-

efficient method of generating peak amplitude information from sine wave signals which was a bases for the AGC function. The major part of the amplitude measurement and envelope extraction is already inherent in the presented flash interpolator and only minor additional electronics has been added. The correction algorithms was analyzed and those suitable for integration (automatic signal conditioning ASC) was implemented in test ASIC EN400B. The results is a speed independent, robust and the world-fastest interpolator ASIC designed in IDS which means growing market for IDS product in incoming years and better products for our domestic client (RLS, for instance, the company which is the IDS leading customer for magnetic type encoders).

10. Samo za aplikativne projekte!
Označite, katerega od navedenih ciljev ste si zastavili pri aplikativnem projektu, katere konkretne rezultate ste dosegli in v kakšni meri so doseženi rezultati uporabljeni

Cilj		
F.01	**Pridobitev novih praktičnih znanj, informacij in veščin**	
	Zastavljen cilj	(•) DA ( ) NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.02	**Pridobitev novih znanstvenih spoznanj**	
	Zastavljen cilj	(•) DA ( ) NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.03	**Večja usposobljenost raziskovalno-razvojnega osebja**	
	Zastavljen cilj	(•) DA ( ) NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.04	**Dvig tehnološke ravni**	
	Zastavljen cilj	(•) DA ( ) NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.05	**Sposobnost za začetek novega tehnološkega razvoja**	
	Zastavljen cilj	(•) DA ( ) NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.06	**Razvoj novega izdelka**	
	Zastavljen cilj	(•) DA ( ) NE
	Rezultat	Dosežen
	Uporaba rezultatov	Uporabljen bo v naslednjih 3 letih
F.07	**Izboljšanje obstoječega izdelka**	
	Zastavljen cilj	(•) DA ( ) NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.08	**Razvoj in izdelava prototipa**	

	Zastavljen cilj	◉ DA ○ NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.09	**Razvoj novega tehnološkega procesa oz. tehnologije**	
	Zastavljen cilj	○ DA ◉ NE
	Rezultat	
	Uporaba rezultatov	
F.10	**Izboljšanje obstoječega tehnološkega procesa oz. tehnologije**	
	Zastavljen cilj	○ DA ◉ NE
	Rezultat	
	Uporaba rezultatov	
F.11	**Razvoj nove storitve**	
	Zastavljen cilj	◉ DA ○ NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.12	**Izboljšanje obstoječe storitve**	
	Zastavljen cilj	◉ DA ○ NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.13	**Razvoj novih proizvodnih metod in instrumentov oz. proizvodnih procesov**	
	Zastavljen cilj	○ DA ◉ NE
	Rezultat	
	Uporaba rezultatov	
F.14	**Izboljšanje obstoječih proizvodnih metod in instrumentov oz. proizvodnih procesov**	
	Zastavljen cilj	○ DA ◉ NE
	Rezultat	
	Uporaba rezultatov	
F.15	**Razvoj novega informacijskega sistema/podatkovnih baz**	
	Zastavljen cilj	○ DA ◉ NE
	Rezultat	
	Uporaba rezultatov	
F.16	**Izboljšanje obstoječega informacijskega sistema/podatkovnih baz**	
	Zastavljen cilj	○ DA ◉ NE
	Rezultat	
	Uporaba rezultatov	
F.17	**Prenos obstoječih tehnologij, znanj, metod in postopkov v prakso**	
	Zastavljen cilj	◉ DA ○ NE
	Rezultat	Dosežen

	Uporaba rezultatov	V celoti
F.18	**Posredovanje novih znanj neposrednim uporabnikom (seminarji, forumi, konference)**	
	Zastavljen cilj	(•) DA ( ) NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.19	**Znanje, ki vodi k ustanovitvi novega podjetja ("spin off")**	
	Zastavljen cilj	( ) DA (•) NE
	Rezultat	
	Uporaba rezultatov	
F.20	**Ustanovitev novega podjetja ("spin off")**	
	Zastavljen cilj	( ) DA (•) NE
	Rezultat	
	Uporaba rezultatov	
F.21	**Razvoj novih zdravstvenih/diagnostičnih metod/postopkov**	
	Zastavljen cilj	( ) DA (•) NE
	Rezultat	
	Uporaba rezultatov	
F.22	**Izboljšanje obstoječih zdravstvenih/diagnostičnih metod/postopkov**	
	Zastavljen cilj	( ) DA (•) NE
	Rezultat	
	Uporaba rezultatov	
F.23	**Razvoj novih sistemskih, normativnih, programskih in metodoloških rešitev**	
	Zastavljen cilj	(•) DA ( ) NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.24	**Izboljšanje obstoječih sistemskih, normativnih, programskih in metodoloških rešitev**	
	Zastavljen cilj	( ) DA (•) NE
	Rezultat	
	Uporaba rezultatov	
F.25	**Razvoj novih organizacijskih in upravljavskih rešitev**	
	Zastavljen cilj	( ) DA (•) NE
	Rezultat	
	Uporaba rezultatov	
F.26	**Izboljšanje obstoječih organizacijskih in upravljavskih rešitev**	
	Zastavljen cilj	( ) DA (•) NE
	Rezultat	
	Uporaba rezultatov	

F.27	**Prispevek k ohranjanju/varovanje naravne in kulturne dediščine**	
	Zastavljen cilj	○ DA ◉ NE
	Rezultat	
	Uporaba rezultatov	
F.28	**Priprava/organizacija razstave**	
	Zastavljen cilj	○ DA ◉ NE
	Rezultat	
	Uporaba rezultatov	
F.29	**Prispevek k razvoju nacionalne kulturne identitete**	
	Zastavljen cilj	○ DA ◉ NE
	Rezultat	
	Uporaba rezultatov	
F.30	**Strokovna ocena stanja**	
	Zastavljen cilj	◉ DA ○ NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.31	**Razvoj standardov**	
	Zastavljen cilj	○ DA ◉ NE
	Rezultat	
	Uporaba rezultatov	
F.32	**Mednarodni patent**	
	Zastavljen cilj	◉ DA ○ NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.33	**Patent v Sloveniji**	
	Zastavljen cilj	◉ DA ○ NE
	Rezultat	Dosežen
	Uporaba rezultatov	V celoti
F.34	**Svetovalna dejavnost**	
	Zastavljen cilj	◉ DA ○ NE
	Rezultat	Dosežen bo v naslednjih 3 letih
	Uporaba rezultatov	Uporabljen bo v naslednjih 3 letih
F.35	**Drugo**	
	Zastavljen cilj	○ DA ◉ NE
	Rezultat	
	Uporaba rezultatov	

Komentar

11. Samo za aplikativne projekte!
Označite potencialne vplive oziroma učinke vaših rezultatov na navedena področja

	Vpliv	Ni vpliva	Majhen vpliv	Srednji vpliv	Velik vpliv	
G.01	**Razvoj visoko-šolskega izobraževanja**					
G.01.01.	Razvoj dodiplomskega izobraževanja	○	○	○	◉	
G.01.02.	Razvoj podiplomskega izobraževanja	○	○	○	◉	
G.01.03.	Drugo:	○	○	○	○	
G.02	**Gospodarski razvoj**					
G.02.01	Razširitev ponudbe novih izdelkov/storitev na trgu	○	○	○	◉	
G.02.02.	Širitev obstoječih trgov	○	○	○	◉	
G.02.03.	Znižanje stroškov proizvodnje	◉	○	○	○	
G.02.04.	Zmanjšanje porabe materialov in energije	◉	○	○	○	
G.02.05.	Razširitev področja dejavnosti	○	○	○	◉	
G.02.06.	Večja konkurenčna sposobnost	○	○	○	◉	
G.02.07.	Večji delež izvoza	○	○	○	◉	
G.02.08.	Povečanje dobička	○	○	○	◉	
G.02.09.	Nova delovna mesta	○	○	○	◉	
G.02.10.	Dvig izobrazbene strukture zaposlenih	○	○	○	◉	
G.02.11.	Nov investicijski zagon	○	○	○	◉	
G.02.12.	Drugo:	○	○	○	○	
G.03	**Tehnološki razvoj**					
G.03.01.	Tehnološka razširitev/posodobitev dejavnosti	○	○	○	◉	
G.03.02.	Tehnološko prestrukturiranje dejavnosti	◉	○	○	○	
G.03.03.	Uvajanje novih tehnologij	○	○	○	◉	
G.03.04.	Drugo:	○	○	○	○	
G.04	**Družbeni razvoj**					
G.04.01	Dvig kvalitete življenja	○	○	◉	○	
G.04.02.	Izboljšanje vodenja in upravljanja	○	○	◉	○	
G.04.03.	Izboljšanje delovanja administracije in javne uprave	◉	○	○	○	
G.04.04.	Razvoj socialnih dejavnosti	◉	○	○	○	
G.04.05.	Razvoj civilne družbe	◉	○	○	○	
G.04.06.	Drugo:	○	○	○	○	
G.05.	**Ohranjanje in razvoj nacionalne naravne in kulturne dediščine in identitete**	◉	○	○	○	
G.06.	**Varovanje okolja in trajnostni razvoj**	○	○	◉	○	

G.07	**Razvoj družbene infrastrukture**					
G.07.01.	Informacijsko-komunikacijska infrastruktura	○	◉	○	○	
G.07.02.	Prometna infrastruktura	○	◉	○	○	
G.07.03.	Energetska infrastruktura	○	○	◉	○	
G.07.04.	Drugo:	○	○	○	○	
G.08.	**Varovanje zdravja in razvoj zdravstvenega varstva**	◉	○	○	○	
G.09.	**Drugo:**	○	○	○	○	

Komentar

"Integrirani optični mikrosistemi", "Integrirani magnetni mikrosistemi" so vključeni v predmete, ki jih predava prof. Anton pleteršek na Univerzi v Ljubljani (FE) in v Mariboru (FERI) na doktorskem študiju in drugi bolonjski stopnji. Anton Pleteršek je soustanovitelj spin-off podjetja IDS - leta 1996, kjer tudi aktivno sodeluje pri razvoju.

12. Pomen raziskovanja za sofinancerje, navedene v 2. točki [12]

1.	**Sofinancer**	IDS Integrirani in diskretni sistemi d.o.o.		
	Vrednost sofinanciranja za celotno obdobje trajanja projekta je znašala:		150.000,00	**EUR**
	Odstotek od utemeljenih stroškov projekta:		25,00	**%**
	Najpomembnejši rezultati raziskovanja za sofinancerja			**Šifra**
	1.	IDS je sofinancer, in nosilna raziskovalna organizacija! Dosežki so našteti v prejšnjih poglavjih.		F.06
	2.	Objave, podane v 6), v priponki članek, sprejet v "BENTHAM SCIENCE" Recent Patents on Engineering: ANTON-PLETERSEK-MS.pdf		A.01
	3.	Jernej Rozman, avtor člankov s področja merilne tehnike je zaposlen v IDS in študira na doktorskem študiju.		A.07
	4.	prof. Pleteršek predava na FERI in doktorskem študiju na FE. Predmet temelji tudi na raziskovalnih izsledkih skupine IDS-RS (Integrirani optični SoC sistemi, Integrirani magnetni SoC sistemi).		D.10
	5.	Samo relevantni patenti (povezani s L2-9304) so podani v 7). Člani IDS-RS imajo sicer preko 100 patentov.		F.32
	Komentar	Ostali rezultati so podani in opisani v razdelkih 3), 4), 6), 7) in 8).		
	Ocena	podana v 3) in 4)		
2.	**Sofinancer**			
	Vrednost sofinanciranja za celotno obdobje trajanja projekta je znašala:			**EUR**
	Odstotek od utemeljenih stroškov projekta:			**%**
	Najpomembnejši rezultati raziskovanja za sofinancerja			**Šifra**
	1.			
	2.			

		3.		
		4.		
		5.		
	Komentar			
	Ocena			
3.	**Sofinancer**			
	Vrednost sofinanciranja za celotno obdobje trajanja projekta je znašala:			**EUR**
	Odstotek od utemeljenih stroškov projekta:			**%**
	Najpomembnejši rezultati raziskovanja za sofinancerja			**Šifra**
		1.		
		2.		
		3.		
		4.		
		5.		
	Komentar			
	Ocena			

C. IZJAVE

Podpisani izjavljam/o, da:

- so vsi podatki, ki jih navajamo v poročilu, resnični in točni
- se strinjamo z obdelavo podatkov v skladu z zakonodajo o varstvu osebnih podatkov za potrebe ocenjevanja, za objavo 6., 7. in 8. točke na spletni strani http://sicris.izum.si/ ter obdelavo teh podatkov za evidence ARRS
- so vsi podatki v obrazcu v elektronski obliki identični podatkom v obrazcu v pisni obliki
- so z vsebino zaključnega poročila seznanjeni in se strinjajo vsi soizvajalci projekta

Podpisi:

Andrej Vodopivec	in	
podpis vodje raziskovalnega projekta		zastopnik oz. pooblaščena oseba RO

Kraj in datum:	Ljubljana,	14.4.2011

Oznaka poročila: ARRS-RPROJ-ZP-2011-1/116

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[1] Zaradi spremembe klasifikacije družbeno ekonomskih ciljev je potrebno v poročilu opredeliti družbeno ekonomski cilj po novi klasifikaciji. Nazaj

[2] Samo za aplikativne projekte. Nazaj

[3] Napišite kratko vsebinsko poročilo, kjer boste predstavili raziskovalno hipotezo in opis raziskovanja. Navedite ključne ugotovitve, znanstvena spoznanja ter rezultate in učinke raziskovalnega projekta. Največ 18.000 znakov vključno s presledki (približno tri strani, velikosti pisave 11). Nazaj

[4] Realizacija raziskovalne hipoteze. Največ 3.000 znakov vključno s presledki (približno pol strani, velikosti pisave 11). Nazaj

[5] V primeru bistvenih odstopanj in sprememb od predvidenega programa raziskovalnega projekta, kot je bil zapisan v predlogu raziskovalnega projekta oziroma v primeru sprememb, povečanja ali zmanjšanja sestave projektne skupine v zadnjem letu izvajanja projekta (obrazložitev). V primeru, da sprememb ni bilo, to navedite. Največ 6.000 znakov vključno s presledki (približno ena stran, velikosti pisave 11). Nazaj

[6] Navedite največ pet najpomembnejših znanstvenih rezultatov projektne skupine, ki so nastali v času trajanja projekta v okviru raziskovalnega projekta, ki je predmet poročanja. Za vsak rezultat navedite naslov v slovenskem in angleškem jeziku (največ 150 znakov vključno s presledki), rezultat opišite (največ 600 znakov vključno s presledki) v slovenskem in angleškem jeziku, navedite, kje je objavljen (največ 500 znakov vključno s presledki), izberite ustrezno šifro tipa objave po Tipologiji dokumentov/del za vodenje bibliografij v sistemu COBISS ter napišite ustrezno COBISS.SI-ID številko bibliografske enote.
Navedeni rezultati bodo objavljeni na spletni strani http://sicris.izum.si/.

PRIMER (v slovenskem jeziku):
Naslov: Regulacija delovanja beta-2 integrinskih receptorjev s katepsinom X;
Opis: Cisteinske proteaze imajo pomembno vlogo pri nastanku in napredovanju raka. Zadnje študije kažejo njihovo povezanost s procesi celičnega signaliziranja in imunskega odziva. V tem znanstvenem članku smo prvi dokazali… (največ 600 znakov vključno s presledki)
Objavljeno v: OBERMAJER, N., PREMZL, A., ZAVAŠNIK-BERGANT, T., TURK, B., KOS, J.. Carboxypeptidase cathepsin X mediates ß2 - integrin dependent adhesion of differentiated U-937 cells. Exp. Cell Res., 2006, 312, 2515-2527, JCR IF (2005): 4.148
Tipopologija: 1.01 - Izvirni znanstveni članek
COBISS.SI-ID: 1920113 Nazaj

[7] Navedite največ pet najpomembnejših družbeno-ekonomsko relevantnih rezultatov projektne skupine, ki so nastali v času trajanja projekta v okviru raziskovalnega projekta, ki je predmet poročanja. Za vsak rezultat navedite naslov (največ 150 znakov vključno s presledki), rezultat opišite (največ 600 znakov vključno s presledki), izberite ustrezen rezultat, ki je v Šifrantu raziskovalnih rezultatov in učinkov (Glej: http://www.arrs.gov.si/sl/gradivo/sifranti/sif-razisk-rezult.asp), navedite, kje je rezultat objavljen (največ 500 znakov vključno s presledki), izberite ustrezno šifro tipa objave po Tipologiji dokumentov/del za vodenje bibliografij v sistemu COBISS ter napišite ustrezno COBISS.SI-ID številko bibliografske enote.
Navedeni rezultati bodo objavljeni na spletni strani http://sicris.izum.si/. Nazaj

[8] Navedite rezultate raziskovalnega projekta v primeru, da katerega od rezultatov ni mogoče navesti v točkah 6 in 7 (npr. ker se ga v sistemu COBISS ne vodi). Največ 2.000 znakov vključno s presledki. Nazaj

[9] Pomen raziskovalnih rezultatov za razvoj znanosti in za razvoj Slovenije bo objavljen na spletni strani: http://sicris.izum.si/ za posamezen projekt, ki je predmet poročanja. Nazaj

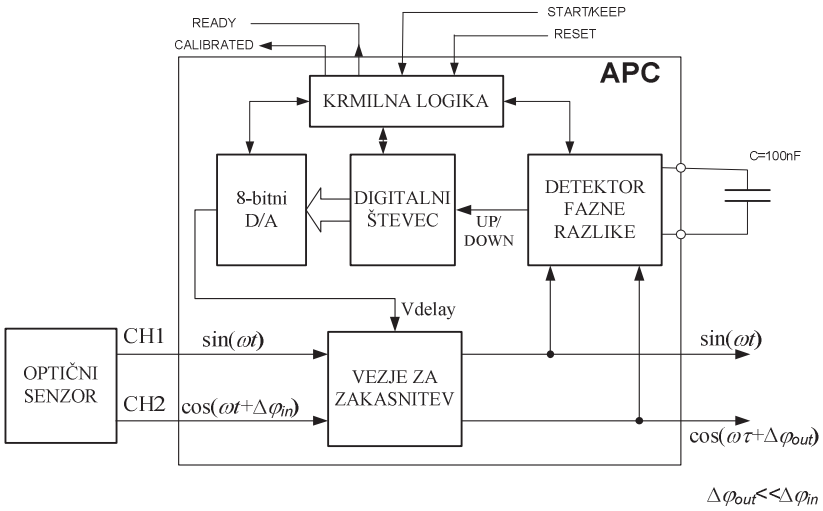
[10] Največ 4.000 znakov vključno s presledki Nazaj

[11] Največ 4.000 znakov vključno s presledki Nazaj

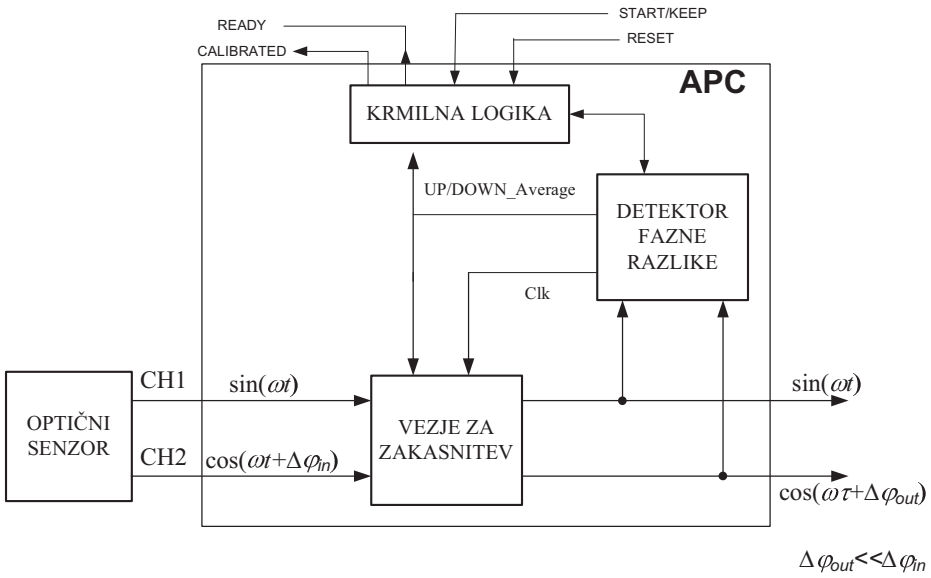
[12] Rubrike izpolnite/prepišite skladno z obrazcem "Izjava sofinancerja" (http://www.arrs.gov.si/sl/progproj/rproj/gradivo/), ki ga mora izpolniti sofinancer. Podpisan obrazec "Izjava sofinancerja" pridobi in hrani nosilna raziskovalna organizacija – izvajalka projekta. Nazaj

Obrazec: ARRS-RPROJ-ZP/2011-1 v1.01
E2-9C-40-4A-CE-DC-C4-D3-46-98-30-40-91-B1-0D-7C-F6-0E-D4-B7

Cilj naše skupine je bil razvoj in preverjanje koncepta za vezje, ki naj med samim delovanjem stroja samodejno kalibrira merilni sistem glede na fazni premik. Hkrati smo tudi dodali še krmilne signale, s katerimi je možno kalibracijo sprožiti in opazovati status izvajanja.



Slika 1 Blokovna shema faznega korektorja

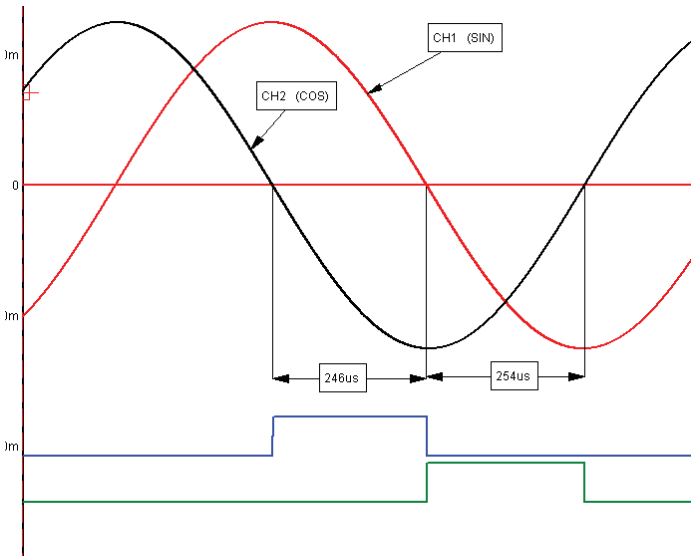


Slika 2 Izboljšana blokovna shema faznega korektorja- zadnja varianta

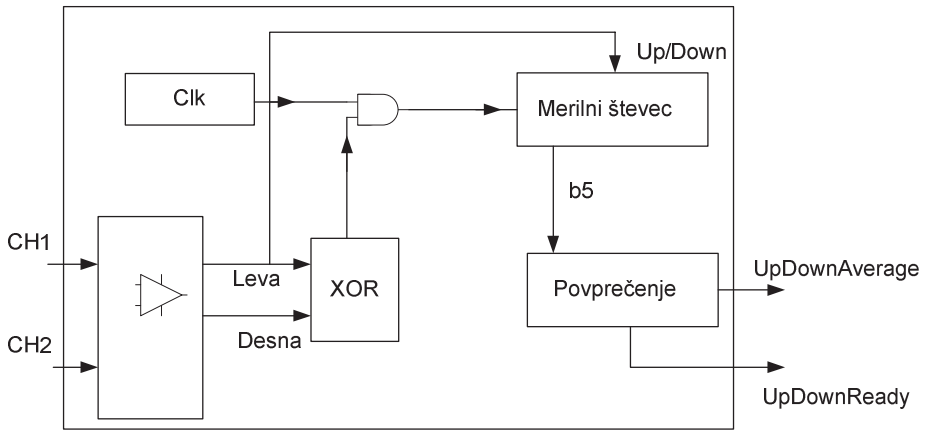
V predhodni varianti je fazni korektor potreboval zunanji kondenzator in 8-bitni D/A pretvornik. V novi verziji smo razvili skoraj popolnoma digitalno varianto detektorja in zakasnilnega vezja (slika 2).

Osnovna ideja, na kateri temelji novi koncept je, da iz obeh signalov izločimo dva digitalna signala, katerih širina je odvisna tudi od fazne zakasnitve (slika 3). Če sta signala različne širine, je med njima fazna razlika, ki jo je potrebno korigirati. To razliko ugotavljamo s 6-

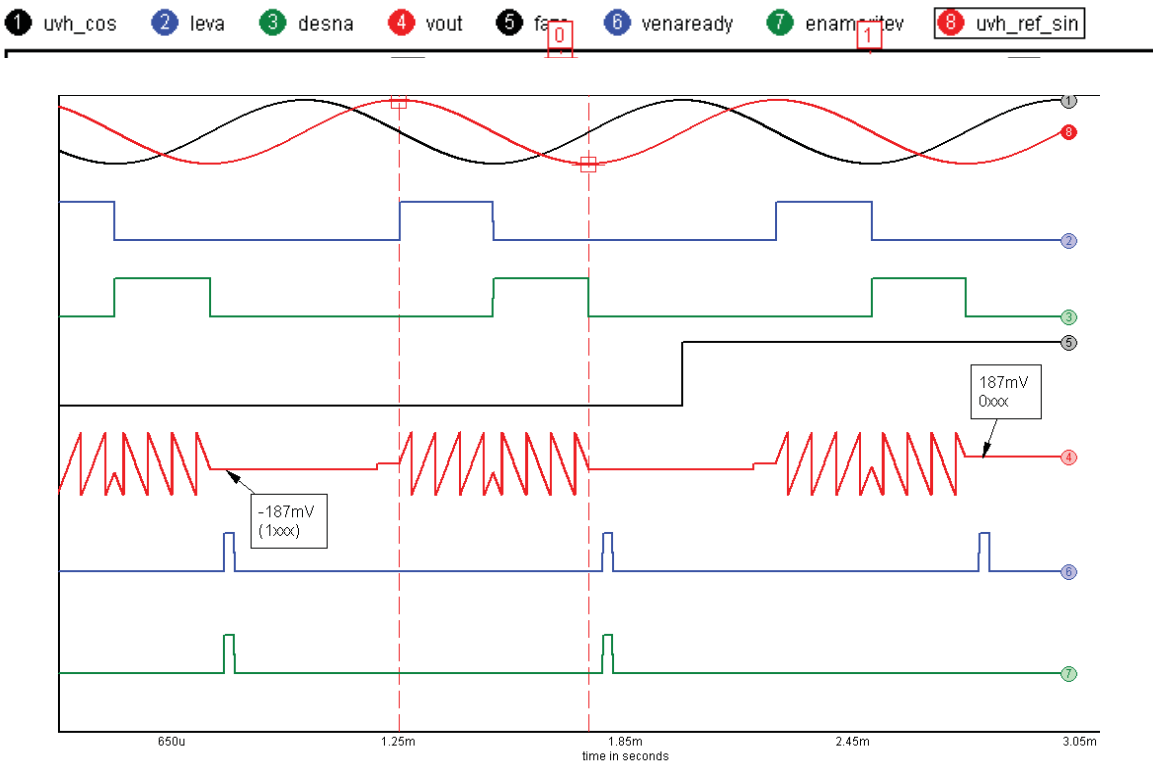
bitnim merilnim števcem, ki najprej šteje navzgor, nato pa navzdol. Najvišji bit pove ali je pri trenutni meritvi faza pozitivna ali pa negativna. Z drugim števcem štejemo število pozitivnih oziroma negativnih faznih razlik. Če ni nobene fazna razlike, je stanje tega števca v idealnih razmerah enako nič, v realnih pa neka nizka vrednost. Glede na stanje bitov z višjo utežjo tvorimo rezultat meritve (signal UpDownAverage). Število meritev je določeno s tretjim števcem. Ker merimo povprečno vrednost, se bodo v merilne napake, ki so naključne, v določenem obdobju izničile. **Natančnost merjenja obstoja fazne razlike je tako odvisna le od frekvence ure in od števila ponovitev meritev ter delno od komparatorja.** Pri frekvenci ure 1MHz je merilna negotovost ±0.1°. Glede na staro verzijo, je to velik napredek, saj sedaj ni več potreben zunanji kondenzator. Hkrati se je zaradi statističnega merjenja merilna napaka zelo zmanjšala.



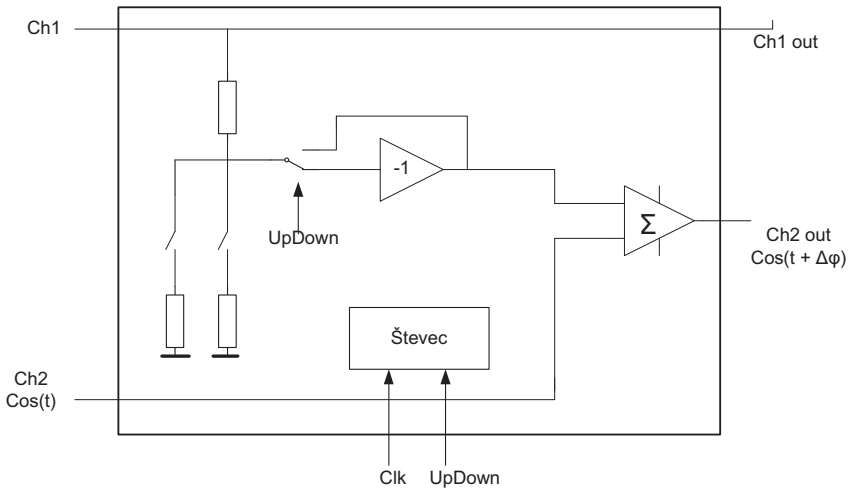
Slika 3 Signala med katerima nastopa majhna fazna razlika



Slika 4 Blokovna shema detektorja



Slika 5 Scenarij, kjer faza (5) iz začetne vrednosti -1° skoči na +1°. Signal (7) *enameritev* kaže rezultat detekcije. Vrednost 1 pomeni negativni fazni kot, vrednost 0 pa pozitivni kot. Signal (4) je analogni prikaz vrednosti stanja števca.



Slika 6 Blokovna shema zakasnilnega elementa

Zaradi spremenjenega faznega detektorja smo spremenili tudi zakasnilni element. Na vhod sta pripeljana dva signala: Clk – impulz, ki ga izločimo iz enega izmed kanalov CH1 ali CH2 in UpDown, ki pove, ali naj ob urinem impulzu povečamo ali zmanjšamo zakasnitev. Na ta vhod je priključen

signal UpDownAverage, ki ga dobimo iz detektorja. Vrednost zakasnitve je shranjena v števcu, katerega izhodi krmilijo stikala, s katerimi določimo zakasnitev. Ko je dosežena kompenzacija zakasnitve, se UpDownAverage zaporedoma spreminja 1->0->1->0,…. Kot krmilna logika to ugotovi, postavi signal CALIBRATED na 1 in s tem je fazna razlika korigirana.

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(54) **INTERPOLATION METHOD AND A CIRCUIT FOR CARRYING OUT SAID METHOD USED IN A HIGH-RESOLUTION ENCODER**

INTERPOLATIONSVERFAHREN UND SCHALTUNG ZUM AUSFÜHREN DES VERFAHRENS ZUR VERWENDUNG IN EINEM HOCHAUFLÖSENDEN KODIERER

PROCÉDÉ D'INTERPOLATION ET CIRCUIT POUR EXÉCUTER LEDIT PROCÉDÉ UTILISÉ DANS UN ENCODEUR À HAUTE RÉSOLUTION

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(45) **Date of Patent: Aug. 17, 2010**

(54) **INTERPOLATION METHOD AND A CIRCUIT FOR CARRYING OUT SAID METHOD USED IN A HIGH-RESOLUTION ENCODER**

(75) Inventors: **Anton Pletersek**, Na Klancu (SI); **Roman Benkovic**, Krzisnikova (SI)

(73) Assignee: **IDS d.o.o.**, Ljubljana (SI)

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See application file for complete search history.

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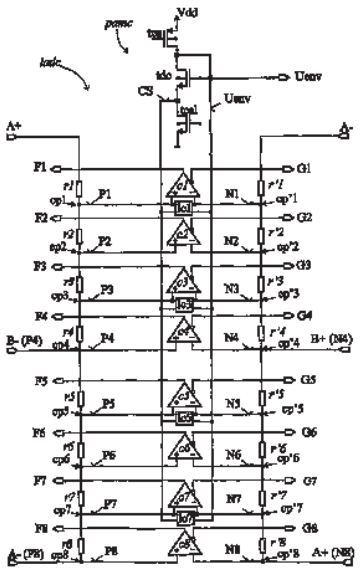
Primary Examiner—Khai M Nguyen
(74) *Attorney, Agent, or Firm*—Jacobson Holman PLLC

(57) **ABSTRACT**

Intermediate digital signals Fi(α), Gi(α), i=1, . . . I, are generated, which result from a comparison of reference potentials of the first input analogue signal at a shifted value of its observed argument and with a suitably reduced amplitude to the potential, which is inverse to said potential, of the third input analogue signal at the same shifted value of the observed argument and with the amplitude reduced in said way, the shifted argument values being uniformly distributed within the first half-period. A value U of the voltage is measured at any value of the observed argument as at that time the highest one of the voltages at terminals with said reference potentials. An actual peak amplitude A of the input analogue signals is determined as $A=k_{I,m}U$ where the factor $k_{I,m}$ is a quotient of the peak amplitude of said input analogue signals and of the mean value of the voltage waveform envelope of the reference potentials pertaining to said peak amplitude.

When the proposed method is used to automatically control the gain, said voltage U is conducted directly to the input of an automatic gain control circuit, whereat the input voltage of this circuit is set to the mean value of the voltage waveform envelope of the reference potentials.

12 Claims, 2 Drawing Sheets



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Published:
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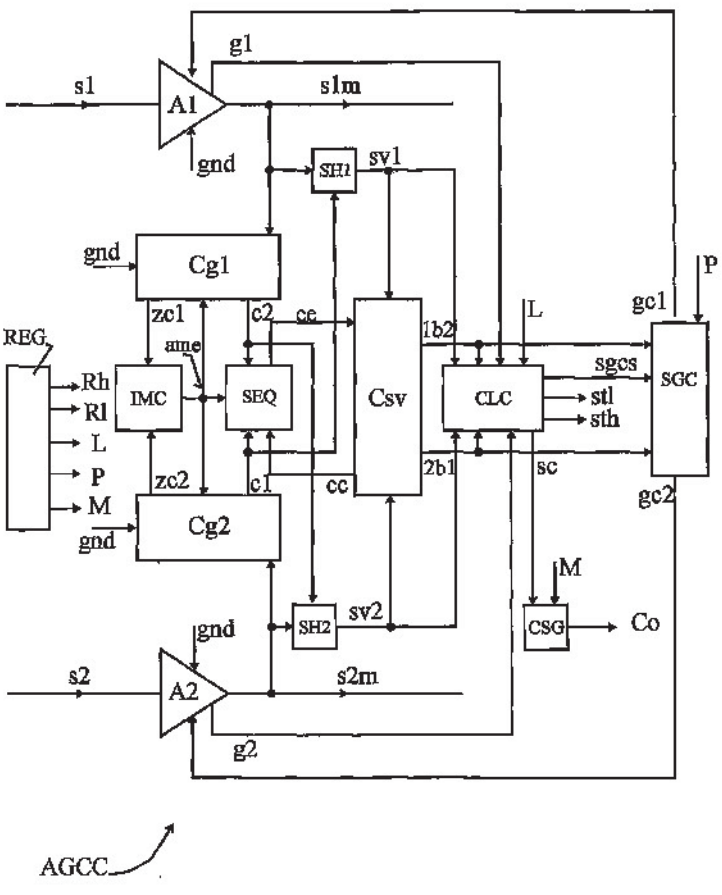
(54) **Title:** METHOD FOR AUTOMATICALLY CONTROLLING THE AMPLITUDE OF INPUT SIGNALS



(57) **Abstract:** Input signals having the same functional time dependence, *e.g.* a sinusoidal one, and being out-of-phase with regard to each other are amplified selectively according to the result of a previous comparison of the amplitudes of a first and a second matched signals (s1m, s2m), which were formed from the input signals (s1, s2) by means of said selective amplifying, which step-by-step matches the output signals to each other in amplitude. There is measured the duration (T) of a time interval between such passings of the matched signals through a signal ground (gnd) that both matched signals have the same polarity in said time interval. It is ascertained on the basis of the time duration (T) that the frequency of the input signals is within preset frequency limits. The first matched signal is sampled the moment the second matched signal passed through the signal ground and the second one the moment the first one passed through the signal ground. Values obtained by sampling are compared to each other. A selective gain control signal is generated as a result of said comparison of the sample values. The gain applied to either input signal is increased or decreased. The method of the invention for automatically controlling the amplitude of input signals initiates an automatic selective amplification of individual input signals.

WO 2008/036053 A1

Interpolation Method and Frequency Independent Peak Amplitude Measurement of Orthogonal – Periodic Signals

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Abstract: A flash interpolator circuit inherent amplitude measurement algorithm, AMM, is described. A flash interpolation circuit converts a pair of periodic and orthogonal sine-signals into a stream of periodic – phase shifted sinusoidal signals, the amplitudes of which can be combined to produce useful information about the peak amplitude of the input sine-signals, independently of the signal's frequency. The proposed technique of amplitude measurement is suitable for automatic gain control, AGC, and the systems for automatic signal conditioning, where a flash interpolator is already a part of the integrated motion control system. An interpolation factor of 4 is shown to be sufficient for measuring amplitudes with an accuracy of 5.8 %. The patents regarding signals conditioning and interpolation are reviewed. The interpolator architecture, combined with an amplitude measuring system, has been designed, integrated as a part of the interpolator ASIC, evaluated and analyzed. The SoC ASIC for incremental optical encoders is designed and processed in 0.35 μm CMOS technology.

Keywords: Interpolation, amplitude measurement, orthogonal signals, flash interpolator, automatic gain control, encoder.

1. INTRODUCTION

Many products in the automation industry require specifically designed devices to provide linear and angular position information to data acquisition and control systems. A typical application in the motion control field is in magnetic or optical linear and rotary encoders, the major part of which comprises integrated electronics. In general, the electronics comprise an opto-sensing area or hall sensors structure, analog front-end and signal conditioning, a fast interpolator and a digital signal processing unit. The front-end performs sensor supply, sensor excitation and signal magnification functions. The operation speed of the encoders, based on magnetic sensors, is usually much slower than one based on light modulation. This holds true mainly for magnetic rotary encoders, the speed of the magnetic linear encoders being faster, but usually never exceeding the speed of optical encoders [1-11].

An analog signal generated from a sensor's array is amplified and digitized to provide incremental orthogonal digital signals named track A and track B, which are counted in a counter circuit. Each "count" records one light-dark cycle of the code disk, relative to the phase (reading) plate. Before digitizing the analog signals they can be further interpolated to achieve better measurement resolution [12-24].

In the case where more than 7-bit resolution is required, conditioning of analog signals needs to be implemented. This includes equalization of the sine and cosine signal amplitudes, their offset equalization and phase difference adjustment to 90 degrees. The most common practice is adjusting analog front-end parameters via a serial interface or reprogramming them with access to internal EEPROM [25]. Automatic offset measurement and cancellation are relatively simple [26], the phase measurement and correction and the amplitude regulation and measurement being more complicated [27-31]. A magnitude and phase estimation algorithm has been published [32] for a signal with time-varying frequency. The method is slow and requires modest computations.

Squaring algorithm using analog multipliers is a well known method for obtaining/extracting DC information from sine-cosine signals [33]. The main disadvantages are the limited linear input voltage range and its temperature behavior. Also, the flash interpolator circuits that comprise the signal generating circuit, of which the out-of-phase signals are generated by gain stages having different magnifications, are much slower [15]. The appropriate comparator circuit [15] compares signals at different common mode levels, which may additionally cause different delays and offsets. The Cordic-based Loeffler discrete cosine transform (DCT) architecture is presented in [24]. It requires a high level of digital complexity and is very suitable for low-power and high-quality codecs.

Anything that can affect the accuracy of the final application is related to the system components of a decoder [34-36] and to the applied algorithms [5, 14 29, 37, 38]. This means that the question of calibration is system related.

The aim of this work is to present a less precise, but cost-effective and robust amplitude measurement algorithm, based on a flash interpolating circuit, suitable for VLSI integration on "system on chip SoC". Amplitude measurement is a basic pre-processing step for automatic signal-amplitude correction and for the AGC function. The major advantage

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of the proposed method is that there is no need for an extra system clock. Due to the lower silicon area consumption, low power consumption and signal frequency independent measurement method, the present solution is suitable for use in all integrated automatic signal conditioning systems.

This paper is organized as follows. The typical application-encoder-that uses AMM, the design considerations and up-to-date patents review are presented in Section 2. A detailed description of the proposed flash interpolation method using sine wave input signals with an interpolator-inherent principle of amplitude measurement is given in the third section and concluded in Section 4. The results of measurements are presented in Section 5.

2. ENCODER SYSTEM

2.1. Principle of Operation

An optical encoder translates an angular or linear position into an electrical signal. It is typically composed of a light source (LED), the main scale with a built-in optical grating with measuring period MP, and an optical scanner that is composed of an opto-sensor array and a reading scale with a built-in optical grating with a reading period, RP Fig. (**1**). The main and the reading scales are glass plates on which a thin layer of chromium metal is deposited, and a regular pattern is etched into this layer. If MP and RP are the same, then, as the scanner moves along the main scale, the patterns on the main and reading scales overlap to a degree, depending on the momentary position of the scanner. The scanning head Fig. (**1**) is composed of four photodiodes (D1 to D4) that produce the quadrature signals, and an additional photodiode (DF) that generates the index signal which is used for absolute position encoding. If the scanning head moves along the main scale with a constant velocity, then the photo sensor will produce a signal current that is periodic in time and has a fundamental frequency of $f = v/p$, where v is the velocity and p is the period of the grating. The spectral purity of this signal is determined mainly by the diffraction and reflection of the light by the two optical gratings in the main and reading scales. Without it the signals would have a triangular rather than a sinusoidal shape.

In short, as the scanner moves along the main scale the amount of light from the light source is modulated. The electrical signal that is produced by the opto-sensor in the optical array is also modulated.

As we have seen, the encoder produces two ninety-degree shifted (quadrature) signals A+, A- and B+, B- Fig. (**2**). The signals in Fig. (**2**) are periodic; this periodicity corresponds to the movement of the scanner head with constant velocity along the main scale. One period of the signal corresponds to the movement of the scanner head equal to the grating period (MP, RP). In general, the signals are not periodic in time, but are periodic in relation to the displacement along the main scale. The signals A+, A-, and B+, B- in Fig. (**2**) are also not pure sine-cosine, but are, in reality, distorted and contain harmonic components. The incoming signals are also imbalanced in phase, offset and amplitude. The encoder system therefore requires signal conditioning prior to interpolation. The amplitude measuring algorithm, described in the next section, is part of the signal conditioning.

The two pairs of signals from the optical array are usually transformed into voltages with a fully-differential voltage amplifier to remove the large DC component and suppress even harmonics to produce the signals to be further interpolated. The voltage amplifier should have a low output impedance to drive the resistive interpolation network. The two quadrature signals enable the position of the scanner head to be detected at all times, just by measuring the values of these two signals. To achieve high interpolation accuracy, the amplitude of the incoming sine signals should be regulated to the acceptable maximum level.

The signals can be digitized directly by an analog comparator. The two resulting digital signals (signal F4 and F8 in Fig. (**2b**) will still be in quadrature while all the information will be in the low-high and high-low transitions of the signals. There are four such transitions per grating period (MP, RP). Therefore the intrinsic resolution of the encoder is one fourth of the grating period. Alternatively, interpolation can be used to increase the resolution.

An incremental type encoder outputs a pair of digital square waves Ao and Bo Fig. (**2b**) that are 90 degrees apart and convey, for instance, the change in the shaft's position, and the direction of rotation. An absolute type encoder, on the other hand, detects an absolute position.

2.2. Patents Review

Current developments and published patents in motion control field are actually based on typical applications and appropriate requirements. Typical apparatus are described in patent [39] and patent [40]. An apparatus for determining values of a periodic function by interpolation is presented in invention [39], where the quadrature signals are combined in a converter using amplification-summing architecture. From here, the sine and cosine signals are derived. From these signals interpolation can be performed by a computer. In terms of high speed, this method needs high bandwidth amplification, not to degrade the quadrature over the frequency of operation. Very similar to this is the method proposed in [15]. Invention [40] describes a system for monitoring signals from a linear or rotary encoder that would provide warnings about the functionality of the encoder or would be able to predict a future malfunction. The system actually monitors the output of the detector by comparing the output with a predefined voltage reference. The generated error signal supplies the light source for maintaining constant and maximum detected light amplitude. In practice, such regulation is not sufficient, mainly due to the possible contamination of the measuring scale and consequently, a large signal reduction. An alarm signal indicates that the error signal used for controlling the light source exceeds a predetermined threshold [40]. Beside the illumination control [40], we also suggest [41] to build up the scanning head from the main scale with the grating period (*pitch*) of N μm and to chose a reading scale period of (N-1) μm to produce a Vernier pattern with a period of M=[N*(N-1)] μm. Inside this M μm we could place four photodiodes with maximum width of 95 μm that would form a scanning cell. The whole scanning head contains K such cells which are used to average out various

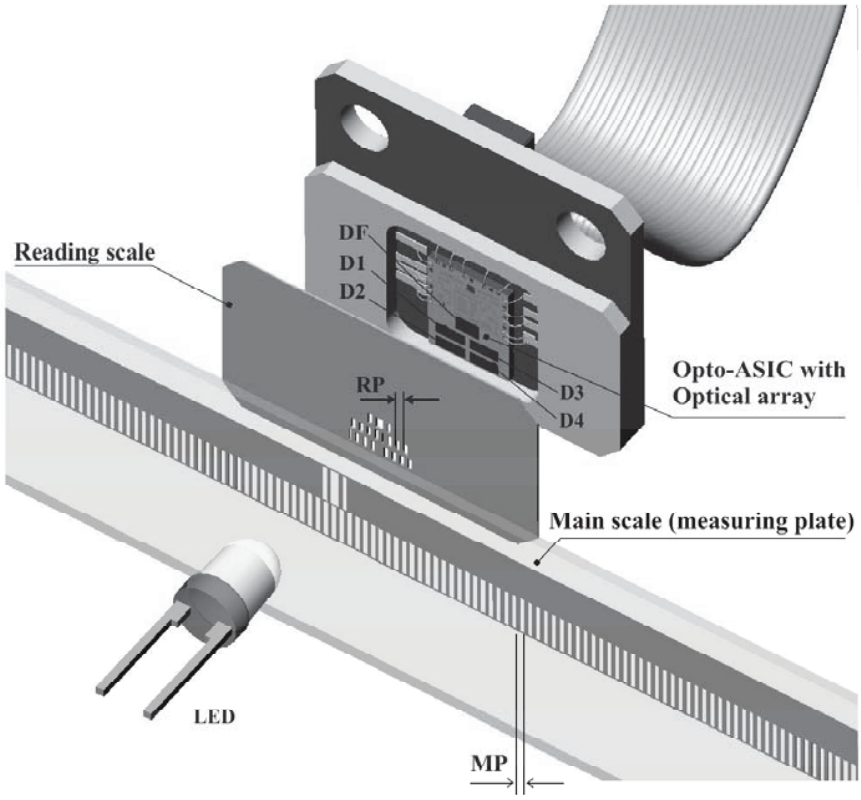

Fig..(**1**). Linear optical encoder system, composed by ASIC having integrated opto-sensors, signal conditioning and incremental interpolator circuit on the same die. The picture demonstrates the principle of the encoder operation. Published with the permission of RLS

unwanted effects, such as defects in the main and reading scale patterns or uneven illumination of the scanning head [41].

Processing of the quadrature signals in [27] uses quadrature reference signals from a high frequency reference oscillator and high frequency multipliers to multiply the base-generated signals which, applied on mixer inputs, cause the reference signal to be shifted by a frequency of the input signals on the mixer output. Further comparison with the reference signal acts as a scanning of the mixed - shifted period with reference signal the result of which interpolates the position of the read-head within the pitch of the marks on the scale. The drawback is the need for high frequency timing which may contaminate the receiving input sine signals and consequently produce harmonic components.

The algorithm to improve the quadrature relationship of the front-end outputs is invented in [37] by monitoring and comparing the two Lissajous figures on an oscilloscope screen. The read-head is being adjusted until the Lissajous figures coincide. Also presented in invention [37], is a method producing a DC output signal, which represents the radius of a hypothetical Lissajous derivable from the signals. A constant DC represents a constant Lissajous radius. The invented method sets proper phase and amplitudes but is a semi-manual method. The method in [42] equalizes the received samples and is related to a modulated optical carrier transmitted through an optical channel with impairments. The invention in [33] measures amplitudes by means of an analog multiplier using a quadritail circuit. This method is efficient but suffers from analog limitations like voltage signal swing and the signal bandwidth.

The most representative method regarding the automatic signal conditioning for encoder systems is presented in [43]. An arrangement as well as a method for the automatic correction of error-containing scanning signals, which contain defined deviations from the ideal signal shape, of incremental position measuring devices is disclosed. The ideal signal shape is presupposed by a down-stream arranged evaluation unit. A processor unit with an appropriate correction algorithm for generating control signals is implemented. A positive feature of this algorithm is that the processor unit, as well as the correction unit, are arranged in such a way that those scanning signals, which have already passed through the correction unit, are present at the input side of the processor unit. It is also an object of invention [43] to further develop the known arrangement and method of the other inventions in order to assure further improvement correction of error-containing analog scanning signals. Methods in [43] are not clearly described in terms of parameter measurements and interpolation used. A number of possible correction steps and parameter measuring algorithms are mentioned as viable options. The generalized system described is complicated in terms of fulfilling requirements for different stages like sample-and-hold, multiplexing, AD converter, CPU, software, non-volatile memory and more.

Our Invention [44] and [45] solves the technical problem how to improve the interpolation method and the circuit for carrying out said method so that it will be possible to determine the peak amplitude of the input signals. The improvement according the invention of the interpolation method and circuit distinguishes itself by the fact that the automatic gain control in a measuring device can be carried out by measuring only a voltage of the upper waveform envelope of the reference potentials. These potentials are generated in the step of the analogue-to-digital conversion of the input analogue signals, whereas the voltage of the upper waveform envelope is present also when the displacing of the sensors with regard to graduated scale is stopped. No complex multiplying or adding circuits are needed to determine the actual peak amplitude of the input analogue signals.

The invention will now be explained in detail by discussing the frequency-independent amplitude measurement of periodic and orthogonal signals. The method is inherent in flash interpolation algorithm itself which we have developed for fast – high frequency incremental measurements.

3. DESCRIPTION OF AMPLITUDE MEASUREMENT

3.1. Flash Interpolator

The basic architecture of the proposed flash interpolation converter consists of four matched resistive chains, connected in a symmetric bridge Fig. (**2a**). The resistivity of each chain is R_v. The differential channel signals CH-A and CH-B, ordinary and inverted (A+, A-, B+, B-), are connected to opposite sides of the bridge, the voltages of which are of equal amplitude, but phase shifted by 0 and 180 degrees (CH-A) and by 90 and -90 degrees (CH-B), as shown in Figs. (**2b** and **3**). An interpolation factor of *IP=4* is chosen as an example. Thus the interpolator circuit in Fig. (**2a**) consists of four resistive chains, each having *IP* resistors (r1 to r4 with total resistivity of $R_v = \sum_{1}^{4} r_i$). It also consists of *2 IP* voltage comparators, C1 to C8, connected to the taps of the bridge. Each comparator always compares tap voltages on the same common mode (CM) level, as shown from simulations in Fig. (**3**) (s1, s2, to s16). Each comparator compares two voltages, shifted in phase by exactly 180 degrees. Although all comparators operate at the same

CM level, they differ in performance, which causes INL and DNL errors of the output code (variations of the separation time). Interpolator linearity is also limited by the resistors' matching requirements. Resistance values in the chain are calculated according to the shape of the incoming orthogonal and differential signals connected to the bridge corners (A+, A-, B+, and B-). Angle resolution *K* is defined by interpolation resolution set by *IP* within a single chain interval of 90 angle degrees. *K* is a constant:

$$K = \frac{90}{IP}, \text{ where } IP \text{ is defined in (6). (1)}$$

From the present example of orthogonal sine signals, calculation of the resistivity of the chain resistors in a resistor bridge is:

Signal-angle calculation on an individual resistor tap:

$$\alpha_I = I \cdot K;\ I=1, 2, \ldots, IP, \quad (2)$$

Where the maximal angle is $\alpha_{\max} = 90\deg$, and resistors are:

$$R_I(\alpha_I) = R_V \cdot \frac{\cos(\alpha_I)}{\sin(\alpha_I)+\cos(\alpha_I)};\ 45\deg \le \alpha_I \le 90\deg \quad (3)$$

$$R_I(\alpha_I) = R_V \cdot \frac{\sin(\alpha_I)}{\sin(\alpha_I)+\cos(\alpha_I)};\ 0\deg < \alpha_I < 45\deg \quad (4)$$

$R_I(\alpha_I)$ is the sum of the resistivity of the resistors from *i=1* to *i=I*. Resistivity of a single resistor in a chain $R(r_i)$ is calculated by subtracting all resistors ($R(r_1)$ to $R(r_i - 1)$) from the previously calculated sum.

Resistors are symmetrically positioned from the center of each resistive chain; thus the resistor values are mirrored within a range from 45 to 90 degrees, and all four chains are matched. It is therefore sufficient to calculate resistors in the range from 0 to 45 degrees. It is also sufficient to process the incoming signals within half of their periods (0 to 180 angle degrees), since the same comparators act in the second half-period Fig. (**2**). As shown in the present example for *IP=4*, the resistivity of *r1* is equal to the resistivity of *r4,* the resistivity of *r2* is equal to that of *r3* and so on. The angle resolution in the present example is 22.5 degrees.

In the case of saw-shaped incoming quadrature signals, the relation is:

$$R_I = \frac{R_V}{IP} \text{ and all resistors are of the same resistivity. (5)}$$

The interpolation factor *IP* is defined by the ratio of two periods:

$$IP = \frac{T_{SIN}}{T_{A,B}} \quad (6)$$

T_{SIN} is the period of the incoming sine signals, while $T_{A,B}$ is the period of the outgoing digital-orthogonal signals **Ao** and **Bo**, as shown in Fig. (**2b**), where track signals **Ao** and **Bo** are generated from the comparators' output signals **Fi** and **Gi** Fig. (**2a**).

Lagging or leading of the track signals depends on the current positions of the sine wave signals or, in other words, on the direction in which the measuring-head is moving. Processor input signals contribute equal delay to the generated tracks, so it is important to achieve a constant separation time between digital output edges over the whole input sine wave period. This is very important at high speed movement.

3.1.1. Identifying the Non-Ideality Sources

Although all comparators operate on the same CM level, they differ in performance, which causes INL and DNL errors of the output code (variations of the separation time).

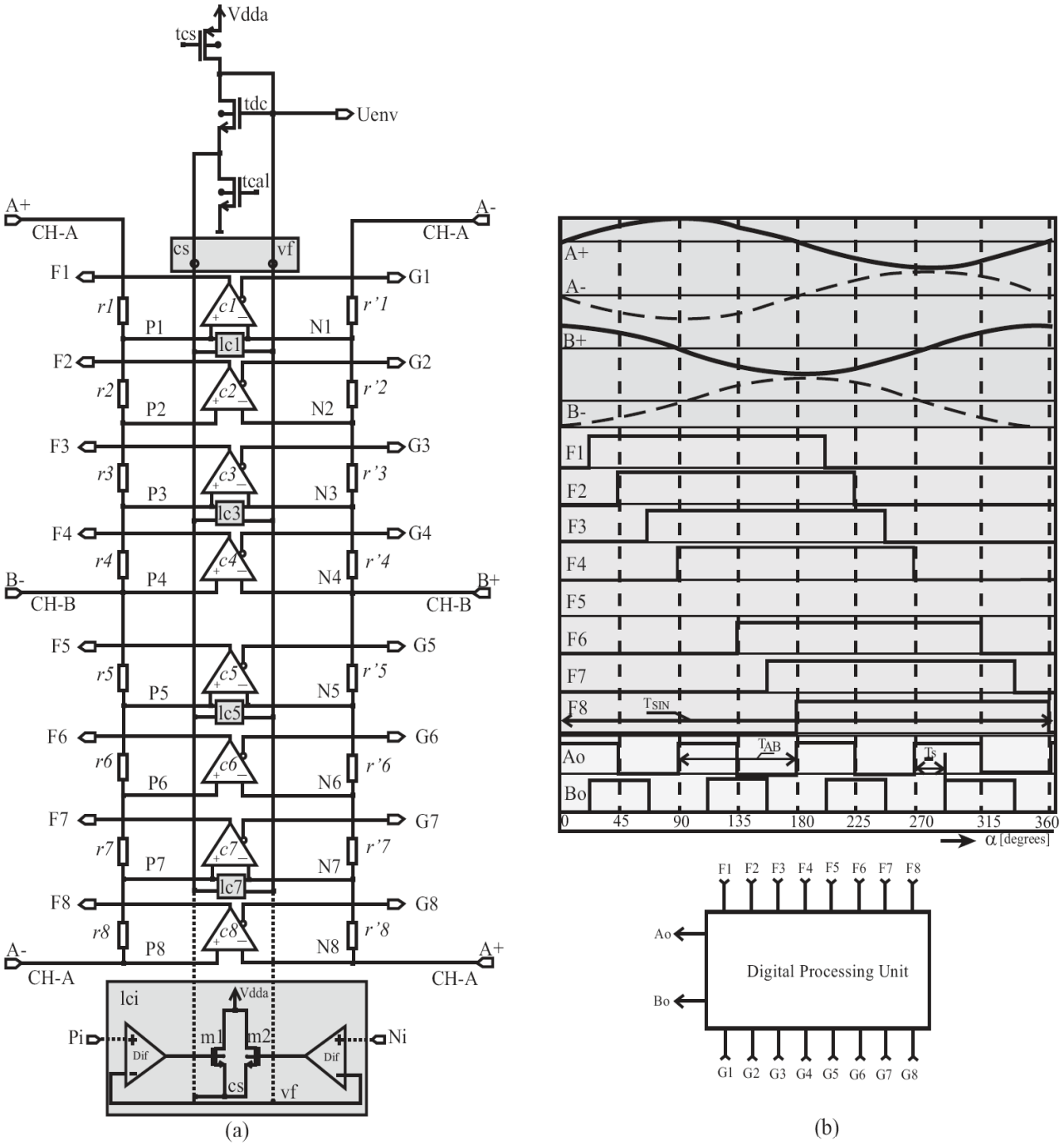

Fig. (2). The linear optical encoder system – principle of operation. The interpolation factor of four is taken as an example, the realization of which is shown in (a). Signals A+, A- and B+, B- are the interpolator's input signals. The interpolator's output signals Fi and Gi are differential–digital signals, generated by the flash A/D converter/interpolator. An XOR in the Digital Processing Unit (b) operates on them to produce a quadrature output signal Ao and Bo. Signals generated at the chain taps P1, P2, P3, P5, P6, P7 and N1, N2, N3, N5, N6, N7 are phase shifted. *The all-follower* common circuit (at the top (**a**) consists of the single load device *tcal*, the level-shift circuit constructed from a diode device *tdc* and the biasing device *tcs*. Topology at the bottom (**a**) shows a distributed amplitude measurement structure within **lc1**, **lc3, lc5** and **lc7**. *Vdda* is positive supply voltage, *vf* is feedback connection and *cs* a common source terminal for all distributed follower pairs, each consisting of two differential amplifiers *Dif* and a follower device *m1* and *m2*.

T_{SIN} is the sine-wave period and corresponds to the grating period RP; T_{AB} is the processor tracks output period and T_S the separation time between the two neighboring edges of tracks Ao and Bo (**b**).

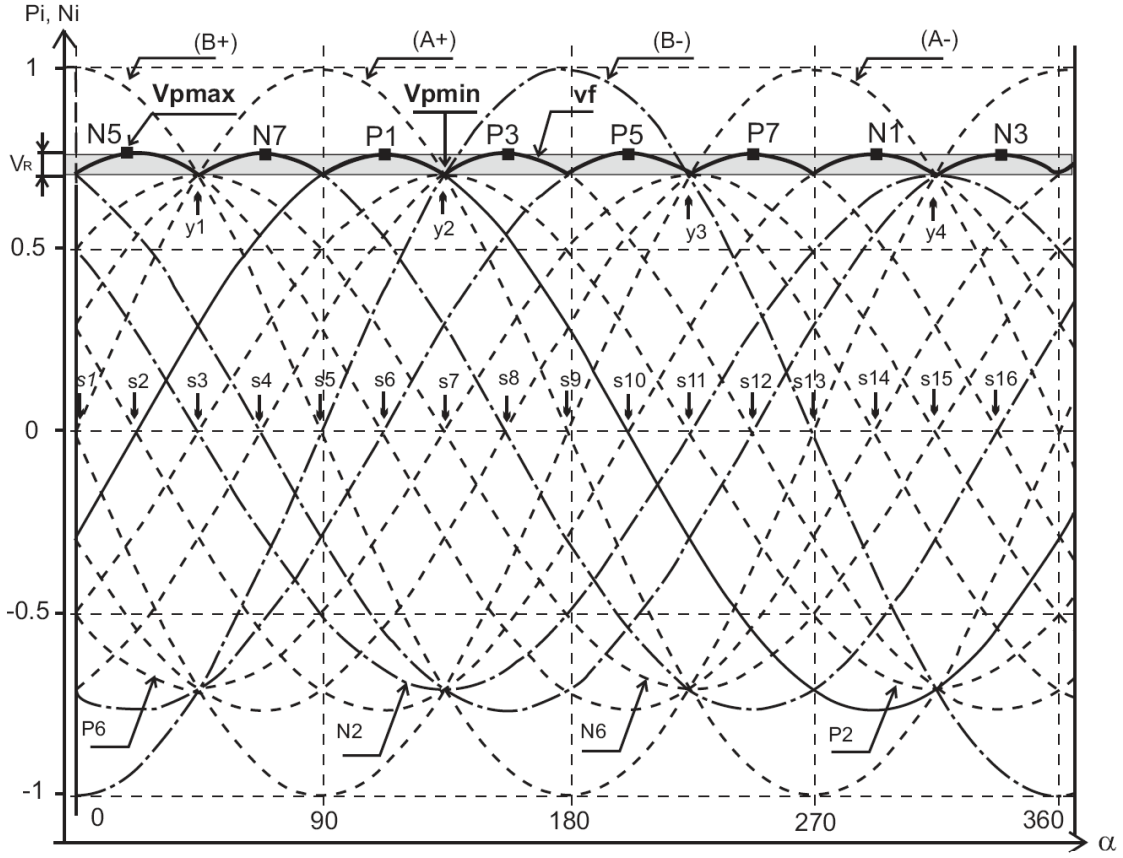

Fig. (3). Simulated waveforms of the phase shifted signals on taps Pi and Ni on the symmetrical resistive bridge of an interpolator from Fig. (**2a**). The shadow area V_R is an envelope range (envelope ripple), showing also local minima and maxima. Signals on taps P2, N2, P6, and N6, as well as input signals from CH-A (A+, A-) and from CH-B (B+, B-), do not contribute to the minimization of the envelope ripple. All signals have the same period and offset as input signals, but differ in amplitude and phase shift.

It is important to note that the comparator's input signals from the resistor taps have different slopes. The offset of the comparators would influence the switching point by the ratio between peak sine signal amplitude and the comparator offset voltage. This impact can be expressed as an angle difference of $d\alpha=\sin^{-1}(Voff)$ (we assume that the peak sine amplitude is 1V). The most critical non-ideality is the comparator offset difference (mismatch). Interpolator linearity is also limited by the resistors' matching requirements. The resistor mismatch directly affects the switching of the comparator. Furthermore, the influence of different non-idealities on the system performance becomes important when a higher order interpolator is an issue (resistor mismatch directly influences tracks separation time). It is therefore important to follow the matching parameter information supplied by an IC manufacturer and design the width of resistors accordingly. Mismatch of the resistors' contacts and taps' resistance are in some cases more important. Therefore, the realization of the current contacts differs from that used only as a voltage tap. Moreover, all the resistors' related layout rules, like dummy material, should also be considered.

The influence of the comparator's delay on the interpolator's performance depends on the scanner speed. The delay degrades the separation time (and the real head position) only minimally at lower speeds, while the effect increases by increasing movement speed. The comparator's delay limits the upper measuring speed. Let us consider this on an example from section 5: the realized interpolation factor of 100 gives 400 transitions per sine signal period (IP=100). Using a grating period of 20μm, a sine signal frequency of 100kHz is achieved by moving the scanner with the speed of 2m/ second. The rate of the track signals Ao and Bo is a 100 times faster and the frequency is 10MHz. The nominal separation time between the two neighboring edges of Ao and Bo is therefore 25ns. At such a high speed, the comparator's delay should not exceed 6 ns (to maintain a minimal separation time of 50% from the nominal one). It is also important to note that the comparator's delay could be much larger; the difference in delays between neighboring comparators should not exceed 6 ns. The position error will accumulate in this case.

Temperature dependence and reliability of the product are the most serious issues in high accuracy motion control.

3.2. Amplitude Measurement

The proposed circuit for measuring amplitude is combined into an interpolator architecture shown in Fig. (**2a**). This results in a compact area-efficient topology that contributes both to better dynamics and better speed performance (lower delays, faster measurement). The interpolator is

therefore a basic structure, upgraded by an envelope detector, the output of which tracks the maxima of relevant signals generated along the resistor bridge. The AMM upgrade consists of distributed voltage followers lc1, lc3, lc5 and lc7, combined to odd comparators *c1*, *c3*, *c5* and *c7* Fig. (**2a**). As described later, only odd comparators handle phase shifted signals having maxima at:

$$P_i, N_i \equiv i \cdot K, \quad i=1, 3, 5 \ldots 2(IP-1) \tag{7}$$

Each follower consists of a differential stage (Dif) followed by a source follower device m1 or m2, the sources of which are connected to a single – active load device *tcal* at the common node *cs* at the top in Fig. (**2a**). The active load structure is common to all followers in the AMM circuit. The drain voltage of the *tcal* device follows voltages on the inputs of the follower devices m1 and m2 from all comparators/followers. Follower feedback voltage, vf, is shifted up by the diode voltage of the *tdc* device, which forces the source voltages of m1 and m2 to be below the gate voltages of m1 and m2 for a diode voltage of the *tdc* device. This action is required for the differential amplifiers *Dif* to be able to compare the input signals to the common feedback signal *cs*, where all input signals have the correct common-mode level. The common source potential, therefore, follows that input voltage on the follower devices m1 and m2, which have the maximum amplitude. Consequently, a higher source potential on node *cs* forces the devices m1 and m2 with lower input amplitudes to the off state. The current source *tcs* provides proper biasing for the diode device *tdc*. The output signal Uenv tracks the input signal on that resistor tap which is currently of the highest amplitude. The potential on node *vf* is therefore the envelope (maxima) of all compared signals and carries useful information about the peak amplitude of incoming signals from channels CH-A and CH-B.

The tracking accuracy depends on differential amplifier gain and offset voltage. All signals within one segment of the bridge cross at the same points (y1, y2, y3 and y4) which are multiples of 45 degrees. The ripple extremes exist at multiples of α=45/2 degree:

$$\alpha = K = \frac{360}{4 \cdot IP} = 22.5 \deg. \tag{8}$$

From this it follows that *IP=4* is sufficient to realize amplitude measuring (AMM) and automatic-gain control (AGC) functions. The extremes of the Uenv envelope are:

- Global minima *Vp*min that are at even multiples of α, where α is 22.5 angle degrees
- Maxima *Vp*max that are at odd multiples of α

As the interpolation factor *IP* increases, the signal amplitudes on the resistor bridge taps closer to input signals increase, while the ripple extremes remain at multiple of the 22,5 degrees Figs. (**3** and **4**). An interpolation factor IP of 4 is therefore optimum for the proposed algorithm. Because the minima are global, a ripple of 5,8% of the peak input amplitude *Vp* is the minimum and is defined as:

$$ripple[\%] = Vrip[\%] = \frac{Vp\max - Vp\min}{Vp} \cdot 100 \tag{9}$$

The *ripple* function $Vrip(\alpha)$ can also be described using a general *modulo* function, valid over the whole signal period:

$$Vrip(\alpha) = Vp \cdot \begin{bmatrix} \sin\left(\alpha\left(\bmod\frac{\pi}{4}\right)\right)\cdot\left(1-\sin\frac{\pi}{4}\right)+ \\ +\cos\left(\alpha\left(\bmod\frac{\pi}{4}\right)\right)\cdot\sin\frac{\pi}{4} \end{bmatrix}, \tag{10}$$

and the extreme functions are:

$$Vrip\_\max(n) = Vrip\left((2n+1)\cdot\frac{\pi}{8}\right) \text{ and is: } 0.76536 \cdot Vp, \tag{11}$$

where maxima are positioned at all odd multiples of $\pi/8$;

$$Vrip\_\min(n) = Vrip\left(2n\cdot\frac{\pi}{8}\right) \text{ and is: } 0.707106 \cdot Vp, \tag{12}$$

minima are positioned at all even multiples of $\pi/8$, where *n* ranges from ….,-2, -1, 0, 1, 2…., and where $\pi/8$ radians is equal to 22.5 angle degrees Fig. (**4**). Any other search for maxima in terms of "searching for minima above global minima" is much more complex and requires much higher speed lc_i circuits, the tracks of which have to be controlled by extra - fast comparators.

3.2.1. Identifying the Non-Ideality Sources

The ripple amplitude is nearly the same at all signal frequencies (simulations for 20 kHz and 100 kHz are shown in Fig. (**4**). Tracking delay of the distributed follower pairs (**lci)** effects track switching and slightly contributes to the average measured signal.

Resistor *r1* mismatches Fig. (**2a**) of 1% and 2% are taken as examples for analysis shown in Fig. (**5**). The larger *r1* resistivity then required slightly reduces the maximum at the corresponding angle position, as is shown in detail on top of the picture (curves *r1_1%_mis* and *r1_2%_mis*). It is evident that the comparator offset cannot affect the sine signals on resistors' taps. On the other hand, the offset voltage of the differential stages Dif drastically affects the envelope extremes. As the Dif is in a source follower configuration, its offset contributes directly to the envelope change with a unity gain as shown in example for 10mV offset (curve *Dif_10mV_offset*) and for -10mV offset (curve *Dif_-10mV_offset*). It is also clear that each Dif stage contributes only at an appropriate angle position area (we put offset voltage to Dif stage, driving m1 in the lc1 block only- Fig. (**2a**). In the present example only the signal from the tap P1, which is processed with **lc1,** is affected Fig. (**5**). As Dif stages have different offset voltages in reality, voltages on resistor taps **Pi** and **Ni** are transformed to output Uenv with additional offset voltages coming from the accompanying **lci** stages. The threshold voltages mismatch of the source follower active devices **m1** and **m2** inside **lci** also contribute to overall **lci** offset voltage with a gain of unity. The overall error of the amplitude measurements is therefore degraded by device mismatch and by offset voltage inside **lci** circuits.

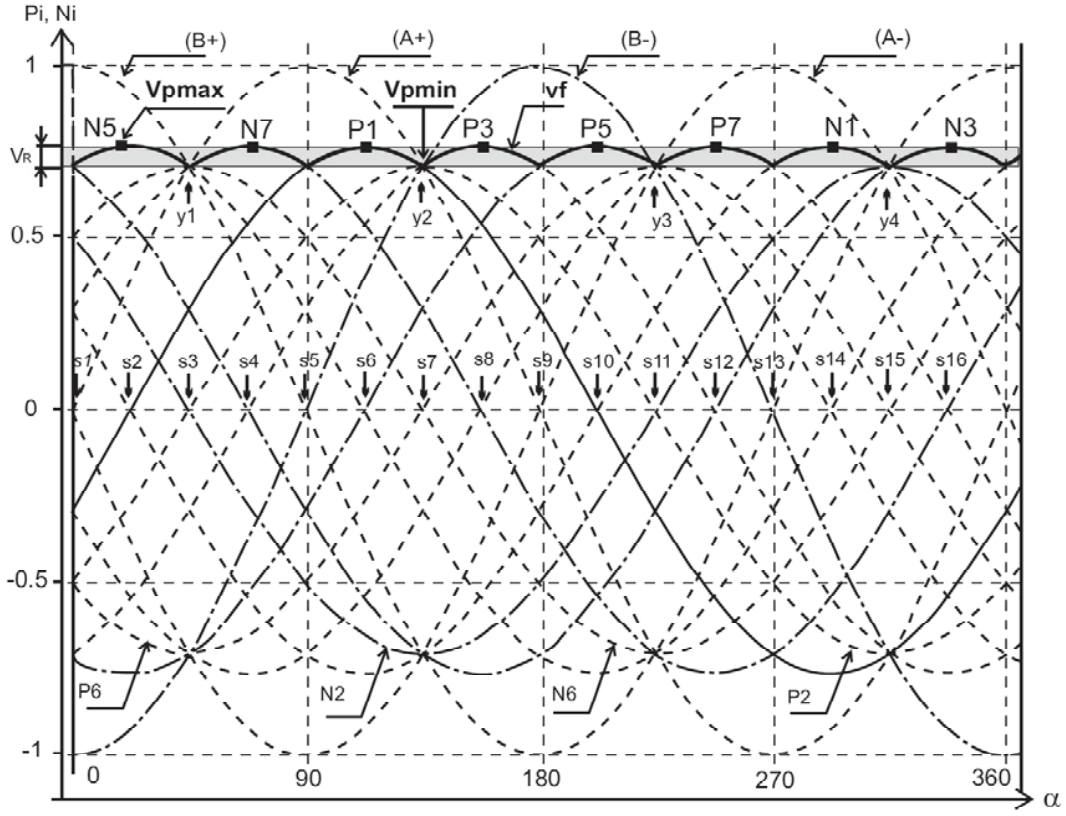

Fig. (3). Simulated waveforms of the phase shifted signals on taps Pi and Ni on the symmetrical resistive bridge of an interpolator from Fig. (**2a**). The shadow area V_R is an envelope range (envelope ripple), showing also local minima and maxima. Signals on taps P2, N2, P6, and N6, as well as input signals from CH-A (A+, A-) and from CH-B (B+, B-), do not contribute to the minimization of the envelope ripple. All signals have the same period and offset as input signals, but differ in amplitude and phase shift.

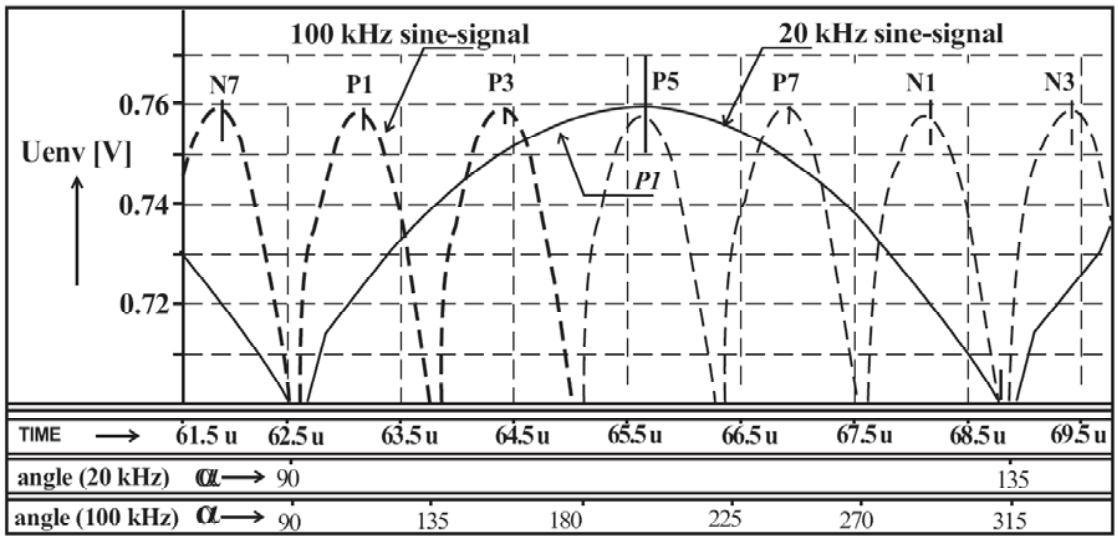

Fig. (4). Envelope voltage peaks (*Vrip*) transformed to output Uenv from the selected chain taps, obtained from simulations for $1V_p$, 20kHz and 100kHz input sine-wave signals.

When measuring the real-time amplitude, the measurement points follow the ripple signal, the amplitude of which is 5,8% of the peak sine signal (Vp) plus ±10mV Dif stage offset and additional ±5mV offset from the MOS device mismatch. In the case of 1V peak Vp amplitude, the worst case offset of ±15mV contributes with additional ±1,5% to intrinsic measurement precision. This is the worst-case scenario. In order to minimize their contribution, appropriate trimming of those four **Ici** blocks needs to be developed.

4. CONCLUSIONS

In general, the *Vrip* amplitude on the Uenv output consists of the full wave rectified AC voltage, the amplitude of which is 5,8% of the input sine peak amplitude *Vp* and is of double the frequency of the original sine signal (10). This AC ripple adds to the DC voltage equal to $(V_P \cdot \sin(45))$ without filtering out the ripple. Only a part of the taps voltages are transformed to output Uenv, ideally voltage the amplitudes of which are above level, defined as $(V_P \cdot \sin(45))$ and form the ripple component in measured information.

The ripple amplitudes (maxima) are the same at all signal frequencies Fig. (**4**). As discussed earlier, tracking delay of the distributed follower pairs (**lci**, i=1, 3, 5, 7) has an impact on switching ripple's minima and therefore may slightly contribute to the average measured signal when the average amplitude within a specified time frame is important. An amplitude integral response over a specified signal bandwidth is usually a more precise measurement which is important for the regulation of signal amplitude for some encoder applications.

Unfortunately, precision of the amplitude measurement is degraded by device mismatch and by the offset voltage inside **lci** circuits Fig. (**5**). When real-time amplitude measurement is the case, the measurement points follow the ripple signal superimposed to DC value. Non-idealities inside **lci** follower stage move the ripple's minima and maxima. The proposed topology inherent ripple of 5,8%Vp is therefore locally degraded. The devices mismatch and Dif stage offset trimming will be essential to provide effective accuracy improvement. There are four **lci** blocks to be considered. On the other hand, the non-ideality inside **lci** circuit has constant and, on the signal amplitude, an independent contribution. Therefore it can be measured and stored after power-up and taken into account instead of being trimmed. Topologies of the regulator AGC of the incoming sine signal depend on the measured principles of the encoder sine signal which could be real time or integral measurement. In this paper we describe the extraction of the flash interpolator's inherent information of the sine signal peak amplitude in the form of DC voltage with a specified ripple that is independent from the signal frequency.

5. EXPERIMENTAL RESULTS

The proposed technique was realized in an ASIC encoder to verify the accuracy of the AMM technique. The realization is an integrated incremental ASIC Fig. (**6**) that uses AMM as the building block. It operates at an input sine wave signal frequency from DC to 100kHz in a temperature range from -40ºC to 125ºC and at a supply voltage of 4.5V±0.5V. Under typical conditions the processed ASIC is fully operational up to 200 kHz.

The opto-sensor array is a separate integrated circuit comprising the reverse biased Si photodiodes and the signal in the form of an electrical current. The light intensity of the LED device is controlled by a part of the generated error signal in the AGC block. The I^2C interface connects the en-

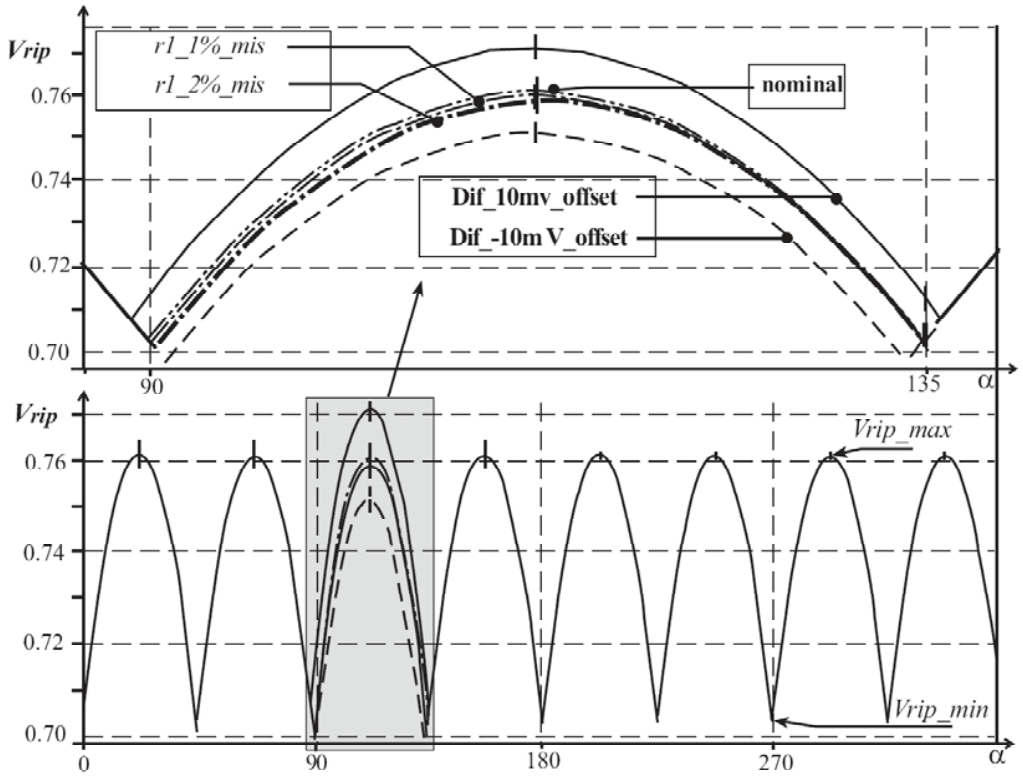

Fig. (5). Simulated envelope voltage, *Vrip*, on Uenv output node at 1V peak sine signal Vp (transformed curve from tap P1 is shown in detail). Example shows worst-case scenario regarding transconductance stage Dif offset voltage and integrated resistors mismatch.

tire circuit to an external EEPROM containing setup data and digital correction information for the sine/cosine amplitude matching control and for the phase difference correction. The measured performances of the AMM are shown in Table **1**. The measured ripple is filtered out at higher frequencies (pad-probe: 300Ω/8pF-1MΩ/90pF) and therefore cannot be reported without filtering action (Table **1**). The recently completed encoder has demonstrated an average THD distortion of less than -60db, measured on monitoring outputs. The result of these measurements is shown in Fig. (**7a**).

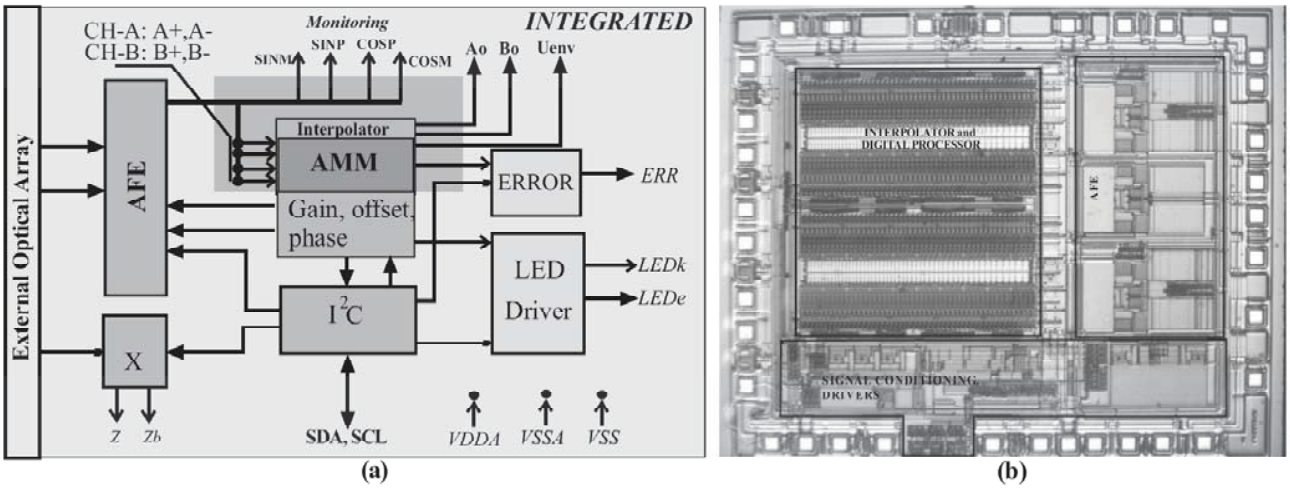

Fig. (6). (**a**) Interpolator ASIC combines a signal conditioning feature, where externally generated input sine signals are applied to the analog-front-end, AFE, and where the AMM module (**am**plitude **m**easurement as part of the interpolator) automatically controls the amplitudes of the incoming orthogonal sine signals to the interpolator circuit. (**b**) Interpolator die photo showing the AFE input on the right, the signal conditioning at the bottom, and the interpolator on the left.

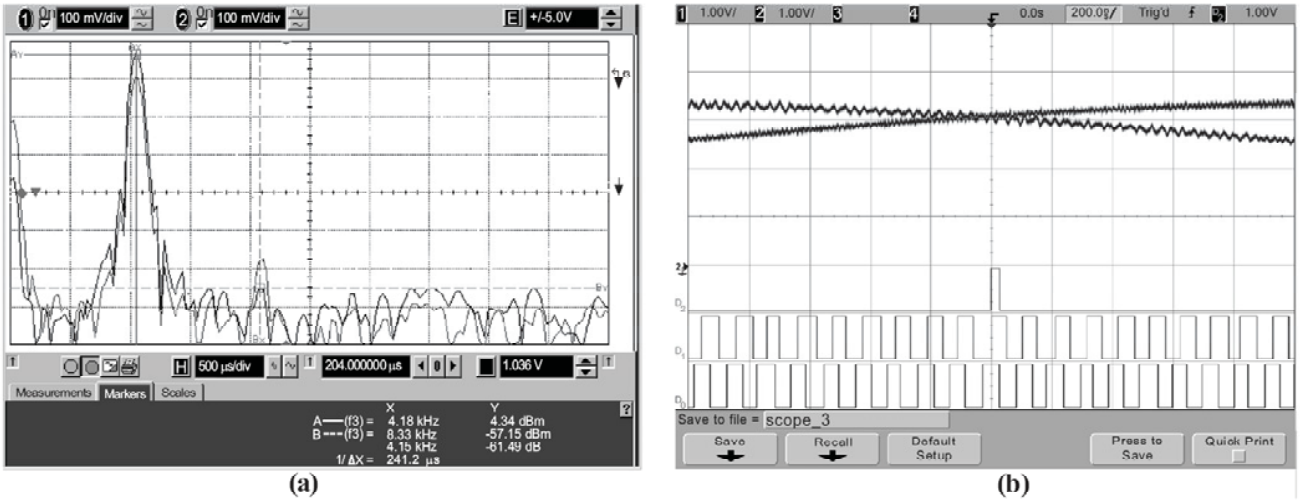

Fig. (7). The sine signal spectrum (**a**), measured on the monitoring output. Differential (SINP/SINM) and single-ended (SINP) measurements are shown. Sine signal frequency, as an example, is 4.18 kHz, As it can be seen from the figure the second harmonic has the highest peak and is below -60dB. (**b**) Measurement of the interpolator at IP=100 and at input sine signal frequency of 100 kHz. The Index is shown in D2, track Ao in D1 and the track Bo in D0.

It is clear that, in practice, the signal conditioning is automatically deactivate when the scanner is moving fast, simply because the measurement, and therefore the interpolation, should not be disturbed by the automatic AMM and AGC. The amplitude measurement and regulation are running within a certain frequency window and that range has to be monitored simultaneously. The result of 5,8% ripple represents an optimum and the minimum for the flash interpolator we proposed. The peak-sine measurement accuracy of 5,8% for the AGC function is sufficient for most industrial applications. If an integral measurement over a longer time frame is recommended for specific applications, averaging of Uenv gives a very precise measurement of the amplitude information. A comparison with the fastest industrial interpolator available is given in Table **2** [26, 46, 47].

Table 1. Simulated Versus Measured AMM Output Signals

Sine/Cosine Frequency [kHz]	Sin/Cosine Peak [mV]	Ripple (Simulated, Uenv Loaded by Chip Pad – 300Ω/7pF)		Ripple (Measured, Uenv Additionally Loaded by the Probe – 1M/90PF)	
		Vrip_Min [mV]	Vrip_Max [mV]	Vrip_Min [mV]	Vrip_Max [mV]
0.1	500	352	383	352	383
1	100	74	80	74	80
1	500	352	383	352	383
20	1000	707	757	709	755
100	1000	705	758	740	740

Table 2. A Comparison of the Proposed Interpolator ASIC with Other Interpolators. The Parameters in the Table are Valid Under all Specified Conditions – Over Specified Temperature and Supply Voltage

Feature	This Work	[46]	[26]	Comments
Max. Interpolation factor IP	100	64	64	Data for Ic-TW2 are taken from data sheet [47].
Sine-cosine frequency at max. IP	100 kHz	115 kHz	75 kHz	
Amplitudes adjust	Automatic	Programmable amplifiers gain	Programmable with two external resistors	

6. CURRENT & FUTURE DEVELOPMENTS:

The aim of this work was to find a cost-effective and area-effective method of generating peak amplitude information from sine wave signals. The major part of the amplitude measurement and envelope extraction is already inherent in the presented flash interpolator and only minor additional electronics has been added. Another goal of this work was to improve the quality of the quadrature signals required to enable higher interpolation factors and higher encoder resolution.

The amplitude information, when evaluated, shows the following: if the AC part of the information is larger than the expected 5.825 % ripple (seen at lower head moving speeds only), it results from the sine-signal-pair to cosine-signal-pair amplitude mismatch (assuming that non-idealities described in Section 3 and 4 have been compensated). To implement a precise amplitude correction, matching of the quadrature sine signals prior to AGC is necessary. Moreover, appropriate comparator circuits that weight the measured signal amplitudes to predefined values need to be designed, having the hysteresis ratiometric generate signal amplitude to overcome undesired ripple at lower signal frequencies. It is also important to regulate sensor supply and light intensity parameters prior to AGC (based on AMM measurement) to maintain the design requirements for the dynamic range. All Improvements mentioned above may further accelerate the actual measuring resolution of the integrated encoder's SoC in CMOS technology down to nanometer range.

The proposed solution for AMM is much more robust than that using a square circuit to generate DC voltage out of sine and cosine signals. The amplitude measurement described in this paper is an inherently linear process that generates envelope by using the same signal processing path as the interpolator itself. Interpolator monotonicity is guaranteed by the proposed architecture.

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