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VSEBINA CONTENT

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COHERENT CURRENT VOLTAGE CHARACTERISTICS OF TRIPLE BARRIER RESONANT TUNNELING DIODES AS IMPROVEMENTS OF STANDARD DOUBLE BARRIER DIODES

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Key words: Resonant tunneling, double barrier diode, triple barrier diode, current voltage characteristic, negative differential resistance

Abstract: In double barrier resonant tunneling diodes (DBRTD) as well as in other small period number structures coherent electron transport dominates the total current through the structure. Since coherent transport is a result of a resonant tunneling phenomenon we can use transmission spectra to derive current density vs. voltage characteristics. The topic of our study is to improve an initial DBRTD by increasing two of the most important parameters of RTDs: peak current density and peak-to-valley ratio (PVR) defining a negative differential resistance region. In order to provide assistance in experimental efforts to design resonant tunneling systems with optimal peaks, both in the transmission spectrum and the current density, we attempt to explore whether the observations seen for the DB diode hold as well for the triple barrier (TB) diode. In this paper we show that by using TBRTDs with an increased barrier height improvements of the initial DBRTD structures are possible. We show the influence of broad resonant peaks of an anti-reflection coating in TBRTD structures on the increase of the peak current density. This extra current density can further compensate an increase of the barrier height that increases the PVR and the operating temperature of the structure.

Koherentna tokovno-napetostna karakteristika diode z resonančnim tuneliranjem s tremi barierami kot izboljšava standardne diode z dvema barierama

Ključne besede: Resonančno tuneliranje, dioda z dvema barierama, dioda s tremi barierami, tokovno-napetostna karakteristika, negativna diferencialna upornost

Izvleček: V strukturah z dvema barierama (DBRTD – Double Barrier Resonant Tunneling Diode) kakor tudi v ostalih strukturah z majhnim številom period, katerih osnovni način delovanja temelji na principu resonančnega tuneliranja, prevladuje koherenten način transporta elektronov po strukturi. Ker je koherentni transport plod fenomena resonančnega tuneliranja, lahko na osnovi prepustnostnega spektra strukture določimo odvisnost tokove gostote od napetosti. Predmet naše raziskave je izboljšati lastnosti neke začetne DBRT diode tako, da povečamo dva najpomembnejša parametra diod z resonančnim tuneliranjem: vrhnjo tokovo gostoto in razmerje med vrhnjo in dolinsko vrednostjo tokove gostote (PVR – Peak-to-Valley Ratio). Oba parametra v največji meri določata območje negativne diferencialne upornosti. Z namenom zagotavljanja pomoči eksperimentalnim naporom pri načrtovanju sistemov z resonančnim tuneliranjem, ki bi imeli optimalne vrhove tako v prepustnostnem spektru kot vrhove tokove gostote, smo poskušali raziskati, ali lastnosti DB diod veljajo tudi za diode s tremi barierami (TB). V tem delu predstavljamo, da lahko z uporabo TBRT diod s povišanimi barierami izboljšamo lastnosti začetne DBRT diode. Prikazujemo vpliv širokih resonančnih vrhov TBRT diode s protiodbojno zaščito na povečanje vrhnje tokove gostote, ki omogoči povečanje višine barier ter s tem PVR-ja. Diode z višjimi barierami pa lahko delujejo pri višjih temperaturah.

1. Introduction

Despite the fact that approximately 30 years have passed since the pioneering theoretical and experimental work on resonant tunneling in semiconductor heterostructures by Esaki, Chang, and Tsu /1, 2/, there is still a significant amount of research in this field, which is being sparked by new technical advances in the nanofabrication of these semiconductor heterostructures /3/ and the potential exploitation of the physics of resonant tunneling in producing solid-state devices.

The basic resonant tunneling diode (RTD) device configuration is a double barrier (DB) heterostructure of nanometer dimensions, including two heavily doped semiconductor contact layers to provide low-resistance made from a degenerate *n*-type semiconductor with a relatively small bandgap, e.g. GaAs, (Fig. 1a). These layers comprise the emitter and collector region on both sides of the DB, respectively. Barriers are made from a semiconductor with a relatively large bandgap, e.g. $Al_xGa_{1-x}As$, and in particular a positive conduction-band offset E_B with respect to the smaller bandgap semiconductor. Between the two barriers is the quantum well made again from the smaller bandgap semiconductor. The structure is explained in terms of a conduction-band energy diagram since we are interested in the electron transport process. Because the characteristic dimensions of the DB structure are comparable with the electron wavelengths, the wave nature of electrons leads to quantum phenomena such as interference, tunneling, energy quantization, etc. /4/. As a result, resonant tunneling phenomena occur and form the basis of RTD operation.

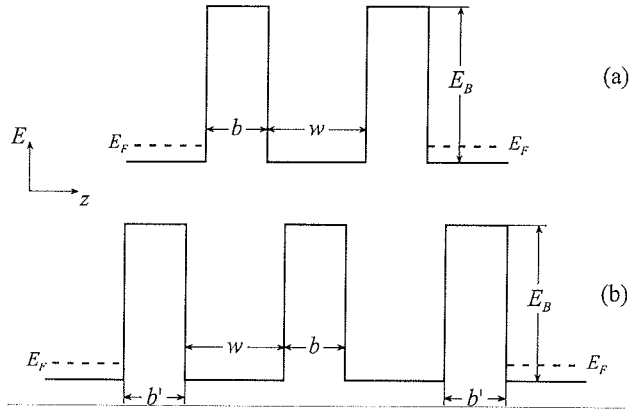

Figure 1: Conduction-energy-band diagram of (a) DBRT and (b) TBRT structure. b *and* w *denotes the barrier and well width, respectively, while* E_B *is the barrier height. For the emitter and collector region Fermi energy* E_F *is shown. In (b)* b' *denotes the outermost barriers width.* z *is spatial coordinate.*

While much of the initial research efforts lie in understanding the physics of resonant tunneling in DB structures, there has been increased experimental /5/ and theoretical /6/ research on resonant tunneling in triple-barrier (TB) semiconductor heterostructures (Fig. 1b). The physics of resonant tunneling in these systems is much more than an extension of the results of the DB case, since it involves the coupling of quasibound states between the two adjacent quantum wells in the semiconductor heterostructure /7, 8/. In particular, while there have been a number of theoretical calculations on the physics of resonant tunneling in DB semiconductor heterostructures in an effort to understand the experimental results /1, 2, 9/, there has been very little theoretical work on systematic understanding of the effects of non-equality of barriers and wells (width and height, respectively) in TB systems /10/. We show that a colorful range of the transmission spectra and corresponding current densities of different TB structures can be constructed. Performed calculations attempt to explore whether the observations seen for the DB diode also hold for the TB diode, while providing theoretical assistance in experimental efforts to design resonant tunneling systems with optimal peaks, both in the transmission spectrum and current-voltage characteristic, respectively.

In this paper we study electron transport by using a coherent model /4, 11, 12/, where particles maintain their phase coherence across the whole structure before losing energy in the contacts (transversal energy and phase coherence during the tunneling process are conserved). As a further approximation we assume that the contacts are perfectly absorbing. This means that when a particle injected from one side reaches the contact region of the other side its phase coherence and excess energy are lost through inelastic collisions with the Fermi sea of electrons in the contact. Thus we assume that an electron injected from one contact at a certain energy E has a certain probability $T(E)$ of being transmitted through the barriers, exits with the same energy and transverse momentum, and finally is absorbed in the opposite contact, where it loses the energy and memory of its previous state. In coherent models electronic conduction in quantum systems is represented by the Landauer and Büttiker /13, 14/ formulation based on the transmission coefficient $T(E_z)$. In this work we use a scattering matrix model /11/ to calculate $T(E_z)$. The transmission $T(E_z)$ as a function of the longitudinal electron energy is the probability ratio of transmitted and incident waves of a particular electron state, which is equivalent to the ratio of the transmitted and incident electron flux. $T(E_z)$ can be calculated from the wave functions available in the solution of the Schrödinger equation. Current flow in this picture is essentially the net difference between the number of particles per unit time transmitted to the right and those transmitted to the left. The current density can be evaluated using the Tsu-Esaki formula /2/ that is obtained by summing the current density of each state over the occupied states multiplied by their transmission probability:

$$J_{total} = \frac{qm^* k_B T}{2\pi^2 \hbar^3} \int_{E_C}^{\infty} T(E_z) \cdot \ln\left(\frac{1+\exp\left(\frac{E_F - E_z}{k_B T}\right)}{1+\exp\left(\frac{E_F - E_z - qV}{k_B T}\right)} \right) dE_z, \quad (1)$$

where q is elementary charge, m^* effective mass, k_B Boltzmann's constant, T temperature, $\hbar$ Planck's constant/2π, E_F Fermi energy, E_z electron's energy in the longitudinal direction, V applied bias, and E_C bottom of the conduction band. The logarithmic term is sometimes called a supply function /15/, since it more or less determines the relative weight of available carriers at a given perpendicular energy and is obtained by integrating over the transverse momentum. This results in a three-dimensional treatment of electron states. In our model space-charge effects are not considered.

In real devices the difference between the measured and calculated results for J_P and PVR can become quite significant, and the voltage range for the occurrence of the Negative Differential Resistance (NDR) does not correspond exactly /16/. Part of the latter problem may be explained by including a series resistance /17/. However, this does not rectify the other discrepancies, particularly the magnitude of J_P which becomes larger than in ideal - coherent - model /16/. The physical processes involved in RTD operation are actually much more complex than the preceding simple description and are especially complicated by the electron's interaction with its environment. The extra valley current represents contributions due to scattering of electrons /18/. Elastic scattering in RTDs may be nominally associated with interface roughness at the heterojunction interfaces, unintentional doping in the tunneling region, impurities, and alloy disorder. Inelastic scattering via phonons and collective excitations do not only break

the assumption of electron energy and transverse momentum conservation but lead also to loss of total phase coherence /11/. The tunneling in both cases can be no longer characterized as coherent, since scattering allows relaxation of the parallel-momentum conservation rule and thus increases the amount of current that may flow off-resonance. Therefore, it can be concluded that the origin of the NDR requires energy and momentum conservation as a condition.

Nevertheless, coherent models representations are in general sufficient to reveal the idea of RTDs operation, especially when small period (barrier + well) number structures /7, 10/ with thin wells and barriers are considered, sometimes when symmetric structures are studied /19/, and in all structures where the mean free path of the electrons is larger than the dimensions of the RT structure (long scattering times) /19, 20/. In these cases scattering can be neglected and coherent models may be applied /8, 20/.

2. DBRT Diodes

Let us start with two DBRT diodes comprised of GaAs/$Al_xGa_{1-x}As$ layers, where the Al composition x was equal to 0.30 and 0.45, respectively. The conduction band offset (barrier height E_B) for those materials is equal to 0.288 and 0.432 eV, while the widths of one well w (GaAs) and two barriers b ($Al_xGa_{1-x}As$) were chosen to be 3.0 and 3.5 nm, respectively. To account for non-parabolicity due to the multiband effects present in the structures /21/ we included in our numerical model energy dependent effective masses $m_{b/w}(E)$ /22/. The temperature and the difference between the Fermi energy and the bottom of conduction band in a degenerate semiconductor were set to 4.2 K (temperature of liquid helium) and 46 meV, respectively. Throughout this work present set of parameters is used unless specified differently.

As seen in Fig. 2, with a positive bias applied to the collector relative to the emitter (contact emitting electrons), the resonant energy level in the quantum well (E_1) approaches the Fermi energy in the emitter increasing the number of electrons that can tunnel. By increasing the bias, the Fermi energy passes through the resonant state making a large current flow due to the increased transmission from the emitter to the collector. At the same time, the back flow of carriers from the collector to the emitter is suppressed as electrons at the Fermi energy in the collector see only a large potential barrier. At a point where the resonant energy aligns with the bottom of the emitter conduction band (Fig. 2b) the number of tunneling electrons per unit area reaches a maximum. Further bias pushes the resonant level under the bottom of the emitter conduction band (Fig. 2c) and cuts-off the electrons coherently tunneling through this resonant state. The supply of electrons is than cut-off. The tunneling current density has therefore a sharp drop from its peak value giving rise to a pronounced region of NDR. A further increase of the bias enables the enhancement of tunneling through higher resonant levels increasing the number of current density peaks. Those current peaks are much higher and wider due to much broader resonant peaks (RPs), which broaden with increasing energy and/or bias. For that reason, the NDR region can become very small. In real devices where scattering is present the NDR region for higher resonant peaks is rarely observed /16/. The current peaks are additionally affected by an increasing temperature that lifts up the electron distribution in the emitter and leads to an increased electron thermionic emission and tunneling through and above the top regions of the barriers /23/. Therefore, we concentrated our study around the first current peak followed by the first NDR region. This is where RTDs are usually used /16, 24/.

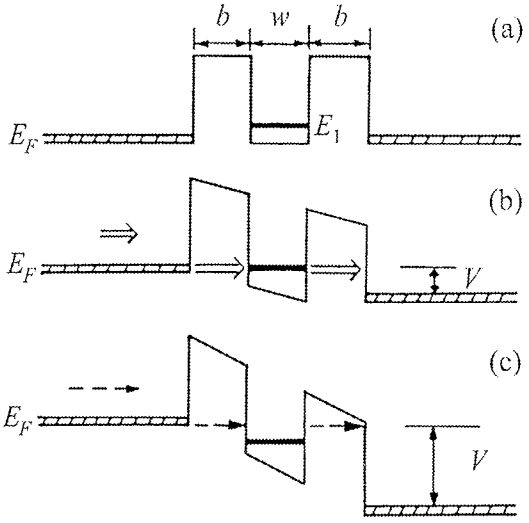

Figure 2: Conduction-energy-band diagram of DBRT structure with three different applied biases.

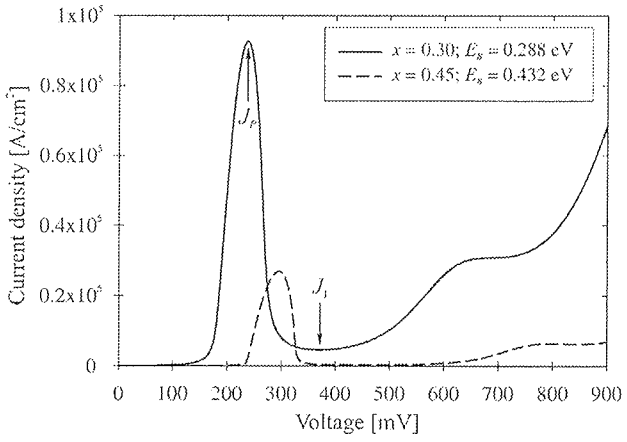

Figure 3: Calculated coherent J(V) characteristics of DBRTD (w = 3 nm and b = 3.5 nm) with Al composition x = 0.30 (E_B = 0.288 eV) and x = 0.45 (E_B = 0.432 eV) at T = 4.2 K are shown by solid and dotted line, respectively.

In Fig. 3 we show the calculated current density vs. voltage characteristics for two DBRTDs with different Al compositions (x = 0.30 and x = 0.45) at T = 4.2 K. We can see that the higher the barriers the smaller the peak current density J_P and the higher the Peak-to-Valley Ratio [PVR = J_P/J_V, where J_V is the valley current density (the minimum current density following J_P by increasing the voltage)] (Table 1). The reasons can be found in the transmission spectrum (TS) of the structures. They show that higher barriers (HB) lead to sharper resonant peaks, although the number of resonant peaks in the quantum well is increased /12/. For most applications /24/, NDR devices such as RTDs should exhibit high J_P and PVR. They both depend physically on the Fermi energy in the emitter and hence the doping there as well as on the temperature /12, 23/. By increasing either of them J_P would increase, while the PVR would decrease until the NDR effect would completely vanish. The reason is in an increase of the resonant tunneling current through higher energy levels, non-resonant currents between the resonant levels, and thermionic emission over the barriers /12/.

For RTDs basically three parameters are important: J_P, PVR, and Voltage Peak-to-Valley Ratio (VPVR) (Table 1). The latter is defined as a ratio between the voltage at J_P (peak voltage V_P) and at J_V (valley voltage V_V) (VPVR = V_P/V_V,). Therefore, the higher the VPVR (approaching toward unity) the steeper the NDR region (with respect to the PVR). A high VPVR is very important for fast logic circuits /25, 26/.

Table 1: J_P, PVR, V_P, and VPVR of DBRTDs from Fig. 3.

x	J_P [10^5 A/cm^2]	PVR	V_P [mV]	VPVR
0.30	0.93	20.18	238	0.64
0.45	0.27	96.20	296	0.67

By using the coherent model we studied different TBRTDs and compared them to DBRTDs. Our main goal was to find a structure, either with two or three barriers, where at the same time the J_P and the PVR would be higher than in the initial (first considered) DBRTD. If possible, in the real device scattering mechanisms should be reduced also compared to the initial DBRTD.

3. TBRT diodes

By studying the coherent picture of TBRTDs the operating principles of DBRTD can be followed. Usually, TBRTDs are used for generating multiple NDR characteristics for multiple-valued logic circuits /25, 26/. In our study the TBRTDs were used in order to improve the coherent $J(V)$ characteristic of the DBRTDs. The novel idea was to vary the width of the two outermost barriers b' of TBRTD structures (Fig. 1b).

In coherent models most of the physical behavior is represented by the transmission spectrum. Fig. 4 shows the transmission spectrum of GaAs/$Al_{0.3}Ga_{0.7}As$ TBRTDs, where the outermost barriers width b' is varied from 0.4 to 4 nm. From the figure it is evident that for thicker outermost barrier widths there are two resonant peaks with a transmission probability equal to unity. As b' decreases, the two peaks forming a quasi-miniband gain stronger coupling. This means that the peaks lie closer to each other, while the valley value between them increases. At a point where b' becomes equal to one half of the central barrier width ($b' = b/2$ - in our case 1.75 nm) both peaks join and form a single resonant peak with a transmission probability equal to unity. Such a b' was presented as an Anti-Reflection Coating (ARC) /27/. We name the whole structure "ARC-TBRTD". By further decreasing b', the two resonant peaks coupled in one peak start loosing their high transmission probability as well as their sharpness (loosing Lorentzian line-shape /28/).

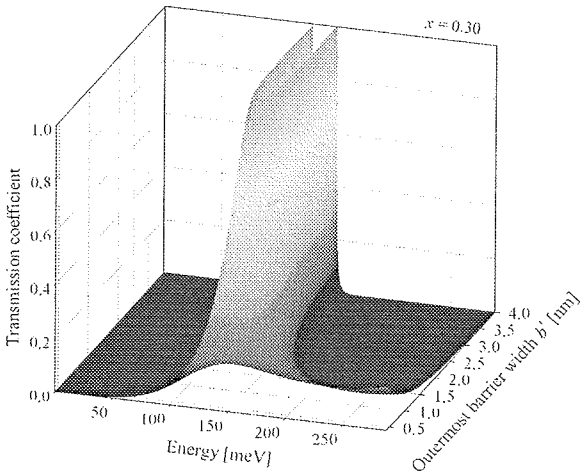

Figure 4: Transmission spectrum for GaAs/$Al_{0.3}Ga_{0.7}As$ TBRTDs with w = 3 nm, b = 3.5 nm *and* b' *varies from 0.4 to 4 nm (no applied bias).*

Another very important parameter for studying TBRTDs is the area under the resonant peaks. In Fig. 5 the area is shown for the structures in Fig. 4 (the area is taken between the energies where the transmission coefficient equals 15%). For real device applications the structure should exhibit the highest J_P with respect to as high PVR as possible. Since a high area under the resonant peaks results in a high J_P, the ARC structures with the highest area are one of the most promising structures. Beside that, the ARC structures can have a relatively high PVR. The reasons lie in the TS. In the ARC structure two coupled resonant peaks form one resonant peak that is much broader than the single resonant peak of the DBRTD, while it is still very steep and has a high transmission probability (Fig. 4). This has many effects on $J(V)$ characteristics of real devices. First of all, the structures can operate at higher temperatures while still exhibiting an NDR region [for x = 0.30 structures, going from 4.2 to 300 K, the PVR of the ordinary ($b' = b$ = 3.5 nm) TBRT device decreases by 57%, while for the ARC-TBRTD ($b' = b/2$ = 1.75 nm) it

decreases for only 9%; the PVR of the DBRT decreases by 63%] /23/. Next, since elastic scattering additionally broadens the resonant peaks in the TS, real devices with broader peaks are relatively less affected by the scattering /12/. For this reason, the operating temperature of the ARC-TBRTD devices can be further increased. In the contrary, for outermost barrier widths smaller than $b/2$, the shape of the resonant peaks (Fig. 4) changes in a way that non-resonant currents are increased (currents not passing through the resonant peaks). The structures can be therefore used only at low temperatures /23/. Finally, b' of the structure should not be too small in order to maintain a steep NDR region (Fig. 6).

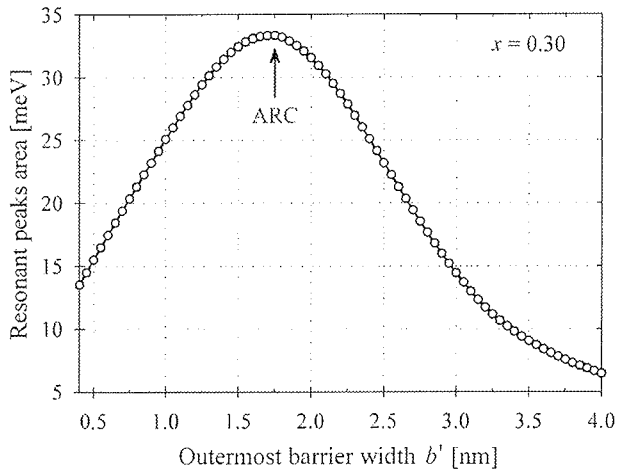

Figure 5: Area of resonant peaks from Fig. 4 vs. b' at zero bias.

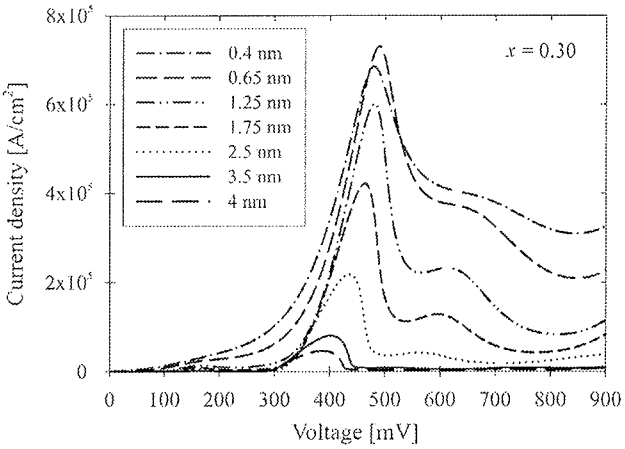

Figure 6: Calculated coherent J(V) characteristics of GaAs/Al$_{0.3}$Ga$_{0.7}$As TBRTDs with w = 3 nm, b = 3.5 nm and b' between 0.4 and 4 nm (T = 4.2 K).

In Fig. 6 we show coherent $J(V)$ characteristics of TBRT diodes with different b'. It is evident that as b' decreases the NDR region gets less pronounced, making the structures less interesting as RTD devices /29/ (Table 2).

Table 2: J_P, PVR, V_P, and VPVR of TBRTDs from Fig. 6.

b' [nm]	J_P [10^5 A/cm^2]	PVR	V_P [mV]	VPVR
0.4	6.85	2.22	480	0.57
0.65	7.30	3.49	488	0.58
1.25	6.00	2.71	480	0.85
1.75	4.22	3.76	464	0.86
2.5	2.18	6.14	436	0.86
3.5	0.80	10.32	402	0.85
4	0.46	12.49	388	0.84

Since the VPVR of the DBRTD that we use in our study as an initial device is not a critical parameter (0.64 for x = 0.3 and 0.67 for x = 0.45) and can be easily obtained with TBRTDs, our detailed analyses concentrate on J_P and PVR, respectively (Fig. 7).

From the study of J_P in Fig. 7a it can be concluded that by changing b' the current density peak varies. By decreasing b' the J_P increases until it reaches a maximum and starts decreasing. For small temperatures /23/ (like in our case where T = 4.2 K) the maximum J_P is not necessarily achieved for the ARC structure (Fig. 7a). This is due to the splitting of the coupled resonant peaks, although the area of the peaks for zero field has a maximum there (Fig. 5). The same holds for the PVR /23/. From Fig. 7b it is evident that by decreasing b' the PVR decreases up to a point where it has a sudden and sharp increase, and after which it decreases again. For TBRTD structures with x = 0.30 the increase of the PVR is at approximately b' = 0.85 nm, which means that the best trade-off between the J_P and PVR is not achieved for an ARC structure ($b' = b/2$). By increasing the height of the barriers (in order to maintain a direct semiconductor x must not be higher than 0.45 in the $Al_xGa_{1-x}As$ system) the increase of the PVR shifts to higher b'. Our detailed analyses showed that by increasing x the highest PVR is achieved for $b' \approx b/2$ (in our case b' = 1.75 nm for x = 0.45). This means that also for lower temperatures the ARC structures can exhibit the best trade-off between the J_P and the PVR.

The reason for the sudden increase of the PVR can be again found in the TS. We have already explained that in the TBRTDs the two resonant peaks couple and form single peak. When a bias is applied these coupled peaks start to split. For that reason the $J(V)$ characteristics can exhibit more current peaks with different heights and widths. These peaks shift their position by changing b'. All this has a big influence on the valley currents. They are composed of the resonant currents as well (the calculated coherent characteristics match better to the measured results) /30/. In this way for a range of b' higher PVRs can be achieved.

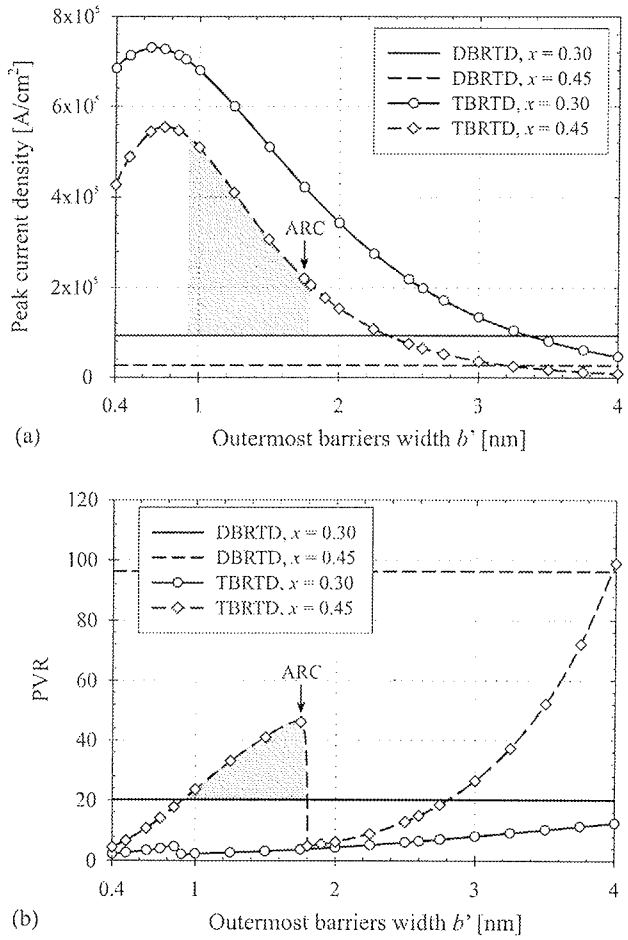

Figure 7: (a) J_P and (b) PVR vs. b'. In both plots the horizontal lines show values of the DBRTDs with different Al composition (different E_B), while symbols connected with an eye-guide line represent the values calculated for the TBRTDs (again for two different E_B). Gray shaded areas show the outermost barrier widths region (0.9 nm < b' < 1.75 nm), where the TBRTDs with x = 0.45 exhibit an improved characteristics with respect to the DBRTD with x = 0.3. (T = 4.2 K)

4. Comparison of structures

Consider the DBRTD with $x = 0.3$ (solid horizontal line in Fig. 7a and b) as an initial structure and compare it to the TBRTDs with different b' and $x = 0.3$ as possible improvements (circles in Fig. 7 connected with a solid eye-guide line). We can see that for $b' < 3.35$ nm the J_P of the TBRTD is higher than 93 kA/cm^2 but the PVR is in the whole studied range smaller than 20.18 (values of J_P and PVR are for the DBRTD - Table 1). The same is for higher b', where the PVR of the TBRTDs becomes higher than in the DBRTD (not shown in the Fig. 6) but the J_P becomes smaller. Therefore, it can be concluded that from a coherent point of view by changing only b' of the TBRTDs it is not possible to construct a structure that would exhibit higher J_P and PVR (at the same time) as they are in the DBRTD with the same b, w, and E_B.

In order to find a structure with improved $J(V)$ characteristics we increased the barrier height. The dashed horizontal lines in Fig. 7 show J_P and PVR of the DBRTD with $x = 0.45$ (Table 1). While the PVR of the latter structure equals 96.20 and is much higher than in the DBRTD with $x = 0.3$ this is not true for the J_P, which is now only 27 kA/cm^2. So again, the DBRTD with $x = 0.3$ cannot be improved by increasing E_B alone.

Finally, we increased E_B of the TBRTDs ($x = 0.45$) (diamonds in Fig. 7 connected with a broken eye-guide lines). It can be seen that the peak current densities decrease and the PVRs increase (a linearly increasing E_B results in a linearly decreasing J_P and an exponentially increasing PVR. This makes structures with higher barriers more interesting as devices /23/). The results of the comparison show again that no TBRTD with $x = 0.45$ has higher J_P and PVR at the same time than the DBRTD with $x = 0.45$. But on the other hand, a comparison between the TBRTDs with $x = 0.45$ and the initial DBRTD with $x = 0.3$ shows that for b' between 0.9 nm and 1.75 nm the J_P as well as the PVR are higher. Only in this way we have at the same time managed to increase the J_P and the PVR of the DBRTD with $x = 0.3$ by using the ARC-TBRTD with $x = 0.45$ from 93 kA/cm^2 and 20.18 to 220 kA/cm^2 and 46.22, respectively.

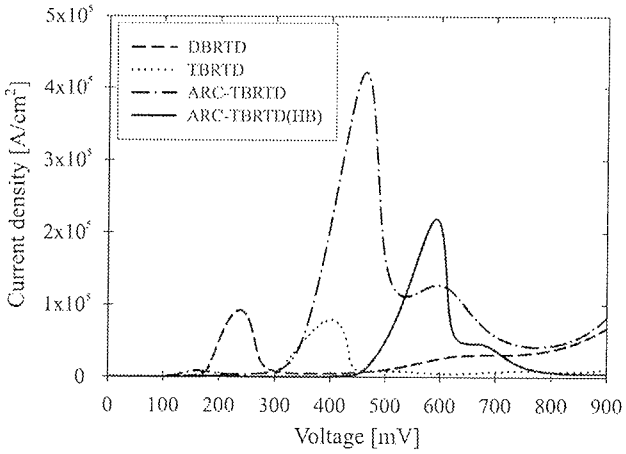

Figure 8: Calculated coherent J(V) characteristics of DBRTD, TBRTD, and ARC-TBRTD all with x = 0.3, and ARC-TBRTD with x = 0.45 (HB); T = 4.2 K.

Fig. 8 shows the final comparison of the coherent $J(V)$ characteristics between the initial DBRTD with $x = 0.3$ and the different TBRTDs that were studied in order to find an improved RTD [TBRTD and ARC-TBRTD both with $x = 0.3$, and ARC-TBRTD(HB) with $x = 0.45$]. It can be seen that for all TB structures the current density peak emerges at higher biases than for the DB structure and that for the structure with higher barriers the peak lies at even some additional bias. It is important to note that all TBRTDs ex-

hibit steeper NDR region than the DBRTD, which is advantageous in fast logic circuits /29/.

Our quest to find an improved structure treated many RTDs with different well and barrier widths. The results show that an improvement of $J(V)$ characteristics is possible only for structures where the barrier width slightly exceeds or is approximately equal to the well width.

5. Conclusions

The most important parameters of RTDs are a high J_P and a high PVR. Both are usually predefined by the device specifications and are especially hard to meet at higher temperatures (200 K and more). The key idea of this paper is how to use TBRTDs in order to improve the coherent $J(V)$ characteristics of DBRTDs. For that reason we have studied different double and triple barrier structures by means of coherent modeling approach, which is applicable for low temperatures. From our analyses it can be concluded that the coherent current-voltage characteristic of the DBRTD cannot be improved only by using the TB structures by itself, nor only by increasing the barrier height. In order to increase both, the J_P and the PVR of the DBRTD, TB structures with different outermost barrier widths and increased barrier height have to be considered.

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ULTRA LOW NOISE PAGC AMPLIFIER FOR MICROSYSTEM SENSOR SIGNAL PROCESSING

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Key words: low noise amplifier, automatic gain control for programmable temperature coefficient (PAGC), microsystems

Abstract: One of the key properties of the microsystems is the quality of the front-end sensor signal processing. Typically a fully differential input and output stages are required for most of the analog signal processing to maintain the best possible rejection of the unwanted signals.

The design of such amplifier is discussed in this article. Special attention is paid to the offset voltage minimization, 1/f noise and thermal noise minimization. Temperature dependent Programmable Automatic Gain Control (PAGC) is incorporated to allow for sensor temperature coefficient compensation. Amplifier parameters are measured and characterized on the realized ASIC.

Ekstremno malošumni PAGC ojačevalnik za procesiranje senzorskega signala v mikrosistemih

Ključne besede: malošumni ojačevalnik, avtomatska regulacija temperaturnega koeficienta (PAGC), mikrosistemi

Izvleček: Ključna lastnost v mikrosistemih je kvaliteta procesiranja vhodnega senzorskega signala. Običajno zahtevamo vhodno stopnjo z diferencialnim vhodom in izhodom. Na ta način zagotovimo najboljše slabljenje neželjenih signalov. V članku je prikazana izvedba takšnega ojačevalnika, kjer sta minimizirana šuma 1/f in termični šum. Temperaturno odvisna avtomatska regulacija ojačenja z možnostjo nastavitve PAGC omogoča kompenzacijo temperaturnega koeficienta senzorja.

Rezultati simulacij in meritev na izdelanem ojačevalniku so podani v članku.

1. Introduction

The target was the amplifier with minimal input noise, differential input stage and single-ended output. The output signal has to be around the reference level V_{ref}.

The most commonly used answer to a problem is combination of either four input amplifier or combination of two unity gain input amplifier and the output stage. In both cases the input noise contribution is the sum of four input transistors together with resistor noise. A solution where the noise contribution is only the noise of two input transistors and the resistor noise is minimised to a negligible level is presented. The front-end block diagram is shown in figure 1.

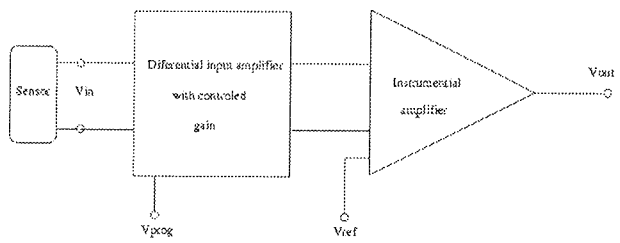


Fig.1: Front-end block diagram

2. Differential input amplifier

Selected topology of the differential amplifier with controlled gain is shown in the figure 2.

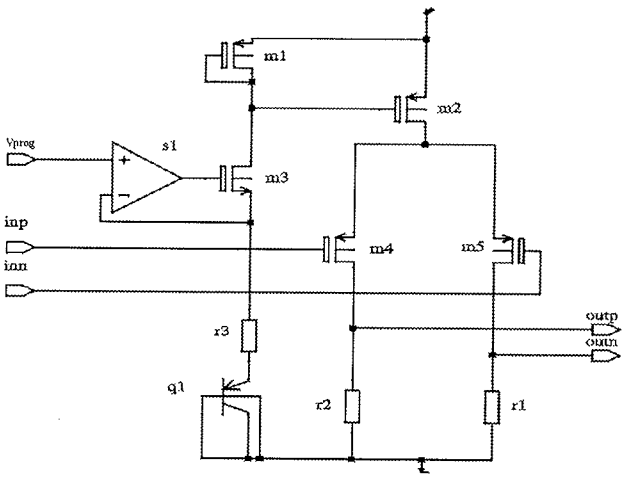


Fig. 2: Differential amplifier

It consists of the differential input transistor pair m4 and m5 and load resistors r1 and r2. The bias generator is made of bipolar transistor q1, resistor r3, MOS transistors m1 and m3 and sub circuit s1 for driving the transistor m3.

The bias generator, its influence and main proprieties is described in section 3. The dimensions of differential pair and bias current are calculated to obtain 26dB gain i.e. 20dB at each output.

The target 1/f noise density of differential amplifier at 1 kHz is less than 7nV/√Hz; the target thermal noise density level at 100 kHz is less than 5nV/√Hz and the gain-bandwidth product over 100MHz.

2.1 Noise characteristic

Several simulations were made to analyze the influence of the input stage transistor type on noise performance. The amplifier was intended to be used in a magnetic microsystem where the equivalent noise resistance of the sensor was 1kΩ. In all simulations and measurements this equivalent noise resistor was included.

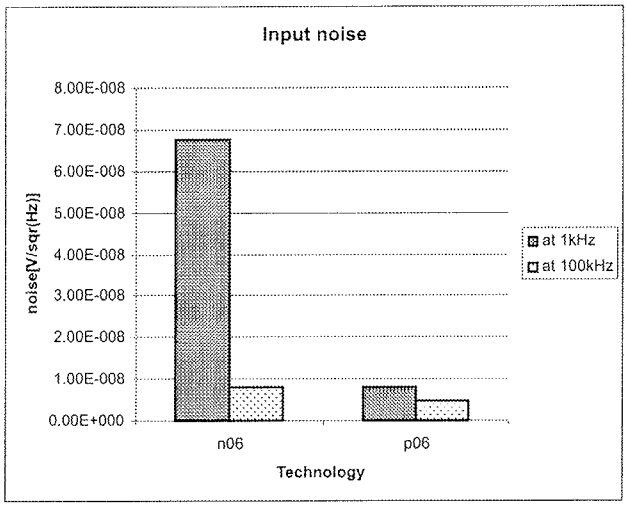


Fig. 3: Noise density for n-type input transistor stage (n06) for p-type input transistor stage (p06)

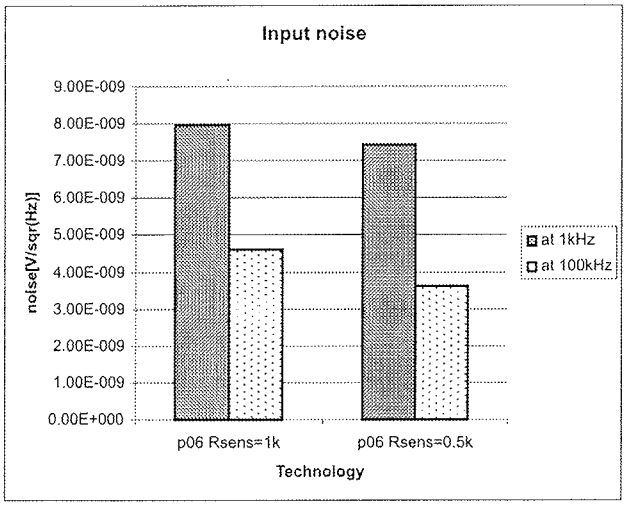


Fig. 4: The influence of equivalent noise resistance of the microsensor

The analyses were made for 0.6μm technology. It was found out, that p-type transistor input stage, using the same transistor sizes, has lower noise than the n-type. Figure 3 presents simulation results for p and n-type input stage. As shown, the noise level for n-type input differential stage is around 68nV/√Hz, and for p-type stage 7,9nV/√Hz at 1kHz (1/f noise mainly). At 100kHz (thermal noise) the noise density levels are 8.1nV/√Hz for n-type and 4.6nV/√Hz for p-type. Even with lowest noise level around 24nV/√Hz at 1kHz for n-type input stage could be achieved.

Figure 4 shows the noise density level at different sensor equivalent noise resistances. As expected, the sensor resistance value has major influence on thermal noise (100kHz). The thermal noise level of the system for 1kΩ sensor equivalent noise resistance is 4,62nV/√Hz and 3,62nV/√Hz for 0.5kΩ sensor equivalent noise resistance.

2.2 Comparing technologies

The basic proprieties of the input differential stage for different technologies have been analysed. Figure 5 shows the noise density level of input differential amplifier in 0,35um, 0,6um and 0,8um CMOS technology. The comparison is done for p-type input stage transistors due to better performance. As expected 1/f noise (at 1kHz) level is lower with smaller technology; meanwhile the thermal noise (at 100kHz) doesn't change a lot. The noise level varies from 5,27nV/√Hz for 0.35um technology, up to 8,95nV/√Hz for 0.8um technology. The thermal noise is around 4.65nV/√Hz, for all technologies.

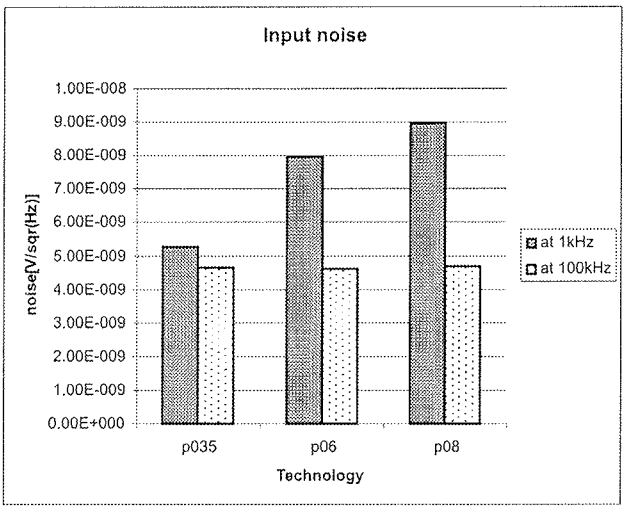


Fig. 5: Noise at different technologies

The influence of different technologies on gain has been analysed. For these simulations the dimensions of input differential transistor pair were modified to achieve the same input capacitances, to compensate the gate oxide thickness change with the technology. For example, the thickness of gate oxide for 0,8um technology is 18nm, for 0,6um technology 12nm and for 0,35um around 15nm. In 0,35um technology, the thickness is larger due to the use of tran-

sistor with mid-gate oxide, operating at 5V. Figure 6 shows the gain for different technologies with p-type input transistors and for comparison the 0,6um n-type input transistor stage is added. As seen, the gain doesn't vary a lot with technologies. As expected n-type input stage has a higher gain factor.

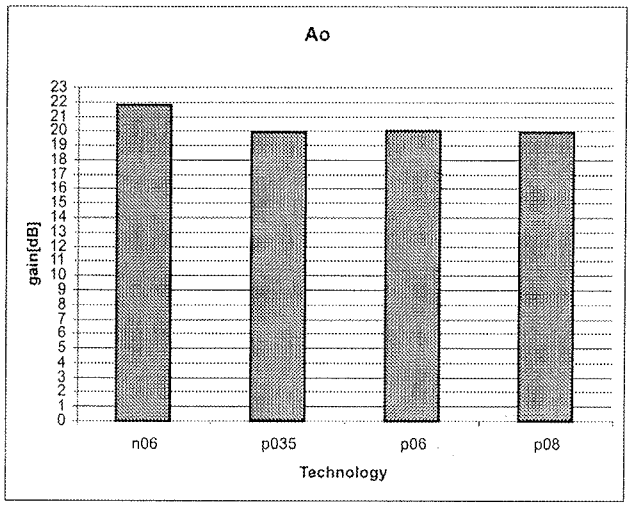
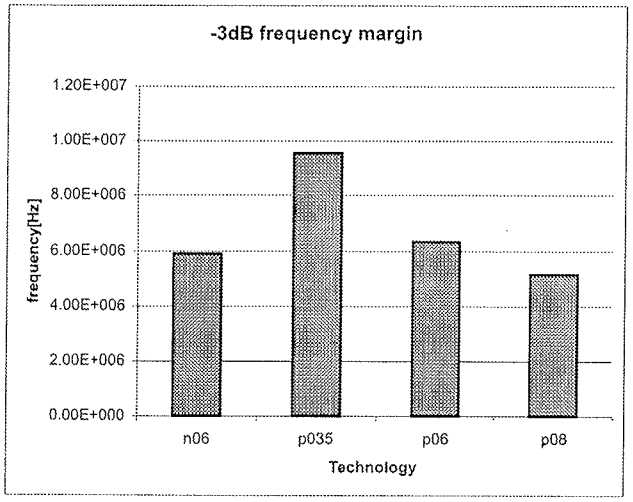


Fig. 6: Gain at different technologies



Fig, 7: -3dB frequency margin

Variation of -3dB frequency margin is shown in figure 7. As shown, n-type of input stage doesn't have the best performance. The best technology is 0,35um where gain-bandwidth product over 190MHz has been achieved.

2.3 Performance of the selected differential input stage

Due to the best performance the p-type input differential stage in 0,35um technology was chosen for our system. Several analyses with different corners (worst cases of technology parameters) have been performed in the temperature range between -20°C and 100°C.

In figure 8, the results for temperature sweep are presented. The gain variation for technology corners *wp* (worst power), *ws* (worst speed), *wz* (worst n-type transistors) and *wo* (worst p-type transistors) can be observed.

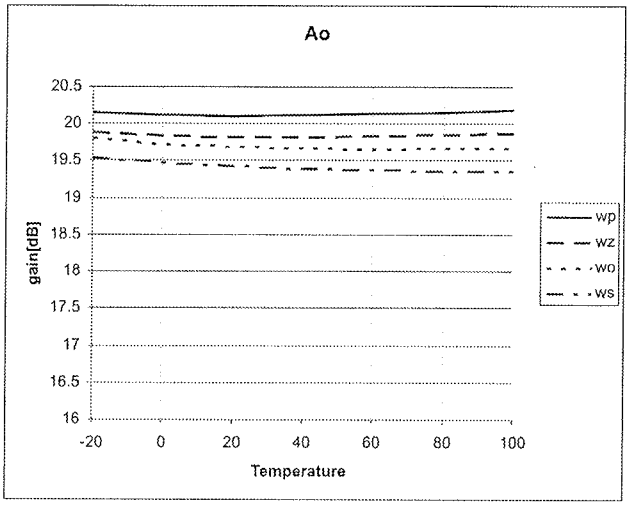


Fig. 8: Gain variations with temperature and process corners

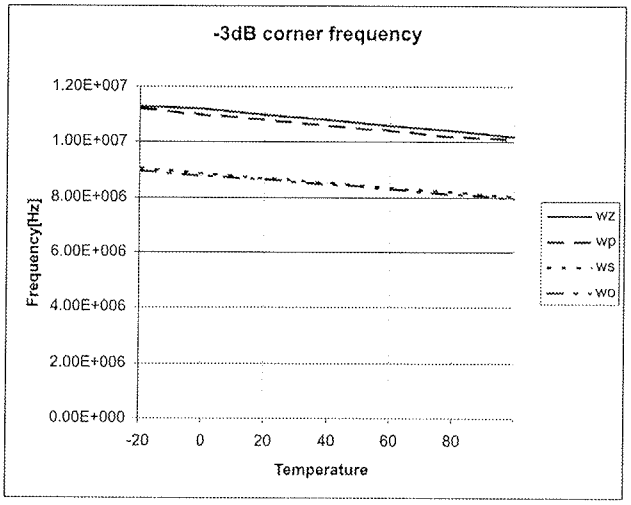


Fig. 9: -3dB corner frequency as a function of temperature and process corners

As shown, in the worst case the gain of the input stage drops to the lowest value around 19,4dB at worse speed parameters and at the highest temperature.

The lowest -3dB corner frequency is 8MHz at worst p-type transistors condition at high temperature. This corresponds to the worst case gain-bandwidth product of 156MHz. The level of input noise density at 1kHz (1/f noise) is shown in figure 10.

When changing the corners there are no noticeable influence to the noise density level. However noise density at 1kHz changes with the temperature from 4,75nV/√Hz to 6,12nV/√Hz, and from 4.25nV/√Hz to 5,25nV/√Hz at

100kHz as seen at figures 10 and 11, in the temperature range of 120 °C.

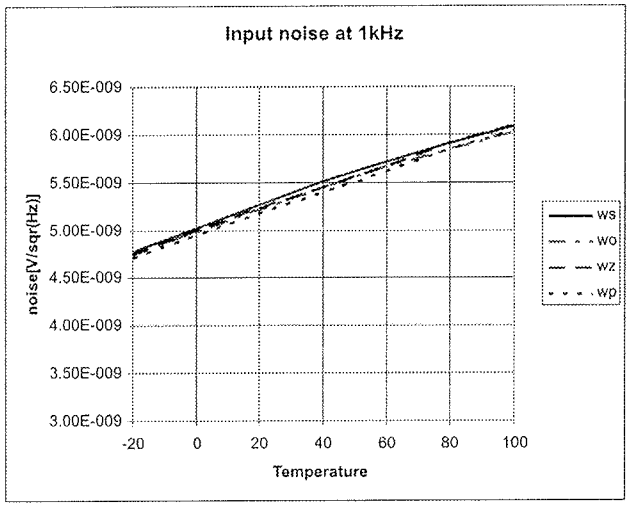


Fig. 10: Input 1/f noise

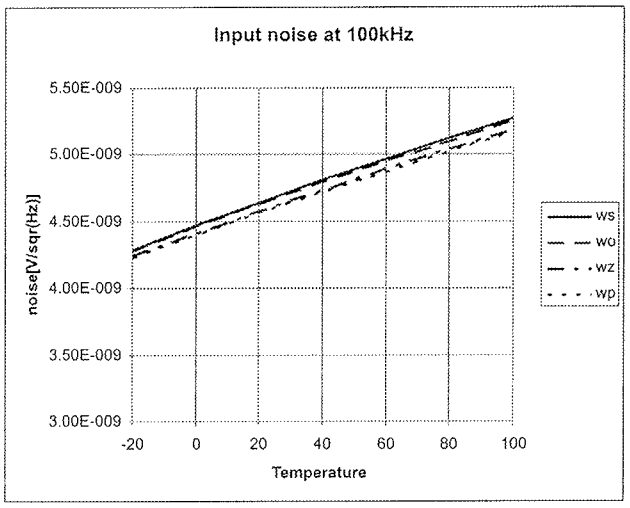


Fig. 11: Input thermal noise

3. Programmable automatic gain control

The programmable bias generator is used to control the gain of the amplifier and to compensate the temperature dependence of the proposed amplifier and of the microsensor.

Special attention was paid to the design of relevant components of the bias generator to minimize its influence to the overall noise. The topology of the bias generator is shown in figure 12.

Minimization of the noise influence is taken care by appropriate sizes of the transistors m1 and m2. The temperature coefficient of the bias current is set by the appropriate selection of the reference voltage and the value of resistor r3.

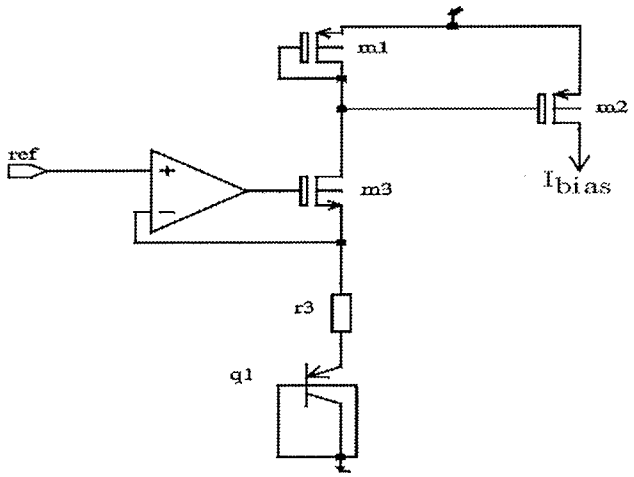


Fig. 12: Bias generator

Figure 13 shows the temperature behavior of the bias current for all corners.

When selecting such temperature dependence of the bias current we obtain minimal gain variation of the amplifier as seen in the figure 8. The sensor temperature coefficient can be programmed by the control voltage on the Prog input. The temperature dependence of the bias current is given by the expression:

$$I_b(temp) = \frac{V_{prog} - V_{be}(temp)}{r_3(temp)}$$

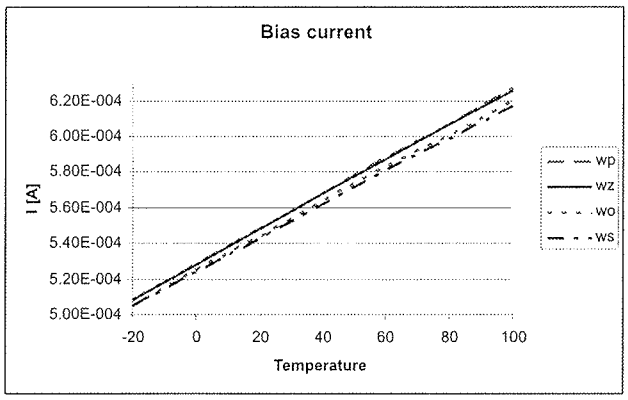


Fig. 13: Bias current

As both the temperature dependance of the V_{be} and r_3 are known for a given technology the wide range of bias current temeprature dependance can be achieved by changing the programming voltage V_{prog}.

The measured results for noise density are shown in figure 14 compared to simulation results. A perfect matching with simulated results has been observed also in other amplifier characteristics.

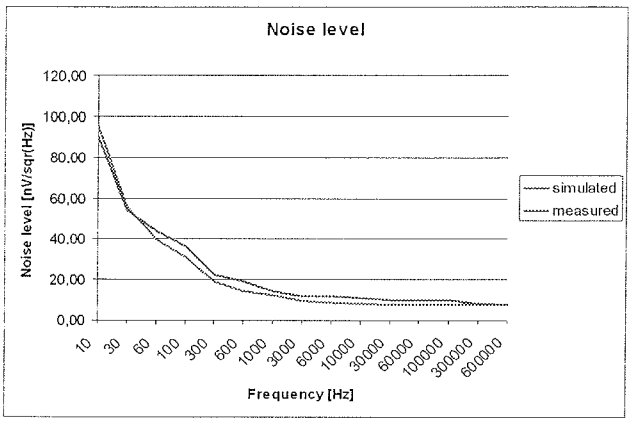


Fig. 14: Measurement results compared to simulation results

4. Conclusion

A minimal noise and offset input amplifier with automatic temperature controlled gain has been introduced. It has been shown, that n-type transistors have larger noise than p-type transistors. When using smaller technology, 1/f noise is decreasing for the same silicon area. Very low 1/f noise density level of 5,27nV/√Hz at 1kHz typical and 4,65nV/√Hz thermal noise density typical with dominant contribution of the sensor equivalent noise resistance has been achieved. The microsystem sensitivity is temperature stabilized by the use of special programmable bias current generator. Typical sensitivity variation of the system with temperature is 70ppm/°C. Typical gain-bandwidth product is 190MHz.

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A SYSTEMATIC APPROACH TO REAL-TIME IMAGE SEGMENTATION IN FPGA DEVICES

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Key words: image processing, image segmentation, FPGA

Abstract: Image segmentation is an important step in image processing and recognition. Processing in real time introduces additional demands, which constrain our ability to choose between segmentation techniques and hardware architectures. The existing literature only describes very specialized image segmentation solutions. This paper introduces a systematic approach to processing block design, which facilitates the selection of a suitable segmentation technique and its adaptation to an FPGA implementation. Research into the published segmentation techniques and existing FPGA solutions enabled us to propose a system architecture suitable for effective implementation of most segmentation techniques. We also present a methodology to search an optimal technique for real time segmentation. The proposed approach has the advantage that it is not constrained to a specific image segmentation area. This wide design space enables us to use the methodology to find an optimal solution for each specific implementation example.

Sistematični pristop k segmentaciji slike v realnem času z vezji FPGA

Kjučne besede: obdelava slik, segmentacija slike, FPGA

Izvleček: Segmentacija slike je pomemben korak pri postopkih avtomatske obdelave in razpoznavanja slike. Pri obdelavi slik v realnem času imamo dodatne zahteve, ki močno zožijo izbor pomembnih tehnik segmentacije in strojne arhitekture. V obstoječi literaturi najdemo rešitve za segmentacijo slike v realnem času za ozko določena področja uporabe. V članku je predstavljen sistematičen pristop k načrtovanju procesnih blokov, ki olajšuje izbiro segmentacijske tehnike in njeno prilagajanje implementaciji z FPGA vezji. Na osnovi pregleda segmentacijskih tehnik in obstoječih rešitev v FPGA vezjih smo določili arhitekturo sistema, ki omogoča učinkovito implementacijo večine segmentacijskih tehnik. Predstavljena je metodologija iskanja optimalne tehnike za izvedbo segmentacije v realnem času. Prednost prikazanega pristopa je v tem, da ni omejen na specifično področje uporabe segmentacije. Ker imamo širok načrtovalski prostor, lahko z uporabo metodologije iskanja pridemo do optimalne rešitve za vsak konkreten primer uporabe.

1 Introduction

Image segmentation has been around for about 40 years and can be considered a relatively mature part of the computer vision. A multitude of segmentation techniques exists, suitable for everything from handwriting recognition to automated vehicle guidance. But there is a rift between research and practical use: the more sophisticated techniques seem to be rarely used in real life /1/. This results in very strict requirements for the imaging part of computer vision systems and limits introduction of computer vision to everyday life.

While several problems are to blame for this situation, one seems to be crucial: advanced image segmentation techniques require impractical amounts of conventional computing power to produce results on traditional CPUs in real time - they have reached the limits of the Von Neumann bottleneck /2/. Designing in the domain of FPGA circuits provides a way to break this barrier /3/: most segmentation techniques can effectively be parallelized in hardware.

A systematic approach to implementation of the image segmentation techniques on FPGA systems does not yet exist. The majority of existing papers only deals with implementation of a particular image segmentation technique as a tailored part of the system (e.g. autonomous robot), and only relatively simple segmentation techniques are used (see /4/, /5/, /6/). Furthermore, these implementations usually aren't reusable. We therefore propose a systematic approach which represents a framework for future implementations and takes into account existing approaches and hardware/software co-design methodologies.

2 Classification of image segmentation techniques

2.1 General overview

Table 1 presents an overview of the segmentation techniques divided into classes.

The technique classes are not sharply delineated and very frequently, customized combinations of techniques are used to achieve best performance for a given application. The presented overview shows:

- image segmentation techniques have pronounced advantages and drawbacks,
- most technique classes already have been efficiently mapped to FPGA devices.

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Table 1: Overview of image segmentation techniques

Segmentation technique class	Advantages	Drawbacks	Applications	Efficient FPGA implementations exist
Global thresholding	very fast, lowest resource consumption	sensitive to uneven illumination, limited application area, no spatial information considered, sensitive to noise	document imaging, fingerprint recognition	yes
Local thresholding	fast, low resource consumption, less sensitive to uneven illumination	limited application area, sensitive to noise	document imaging, fingerprint recognition	yes
Watersheds	correct placement of boundaries, fast	usually requires subsequent region merging step to reduce over-segmentation, sensitive to noise	medical imaging, face detection, content-based image retrieval (CBIR), surveillance	yes
Region growing	tolerant to noise, connected edges, custom similarity criteria can be used	computationally expensive, sensitive to seed selection	medical imaging, image compression, motion estimation, CBIR, face detection	yes
Split-and-merge	segments objects on different scales (pyramid structure)	requires post-processing, slow convergence, computationally expensive	range images, aerial photographs, radiography	no
Clustering	custom similarity criteria can be used, can detect small variations	sensitive to noise, no spatial information considered, user must specify number of clusters in advance, computationally expensive	range images, satellite images, medical imaging, CBIR, robot vision, non-destructive testing (NDT), scene analysis	yes
Model based	tolerant to noise, takes into account a-priori information	very computationally expensive	medical imaging	no
Statistical	extremely general, tolerant to noise	very computationally expensive	CBIR, medical imaging, road segmentation, face recognition, robot vision, satellite imaging, NDT	yes
Neural network based	fast, tolerant to noise	large sample set required for training, computationally expensive	medical imaging, CBIR, NDT, road segmentation, face recognition, robot vision	yes
Fuzzy set based	tolerant to noise	very computationally expensive	medical imaging, CBIR, road segmentation, NDT, robot vision	yes
Physics based	proper segmentation of highlights	very computationally expensive, restricted set of materials	satellite images, visual inspection	no

2.2 Existing classifications

The papers describing the image techniques usually lack comprehensive comparisons with other techniques, especially regarding the execution efficiency. Only few papers offer direct comparison and classification of image segmentation techniques:

In an early comparison /7/, desirable characteristics of segmentation are defined: uniformity and homogeneity of regions, simple regions without many holes, clear differences between adjacent regions and spatially accurate, non-ragged boundaries.

In /8/, techniques are classified and compared. Objective evaluation of segmentation techniques is discussed and some general criteria for quality of segmentation (correlation, uniformity and entropy) are given.

In /9/, color representations are discussed, with emphasis on perceptually uniform color spaces. The segmentation techniques are divided into feature-space (clustering and thresholding approaches), image-domain (split-merge, region growing and edge based approaches), neural network classification, and physics based techniques (using

reflection models), with discussion on individual techniques in the different classes.

In /10/, color segmentation techniques (including texture segmentation) are overviewed and pre- and post-processing is discussed. An array of techniques is then implemented in software, tested on natural images, and carefully compared.

We propose the creation of a classification of image segmentation techniques, where the performance of these techniques for different application areas is evaluated. This will allow the designer to objectively compare different techniques and choose the one most suitable for his application.

2.2.1 Technique comparison

The scope of usability of a technique is usually already defined by the author of the technique. Detailed comparison should therefore be limited to techniques that are a priori suitable for a certain application area, using a performance metric to make an objective comparison.

In /11/, the evaluation methods for image segmentation techniques are divided into two types: the analytical and empirical methods. The analytical methods are not very common, due to the lack of formal image segmentation theory, so only few examples are given. The empirical methods are divided into goodness and discrepancy methods. The goodness methods evaluate desirable properties of segmentation technique, while the discrepancy methods compare the actual segmentation results with "ideal" segmentation, usually defined by a human. Different empirical methods are then compared and the discrepancy methods are found to be more powerful.

We propose that discrepancy metrics, customized for different application areas, are used to compare the segmentation techniques. After evaluating a particular segmentation technique, its strong and weak points should be clearly outlined. This will enable the designer to select the optimal technique for the proposed application.

3 Processing structure of segmentation techniques

Most image segmentation techniques can be divided into three main steps: preprocessing, segmentation and post-processing (see Figure 1). While the segmentation steps usually differ, many techniques share the same pre- and post-processing steps.

A typical preprocessing step is Gaussian filtering of the image to reduce the impact of noise or to construct different scale spaces of the image. Similar 2D convolution process is also used for edge detection (Laplacian, Sobel) or texture filtering. This is a time consuming task on architectures with a single processor, but also one that can be accelerated using an FPGA /12/.

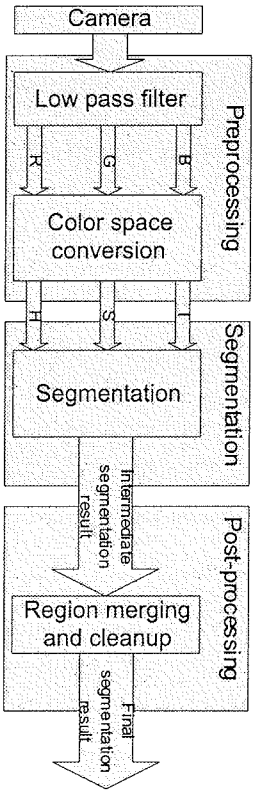

Figure 1: Image segmentation processing steps

Another common preprocessing step is color space transformation. The normal RGB color space is not optimal for color image segmentation and many features have much better contrast if a proper color space is used. This is a time consuming operation involving matrix multiplication on every pixel, especially when performed twice (e.g. RGB to HSI and back). It can be effectively parallelized (each pixel can be processed independently) and is a good candidate for FPGA implementation. An interesting implementation can be found in /13/, where the trigonometric functions were replaced with simple arithmetic.

Post-processing tasks include morphological operations, region merging or removal of unwanted segments. Efficient mapping of morphological operations in FPGAs has been demonstrated in /14/ and region merging is being looked into /15/. Nevertheless, post-processing tasks are not always well suited to FPGA implementation and are usually implemented in software, facilitated by the reduced amount of data due to preceding segmentation.

3.1 Architecture of an image segmentation block

An analysis of the preprocessing→segmentation→post-processing workflow enables us propose a general architecture of image segmentation blocks.

The preprocessing steps are suitable for implementation with FPGA devices. The segmentation process is usually less regular and the use of a processor with an additional FPGA coprocessor is needed to implement the segmen-

tation algorithm effectively. The FPGA coprocessor computes the regular computationally expensive parts of the algorithm, while the processor processes these results on a higher level. The same combination can also be used for post-processing tasks, since they usually aren't suitable for a pure FPGA implementation.

The proposed architecture consists of a preprocessing FPGA block, processor and an FPGA coprocessor with external image and segmentation data buffers, as shown in Figure 2. The link between the processor and the FPGA coprocessor can be implemented in different ways, as custom instructions (especially usable for soft-core processors), as a coprocessor or through a dedicated bus. The FPGA devices containing hard-core processors (Xilinx Virtex II Pro) or soft-core processors (Altera Nios) are most suitable for this implementation.

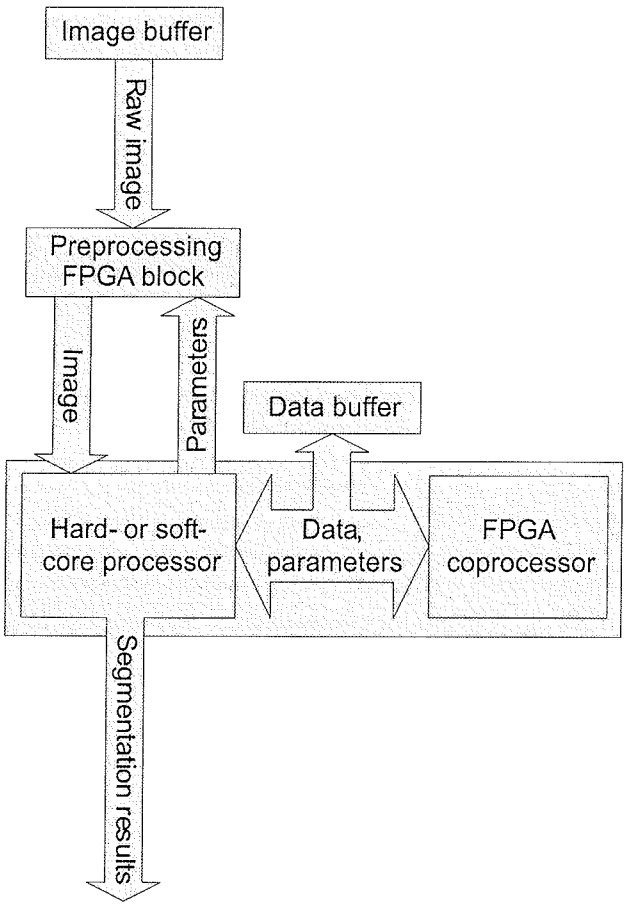

Figure 2: General image segmentation block architecture

4 Proposed design flow

An integral part of the proposed systematic approach to image segmentation is the image segmentation technique implementation workflow. It consists of two main parts, technique selection (using the classification of image segmentation techniques) and adaptation of technique to make it suitable for implementation on an FPGA-based system.

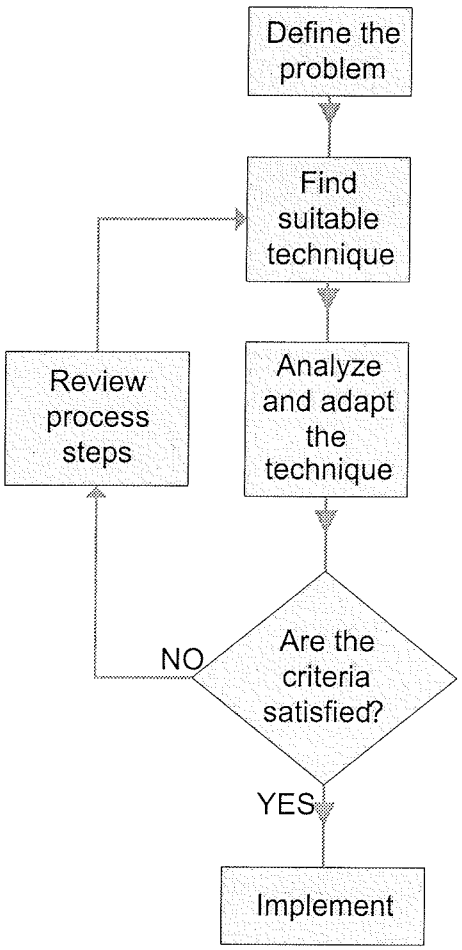

Figure 3: Design flow

4.1 Technique selection

The definition of the problem consists of the definition of the input image or video properties (source of image, expected image content, resolution, frame rate, grayscale or color, color space, amount and type of noise, etc.) and the definition of the environment, performance criteria and goals of segmentation (static or temporal segmentation, well defined or natural objects, stable or variable lighting, expected number of objects, tolerance of erroneous segmentation results, time to process one image, real-time requirements, etc.). The hardware must be defined in terms of resources that are available to the image segmentation block (architecture, free processor cycles, free memory, free FPGA blocks, and power limitations).

Once the properties of the desired system are known, classification of image segmentation techniques is used to determine the adequate technique. The application is matched to one of the application types in the classification. The recommended techniques are compared and the most suitable is chosen. Next, the preprocessing steps to make it compatible with input image properties must be defined. This can include filtering and/or color space conversion. Also, any necessary post-processing should be defined (e.g. morphological operations, etc.)

4.2 Adaptation

Once the general structure of the segmentation block is defined, adaptation of the segmentation block for FPGA implementation must be performed, using the following criteria:

- numerical precision,
- complexity of mathematical operations,
- parallelization,
- data throughput and memory usage.

4.2.1 Numerical precision

Floating point algorithms are generally not suitable for FPGA implementation, due to their increased complexity and silicon footprint. Usually, the image segmentation techniques are robust enough to convert them to fixed point computation without major changes. If this is not possible, the technique must be adapted to fixed point precision.

4.2.2 Complex mathematical operations

Complex arithmetic operations can be defined as operations that are not easily broken down into the basic arithmetic operations already built-in or easily implemented in FPGA-s: addition, subtraction and multiplication. Some examples are: division, roots, trigonometric functions and logarithms.

These operations are generally hard to implement efficiently and precisely at the same time. To implement them, approximations /13/ or look-up tables /16/ must be used and a careful analysis of the tradeoff between needed precision and allowable complexity must be completed. A better approach is to simplify the operations by reorganizing data structures and by mathematical simplification of required operations.

4.2.3 Parallelization

FPGA implementations usually depend on parallelism. In contrast to processors, where one task of essentially unlimited complexity can be processed at a time, FPGA devices are better suited to parallel execution of many simpler tasks.

Most image processing and segmentation techniques are of a local nature i.e. they work on one or a small range of pixels at a time. An array of parallel processing units can be used to accelerate computation by working on many pixels at a time. If this is not possible, other techniques to exploit parallelism exist, e.g. loop unrolling.

4.2.4 Data throughput and memory usage

FPGA devices have a small amount of fast internal RAM, which is not large enough to buffer the whole image or segmentation results. An effective implementation should minimize accesses to external RAM, reusing the data already transferred into the internal memory as much as possible, while using the smallest practical amount of the internal memory. This can be achieved by data structures reorganization and pipelining. Careful buffering will keep the time spent waiting for data to a minimum. The local processing techniques are advantageous in this respect.

4.3 Evaluation

After the adaptation process, the proposed image segmentation block should be evaluated using design-specific criteria like real-time performance, silicon area, power consumption etc. If the criteria are not fulfilled, processing steps should be redefined and adaptation repeated. If this is not enough, a different segmentation technique must be chosen or the problem must be redefined.

5 Case study

For our short case study, we decided to analyze, adapt and implement the image binarization technique described in /17/.

5.1.1 Analysis

The technique consists of 9 processing steps in the following order: 5x5 mean smoothing of the original 8-bit grayscale image, activity calculation, Laplacian calculation, label image generation, label image processing, label image thresholding, 3x3 mean smoothing, gradient magnitude calculation and removal of false print pixels.

An analysis of these steps shows that six steps are good candidates for hardware implementation: the 5x5 mean smoothing, the 3x3 mean smoothing, the gradient magnitude calculation, the Laplacian calculation, the label image generation and the Sobel filtering step. These steps are suitable for hardware implementation (fixed point precision, local processing) and can work concurrently, while the remaining tasks are better suited for software implementation. The mathematical operations are limited to addition and constant multiplication. The local nature of processing enables reuse of data in internal buffers, reducing the data throughput.

5.1.2 Adaptation

We can adapt the mean smoothing blocks by using simple shifting instead of multiplication. The errors thus introduced are constant (21.9% for 5x5 and 43.8% for 3x3 mean smoothing) and can be entirely compensated for by changing the two thresholds used by the technique. Multiplier stages are no longer needed, at the cost of slightly reduced dynamic range. The Laplacian calculation and Sobel filtering hardware blocks require only multiplication by powers of two, also enabling us to use shifting instead of multipliers.

Furthermore, the blocks can be grouped into stages, where two or more blocks can work in parallel: First, 5x5 and 3x3 mean smoothing blocks process the input image. Second, activity, Laplacian and label image calculation is

performed on 5x5 mean smoothed image, while the last stage performs Sobel filtering on 3x3 mean smoothed image.

5.1.3 Implementation

We decided to implement the hardware blocks on an Altera Apex prototype board with an Apex EP20K200EFC484-2X device. The implementation used a 100 x 100 pixel image, stored in external SRAM memory, and a state machine to read pixel data, compute the results of the processing steps and write them back to the SRAM memory. The design was done in VHDL in Altera Quartus II 4.1 IDE.

The external SRAM memory represents a bottleneck, because data can only be read one pixel at a time. We therefore divided the processing into a pipeline consisting of three stages: First 27 states of the state machine were used to concurrently compute the 5x5 and 3x3 mean smoothing results for the given pixel and store them into SRAM (25 pixels read, 2 written). Next 19 states were used to concurrently compute the activity, Laplacian and label image for the given pixel of the 5x5 smoothed image and store the label image in the SRAM memory (18 pixels read, 1 written). The final 10 states were used to compute Sobel filtered result of the given pixel of the 3x3 mean smoothed image and write it into SRAM (9 pixels read, 1 written). When processing reaches the last pixel of the input image, it resumes at the first pixel, refreshing the results regularly. The pipeline design means that three passes through the data are needed to obtain all the results for the first frame and afterwards each subsequent pass returns the results for subsequent frames.

The worst case propagation delay in the design amounts to 146 ns, SRAM read and write delays included, allowing an 6.8 MHz system clock, which results in a refresh rate of about 12 fps. The design uses 3300 logic elements (39% of the device) and 6144 memory bits (5% of the device). There are enough resources remaining to enable us to include a Nios soft core processor into the design to perform the remaining processing tasks.

This implementation, while not optimized for performance, is intended as a demonstration of the second part of the image segmentation implementation design flow, outlining the basic tasks needed to implement image segmentation in FPGA devices. It shows that analysis and adaptation of the technique in accordance with the proposed guidelines are vital for a successful implementation, enabling us to save silicon and improve performance.

6 Future work and conclusion

We have shown that a systematic approach to image segmentation on modern FPGA platforms is needed. To make the proposed systematic approach to image segmentation practically useful, we plan to research a comprehensive overview of different types of segmentation techniques regarding their performance for particular application types.

Our proposal consists of an image segmentation technique comparison, criteria for adaptation of techniques for implementation on FPGA devices, an architecture for image segmentation blocks and a workflow to efficiently select and adapt a suitable technique for image segmentation on an FPGA device.

The approach was illustrated by analyzing, adapting and implementing a sample image segmentation technique in accordance with the given criteria, resulting in reduced implementation complexity and the ability to perform some tasks in parallel.

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EFFICIENT IMPLEMENTATION OF A THREE-CHANNEL ECG DIGITAL ACQUISITION MODULE

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Key words: ECG, PSoC, mixed-signal array, microcontroller, analog signal acquisition, quantization, sampling, holter monitor

Abstract: ECG signal acquisition has to deal with small signal measuring. The amplitude of the ECG signal is only a few mV and the signal frequency ranges from a few mHz to a few hundred Hz. The signal baseline drift caused by respiration or variable contact between the electrode and the skin, signals generated because of power line interference from power mains, and noise often obstruct otherwise simple ECG signal measurements. In this paper, one of the possible ECG signal acquiring systems that overcome these problems is shown. The developed system is a three-channel signal acquiring device easily comparable to some of the commercially available holter monitors. The specialty of the device acquisition part is that it is realized with only two active components, i.e. an instrumentation amplifier and a PSoC mixed-signal array.

Učinkovita implementacija digitalnega modula za trikanalen zajem EKG signala

Kjučne besede: EKG, PSoC, mikrokrmilnik, zajem analognega signala, vzorčenje, holter

Izvleček: Merjenje EKG signalov je merjenje signalov nizke amplitude. Amplituda EKG signala je le nekaj mV, njegov frekvenčni razpon pa je med nekaj mHz in nekaj sto Hz. Merjenje EKG signala otežujejo motnje kot so neprenehno spreminjanje enosmerne referenčne napetosti elektrod, ki jo lahko povzroči dihanje ali pa spreminjanje upornosti med kožo in elektrodami, motnje zaradi napetosti, ki se v merilnih priključkih inducirajo zaradi elektromagnetnega polja električnega omrežja, in pa nenazadnje šum. V članku je opisana ena od možnih izvedb sistema za zajemanje EKG signala, ki lahko, ne glede na moteče dejavnike, kakovostno meri EKG signal. Razviti trikanalni merilni sistem lahko brez težav primerjamo s komercialno dobavljivimi holterji. Posebnost merilnega dela je, da je sestavljen le iz dveh aktivnih elementov; instrumentalnega ojačevalnika in PSoC mikrokrmilnika, ki je prilagojen za delo z analognimi in digitalnimi signali.

1. Introduction

Polarization and depolarization of the heart muscle mass creates a three-dimensional electrical field that changes with time. As a result, voltages can be measured on the surface of the body. They represent the pumping cycle of the myocardium. The most widely used three differential voltages that represent the heart activity are: from the right arm (RA) to the left arm (LA), from LA to the left leg (LL), and from LL to RA. These voltages are known as ECG leads I, II, and III. The right leg electrode (RL) acts as the neutral pole in this system. This configuration is known as the Einthoven triangle.

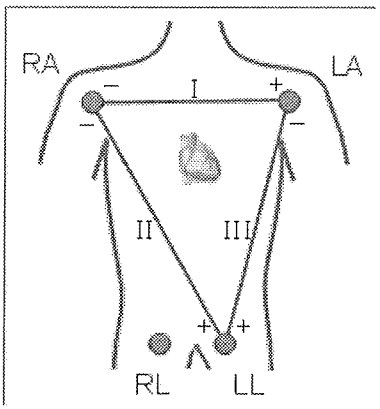

Figure 1-1: Einthoven Triangle

It is clearly seen that the three leads are defined as:

$$\text{Lead I: } V_I = V_{LA} - V_{RA} \quad (1)$$

$$\text{Lead II: } V_{II} = V_{LL} - V_{RA} \quad (2)$$

$$\text{Lead III: } V_{III} = V_{LL} - V_{LA} \quad (3)$$

This three-lead voltage system is the basis of ECG signal measuring.

The amplitude of the ECG signal as measured on the skin ranges from 0.1 mV to 5 mV and its frequency approximately extends from 0.05 Hz to 300 Hz. However, according to /1/ and /7/, ECG signal measuring in the frequency range of 0.5 Hz to 100 Hz is sufficient to do the basic analysis while a lot of devices on the market only cover the 0.5 Hz to 50 Hz frequency range which is still sufficient for monitoring applications. Since the ECG signal has a very low voltage, the average amplitude of the signal is only around 1 mV, and its frequency is low, too, there are several problems preventing its efficient measurement. One of them are large DC offset voltages resulting from electro-

chemical processes between the electrode attached to the patient and the patient's skin. These voltages can be as high as +/-500 mV. Also, the contact resistance between an electrode and the body surface can vary very much. The presence of 50 Hz (60 Hz in USA) power line noise is one of the major problems to be copped with, because common-mode voltages as high as several volts peak-to-peak can be superimposed on the body. Signals originating from muscle contraction are present in the ECG signal as well. Eliminating this source of noise is one of the major tasks of an ECG amplifier.

When one encounters health problems that indicate there is something wrong with her/his heart activity, one's ECG is usually measured. In case problems come up irregularly, usually a holter recorder is used to record heart activity over a longer period of time, usually through 24 or 48 hours. The data is stored on a removable memory media such as audio cassette or CompactFlash card. During the recording time, the person wearing the holter recorder can live her/his normal everyday life and as soon as the holter recorder is returned to the hospital, the recorded data is transferred to a PC running ECG analysis software. Doctors can now make an exact diagnosis of the problem. 24-hour holter recorders usually offer one to three-channel ECG recording with 100 to 300 samples per second at eight to ten-bit sample resolution.

The main goal of our research work was to design a low-cost ECG signal acquisition module operating as a holter recorder or an event monitor and having characteristics similar to the ones of commercially available holter recorders. We also wanted the device to consist of inexpensive, widely used and commercially available electronic components. We found it important that only components with low power consumption are used since the device is powered from battery cells. The acquired data is either saved to a SecureDigital memory card or sent to a wireless instrumentation network providing real-time global powerful data processing capabilities. Moreover, the applied wireless instrumentation network allows also on-line diagnostics of any human being under investigation, alarming, heart-attack detectors, etc.

This paper focuses on the device's acquisition part and the pertaining communication interface composed of just two different types of active components and some passive components. Differential signals of each of the three measurement channels are amplified by INA118 precision low-power instrumentation amplifiers (IA). They were chosen because of their good electrical characteristics described in /5/, they have high CMR of 120 dB, their gain is set with an external resistor and their power consumption is low.

For general processing and signal filtering, a PSoC from Cypress MicroSystems is used. This is a low-power 8-bit microcontroller designed with a different approach compared to other microcontrollers on the market. The microcontroller comprises an 8-bit core processor, eight digital

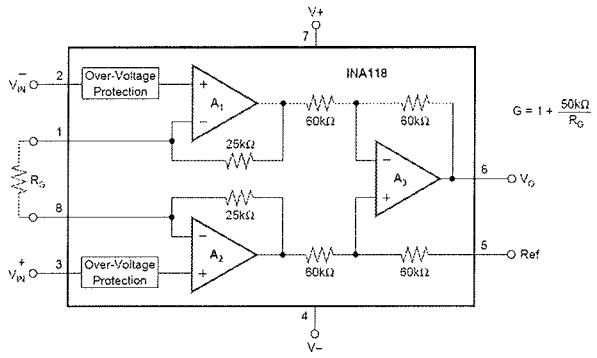

Figure 1-2: INA118 Instrumentation Amplifier

blocks and twelve analog blocks. Digital blocks provide all communication peripherals, counters, timers and PWMs while analog blocks consist of digital-to-analog converters (DAC), analog-to-digital converters (ADC), programmable gain amplifiers, programmable filters and comparators. A more detailed description can be found in /6/. A PSoC top level block diagram is shown in *Figure 1-3*.

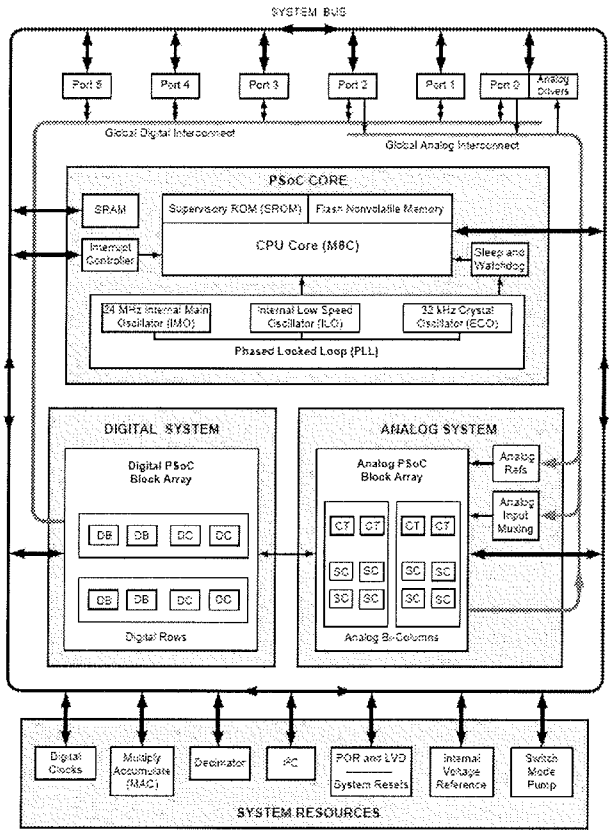

Figure 1-3: PSoC Top Level Block Diagram

2. ECG Measurement Loop

From the nature of the ECG signal and problems that interfere with the quality signal measurement, it can be seen that the overall system must protect the patient and filter out disturbing signals. As one of the most important fac-

tors is DC offset voltage elimination, the system must act as a high-pass filter that passes all signals of the frequency greater than 0.05 Hz (or at least greater than 0.5 Hz) and at its input compensates any signals of a lower frequency. The basic idea of signal acquisition is to amplify the input signal, filter it, digitize it, and store the samples. Problems caused by the DC offset voltage are detected and eliminated by a feedback loop.

Input Stage and Active Driving of Body Reference

One of DAC in PSoC is used to generate a 1.3 V signal named the body reference. This signal is used as the right leg drive signal RA shown in *Figure 1-1* and sets the patient's body to a virtual potential of 1.3 V against the measurement system which is this way placed at a virtual potential of 0 V. The ECG signal is led to the INA118 IA through high-resistance series resistors (R_{PROT}) used to prevent either possible quick discharges of IA input capacitors through the patient's body or high-current flows through the patient's body in case of device malfunction. The same kind of resistor is used on the body reference signal as well. IA gain K_{IA} is set to 16 meaning the input differential signal voltage is multiplied by 16 at the IA output. At the same time, the IA's common-mode rejection ratio (CMRR) of 120 dB assures that only one millionth of the input common mode signal voltage passes to the output of the amplifier.

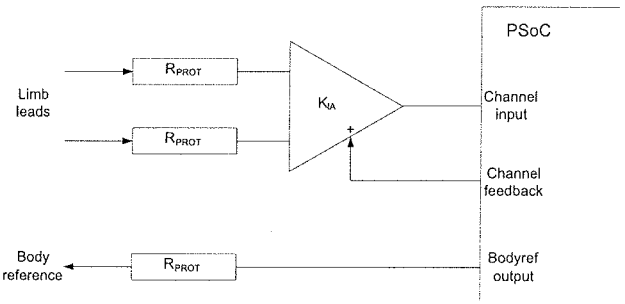

Figure 2-1: Input/Output Stage

This CMRR assures that almost no common-mode interference voltages (usually inducted in wires because of the power line electromagnetic field) pass the IA. Once the signal is amplified, it is acquired by the PSoC where it is again amplified by one of the programmable gain amplifiers (PGA). Here, too, the gain is set to 16 (K_{CHIA}). A simple diagram of the PGA block is shown in *Figure 2-2*.

Analog-to-Digital Conversion

After amplification, the signal is digitized with integrating ADC represented with a block named H_{AD}. H_{AD} is an ADC converter transfer function which can be derived from the equation characteristic for integration:

$$V_{OUT}=\frac{\int_{t-T_{int}}^{t} V_{IN}}{T_{int}} \qquad (4)$$

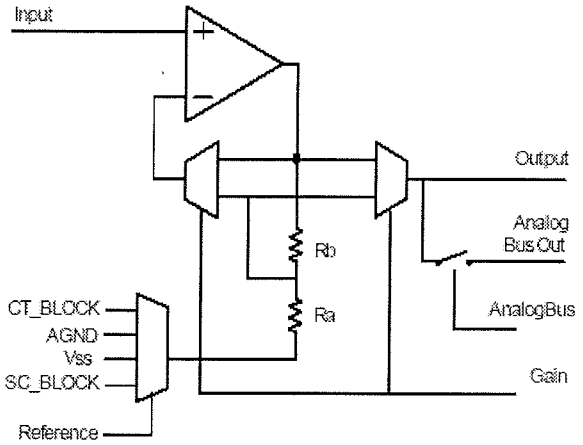

Figure 2-2: PSoC PGA Block (K_{CHIA})

which after Laplace transformation becomes:

$$V_{OUT}(s)=V_{IN}(s)\cdot\frac{1}{T_{int}\cdot s}\Rightarrow H_{AD}=\frac{1}{T_{int}\cdot s} \qquad (5)$$

T_{int} (integrating time) can be calculated according to instructions in the PSoC datasheet. In our case, T_{int} is 6.8267 ms. But as there is also delay to perform the above calculation within the PSoC, the total time spent for integration is 10 ms. Since the function of integration is not active all the time, but rather at short time intervals, the integrating part can be omitted and the transfer function can be written in a completely different way. We can say that its value depends on the input voltage range and number of output bits (resolution).

$$H_{AD}=\frac{N}{V_{ADC}}=\frac{256}{2.6} \qquad (6)$$

An important benefit of the ADC used is that it consists of three separate ADCs which can all operate simultaneously. A simplified block diagram of this triple ADC is shown in *Figure 2-3*. Although their resolution ranges from 7 to 13-bits per sample and the sample rate can go as high as 10,000 samples per second, 8-bit resolution at 100 samples per second was chosen. Samples are stored in a 24-bit register to enable further signal processing. ADC default reference voltage V_{ref} is set to 1.3 V and can therefore efficiently digitize voltages that range between 0 V to 2.6 V (V_{ref} ± 1.3 V). V_{ref} is the reason for setting the body reference to 1.3 V. As already mentioned, the peak-to-peak voltage of the ECG signal is approximately 10 mV. In order to stretch these 10 mV to the entire 2.6 V scale of the ADC, the signal is amplified.

$$V_{ADC}=K_{IA}\cdot K_{CHIA}\cdot V_{ECG} \qquad (7)$$

With V_{ECG} = 10 mV and K_{IA} = K_{CHIA} = 16, V_{ADC} as an input voltage to the ADC equals 2.56 V which almost covers the entire ADC input range.

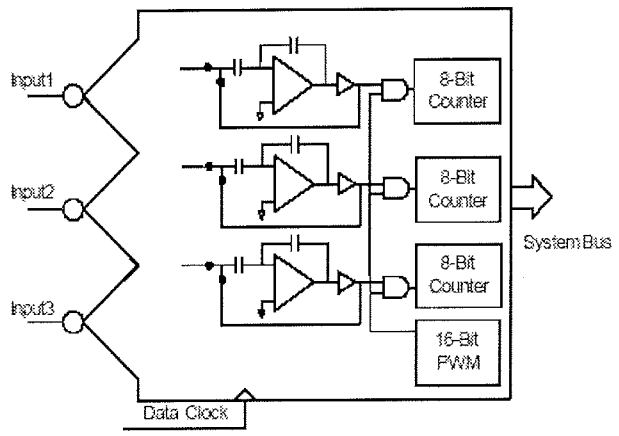

Figure 2-3: PSoC Triple Input ADC - Simplified

Though the signal is now ready to be stored to the memory card, there is still one more problem to be solved.

Feedback Loop – Integrator and Pole Positioning

As the first step in the DC component detection and elimination, an integrator is used to continuously integrate the digitized ECG signal.

An important detail of the design is also a correct system transfer function pole placement. The pole defines which frequencies will be attenuated and which not. In order to get the desired effect and place the pole near to 0.05 Hz or 0.1 Hz, the signal is multiplied by 16 (K_P).

Feedback Loop – Digital-to-Analog Conversion

Conversion back to the analog signal is necessary to provide offset voltage compensation to the input IA. Digital-to-analog conversion is done with an 8-bit pulse-width modulator (PWM) and a low-pass RC filter. Voltage conversion using just an 8-bit PWM usually gives satisfying result in low-precision systems, whereas in our case any minor integrating change would immediately result in DC offset voltage modification at the low-pass filter. Since this is not desired, the precision was improved with a software delta-sigma modulator placed in front of the PWM.

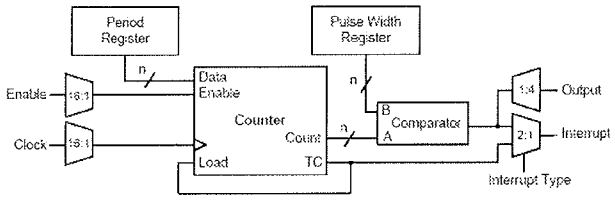

Figure 2-4: PSoC PWM Block Diagram

A software delta sigma modulator upon 8-bit PWM hardware enhances resolution for additional 7-bits, yielding a 15-bit DAC. Eight most significant bits are actually used as an input signal to the PWM, while seven less significant bits are used as its decimal value. Although an 8-bit PWM is used, together with a delta-sigma modulator the overall performance increases as if a 15-bit PWM was used. Because of the nature of digital-to-analog conversion a conversion factor K_C of 3.3/256 has to be taken in consideration. The PWM output is connected to a low-pass RC filter with components R=6.8 kΩ and C=22 μF.

$$H_{RC}(s)=\frac{1}{1+s\cdot R\cdot C} \tag{8}$$

The output voltage generated on the filter is finally inverted by PSoC (K_{REF}) and to IA where it is added to the input ECG signal.

Other Overall System Design Considerations

A possible problem that arises with digital-to-analog transformation is noise generation. It reflects itself in a noisy feedback offset voltage which is consequently inserted into the ECG signal. This problem is minimized in two ways. Noise is at first very much reduced by a low-pass RC filter placed after the IA and is again reduced by integrating ADC. Integrating time (T_{int}) of ADC and PWM pulse period (T_{PWM}) are set in such way that T_{int} is a wholenumber multiple of T_{PWM}.

$$T_{int}=k\cdot T_{PWM};\ k\in N \tag{9}$$

This relation maximizes rejection of noise generated by the PWM, while other high-frequency (stochastic) noise is also much reduced with ADC signal integration.

AC Filter

Using the blocks mentioned above, a first order AC-filter eliminating the DC voltage at the input is constructed. We can briefly describe the process that is hiding behind the system. Although the body reference voltage potential is set to 1.3 V, it is not necessary that this is also a reference or offset voltage for each ECG channel. It is more likely that each channel differential voltage will have its own offset voltage drifting around 1.3 V value. This deviation can cause incorrect ECG signal measurement because an incorrect offset voltage can cause the ADC input range to be exceeded. Any DC or very low frequency components must therefore be removed from the signal being taken care of by the feedback loop. The integrator in the loop detects this error which is then converted back to the analog signal and subtracted from the source ECG signal by the IA.

Offset Compensator

The offset compensator is an additional part to the overall AC filter design. Its position in the system can be seen in the lower right part of the overall system block diagram shown in *Figure 2-6.* The offset compensator is responsi-

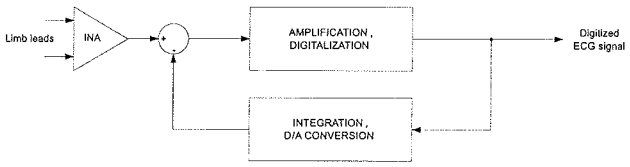

Figure 2-5: Basic System Loop

ble for setting the ECG signal to the centre of the ADC input voltage range when certain conditions are not met. The AC filter integrator located in the upper branch (INT) operates all the time while the integrator in the lower branch (INT_{OC}) is only active when the signal reaches the upper or lower ADC limit. The part of the design that enables or disables the second integrator is shown as a block with a non-linear transfer function. This offset compensator continuously monitors sampled values and centers the signal to $V_{PP}/2$, where V_{PP} is the ECG signal peak-to-peak voltage. When the values are within a preset range, the second integrator is disabled, but when the values fall out of the preset range, the second integrator is enabled.

System Transfer Function Calculation

After having described the system, we can show a complete block diagram for one of the three measurement channels (one lead). The remaining two channels are designed in a similar way, except for the body reference which is common for all the three channels.

The *Figure 2-6* shows which functional blocks are realized in PSoC and which are realized with external components. It can be seen that only input IA (K_{IA}) and low pass filter (H_{FILT}) are placed outside the PSoC boundary and therefore realized with external components.

The following transfer function can be written for the system presented in the *Figure 2-6*:

$$H(s)=K_{INA}\cdot\frac{K_{CHIA}\cdot H_{AD}}{1-K_{INT}\cdot K_P\cdot H_{DA}\cdot K_C\cdot H_{FILT}\cdot K_{REF}} \quad (10)$$

After all values are entered in this equation, the result is:

$$H(s)=\frac{1616\cdot\frac{256}{2.6}}{1-\frac{100}{s}\cdot 16\cdot\frac{1}{2^{16}}\cdot\frac{3.3}{256}\cdot\frac{1}{1+0.15\cdot s}\cdot(-1)}=$$

$$=\frac{25206.15\cdot(0.15\cdot s+1)\cdot s}{(0.15\cdot s+1)\cdot s+0.5} \quad (11)$$

Both poles of the transfer function are negative which is common to absolutely stable systems. One of the transfer function poles is at -0.544 and the other at -6.122. After recalculation from the s domain to the frequency domain this means the poles are at -0.087 Hz and -0.974 Hz. The pole that is closer to zero has a dominant influence on the system transfer function. It is therefore expected that signals of frequency lower than 0.087 Hz will be attenuated.

For testing purposes, the system response to the unit step can simply be calculated by multiplying H(s) with 1/s which is Laplace transformation of the unit step. Using the Mathcad tool, we performed inverse Laplace transformation of the response and got a result shown in *Figure 2-7*. It can be seen that soon after the input signal goes high at t=0 s and stays high, the system detects this as a DC offset and starts with compensation. After two seconds, the signal already drops by 63%.

This is the expected response. At the beginning, there is no input signal to the system. Once the unit step is present, the system samples the change and outputs it. But as the input voltage does not change with time, the system treats it as a large DC offset. Input DC offset should not be a part of the desired ECG signal measurement, therefore the PSoC starts compensating it. Consequently, the output voltage starts falling towards 0 V.

3. Communication interface

Processed ECG data samples are sent to the second processor that handles wireless data transfer or data storage to removable media. Data exchange is done via both proces-

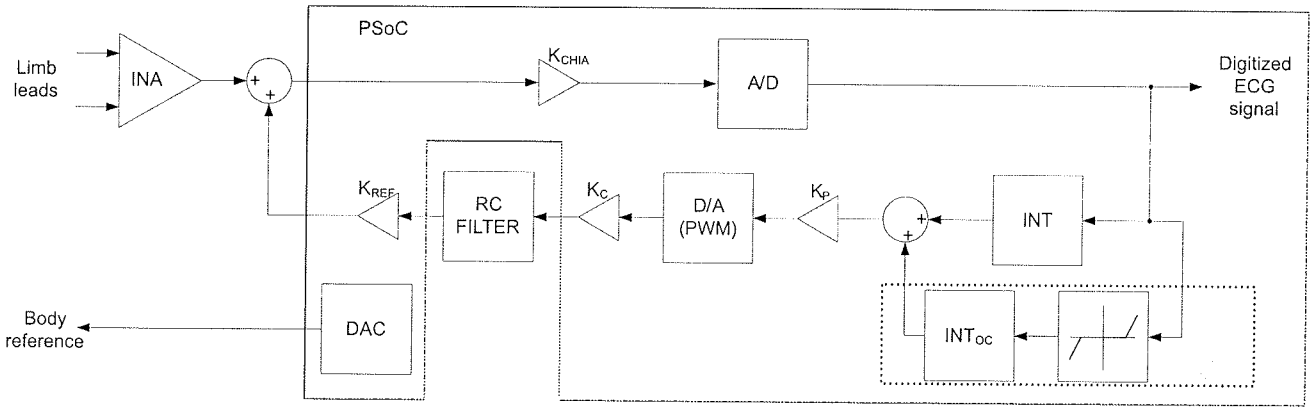

Figure 2-6: Complete Measurement Loop

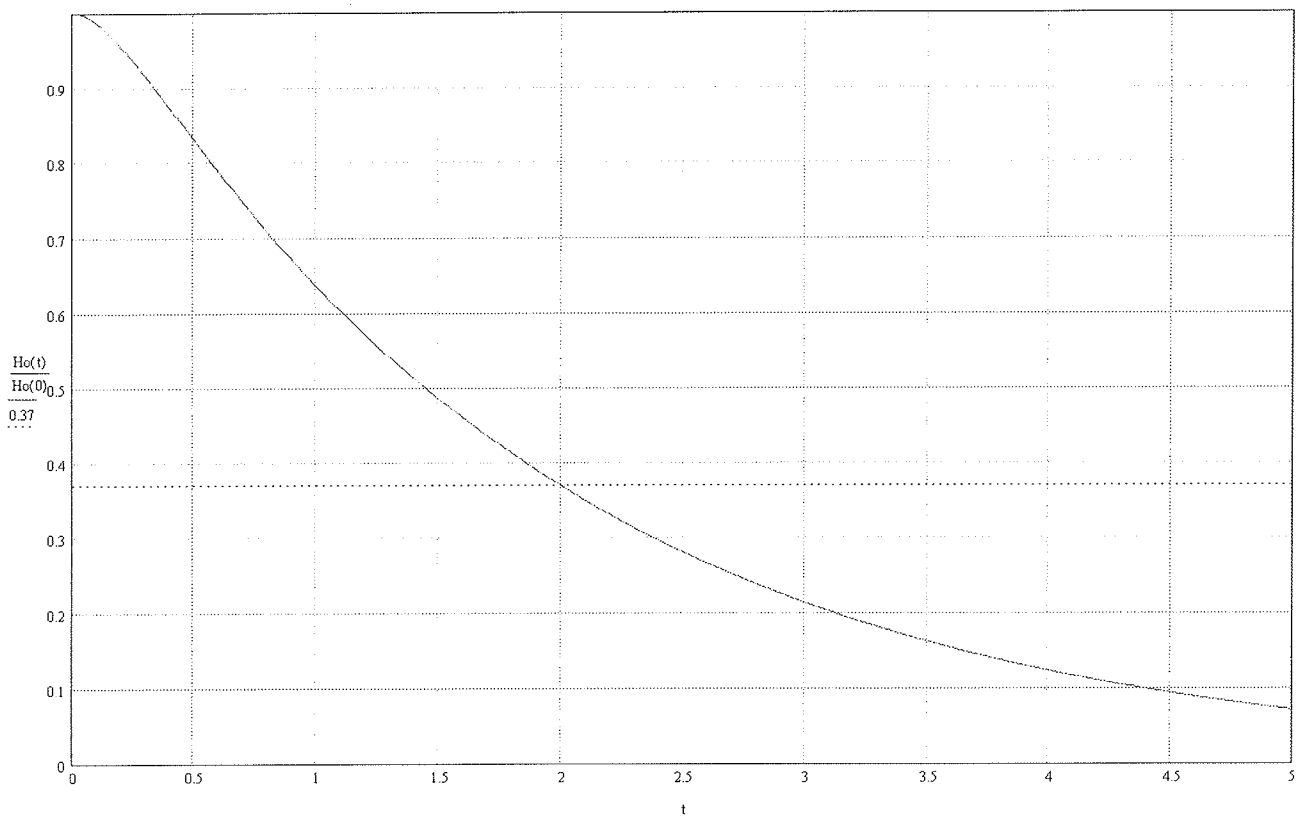

Figure 2-7: Calculated System Response to Input Unit Step

sors' I2C interfaces. As the design is battery powered, it is crucial that ECG data is sent as infrequently as possible in order to save power. For making this possible, data compression is done in the PSoC. For this purpose we implemented Huffman variable length coding (VLC). This is an entropy encoding algorithm that finds the optimal system of encoding strings based on the relative frequency of each symbol. Fixed 8-bit size binary symbols are replaced with variable length codes of an optimal length in such a way that the most common symbols are presented in the shortest way possible. The larger is the probability of a symbol to occur, the shorter is its code.

Because of the dynamic nature of the ECG signal, the range of different values it can take is relatively large. *Figure 3-1* shows how often individual 8-bit sampled values of the ECG signal are repeated over a certain period of time.

The number of different values can be significantly reduced if the ECG signal is represented with differences between adjacent signal values. Distribution of such signal representation is shown in *Figure 3-2*.

We can see that this kind of signal representation is more concentrated around one value and is less dispersed over the whole range. A system with less different values can more easily and efficiently be encoded, therefore the second signal representation was chosen. As an offset value of the signal must be known, the first data sample needs to have its real sampled value. All other ECG signal values

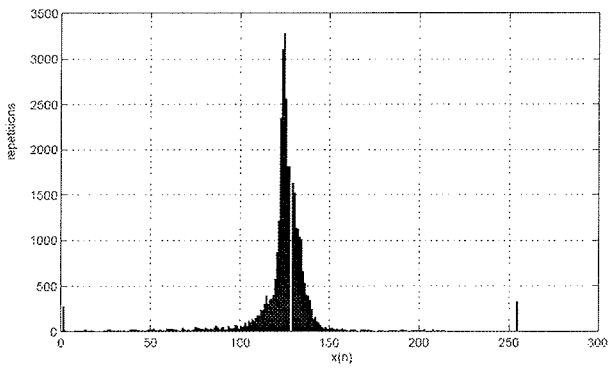

Figure 3-1: Value Distribution of a Sampled ECG Signal

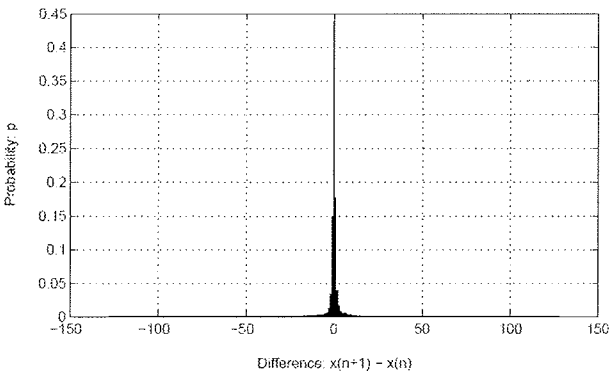

Figure 3-2: Distribution of Differential Values Between Adjacent ECG Samples

are derived from the given differences. The resulting ECG signal vector would thus be:

$$X=[x(1), d_{1,2}, d_{2,3}, \ldots, d_{n-1,n}] \quad (12)$$

where x(1) is the first data sample and $d_{i,j}$ is the difference between sample x(i) and x(j). This kind of data stream can be efficiently encoded at this point. A set of Matlab/Octave dedicated functions was used in order to generate the Huffman codes from the distribution shown in *Figure 3-2*. Because of power saving, the encoded ECG signal data needs to be sent out of the PSoC microcontroller in bursts of packets. A calculation of the compression ratio versus the packet size was used to find an optimal packet length. To find the optimum packet size, an N bytes long input vector was compressed and repacked to P bytes long output packets. The compression ratio is represented as:

$$\text{Compression\_Ratio}=\frac{\text{Input\_Packets}}{\text{Output\_Packets}}=\frac{N}{P} \quad (13)$$

Results are shown in *Figure 3-3* where it can be seen that the packet size greater than 10 bytes should be sent to the second microcontroller.

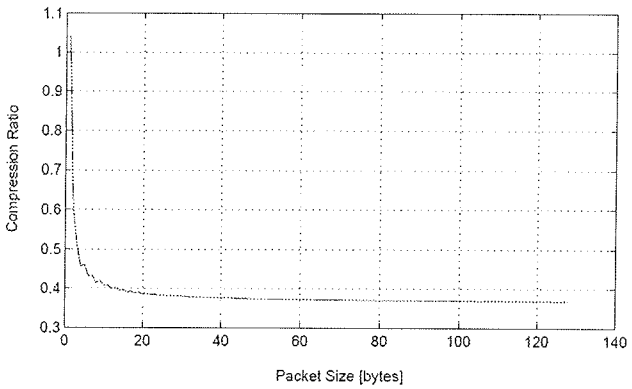

Figure 3-3: Compression Ratio vs. the Packet Size

4. Results

Hardware implementation was verified using a sine generator to scan the frequency response function. Measurements showed that the system started to attenuate input signals of the frequency lower than approximately 0.4 Hz. Attenuation of $\sqrt{2}$ was achieved at approximately 0.075 Hz which is very near to one of the calculated poles of the system transfer function.

In the next step we measured how the system responds to a unit step input signal. *Figure 4-1* depicts this measurement performed on the third channel. As the other two channels were short circuited, they are not shown. The markings in the figure are used for a quicker orientation. It can be noted that the response is very similar to the calculated response depicted in *Figure 2-7*, meaning that implementation results overlap with theoretical results.

After verifying characteristics of each channel, the ECG signal was measured using the placement as described for a popular holter manufactured by Spacelabs Burdick, Inc. The lead placement and placement description according to /4/ are shown in *Figure 4-2* and *Table 4-1*.

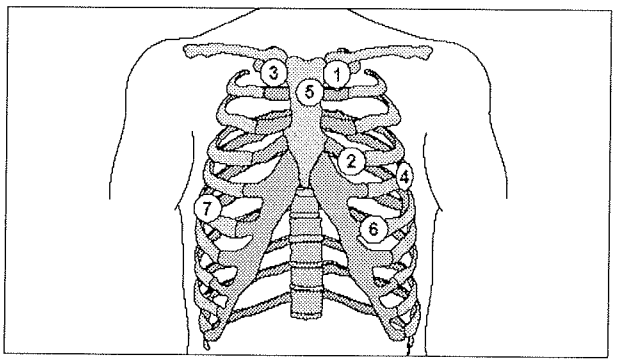

Figure 4-2: ECG Lead Placement

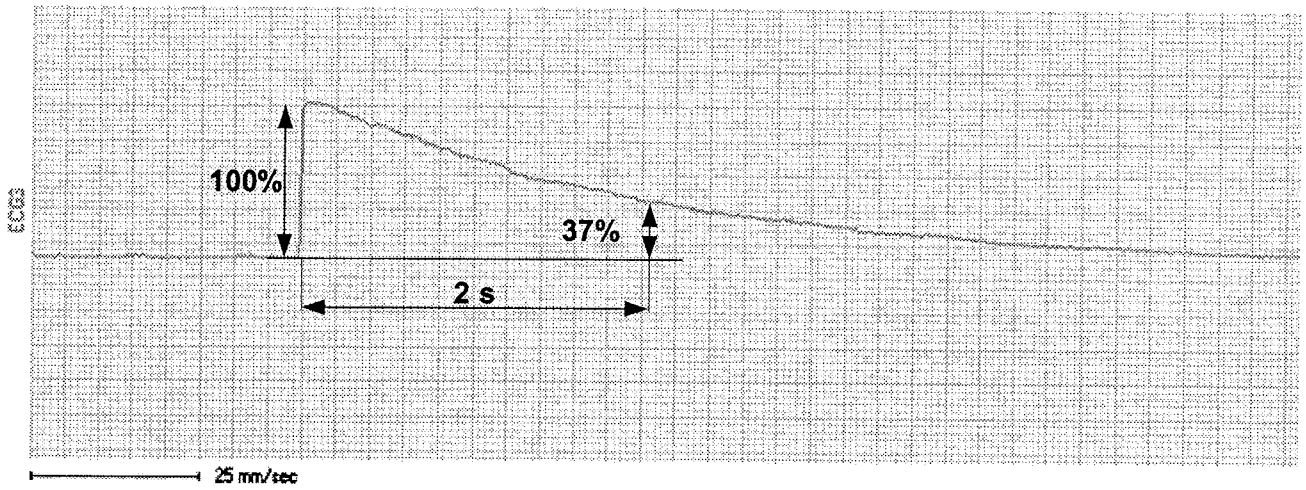

Figure 4-1: Response to Low-frequency Square-wave Input Signal on Channel 3

Table 4-1: Lead Placement Description

#	Channel	Color	Lead	Placement
1	1 (-)	white	LA	Below left clavicle, just lateral to the midclavicular line.
2	1 (+)	red	Mod V5	At the fourth rib to the left of the sternal border.
3	2 (-)	brown	RA	Below right clavicle, just lateral to the midclavicular line.
4	2 (+)	black	Mod V6	Fifth rib at anterior axillary line.
5	3 (-)	blue	Sternum	At manubrium sterni.
6	3 (+)	orange	Mod V4	At the sixth rib on the midclavicular line.
7	Bodyref	green	Reference	Lower right chest wall, rib.

Measurement results according to the above lead placement:

Figure 4-3: 3-channel ECG Measurement

5. Conclusion

One of the possible ways of implementing an ECG signal acquiring unit was discussed in this paper. We have decided to design a device similar to the commercially available ECG holter monitors with as little electronic components as possible. In fact, only instrumentation amplifiers, passive RC filters and a PSoC microcontroller were used for our implementation. We started by identifying the problems present at ECG signal measurements, then we defined a model eliminating these problems and at last calculated its response to the input signal.

The design in hardware and software proved to work in the same way as the theoretical model. Measurements showed that the input DC voltage and common mode voltage are successfully reduced and therefore do not have any major influence on the ECG signal measurement quality. Our design samples and records the input signal at the rate of 100 samples per second with 8-bit resolution. The input signal frequency range is between 0.1 Hz and 50 Hz. Signals of the frequency out of this range are either attenuated or not sampled correctly.

In the next step we shall investigate the possibilities of increasing both the sampling frequency and the number of bits per sample. The microcontroller is loaded as little as 30%. The theoretical limitations show the maximum sampling frequencies to be up to 800 Hz @ 9 bits and maximum resolution 12 bits @ 100 Hz. Some of the possible limitations will surely be additional tasks the microcontroller shall have to perform in a target system. Also to be investigated is the allowed power consumption of the target system.

Acknowledgement: This work was supported by Ministry of Education, Science and Sport of Republic of Slovenia as part of Research Program P2-0246 "Algorithms and Optimization in Telecommunications"

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THE PRINCIPLE OF NEW SIGMA DELTA MODULATION TECHNIQUE BASED UPON THE USE OF A FLIP-FLOP

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Key words: sigma delta modulation, flip-flop, capacitive accelerometers

Abstract: This paper describes a new sigma delta modulation technique. This technique is used for measurement of changes in half capacitive bridge to detect deflections, which can result from acceleration input in practice. The half bridge is connected to a modified flip-flop circuit, the outputs of which are used for one-bit force feedback. The modification of flip-flop consists in the implementation of a switched capacitor structure to achieve a perfect flip-flop value symmetry and compensation of a flicker noise. Some theoretical considerations are verified by experimental results. An experimental circuit has been constructed from discrete elements.

Osnove nove sigma-delta tehnike modulacije na osnovi uporabe flip-flopa

Kjučne besede: sigma-delta modulacija, flip-flop, kapacitivni merilniki pospeška

Izvleček: V prispevku opisujemo novo sigma-delta tehniko modulacije. Uporabljamo jo pri meritvi spremembe kapacitivnosti na mostičku namenjenemu zaznavanju odmikov pri pospeševanjih. Mostiček je priklopljen na flip-flop vezje, katerega izhode uporabljamo za povratno vezavo na mostiček. Mostičku je dodana struktura stikalnega kondenzatorja, s pomočjo katerega dosežemo popolno simetrijo izhoda flip-flopa in kompenziramo šum. Nekatere teoretične predpostavke smo preverili s preiskusi. Preizkusno vezje smo izdeleli z diskretnimi elementi.

I. Introduction

A. Capacitive accelerometers

In a typical capacitive accelerometer, the proof mass is suspended above a substrate by compliant springs. Two nominally equal-sized sense capacitors are formed between the electrically conductive proof mass and stationary electrodes /1/. When the substrate undergoes acceleration, the proof mass displaces from the nominal position, causing an imbalance in the capacitive half-bridge, shown in Fig.1a. This imbalance can be measured using charge integration technique /1/. Other techniques can be found in reference /2/.

Force balancing of the proof mass is attained by enclosing the proof mass in a negative feedback loop. The feedback loop measures deviations of the proof mass from its nominal position and applies a force to keep the proof mass centered. The accelerometer output is taken as the force needed to null, or zero, the position, shown in Fig.1b.

Taking into account only electronics of the system, the precision of measurement largely depends on position sense

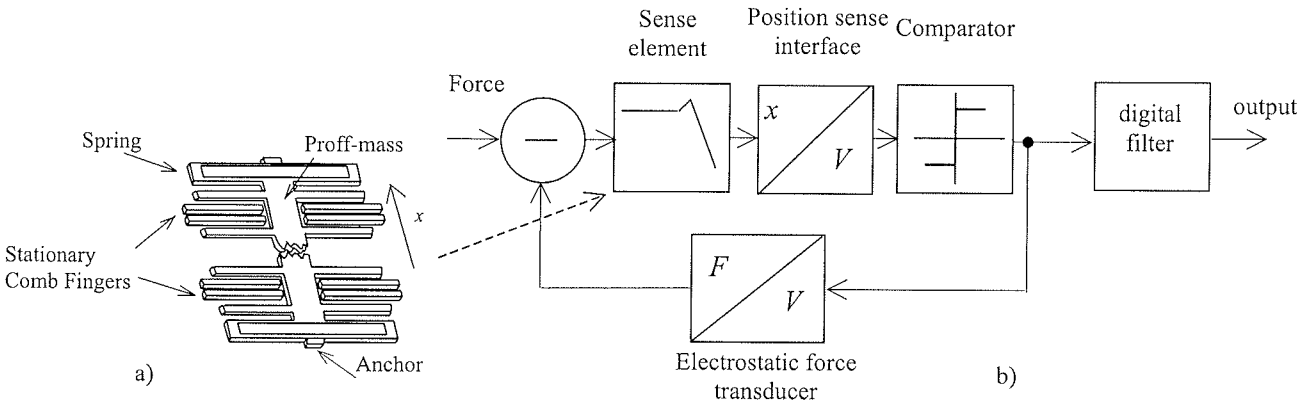

Figure 1a) Sense element, b) schematic of sigma- delta feedback loop

interface. A great deal of contributions therefore focuses on elimination of errors of charge amplifier as a main part of the sense interface. Common-mode rejection ratio, flicker noise, dc offset of operational amplifier, and mismatches in reference capacitors are the main problems that must be solved. An excellent solution can be found, for example, in /1/. In this solution, the op-amp flicker noise and dc offset are measured and subtracted using correlated double sampling /1/. By using an input common-mode feedback /1/, the problems with common-mode rejection ratio and with mismatches in reference capacitors are solved. However, using this approach the system complexity rapidly increases.

Considering the above-mentioned discussion, this paper explores a new sigma-delta technique based upon the use of a flip-flop circuit. Properties of the flip-flop and some topics are therefore depicted in the following paragraph.

B. Utilization of the flip-flop circuits in sensor-based systems

First idea to use the flip-flop in sensor-based systems can be found in /3/. The circuit in Fig.1 as the sensor based on a flip-flop circuit has been introduced in this reference. In comparison to the standard flip-flop, the control impulses are not applied to the bases of the transistors but the circuit is repeatedly connected to a voltage source, shown in Fig.2. Note that flip-flop can be also controlled by a triangular or sine wave signal. The standard flip-flop consisting of two transistors and two resistors is characterized by two stable states, one and zero. In case of ideal value symmetry because of a noise it is not possible to decide that the stable state will be final. However, over a large number of cycles the ratio of ones to zeros will be one - 50 % state of the flip-flop /3/.

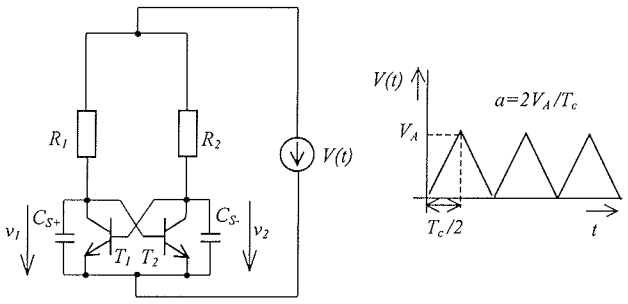

Figure 2. A flip-flop circuit with triangular control signal

As described in /4/, when $C_{S+}>C_{S-}$ and other parameters are identical, the flip-flop takes the stable state 'one'. It means that a high potential V_h is applied across capacitor C_{S+} while a low potential V_l is applied across capacitor C_{S-}. Assume that standard capacitors of the flip-flop are replaced by sense capacitors according to Fig.3.

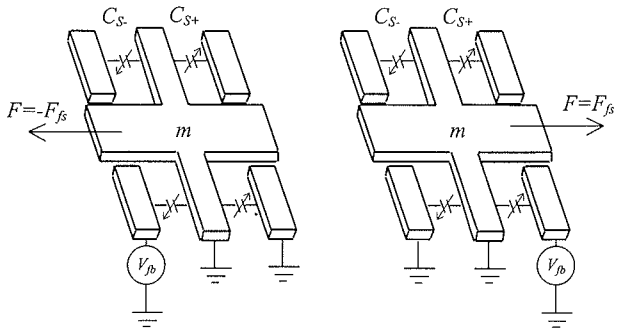

Figure 3. Schematic of capacitors C_{S+},C_{S-}

An electrostatic force between parallel plates of capacitor C_{S+} is given by

$$F_{+} = \frac{1}{2}\frac{\partial C_{S+}}{\partial x}V_h^2 \tag{1}$$

while between parallel plates of capacitor C_{S+} it is a force given by

$$F_{-} = \frac{1}{2}\frac{\partial C_{S-}}{\partial x}V_l^2 \tag{2}$$

The resultant force $F_{fs}=F+-F-$ may be shown to be

$$F_{fs} = \frac{1}{2}\frac{\partial C_S}{\partial x}V_{fb}^2 \tag{3}$$

where $\frac{\partial C_S}{\partial x} = \frac{\partial C_{S+}}{\partial x} = \frac{\partial C_{S-}}{\partial x}$ and $V_{fb}^2 = V_h^2 - V_l^2$. In case that flip-flop holds the stable state 'zero' it is a force $F=-F_{fs}$, shown in Fig.3. Hence, controlling the flip-flop by a triangular signal, the force is applied between parallel plates of the sense capacitors to keep the proof mass m centered, which corresponds with the principle of a capacitive accelerometer.

To use the above mentioned principle, the perfect value symmetry of the flip-flop must be achieved. Note that manufacture inaccuracy of the resistors in the standard CMOS technology is at least 15 %. Primarily, the problem with mismatches in resistances of the flip-flop must be solved. A modification of the flip-flop is described in the following section.

II. Modified flip-flop circuit

A. Switched capacitor based flip-flop circuit

As it can be seen in Fig.4a, the standard resistors are replaced by switched capacitors. The switches are repeatedly turned on and off in the following order S3,S2,S1 and again S3. Corresponding control signals are shown in Fig.5. When control frequency f_{SW} of the switched capacitor C is at least two orders higher than the frequency fc of the triangular impulse generator V, the circuit is equivalent to the scheme shown in Fig.4b. To the point 1 as

well as to the point 2 an equivalent resistance R_{eqv} is connected.

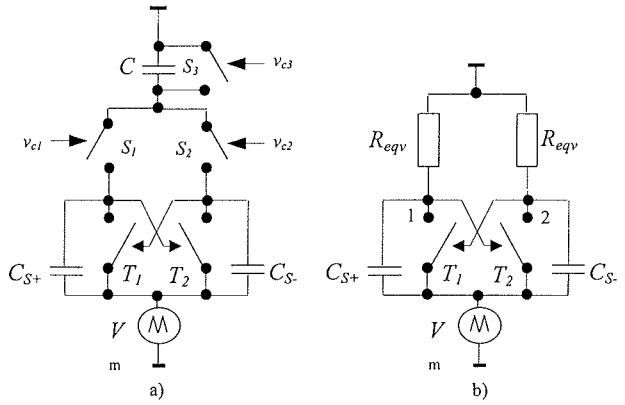

Figure 4a) Flip-flop with the switched capacitor,b) equivalent circuit diagram

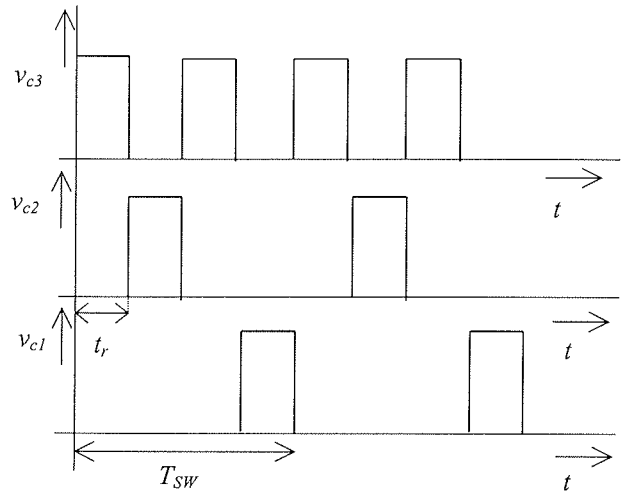

Figure 5. Control signals vc1,vc2, and vc3 of the switches S1,S2, and S3

Equivalent resistance R_{eqv} is given by well-known formula

$$R_{eqv} = \frac{1}{Cf_{SW}} \tag{4}$$

The approach shown in Fig.4a has several important advantages, including its non-sensitivity to changes of the capacitor C and the control frequency f_{SW}. The circuit is also realizable using CMOS technology. On the other hand, switch charge injection as a new influence must be taken into account. Switch charge injection and a noise within the flip-flop are analysed in the following paragraphs.

B. Analysis of a flicker noise

Flicker noise in the flip-flop is mainly due to switches S1,S2,S3. Flicker noise due to unipolar transistors T1,T2 can be omitted because these transistors are turned off in the moment of turnover. Fig.6 shows a CMOS switch. Since the switches are repeatedly turned on and off, a non-stationary model and usage of time domain analysis is needed to analyse the influence of flicker noise.

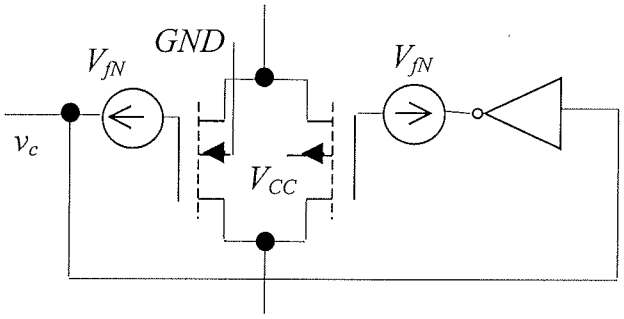

Figure 6. CMOS switch

As shown in /5/, the root mean square (RMS) of noise voltage V_{fN} relating to the control circuit is given by

$$V_{fN} = \left(\frac{q}{AC_{ox}}\right)^2 \frac{1}{t_r^2} \int_0^{t_r}\int_0^{t_r}\int_{\lambda_L}^{\lambda_H} g(\lambda) C_\lambda (s_1, |s_1 - s_2|) d\lambda ds_1 ds_2 \tag{5}$$

where C_{ox} is the gate oxide capacitance, A is the channel area, q is the elementary charge, λ_H is the fastest transition rate, and λ_L is the slowest transition rate of the carriers, g represents the distribution of λ, C_λ is an autocovariance in the time domain /5/ and t_r is the time during which the switch is turned on. Typical values for 0.8μm CMOS process are as follows: $\lambda_H = 10^{10} s^{-1}$, $\lambda_L = 4.10^{-21} s^{-1}$, $C_{ox} = 0.8$ fFμm^{-2}, $k_F = 10^{-27}$, A=1 μm^2. By numerical solving of (5), for t_r=0.1 μs, we get V_{fN}=1.2 μV. Because of such a small noise voltage, the influence of the flicker noise can be neglected.

C. Analysis of kT/C and shot noise

Because both kT/C and shot noise are high frequency, they are analysed in this paragraph together. To quantify the effects of the noise on the value symmetry of the flip-flop, it is useful to refer all noise sources to the points 1,2, shown in Fig.4b.

As it is described in paragraph IIa, the switches of the flip-flop are repeatedly turned on in the following order S_3,S_2,S_1, and again S_3. When it holds that C_{S+},C_{S-}>>C_{SW}, where C_{SW} is an output capacitance of the switch, kT/C noise is largely due to sense capacitors C_{S+},C_{S-} . Therefore, RMS of the noise relating to the points 1,2 (see Fig.4a) is given by $V_{Th} = \sqrt{2kT\ C_S}$, where k is the Boltzman constant, T is the thermodynamic temperature, and C_S=(C_{S+}+C_{S-})/2.

Shot noise is due to switches S_1,S_2. Shot noise due to switch S_3 can be omitted, because the noise of this source is equally distributed to the right and left side of the flip-flop. As shown in /5/, RMS of the shot noise of the switch, which is repeatedly turned on and off, leads to

$V_{sh} = \sqrt{qV_m / (2C_{SW})}$ where V_m is maximal voltage across the switch and q is the elementary charge. By means of Duhamel's integral it can be shown that v_1

$$v_1 = at - aR_{eqv}C_{S+} \quad (6)$$

and v_2

$$v_2 = at - aR_{eqv}C_{S-} \quad (7)$$

where function *at* describes the triangular control signal of the flip-flop (see Fig.2). Therefore, the maximal voltage across the switch S_1 is $aR_{eqv}C_{S+}$ and across the switch S_2 it is a value $aR_{eqv}C_{S-}$. In case of our circuit, shot noise due to the switches S_1,S_2 is given by $V_{sh} = \sqrt{\frac{qaR_{eqv}C_S}{4C_{SW}}}$. Thus, the resultant high frequency noise between the points 1,2 of the flip-flop is given by

$$V_{no} = \sqrt{\frac{qaR_{eqv}C_S}{4C_{SW}} + \frac{kT}{C_S}} \quad (8)$$

III. Experimental results

A. Verification of the flip-flop functionality

An experimental circuit was constructed from discrete elements. The switches were realized by means of an integrated circuit 74HCT4066, and the transistors T_1,T_2 in N3515 differential pair were used. Primarily, the existence of two stable states had to be verified. The flip-flop was controlled by triangular impulses with the parameters as follows: $a=0.85\ 10^{-4}\ Vs^{-1}$, T_c=340 μs, and other parameters were t_r=0.1 μs, T_{SW}=0.4 μs, C_{SW}=3.5 pF, and C_{S+} ,C_{S-} about 28 pF.

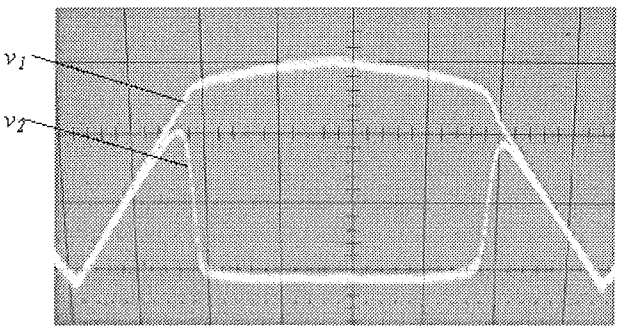

Figure 7. Courses of voltages v_1,v_2

Fig.7 shows oscilloscope courses of the voltages v_1,v_2 . During the experiment the flip-flop according to Fig.4a took the stable state one or zero. It is sufficient evidence of the existence of only two stable states.

B. Influence of a noise

Using (4), (8) and parameter values shown in the previous paragraph it follows that RMS of the total high frequency noise should be about 20 μV.

Fig.8a) shows the change of voltage v_1 which is caused by a charge injection of the switch S_1. When the switch S_1 is turned on, the switch S_2 is turned off and therefore switch charge injection can break the value symmetry of the flip-flop. However, a frequency jitter of the triangular signal must be taken into account in relation to the control frequency f_{SW} of the switches. From this point of view the influence of switch charge injection relating to the points 1,2 (see Fig.4b) is only an additive noise. The resultant probability of distribution is then shown in Fig.8b. As it can be seen, expected RMS of the total noise V_{nois} is 260 μV. Experiments have been carried out to verify this value. The measurement set up is shown in Fig.9a. The impulses from flip-flop outputs were processed, through additive invertors T_3,R; T_4,R, in a personal computer (PC). The measurement procedure first involves the adjustment of the offset compensation voltage V_{of} until 50 % state of the flip-flop is obtained, as shown in Fig.9b. This voltage is then again

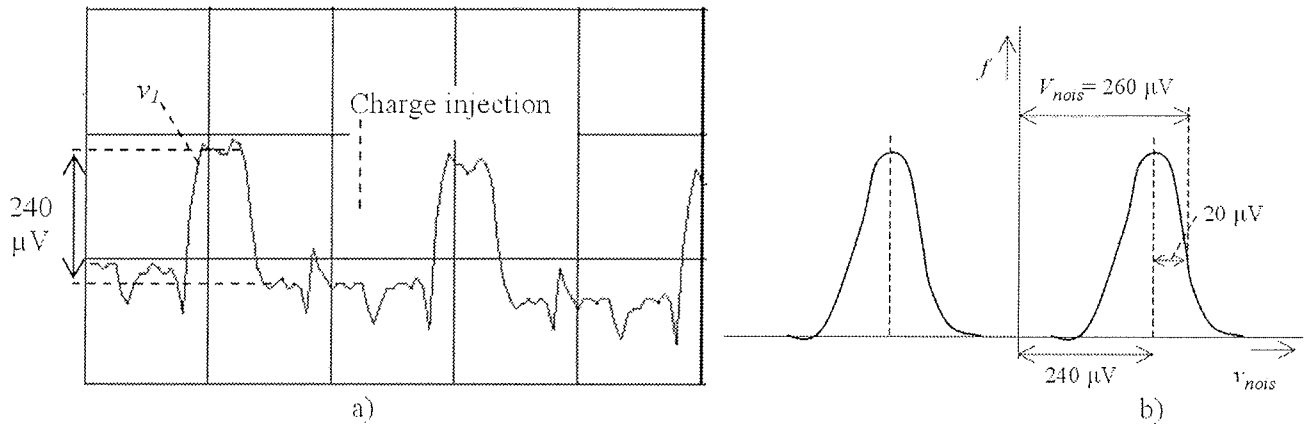

Figure 8a) Charge injection, b) resultant probability of distribution

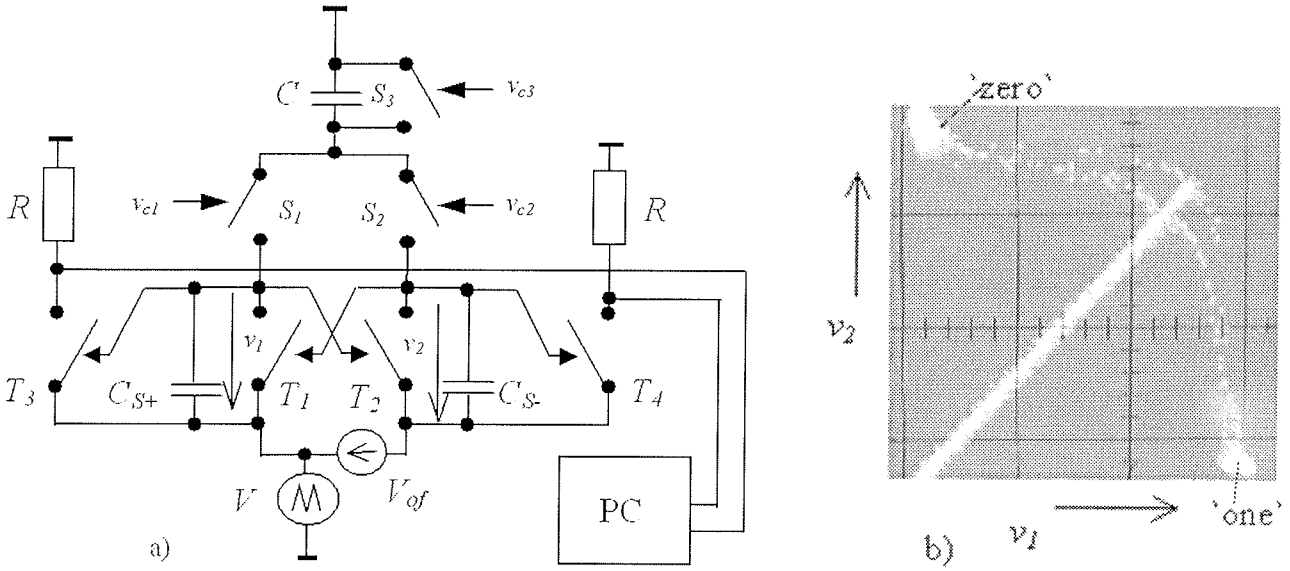

Figure 9a) Measurement set up, b) 50 % state of the flip-flop

tuned until 84 % is obtained. The difference in the two offset voltages is then the RMS of the noise. "Eighty-four percent" is used because this is the probability of obtaining a `one` when the shift in the distribution equals V_{nois}. According to the theoretical conclusion, V_{nois} is 260 μV, whereas the measured V_{nois} was 290 μV.

It is useful to know the measured capacitive error caused by the noise. Since V_{of} is defined as a difference between v_2 and v_1, by means of (6) and (7) we get $V_{of}=aR_{eq}(C_{S+}-C_{S-})$. According to the parameters of our circuit it follows that $V_{of}/(C_{S+}-C_{S-})=1$ mV/pF. Therefore, the noise causes the capacitive error 290 fF.

In another experiment, soma extra capacitors were added to the capacitor C_{S+}. Predicted and measured values of the offset voltage V_{of} are shown in Tab.1.

Table 1. Predicted and measured values of V_{of} in the dependence on an additive capacitance

Additive capacitance [pF]	*Measured voltage* [mV]	*Predicted voltage* [mV]
5.5	5.7	5.5
11.9	11.7	11.9
12.7	13	12.7

IV. Conclusions

A new capacitive sigma-delta modulation technique has been presented. This technique consists in usage of a switched capacitor based flip-flop. Equivalent circuit is then characterized by perfect matched load resistances. Another main advantages in comparison to the ordinary approaches are as follows: negligible flicker noise (only a few μV), simplicity (charge amplifier, comparator and another compensating circuits are not needed), high capacitive sensitivity (in relation to an offset voltage it is 1mV/pF). The capacitive sensitivity may be at need regulated by a control frequency of the switches. A disadvantage is relatively high charge injection of the switches. However, tested circuit was made only from discrete elements. By realization on a chip the substantial enhancement can be expected.

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INTELIGENTNE TEKSTILIJE IN OBLAČILA

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Kjučne besede: inteligentna oblačila, inteligentne tekstilije, področja uporabe

Izvleček: Prispevek podaja pregled dosežkov pri razvoju inteligentnih tekstilij in oblačil, prav tako pa tudi namen in možnosti njihove uporabe. Ker so inteligentna oblačila kot odzivno-sporočilna oblačila kombinacija dodane elektronike, neelektronskih komponent in inteligentnih tekstilnih materialov, so v prispevku predstavljeni tudi inteligentni materiali, ki so nova generacija vlaken, prej in tekstilnih materialov, iz katerih se izdelujejo tovrstna oblačila. Nova generacija vlaken in tekstilnih materialov ter miniaturne elektronske komponente omogočajo izdelavo uporabnih inteligentnih oblačil, ki so obdržala običajen videz, le da je vanje vgrajenih več miniaturnih elektronskih naprav. Nosijo se kot vsakdanja oblačila, ki zagotavljajo pomoč v različnih okoliščinah s širokim spektrom uporabe. Predstavljene so tudi ciljne skupine uporabnikov tovrstnih oblačil, za katere bi se proizvodnja takšnih oblačil lahko začela.

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Intelligent Textiles and Clothing

Key words: intelligent clothing, intelligent textiles, applications

Abstract: The paper gives an overview of achievements in the field of development of intelligent textiles and garments and their end-use. An intelligent garment is a combination of incorporated electronics, non-electronic components and intelligent textile materials. Intelligent materials, which are used for manufacture of intelligent garments, such as new generation fibres, yarns and textile materials are presented. These new materials and miniature electronic components enable production of really useful intelligent garments, which retain their conventional appearance but have electronic components incorporated. They are worn as everyday garments but provide help in many different situations with a wide range of applications. Target user groups for which production of intelligent garments could start are presented.

1.0 Uvod

Inteligentne ali pametne (angl.: smart) tekstilije so nova generacija tekstilnih vlaken, prej in izdelkov, narejenih iz njih, s širokim spektrom uporabe. Inteligentne tekstilije so po eni od definicij definirane kot materiali, ki so zmožni zaznati stimulanse okolja, se nanje odzivati ter se jim prilagoditi /1/. Ti stimulansi, kot tudi reakcije, so lahko električnega, toplotnega, kemičnega, mehanskega, magnetnega in drugega izvora. Glede na način odzivanja delimo inteligentne materiale v tri skupine /1/:

- pasivni inteligentni materiali, ki lahko le zaznavajo stimulanse zunanjega okolja, torej delujejo kot senzorji,
- aktivni inteligentni materiali, ki lahko zaznavajo stimulanse okolja in se nanje odzivajo, torej imajo funkcijo senzorjev in aktuatorjev (sprožilcev) ter
- visoko inteligentni materiali, ki lahko zaznavajo, se odzivajo in se prilagodijo stimulansom zunanjega okolja.

Na trgu se že uveljavljajo številni tekstilni materiali, ki kažejo »inteligentno« obnašanje: npr. uravnavajo toplotno ravnotežje telesa, spreminjajo barve z namenom izboljšanja počutja, nas v primeru športnih aktivnosti ohranjajo suhe, preprečujejo potenje, nas varujejo pred nevarnim sevanjem, itd. K hitremu razvoju inteligentnih tekstilij je pripomogla predvsem vojaška industrija, ki uporablja tekstilije v različne namene, npr. v ekstremnih razmerah za jakne ali uniforme, ki spreminjajo barve za izboljšanje kamuflažnih učinkov /2/; izredno hiter razvoj in prodor elektronskih naprav v različnih izvedbah in funkcijah pa je privedel do ideje o vključevanju teh proizvodov tudi v oblačila in s tem do nastanka t.i. inteligentnih oblačil.
V nadaljevanju bodo predstavljeni inteligentni materiali in oblačila z uporabnega vidika in nakazane ciljne skupine uporabnikov.

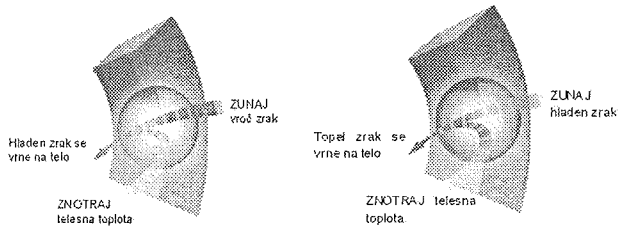
2.0 Inteligentni tekstilni materiali

Inteligentni tekstilni materiali, ki so zmožni zaznati stimulanse okolja, se nanje odzvati ter se jim prilagoditi, imajo čedalje pomembnejše mesto v raziskavah, ki so usmerjene v iskanje novih funkcionalnih lastnosti tovrstnih materialov.

Ena pomembnih lastnosti inteligentnih materialov je vsekakor možnost uravnavanja telesne temperature z dinamičnim shranjevanjem in sproščanjem toplote v temperaturnem območju blizu temperature kože (od 29 do 35 °C) s spreminjanjem agregatnega stanja iz trdega v tekoče in nazaj. Za ta namen so bili razviti t.i. materiali PCMs (PCMs, angl. Phase Change Materials), ki so pri določeni temperaturi izpostavljeni faznemu prehodu. To so materiali z vgrajenimi mikrokapsulami PCMs v vlakna, netkane tekstilije ali pene. Aktivna substanca v mikrokapsuli PCM so lahko različni parafinski voski, pri katerih se izkorišča sprememba toplote, ki jo aktivna substanca sprosti oz. prejme pri spremembi

agregatnega stanja trdo-tekoče in nasprotno, po čemer so tudi dobili ime PCMs. Med spremembo agregatnega stanja mikrokapsula PCMs prejme in akumulira razmeroma velike količine toplote iz svojega okolja. Med ohlajanjem se nakopičena toplota sprosti in s tem pomaga vzdrževati stalno telesno temperaturo /2, 3, 4/. Pionir na področju razvoja tehnologije vgrajevanja mikrokapsul PCMs v vlakna PAN je ameriška družba Triangle Research and Development Corporation (TRDC), ki je za Naso razvila prvi material PCMs pod zaščitnim imenom Outlast®, in sicer za astronavtska oblačila /3/.

Vlakna z vgrajenimi mikrokapsulami PCMs so sposobna absorbirati odvečno toploto, jo shraniti in sprostiti oziroma vrniti telesu, ko jo le-to potrebuje. Poskrbijo torej za aktivno toplotno izolacijsko delovanje. Če npr. telo proizvaja več toplote, kot je sloji oblačila lahko odvajajo v okolje, to odvečno toploto PCMs sprejme oz. absorbira in jo shrani (skladišči); kar človeku daje osvežujoč občutek, slika 1a. Nasprotno pa se pri mirovanju, ko zaradi temperaturne razlike v okolju temperatura telesa pada, odvajanje toplote zmanjšuje, mikrokapsule PCMs sprostijo uskladiščeno toploto, kar daje toplejši občutek, slika 1b. Materiali PCMs, ki shranjujejo ali sproščajo toploto, ko jo telo potrebuje, se uporabljajo za izdelavo oblačilnih predmetov, kot so vetrovke, bunde, jakne, telovniki, športna in smučarska oblačila, delovna oblačila (gasilske uniforme, potapljaška, vojaška in astronavtska oblačila), rokavice, nogavice in spodnje perilo. Lahko se uporabljajo tudi pri posteljnih vzmetnicah in v medicinske namene za obveze, pri opeklinah ter za vroče/hladne terapije /1, 3, 5/.



Slika 1: Uravnavanje telesne temperature z materiali PCMs; a) absorbiranje odvečne toplote b) sproščanje toplote /5/

Naslednji tip inteligentnih tekstilij so materiali z oblikovnim spominom (angl. Shape Memory Materials). To so materiali, ki se na spremembe okolja, tj. temperature ali pH medija, odzovejo s spremembo oblike. To pomeni, da imajo sposobnost vrniti se v neko prej definirano obliko oz. imajo sposobnost »zapomniti« si obliko, sproženo pri toplotnem učinku skozi deformacijsko povrnitev. Na splošno se ti materiali pri nizki temperaturi deformirajo in pri visoki temperaturi povrnejo v svojo prvotno obliko, tj. v obliko pred deformacijo. Uporabljajo se za izboljšanje toplotnega in vlažnostnega uravnavanja funkcionalnih oblačil, kot so športna oblačila, zaščitna oblačila pred mrazom ali toploto, ter za vojaška zaščitna oblačila /6/. Mitsubishi Heavy Industries je razvil nov tip inteligentnega materiala z dimenzijskim spominom za vrhnja oblačila, namenjena aktivnim športnikom. Na poliuretanu temelječi polimerni material z dimenzijskim spominom, imenovan DiAPLEX, je visokoučinkovit material, ki zagotavlja udobnost nepremočljivih oblačil /7/. Za ohranjanje udobne mikroklime znotraj oblačila je diaplex izdelan tako, da reagira pri temperaturi prehoda, kar prilagodi razmere materiala spremembam notranjega in zunanjega okolja. Ko prihaja do aktivnosti ali sprememb v zunanjem okolju, material avtomatično postane ali bolj vodoodporen ali pa bolj vodoprepusten. Diaplex bi torej lahko imenovali kot material, ki obvlada samega sebe. Del Diaplexa je ultra tanka neporozna polimerna membrana. Kot rezultat toplotnega gibanja (ki nastaja znotraj membrane pri vnaprej določeni aktivacijski točki temperature) nastajajo mikropore v membrani, kar omogoča molekulam vodne pare in telesni toploti prehajanje skozi mikropore v zunanjost. Diaplex torej poskrbi za kombinacijo toplotne izolacije in zračne prepustnosti ali prepustnosti vodne pare, saj tedaj, ko je temperatura telesa nizka, omogoča oz. služi za zmanjšanje prepustnosti in preprečitev vstopa zračnih in vodnih molekul skozi membrano, kar omogoča ohranjanje telesne toplote. Ko pa temperatura telesa narašča, toplotno gibanje aktivira mikropore med molekulami membrane ter poveča prepustnost, tako da vodna para in telesna toplota lahko prehajata v zunanje okolje, s čimer se zagotovi optimalno udobje /7/.

Materiali, ki prav tako izkazujejo inteligentno obnašanje, so t.i. barvno aktivni materiali, ki glede na zunanje okoliščine povratno spreminjajo barvo /2/. Poznamo različne vrste barvno aktivnih materialov, ki jih glede na dejavnike, ki vplivajo na spremembo barve, delimo na /2/:

- foto barvno aktivne materiale: odzivajo se na svetlobo,
- toplotno barvno aktivne materiale: odzivajo se na toploto,
- elektro barvno aktivne materiale: odzivajo se na električne impulze,
- (barvno) aktivne materiale, ki se odzivajo na tlak,
- tekočinsko barvno aktivne materiale: odzivajo se na tekočine ter
- barvno aktivne materiale, ki se odzivajo na elektronske žarke.

Pri foto barvno aktivnih materialih se barva spremeni v stiku s svetlobo (material absorbira svetlobo in pri tem spremeni barvo). Poznamo foto barvno aktivne materiale, ki spremenijo barvo v stiku z vidno svetlobo, in materiale, ki spremenijo barvo v stiku z UV svetlobo. Foto barvno aktivni materiali se lahko uporabljajo za izdelovanje »pametnih« oken (angl. *smart windows*), ki spreminjajo barvo, za računalniške prikazovalnike in drugo elektroniko, za vzvratna ogledala v avtomobilih in tovornjakih, foto-kromove leče za sončna očala, nove tipe svetlobnih detektorjev, optična stikala itd. /8/. Poleg navedenih materialov so zdaj na voljo tudi barvno aktivna odzivna vlakna, to so vlakna, ki spremenijo barvo, in vlakna, ki postanejo nevidna. Vlakna oz. preja za tkanje

in pletenje prav tako temeljijo na foto barvno aktivnem efektu, saj prvotno beli material ob izpostavitvi zunanji dnevni svetlobi spremeni barvo. Sedem prvotno belih barv se lahko spremeni v rumeno, modro, vijoličasto, škrlatno, barvo lubenice in morsko zeleno barvo. Na trgu so že tudi štiri nova barvila, ki omogočajo v stiku s svetlobo spremembo iz ene barve v drugo, npr. rumene v oranžno, barvo breskve v barvo vina, turkizno v modro-vijoličasto in svetlo rožnato v temno rožnato /9/. Tekočinsko barvno aktivni materiali pa spreminjajo barvo, ko pridejo v stik s tekočino, npr. z vodo. Ti materiali se ponavadi uporabljajo za kopalna oblačila. Nedvomno najpomembnejše področje uporabe barvno aktivnih materialov je področje modnih oblačil, za oblikovanje zanimivih kreacij, ki spreminjajo barvo v odvisnosti od količine svetlobe. Barvno aktivna vlakna zaradi svoje presenetljive in zanimive narave povečujejo zanimanje ljudi za tovrstne materiale. Za uvajanje teh vlaken v vsakdanje življenje je posebej pomembno dokazati njihovo obstojnost na svetlobi /2/.

Električno prevodni materiali so materiali, katerih električna prevodnost je večja od 10^4 S/cm ($S=1\Omega^{-1}$). To so materiali z visoko vsebnostjo kovin (kovinska vlakna oz. niti iz taljivih kovin, kot so žlahtne kovine in Al, Pb, Fe, Cu, Ni ter zlitine-bromi in medenine) ter elektroprevodni polimeri. Čeprav je na trgu veliko tržnih različic prevodnih materialov, imajo vsi enake ali podobne lastnosti. So lahki, trpežni, prožni in stroškovno konkurenčni. Dve od pomembnih lastnosti prevodnih materialov sta elektromagnetna zaščita in električna prevodnost, zahvaljujoč njihovim posebnim zgoraj omenjenim lastnostim /2/. Raziskovalni tim podjetja *ElekSen* iz Londona, ki dela na razvoju prevodnih materialov, materialov, občutljivih na tlak, elektronike, računalniške programske opreme in proizvodnega inženirstva, je razvil t.i. tehnologijo ElekTex /10/. Gre za visoko spremenljivo in inventivno tehnologijo, ki zagotavlja osnovo za mehke, prilagodljive in prijazne vmesnike med uporabnikom in elektronskimi napravami. Tehnologija je kombinacija senzorskih materialov ElekTex, elektronike ElekTex in programske opreme. Ta struktura materiala lahko natančno zazna položaj na treh oseh (X, Y, Z) znotraj strukture materiala, debeline, manjše od 1 mm. Struktura materialov ElekTex torej ne zaznava samo položaja X-Y (položaja mesta oz. točke delovanja tlačne sile oz. dotika, npr. pritisk prsta), ampak tudi intenziteto tlačne sile (položaj oz. točke delovanja sile), torej Z-os /10/.

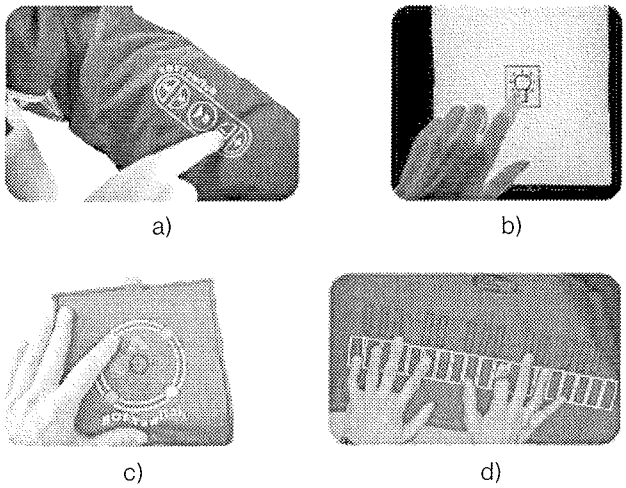
Uporaba materialov, občutljivih na dotik oz. tlak, je raznolika. Ena izmed možnosti je izdelovanje nočnega perila iz tovrstnih materialov, ki bi med spanjem merili tlačne sile telesa na površino ležišča. Na mestih delovanja največjih tlačnih obremenitev bi bilo mogoče skupaj z ležiščem uravnavati ravnino površine ležišča. Tako bi se na mestih največjih tlačnih obremenitev upogibala površina ležišča tako dolgo, dokler se tlačne obremenitve ne bi izenačile, s čimer bi se povečala udobnost spanja, hrbtenica pa bi se postavila v pravilen položaj. Na podoben način bi bilo mogoče meriti tudi tlačne sile, torej tlačno obremenitev na avtomobilskih sedežih, ki bi se električno uravnavala tako dolgo, dokler se tlak, s katerim telo deluje na naslon in površino sedala, ne bi izenačil in povečal udobnost vožnje predvsem na daljših razdaljah.

Za zaznavanje delovanja in merjenje intenzitete tlačne sile ter položaja delovanja sile je podjetje ElekSen razvilo prožno, upogljivo tipkovnico ElekTex, vgrajeno v tekstilni material. Današnji materiali za tipkovnice so v glavnem trdi ali poltrdi materiali v obliki plastičnih ali tiskanih membranskih stikal, ki se najpogosteje montirajo na trdo podlago.

Mehko-stikalna tehnologija t.i. tehnologija **SOFTswitch** materialu omogoča delovati kot elektronska naprava. V resnici to pomeni, da so lahko mehki in fleksibilni materiali uporabljeni na področju konvencionalnih trdih, plastičnih tipkovnic, stikal in gumbov. Materiali SOFTswitch so občutljivi na dotik, tako da se lahko uporabljajo za nadzor in zaznavo tlaka. Lahko neposredno sodelujejo s katerim koli tipom elektronske naprave brez potrebnega podajanja znakov ali softverske interpretacije. Povezava med človekom in napravami postaja torej čedalje bolj mehka; otipljiva in nosljiva elektronika predstavlja del oblačila, ki ga nosimo. SOFTswitch materiali so izdelani z združevanjem lahkih prevodnih materialov z zelo tankim slojem kompozitnega materiala, ki skrbi za delni nadzor elektronskih naprav in preprosto preklapljanje *on/off*. Tekstilne stikalne naprave so izdelane za sodelovanje s katero koli elektronsko napravo, kar je ponavadi izvedeno z uporabo stikal, tipkovnic, gumbov, senzorjev itd.

Ključna komercialna uporabna področja mehko-stikalnih izdelkov SOFTswitch so: »elektronika, ki jo oblečemo« (angl. *wearable electronics*), kot so mehka tipkovnica, jakna z mehko tipkovnico in rokavice, ki omogočajo medsebojno brezžično komuniciranje z elektronskimi napravami v našem domu, v avtu ali na delovnem mestu; odzivno-sporočilne notranje površine, kot so stikala za luč, TV daljinec in druga stikala, ki so vgrajena v notranjost tekstilij v našem domu ali na delovnem mestu za nadzor osvetljave, varnosti, temperature idr. elektronskih naprav; fleksibilne računalniške in igralne naprave, kot so miška, tipkovnica in kontrolna konzola, ki omehčajo plastične komponente ter jih s tem naredijo za uporabnika bolj prijazne; izdelki za učenje (igrače, glasbila in senzorji tlaka, kamor sodijo medicinski materiali občutljivi na tlak, športna oblačila in avtomobilski sedežni senzorji. Nekatere inteligentne proizvode,izdelane iz SOFTswitch materialov prikazuje slika 2 /12, 13/.

Velik pomen lahko danes pripišemo tudi **tekstilijam z elektromagnetno zaščito oz. zaščito pred elektrosmogom**. Elektrosmog se lahko definira kot skupni pojem za vsa namerno povzročena električna in magnetna polja, ki nastopajo oz. izstopajo tam, kjer teče električni tok ali nastaja električna napetost in pogosto povzroča zdravstvene težave pri občutljivih ljudeh, starejših in bolnikih, npr.: utrujenost, stres, depresija, glavobol, nespečnost, nervoza, vedenjske motnje pri otrocih, visok krvni tlak, motnje spanja itd. Nevarno elektromagnetno valovanje oddajajo številne električne in elektronske naprave, ki nas obdajajo na delovnem mestu, kot tudi v zasebnem življenju, npr. računalnik in druge računalniške ter pisarniške



Slika 2: Mehko-stikalni izdelki SOFTswitch /13/ a) jakna z mehko tipkovnico, b) stikalo za luč, c) računalniška miška, d) klaviatura

naprave, gospodinjski aparati, radijske in televizijske naprave, mobilni in brezžični telefoni, javna prevozna sredstva, radarji, medicinska in industrijska oprema, naprave za distribucijo in uporabo električne energije itd. Za zaščito pred električnim poljem se lahko uporabljajo elektroprevodni materiali, kot so kovinska vlakna, pred magnetnim poljem pa t.i. feromagnetni materiali, kot so npr. železovi in nikljevi delci oz. prah. Na trgu so že različni materiali, ki pa največkrat varujejo le pred nizkofrekvenčnim poljem, ne pa pred magnetnim /14/. Po nekajletnem raziskovanju je švicarski firmi *Swiss Shield* /16/ iz Fluma uspelo v sodelovanju s strokovnjaki z različnih področij razviti tanko fino tekstilijo, ki prvič učinkovito varuje pred električnim in elektromagnetnim sevanjem. Deluje po principu Faradayeve kletke. Rešitev so našli v 0,02 mm tanki kovinski niti, ki je skupaj z vlakni oplaščena v nit. Kot las tanka bakrova nit je posrebrena in z bombažnimi ali PES vlakni oplaščena tako, da nastane oplaščena nit s prevodnim jedrom. Tkanina Swiss Shield® je tako stkana, da nastane zelo fina, za oko neopazna kovinska rešetka. Le-ta deluje kot ogledalo, ki odbija vpadne žarke več kot 99-odstotno. Tkanina je svetovno patentno-pravno zaščitena in optimalno varuje pred elektromagnetnim valovanjem (z 90 - 99-odstotnim učinkom zaščite) ter široko paleto uporabe. Je zelo tanka in prosojna, pralna pri 30 °C, prožna ter dosegljiva v različnih dizajnih (v različnih barvah in tisku) in se enostavno predeluje za različne namene uporabe, npr. za zaščitna in delovna oblačila, zavese, baldahine in predelne stene, posteljno perilo, zaščitne sisteme za tla, stene in strop, zaščitne sisteme za industrijsko varnost itd. /15/.

Poleg navedenih je potrebno omeniti tudi Tekstino, d.d., v Ajdovščini, ki je razvila novo blagovno znamko tkanin in prej bombažnega tipa, imenovano Tekstim, ki učinkovito ščitijo pred škodljivimi elektromagnetni sevanji (EMS). Tkanine in preje Tekstim bombažnega tipa imajo vgrajena nerjaveča kovinska vlakna, ki ščitijo pred škodljivim EMS tako, da odbijajo okrog 80 % vpadnega signala EMS v frekvenčnem območju 10 do 1000 MHz. Visokofrekvenčno območje od 10 do 1000 MHz je praktično območje vseh visokofrekvenčnih virov EMS, kamor spadajo radio, TV, vsi oddajniki, radiodifuzija, mobilni telefoni, bazne postaje, radarji, repetitorji in drugi oddajniški sistemi. Raziskave učinkovitosti slabljenja tovrstnih metaliziranih tkanin so potrdile uporabnost teh tudi za ljudi z vgrajenimi elektronskimi implantanti ali srčnimi spodbujevalniki /16/. Preje in tkanine Tekstim so namenjene izdelovanju lahkih zaščitnih oblačil, dnevnih oblek, spodnjega perila, dekorativnih tkanin in drugih zaščitnih izdelkov /16/.

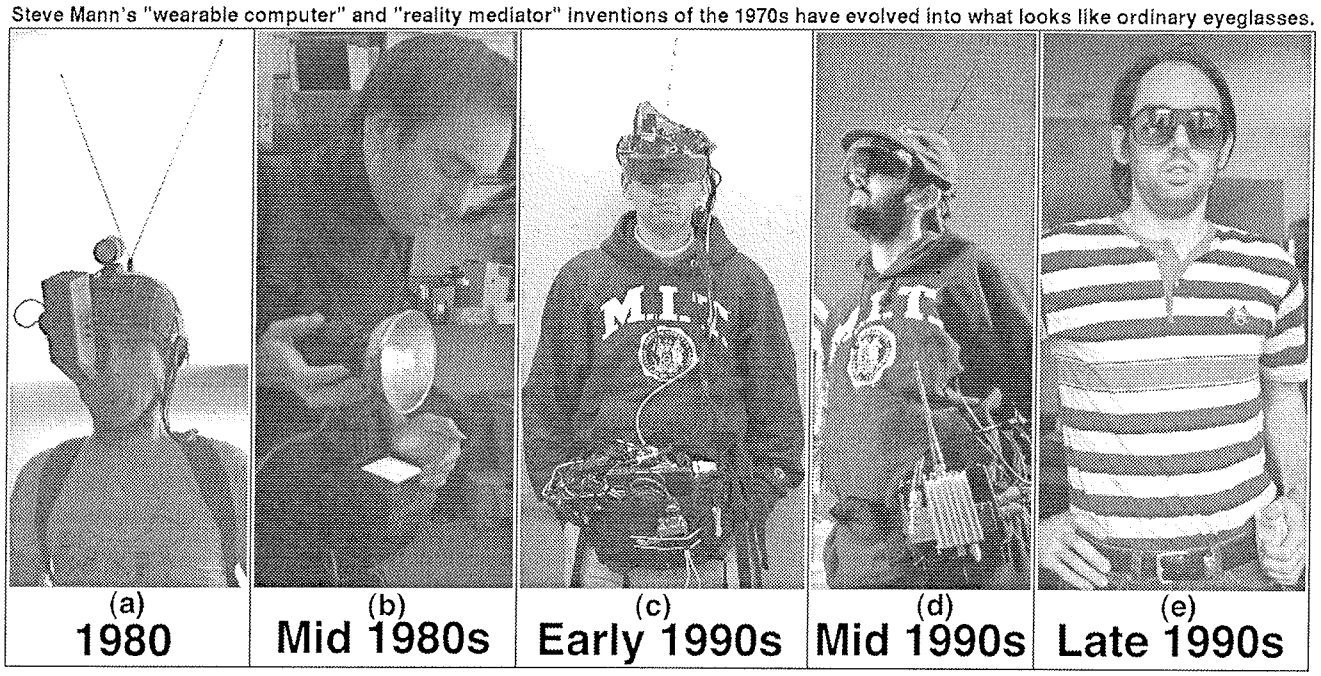
K inteligentnim tekstilijam prištevamo tudi **optična vlakna**, ki se v tekstilnih izdelkih uporabljajo v dva različna namena, in sicer za optične senzorje za merjenje temperature, tlaka in prisotnih plinov, ter kot vlakna, ki so sposobna prenašati svetlobni signal na velike razdalje. Na hongkonški Polytechnic University so razvili različna sredstva z uporabo optičnih vlaken, namenjena merjenju tlaka in temperature v kompozitnih materialih. Steklena optična vlakna v tekstilnih strukturah pa se uporabljajo tudi za izdelovanje gibkih prikazovalnikov. Ti prikazovalniki temeljijo na tkaninah, izdelanih iz optičnih vlaken in klasičnih prej. Video zasloni LCD ali CRT niso primerni za vgrajevanje v inteligentna oblačila zaradi svoje notranje togosti ter precej velike prostornine in svoje teže. Novi tekstilni gibki prikazovalniki olajšajo, poenostavijo in premostijo slabe strani teh težkih zaslonov. Razvoj fleksibilnih prikazovalnikov, ki temeljijo na optičnih vlaknih, odpira nova področja, kot so inteligentna in komunikacijska oblačila, avtomobilska in hišna oprema ter dekorativna oprema. Prototip optičnega prikazovalnika (OFFD, angl. *optical fibre flexible display*) je bil predstavljen na Avantexu 2002 /17/.

3.0 Razvoj inteligentnih oblačil

Ljudje uporabljamo več in več elektronskih izdelkov; mobilne telefone, prenosne računalnike, dlančnike, osebne hi-fi naprave in še marsikaj drugega. Izredno hiter razvoj in prodor elektronskih naprav v različnih izvedbah in funkcijah je privedel do zamisli o vgrajevanju teh izdelkov tudi v oblačila.

Tako zasledimo prve vgrajene mikroračunalnike v oblačila in s tem razvoj prvih t.i. inteligentnih oblačil že v poznih 70. letih prejšnjega stoletja. Tedaj je bil tudi prvič vpeljan pojem »nosljiv računalnik« (angl. *wearable computer*), in kasneje pojem »pametno« oblačilo (angl. *smart clothing*). Številni strokovnjaki, ki se ukvarjajo s tekstilnimi materiali in oblačili, pojmujejo leto 2000 kot obdobje prvega izrazitega pojava t.i. inteligentnih oblačil; to so oblačila, ki kažejo lastnost »inteligentnega«, odzivnega obnašanja.

Številni raziskovalci, ki sodelujejo pri razvoju inteligentnih oblačil, štejejo Steva Manna za idejnega ustvarjalca tovrstnih oblačil, saj se je v poznih 70. oz. zgodnjih 80. letih prejšnjega stoletja začel zanimati za brezžične računalniške sisteme, ki bi se lahko nosili na telesu /18/. Prvi njegov prototip oz. izdelek »v oblačilo vgrajenega računalnika« je nastal v 80. letih prejšnjega stoletja. Nekoliko čuden prvi



Slika 3: Prototip „nosljivega računalnika" skozi leta razvoja /18/ a) zgodnja 1980, b) sredina 80. leta c) zgodnja 90. leta, d) sredina 90. let, e) pozna 90. leta

prototip z 1,5-palčnim zaslonom CRT je morala podpirati kolesarska čelada in je lahko prikazoval le 40 znakov besedila. Čelado je pozneje nadomestil pas, v katerega so bile vgrajene komunikacijske naprave. V zgodnjih 90. letih je nastal udoben in praktičen sistem na podlagi očal (z 0,6-palčnim zaslonom CRT), ki so se pozneje spremenila v sodobnejši vizir, kjer je sporazumevanje omogočila antena, vgrajena v pokrivalo. V sredini 90. je nastal prototip, ki združuje komercialno dosegljiv prikazovalnik izdelovalca Kopin (ameriški izdelovalec naglavnih prikazovalnikov) skupaj s komercialno dosegljivo celično komunikacijo. Prototip, ki je nastal v poznih 90., je skoraj neločljiv, sestavljen iz naglavnih očal in računalnika, ki ga oblečemo pod majico. Slika 3 prikazuje razvoj Mannovega prototipa »računalnika, ki ga oblečemo« (*wearable computer*) /18/.

S. Mann se že od 1980. leta kot avtor raziskovalnega projekta na *Massachussets Institute of Technology* (MIT) v Cambridgeu ukvarja z raziskovanjem in možnostmi reševanja tehničnih problemov nemotene uporabe računalnikov in njihovih zunanjih enot, vgrajenih v oblačila. Iz raziskav v letih 1980-1996 je videti, kako se z razvojem računalniške tehnike in opreme zmanjšujeta teža in dimenzije računalniških komponent, rastejo pa njihove procesne zmogljivosti ob nenehnem zniževanju proizvodnih stroškov. Pri tem je prišel do spoznanja, da so računalniki dovolj majhni za vgradnjo v oblačilne predmete in da je njihova vgradnja zelo praktična, saj jih lahko ves čas uporabljamo, uporabnikom pa jih ni treba nositi v posebnih torbah. S. Mann je tako postal avtor imena w*earable computer* tj. računalnika, vgrajenega v oblačila in kasneje tudi pojma *smart clothing* (pametna oblačila). Poleg tega je postavil niz zahtev in funkcij, ki bi jih tovrstna oblačila morala vsebovati oz. bi morala biti obvezno opremljena z zmogljivim PC računalnikom z vgrajenimi kamerami, računalniškimi kazalci in drugimi senzorji, ki so mrežno in brezžično vezani na internetno omrežje /18, 11/.

Nova vlakna in tekstilni materiali ter miniaturne elektronske komponente omogočajo izdelavo resnično uporabnih inteligentnih oblačil, ki so obdržala običajen videz, le da je v njih vgrajenih več miniaturnih elektronskih naprav, ki se v veliki meri uporabljajo v vsakdanjem življenju in so nastale kot posledica intenzivnega tehnično-tehnološkega razvoja elektronike, še posebej miniaturizacije elektronskih komponent. Nosijo se kot vsakdanja oblačila, ki zagotavljajo pomoč v različnih okoliščinah s širokim spektrom uporabe /19/.

3.1 Prva inteligentna oblačila

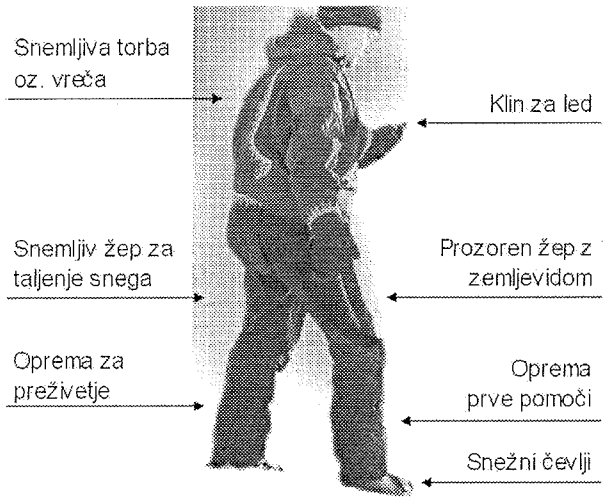
Od leta 1998 se z razvojem inteligentnih oblačil ukvarja večje število podjetij. Tako delujejo znana podjetja, kot so Reima-Tutta, DuPont, Nokia, Polar Electro, Suunto idr., v okviru projekta »**Smart Clothing project**«, ki so v sodelovanju z raziskovalno skupino s Tampere University of Technology in University of Lapand iz Finske konec marca 2000 predstavila *prototip inteligentnega oblačila*, namenjenega predvsem *voznikom motornih sani* (angl. *snowmobile*) /19/. Oblačilo je bilo razvito za primere, ko se uporabnik izgubi v arktičnem območju, pade v hladno reko ali jezero, doživi nesrečo ali okvaro na snežnih saneh, se znajde v temi, doživi nenaden napad kakšne bolezni ali pa v primeru podhladitve. Inteligentno oblačilo za voznike motornih sani je sestavljeno iz dveh spodnjih oblačil, zaščitnega telovnika ter jakne in hlač. Oblačilo je zmožno dajati sporočila o zdravju, lokaciji in gibanju uporabnika. Z različnimi vgrajenimi senzorji je mogoče spremljati uporab-

nikovo zdravstveno stanje in položaj gibanja. Če uporabnik doživi nesrečo ali naleti na kakšno drugo nenormalno okoliščino, oblačilo avtomatično pošlje sporočilo v bolnišnico z informacijami o splošnem stanju uporabnika ter o tehničnih ali drugih težavah. Sporočilo vsebuje trenutne koordinate uporabnikovega položaja in podatke o fizioloških parametrih uporabnika. Funkcionalna arhitektura je dovršena z uporabo navigacijskega sistema GPS, telefona GSM za komuniciranje, pozivnika SOS in kompasa. Senzorski sistem je sestavljen iz tipala za merjenje srčnega utripa, treh senzorjev za določanje položaja in gibanja, desetih tipal za merjenje temperature, enega elektroprevodnega senzorja in dveh parov senzorjev zaznave. Pozivnik SOS se lahko aktivira ročno ali avtomatsko s spremljanjem telesnih funkcij, ki prikazujejo potrebo po pomoči. Oblačilo ima osnovne lastnosti določanja točne lokacije (skozi koordinate 3 do 12 satelitov), komunikacije in zaščite v hladnih okoliščinah. Skupaj z vgrajeno opremo oblačilo tehta 4,5 kg. Elektronski dodatki so vgrajeni v notranjost oblačila, da so blizu površine telesa, s čimer so zaščiteni pred nizkimi temperaturami, čeprav delujejo do temperature -20 °C. Oblačilo je sestavljeno iz treh slojev toplotne zaščite, od katerih se lahko notranji sloj ob telesu, še električno ogreva. Oblačilo, ki omogoča ohranjanje telesne toplote in je zračno prepustno ter hkrati neprepustno za vodo in vremenske vplive, je izdelano iz materialov outlast (material PCMs) in gore-tex. Sprejemne in oddajne antene so izdelane iz električno prevodnih vlaken. V oblačilo je vgrajena baterija, ki omogoča 24-urno neprekinjeno delovanje in se lahko napolni prek napetostne vtičnice na snežnih saneh. Posebna zanimivost so vgrajene naprave, ki lahko zaznajo trčenje, padec, gibanje ali mirovanje ponesrečene osebe, in drugi senzorji, ki spremljajo delovanje srca in utripa ter telesne temperature med reševanjem ponesrečenega.

Oblačilu za pomoč uporabniku v nesrečah ali za zaščito oblačilnih funkcij so dodane različne neelektronske posebnosti. To so npr. snemljiva neprepustna in nepremočljiva torba oz. vreča, ki uporabnika štiri ure varuje pred podhladitvijo, snemljiv negorljiv žep za taljenje snega (za pridobivanje vode), prva pomoč, prozoren žep z zemljevidom itd. Na sliki 4 so prikazane posebnosti polarnega inteligentnega oblačila /1, 19, 20/.

Oktobra 2001 je finska oblačilna družba **Reima** predstavila prvo inteligentno oblačilo v evropskih državah, t.i. Reima Smart 3305. Mobilni telefon, povezan z miniračunalnikom, zvočnikom in mikrofonom, je integriran v jakno in omogoča boljše komuniciranje med skupino, na primer deskarjev na snegu. Prvo komercialno oblačilo Reima Smart 3305 je izdelano za enostavno sporazumevanje in je nekakšen »oblečen« dodatek k telefonu GSM. Uporablja se za pošiljanje glasovnih sporočil med skupino uporabnikov /20/.

Podjetji **Lewi's** in **Philips**, ki sodelujeta pri projektu, sta prehitela družbo Reima in dala na trg svojo prvo kolekcijo oblačilnih izdelkov z integrirano računalniško mrežo. Lewi'sove ICD+ jeans jakne z integrirano komunikacijsko



Slika 4: Posebnosti polarnega inteligentnega oblačila /20/

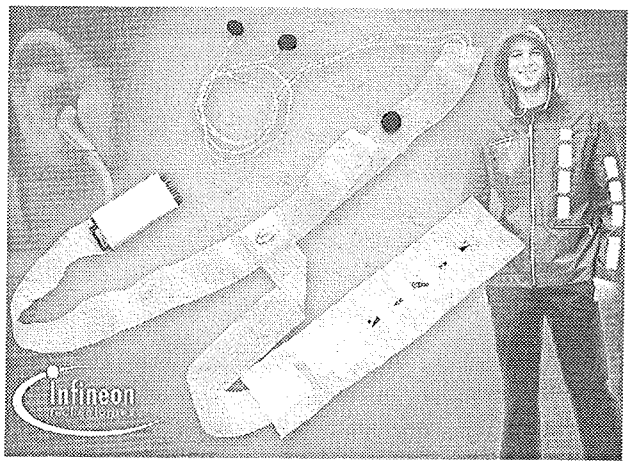
mrežo, ki uporabniku omogočajo stalno povezanost z internetom, so bile že jeseni leta 2000 na trgu (za 990 EUR). Oblačila, blagovne znamke Lewi's ICD+ (Industrial Clothing Devision), imajo vgrajen mikrofon, slušalke, vstavljene na ovratniku jakne, Philipsov mobilni telefon in prenosni MP3-predvajalnik. Philips je posebej za ta oblačila razvil komunikacijski sistem z daljinskim upravljanjem, ki uporabniku omogoča preprosto uporabo mobilnega telefona in MP3-predvajalnika. Pred pranjem oblačila prenosni telefon in MP3-predvajalnik preprosto odstranimo /21/.

Na Avantexu 2002 je bilo predstavljenih kakih 100 novosti na področju t.i. high-tech oblačil, med njimi tudi **Infineon Technologies AG.** Infineon Technologies je aprila 2002 prvič predstavil rešitve za t.i. *wearable electronics* (v oblačilo integrirano elektroniko) in inteligentne tekstilije. Poleg tega je predstavil tehnično dovršene, robustne in delovno sposobne prototipe z mikroelektronskim vezjem, vgrajenim v inteligentne tekstilije oz. oblačila. V kategoriji novih t.i. high-tech oblačil je Infineon prejel nagrado za *miniaturni termogenerator*, ki izrablja temperaturno razliko med površino telesa in obdanim oblačilom, za pridobivanje električne energije. Ker ljudje proizvajamo energijo v obliki telesne toplote (nekateri celo nekaj 10 W) so raziskovalci Infineona del te energije poskusili uporabiti oz. izrabiti. To so jim omogočili polprevodni materiali, kot je silicij, ki ustvarja električno izhodno moč nekaj mW/cm2. Za doseganje visoke temperaturne razlike so termogeneratorji neposredno združeni s tkanino, da dosežejo dober toplotni kontakt s kožo. Dve majhni bakreni ploščici (prevlečeni s srebrom ali zlatom) sta nameščeni, ena na zunanji, druga na notranji strani, za izkoriščanje visoke toplotne prevodnosti teh materialov /22, 23/. Termogeneratorji imajo veliko možnosti za potencialno uporabo v inteligentnih oblačilih, saj lahko služijo za napajanje naprav, vgrajenih v oblačila. Proizvodnja energije od 100-300 mW zadostuje za pogon medicinskih senzorjev (senzorjev za merjenje telesne temperature, srčnega utripa, krvnega tlaka), kot tudi za brezžično oddajanje podatkov v kontrolnih napravah in za mikroelektronske čipe. To daje pacientom več svo-

bode v primerjavi s standardnimi napravami, ki so povezane s kabli. Možnost uporabe se kaže tudi pri sodobnih slušnih aparatih, kjer lahko z uporabo termogeneratorjev namesto baterij zmanjšamo stroške. V primerjavi z baterijami imajo termogeneratorji naslednje prednosti /23/:

- so pralni in vzdržljivi,
- sestavljeni so iz ekološko prijaznih materialov in
- imajo neomejen življenjski čas.

Raziskovalci Infineona so v sodelovanju z dijaki srednje šole za oblikovanje (*Deutschen Meisterschule für Mode*) iz Münchna razvili jakno z integriranim MP3-predvajalnikom, slika 5. Predstavili so t.i. govorno upravljan (angl. *speech-controlled*) MP3-predvajalnik, ki je sestavljen iz centralnega avdiomodula, pomnilnika za glasbene podatke, snemljive baterije in multimedijske kartice, slušalk in mikrofona ter fleksibilne tipkovnice s senzorskim modulom.



Slika 5: *Jakna z integriranim MP3-predvajalnikom /22/*

Vse elektronske enote so medsebojno povezane z ozkim trakom z vgrajenimi prevodnimi nitmi. Elektronika MP3-predvajalnika je vgrajena neposredno na oblačilne dele in zavarovana tako, da prenese celo pranje oblačila. Proizvajalci oblačil lahko pralen MP3-paket našijejo neposredno na oblačilne dele /22, 24/

Izdelovalec športnih oblačil **O'Neill Europe** je v sodelovanju z **Infineon Technologies** razvil jakno, imenovano »The Hub«, ki je namenjena deskarjem na snegu. Ta predstavlja inovacijo v O'Neillovi zimski kolekciji 2004/05. »The Hub« mobilni komunikacijski center s čipom, ki ga je razvil Infineon, združuje prenosni 128 Mb MP3-predvajalnik, tehnologijo Bluetooth za mobilni telefon ter mikrofon, vstavljen v ovratnik jakne, ki omogoča prostoročno telefoniranje /25/.

Zanimiva novost na področju inteligentnih oblačil so tudi tekstilne elektronske etikete (angl. *smart labels*), ki so jih začeli vgrajevati v svoje izdelke proizvajalci oblačil. Gre za tanke in upogljive radiofrekvenčne čipe, imenovane tekstilne elektronske etikete. Sestavljene so iz majhnih mikročipov RFID, ki shranjujejo različne informacije, ter integrirane antene, s katero se informacije brezžično, torej brez električnih kablov, medsebojno izmenjujejo. Vgrajeni radiofrekvenčni čipi (RFID, angl. *Radio Frequency Identification*) se lahko uporabljajo v proizvodnji, za spremljanje proizvodnega procesa izdelave oblačil ter upravljanje z avtomatiziranim medfaznim transportom v proizvodnji. Spominske zmogljivosti tovrstnih čipov so se povečevale, tako da je mogoče kodiranje tudi niz drugih informacij, kot so informacije o surovinski sestavi, velikostni številki ter natančnih podatkov o načinih vzdrževanja in nege oblačila. Ti čipi se lahko uporabljajo tudi pozneje, npr. v velikih pralnicah in kemičnih čistilnicah za avtomatsko razvrstitev oblačil po programu pranja ali čiščenja, kot tudi kasneje med razvrščanjem distribucijskim centrom oz. lastnikom oblačil /22, 26/. Francosko podjetje **Tagsys**, ki je pionir v razvoju 13,56 MHz etiket, je izdelalo čip z optimalnim spominom, velikostjo in podatkovno strukturo. Tagsys RFID čip, izdelan za sledenje umazanega perila v velikih pralnicah, se lahko z zelo majhnimi stroški neposredno vstavi že v procesu izdelave oblačil ali pa v pralnicah z uporabo avtomatskega sistema (angl. *Automatic Chip Attachment System*). Predstavili so ArioTM 10 - TL čip, ki deluje na frekvenci 13,56 MHz, masa čipa znaša 2,54 g, oblika diska pa ima premer 22 mm in debelino 2,8 mm. Lahko zdrži 200 pranj po 16 minut pri temperaturi 85 °C in 200 ciklusov sušenja v trajanju po 10 minut v tunelskem finišerju pri temperaturi do 180 °C. Odporen je tudi proti kemikalijam, uporabljenim pri čiščenju in sušenju /27/.

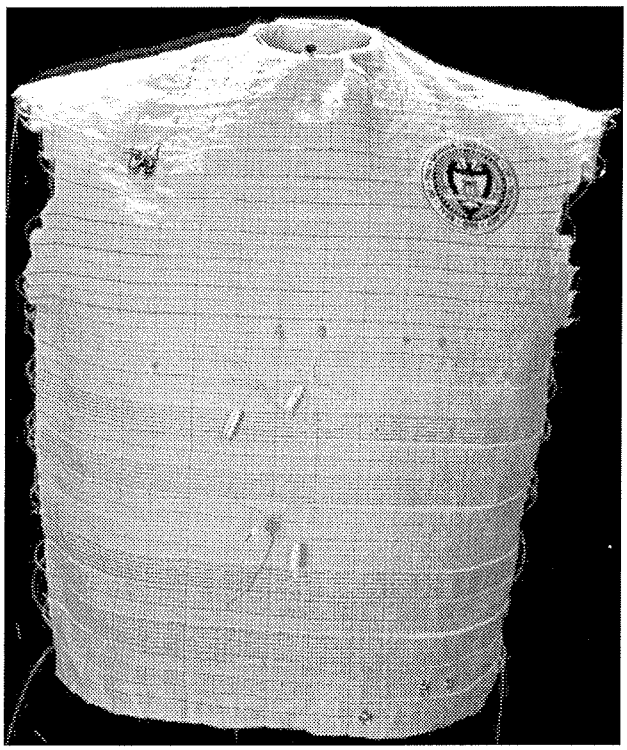
Zanimive so tudi novosti na področju novih zvrsti oblačil. Tako je italijanska modna oblikovalka **Alexandra Fede** na Avantexu 2002 predstavila popolnoma nov tip oblačila, t. i. aktivnega oblačila (angl. *activating apparel, a-apparel*). Udobnost med nošenjem se doseže z nežnimi masažnimi in vibracijskimi blazinicami, ki so vgrajene v večerno ali poslovno obleko. Te lahko obvladujemo z majhnim računalniškim čipom, ki aktivira eno ali več vgrajenih blazinic tako, da je na uporabnikovi koži povzročen prijeten spodbujevalni učinek. Lahke in gibke vibracijske blazinice (angl. *vibrapads*) nihajo programirano. Majhna krmilna blazinica z elektronskim čipom sproži - glede na program - tresenje ene ali več vibracijskih blazinic, ki uporabniku oblačila oddajajo prijetne spodbujevalne občutke. Vibracije na t.i. JoyDress obleki se programirajo na zelo enostaven način /28/.

Sächsisches Textilforschungsinstitut *e.V* iz Chemnitza je razvil inventivno inteligentno zaščitno oblačilo za gasilce z vgrajenim elektrosenzorskim sistemom, ki naj bi z različnimi senzorskimi enotami varoval človeka pri izpostavljenosti npr. pri visokih temperaturah ali elektromagnetnemu sevanju. Elektro-senzorska zaščitna obleka ima naslednje funkcije /29/:

- toplotni senzorji, vgrajeni oz. vstavljeni na zunanji in notranji strani oblačila, zaznavajo toplotno izpostavljenost,
- merjenje in nadziranje dihalne frekvence ter srčnega utripa za spremljanje zavesti gasilca,

- spremljanje temperature zunanjega in notranjega ogrinjala za preprečitev lokalnih kožnih opeklin in za določitev stopnje toplotnega tveganja,
- zaznavanje nepričakovanih močnih zunanjih vplivov (npr. EM sevanje),
- določanje lege oz. kraja nesreče gasilca s pomočjo sistema GPS (12-ih satelitov na 20000 m višine),
- vsi ugotovljeni podatki se prek modema posredujejo na gasilsko postajo.

Na Univerzi Georgia Tech iz Atlante so razvili jopič, ki je nekakšna »računalniška osnovna plošča, ki jo lahko oblečemo« (angl. Georgia Tech Wearable Motherboard-GTWM), slika 6. V začetku razvoja je bil namenjen predvsem za vojaške potrebe. Jopič je izdelan iz optičnih vlaken za odkrivanje položaja strelne rane na telesu in posebnih senzorjev, ki spremljajo fiziološke funkcije uporabnika med vojaškimi aktivnostmi. GTWM je stkan tako, da so optična vlakna (POF) in druge posebne niti vgrajene v strukturo tkanine brez vidnih prekinitev. GTWM je za komercialno uporabo izdelan pod imenom »*Smart Shirt*« firme Sensatex. Inteligentni jopič, ki se obleče pod oblačilo, je pralen in se vzdržuje po ustaljenih postopkih čiščenja. Uporablja se v vojaške namene, prav tako pa tudi za merjenje in spremljanje življenjskih telesnih funkcij športnikov, bolnikov in starejših oseb, ki so oddaljeni od medicinskih središč, za spremljanje razvoja bolezni, spremljanje stanja novorojenčkov in za potrebe posebnih služb /1, 30/.



Slika 6: »Računalniška osnovna plošča, ki jo lahko oblečemo«, »Smart Shirt« /1, 30/

5.0 Ciljne skupine uporabnikov

Inteligentna oblačila bodo na začetku zelo draga. Kljub temu pa obstajajo ključni uporabniki, ki bi bili pripravljeni plačati visoko ceno za ugodnosti, ki jih ponuja uporaba različnih vrst inteligentnih oblačil.

Prva ciljna skupina uporabnikov je vsekakor **vojska**. Inteligentna, odzivno-sporočilna vojaška oblačila bodo imela vgrajene senzorje, predvsem zvoka, toplote, navigacijskega in komunikacijskega sistema, radarje ter avtonomno napajanje vseh vgrajenih naprav za šest dni. Oblačilo naj bi imelo možnost spreminjanja barv v skladu z okoljem, v katerem se bo nahajal vojak, in bo uporabljalo tehniko spreminjanja barv v veznih točkah. Imelo naj bi tudi možnost regulacije premera por na oblačilu, s čimer se ustvari aktivna filtracija zraka, predvsem prepuščanje kisika in zadrževanje vhoda vojaških strupov in drugih nečistoč. Poleg tega bo imelo aktivno toplotno zaščito ter vgrajeno tehnično opremo. Inteligentna oblačila za vojsko bodo verjetno tudi varovala pred vdorom nabojev, torej bodo odporna na udarce in preboj. V primeru strelne rane bo na mestu preboja naboja v telo nastala prekinitev v vlaknih, katero bo tovrstno oblačilo zaznalo. Tako bo mogoče natančno določiti lokacijo rane na telesu, na podlagi katere se bo lahko ocenila prioriteta sanacije rane. Podatki o lokaciji rane, izgubi krvi, srčnem impulzu ipd. bodo neposredno poslani ekipi, ki skrbi za ranjence. Predvideva se, da bo vojska prva pomembna skupina uporabnikov inteligentnih oblačil.

Druga skupina so **delovna odzivno-sporočilna oblačila**, namenjena delavcem v gradbeništvu, ladjedelništvu, velikih skladiščih idr. ter pri vrstah nadzornih aktivnosti, ki se potekajo na velikih površinah. Oblačila, namenjena nadzoru industrijskih procesov, bodo opremljena z zmogljivim brezžičnim računalnikom z zelo velikim spominom, v katerega se bodo shranjevali procesni parametri in baze znanja strokovnih sistemov. Poleg tega bo opremljeno z večjim številom senzorjev za spremljanje industrijskih procesnih parametrov oz. vrednosti.

Tretja ciljna skupina so inteligentna oblačila, namenjena **poslovnežem**. Njihova oblačila bodo navzven obdržala strogo poslovno obliko, le da bo v oblačilo vgrajenih veliko elektronskih naprav, ki se uporabljajo za poslovne aktivnosti. Najbolj značilna aktivnost je vsekakor stalna povezanost z internetom ter prek njega s pisarno in z vsemi poslovnimi napravami, nameščenimi v pisarni. Poslovni človek bo lahko med svojo odsotnostjo prejemal in pošiljal poslovna poročila in urejal razne zadeve, kot da bi bil v pisarni. Prav tako bo lahko vzpostavil komunikacijo s svojim avtomobilom, izbral najboljšo pot med vožnjo (tudi v primeru prometnih zamaškov) ali pa se sporazumeval s trgovinskim centrom, v katerega bo namenjen. Neposredno pred prihodom domov bo lahko po internetu in brezžični telefonski zvezi nastavil želeno temperaturo v hiši ali stanovanju, vključil klimatsko napravo, štedilnik, mikrovalovno pečico s pripravljeno hrano, ali celo zalivanje cvetja ob daljši odsotnosti od doma.

Četrta ciljna skupina so ljudje, ki bodo inteligentno oblačilo uporabljali za **spremljanje svojega zdravstvenega stanja** ali **določene terapije**. Ta oblačila bodo imela vgrajene različne senzorje za spremljanje telesnih funkcij, npr. senzorje za merjenje srčnega utripa, telesne temperature, temperature okolice, plinov in onesnaženosti zraka itd. Odvisno od potreb uporabnika bi takšna oblačila lahko imela vgrajene senzorje, ki bi spremljali ciljne zdravstvene parametre, npr. količino sladkorja v krvi, ter vgrajen računalnik, ki bi skrbel za določene terapevtske potrebe ali vnaprej vodil določeno terapijo s časovno reguliranim dajanjem zdravil skozi upravljane membrane (nameščene v obliki obližev na človeško kožo). Poleg tega bi oblačila lahko imela vgrajen senzor SOS, če bi uporabnik potreboval kakršno koli pomoč, ter vgrajen navigacijski sistem GPS za določanje trenutne lege uporabnika v primeru nesreče ali klica na pomoč.

Peta ciljna skupina so **mladi**, ki zelo dobro sprejemajo in spremljajo izdelke sodobne tehnologije. Mladi bi nosili inteligentna oblačila z vgrajenimi MP3- in CD-predvajalniki, mikrofonom, zvočniki, slušalkami, računalniškimi igricami ter integriranimi videosistemi z vgrajeno miniaturno kamero. Zanimivo je, da se je proizvodnja takšnih oblačil z vgrajenimi elektronskimi napravami že začela in da so nekateri izdelki, namenjeni mladi populaciji, na trgu že dosegljivi. Tu pa ne smemo pozabiti na zaščito uporabnika inteligentnega oblačila pred elektrostatičnim in magnetnim poljem oz. elektromagnetnim sevanjem raznih naprav, vgrajenih v oblačilo. Zato je treba uporabljati tekstilne materiale z različno prevodnostjo (npr. prevodne materiale), tako da njihov določen del omogoča zaščito telesa pred sevanjem vgrajenih elektronskih naprav.

Šesta ciljna skupina so **športniki in rekreativci**. Športna inteligentna oblačila bi služila za zapisovanje in spremljanje vseh podatkov med večjimi telesnimi obremenitvami pri doseganju vrhunskih rezultatov, spremljanju telesnih naporov ter spremljanju in analizi rezultatov treninga. Pri rekreativnih športnikih bi bila tovrstna oblačila izdelana v »blažji« obliki. Za osebe, ki dosti truda vložijo v svoj telesni videz in kondicijo, bi oblačila imela vgrajene senzorje hoje, ki bi beležili število korakov, dolžino hoje in hitrost hoje, na podlagi katerih bi lahko izračunali porabljeno telesno energijo. Računalnik bi prikazoval porabljeno telesno energijo in izračunal količino energije, ki bi jo taka oseba še morala porabiti, kot tudi pripadajoče telesne aktivnosti, da bi dosegla želeno dnevno porabo telesne energije za ohranjanje optimalne fizične pripravljenosti in telesne teže. Vgrajeni senzorji bi lahko vsak dan spremljali aktivnosti osebe, zbirali, shranjevali ter analizirali podatke na podlagi umetne inteligence. Vse elektronske naprave, vgrajene v oblačilo, bi morale zadovoljevati zahteve upogibanja in prilagajanja gibanju telesa. To se nanaša predvsem na spominske naprave, ki bi se vgrajevale v podlogo, oblačila ter tipkovnice in računalniške zaslone, ki bi se vgrajevali na zgornje dele rokava, v bližini sklepa pesti leve roke. Poleg tega morajo biti naprave odporne proti udarcu, dežju in temperaturnim spremembam ter morajo prenesti vse postopke nege in vzdrževanja takšnega oblačila.

Sedma ciljna skupina bi bili **vsi drugi ljudje**, ki niso zajeti v zgornjih skupinah in ki bi inteligentno oblačilo uporabljali za natančno določen namen. Po potrebi in individualnih željah bi se po nakupu takšnega oblačila poljubno dograjevale posamezne naprave, s čimer bi oblačilo služilo natančno določenemu namenu.

5.0 Sklep

Tekstilni materiali in oblačilni izdelki bodo vedno bolj in bolj prevzemali inteligentne funkcije, ki so jih do sedaj delno prikazovali npr. filmski liki, kot je James Bond. Oblačila bodo združevala funkcije različnih medijev in naprav za širok spekter uporabe. Na področju mikrotehnologije bodo nenehno razvijali čedalje manjše komponente, ki bodo omogočale nevidno vgrajevanje inteligentnih funkcij v klasične izdelke. Ta nova generacija inteligentnih oblačil postavlja številne potrebe po inventivnem razvoju znotraj oblačilne industrije ter zahteve, ki odpirajo nove možnosti razvoja na tem področju.

Iz tega pregleda je jasno videti, da se z izdelovanjem tovrstnih oblačil ne bodo več ukvarjali samo inženirji oblačilne tehnologije, ampak bodo morali pri tem sodelovati strokovnjaki različnih profilov in področij, od tekstilnih inženirjev, inženirjev elektronike, elektrotehnike, strojništva, računalništva in fizike, do strokovnjakov za radiokomunikacije, elektromagnetno sevanje itd.

Z nastankom inteligentnih tekstilij in še posebej z nastankom inteligentnih oblačil, ki bodo lahko samostojno izbirala odločitve na podlagi izmerjenih vrednosti senzorjev, vgrajenih naprav ali podanih človekovih zahtev, nastaja v oblačilni industriji novo dinamično obdobje. Razvoj novega tipa oblačil daje pobudo, da bo zanimanje za tekstilno in oblačilno tehnologijo spet postalo izrazito pozitivno, živahno in polno izzivov.

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APLIKACIJSKI ČLANEK
APPLICATION ARTICLE

TD350 IGBT driver IC including advanced control and protection functions

by Jean-Francois Garnier, Standard Linear Division, STMicroelectronics

Introduction

IGBT devices play a large role in power applications due to their high current/voltage capability and ease of driving. The majority of industrial applications use a 3-phase inverter with 1200V IGBT. Driving these devices in medium or large power applications requires separate, floating high- and low-side drivers with galvanic insulation. Control and protection functions are also required to ensure reliable operation. The device presented hereafter is a new integrated circuit that includes all the functions necessary to directly drive an IGBT in power applications and is especially adapted to 1200V IGBT with current ratings of 25 to 80A in Econopak-like modules.

Device description

The new TD350 IC uses STMicroelectronics' BCD3S process, and fits in a standard SO14 package. The block diagram is shown in Figure 1. The TD350 can be used with either a single positive power supply (VH pin), or a dual positive/negative supply (VH/VL pins). Separated source (OUTH) and sink (OUTL) output pins allow the use of different gate resistors for turn-on and turn-off. The source stage is built with a bipolar npn Darlington, whereas the sink stage uses a MOSFET. Peak output currents are 1.2A sink, 0.75A source minimum over the full temperature range (-20°C to 125°C). The IN input controls the driver outputs and is active low. Both optocoupler or pulse transformer can be used. A special filtering function rejects input signals smaller than 100ns for safe pulse transformer operation. An under-voltage lockout function protects the application in case of invalid supply voltage levels by driving the IGBT gate low when the TD350 supply is lower then the UVLO level (about 10V).

The DESAT and FAULT pins are used for the desaturation protection with adjustable blanking time and fault status signal. The IGBT collector-emitter voltage is monitored, whenever it may exceed 7V, the IGBT gate will be driven low and desaturation information will be feedback to the application controller by the FAULT pin.

In addition to these well-known functions, the TD350 integrates two innovative features that will be described in more detail hereafter:

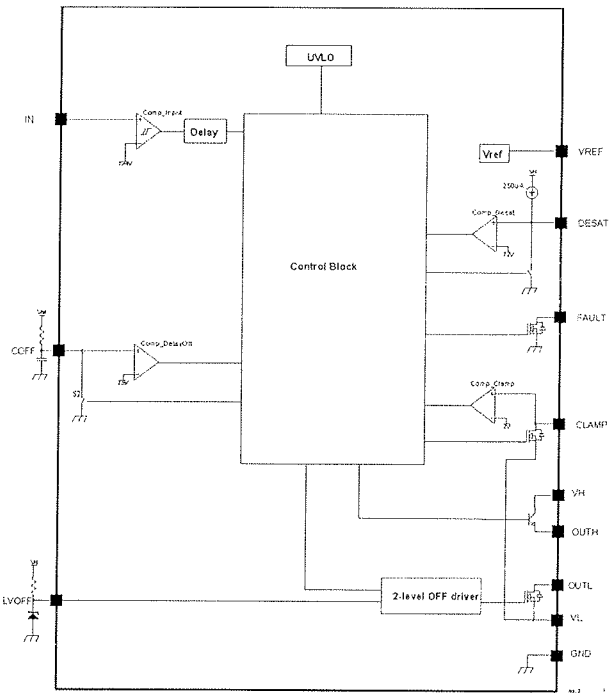


Figure 1: IGBT Driver Block Diagram

- The CLAMP pin is an input/output pin used for the Active Miller clamp function.
- The optional 2-step turn-off function uses the COFF pin connected to an external R/C timing circuit and the LVOFF pin connected to an external reference voltage.

Active Miller clamp function

The Active Miller clamp function is used to reduce the risk of induced turn-on in high dV/dt conditions. Through this function, the TD350 offers an alternative solution to the problem of the Miller current in IGBT switching applications. Instead of driving the IGBT gate to a negative voltage to increase the safety margin, TD350 uses a dedicated CLAMP pin to control the Miller current. When the IGBT is off, a low impedance path is established between IGBT gate and emitter to carry the Miller current, and the voltage spike on the IGBT gate is greatly reduced (see Figure 2).

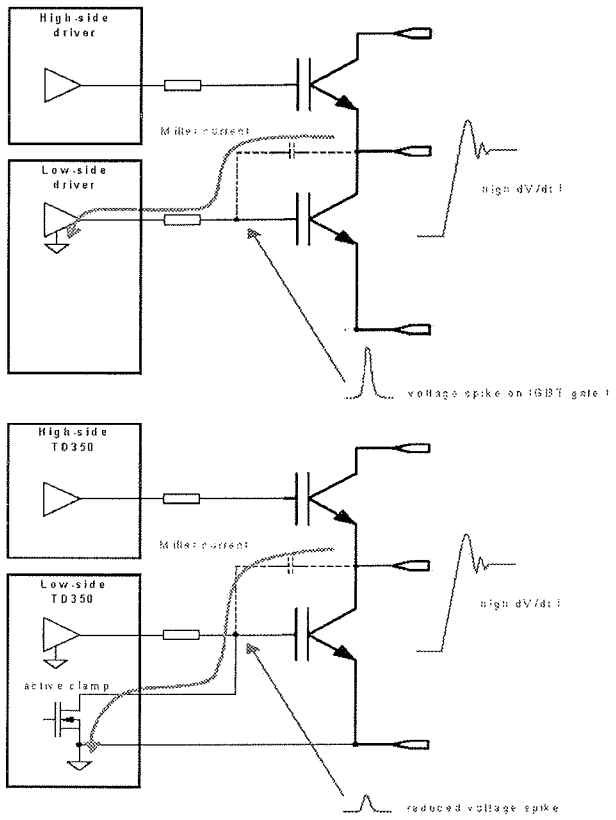


Figure 2: Miller Effect and Active Miller Clamp Principle

The Active Miller Clamp function is implemented using a comparator that monitors the IGBT's actual voltage (see Figure 3). When the gate voltage goes lower than about 2V relative to the GND level, then an internal latch is set and the CLAMP pin is pulled to ground. Even if there occur voltage spikes due to the Miller current, the clamp is not released due to the latched state. The clamp is released only when the output is driven to again to the high level. In this way, the CLAMP function doesn't affect the turn-off characteristic, but only keeps the gate to the low level during all the off time.

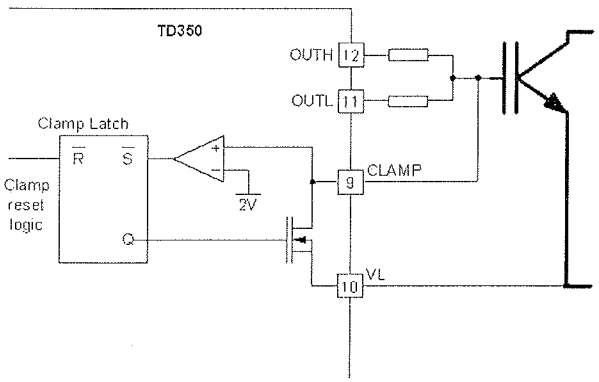
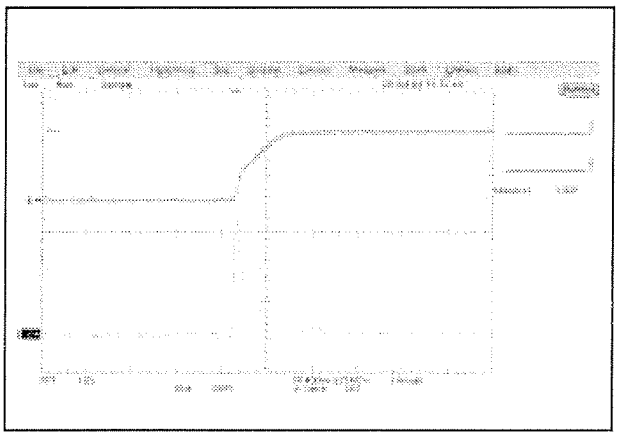


Figure 3: TD350 Active Miller Clamp Function

The clamp switch characteristic is similar to the sink part of the output stage, i.e. 1.2A peak minimum, and a maximum VOL=3V at 0.5A over the full temperature range.

The main benefits of the Active Miller Clamp are: no need to use a negative gate voltage to keep the IGBT in safe off state (allowing bootstrap technique for the high side driver supply), and the possibility to adjust the gate resistor to optimize the turn-off characteristics (commutation losses and EMI behavior) independently of the Miller current issues.

The waveforms shown in Figure 4 show how the Active Miller Clamp results in a consistent reduction of voltage spikes on IGBT gate, both in amplitude and duration. Tests were done on a 1200V, 25A IGBT module with a gate resistor Rg=47Ohms.



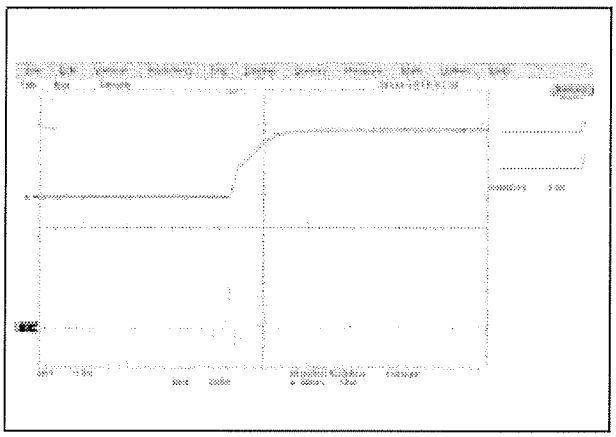


Figure 4: Vce and Vge waveforms without and with Active Miller Clamp function

In large power applications where a negative voltage drive has to be used, the CLAMP pin can be used as a second gate discharge path during the turn-off (see Figure 5). When the gate voltage goes below 2V (i.e. the IGBT is already driven off), the CLAMP pin is activated and the gate is rapidly driven to the negative voltage. Again, the benefit is an improvement in the time taken to drive IGBTs with a large gate capacitance to low level without affecting the IGBT turn-off characteristics.

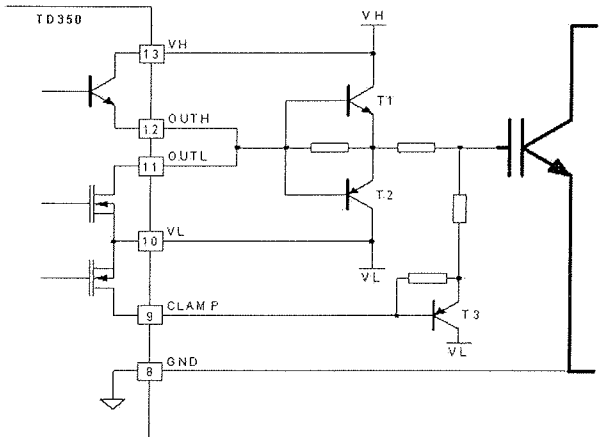


Figure 5: CLAMP used as secondary gate discharge path in large power application

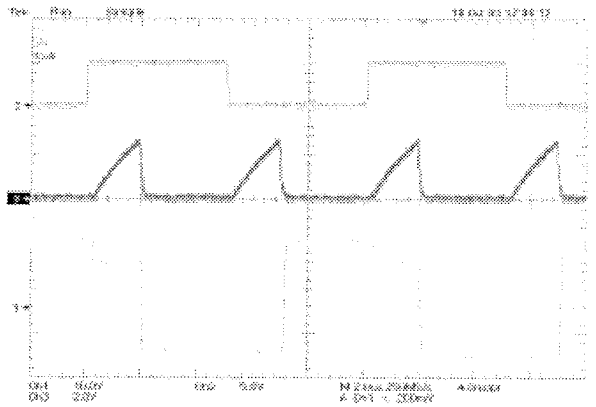


Figure 7: Input signal, COFF timing and output waveform with the 2-level turn-off function (the COFF timing is exaggerated for illustration)

Two-level turn-off function

If there is a short-circuit or overcurrent in the load, a large voltage overshoot can occur across the IGBT at turn-off and can exceed the IGBT breakdown voltage. By reducing the gate voltage for a short time before turn-off, the IGBT current is limited and the potential overvoltage is reduced. This technique is called 2 level turn-off. Both the level and duration of the intermediate off level are adjustable. The level can be easily set by an external Zener diode; its value depends on the IGBT characteristics and is about 11V for a typical IGBT (see Figure 6).

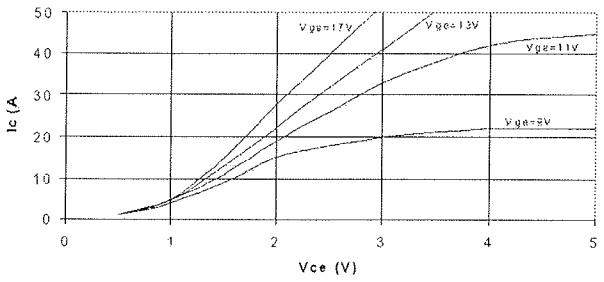


Figure 6: Ic=f(Vce,Vge) curves for a typical 1200V, 25A IGBT module

The duration is set by an external resistor/capacitor in conjunction with the integrated voltage reference for accurate timing, and is in the range of a few microseconds. This 2-level turn-off sequence takes place at each cycle, and has no effect if the current doesn't exceed the normal maximum rated value, but it protects the IGBT in case of overcurrent event (with a slight increase of conduction losses).

To keep the output signal width unchanged relative to the input signal, the turn-on is delayed by the same value as the 2-level turn-off duration (see Figure 7). Using the same timing element guarantees minimum pulse distortion. The turn-on delay also provides a minimum on-time function as input signals smaller than this delay are ignored. Minimum on-time and low pulse width distortion allow safe and easy driving from a microcontroller or DSP system

The two-Level Turn-off function principle is shown in Figure 8. Whilst the device is in 2-level turn-off, the OUTL output is controlled by a comparator between the actual OUTL pin and an external reference voltage. When the voltage on OUTL goes down as a result of the turn-off and reaches the reference threshold, then the OUTL output is disabled and the IGBT gate is not discharged further. After the 2-level turn-off delay, the OUTL output is enabled again to end the turn-off sequence.

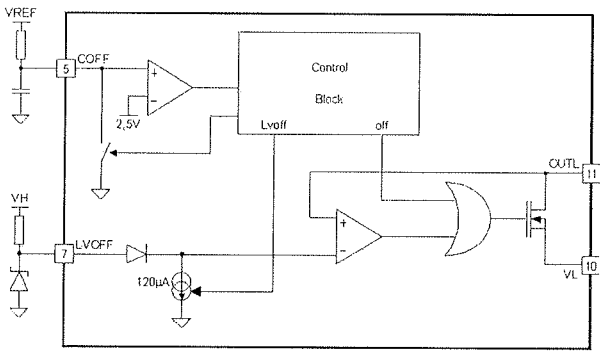


Figure 8: Two-Level Turn-off Function Principle

Tests were done with a standard 1200V 25A IGBT module (Eupec FP25R12KE3) in a simple chopper circuit (see Figure 9) that allows one to adjust the level of the current at turn-off. Waveforms at turn-off are shown in Figure 10 and Figure 11 at the 150A level, which simulates an overcurrent event.

Maximum voltage reached on the IGBT collector and commutation losses are shown in Table 1 for both nominal rated current at 25°C (40A) and overcurrent (150A) conditions. There is no noticeable difference at nominal current, and the overvoltage is greatly reduced in the case of an overcurrent event.

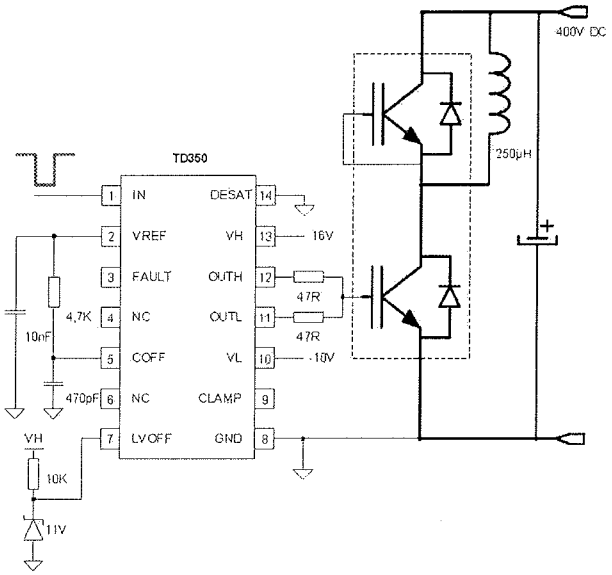


Figure 9: Circuit for 2-level turn-off test

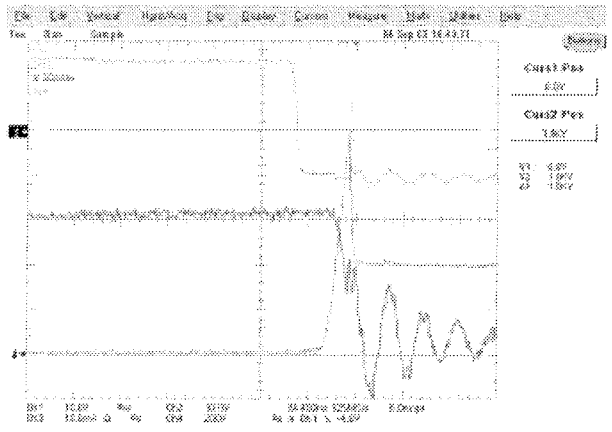


Figure 10: Classical turn-off (VH=16V to VL=-10V): driver output, Vge, Ic and Vce waveforms

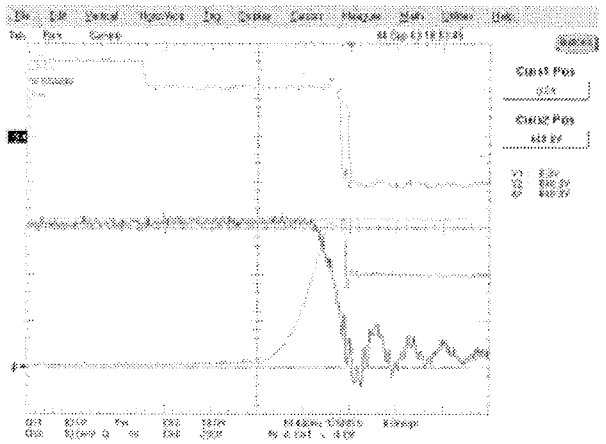


Figure 11: 2-level turn-off (OUT voltage is turned-off from VH=16V to LVOFF=11V during 1.5µs and ultimately OUT is pulled to VL=-10V): driver output, Vge, Ic and Vce waveforms

Table 1: Comparison between classical turn-off and 2-level turn-off

	nominal 400V/40A		overcurrent 400V/150A	
	Eoff (mJ)	Vce max(V)	Eoff (mJ)	Vce max(V)
Classical turn-off	2.5	620	15	1000
2-level turn-off with LVOFF=11V	2.5	620	23	640

Conclusion

The new IGBT driver IC presented here is a versatile device that can be used in a wide range of power applications. The advanced functions (Desaturation protection, Active Miller Clamp, 2-level turn-off) integrated inside the IC allow safe and reliable operation with minimum external circuitry in applications such as motor control and UPS systems.

Predstavitev Iskre Avtoelektrike d.d.
Presentation of Iskra Avtoelektrika d.d.

Iskra Avtoelektrika d.d.

Delniška družba Iskra Avtoelektrika je globalni proizvajalec električne in elektronske opreme za potrebe avtomobilske industrije, elektromotornih pogonov za namene industrije logistične opreme ter komponent in sklopov na osnovi izbranih tehnologij.

Družba je bila ustanovljena leta 1960. Ponaša se z dolgoletno tradicijo. V svoji preteklosti je doživljala hitro rast, velike in stalne spremembe. Oblikovale so jo zahteve stalno spreminjajočega se okolja. Na osnovi proizvodnih začetkov je v svoji zgodovini razvila in danes samostojno obvladuje vse funkcije poslovnih procesov od razvoja do poprodajnih aktivnosti. Prerasla je lokalne okvire delovanja in se vse bolj usmerja v globalne tokove modernega sveta. Tako se danes uvršča med največja slovenska industrijska podjetja in sodi v sam vrh med slovenskimi izvozniki. Danes delniška družba Iskra Avtoelektrika obvladuje proizvodnjo zaganjalnikov, alternatorjev, enosmernih motorjev, elektronike, hladno kovanih delov, sestavnih delov in komponent. Skupina Iskra Avtoelektrika kot celota pa združuje še osem proizvodnih in eno pridruženo proizvodno družbo doma in po svetu in šest trgovskih družb v svetu v okviru lastne distribucijske mreže.

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Pregled diplomskih del, magisterijev in doktoratov v letu 2004
BS, MS and PhD abstracts, year 2004

DIPLOMSKA DELA

Naslov naloge: **Meritve fotoprevodnih tankih plasti organskih kristalov**

Avtor: **Primož Rebernik Ribič**

Mentor: **doc.dr.Gvido Bratina, Politehnika, Nova Gorica**

Univerza v Ljubljani, Fakulteta za matematiko in fiziko

Izmerili smo odvisnost toka fotogeneriranih nosilcev naboja od energije vpadne svetlobe v tankih plasteh organskega polprevodnika *3,4,9,10-perilen-dianhidrid-tetrakarboksilne kisline* (PTCDA) pri različnih vrednostih zunanjega električnega polja. Vakumsko naparjena struktura vzorcev je bila ITO/PTCDA/In na stekleni podlogi. Ugotovili smo, da fotogeneracija naboja poteka preko generacije vzbujenih stanj molekul *(ekscitonov),* ki nato razpadejo na stikih ITO/PTCDA in In/PTCDA oz. v sami organski plasti. Pri disociaciji ekscitonov igra glavno vlogo električno polje na stikih oz. polje v sami organski plasti. Izkaže se, da je električno polje v glavnem prisotno na stikih ITO/PTCDA in In/PTCDA, električno polje v organski plasti pa je majhno.

Naslov naloge: **Karakterizacija polprevodnih lastnosti PTKU keramike**

Avtor: **Matjaž Dežman**

Mentor: **prof.dr.Danilo Suvorov**

Univerza v Ljubljani, Fakulteta za matematiko in fiziko

Cilj pričujoče diplomske naloge je bil dvojni, namreč preveriti lastnosti pulznega merilnika varistorskega efekta na Odseku za raziskave sodobnih materialov K9 Instituta Jožef Stefan in karakterizirati materiale, ki izkazujejo pozitivni temperaturni koeficient upornosti (PTKU). Diploma vsebuje teoretično ozadje vseh pomebnih merjenih mehanizmov kakor tudi opis merilnih sistemov in poteka meritev. Drugi del diplome predstavljajo meritve in rezultati z diskusijo, v dodatku pa podajam navodilo za uporabo pulznega merilnika varistorskega efekta, spisanega na podlagi pridobljenih izkušenj med opravljanjem meritev z njim.

Naslov naloge: **Meritev temperaturne odvisnosti električne prevodnosti svežnjev nanožičk $Mo_6S_3I_6$**

Avtor: **Boštjan Berčič**

Mentor: **prof.dr.Dragan Mihailovič**

Univerza v Ljubljani, Fakulteta za matematiko in fiziko

V svoji diplomski nalogi bom opisal meritev temperaturne odvisnosti električne prevodnosti svežnjev nanožičk $Mo_6S_3I_6$. Stik z drobnimi svežnji smo dosegli z izdelavo majhnih kontaktov, ki smo jih izdelali z elektronsko nanolitografijo. Najprej bomo spoznali osnovne principe in težave izdelave drobnih vezij z elektronsko nanolitografijo, nato pa si bomo podrobneje ogledali še pripravo vzorca in potek same meritve.

V drugem delu si bomo ogledali teoretične napovedi, ki izhajajo iz teorije elektronov v neurejenem mediju in njihovo ujemanje z izmerjenimi podatki. Iz meritev smo ocenili nekatere osnovne parametre, ki pogojujejo temperaturno odvisnost električne prevodnosti (preskakovalna razdalja, stopnja lokalizacije).

MAGISTRSKA DELA

Naslov naloge: **Pregled delovanja Bluetooth tehnologije ter kvalifikacijskega in tipskega postopka odobritve naprav**

Avtor: **Janez Dejak**

Mentor: **prof.dr.Sašo Tomažič**

Univerza v Ljubljani, Fakulteta za elektrotehniko

V magistrskem delu so predstavljene splošne karakteristike tehnologije Bluetooth ter osnovno delovanje fizičnega, podatkovnega ter mrežnega sloja. Prek osnovnega komunikacijskega modela je podana komunikacija med napravama, ki je podrobno podana s specifikacijskimi dokumenti Bluetooth. Specifikacijski dokumenti se delijo na: sekcijo jedrnih specifikacij in sekcijo profilov. V okviru jedrnih specifikacij delo opisuje delovanje oddaje in sprejema radijskega vmesnika, topologijo malega in sestavljenega omrežja, delovanje sinhronih in asinhronih povezav, format paketa in naslavljanje naprav, tipe paketov in njihove oblike, mehanizme popravljanja napak, frekvenčno in časovno sinhronizacijo vodilnih in podrejenih naprav, izbiro skakalnih zaporedij, prehode krmilnika povezav iz stanja pripravljenosti v stanje povezave ter zagotavljanje varnosti. Delovanje Bluetooth profilov pa je v delu obravnavano samo z uporabniškega vidika, saj je osnovni namen poglavja predstaviti

tehnologijo v obsegu, ki zagotavlja podlago za razumevanje kvalifikacijskega in tipskega postopka odobritve Bluetooth naprav.

V nadaljevanju delo obravnava Bluetooth kvalifikacijski postopek, ki je obvezen za vsako napravo, ki se želi tržiti pod blagovno znamko Bluetooth. Osnovni namen kvalifikacijskega postopka je zaščita blagovne znamke in zagotovitev pravilnega vzajemnega delovanja različnih Bluetooth naprav različnih proizvajalcev. V okviru kvalifikacijskega postopka so podane vloge posameznih organov, vloga Posebne interesne skupine in članstva v skupini. Podrobneje je obravnavano kvalifikacijsko preskušanje v neodvisnem laboratoriju, priprava preskusnih specifikacij, preskusne dokumentacije ter tehnične mape skladnosti. Ta način ocenjevanja skladnosti naprav s specifikacijami Bluetooth se je izkazal za učinkovitega, saj omogoča popolno vzajemno delovanje različnih Bluetooth naprav različnih proizvajalcev tudi na nivoju aplikacije.

V zadnjem delu je obravnavana tipska odobritev Bluetooth naprav, ki jo je treba izvesti pred postavitvijo naprave na trg. Tipska odobritev naprave pomeni ocenjevanje skladnosti naprave z nacionalno zakonodajo države, v kateri se bo naprava tržila in/ali uporabljala. Magistrsko delo se tukaj omejuje na tipsko odobritev proizvoda na prostoru Evropske unije oziroma Evropskega gospodarskega prostora. Delo v tem poglavju opisuje splošno evropsko ter slovensko zakonodajo na področju odobritve proizvodov, novi pristop ocenjevanja skladnosti, ki ga uvajajo evropske direktive, uporabo modulov globalnega pristopa, vlogo bistvenih zahtev, pomen izbire harmoniziranih ali neharmoniziranih preskusnih standardov, znak skladnosti CE in ostale dodatne znake, ki jih vpeljujejo direktive novega pristopa, izjavo o skladnosti ter odgovornosti za hibni proizvod. Na koncu je opisana slovenska oziroma evropska zakonodaja na področju tipske odobritve Bluetooth naprav. Predstavljena je *Direktiva* 1999/5/EC *za radijsko in telekomunikacijsko terminalsko opremo* oziroma slovenski *Pravilnik o radijski in telekomunikacijski terminalska opremi,* ki je relevanten za ocenjevanje skladnosti Bluetooth naprav. Opisani so vsi štirje možni načini ocenjevanja skladnosti radijske in telekomunikacijske terminalske opreme, ki jih zakonodaja predvideva, ter podrobneje načini ocenjevanja skladnosti Bluetooth naprav.

Naslov naloge: **Razvoj plinskega odvodnika za uporabo v nizkonapetostnih elektroenergetskih omrežjih**

Avtor: **Aleš Štagoj**

Mentor: **doc.dr.Grega Bizjak**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Ljudje smo danes življenjsko odvisni od električne energije ter od različnih naprav in strojev, ki jih le-ta poganja. Zahteve po neprekinjeni dobavi električne energije so vse večje in s tem tudi zahteve po preprečevanju neželenih pojavov v električnem omrežju. Eden takih pojavov so tudi različne prenapetosti, ki nastajajo v prvi vrsti zaradi posrednih ali neposrednih atmosferskih razelektritev, pa tudi zaradi stikalnih manevrov. Prenapetosti v omrežju praktično ne moremo preprečiti, lahko pa s pomočjo prenapetostnih odvodnikov precej zmanjšamo njihov vpliv na delovanje naprav, ki so priključene na omrežje.

V tem magistrskem delu je predstavljeno, kako pride do elektromagnetnih motenj, ki so vzrok udara strele. Kakšne so njene posledice za nizkonapetostna omrežja in kako se spoprijeti z njenimi vplivi. Predstavljene so osnovne smernice sistema zaščit po priporočenih ali obveznih dokumentih in pravilnikih (standardih). Predstavljenih je nekaj osnovnih gradnikov kompleksne zaščite električnih naprav pred nevarnimi prenapetostmi zaradi atmosferskih razelektritev. Prehode med različno definiranimi zaščitnimi conami pa povezujejo zaščitni elementi; najpogosteje so to iskrišča, plinski in varistorski odvodniki.

V nadaljevanju je poudarek na plinskem odvodniku *(Gas Discharge Tube* - GDT), kot zaščitnem elementu *(Surge Protection Device* - SPD). Prikazane so lastnosti in zahteve plinskih odvodnikov za uporabo v nizkonapetostnih elektroenergetskih omrežjih. Opisan je ustrezen prototip plinskega odvodnika skupaj z osvojeno tehnologijo izdelave. Prikazani so rezultati opravljenih električnih preizkusov po ustreznem standardu. Izpostavljena je problematika gašenja pričakovanih omrežnih, sledilnih tokov v odvodniku, možne rešitve in smernice za izdelavo samougasnega plinskega odvodnika. In nenazadnje so prikazani se statistični podatki razvojnih električnih meritev pomembnih parametrov plinskega odvodnika z zunanjim premerom 14 *mm.*

Naslov naloge: **Etalon za gostoto magnetnega pretoka s permanentnim magnetom**

Avtor: **Samo Beguš**

Mentor: **prof.dr.Dušan Fefer**

Univerza v Ljubljani, Fakulteta za elektrotehniko

V magistrski nalogi je v uvodnem poglavju predstavljena merilna sledljivost, ter definicija primarnega etalona. Predstavljen je Laboratorij za magnetna merjenja in njegovo trenutno akreditirano območje za gostoto magnetnega pretoka. Za merjenje gostote magnetnega pretoka od nekaj mT do nekaj sto mT predstavlja primarni etalon protonski magnetometer, ki deluje *na* principu merjenja absorpcije energije. Delovanje protonskega magnetometra temelji na jedrski magnetni resonanci.

Drugo poglavje podaja kratek zgodovinski pregled poskusov ter teoretično ozadje jedrske magnetne resonance.

Če se električno nabit delec giblje, povzroči nastanek magnetnega polja. Delec se lahko premo giblje ali rotira.

Takšen električno nabit delec je lahko tudi atomsko jedro. Atomsko jedro ima maso, magnetni moment in spin ali kotni moment. Atomsko jedro se obnaša kot majhen magnetni dipol. V prisotnosti magnetnega polja lahko zavzame delec dve energijski stanji. Z absorpcijo fotona lahko delec preskoči na drug energijski nivo, če je energija fotona enaka razliki energij nivojev.

Magnetizacija vzorca v magnetnem polju v smeri polja *Mz* je vsota prispevkov vseh mikroskopskih spinov. Opazovanje magnetizacije je možno z resonančnim eksperimentom. Za eksperiment mora biti magnetno polje *Bo,* v katerem se nahaja vzorec s protonskimi spini, dovolj homogeno in stabilno. Če vzorec izpostavimo motnji - visokofrekvenčnemu (VF) pulzu, spini absorbirajo energijo in preskočijo na višji energijski nivo. Največja stopnja absorpcije je, ko je VF pulza enaka Larmorjevi frekvenci. Poznana sta dva osnovna principa merjenja gostote magnetnega pretoka s pomočjo jedrske magnetne resonance: Blochova metoda in Purcellova metoda. Pri Blochovi metodi, to je merjenju s principom proste precesije, se vzorec (večkrat destilirana voda) nahaja v konstantnem homogenem magnetnem polju *Bo.* Vzbudimo ga z elektromagnetno motnjo, z VF pulzom. Po prenehanju VF pulza protoni v vodi prosto zanihajo z resonančno frekvenco. Nihanje lahko opazujemo in določimo resonančno frekvenco. Voda v vzorcu mora biti zelo čista, iskanje resonančne frekvence je dolgotrajno. Potrebno je zelo homogeno magnetno polje zato se merjenja lahko izvajajo le v popolnoma neferomagnetni okolici.

Purcellova metoda temelji na principu merjenja absorbirane energije. Vzorcu (vodi) se doda proste protone. S tern se razširi resonančna krivulja: lažje je najti resonance, težje pa je določiti resonančni vrh. Meritve so relativno hitre. Homogenost polja je lahko manjša kot pri merjenju s prosto precesijo. Zaradi dodajanja prostih protonov se spremeni tudi vrednost giromagnetnega razmerja ψ_p.

V tretjem poglavju je na kratko opisan permanentni magnet, ki ima v zračni rezi gostoto magnetnega pretoka 0.31 T. Homogenost magnetnega polja v zračni reži omogoča merjenje gostote magnetnega pretoka z jedrsko magnetno resonanco na principu merjenja absorpcije energije.

Četrto poglavje opisuje protonski magnetometer za merjenje gostote magnetnega pretoka v zračni reži permanentnega magneta. Protonski magnetometer ne uporablja mejnega oscilatorja, temveč generira VF signal z direktnim digitalnim sintetizatorjem (DDS). Prednost DDS generatorja je predvsem v tem, da omogoča nastavljanje frekvence z visoko razločljivostjo. Ker se frekvenca nastavlja digitalno, z mikrokontrolerjem, tudi ni potrebno merjenje frekvence tako kot pri mejnem oscilatorju. Sonda za merjenje je vodna raztopina bakrovega sulfata in se nahaja v tuljavi nihajnega kroga. DDS generator je priključen na nihajni krog preko upora. Za zaznavanje sprememb napetosti na nihajnem krogu je uporabljen občutljiv amplitudni demodulator - vzorčevalni detektor. Uporabljen je tudi v vezju fazno občutljivega detektorja (Phase Sensitive Detector - PSD), ker ima tudi pasovno prepustno karakteristiko. Krmiljenje DDS generatorja, LCD prikazovalnika in preračunavanje resonančne frekvence v gostoto magnetnega pretoka opravlja mikrokrmilnik. Protonski magnetometer lahko meri temperaturo z dvema senzorjema, tako da je možno meriti temperature stalnega magneta in okolice.

Programska oprema mikrokrmilnika je predstavljena v petem poglavju. Program je sestavljen iz glavne neskončne zanke, ki pregleduje tipke, ustrezno reagira, če je katera tipka (ali več) pritisnjena in piše na prikazovalnik. Drugi del programa, generiranje sinusnega modulacijskega signala ali signala za frekvenčno modulacijo VF signala, pa prožijo prekinitve v določenih časovnih intervalih.

Protonski magnetometer omogoča ročno iskanje resonance, avtomatsko sledenje resonančni frekvenci, avtomatsko iskanje resonančne frekvence in shranjevanje rezultatov v pomnilnik mikrokrmilnika. Shranjene rezultate je možno shraniti v datoteko na osebnem računalniku in grafično prikazati.

V šestem poglavju je opisana čelna plošča in priključki protonskega magnetometra. V tabelah so zbrane funkcije tipk in funkcije tipk ob vklopu ali resetu mikrokrmilnika.

V sedmem poglavju so podani prispevki k merilni negotovosti protonskega magnetometra in prispevki k skupni merilni negotovosti kalibracije.

Rezultati meritev so prikazani v osmem poglavju. Gostota magnetnega pretoka v reži permanentnega magneta je bila izmerjena v 63 točkah, v obliki matrike z 9 x 7 elementi, kjer je bila homogenost magnetnega polja primerna za merjenje z jedrsko magnetno resonance. Ker se gostota magnetnega pretoka spreminja s temperaturo, je vsaka meritev sestavljena iz dveh: iz meritve v referenčni točki (x = 0 cm, y = +1.5 cm) in meritve v eni izmed 63 točk. Ti dve meritvi sta izvedeni v čim krajšem časovnem obdobju, običajno manj kot minuti, tako da je spreminjanje gostote magnetnega pretoka zaradi temperature zanemarljivo. Hkrati z gostoto magnetnega pretoka je bilo izmerjeno tudi razmerje signal/šum v merjenih točkah. Območje, kjer je razmerje signal/šum najboljše, je bilo kasneje izmerjeno z gostejšo mrežo merilnih točk (raster 2.5 mm).

Prikazani so tudi rezultati avtomatskih meritev v daljšem časovnem obdobju. Spreminjanje gostote magnetnega pretoka preko dneva, ko ni dodatnega segrevanja zaradi sonca, je manjše od 200 (μT. Koeficient temperaturne odvisnosti gostote magnetnega pretoka v reži je $k_t = - 0.00041\ K^{-1}$).

V devetem poglavju je opisan osnutek delovnih navodil za kalibracijo magnetometrov z etalonskim sistemom. Podani so tudi rezultati testne kalibracije magnetometra BELL 9953 s 3D sondo.

Razširjena merilna negotovost etalonskega sistema je 0.003 mT, pri gostoti magnetnega pretoka v zračni reži

307.053 mT, oziroma v relativni obliki 9.10^{-7}. Razmerje signal/šum signala faznega detektorja pa je 24 dB.

V zaključku so na kratko podani doseženi rezultati ter načrti in predlogi za izboljšavo, oziroma nadgradnjo etalonskega sistema. *Izkazalo* se je, da je zelo pomembno pravilno pozicioniranje sonde v reži magneta. Za doseganje boljših rezultatov bo potrebno izdelati posebne vmesnike za sonde, saj bi se s tem izboljšala ponovljivost meritev in tudi same kalibracije.

DOKTORSKE DISERTACIJE

Naslov naloge: **Vpliv anizotropnih in električnih lastnosti membrane na stabilnost membranskih mikro in nano struktur**

Avtor: **Miha Fošnarič**

Mentor: **prof.dr.Aleš Iglič**

Somentorica: **prof.dr.Veronika Kralj-Iglič**

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V doktorskem delu predstavimo teoretični model membrane, ki jo sestavljajo v splošnem anizotropni gradniki. Kot membranski *gradnik* obravnavamo molekulo ali pa skupek molekul v membrani, ki ga v izbranem teoretičnem modelu popišemo kot celoto. Za *anizotropen* gradnik je značilno, da njegova rotacijska stanja okoli normale na površino membrane v splošnem niso energijsko enakovredna.

V predstavljenem delu poskušamo z anizotropnimi lastnostmi membranskih gradnikov pojasniti nekatere pojave v organskih in anorganskih mikro in nano strukturah, kot so stabilnost por v membranski dvojni plasti, stabilnost torocitnih oblik membranskih mehurčkov ter sesedanje anorganskih mikro in nano cevk.

Vpeljemo teoretični model, ki pojasni povečano stabilnost por v lipidni dvojni plasti membrane kot posledico lateralne preporazdelitve anizotropnih membranskih gradnikov. Prosto energijo membrane obravnavamo kot vsoto energije roba pore, proste energije anizotropnih membranskih gradnikov in elektrostatske proste energije naelektrene membrane. Pri slednji upoštevamo, da membrano obdaja elektrolitska raztopina. Zaradi povečane energije roba je energijsko neugodno, da membrana tvori poro. Po drugi strani pa nastanek por v membrani zmanjšuje elektrostatsko prosto energijo membrane. Zaradi nastanka pore so namreč nekateri enako naelektreni gradniki membrane med seboj oddaljeni bolj kot v nepretrgani membrani. Zato elektrostatski prispevek k prosti energiji membrane favorizira čim večjo poro. Od naelektrenosti membrane in od ionske jakosti okolne raztopine je odvisno, ali bo prevladal pozitivni prispevek energije roba ali pa negativni prispevek elektrostatske proste energije. V prvem primeru se nastala pora zapre, v drugem primeru pa radij pore zelo naraste in s tem uniči membrano, Stabilne pore tako ne moremo razložiti z minimizacijo vsote energije roba in elektrostatske proste energije membrane. S predstavljenim modelom pokažemo, da se lahko primerno izbrani anizotropni gradniki naberejo na robu pore in z njega izrinejo izotropne lipidne molekule. Na ta način zmanjšajo energijo roba pore in elektrostatska energija lahko močno zniža prosto energijo membrane. Leta ima tako globok minimum pri končnem radiju pore, ki predstavlja stabilno ravnovesno stanje sistema.

V nadaljevanju pokažemo, da lahko anizotropija membranskih gradnikov pojasni tudi stabilnost opaženih torocitnih oblik membranskih struktur. Torocit je mehurček, ki ima ploščat, tanek osrednji del ter odebeljen, toroiden zunanji del. V osrednjem delu mehurčka sosednji membrani nista v stiku. Stabilnosti opisanih mehurčkov ni mogoče razložiti z doslej znanimi izotropnimi modeli membrane. V doktorskem delu pokažemo, da se anizotropni membranski gradniki naberejo na odebeljenih robovih torocitnega mehurčka in tako stabilizirajo značilno torocitno obliko.

Na koncu predstavljeni koncept anizotropije tankih struktur uporabimo pri teoretični razlagi sesedanja anorganskih mikro in nano cevk. Predstavimo preprost model, ki vsebuje anizotropijo večplastne stene cevke. Pokažemo, da je lahko cevka pri majhnih debelinah stene cevke stabilna, pri večjih debelinah stene pa se sesede in splošči v trak.

V doktorskem delu torej pokažemo, da imajo lahko anizotropne lastnosti tankih membranskih struktur pomemben vpliv na obliko membrane. Anizotropne lastnosti pridejo se posebej do izraza v primerih, kjer ima del membrane močno anizotropno geometrijo in velike ukrivljenosti.

Naslov naloge: **Analiza temperaturnih razmer pri kalibraciji standardnih platinastih uporovnih termometrov v fiksnih celicah**

Avtor: **Valentin Batagelj**

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Kalibracija standardnih uporovnih termometrov (SPRT-jev) v fiksnih točkah predstavlja enega od osnovnih gradnikov mednarodne temperaturne lestvice ITS-90, ki je temelj za praktična merjenja temperature v znanosti, industriji in vsakdanjem življenju. Obvladovanje merilnih postopkov pri kalibraciji in objektivna ocena z njimi povezanih merilnih negotovosti je brez dvoma tisti cilj, ki zagotavlja, da bodo rezultati meritev temperature konsistentni, tako pri rutinskih merjenjih, kot tudi merjenjih na najvišjem metrološkem nivoju.

Doktorska disertacija na poglobljen način obravnava analizo temperaturnih razmer, ki jih srečamo pri kalibraciji SPRT-jev v fiksnih celicah. V ta namen je bil izdelan numerični model temperaturnih potekov, ki predstavlja učinkovito orodje za objektiven vpogled v kompleksne fizikalne po-

jave, katerih ozadje lahko sicer na podlagi meritev le slutimo. V okviru disertacije je bil numerični model uporabljen predvsem pri analizi prispevka negotovosti zaradi izgubnih toplotnih tokov, vendar pa njegova uporabnost vsekakor presega ta okvir. V disertaciji so bile tako nakazane tudi druge možnosti uporabe, pri čemer velja posebej izpostaviti možnost uporabe numeričnega modeliranja pri načrtovanju novih fiksnih celic in termometrov, ter možnosti optimizacije merilnih postopkov pri uporabi obstoječe merilne opreme. Z numeričnim modelom lahko analiziramo tudi pojav lastnega segrevanja uporovnih termometrov, ki je bil v okviru disertacije podrobneje obdelan, pri čemer je bil poudarek predvsem na objektivni določitvi merilne negotovosti in na možnostih izboljšave merilnih postopkov z uporabo različnih kombinacij merilnih tokov.

Naslov naloge: **Direktni AC/DC pretvornik s korekcijo faktorja moči z modulacijskim algoritmom**

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Z uporabo vezij in modulacijskih strategij za korekcijo faktorja moči lahko v enofaznih in trifaznih sistemih dosežemo faktor moči blizu vrednosti 1. V disertaciji je predstavljena izdelava trifaznega stikalne ga usmernika od matematičnega modela, izračuna modulacijske strategije, simulacije do končne izdelave prototipa. S pomočjo stikalno matričnega pristopa je bil izveden modulacijski algoritem, ki je zagotovil sinusne oblike vhodnih tokov pri sinusnih vhodnih napajalnih napetostih. Pri tem se je iz matematične analize procesa pokazalo, da za korekcijo faktorja moči tokovni senzorji niso potrebni. Izdelana je bila sinteza usmernika po W oodovi metodi. Za potrebe regulacije je bil izračunan dinamični model vezja.

Matematično izpeljano strukturo vezja in izračunani modulacijski algoritem je bil najprej preskušen s simulacijo. Uporabljen je bil simulator Spice.

Rezultati simulacije so potrdili teoretično napovedano delovanje usmernika brez tokovnih senzorjev s faktorjem moči blizu 1. Na osnovi matematične izpeljave strukture vezja in modulacijskega algoritma je bil izdelan prototip usmernika, na katerem so bile potrjene teoretične predpostavke, ki izhajajo iz matematične analize matrično organiziranega usmernika.

Modulacijski algoritem je bil implementiran s pomočjo mikrokrmilnika.

Izhodna enosmerna napetost je bila nastavljiva in regulirana z digitalnim regulatorjem, implementiranim v mikrokrmilnik.

NOVICE NEWS

ASML/Applied team up on 65nm technology

DUTCH lithography company ASML and US semiconductor equipment behemoth Applied Materials have joined forces to speed up the development of 65nm and below process equipment technology.

Under the deal, ASML will deliver an immersion lithography system to Applied Materials' Maydan Technology Centre in early-2005.

The scanner will be used by Applied and its customers to develop and test processes for production chip manufacturing. "Matching advanced lithography with process system development is becoming critical to achieving the dimensional control and rapid yield ramps required by chipmakers for manufacturing sub-90nm designs," said Mark Pinto, senior vice president of Applied Materials.

"Having ASML's most advanced system in our development facility provides us with the unique capability to merge the requirements of lithography with a host of other process equipment challenges facing the industry, with the goal of offering timely, reliable, production-ready solutions."

ASML is also working with Belgium research centre IMEC on developing a sub-45nm research platform based on advanced lithography. The IMEC research will investigate process and resist related issues with the goal of preparing immersion lithography for production use by 2007.

Soitec joins ATDF's 45nm research project

FRENCH company Soitec has announced that it will supply silicon-on-chip (SOI) substrates for a major initiative aimed at developing multi-gate field effect transistor (MuGFET) technology for the 45nm node and below.

The research project is being spearheaded by Texas based research body Advanced Technology Development Facility (ATDF) -a subsidiary of trade consortium Sematech - and involves chip makers, equipment suppliers and universities.

MuGFET is a generic term used to describe a variety of new, multiple-gate field effect transistors, including CMOS FinFETs (FETs with "fin-shaped" transistors) and triple-gate devices. These transistors are increasingly being seen as an alternative to simple scaling down in the race to keep up with Moore's Law.

Important milestone for thin-film crystalline silicon solar cells

IMEC achieved an efficiency of 5% for thin-film crystalline silicon solar cells by applying aluminum-induced crystallization (AIC) in combination with high-temperature epitaxial deposition on ceramic substrates.

Thin-film crystalline silicon solar cells on cheap substrates are a promising alternative to traditional bulk crystalline silicon solar cells because of their higher potential for cost reduction. However, these cells have up to now a limited efficiency due to the lower crystallographic quality of the layers obtained by deposition and/or crystallization. An appealing solution is AIC followed by epitaxial deposition to create the active layer.

AIC is typically used on glass substrates, which usually have a very flat surface (roughness below 10nm) but cannot withstand the high temperatures needed for good epitaxy. Ceramic substrates however show a large roughness, ranging from 50nm up to several microns. If no particular measure is taken, the grain size in the AIC layer is small (1 μm) and a large number of islands are formed on the surface of the AIC layer. The presence of these islands is very detrimental for epitaxy.

To suppress excessive nucleation and to reach a large grain size and a low island density, IMEC used an intermediate spin-on oxide between the ceramic substrate and the AIC layer. Epitaxial deposition on these improved seed layers yielded in thin active layers with good crys-tallographic quality and with a grain size larger than 5nm. By applying hydrogen passivation a substantial improvement of the electronic quality of the layers has been obtained. Solar cells with efficiencies up to 5.0% (area km^2, thickness 4um) and Voc values approaching 460mV have been realized with this technique. While these values have to be increased substantially to become competitive with bulk silicon solar cells, these results are an important milestone for thin-film silicon solar cells on cheap substrates and indicate that AIC combined with high-temperature epitaxy is a promising technique for the next solar cell generation.