TRIPLE DIFFUSED BiCMOS TECHNOLOGY FOR ANALOG - DIGITAL ASICS

I. Šorli, T. Athanas*, I. Nedev**, W. Kausel*, Z. Bele, R. Ročak
MIKROIKS d.o.o., Ljubljana, Slovenia
*SEMCOTEC, Vienna, Austria
**IME, Sofia, Bulgaria

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Abstract: Synergy of CMOS and bipolar performances has been for a long time a designer's dream. BiCMOS, a technology which enables making CMOS, bipolar and other passive devices on the same chip allows realisation of this dream. In particular, we have developed so called triple diffused BiCMOS technology suitable for analog-digital design of ASICs for medium power supply voltages of up to 15 V. Besides added flexibility, good price - performance ratio, this technology also allows a new qualitative step ahead with almost zero investment into new process equipment and clean room construction.

Trojnodifundirana BiCMOS tehnologija za izdelavo analogno-digitalnih integriranih vezij po naročilu

Ključne besede: mikroelektronika, IC vezja integrirana, vezja analogno digitalna, CMOS naprave, naprave bipolarne, transistorji bipolarni, snovanje vezij, izdelava naprav, lastnosti komplementarne, NPN transistorji bipolarni vertikalni, PNP transistorji bipolarni vertikalni, PNP transistorji bipolarni lateralni, BiCMOS vezja, BiCMOS tehnologija trojno difundirana, MOS kondenzatorji, naprave aktivne, naprave pasivne

Povzetek: Sinergija lastnosti, ki jih ponujata CMOS in bipolarna tehnologija je sen vsakega načrtovalca integriranih vezij. BiCMOS tehnologija, ki omogoča izdelavo CMOS, bipolarnih in drugih pasivnih elementov na enem čipu, pa je tista, ki lahko ta sen tudi uresniči. V prispevku opisujemo posebno, tki. trojno difundirano BiCMOS tehnologijo, ki smo jo razvili za potrebe načrtovanja analogno - digitalnih naročniških integriranih vezij z napajalno napetostjo do 15 V. Poleg dodane fleksibilnosti in zadovoljive cene na enoto funkcije, pa nam ta tehnologija omogoča kvalitativen korak naprej, skoraj brez investicije v novo procesno opremo in čiste prostore.

1. INTRODUCTION

Bipolar technology has been for long time the working horse of early days microelectronics. Being typical "analog" technology at the beginning, it has forced designers to thoroughly characterise and optimise many analog subcircuits. The emergence of MOS technology in early seventies and especially the invention of CMOS has revolutionarized microelectronics a great deal. After all bugs were taken care of, CMOS was easier to integrate, less complicated, cheaper per silicon area and had less power consumption. It was ideal for integration of digital functions which was later proved by many successful designs.

Depending on which design group somebody belonged to from the beginning, designers have actually through time divided themselves into fans of either "digital -MOS" or "analog - Bipolar" design approach. Late eighties have brought certain new waves of thinking among them. Having realised that modern telecommunication, automotive and industrial electronics started needing ASICs capable of integrating analog and digital functions, they have also started thinking how to realise all these functions on the same chip, or at least in the same electronics system.

To start with, at that time CMOS has already been a mature, low cost high yielding digital technology. However, some innovative design approaches like the discovery of SC (Switch-Capacitor) circuits, successful realisation of operational amplifiers in CMOS and some others have proved that CMOS can be also turned into attractive process to make analog-digital ASICs. As well, built in the CMOS technology is the possibility to make lateral and low performance vertical NPN or PNP bipolar transistors with no extra process steps or cost. This capability has been for long time used by designers if they really needed bipolar transistors besides MOS ones, /1/, /2/. So basically, CMOS already is a certain kind of "BiCMOS", a mixed Bipolar&CMOS technology which allows realisation of MOS and bipolar transistors on the same chip.
And here is where the whole story begins.

2. DO WE REALLY NEED BiCMOS ?

Since most of the analog-digital functions can be realised with CMOS, do we really need special BiCMOS technology?

Our answer is yes, since CMOS is after all limited to certain extent in making the best performance analog-

digital functions. We believe that only synergy of MOS and bipolar transistors within certain subcircuits where advantageous behaviour of each component is utilised can bring to the optimum price - performance ratio.

This has already been proven by others, /3/, and by our own design experience, /4/. We will better understand this if we take into consideration basic differences between MOS and bipolar transistor. These differences are briefly explained in this section, but the reader can find more information on this subject in references /3/, /5/ and /9/.

2.1 Comparison of MOS and Bipolar Transistors

2.1.1 Transconductance

Transconductance of a bipolar transistor is given by:

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{U_T} = \frac{qI_C}{kT} \qquad (1)$$

g_m : transconductance

I_C : collector current

V_{BE} : base to emitter voltage

U_T : thermal voltage given by $U_T = kT/q$

while transconductance of an MOS transistor in saturation is given by equation:

$$g_m = \sqrt{2k\frac{W}{L}I_{DS}} \qquad (2)$$

k : transconductance parameter

W, L : width and length of the transistor

I_{DS} : drain current

Comparing both equations we can quickly see that bipolar transistor outperforms MOS. Not only that the absolute value of the transconductance is much higher, see figure 1, but its value depends linearly on current, inversely on temperature and is geometry independent. In other words, minimal geometry bipolar transistor has same transconductance as large one at the same current level. To obtain same value of transconductance with MOS transistor it must be 50 to 700 times larger than its bipolar counterpart.

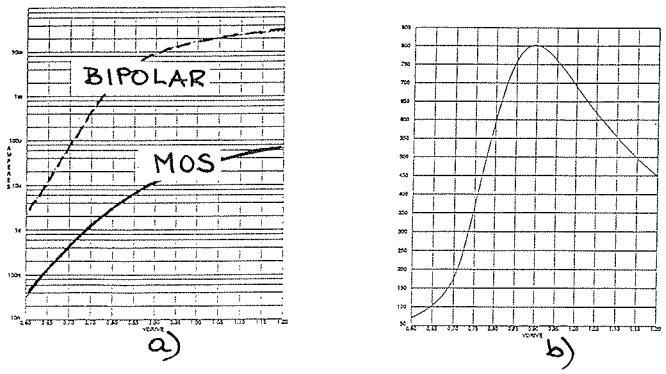

Fig. 1: Transconductance comparison between equal sized MOS and bipolar transistors at different current levels, a) transistor current as a function of V_{BE} (V_{GS}), b) BIP/MOS g_m ratio as a function of V_{BE} (V_{GS})

2.1.2 Open circuit voltage gain

Open circuit voltage gain of a bipolar transistor in common emitter configuration is given by:

$$a_0 = \frac{\partial V_{CE}}{\partial V_{BE}} = g_m r_0 = \frac{V_A}{U_T} \qquad (3)$$

V_{CE} :collector to emitter voltage

r_0 : output impedance

V_A : Early voltage

while open circuit voltage gain for an MOS transistor in saturation is given by:

$$a_0 = g_m r_0 = \frac{1}{\lambda I_{DS}}\sqrt{2k\frac{W}{L}I_{DS}} \qquad (4)$$

λ : channel length modulation parameter

Analog design requires high open circuit voltage gain values. We again see that bipolar transistor is not only better than MOS but its gain is again geometry independent. We can easily make bipolars with V_A above 50 V which gives us a_0 around 2000 while for MOS transistor to achieve this value at 1 mA current level, we must make W/L ratio around 10^5 !!

2.1.3 Temperature Effects

We can show that for two bipolar transistors with emitter area ratio N, their base to emitter voltage difference varies according to the equation :

$$\Delta V_{BE}(T) = \frac{kT}{q}\ln N \qquad (5)$$

N : emitter area ratio of two bipolar transistors

This equation predicts simple relationship among base - emitter voltage difference, absolute temperature and emitter area ratio of two neighbouring bipolar transistors. This is actually the basis for the design of temperature independent subcircuits and electronic temperature sensors.

On the contrary, V_{GS} of an MOS transistor is quite complicated function of temperature and its geometry which favours use of bipolar oriented design for temperature insensitive electronics.

2.1.4 Offset Voltage

It can be shown that the offset voltage of the bipolar differential stage can be written as:

$$V_{OS} = \frac{kT}{q}\left(-\frac{\Delta R}{R} - \frac{\Delta A_E}{A_E} - \frac{\Delta Q_B}{Q_B}\right) \quad (6)$$

V_{OS} : offset voltage

R : load resistance

A_E : emitter area

Q_B : Gummel base number given by

$$Q_B \equiv \int_{base} N(x)dx \quad (7)$$

Same expression for MOS transistor is:

$$V_{OS} = \Delta V_{TH} + \frac{V_{GS} - V_{TH}}{2}\left(-\frac{\Delta R}{R} - \frac{\Delta(W/L)}{W/L}\right) \quad (8)$$

V_{TH} : threshold voltage

Both expressions in parenthesis are caused by process and geometry short range variations. If we suppose that their value is about the same for both transistors, we see that the offset voltage of a bipolar differential stage is much lower since the value of kT/q factor (0.025 V at the room temperature) is also much lower than (V_{GS} - V_{TH})/2 of MOS transistor which is in the range of 0.25 V.

Typical offset voltage of bipolar differential stage is 1 mV while for MOS differential stage it is around 10 - 15 mV.

2.1.5 Noise

It would be out of the scope of this paper to discuss the noise aspects of both transistors in details. However, some general statements can be made. It has been widely accepted for a long time that bipolar transistors have lower noise than MOS especially since they exhibit low 1/f noise which is usually neglected, while for MOS transistors' 1/f noise is high. Lately, MOS designers have, using some inventive and careful design techniques, succeeded in bringing MOS circuit noise figures down to the levels comparable to bipolars. This was achieved at the expense of larger circuit area/silicon but at the same time such MOS stages have several times lower input currents than bipolar counterparts.

2.1.6 Power Consumption

In general, bipolar ICs are known to dissipate a lot of power while due to inherent working principles CMOS circuits assure zero power supply quiescent current at DC conditions.

2.1.7 Input Current

MOS transistors have almost infinite input impedance, since there is practically no current flow into MOS gates.

2.1.8 Ideal Switch

So far we have compared MOS and bipolar transistors as voltage controlled current sources. It is obvious that in the active region of operation bipolar transistor outperforms MOS.

However, bipolar transistor in saturation (very low values of V_{CE}) actually operates with forward polarised collector to base voltage. This region of operation is difficult to control. On the contrary, MOS transistor can be used either as voltage controlled resistor (linear region) or just as a switch; with gate voltage below threshold it is completely blocked, while condition $V_{GS} > V_{TH}$ assures conduction, figure 2.

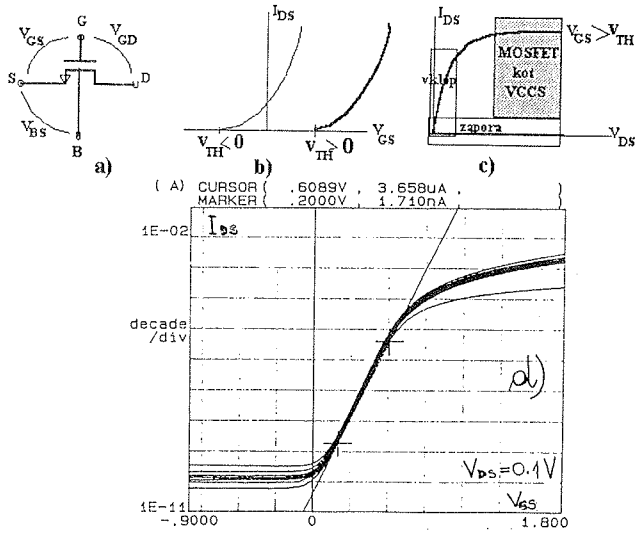

Fig. 2: MOS transistor and its regions of operation
a) electrical symbol
b) input characteristics
c) output characteristics
d) subthreshold characteristics

2.2 Synergy of Bipolar and MOS Technology

In table 1 advantages and disadvantages of bipolar and CMOS transistors are listed regarding their use in analog-digital design. BiCMOS option is added.

Ideally, it seems like BiCMOS technology could pick up only good sites of each technology. Only to start with, somebody could design certain full MOS or full bipolar subcircuits within one single chip. This is probably the easiest way to integrate MOS and BIP transistors but as mentioned previously synergy of MOS and BIP transistors on the cell level would be a new qualitative jump.

Although BiCMOS is more complex due to more process steps, it is also more robust and offers more flexibility to the designers.

But there is another aspect which makes BiCMOS technology so attractive. Introduction of BiCMOS practically does not require any investments into clean rooms or new equipment, only the process must be modified as a first step. It seems that by smartly transferring some designs originally fabricated using CMOS or BIP processes to BiCMOS their performance increases by as much as factor 2. This is definitely a strong argument for an ASIC manufacturer who is strongly involved in analog-digital design to start introducing this new technology in his technology portfolio.

Table 1: CMOS and BIPOLAR technology comparison

PARAMETER	CMOS	BIP	BiCMOS
High transconductance		0	0
High open circuit voltage gain		0	0
Simple temperature behaviour		0	0
Low offset voltage		0	0
Low noise	(1)	0	0
High speed	(2)	0	0
Low power consumption	0		CMOS part
Zero input current - high input impedance	0		CMOS part
Ideal switch	0		CMOS part
Good capacitive load driving capabilities		0	BIP part
Very small geometries (ULSI)	0	(3)	CMOS part
Mature high yielding technology	0		CMOS part

(1) CMOS noise improves with smart design techniques
(2) CMOS speed improves with smaller gate lengths
(3) minimum geometry MOS transistor is smaller than minimum geometry BIP transistor

3. BiCMOS TECHNOLOGY

3.1 Introduction

Three categories of BiCMOS ICs have emerged, / 6 /:
- low cost, medium speed 5 V digital
- high performance, higher cost 5 V digital
- analog - digital

The distinction among these are based on differences in the process flows used to produce them.

Low cost BiCMOS parts are fabricated with slightly modified, single well CMOS processes (only one or two masks are added to a baseline CMOS process).

High performance digital BiCMOS ICs are fabricated with twin well, CMOS based process flows that are significantly modified from the baseline CMOS process (three or four mask levels are typically added).

Analog - digital BiCMOS ICs are fabricated with processes designed to accommodate the larger voltage levels of analog applications (e.g. 10-30 V for low voltage analog circuits and more than 30 V for power applications). Analog digital processes must also permit the production of the resistors, capacitors and isolated PNP transistors needed in analog circuits in addition to allowing the fabrication of NPN bipolar and CMOS structures. Analog circuit requirements are such that they can still be met by devices built with less aggressive design rules than those needed in digital circuits.

3.2 Medium Voltage Analog-Digital BiCMOS

As mentioned earlier, the possibility to produce analog and digital functions on the same chip provides significant benefits to the manufacturer of ICs. For example, CMOS can be used to minimise DC power dissipation and provide high impedance FET inputs for certain operations. Bipolar devices can not only provide high current gain and extended bandwidth capabilities but they can also be used to minimise noise factors and provide good on chip voltage references.

The differences between analog-digital BiCMOS and 5 V digital BiCMOS processes stem primarily from the fact that analog functions generally operate over a much wider range of power supply voltages (higher than 10 V) and power dissipation levels. However, medium voltage analog-digital circuits require 10-15 V operating voltages in order to maintain high signal to noise ratios and to permit the use of cascading in analog design. Some CMOS speed performance must be traded off to gain reliable operation at the increased voltage levels, for example thicker gate oxides are needed to withstand higher gate voltages while due to this, MOS transistor transconductances are reduced.

For analog function circuit design, the most important device characteristics are those of NPN transistors. High gain is required to reduce input bias current into transistor and to prevent the loading of a previous stage. A value of 100 or more is usually satisfactory and f_T values above 2 GHz are welcome. The transistors must also have low R_C values (below 100 Ω) to allow high current operation, as well as high Early voltage (V_A) values (greater than 50 V), since, as noted in section 2.1.2, the intrinsic small signal voltage gain of an amplifier is proportional to V_A.

Isolated PNP transistors are also needed in some analog circuits. Although lateral PNP transistors are "free" devices, their speed performance is poor. So in certain cases vertical isolated PNP transistors must be built to satisfy above requirements.

The higher operating voltages also limit the minimum gate lengths of MOS devices to 2-3 μm in analog-digital BiCMOS to prevent premature breakdowns and short

channel effects. Furthermore, since analog designs often use both positive and negative supply voltages, isolated CMOS structures are desirable.

Thicker field oxides are also usually needed to provide field region threshold voltage values that exceed the maximum operating voltage. Likewise, the CMOS devices must be protected against hot carrier effects that arise as a result of exposure to higher supply voltages. Latchup is another concern due to high substrate currents common in many analog BiCMOS designs.

3.3 Triple Diffused BiCMOS Technology

Triple diffused (3D) BiCMOS technology has got its name according to the way that bipolar NPN or isolated PNP transistors are produced. In this case *all three* transistor regions: Emitter, Base and Collector are first successively doped, usually by ion implantation, and then separately *diffused* into silicon substrate to form corresponding areas.

The easiest way to realise such an approach is to start with "digital" high yielding n-well CMOS process to which certain process modules are added, /4/. Basic CMOS allows the formation of standard MOS structures which are well characterised while with new modules bipolar vertical NPN transistors, isolated vertical PNP transistors, double poly capacitors and high resistivity polysilicon resistors are made. This approach is depicted in figure 3.

Please, note that this modular approach allows easy tailoring of the technology to the specific needs of the design, as well as easy deletion or addition of the components in question.

3D BiCMOS as presented here has some advantages and some disadvantages regarding analog-digital design.

Advantages are the following:

- starting material is the same as for the established n-well digital CMOS which means that there is no need to buy expensive EPI wafers
- this process does not require formation of buried layers
- basic process flow is altered only as much as needed which assures high yield and built-in reliability
- there is no need to buy new generation of equipment: all new modules can be realised with the equipment which is already on the floor

Disadvantages are the following:

- bipolar transistors are not optimised regarding low collector resistance
- although simple to start with, 3D BiCMOS becomes complex with addition of new masks if we want to optimise several device parameters at a time
- BiCMOS built on wafers without EPI is more susceptible to latch up and less immune to noise

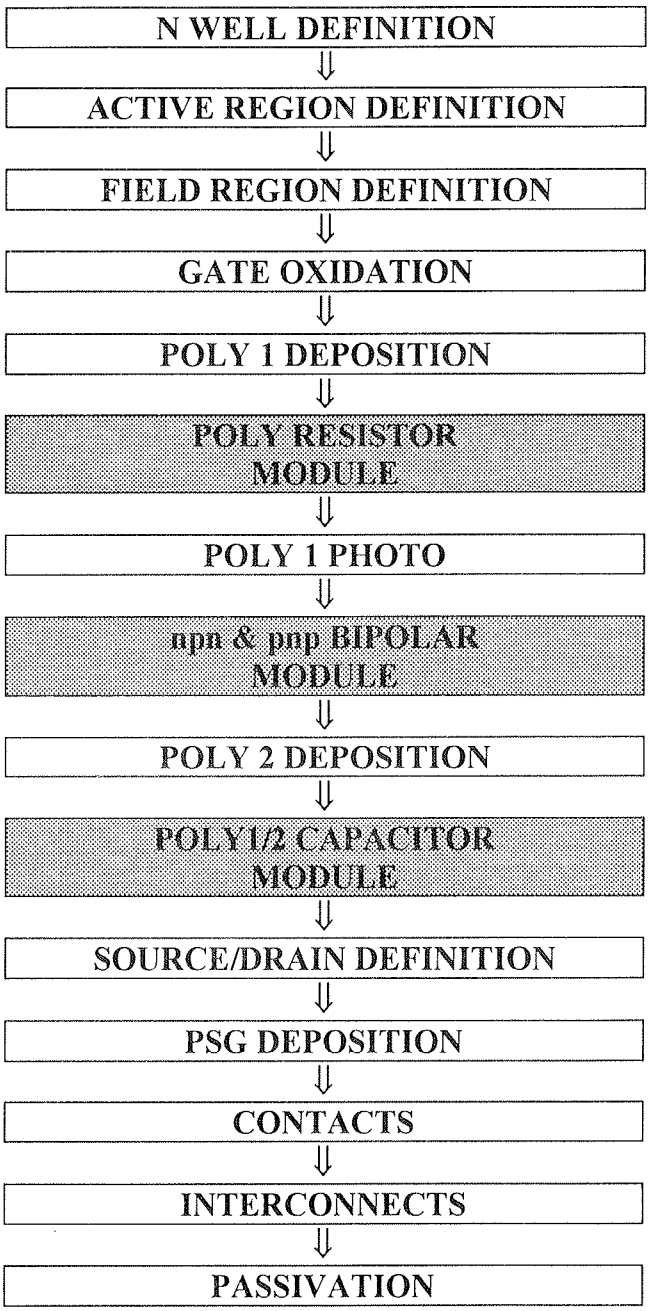

Fig. 3: Simplified flow chart of 3D BiCMOS process showing modules added to basic n-well CMOS in order to make vertical NPN and PNP bipolars, double poly capacitors and polysilicon resistors

In the next sections the overview of all active and passive components that can be built with 3D BiCMOS is presented.

3.3.1 MOS Transistors

The structure of NMOS and PMOS transistors is a basic one as can be seen in figure 4. N type polysilicon gate together with gate oxide and channel implant define threshold voltage which is one of the most important

transistor electrical parameters. Its typical value range is between 0.6 V and 1.0 V, figure 5. It is important to mention that PMOS transistor is of a buried channel type, since its surface is, due to boron channel implant, p type and conduction channel is actually formed below the surface.

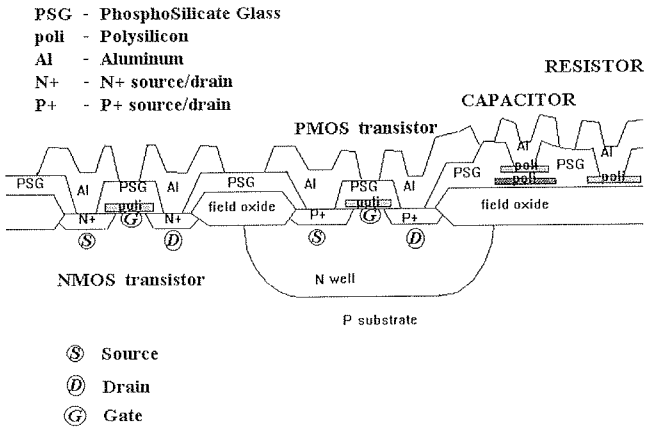

Fig. 4: Cross section of the basic CMOS process showing NMOS and PMOS transistors, double poly capacitors and polysilicon resistors

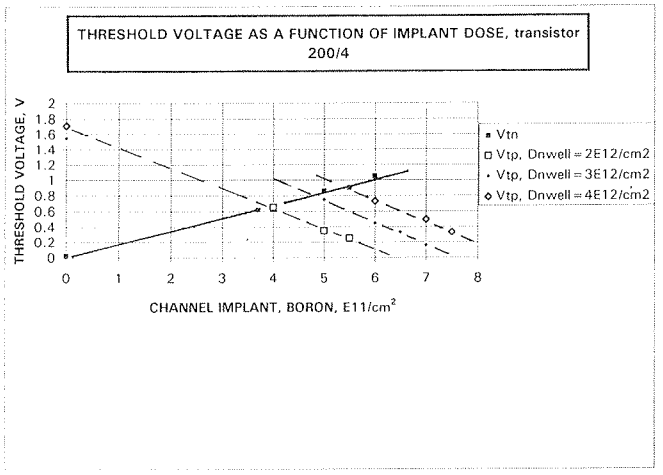

Fig. 5: NMOS and PMOS transistor thresholds as a function of n well and channel implant doses.

Concentration of the p substrate for NMOS and of the n well for PMOS transistors, defines their body factors which describe the behaviour of threshold voltage as a function of applied substrate bias. Due to higher n well concentration, compared to p substrate, PMOS transistors have higher body factor. Ideally, it should be as low as possible.

Another important transistor parameter is its transconductance which is given as :

$$g_m = \mu \cdot C_{OX} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{DS} \qquad (9)$$

μ : charge mobility

C_{OX} : gate capacitance per unit area

W_{eff} : effective channel width

L_{eff} : effective channel length

V_{DS} : drain to source voltage

Device designer would like to have as high transconductance as possible. This can obviously be achieved with high mobility, large gate oxide capacitance (thin gate oxide), wide and short channel and high applied voltage. Of course, all these parameters can not be altered deliberately. On one side, electron (hole) mobility decreases with increasing channel concentration, increasing gate voltage and finally with increasing lateral electric field which is defined as the ratio of applied voltage and effective channel length. Also, too thin gate oxide can cause reliability problems, while short channel effects can cause premature transistor breakdown and excessive leakage currents. Generally, we can say that maximum allowable substrate concentration is dictated by maximum allowable values of body factor and parasitic junction capacitances in the chip. On the other side, high substrate concentration allows higher transistor breakdowns and less pronounced short channel effects. The same is true for channel doping: its maximum value affects subthreshold swing and charge mobility while low values allow premature surface breakdown. To conclude: careful device design is needed which must take into account all these factors to bring all important transistor electrical parameters within the acceptable window for successful analog-digital design.

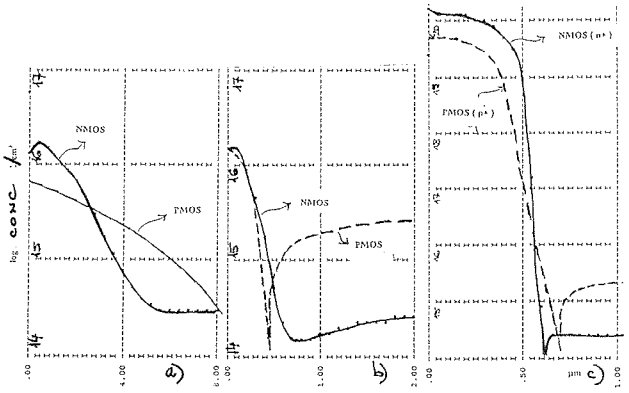

Fig. 6: Dopant profiles for different device regions, CMOS part of 3D BiCMOS
a) passive (field) region
b) active region, MOS transistor channel
c) active region, source/drain

In figure 6 simulated dopant profiles for different CMOS regions are depicted, while in table 2 some basic process and electrical parameters are presented.

Table 2: Typical process and CMOS device electrical parameters, 3D BiCMOS process

PARAMETER	unit	NMOS	PMOS
PROCESS PARAMETERS			
Gate oxide thickness	nm	70(50)	70(50)
Field oxide thickness	nm	1000	1000
Polysilicon thickness	nm	500	500
Junction depth, MOS source/drain	µm	0.54	0.64
Junction depth, n well	µm		9.5
ELECTRICAL PARAMETERS			
Power supply voltage, digital part	V	5	5
Power supply voltage, analog part	V	12	12
Field transistor threshold	V	>15	<-15
Active transistor threshold, 200/4	V	0.8	-0.8
Transconductance factor at V_{DS} = 0.1 V	$\mu A/V^2$	32	12
Body factor at V_{BS} = 5V	$\sqrt{V}$	0.23	0.76
Active transistor source - drain breakdown, BV_{DSS}	V	>15	<-15
Maximum carrier mobility	cm^2/Vs	696	260
Substrate concentration	$/cm^3$	3.2E14	3.8E15
Source/drain sheet resistivity	Ω/□	17	65
N well sheet resistivity	kΩ/□		4

All MOS discrete devices have been electrically characterised for their relevant parameters, their temperature dependence measured when necessary and their uniformity on the wafer evaluated. As an example, in figure 7 we show comparison of measured and calculated transistor characteristics using extracted SPICE parameters. Obviously, the match is satisfactory.

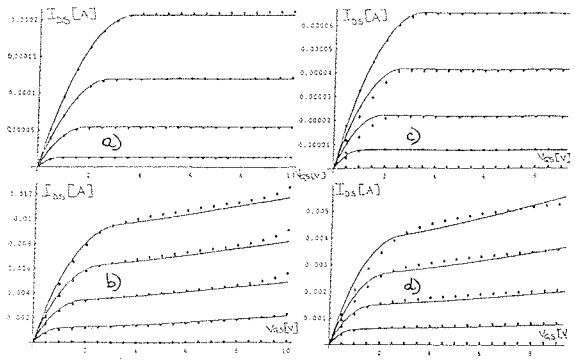

Fig. 7: Measured (points) and calculated (solid lines) transistor characteristics from SPICE
a) NMOS 100/100
b) NMOS 200/4
c) PMOS 100/100
d) PMOS 200/4

3.3.2 Composite Bipolar Transistor

Original n-well CMOS process allows formation of lateral isolated PNP and vertical PNP bipolar devices. However their performance is quite poor and usually they are used by designers as one composite device, where collector of the isolated PNP is tied to the wafer substrate which is at the same time collector for vertical PNP bipolar transistor, figure 8.

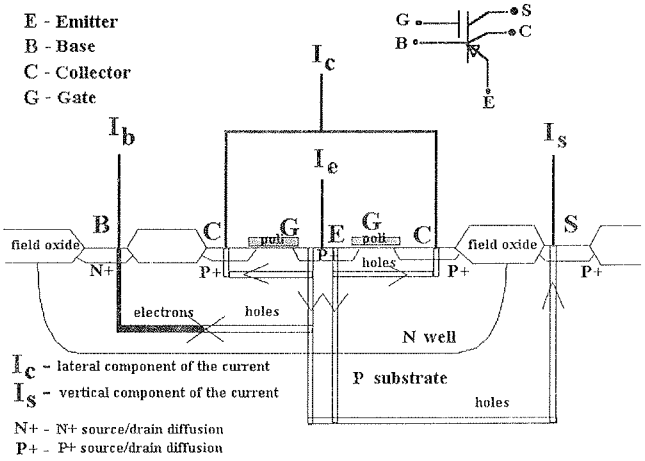

Fig. 8: Cross section and components of the current, composite PNP transistor

As can be seen from the figure 8, transistor base width is determined by difference in junction depths of its emitter and n-well in case of the vertical PNP device and by lateral distance between emitter and collector (two p+ source/drain diffusions) in case of the lateral PNP transistor. Please, note that in the particular transistor design shown in figure 8, polysilicon gate is used to define lateral E-C distance.

Transistor current components can be expressed as follows:

$$I_C = \alpha \cdot I_E \quad and \quad I_S = (1-\alpha) \cdot I_E \tag{10}$$

I_E : emitter current

$\alpha < 1$

I_S : substrate, collector current of the vertical PNP

Out of this we can define several transistor current gains as:

$$\beta_L = \frac{I_C}{I_B} \quad and \quad \beta_V = \frac{I_S}{I_B} \quad and \quad \beta_{tot} = \beta_L + \beta_V \tag{11}$$

β_L : lateral transistor common emitter current gain

β_V : vertical transistor common emitter current gain

β_{TOT} : composite transistor common emitter total current gain

Basically, designers could use each of the three transistors separately. In that case, their common emitter current gains are defined with equation 11. In case only isolated lateral PNP is needed, it should be optimised regarding lateral current component by increasing periphery to area ratio and by minimising vertical current component. The opposite is true for vertical PNP transistor.

In table 3 typical electrical parameters of the composite PNP bipolar transistor are given.

Table 3 : Typical electrical parameters for the composite PNP bipolar transistor, 3D BiCMOS process

PARAMETER	unit	value	comment
Emitter area	μm^2	8 x 8	changeable
Maximum common emitter current gain		150-200	process dependent
Collector series resistance	Ω	500-800	process dependent
Early voltage	V	<70	process dependent
BV_{EBO}	V	35-40	process dependent
BV_{CBO}	V	35-45	process dependent
BV_{CEO}	V	25-30	process dependent

Process parameters which affect composite PNP transistor electrical parameters and which can be changed during the process are:

- transistor lateral dimensions (polysilicon mask change)
- implant and well diffusion conditions for n-well definition
- implant and n+/p+ diffusion conditions for source/-drain definition

3.3.3 Vertical Isolated NPN Transistor

We need to introduce at least one new mask, one implant and one high temperature step to be able to make vertical isolated NPN transistor which would be suitable for analog design. After polysilicon resistor mask, the following steps should be added to the basic CMOS flow chart, figure 9:

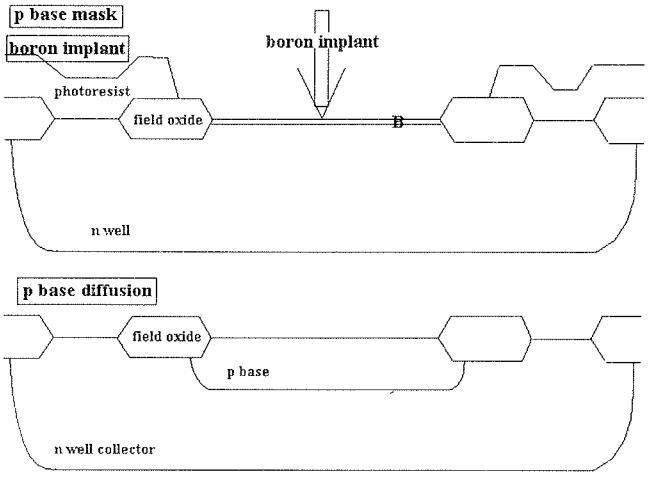

Fig. 9: Process steps needed to make collector and base of the vertical isolated NPN bipolar transistor, 3D BiCMOS process

- p base mask
- p base implant, boron, 100 keV, dose in the range 0.5 - 3E13/cm^2
- p base diffusion

In this case, transistor collector is defined with n-well mask, n-well implant and diffusion conditions, its base with the above described process steps, while emitter is defined with same process steps as NMOS transistor's source/drain.

Table 4: Vertical isolated NPN bipolar transistor electrical parameters as function of process parameters, 3D BiCMOS process, minimum size transistor

n well dose /cm^2	p base dose /cm^2	W_B simulated µm	β max	rc kΩ	BV_{EBO} V	BV_{CBO} V	BV_{CEO} V	V_A V
4.5E12	9E12	1.35	350	0.869	18	43	43	55
4.5E12	1.25E13	2.85	110	1.67	18	52	52	>60
4.5E12	2E13	3.2	60	1.73	15.5	68	68	>60
3E12	2E13	3.48	66	4	16.4	90	90	
2E12	2E13	3.76	65	16.6	16.4	105	105	
1E12	2E13	3.96	1	17.3	14	90	90	

Of course, transistor electrical characteristics are very sensitive to the process conditions used to make its active regions. This is well demonstrated in table 4, where basic isolated NPN transistor electrical parameters are shown together with some process data.

Immediately, we notice that high enough current gains (usually above 100 is required), figure 10, and suitable breakdown voltages can easily be achieved, while collector series resistances are very high, as expected. Also, Early voltages are well above the limits needed for analog design.

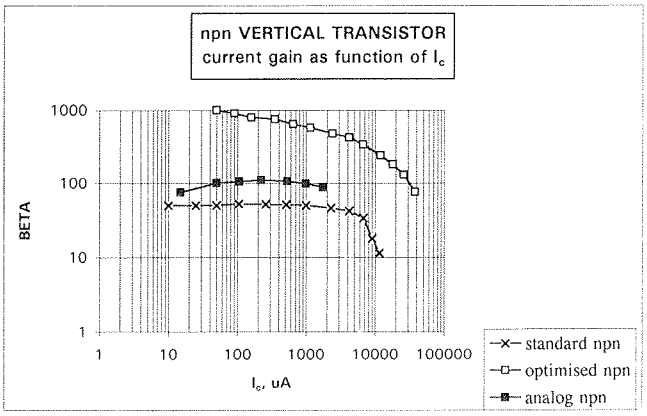

Fig. 10: Current gain as a function of collector current, vertical isolated NPN bipolar transistor, 3D BiCMOS process

High collector series resistance calls for some immediate corrective actions which will be described in the next section.

3.3.4 Collector Series Resistance Optimisation - NPN Vertical Bipolar Transistor

In figure 11, different contributions to collector series resistance are shown. Besides lateral contribution (r_{Cl}) due to collector current flowing below base, there is also vertical contribution due to current flowing into the surface contact (r_{Cv}). Ideally, both of them should be as low as possible.

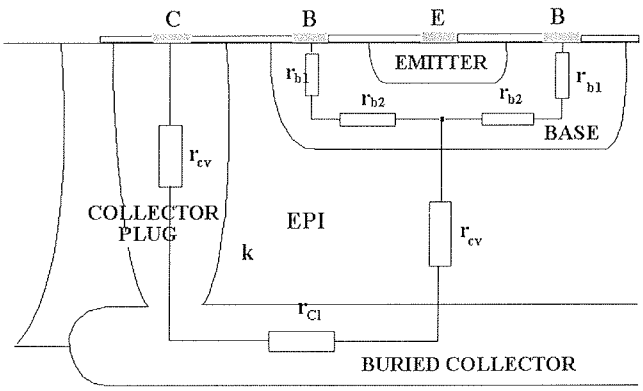

Fig. 11: Contributions to collector series resistance, vertical NPN bipolar transistor

There are two basic approaches for diminishing collector series resistance:

- process
- geometric

Process approaches usually require addition of one or more process steps (mask, implant, diffusion) while geometric approaches require change in device geometry. We will first describe some process and then one geometric approach to device collector series resistance optimisation.

Introduction of Extra Collector N-Well

In order to diminish lateral and vertical component of collector resistance, we must increase collector doping level. If we use the same well as for MOS devices we can not alter its concentration deliberately since we are limited by required active MOS devices performance, which would be affected by this change.

So, in order to be flexible enough, we must introduce new collector n-well which background concentration must be much higher than that of the device n-well. Of course, this requires at least one new mask and one phosphorous implant more while collector n-well diffusion can be done at the same time as device well diffusion.

In figure 12 we show the effect of extra collector well implant on collector resistance of vertical NPN bipolar transistor. Unfortunately, other device parameters are also changed. This can be seen in table 5. By increasing collector concentration we decrease its resistance and all transistor breakdown voltages, while current gain increases. Of course, for analog design there is an optimum set of process conditions which must be used to make suitable vertical NPN transistor. Taking this into account, we see that collector resistance reduction that can be achieved by this method is in the range of 50%.

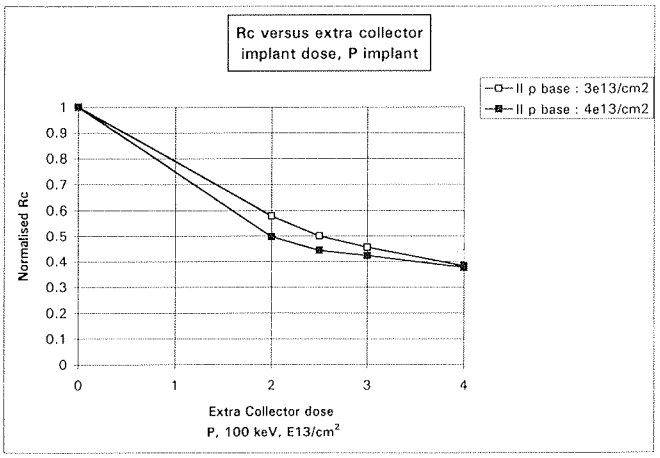

Fig. 12: Collector resistance relative change as a function of extra collector well implant dose, vertical isolated NPN bipolar transistor

Table 5: Effect of extra collector well implant on electrical parameters of vertical NPN bipolar transistor, 3D BiCMOS process, minimum size transistor

Collector well dose /cm^2	W_B simulated µm	β max	r_c normalized	BV_{EBO} V	BV_{EBO} V	BV_{EBO} V
3E12	3.9	55	1	16	95	51
2E13	2.1	120	0.58	19	25	18
2.5E13	1.9	158	0.5	21	21	15
3E13	1.7	293	0.46	21	20	13
4E13	1.3	780	0.38	28	18	11

Introduction of Collector Plug

We have seen that higher collector well doping affects whole transistor area and all of its electrical parameters. It would be ideal if we were able to increase collector doping only in its passive area, away from base. In fact, this can partially be achieved by additionally implanting only collector contacts as shown in figure 13. In this way only vertical part of collector series resistance would be affected. This implantation is performed prior to base diffusion and requires additional "plug" mask which is in effect reverse p base mask which allows implantation only in the transistor collector contact areas. Again, phosphorous is implanted and total emitter contact & plug profile is shown in figure 13b.

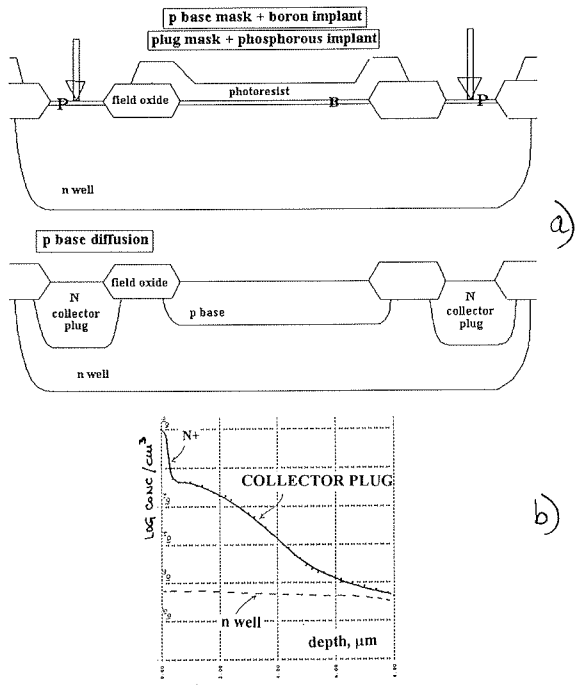

Fig. 13: a) Process steps needed to make collector plug of the vertical isolated NPN bipolar transistor, 3D BiCMOS process
b) Doping profile of the collector plug, SUPREM simulation

By introducing collector plug we expect to further decrease collector series resistance by 50%.

Buried Collector

The most effective way to lower only lateral component of collector series resistance is to increase collector doping level below base leaving enough space between base and buried collector not to affect BV_{CBO}, figure 11. This is usually achieved by first selectively implanting all collector areas in a chip with arsenic and then by growing silicon EPI layer over it. In the EPI layer all active devices are then built above their respective buried layers.

This approach requires EPI reactor in house or use of EPI deposition service in another company.

Although being the most effective, this approach is also the most expensive.

There exist some other techniques to make buried layers without need for subsequent EPI deposition. One of the most exotic ones is high energy ion implantation /10/. In this case phosphorous (arsenic) is implanted through suitable mask 1 to 3 µm deep into silicon to make high concentration buried layer below NPN transistor base. Again, this approach requires expensive equipment and is limited in the depth to which ions can be implanted.

Neither of the above two mentioned techniques for formation of buried layer were implemented into our 3D BiCMOS process.

Transistor Topology Optimisation

Standard vertical NPN transistor geometry is shown in figures 14a and 15a. Emitter is in the middle of the structure, completely surrounded by the base and col-

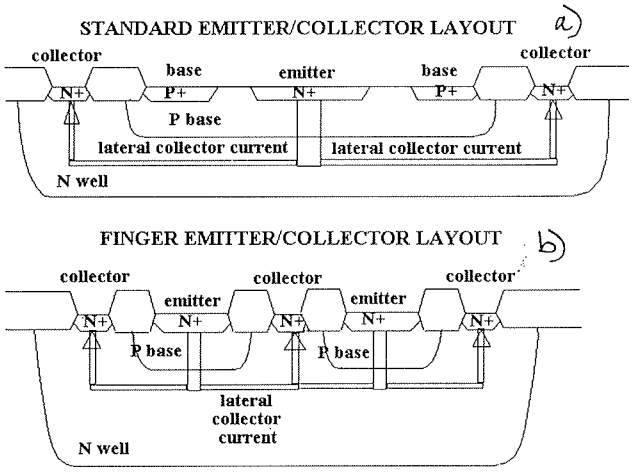

Fig. 14: Cross section of vertical NPN transistor
a) structure with emitter in the centre
b) structure with interdigitated emitter and collector

lector. Since collector current flows laterally below the base, lateral component of collector series resistance is directly proportional to the distance between emitter and collector contacts on the surface. In order to lower this resistance, we should make these two contacts as close to each other as possible. This is actually achieved by finger layout where emitter and collector are interdigitated, figures 14b and 15b.

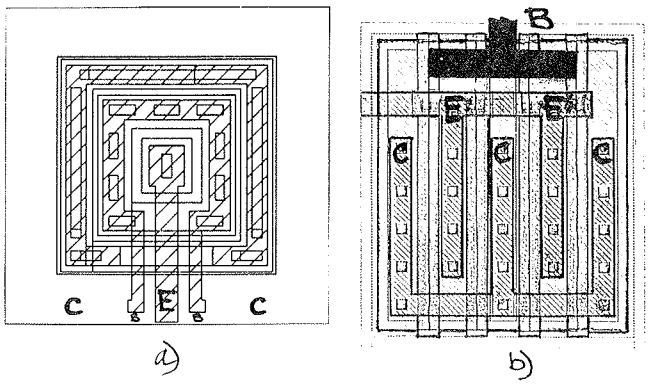

Fig. 15: Layout of vertical NPN transistor
a) standard layout with emitter in the middle
b) optimised layout, structure with interdigitated emitter and collector

Comparison of the current characteristics of two bipolar NPN transistors with approximately equal emitter areas shows pronounced improvement of collector series resistance of the finger structure compared to standard one, figure 16.

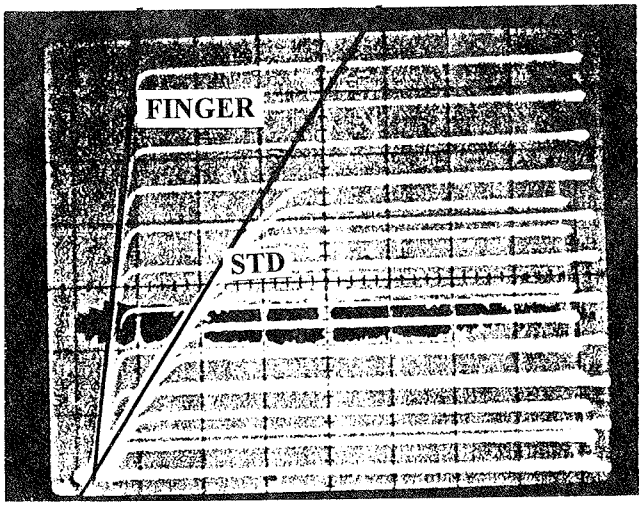

Fig. 16: Comparison of the current characteristics of two bipolar NPN transistors with approximately equal emitter areas,
$r_{C\ standard} / r_{C\ finger} \approx 4$.

Conclusion

In this section we have shown that we are able to make vertical isolated NPN bipolar transistor with the electrical parameters very suitable for analog applications.

We can easily obtain current gains well above 100, all breakdown voltages above 18 V and Early voltage in the range of 50-60 V. Due to its inherent structure, 3D vertical NPN transistor has high collector series resistance. However, with some improvements in the geometrical layout of the structure, with introduction of one to two new masks and ion implant steps we can lower this resistance by factor of 4-8, compared to standard - one added mask 3D BiCMOS NPN transistor. This means that by increasing 3D BiCMOS process complexity we are able to bring collector series resistance down to the values acceptable for analog design.

3.3.5 Vertical Isolated PNP Bipolar Transistor

The idea behind making another, this time isolated vertical PNP transistor (remember: vertical PNP already comes for free in original CMOS, but with wafer substrate as its collector) is to use p base of vertical NPN as the collector for isolated vertical PNP transistor. Of course, this can be achieved by adding another n base mask after p base diffusion and by implanting n base areas of PNP transistor with phosphorous. A short drive in cycle follows this implantation to allow phosphorous to diffuse deeper into the base. Cross section of vertical isolated PNP transistor together with its simulated profile is shown in figure 17.

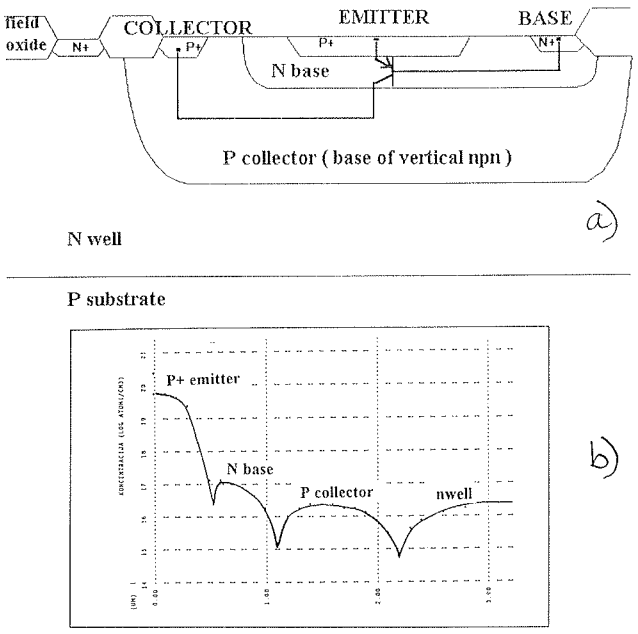

Fig. 17: Vertical isolated PNP bipolar transistor, 3D BiCMOS process
a) cross section
b) simulated SUPREM profile

Electrical characteristics of such a transistor are very attractive as shown in table 6. As well its current gain versus collector current is depicted in figure 18.

Table 6: Vertical isolated PNP bipolar transistor, basic electrical parameters, emitter area 20x20 μm², 3D BiCMOS process

W_B, simulated μm	β_{max}	BV_{EB0} V	BV_{CB0} V	BV_{CE0} V	V_A V
0.73	110	11.5	32	17	11

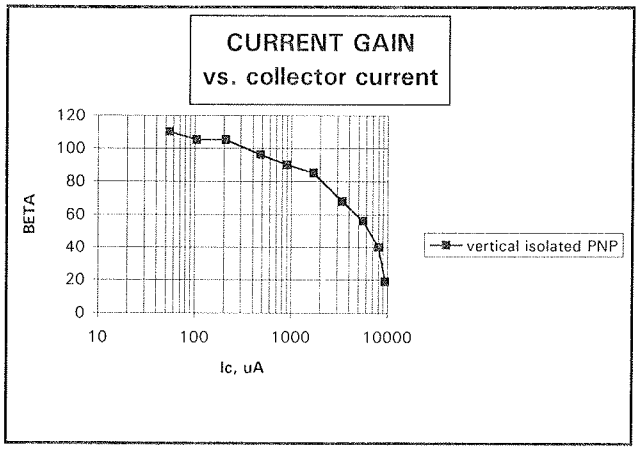

Fig. 18: Common emitter current gain as function of collector current, vertical isolated PNP bipolar transistor, 3D BiCMOS process

3.3.6 Integrated Diodes

Any of the several pn junctions made in 3D BiCMOS process can be used as a diode. They come for free although their leakage current, as well as capacitance are parasitic parameters, unless used on purpose. In table 7 we present an overview of all possible diodes encountered in our particular 3D BiCMOS process.

3.3.7 Integrated Capacitors

3D BiCMOS technology offers wide spectrum of diffused and MOS capacitors. In today's modern design of analog digital ASICs, the designers relatively seldom use dif-

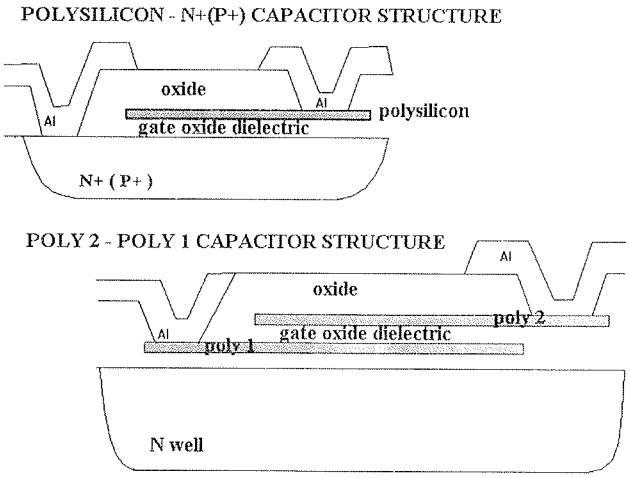

Fig. 19: Cross section of two possible capacitor structures, 3D BiCMOS process

Table 7: All possible diode structures in 3D BiCMOS process

DIODE TYPE	DIODE STRUCTURE	BV at 10 μA, V	COMMENT
n+ psub	n+: source/drain of NMOS psub: p substrate	>19	breakdown of n+ to p field
n+ pbase	n+:source/drain of NMOS pbase: base of a vertical NPN	10	
nbase psub	nbase: base of a vertical PNP psub: p substrate		
nbase pbase	nbase: base of a vertical PNP pbase: base of a vertical NPN	>30	affected by base doping
nwell psub	nwell: nwell for PMOS psub: p substrate	190	affected by substrate resistivity
p+ nwell	p+: source/drain of PMOS nwell: nwell for PMOS	-19	breakdown of p+ to n field
p+ nbase	p+: source/drain of PMOS nbase: base of a lateral PNP	-35	breakdown of p+ to n well
p+ nbase	p+: source/drain of PMOS nbase: base of a vertical PNP	-12	breakdown of p+ to n base of PNP
pbase nwell	pbase: base of a vertical NPN nwell: nwell for PMOS	-95	affected by nwell doping
n+ p+ ZENER	n+: source/drain of NMOS p+: source/drain of PMOS	5.3 - 5.6	lateral ZENER diode

fused capacitors due to their voltage dependent capacitance. MOS capacitors are more interesting since high capacitance per unit area and voltage independence can be easily achieved.

Two MOS capacitor structures are of great importance, as shown in figure 19: polysilicon to n+ (p+) capacitor and double poly capacitor.

In both cases we use silicon dioxide as the dielectric, grown during gate oxide step. Capacitance of such a structure is given with the expression:

$$C = \frac{\varepsilon \cdot \varepsilon_0}{d_{ox}} A \qquad (12)$$

ε : silicon dioxide dielectric constant (3.8)

dox : capacitor oxide thickness

A : capacitor area

Since oxide thickness is usually in the range of 50-90 nm, typical obtained capacitance is in the range of 0.37-0.67 fF/μm^2. In our particular case, this capacitance is 0.4± 0.02 fF/μm^2.

With both presented structures we can make capacitors which are voltage independent (less than 50 ppm/V), with low temperature coefficient of capacitance (below 30 ppm/°C), as well as achieved capacitance ratios are within 0.1%. However, double poly capacitor structure is the most popular one in analog digital design due to its low leakage current towards substrate.

Designers of analog circuits usually use so called "unity" capacitors with which very precise capacitance ratios can be achieved. These capacitors are usually square in geometry with absolute capacitance in the range of 1 pF. In such a case its dimensions would be 50 μm x 50 μm. Change in absolute capacitance is due to variation of capacitor area, dielectric thickness and its dielectric constant. Summing all these contributions we arrive to the capacitance relative accuracy value of ±6% within one lot. However, better results can be achieved for matching, as we will see later.

3.3.8 Integrated Resistors

General

3D BiCMOS process allows realisation of:

- diffused and
- thin film

resistors, table 8. Diffused resistors are defined usually by ion implantation and then by subsequent diffusion step. All implants used in the process like nwell, pbase, nbase, n+, and p+, already give resistors with sheet resistivity in the range 25-4000 Ω/□.

There are also two thin film resistors: polysilicon and aluminium. While aluminium has very low sheet resistivity (about 35 mΩ/□ for the thickness of 1 μm), polysilicon looks more promising since its resistivity can be changed by thickness and doping variation within very broad range.

In figure 20 the geometries of diffused and thin film resistors are compared. In both cases their resistance is defined by the equation:

$$R = \rho \cdot \frac{L}{d \cdot W} = R_{sh} \cdot \frac{L}{W}, \quad R_{sh} = \frac{\rho}{d} \qquad (13)$$

ρ : specific resistivity of the film or doped region

L : resistor length

W : resistor width

d : resistor thickness

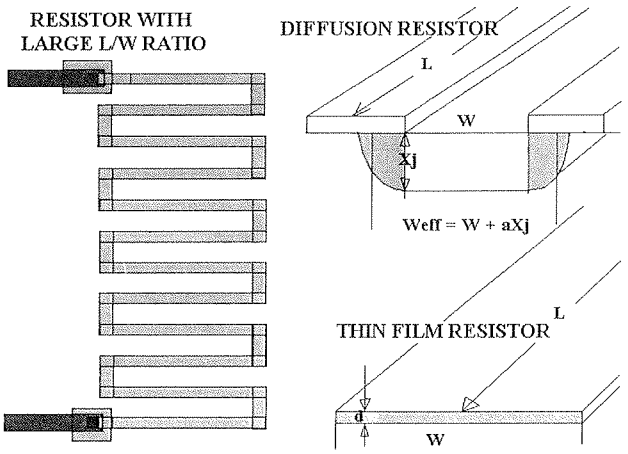

Fig. 20: Geometry and structure of diffused and thin film resistors, 3D BiCMOS process

Diffused resistor lateral dimensions are defined with active mask (for p+, n+, pbase or nbase resistor) or nwell mask (for nwell resistor). Polysilicon resistor lateral dimensions are defined only by poly mask and plasma etch step. Absolute mask dimension accuracy is in both cases similar while for diffused resistor we know that side dopant diffusion additionally affects its lateral dimensions especially in the case of deep well. In this case we must rewrite equation 13 as:

$$R = R_{sh} \cdot \frac{L}{W_{eff}} = R_{sh} \cdot \frac{L}{W + \alpha \cdot x_j}, \quad \alpha < 1 \qquad (14)$$

xj : junction depth, diffused resistor

Weff : effective resistor width

Even in the case of large L/W ratios relative accuracy achieved is in the range ±6 % for low R_{sh} and ±10% for high R_{sh} resistors within one wafer lot.

One big drawback of weakly doped diffused resistors (nwell, pbase, nbase) is their voltage dependent resistance. This happens because depletion layer width changes with voltage, inducing resistor geometry and consequently its resistance change.

Table 8: Overview of diffused and thin film resistors, 3D BiCMOS process

RESISTOR	Dopant	R_{sh} Ω/□	Relative accuracy, %	Temp. coeffic. Ω/□/°C
n+ diffusion	AS implantation	17	6-8	0.06
p+ diffusion	B implantation	65	6-8	0.08
n well	P implantation	3500	10-20	
n base	P implantation	≥800		
p base	B implantation	≥700		
n+ poly1 or poly2	P, gaseous source	25	5	0.02
n/p poly	P/B implantation	500-40000	5-15	-41 at 10kΩ/□

High Sheet Resistivity Polysilicon Resistors

Polysilicon resistors are suitable for analog design since their geometry and doping levels can be precisely controlled within wide value range without need to worry about resistance voltage dependency like in the case of diffused resistors. As well, they are not made in the substrate which means that parasitic leakage currents and parasitic capacitances are very low.

Figure 21 presents poly sheet resistivity variation with ion implant dose for polysilicon thickness of about 500 nm. We can clearly see that sheet resistivities in the range of 500-40000 Ω/□ can be achieved.

However, when designing polysilicon resistors, we must be aware that their sheet resistivity, uniformity on the wafer and resistance matching depend on the following parameters, /11/ :

- polysilicon thickness
- dopant type and implant dose
- polysilicon deposition parameters
- polysilicon thermal history during subsequent processing
- final low temperature anneal conditions during Aluminium alloy
- final passivation type

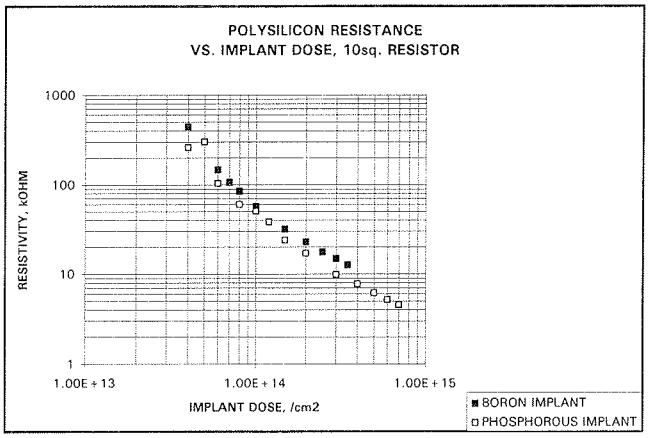

Fig. 21: Polysilicon resistance variation with ion implant dose, 3D BiCMOS process

As an illustration of above statements we show in the figure 22 polysilicon sheet resistivity change with time of anneal in hydrogen at 450°C. Hydrogen diffusion through polysilicon and its segregation on the surface of poly grains causes effective increase of free dopant concentration, consequently lowering polysilicon resistance. We see similar effect when depositing plasma silicon nitride passivation above poly resistors. It is well known that PECVD nitride contains up to 10% of free hydrogen which, during aluminium alloy, diffuses to polysilicon, causing similar resistance changes described previously.

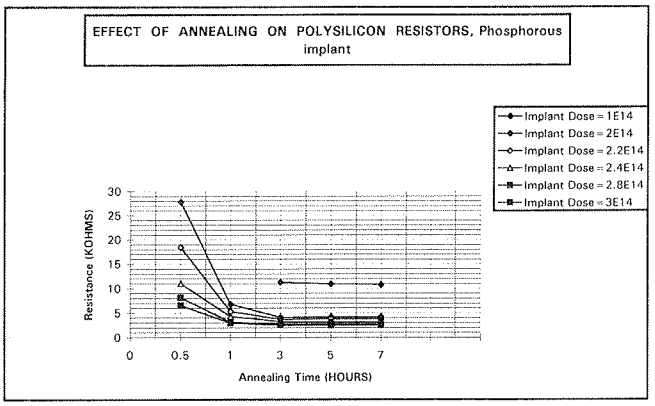

Fig. 22: Polysilicon resistance variation with anneal time in hydrogen at 450°C.

3.4 Matching of Active and Passive Devices

When talking about changes of dimensions and electrical parameters of active and passive devices in 3D BiCMOS process, we must differentiate between two basic ideas:

- global changes of parameters on a wafer or within a lot
- local changes within single chip, or difference of the same parameter between two neighbouring elements in the same chip; the degree to which we can make two devices equal locally, is cold matching

Today's design of precision analog ICs is based on devices' and their parameters' ratios rather than absolute values. This means that the precision of most analog operations within an IC is limited by poor device matching. That's why it is important to evaluate critical parameters' matching and find out reasons for mismatch.

In table 9 we bring an overview of typical values of dimensional and electrical parameters' matching for active and passive devices. Matching is defined as a difference in parameter value (absolute matching) divided with its average value (relative matching) for two neighbouring devices.

Table 9: Typical parameters' matching values, 3D BiCMOS process

PARAMETER	SYMBOL/ UNIT	TYPICAL VALUE	MATCHING max σ
MOS TRANSISTOR			
Threshold Voltage	V_{TH}, V	0.8	1%
Mobility (n)	μ_n, cm^2/Vs	700	≤1%
Mobility (p)	μ_p, cm^2/Vs	300	≤1%
Capacitance, Gate Oxide	C_{OX}, $fF/\mu m^2$	1.12	0.1%
Channel Length, Drawn	L, μm	1-5	0.1 μm
Channel Width, Drawn	W, μm	2-2000	0.1 μm
POLY2-POLY1 CAPACITOR			typical σ
Dielectric Constant	ε_{OX}	3.8	0.02%
Thickness, Gate Oxide	t_{OX}, nm	50	0.03%
Thickness, Poly1 Oxide	t_{OX}, nm	80	0.05%
Capacitor Length	L, μm	10-500	0.1 μm
Capacitor Width	W, μm	10-500	0.1 μm
DIFFERENT RESISTORS			
Diffused	R ,Ω/□	40	2%
Poly1, Difussed	R ,Ω/□	30	1%
Poly1, Implanted	R ,Ω/□	1000	1%
Resistor Length	L, μm	2-2000	0.1 μm
Resistor Width	W, μm	1-20	0.1 μm

Using above values, we can calculate matching of transconductance parameter for two neighbouring MOS transistors, as follows, /12/:

$$\frac{\sigma_k^2}{k^2} = \frac{\sigma_L^2}{L^2} + \frac{\sigma_W^2}{W^2} + \frac{\sigma_\mu^2}{\mu^2} + \frac{\sigma_C^2}{C^2} \qquad (15)$$

Taking for L = 3 μm and W = 6 μm, we get σ_k/k = 3.8 %. However, choosing larger transistors with L = 12 μm and W = 48 μm, matching goes down to about 1 %. Similarly, we can anticipate V_{TH} matching to 1 %, which gives us final MOS transistor current matching between 1-5 % !! Very important conclusion is that V_{TH}, k and I matching depend very much on transistor geometry. So, it is very important to use long and wide transistors for optimum matching.

We can draw similar conclusions for polysilicon resistors matching. Actually, we have measured matching of two neighbouring polysilicon resistors on couple of wafers made with 3D BiCMOS process. The results are shown in figure 23 for a wafer with average poly sheet resistivity of 5 kΩ/□ .

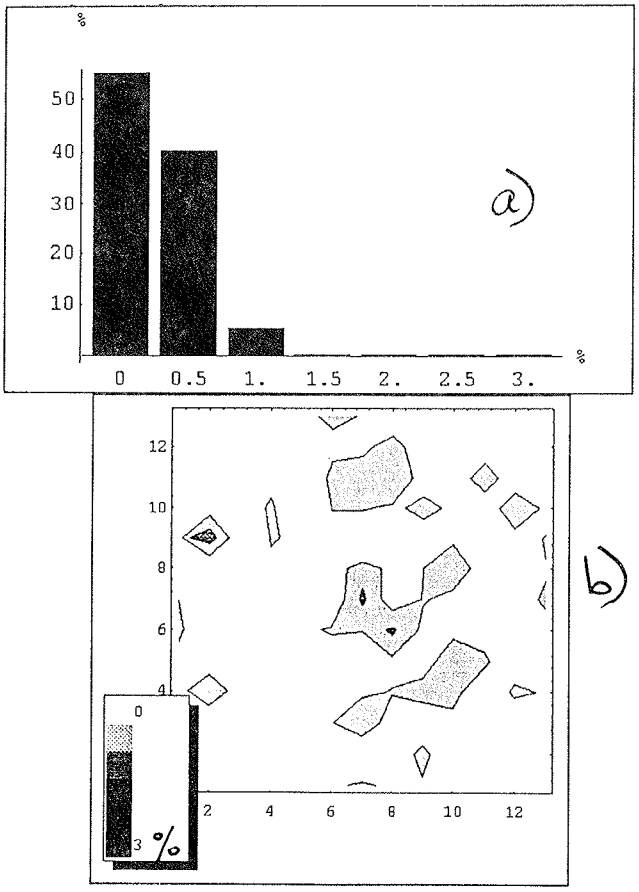

Fig. 23: Polysilicon sheet resistivity matching
a) histogram and
b) on wafer uniformity in %.
Two neighbouring polysilicon resistors with same dimensions, L = 200 μm, W = 20 μm.

Below 1% matching of resistors is typical for the average polysilicon sheet resistivity value of about 5 kΩ/□. Even better matching was observed for lower values of sheet resistivities (higher implant doses) and larger W/L ratios, as expected.

We did not directly evaluate double poly capacitance matching. However, indirect measurements of SC filter performance indicate matching to be in the range of 0.1 %.

4. CONCLUSION

We are able to join typically good CMOS technology performances as:

- low power consumption,
- almost infinite MOS transistor input impedance,
- low price per function,
- high yielding, mature digital technology,

with good bipolar transistor-technology performances like:

- large transconductance,
- low noise,
- low offset voltage,
- good driving capabilities of large capacitive loads,
- predictable temperature behaviour,

into **BiCMOS** - a new technology which offers better price-performance ratio, a lot of flexibility to the designers and a new step ahead with almost zero investment into new process equipment and clean room.

Out of several possible BiCMOS technologies, we have developed 3D BiCMOS suitable for making medium power supply voltage analog - digital ICs.

The idea behind our approach is to start with standard digital nwell CMOS technology to which certain process modules are added which allow realisation of additional:

- double poly capacitors
- high sheet resistivity polysilicon resistors
- vertical isolated NPN bipolar transistors
- vertical isolated PNP bipolar transistors

In order to allow optimisation of each of the above components for analog - digital design, several masking, implant and diffusion steps are added, thus increasing process performance and complexity. In table 10, we bring an overview of respective growing process complexity in terms of mask and process step numbers.

Table 10: Comparison of several 3D BiCMOS processes regarding process complexity

Process Steps	Digital CMOS	Analog-Digital CMOS with capacitors and poly resistors	Analog-Digital BiCMOS with simple NPN	Analog-Digital with optimised NPN	Analog-Digital BiCMOS with optimised NPN and isolated PNP
MASK LEVELS	8	10	11	13	14
PLASMA ETCHING STEPS	3	4	4	4	4
IMPLANT	5	7	8	10	11
DIFFUSION	16	17	18	18	19

Such an approach allows process tailoring to the designers' needs, as well as we believe that it is cost-performance competitive to the modern BiCMOS processes being developed for the specific product range of 10-15 V power supply analog - digital ASICs.

5. LITERATURE

/1/ E.A.Vittoz, *MOS Transistors Operated in the Lateral Bipolar Mode and their Application in CMOS Technology*, IEEE Journal of Solid State Circuits, vol.SC-18, No.3, June 1983

/2/ S.Smedley, *BiCMOS Circuit Design Using the Lateral PNP. A Model and some Circuit Applications*, Informacije MIDEM 23(1993)2, pp. 3-5

/3/ B.Gilbert, *Synergy of BiCMOS Analog Cell Design*, Intensive Summer Course on CMOS & BiCMOS VLSI Design'92, EPFL - Lausanne, Switzerland

/4/ T.Athanas, I.Šorli, I.Nedev, Modular Mixed Technology for Analog-Digital Design, to be published on MIPRO'95, Opatija, Croatia

/5/ A.Alvarez, *BiCMOS Technology and Applications*, Kluwer Academic Publishers, Boston/Dordrecht/London, 1989, ISBN 0-89838-302-1

/6/ S.Wolf, *Silicon Processing for the VLSI Era, Volume 2 - Process Integration*, Lattice Press, Sunset Beach, California, 1990, ISBN 0-9616721-4-5

/7/ T.Athanas, I.Šorli, *Mixed Technology for ASIC Devices*, Proceedings of MIEL-SD'92 Conference, 1992, Portorož, Slovenia

/8/ T.Athanas, Z.Bele, I.Šorli, *SPICE Parameter Extraction for Enhancement Silicon MOS Transistors*, Proceedings of MIEL-SD'93 Conference, 1993, Bled, Slovenia

/9/ J.Trontelj, *Trends in Mixed Signal ASIC Design*, Informacije MIDEM 24(1994)4, pp.221-226

/10/ D.Pramanik, M.I.Current, *MeV Implantation for Silicon Device Fabrication*, Solid State Technology, May 1984, pp.211-216