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Dear Reader,

This issue brings 8 selected papers based on the presentations at the two international conferences that took place in Slovenia in 2013.

The first four papers are contributed from the invited speakers at the MIDEM 2013 Conference (49th International Conference on Microelectronics, Devices and Materials with the Workshop on Digital Electronic Systems, Kranjska Gora, Slovenia, 25-27 Sep 2013) and selected by co-chairpersons Prof. Andrej Žemva and Assoc. Prof. Andrej Trost to reflect the state-of-the-art achievements from the broad field of Digital Electronic Systems.

The last four papers are a selection from the CPE 2013 (8th International Conference-Workshop Compatibility and Power Electronics, Ljubljana, Slovenia, 5-7 June 2013) by Prof. Vanja Ambrožič and Prof. Ryszard Strzelecki as General Chairmen of CPE 2013.

Since this is the last issue of the volume 43, let me reveal some statistics of the submitted manuscripts. In 2013 we have received more than 75 manuscripts, out of which 32 were accepted for publication (3 review scientific papers, 23 original scientific papers and 6 Professional Articles), whereas a dozen are still under review. Despite a well defined title of our journal and on-line instructions for authors we receive each year few manuscripts that are out of our journal's scope. The success rate of 50% in 2013 is a good foundation for the long-term quality growth of the journal. I would like to sincerely thank all reviewers for their valuable contribution to the journal quality and growing reputation. Editorial Board's commitment to high quality in the review process paths a way toward a better profiling of our journal.

Year 2013 is silently fading out. Let the last December days bring festive atmosphere, joy and peace in each home, office or research laboratory. It is the time to look back, but also to look ahead ambitiously and make plans for the coming year. This brings me to editorial wishes for 2014 that as a part of your success we have the privilege of seeing your next manuscript(s) in our inbox (editor@midem-drustvo.si).

Merry Christmas and a Happy and Prosperous New Year!

Prof. Marko Topič
Editor-in-Chief

P.S.
All papers published in Informacije MIDEM –Journal of Microelectronics, Electronics Components and Materials (since 1986) can be access electronically for free at http://midem-drustvo.si/journal/home.aspx. A search engine is provided to use it as a valuable resource for referencing previous published work and to give credit to the results achieved from other groups.

Review scientific paper

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Fixed-point Multiplication and Division in the Logarithmic Number System: a Way to Low-Power Design

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Abstract: In this article we present the use of the logarithmic number system (LNS) to implement fixed-point multiplication and division. LNS has recently attracted the interest of researchers for its low-power properties. The reduction of power dissipation in LNS arises from the simplification of basic arithmetic operations.

In this paper we give a survey of the recently proposed digital circuits for logarithm and anti-logarithm conversion and multiplication and division in LNS. We also compare these methods in terms of accuracy, area, time and power. Finally, we give an overview of the real world applications that benefit form the use of LNS arithmetic.

Keywords: computer arithmetic, logarithm number system, power dissipation

Zmanjševanje porabe v vezjih z uporabo celoštevilskega množenja in deljenja v logaritemskem številskem sistemu

Izvleček: V tem preglednem članku predstavimo uporabo logaritemskega številskega sistema za implementacijo množenja in deljenja v fiksni vejici. Logaritemski številski sistem zadnje čase vabi pozornost raziskovalcev zaradi lastnosti nizke disipacije moči. Glavni razlog za manjšo porabo energije leži v lastnosti logaritemskega številskega sistema, da poenostavlja osnovne aritmetične operacije. V članku podamo pregled predlaganih nenatančnih digitalnih vezij za množenje in deljenje v logaritemskem sistemu ter jih primerjamo glede na natančnost ter porabo prostora, časa in moči. Na koncu podamo pregled vsakdanjih aplikacij v katerih lahko učinkovito uporabimo nenatančno logaritemsko aritmetiko in tako zmanjšamo porabo energije, ne da bi bistveno vplivali na natančnost in zanesljivost algoritmov.

Ključne besede: računalniška aritmetika, logaritemski številski sistem, poraba moči

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1 Introduction

Real time digital signal processing applications often use data from acquisition devices, which are corrupted with noise. If in such applications area, power or processing speed are more important than accuracy, then faster, less-power and less-hardware consuming approximate solutions can be used. Multiplication and division are among the most used arithmetic operations in digital signal processing, neural networks and adaptive systems. A great number of repeated multiplications and divisions impose a significant power and time consumption. An approximation of these operations should not lead to considerable degradation of applications' performance; therefore the introduced error should be as low as permitted by an application.

The choice of the number system affects the power dissipation, since the number system has an effect on several levels of the design abstraction. In particular, the appropriate selection of the number system can reduce power dissipation, because it can reduce the number of the operations, the strength of the operators and the activity of the data.

This review paper is organized as follows: in the following subsections we give an overview of the switching power consumption in digital circuits and discuss how the choice of the number system can affect power dissipation. In Section 2 various methods for multiplication in LNS are presented. Section 3 gives an overview of the algorithms used in binary logarithmic and antilogarithmic approximations. A general logarithmic multiply/divide unit is also discussed. In section 4 we give an overview of the real world applications that benefit from the usage of the arithmetic in the logarithm number system. We conclude the paper in Section 5.

1.1 Power dissipation

Power dissipation is a prime design issue, mainly due to the growing need for portable electronic devices. Low-power design requires optimization at all levels of abstraction. Dynamic power consumption is due to charging and discharging of capacitance. The energy consumed for N clock cycles is

$$E_N = n(N) \cdot C \cdot V_{DD}^2 \tag{1}$$

where *n(N)* is the number of 0 to 1 transitions in *N* clock cycles, *C* is switching capacitance and V_{DD} is supply voltage. The switching power is given as energy per transition and can be expressed as:

$$P_{avg} = \lim_{N\to\infty} \frac{E_N}{N} \cdot f = \lim_{N\to\infty} \frac{n(N)}{N} \cdot f \cdot C \cdot V_{DD}^2 \tag{2}$$

Where *f* is the clock frequency. The term $\lim_{N\to\infty} \frac{n(N)}{N}$ represents the switching activity on a signal line, and is denoted as $\alpha_{0\to1}$:

$$\lim_{N\to\infty} \frac{n(N)}{N} = \alpha_{0\to1} \tag{3}$$

The switching power dissipation in a circuit is then given as:

$$P_{avg} = f \cdot C \cdot V^2 \cdot \alpha_{0\to1} \tag{4}$$

Three main principles of power reductions are:
- reduction of voltage,
- reduction of the switching activity, i.e. minimize spurious glitches, and
- reduction of the area complexity, i.e. reduce the switching capacitance.

Low-power design usually requires operation at lowest possible voltage and clock speed. Glitches are temporary changes in the value of the output and as such they represent unnecessary transitions. They are caused due to the skew in the input signals to a gate. Gate sizing and path balancing techniques like pipelining can reduce glitches.

In this paper we will focus on two techniques that affect all factors in power Eq. (4):
- the choice of the number system,
- optimization of arithmetic circuits.

1.2 Logarithmic number system

Stouraitis and Paliouras [1,2] studied the impact of the logarithmic number system on the power dissipation. They showed that, if the data distribution is uniform, the probability of the *i*-th bit transition from 0 to 1 (probability of the bit assertion) is constant in the fixed-point number representation, and is 0.25 for each bit in a word. On the other side they showed that the probabilities of bit assertion in LNS operands are not constant – they depend on the significance of a bit. The probability of bit assertion for the more significant bits is substantially lower than the probability of bit assertion for the less significant bits. This is due to the inherent data compression probability of the logarithm and this behavior leads to a reduction of the average switching activity in the entire word. The study [1] showed that the activity savings percentage can be more than 15%. Paliouras and Stouraitis report that approximately a two-times reduction in power dissipation is possible for operations with word size of 8 to 14 bits.

The logarithmic number system can simplify certain arithmetic operation and can reduce the strength of the operators. For example, the multiplication is reduced to the addition and the division is reduced to subtraction. In order tu use this benefit of the logarithm number system, a conversion circuitry is required to perform the conversion from the fixed-point number representation to LNS and vice-versa. The basic arithmetic operations and their counterparts are presented in Table 1.

Table 1: Basic arithmetic operations in the fixed-point number representation and their LNS counterparts.

Fixed-point operation	Logarithmic operation
A = B . C	$\log_2 A = \log_2 B + \log_2 C$
A = B / C	$\log_2 A = \log_2 B - \log_2 C$
$A = B^2$	$\log_2 A = (\log_2 B) << 2$

Paliouras and Stouraitis in [2] claim that LNS due to savings in signal activity and the reduction of the strength of the operators can be a successful candidate for the implementation of low-power arithmetic circuits.

2 Multiplication in LNS

Multiplication has always been a hardware-, time- and power consuming arithmetic operation, especially for large-value operands. This bottleneck is even more emphasized in digital signal processing (DSP) applications that involve a huge number of multiplications. In many real-time DSP applications, speed is the prime target and achieving this may be done at the expense of the accuracy of the arithmetic operations. Signal processing deals with signals distorted with the noise caused by non-ideal sensors, quantization processes, amplifiers, etc., as well as algorithms based on certain assumptions, so inaccurate results are inevitable. For example, a frequency leakage causes a false magnitude of the frequency bins in spectrum estimations. The signal-compression techniques incorporate quantization after a cosine or wavelet transform. When transform coefficients are quantized, instead of calculating high-precision coefficients and then truncating them, it is reasonable to spend less resources and produce less accurate results before the quantization. In many signal-processing algorithms, which include correlation computations, the exact value of the correlation does not matter; only the maximum of the correlation plays a role. Additional small errors introduced with multipliers, as mentioned in the application described and others, do not affect the results significantly and they can still be acceptable in practice.

Logarithmic multiplication introduces an operand conversion from integer number system into the logarithm number system. The multiplication of the two operands N1 and N2 is performed in three phases, calculating the operand logarithms, the addition of the operand logarithms and the calculation of the antilogarithm, which is equal to the multiple of the two original operands.

The main advantage of this method is the substitution of the multiplication with addition, after the conversion of the operands into logarithms. LNS multipliers can be generally divided into two categories, one based on methods that use lookup tables and interpolations, and the other based on Mitchell's algorithm (MA) [3], although there is a lookup-table approach in some of the MA-based methods [4]. Generally, MA-based methods suppressed lookup tables due to hardware-area savings. However, this simple idea has a significant weakness: logarithm and anti-logarithm cannot be calculated exactly, so there is a need to approximate the logarithm and the antilogarithm.

The binary representation of the number *N* can be written as:

$$N = 2^k \cdot \left(1 + \sum_{i=0}^{k-1} b_i \cdot 2^{i-k}\right) = 2^k \cdot (1+x) \tag{5}$$

where k is a characteristic number, i.e. the place of the leading-one bit, b_i is a bit value at the *i*-th position and *x* is the fraction. The logarithm with the basis 2 of the number *N* is:

$$\log_2 N = \log_2 (2^k \cdot (1+x)) = k + \log_2 (1+x) \tag{6}$$

The expression $\log_2(1+x)$ is usually approximated and the approximation affects the accuracy. Many methods for the logarithm and anti-logarithm approximation have been proposed in the past [3,4,5,6,7,8,9].

2.1 Mitchell's algorithm based multiplier

One of the oldest methods to approximate the multiplication and division in LNS is Mitchell's based logarithm computation [3] that approximates the logarithm with piecewise straight lines:

$$\log_2 N \approx k + x \tag{7}$$

The Mitchell's based approximation (MA) of the logarithm of the product is:

$$\log_2 (N_1 \cdot N_2) \approx k_1 + k_2 + x_1 + x_2 \tag{8}$$

Mitchell proposed the following approximation of the product:

$$(N_1 \cdot N_2)_{MA} \approx f(x) = \begin{cases} 2^{k_1+k_2} \cdot (1 + x_1 + x_2), & | \; x_1 + x_2 < 1 \\ 2^{k_1+k_2+1} \cdot (x_1 + x_2), & | \; x_1 + x_2 \geq 1 \end{cases} \tag{9}$$

The approximation of the product requires the comparison of the sum of mantissas, i.e. the product approximation depends on the carry bit from the sum of mantissas. The Mitchell's method computes the product using only shift and add operations. The architecture of the multiplier proposed in [11] is depicted in Figure 1.

The Mitchell's based multiplication produces a significant error. The relative error increases with the number of bits with the value of '1' in the mantissas. The maximum possible relative error for MA multiplication is around 11%, and the average error is around 3.8%. The Mitchell's multiplier consumes only 17% of the power consumed by a standard fixed-point multiplier.

Numerous attempts have been made to improve the MA's accuracy. Hall [10], for example, derived differ-

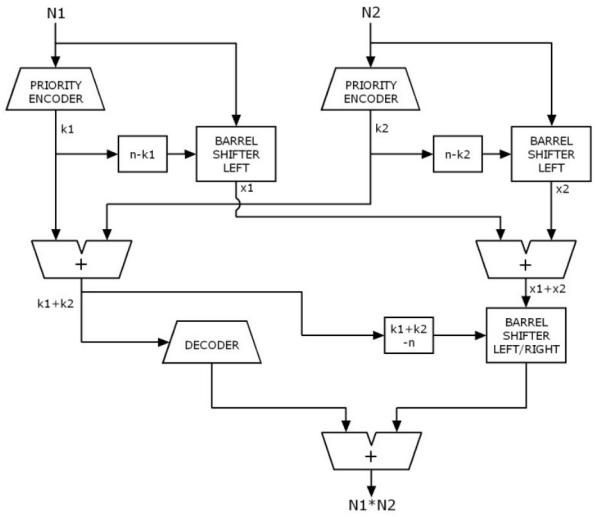

Figure 1: The architecture of the Mitchell's multiplier.

ent equations for error correction in the logarithm and antilogarithm approximation in four separate regions, depending on the mantissa value, reducing the average error to 2%, but increasing the complexity of the realization. Among the many methods that use look-up tables for error correction in the MA algorithm, McLaren's method [4], which uses a look-up table with 64 correction coefficients calculated in dependence of the mantissas values, can be selected as one that has satisfactory accuracy and complexity.

2.2 Operand decomposition in the Mitchell's algorithm

Mahalingam and Ranganathan [11,12] proposed a method based on operand decomposition for improving the accuracy of Mitchell's logarithmic multiplication. The operand decomposition is applied to the inputs as a preprocessing step to Mitchell's logarithmic multiplication in order to reduce the number of ones in the input operands. In this method the *n*-bits input operands *X* and *Y* are decomposed into *n*-bits operands:

$$A = X \vee Y$$
$$B = X \wedge Y$$
$$C = \overline{X} \wedge Y$$
$$D = X \wedge \overline{Y}$$

where $\vee$ and $\wedge$ denote bitwise OR and AND operations. The product is then calculated as

$$X \cdot Y = (A \cdot B) + (C \cdot D) \tag{10}$$

and the computation requires two Mitchell-based multipliers. The authors reported that the average relative error has been decreased to 2.1%, while the area is doubled in comparison to MA. It has been reported that operand decomposition based multiplier consumes only 30% of the power consumed by a standard fixed-point multiplier. The architecture of the operand decomposition based multiplier proposed in [11] is depicted in Figure 2.

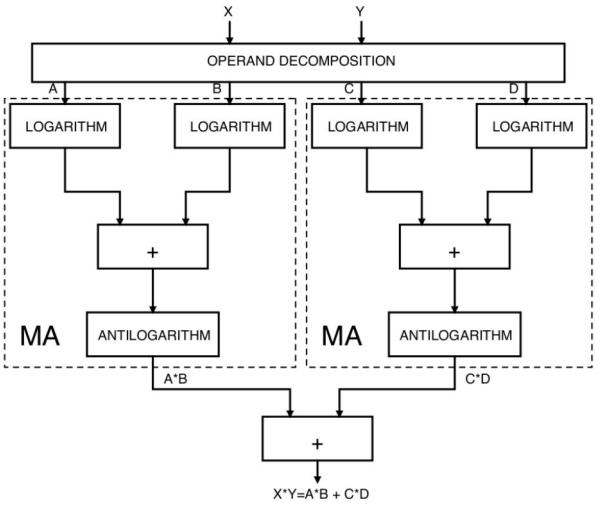

Figure 2: The architecture of the operand-decomposition based multiplier.

2.3 Babic's multiplier

Babic et al. [13,14] proposed a solution that simplifies logarithm approximation introduced by Mitchell in Eq. (9) and introduces an iterative algorithm with various possibilities for achieving the multiplication error as small as required and the possibility of achieving the exact result. By simplifying the logarithm approximation introduced in Eq. (9), the correction terms could be calculated almost immediately after the calculation of the approximate product has been started. In such a way, the high level of parallelism can be achieved by the principle of pipelining, thus reducing the complexity of the logic required by Eq. (9) and increasing the speed of the multiplier with error rectification circuits. From the binary representation of the numbers in Eq. (5), we can derive a correct expression for the multiplication:

$$N_1 \cdot N_2 = (2^{k_1} + (N_1 - 2^{k_1}) \cdot (2^{k_2} + (N_2 - 2^{k_2})) \tag{11}$$

$$N_1 \cdot N_2 = 2^{k_1} 2^{k_2} + 2^{k_2}(N_1 - 2^{k_1}) +$$
$$+ 2^{k_1}(N_2 - 2^{k_2}) + (N_1 - 2^{k_1})(N_1 - 2^{k_1}) \tag{12}$$

The last term $(N_1 - 2^{k_1})(N_1 - 2^{k_1})$ requires the multiplication, while all other terms can be calculated using

only shift and add operation. Babic et. al proposed the following approximation of the product:

$$N_1 \cdot N_2 \approx P_{approx} = 2^{k_1}2^{k_2} + 2^{k_2}(N_1 - 2^{k_1}) + 2^{k_1}(N_2 - 2^{k_2}) \quad (13)$$

Discarding the term $(N_1 - 2^{k_1})(N_1 - 2^{k_1})$ from Eq. (12) gives an approximate product $P_{approx'}$ which can be underestimated for at most 25%. The architecture of the Babic's multiplier is depicted in Figure 3.

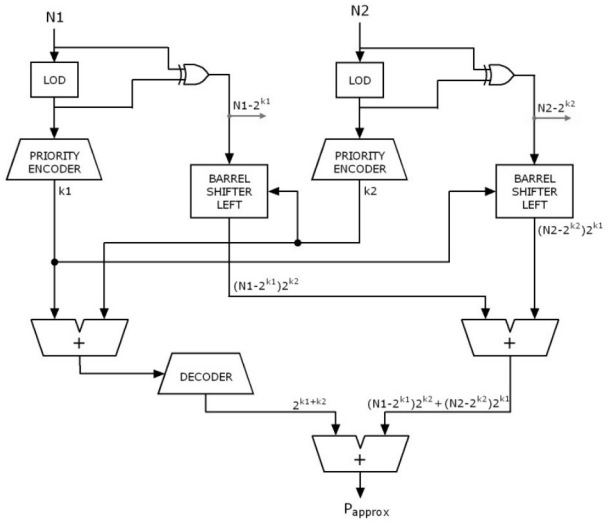

Figure 3: The architecture of the Babic's multiplier.

Babic et al. also proposed a simple scheme for error rectification. Instead of neglecting the term $(N_1 - 2^{k_1})(N_1 - 2^{k_1})$ in Eq. (12), we can calculate the product $(N_1 - 2^{k_1})(N_1 - 2^{k_1})$ in the same way as $P_{approx'}$ i.e. using Eq. (13). In such a way the error rectification can start immediately after removing the leading ones from the both input operands. By repeating the above procedure we can approximate the product to an arbitrary precision without using the exact multiplier. Babi´c et al. showed that in the worst case scenario the relative error decays exponentially with the rate 2^2 per pass. The average relative error with one error rectification has been decreased to 0.97%.

It has been reported in [13] that Babic's multiplier consumes only 30% of the power consumed by a standard fixed-point multiplier. Area used by Babic's multiplier is 93% of the area used by the operand decomposition based multiplier.

3 Logarithmic converters and division

To improve the error in logarithm and antilogarithm conversion in Mitchell's algorithm many efficient logarithm and antilogarithm converters have been proposed in literature [6] [7] [8] [9]. The logarithm of the binary number *N* is:

$$\log_2 N = k + \log_2(1 + x) \quad (14)$$

In order to calculate $\log_2 N$ we have to approximate the term $\log_2(1+x)$

3.1 Abed-Siferd logarithm and antilogarithm approximation

Abed and Siferd [6,7,15] proposed a low-power logarithmic converter where they further divided intervals for piecewise linear curve that is used to approximate the logarithm and anti-logarithm. They proposed a 2-region approximation of $\log_2(1+x)$ as follows:

$$\log_2(1+x) \approx \begin{cases} x + \frac{1}{4}x_{3MSB}, & x \in [0.0, 0.5] \\ x + \frac{1}{4}\bar{x}_{3MSB}, & x \in [0.5, 1.0] \end{cases} \quad (15)$$

Where $\bar{x}_{3MSB} = (1 - x_{3MSB} - 2^{-3})$ and x_{3MSB} represents the tree most significant bits in the mantissa x. The proposed correction equations use only the three most significant bits of the mantissa and all coefficients are restricted to powers of 2. The block diagram of the proposed logarithmic converter is depicted in Figure 4.

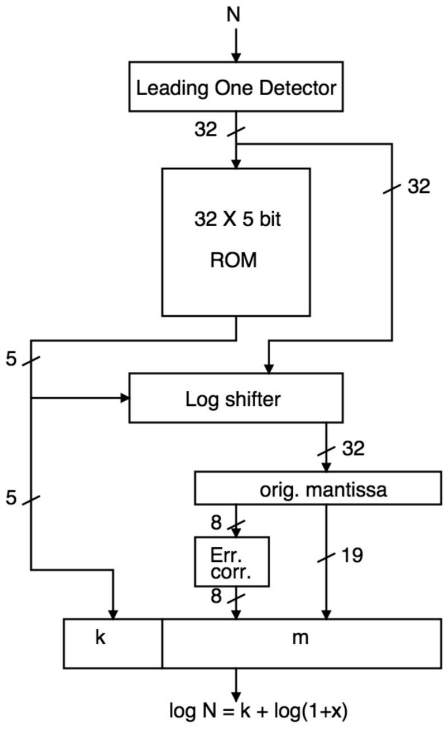

Figure 4: A block diagram of the Abed-Siferd low-power logarithmic converter [6].

Abed and Siferd also proposed a low-power antilogarithmic converter [7]. If the logarithm of the number *N* is $\log_2 N = k + \log_2(1+x) = k + m$ then the antilogaritm is

$$N = 2^k 2^m \tag{16}$$

To approximate 2^m Abed and Siferd proposed the following 2-region approximation:

$$2^m \approx f(x) = \begin{cases} m + \frac{3}{16}\bar{m}_{7MSB} + \frac{13}{16} + 2^{-10} + 2^{-11}, & m \in [0,0.5) \\ m + \frac{3}{16} m_{7MSB} + \frac{13}{16}, & m \in [0,0.5) \end{cases} \tag{17}$$

Where $\bar{m}_{7MSB} = (1 - m_{7MSB} - 2^{-7})$ and m_{7MSB} represents the seven most significant bits in the number *m*.

3.2 Multiplication and division using logarithmic converters

Multiplication and division are reduced to addition and subtraction after the input operands have been converted to logarithms. The conversion from LNS to the fixed-point notation is required after the addition or subtraction in LNS. The general architecture of a multiplier and/or divider using LNS is depicted in Figure 5.

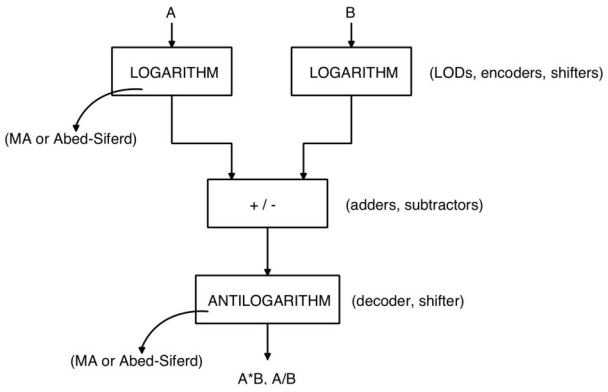

Figure 5: General architecture of a multiply/divide unit in LNS.

For logarithm and antilogarithm approximation we can use any of the methods proposed in [6] [7] [8] [9]. Using Abed-Siferd approximation, the relative error is reduced to 2.5% and the multiplier circuit uses only 40% of the area used by the array multiplier.

4 The appropriateness of LNS arithmetic in real-world applications

In this section we give an overview of the real world applications that benefit form the use of LNS arithmetic.

4.1 3-D graphics systems

In [16] a 32-bit fixed-point logarithmic arithmetic unit (LAU) is proposed for the possible application to mobile three-dimensional (3-D) graphics system. The proposed logarithmic arithmetic unit performs division, reciprocal, square-root, reciprocal-square-root and square operations. The unit is composed of two binary logarithmic converters, a calculation unit and a binary antilogarithmic converter. Instead of general 2-region piecewise-linear interpolation of the logarithm, the authors proposed a new 8-region piecewise-linear interpolation approximation algorithm, which is used in the proposed binary logarithmic converter block. Also, the piecewise interpolation method is used for the binary antilogarithmic converter.

The proposed LAU is implemented with 0.18 um CMOS technology and is verified in the 3-D graphics processing software environment before its chip is implemented. The test model consisted of 1700 polygons with lighting and texture mapping. The screen resolution was 512x512 and the texture size was 256x256. All 3-D graphics operations (vertex matrix transformation, vertex lighting, rendering, and texture mapping are performed by LAU.

The authors [16] claim that no noticeable difference was found by naked eyes between the two images. The small error range was within a tolerable range for the small screen size images of the mobile system. By using the LAU in fixed-point arithmetic, the performance is improved by five times compared with the complex radix-4 method. The power consumption of the LAU is 2.18 mW, while the power consumption of radix-4 unit is 4.29 mW, which is 1.97 times that of LAU's.

4.2 Motion vector

The authors in [13] considered the calculation of motion vectors using Babic's logarithmic multiplier. In video compression, a motion vector is used to represent a macro-block in a picture based on the position of this macro-block (or a similar one) in another picture, called the reference picture. For a block from observed frame (observed block), block-matching techniques try to find the best matching block in the reference frame. When the best matching is found, the displacement is

calculated and used as a motion vector, in applications like MPEG video compression.

In order to show the usability of the Babic's multiplier for motion-vector calculations, the described block-matching algorithm was applied on a selected region of the successive CT scan frames.

The results obtained with the Babic's multiplier with one error correction term are compared with the results of the regular multiplication. The mismatching percentage for the Babic's multiplier was between 3.17 and 3.9. These results prove that the percentage of mismatching is very low. Due to the heavy computational requirements, the block matching is often performed in two stages, a rough estimation of a moving vector and then an accurate refinement. In video compression, the errors in motion vectors will only slightly decrease the compression, but will speed up the compression algorithms and minimize power dissipation.

4.3 Multilayer perceptron with a highly parallel neural unit

Neural network processing comprises a huge number of multiplications. To gain as much as possible from the custom design, multiplications must be performed in parallel. However, multiplication circuits consume a lot of resources, time and power. Since the resources on a chip are limited, different strategies are applied to overcome the limitations. The first idea is to replace the floating-point arithmetic with fixed-point arithmetic. However, to further increase the performance the exact fixed-point matrix multipliers must be replaced with some approximate solutions. The hardware neural network presented in [17,18] is built around an iterative logarithmic multiplier, which can use many levels of correction circuits to iteratively approximate a product to the arbitrary precision. It also enables the pipelined design of correction circuits, which significantly reduce the propagation time of a signal through a circuit. The logarithmic multiplier with only one correction circuit is enough to reduce the multiplication error, on average, to less than 1%. In contrast to the majority of the proposed designs, where a special hardware unit is used for each neuron, the design presented in [17,18] contains only one highly parallel neural unit, which is capable of the fast parallel calculation of a neuron output. Since the same circuit can be used in forward and backward passes, it is more suitable for hardware neural network designs targeting small FPGA chips. The performance of the proposed hardware neural network with iterative logarithmic multipliers was compared to the usual software models and hardware neural network with exact matrix multipliers.
The neural-network models were tested on the PROBEN1 benchmark dataset, consisting of classification and approximation problems. Due to the highly adaptive nature of neural network models, which compensated the erroneous calculation, the replacement of the multipliers did not have any notable impact on the models' processing and learning accuracy. Furthermore, the consumption of fewer resources per multiplier also results in more power efficient circuits. The power consumption, which was reduced by roughly 20%, makes the hardware neural network models with logarithmic multipliers favorable candidates for battery-powered applications.

4.4 Adaptive Control Systems

The authors in [19] implemented the Kalman filter for object tracking using the logarithmic multipliers and reciprocal units. Object-tracking systems require a large number of complex arithmetic operations, which impose a significant power dissipation. Since adaptive algorithms can adjust to changes in the environment, they are also able to compensate for the computational errors, internally produced by the arithmetic units in LNS. The Kalman filter is able to iteratively update and estimate the underlying system state given a series of inaccurate and uncertain measurements. It can grasp the dynamics of a given system solely by observing its location over time. The Kalman filter equations comprise a large number of matrix multiplications and a matrix inverse.

To make these computations effective, the authors in [19] proposed two special purpose hardware units, a dot product unit and a multiply-and-divide unit. The dot product unit exploits the fact that any matrix multiplication can be decomposed to a series of independent dot products. Each dot product unit consists of four logarithmic multipliers and three adders. Four dot-product units are integrated the larger multiply-and-divide (MAD) unit that is capable of computing four dot products in parallel. The MAD unit also includes two logarithmic reciprocal units that serve in computation of the inverse.

The authors in [19] showed that the application of approximate arithmetic units importantly reduces power dissipation of the Kalman filter circuitry. The approximate units dissipate less power than the exact ones, but they usually need more clock cycles to get the result. Nevertheless, the implementations with logarithmic multipliers and reciprocal units are smaller and more energy efficient than the implementations with exact arithmetic. In such a way, the energy consumption per one iteration in the Kalman filter reduces to 70% - 80% of exact arithmetic. Moreover, the logarithmic arithmetic units reduce the critical path for up to 40%.

5 Conclusion

In this study we discuss the use of logarithmic number system to reduce the power in digital systems. The choice of LNS can lead to substantial savings in power dissipation, since LNS affects the signal activity and the strength of operators. The replacement of multipliers and dividers in adaptive systems will not have any notable impact on the systems' processing and learning accuracy. The same is true for signal processing systems, as signal processing deals with signals distorted with the noise caused by non-ideal sensors, quantization processes, amplifiers, etc., as well as algorithms based on certain assumptions, so inaccurate results are inevitable.

6 Acknowledgements [11]

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Tracking of MPP for three-level neutral-point-clamped qZ-source off-grid inverter in solar applications

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Abstract: This research work analyzes the most popular maximum power point tracking algorithms for an off-grid photovoltaic system based on three-level neutral-point-clamped quasi-z-source inverter topology to transfer the maximum power to the loads or storage systems. Classical methods, such as dP/dV feedback, perturb and observe method and incremental conductance, have been adapted for this novel topology and tested by simulation in SimPowerSystem from Matlab/Simulink. All of them use the shoot-through duty cycle as a control variable in dynamic conditions of irradiance to generate the reference shoot-through duty cycle in the modulation technique. In the studied case the power converter is feeding a pure resistive load in all the methods compared. Finally, the dP/dV method has been implemented in the control system of an experimental prototype and verified in a real photovoltaic system.

Keywords: Multi-level inverter, solar energy, pulse width modulation converters, neutral-point-clamped inverter, quasi-z-source inverter, shoot-through, maximum power point tracking, photovoltaic system

Sledenje točke največje moči s trinivojskim NPC quasi-Z-source neomrežnim razsmernikom v solarnih aplikacijah

Izvleček: Raziskava opisuje najbolj popularen algoritem sledenja točke največje moči za neomrežne fotonapetostne sisteme na osnovi trinivojskih NPC quasi-z-source topologij razsmernika za prenašanje največje moči v bremena ali shranjevalnike. Klasične metode, kot so dP/dV, motilno opazovalne metode in inkrementalna prevodnost, so bile prirejene za novo topologijo in preizkušene s simulacijskimi orodji SimPowerSystem in Matlab/Simulink. Za generiranje referenčnega kratkostičnega vklopnega razmerja v tehniki moduliranja vse metode za kontrolni parameter v dinamičnih razmerah sevanja uporabljajo kratkostično vklopno razmerje. V raziskavah je v vseh primerih razsmernik napajal čisto uporovno breme. Končno se je dP/dV metoda vgradila v kontrolni sistem prototipa in se preverila na realnem fotonapetostnem sistemu.

Ključne besede: večnivojski razsmernik, solarna energija, pretvornik s pulzno širinsko modulacijo, NPC, quasi-z-source razsmernik, slednje točke največje moči, fotonapetostni sistem

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1 Introduction

Today's power electrical system scenario differs essentially from the traditional configuration. Several factors such as increased electrical consumption, electricity market liberalization, the need to reduce pollution and CO_2 emissions and technological advancement are boosting the distributed generation (DG).

Photovoltaic solar energy is one of the most relevant distributed energy resources in this new scenario [1]. Due to increased use of this technology, several regu-

lations [2] have been established in order to manage the photovoltaic plant inverters. These regulations stipulate that the inverters are to provide support and stability during grid fault events and injected reactive power is necessary in order to restore the voltage at the point of common coupling (PCC), especially when voltage sag occurs.

This energy can output only DC voltage, therefore an inverter interface has to be used, which requires reduced cost and increased reliability inverter topologies. Among inverter topologies, the three-level neutral-point-clamped (3L-NPC) inverter has several advantages over the two-level voltage source inverter, such as lower semiconductor voltage stress, lower required blocking voltage capability, decreased dv/dt, better harmonic performance, soft switching possibilities without additional components, higher switching frequency due to lower switching losses, and balanced neutral-point voltage. As a drawback, it has two additional clamping diodes per phase-leg and more controlled semiconductor switches per branch. The 3L-NPC can normally perform only the voltage buck operation. In order to ensure voltage boost operation, an additional DC/DC boost converter should be used in the input stage [3]-[5]. It is necessary because in solar energy application, a wide range regulation capability of the input voltage is required due to its dependence on irradiance (W) and temperature (T).

To obtain buck and boost performance in a single stage, the focus is turned to a quasi-Z-source inverter (qZSI). The qZSI was introduced in [6] and it can buck and boost the DC-link voltage in a single stage without additional switches.

The qZSI can boost the input voltage by introducing a special shoot-through switching state, which is the simultaneous conduction (cross conduction) of both switches of the same phase leg of the inverter. In addition, the qZSI has a continuous mode input current (input current never drops to zero), which makes it especially suitable for renewable energy sources (e.g. fuel cells, solar energy, wind energy).

A new qZSI topology was proposed and described in [7]. It is a combination of the qZSI and the 3L-NPC inverter. The three-level neutral-point-clamped quasi-z-source inverter (3L-NPC qZSI) has advantages of both of these topologies.

Since the mentioned topology is rather new, in all previous studies the 3L-NPC qZSI was considered as an off-grid system [7]-[10]. To be connected to the electrical grid, a wide range of conditions should be considered (synchronization with the grid voltage, MPPT, anti-islanding methods, reactive power control, etc).

This paper discusses three MPPT algorithms (dP/dV feedback, perturb and observe method and incremental conductance) by simulation that can be used in this topology, using the shoot-through duty cycle as a control variable. In our experimental investigation one of the algorithms was verified in a real photovoltaic system.

2 System description

Fig.1 shows the photovoltaic conversion system each stage of which will be explained in this section.

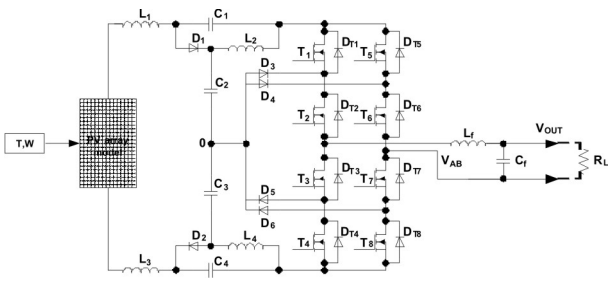


Figure1: Off-grid photovoltaic conversion system based on the 3L-NPC qZSI.

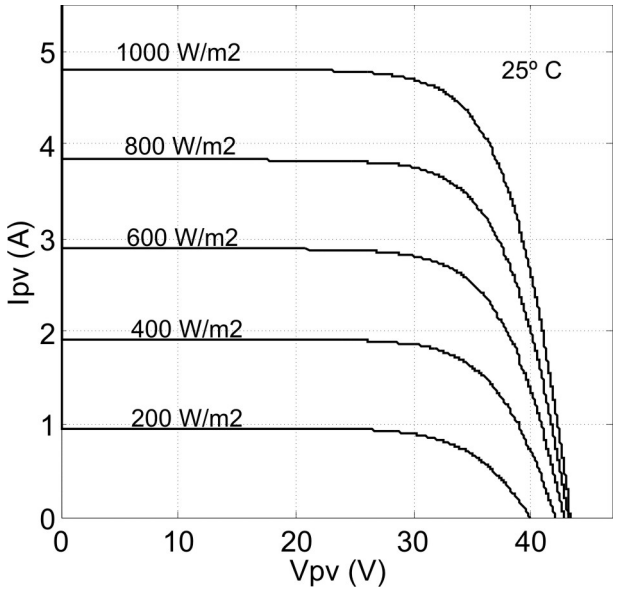
2.1 PV Array Model

Solar panels provide a limited voltage and current following an exponential I-V curve.

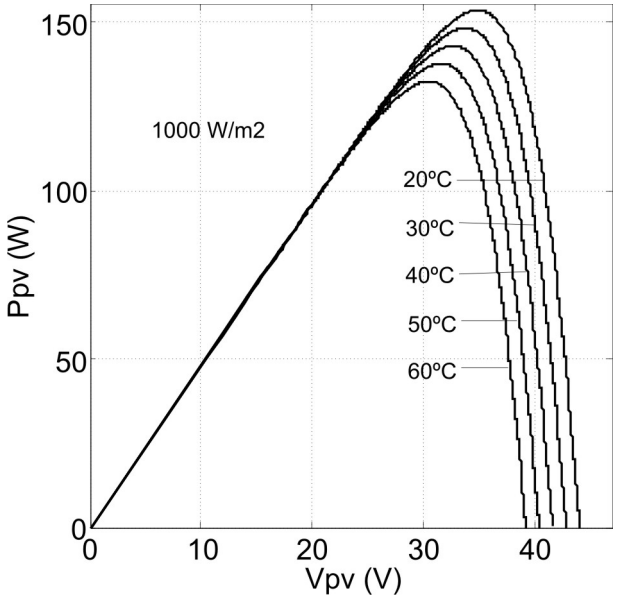
Several models have been proposed for solar panel simulation in the literature [11]-[15]. Most of them model the solar cell as an electrical equivalent circuit where such parameters as junction resistor between P-N unions, the contact resistor between cells and metal parts (R_s) and the resistor for shunt currents (R_{sh}) are needed. In [11-13], even the diode factor and the effective cell area are necessary. These parameters are not provided by the solar panel manufacturers in datasheets, which makes it difficult for engineers and users to apply these models.

Due to these reasons, a mathematical model based on I-V exponential curves and parameters provided by manufacturers in a datasheet was used to simulate the PV array. Mathematical foundation is detailed in [16]. By means of this model and the appropriate series-parallel association of modules, any PV array could be simulated. The family of I-V and P-V curves simulated in different conditions of temperature (T) and irradiance (W) for the case of solar panel Shell SP150-P [17] is shown

in Fig. 2 a) and b). The values of V_{oc}, I_{sc}, I_{MPP} and V_{MPP} were achieved with an error less than 1% in comparison with those provided by the manufacturer.



(a)



(b)

Figure 2: a) I-V family curves changing irradiance. B) P-V family curves changing temperature.

2.2 DC/AC Interface

DC/AC conversion is carried out by means of a single phase 3L-NPC qZSI [7]. This topology presents some particular features, such as continuous input current, higher switching frequency due to lower switching losses, balanced neutral-point voltage and high quality of the output voltage in comparison with traditional inverters providing benefits in PV conversion applications. One of the most important capabilities of the qZS family of inverters is the possibility of boosting the input voltage by means of shoot-through switching states. This boosting possibility avoids the use of a DC-DC boost converter between the PV array and the inverter to achieve the MPP operation and the control of the system. Passive elements of the qZ network have been calculated according to the method proposed in [9].

2.3 Output Filter and Load

An L-C filter has been chosen to minimize the THD of the output voltage. Filter values have been calculated according to the guidelines in [18]. It is based on current and voltage ripples among others criteria.

To analyze the transferred power from the PV array to the load, a pure resistive load is connected between the branches.

3 Modulation technique

A special sinusoidal pulse-width modulation (SPWM) technique was implemented in order to generate the switching signals of the power converter.

There are two kinds of switching signals to generate separately in ZS and qZS inverters. On the one hand, it is necessary to generate the normal switching signals (S_{Ti}) in order to track the reference signal. On the other hand, the shoot-though states must to be added carefully.

Some requirements must be satisfied when shoot-through states are generated, for instance, the average output voltage should remain unaffected and the shoot-through states have to be uniformly distributed during the whole output voltage period with constant width. These features result in several advantages, such as minimum ripple of the input current, minimum value of the passive elements, reduction of the THD of the output voltage, and gaining of the desired boost factor.

In this work the modulation technique proposed in [10] was used to achieve the aforementioned features. Fig. 3 shows the generation of the normal and shoot-through switching states with this modulation technique and Fig.4. depicts its implementation sketch.

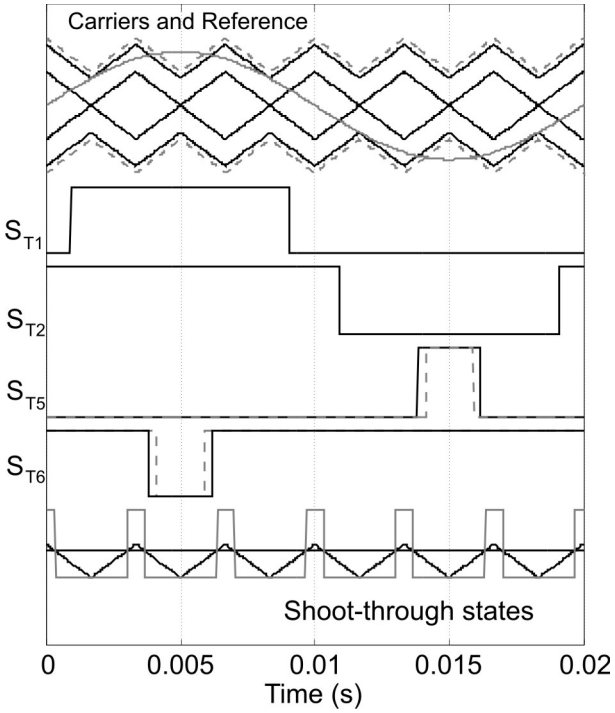


Figure 3: Simulation of the used shoot-through modulation technique.

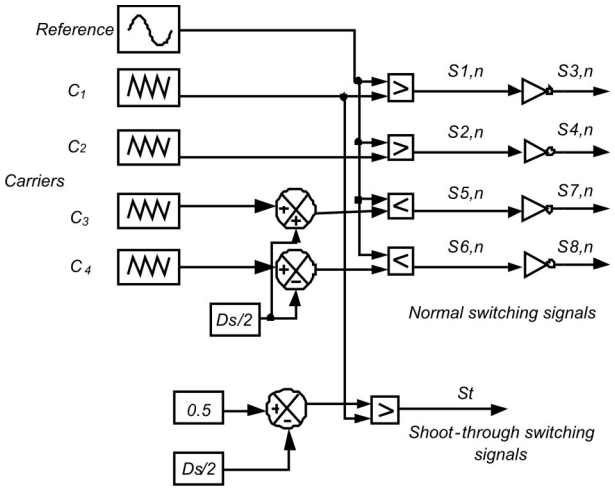


Figure 4: Sketch of the implementation of the modulation technique.

4 MPPT algorithms for 3l-npc qzsi

Tracking the maximum power point (MPP) of a PV array is necessary due to the high cost of solar panels and the dependence of power with W and T [19], being an essential task of PV inverters. In this way, many maximum power point tracker (MPPT) algorithms have been proposed in the literature [20]. Those methods vary in complexity of implementation, sensors required, convergence speed, cost, range of effectiveness and hardware implementation among others [20].

Three most traditional MPPT algorithms are highlighted due to their capabilities: perturb and observe (P&O), incremental conductance (InC) and the method based on DP/dV or dP/dI feedback.

Explained in this section, these MPPT methods have been adapted for the 3L-NPC qZSI topology. All of them work using the shoot-through duty cycle (D_s) as a control variable to track the MPP in dynamic irradiance conditions as well.

Fig. 5 shows the block diagram of the photovoltaic conversion system to be controlled in which the MPPT algorithms have been implemented.

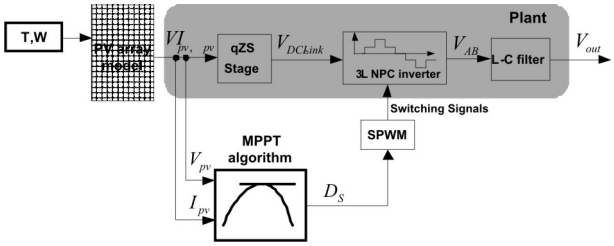


Figure 5: Block diagram of the studied photovoltaic conversion system.

4.1 Method Based on dP/dV Feedback

One way to achieve the MPP operation is to calculate the slope (dP/dV) [21]-[25] of the PV array power curve and feed it back to the converter with any control method to drive such slope to zero.

Depending on the topology and the mode of working of the converter, the slope can be computed in different ways. In our case, a PI controller that adjusts the D_s of the shoot-through modulation technique explained in section III is used to drive the slope to zero. The PI controller was tuned manually, looking for a slow response without error in steady state. This fact is considered to emulate the inertia and the response times of the electrical grid (synchronous machines and conventional power plants) to avoid instabilities and transient non-desired effects [26] when the converter is connected to the grid. Fig. 6 shows the implementation scheme of the MPPT algorithm based on dP/dV feedback for the 3L-NPC qZSI using the D_s as a control variable.

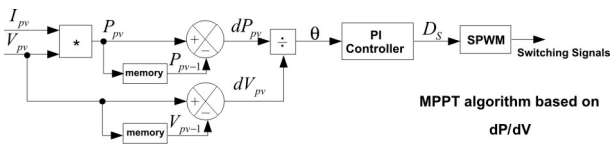


Figure 6: Implementation scheme of dP/dV feedback method.

4.2 Perturb and Observe Method (P&O)

This method [27]-[29] has been used by many researchers in different ways but the idea remains the same. A perturbation in the voltage of the PV array is perturbing the PV array current, resulting in the modification of the PV array power. By means of the increment of the PV voltage when the operation is on the left of the MPP, the PV power is increased and the PV power is decreased if the operation is on the right of the MPP. The same reasoning is possible when the PV voltage is decreased. If one perturbation in one direction produces the increment of the PV power, the next perturbation should be in the same direction and if it is not the case, the perturbation has to be reverse. Table I summarizes the process.

To produce the perturbation in the voltage of the PV array of our case where the DC/AC is converted by a 3L-NPC qZSI, perturbations in the D_s are inserted. The value of this perturbation is equal to 0.005. By means of this process the MPP is reached and the system oscillates around the MPP, as shown in Fig. 7 (points A and B). Fig. 8 depicts a sketch of the implementation of this method.

Table 1: Summary of MPPT Algorithm Based on P&O

Perturbation	Change in Power	Next Perturbation
Positive	Positive	Positive
Positive	Negative	Negative
Negative	Positive	Negative
Negative	Negative	Positive

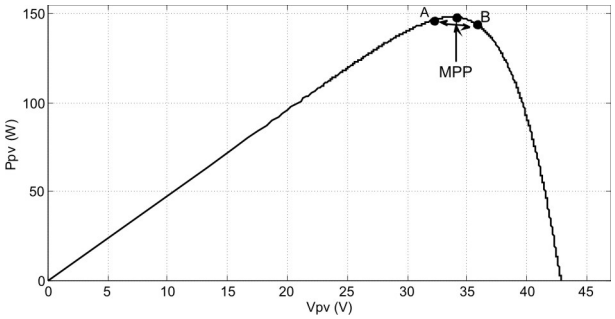


Figure 7: Power operation with the P&O MPPT method.

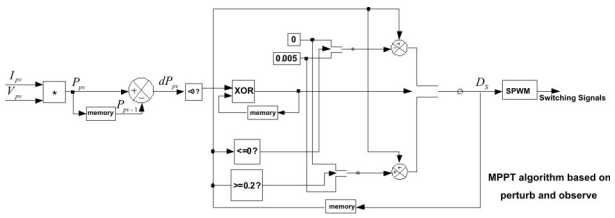


Figure 8: Implementation scheme of the P&O method.

4.3 Incremental Conductance (IncCond)

This method [30]-[31] analyzes the slope of the PV array power curve. This slope is zero at the MPP, positive on the left of the MPP and negative on the right. Thus:

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\frac{dI}{dV} \cong I + V\frac{\Delta I}{\Delta V} \quad (1)$$

and as a consequence, the incremental conductance ΔI/ΔV is equal, greater than or less than –I/V at the MPP, on the left of the MPP and on the right of the MPP, respectively. The MPP can be tracked by comparing the instantaneous conductance (I/V) with the incremental conductance (ΔI/ΔV) as the flowchart in Fig. 9 shows. In our case by changing D_s, the voltage V_{pv} where the PV array is forced to operate is changed, trying to find the MPP (ΔI/ΔV= –I/V).

The size of the incremental step (changes inserted in D_s) determines the convergence (velocity and accuracy) of this MPP tracking method. Using larger increments in the control variable, the system will be faster but it will not operate close to the MPP. The step size was designed taking into account the same criteria as the tuning of the PI controller in the method based on dP/DV feedback.

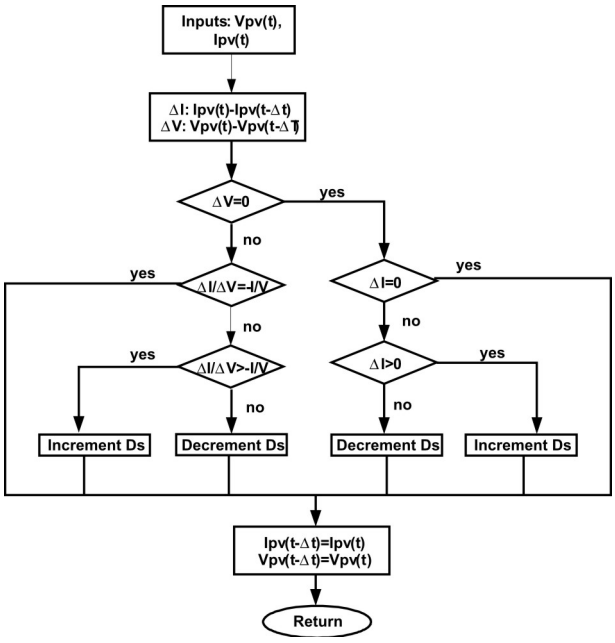


Figure 9: Incremental conductance flowchart.

5 Simulation results

In order to verify the explained MPPT algorithms, a comprehensive simulation study was performed in SimPowerSystems of Matlab/Simulink. Parameters of

the simulation are described in Table II. To analyze the transferred power to the load and the effectiveness of each MPPT method, a smooth step (Fig. 10. a) in the irradiance from 1000 W/m2 to 900 W/m2 (Fig. 10. b)) in second eight up to sixteen was made while the temperature was maintained constant (25 ºC). This action emulates the shadows phenomena. Fig. 11 shows the evolution of the transferred power from the PV array to the load and the evolution of the control variable (D_s) in dynamic conditions by using each MPPT algorithm.

Table 2: Simulation parameters.

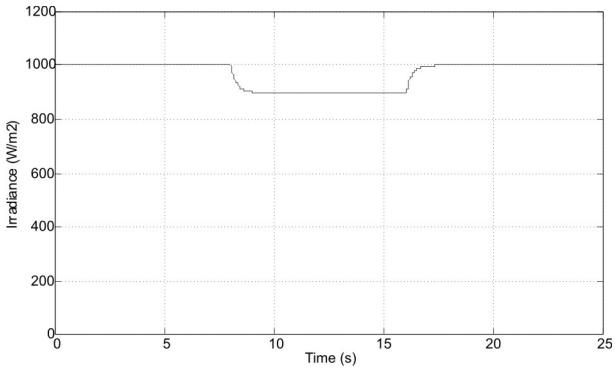
Group	Parameter	Description and unit	Value
PV Array	V_{oc}	Open circuit voltage (V)	43.4
	I_{sc}	Short circuit current (A)	4.8
	I_{MPP}	Maximum power point current (A)	4.4
	V_{MPP}	Maximum power point voltage (V)	34
	N_S	Series connected panel	7
	N_p	Parallel connected panel	1
Passive Elements	Inductors L_1,L_3	(mH)	2.55
	Inductors L_2,L_4	(mH)	0.255
	Capacitor C_1,C_4	(mF)	4
	Capacitor C_2,C_3	(mF)	1.3
	R_{load}	(Ω)	60
	C_{filter}	(μF)	0.47
	L_{filter}	(mH)	4.4
dP/dV	K_p	Proportional constant of PI controller	0.001
	K_i	Integral constant of PI controller	0.01
P&O		Perturbation size in D_s	0.005
Inc Cond		Perturbation size in D_s	0.005

5.1 Method Based on dP/dV Feedback

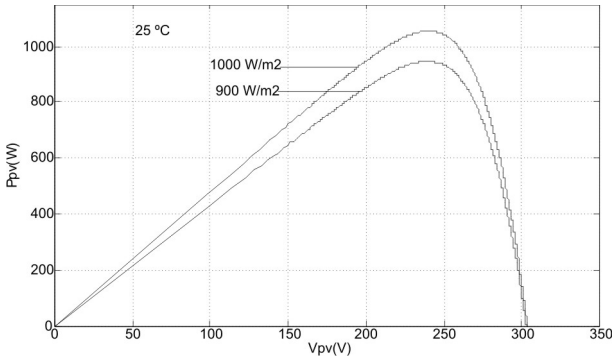
Figs. 11 (a) and 11 (b) show the evolution of the transferred power to the load and the evolution of the D_s when the MPPT algorithm based on *dP/dV* feedback is working. We can see how the system works in the MPP in each level of irradiance at high accuracy by means of the adjustment of the D_s. It is important to pay attention to some singularities (second sixteen) that could appear when any of the denominators (dV) are equal to zero during the iterative process. The algorithm must be protected against this cause of instability.

5.2 P&O

Figs. 11 (c) and 11 (d) show the evolution of the output power and the D_s in the case of the P&O method. The



(a)



(b)

Figure 10: a) Smooth step applied in the solar system. b) P-V array curves in each level of irradiance during the step.

system again tracks the MPP with accuracy. In this case the system is working around the MPP.

5.3 IncCond

In Figs. 11 (e) and 11 (f) the same variables are shown for the third presented MPPT algorithm. The MPP is also achieved in each level of irradiance using this method.

6 Analytical comparison

In order to compare the exposed MPPT algorithms for a 3L-NPC qZSI, each algorithm is analyzed in this section.

According to the number of required sensors, all of them need the measure of voltage and current of the PV system to track the MPP. There are other traditional algorithms, such as the MPPT algorithm based on the fractional control of V_{oc} and I_{sc} or the method based on the DC link capacitor drop control that only requires the measure of one variable.

In terms of the complexity of the implementation of the analyzed methods, perturbation and observation and incremental conductance are of low complexity level because they are based on simple mathematical

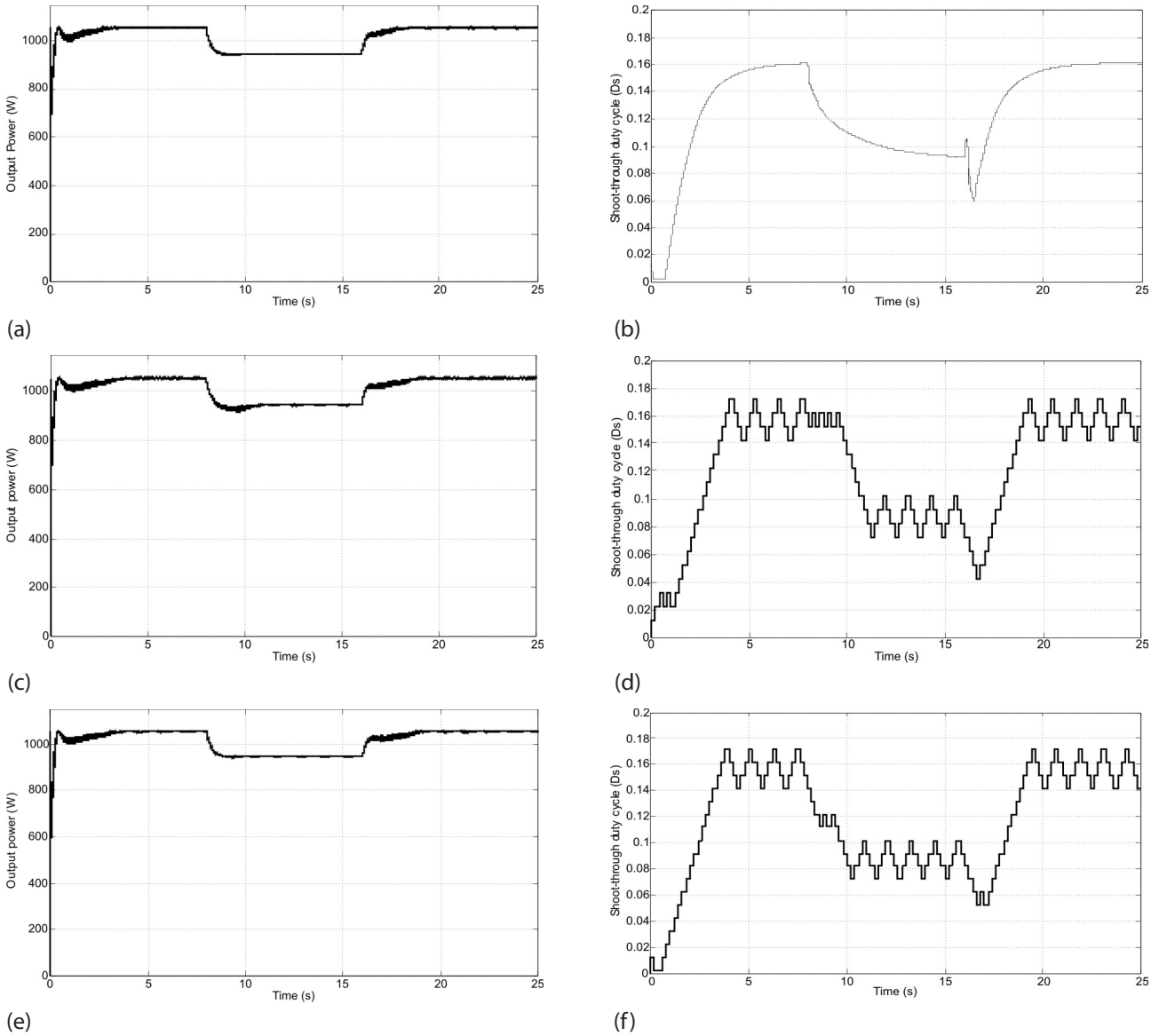


Figure 11: Evolution of transferred power and the evolution of Ds during a step in irradiance in each MPPT algorithm analyzed.

calculations. The MPP tracking algorithm based on dP/dV feedback is more complex due to the necessity to tune a PI controller and the calculation of a division of derivates in which it is necessary to prevent possible denominators equal to zero.

Another interesting feature is that the three algorithms can be implemented in digital or analogical technologies.

The speed of convergence of each method is quite different. On the one hand, methods based on perturbation and observation and incremental conductance present a variable speed that depends on the size of the step. A larger step produces faster convergence but at the same time, lower accuracy is achieved because the oscillation around the MPP will be larger. On the other hand, the MPPT algorithm based on dP/dV feedback, in general, has fast convergence. This speed depends on the parameters of the PI controller. In our case, every method has been implemented to find a slow response without error in steady state. This fact is considered to emulate the inertia and the response times of the electrical grid (synchronous machines and conventional power plants) to avoid instabilities and transient non-desired effects when the converter is connected to the grid and some changes in the irradiance or temperature occur. Also, the designed D_s gap of each method has been chosen between 0 and 0.2. Maximum power per used panel is 149.6 W when irradiance and temperature are 1000 W/m^2 and 25 ºC. After the step when irradiance decreases to 900 W/m^2, the maximum power is 135.17 W per panel. In the studied case where there are seven panels connected in series,

the array maximum power is 1054 W and 946.2 W in each situation. Using any of the studied methods, such values were achieved with accuracy.

7 Experimental results

In this section the experimental tests are explained. The chosen MPPT algorithm to be implemented in the experimental prototype is based on the adapted P&O using D_s as a control variable to introduce the perturbation in the system to reach the MPP. It is due to several reasons: it has a simple structure which allows an easy implementation: only two sensors are needed (to measure I_{pv} and V_{pv}), it can be used for digital or analog systems and it is not necessary to adjust any control system as a PI controller among others.

The converter built is described below. Table III shows the parameters of the experimental prototype of the 3L-NPC qZS inverter, with values of passive elements and also the type of semiconductors indicated. Passive elements were calculated according to [9] and [18], as in simulation studies. Fig. 12 shows the full system.

The control system is implemented in a low cost FPGA Cyclone IV family from Altera company [8]. Flexibility is the main advantage of this option, which allows realizing the shoot-through modulation technique with digital signal processing at high sample frequency. The measurement board is composed of the required current and voltage sensors.

Table 3: System parameters of the experimental prototype.

ELEMENT	VALUE OR MODEL
Control Unit (FPGA)	Cyclone IV EP4CE15E22C8
Driver Chip	ACPL-H312
Power switches	FCH47N60NF
qZS and clamp diodes	CREE C3D20060D
Input DC voltage U_N	220-450 V
Nominal Output AC voltage U_{OUT}	230 V
Capacitance value of the capacitors C_1, C_4	4000 µF
Capacitance value of the capacitors C_2, C_3	1000 µF
Inductance value of the inductors L_1 ... L_4	145 µH
Inductance of the inverter filter inductor L_i	560 µH
Inductance of the grid filter inductor L_{gi}	200 µH
Capacitance of the filter capacitor C_f	0.47 µF
Switching frequency	100 kHz

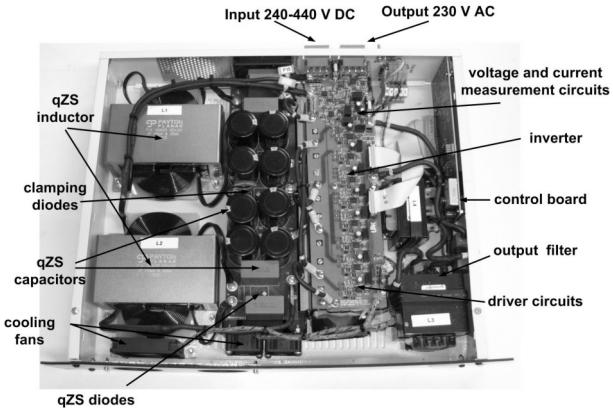


Figure 12: 3L-NPC qZS experimental prototype.

The experimental tests were carried out with a solar array composed of 14 modules LDK 185 D-24 (s), the principal parameters of which in standard conditions of W and T are shown in Table IV. Two strings of 7 serial panels were connected in parallel (2x7 configuration) to obtain a proper input voltage range. The output power is transferred to a pure resistive load.

Table 4: Parameters of module LDK 185 D-24 (s).

Parameters	Value at standard conditions (1000 W/m² and 25 °C
Nominal output power (Pmax)	185 W
Voltage at Pmax (Vmpp)	36.9 V
Current at Pmax (Impp)	5.02 A
Open circuit voltage (Voc)	45.1 V
Shot circuit current (Isc)	5.48 A

Fig. 13 shows the obtained results after reaching the maximum power point operation: the output current, output voltage, input PV voltage and input PV current.

Output magnitudes have a high level of quality. Measured total harmonic distortion (THD) with YOKOGAWA DL850 V equipment is 1.5 %. Input PV voltage presents a low frequency ripple at 100 Hz. It is typical of single phase systems. Input PV current presents this low frequency ripple and also ripple at high frequencies due to the switching frequency.

The transferred output power to the load is 1945 W, corresponding to the solar array maximum power at real conditions.

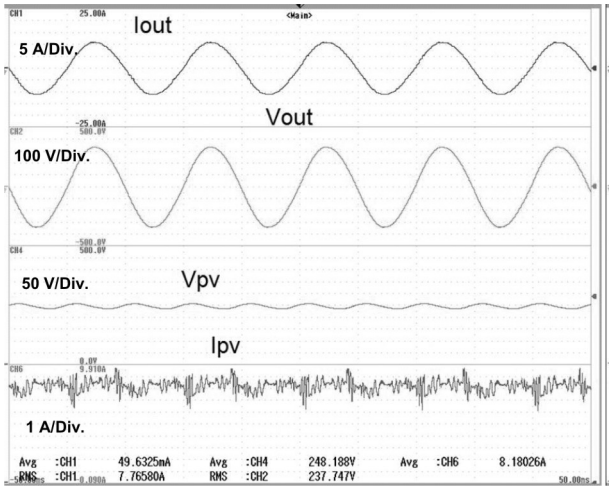


Figure 13: Experimental results at the maximum power point operation. From top to bottom: output current, output voltage, input PV voltage and input PV current.

8 Conclusion

Three traditional maximum power point tracking algorithms (methods based on dP/dV feedback, perturb and observe and incremental conductance) have been compared by means of simulation using SimPowerSystem of Matlab/Simulink. Each method has been adapted for a 3L-NPC qZSI using the shoot-through duty cycle as control variable to reach the MPP operation. Theoretical fundamentals and simulation results have been presented and discussed according to different criteria in order to choose the best solution for a real system. The P&O method, as the best solution, was chosen and implemented in the prototype and validated in a real solar plant.

9 Acknowledgment

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A linear current-controlled floating negative resistor

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Abstract: In this article, a low voltage CMOS current controlled floating negative resistor which is convenient for integrated circuit implementation is designed by using a self-cascode composite transistor. The proposed circuit only required ± 0.75 V as a power supply has a simple circuit structure and a low power consumption of which value is only 65 µW. The basic advantages of this circuit are a wide tuning range of the resistance value, an acceptable frequency performance and a wide dynamic range. The performances of the proposed circuit are simulated with SPICE to confirm the presented theory.

Keywords: Negative resistance, CMOS active resistor, current-controlled circuits, Current-mode, Integrated circuits

Linearen tokovno kontroliran plavajoči negativni upor

Izvleček: V članku je predstavljen nizko napetostni CMOS tokovno kontrolirani negativen upor, ki je uporaben v integriranih vezjih. Upor uporablja samo kaskaden kompozitni tranzistor. Predlagano vezje z napajalno napetostjo ± 0.75 V izkazuje nizko porabo okoli 65 µW. Glavne prednosti vezja so široko uporovno območje, sprejemljive frekvenčne lastnosti in široka dinamično območje. Teoretični rezultati so preverjeni s pomočjo SPICE simulacij.

Ključne besede: negativna uporost, CMOS aktiven upor, tokovno kontrolirano vezje, tokovni način, integrirana vezja

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1 Introduction

In recent years, the disposition of the analog circuit design with low-voltage operation capability has been raised owing to the fact that it is aimed to consume as little power as possible. The low power dissipation is an important factor for the weight and life of a battery. Thus, the design techniques and device technology for low-voltage low-power operation of the analogue circuits are required [1].

Large areas of the chip are required to obtain resistors which can be implemented by using diffusion areas in an integrated circuit. Also, these resistors cannot be easily adjusted to demanded values. To overcome these drawbacks, MOS and bipolar based active resistors topology have been reported in the previous studies [2-5].

Bipolar-based floating resistor was presented in the literature [4, 6]. Though these resistors have a good frequency performance, they have not only narrow dynamic range but also consume more power than the MOS-based active resistors. But at the same time, MOS resistors are limited with regard to frequency response and electronically tunability.

The voltage-controlled resistors have been used as an application in the analog circuit design area [7, 8]. The tunable resistance value of these circuits has been restricted by supply voltage. However, they have a wide dynamic range. The current-controlled resistors can be independently tuned over a wide range by biasing current. Also, they have a good frequency performance. Recently, active resistors have been used as not only positive but also negative resistor in some applications. Active positive/negative resistors have been used in a lot of implementations such as oscillators, amplifiers and filters [4, 9, 10,11].

In this paper, a linear current-controlled negative resistor based on self-cascode composite transistor has been introduced. The proposed circuit offers the advantages of a good linearity, a high dynamic range

and low power consumption. This circuit only operates at low voltage as ± 0.75 V. Until now, it has not been shown that low-voltage negative resistor structures are designed in somewhere else. The main contribution of this design to the literature leads to use the low voltage and low power applications. Having a simple structure, the resistance value of the resistor is obtained as the positive and negative.

2 Floating negative resistor

Self-cascode composite transistor structure is shown in Fig. 1. In practical cases, for optimal operation the W/L ratio of the M_A should be larger than the W/L ratio of the M_B, that is, a > 1. Moreover, the transistor M_B must be in triode region. Depending on the drain voltage, transistor M_A can work in saturation region or triode region. The aspect ratio (W/L) of the equivalent MOS transistor shown in Fig. 1 is decreased. This circuit structure takes an advantage in terms of linearity, dynamic range and electronically controllable resistance range.

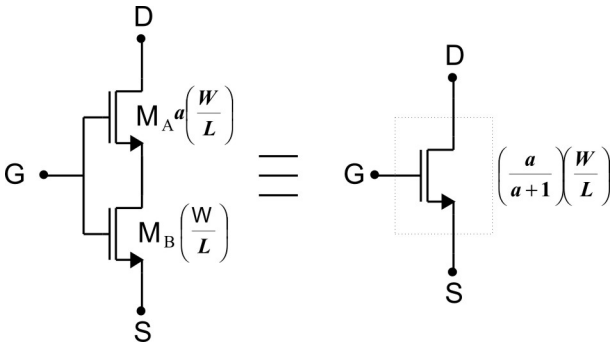

Figure 1: The self-cascode composite transistor.

Fig. 2 indicates the proposed linear current-controlled floating negative resistor.

The drain currents of transistors M_1 and M_4 can be written as,

$$I_{D1} = \frac{1}{2}k_n\left(\frac{a}{a+1}\right)\left(\frac{W}{L}\right)\left(V_1 - V_{S5} - V_{TH}\right)^2 . \quad (1)$$

$$I_{D4} = \frac{1}{2}k_n\left(\frac{a}{a+1}\right)\left(\frac{W}{L}\right)\left(V_2 - V_{S8} - V_{TH}\right)^2 . \quad (2)$$

I_{D1} and I_{D4} are the drain currents of transistors M_1 and M_4, respectively. In addition, V_{S5} and V_{S8} are the source voltages of transistors M_5 and M_8, respectively. From Eqs. (1) and (2), the relationship between V_1 and V_2 shown in Fig. 2 can be expressed as

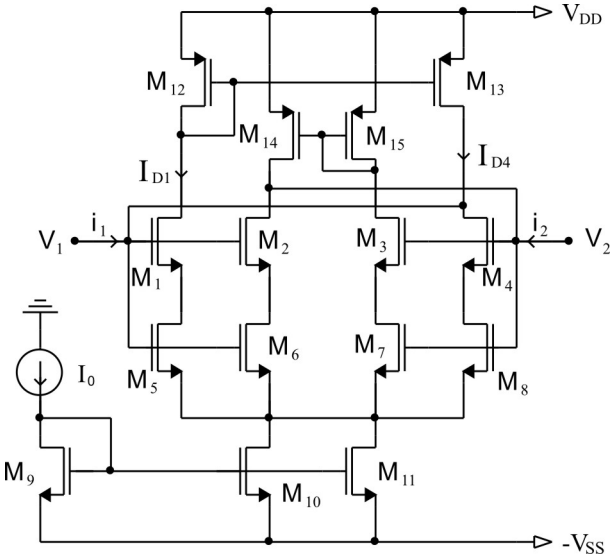

Figure 2: The current-controlled floating negative resistor.

$$V_1 - V_2 = \sqrt{\frac{I_0 - i_1}{k_n\left(\frac{a}{a+1}\right)\left(\frac{W}{L}\right)}} - \sqrt{\frac{I_0 + i_1}{k_n\left(\frac{a}{a+1}\right)\left(\frac{W}{L}\right)}} . \quad (3)$$

Current i_1 shown in Fig. 2 is given as:

$$i_1 \cong -\left(V_1 - V_2\right)\left[\frac{1}{2}k_n\left(\frac{a}{a+1}\right)\frac{W}{L}\right]^{1/2} \times$$

$$\times\left[2I_0 - \frac{1}{2}k_n\left(\frac{a}{a+1}\right)\frac{W}{L}\left(V_1 - V_2\right)^2\right]^{1/2} . \quad (4)$$

where $k_n = \mu_n C_{ox}$ is the transconductance parameter of the NMOS transistor. μn is the electron mobility and *Cox* is the oxide capacitance per unit area. I_0 is the biasing current. For a very small difference voltage which gives $2I_0 >> (1/2)k_n(a/a+1)(W/L)(V_1-V_2)^2$, the current i_1 exhibits a quite linear behavior. As shown in Eq. (4), linearity of the resistance highly depends on the aspect ratio (W/L) of the equivalent self-cascode composite MOS transistors and the difference voltage. Therefore, i_1 can be further reduced to:

$$i_1 \cong -\left(V_1 - V_2\right)\left[k_n\left(\frac{a}{a+1}\right)\frac{W}{L}I_0\right]^{1/2} . \quad (5)$$

In this instance, it is clear that $i_2 = -i_1$. The resistance of the proposed circuit can be written as

$$R_{12} \cong -\left[k_n\left(\frac{a}{a+1}\right)\frac{W}{L}I_0\right]^{-1/2} . \quad (6)$$

The resistance value can be easily controlled by biasing current as shown in Eq. (6). The proposed negative resistor shown in Fig. 2 can be easily converted to the positive resistor. A connection is made between the gates of transistor M_1, M_2 and drain of M_2 instead of M_4's drain. Additively, the gates of M_3 and M_4 are connected to the drain of M_4 instead of M_2's drain. In this case, it is clear that $i_1 = -i_2$. So, the definition of the positive resistance may be as follow:

$$R_{12} \cong \left[k_n \left(\frac{a}{a+1} \right) \frac{W}{L} I_0 \right]^{-1/2} . \quad (7)$$

The positive resistance of the resistor is able to be easily tuned by biasing current, too. Also, building two different kinds of in a single circuit is one of the important features of the proposed circuit. These features take essential advantages for the analog circuit applications.

For operating at low-voltage, this circuit requires to ensure the below-mentioned condition.

$$V_{DD} - \left(-V_{SS} \right) \geq V_{THP} + 4V_{DSsat} . \quad (8)$$

where V_{DD} and $-V_{SS}$ are the supply voltages of the circuit. V_{THP} is the threshold voltage of the PMOS and V_{DSsat} is the drain-source saturation voltage of the transistors. The value of the V_{THP} is approximately 0.4 V for 0.13 µm technology [12]. The lower drain currents have values, the more drain-source saturation voltage is reduced. Thus, the proposed circuit can be operated at low-voltage. Additionally, the estimation of the proposed circuit's dynamic-range is calculated as

$$\left| V_1 - V_2 \right| \leq \left[\left(\frac{a+1}{a} \right) \left(\frac{I_0}{\frac{1}{2} k_n \frac{W}{L}} \right) \right]^{1/2} . \quad (9)$$

The dynamic range highly depends on the biasing current as shown in Eq. (9). Thus, the dynamic range will be expanded for the high values of the biasing current.

3 Simulation results

The proposed linear current-controlled floating negative resistor was simulated by SPICE owing to approve the theoretical approaches. The SPICE model 0.13 µm CMOS parameter for the transistors are used in [12]. The supply voltage is ± 0.75 V and the aspect ratio of the transistors is presented in the Table I.

Table 1: Aspect ratio of the transistors.

Transistor	$M_1 - M_4$	$M_5 - M_8$	$M_9 - M_{15}$
W/L	5/1	1/2	30/0.26

I / V characteristics of the proposed resistor are shown in Fig. 3.

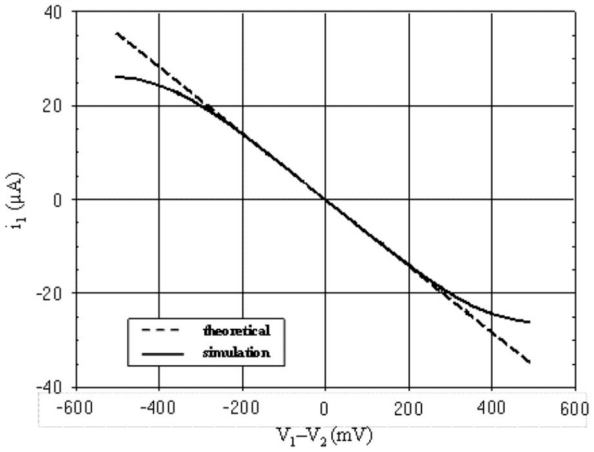

Figure 3: I / V characteristics of the proposed resistor.

Both theoretical and simulation results of the proposed resistor have been given in Fig. 3. It is shown that behaviour of the proposed resistor is highly linear from -250 mV to +250 mV. Fig. 4 shows the input voltage versus the input current of the simulated resistor.

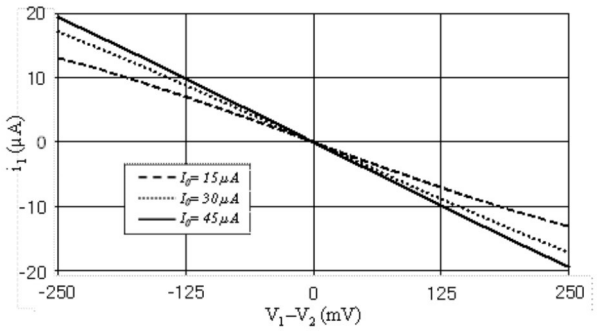

Figure 4: I / V characteristics for the different biasing current.

The biasing current of the resistor is varied from 15 µA to 45 µA step by step. The resistance value of the resistor can be easily adjusted by biasing current I_0 as shown in Fig. 4. The frequency response of the proposed resistor is illustrated in Fig. 5.

When the frequencies are increased, it is found that the proposed resistor can be operated with the –3dB bandwidth of about 148.3 MHz, 195.4 MHz and 222.1 MHz for 15 µA, 30 µA and 45 µA of the biasing current, respectively. Taking into consideration these results,

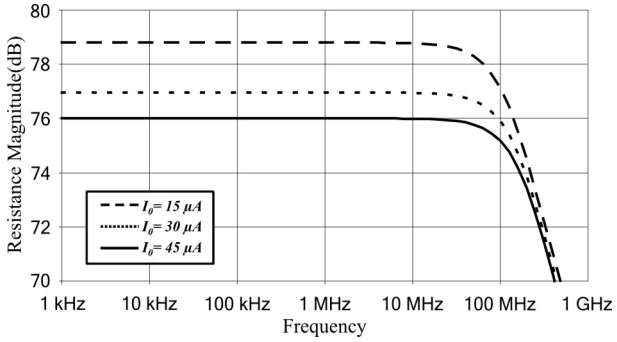

Figure 5: The frequency response of the proposed resistor.

the proposed circuit exhibits a good frequency performance.

The variation of the total harmonic distortion with peak to peak input voltage for I_0 = 15 μA and R_{12} = 8.7 kΩ is displayed in Fig. 6.

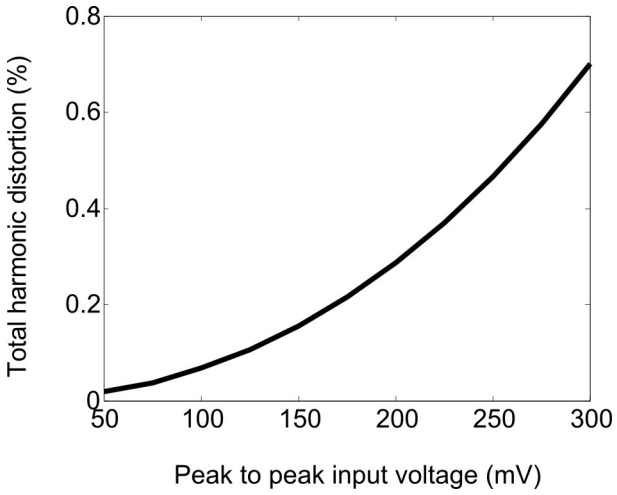

Figure 6: THD % versus input voltage.

The variation of the THD with input signal amplitude for a biasing current of 15 μA as shown in Fig. 6 is illustrated. We can evidently see that the THD value is 0.465 % at 250 mV_{p-p}. It is depicted that the THD values obtained according to different peak to peak input voltages are acceptable values. Also, the total power consumption of the proposed circuit is obtained as low value as 65 μW. The resistance of the proposed circuit has been calculated as both theoretical and simulation. The negative resistance of the proposed resistor for different bias currents is shown in Fig. 7.

The negative resistance is able to be tuned from 5.9 kΩ to 243 kΩ when the biasing current is adjusted between 0.1 μA and 60 μA. Note that, this circuit has a wide range negative resistance (R_{12}).

Noise is a main contributor to the inaccuracy of the analog circuits. The main source of the noise in a MOS

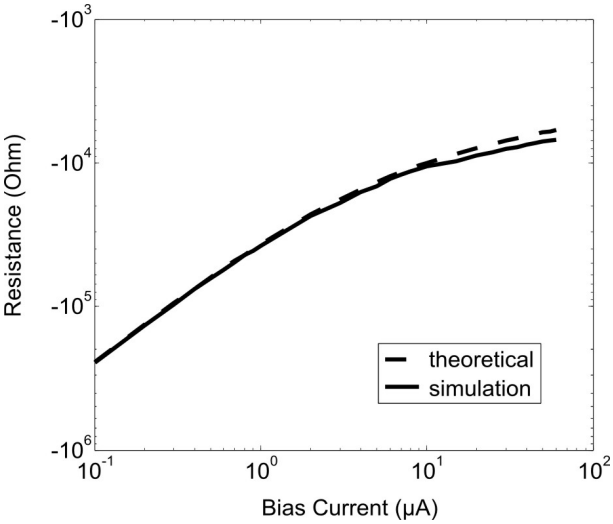

Figure 7: The negative resistance versus bias current.

transistor is the thermal noise owing to the thermal effect of the electrons in the resistive channel. The voltage noise of a MOS transistor is given in Eq. (10).

$$\overline{V^2} = \frac{8}{3} kTg_m r_0^2 \frac{V^2}{Hz} \tag{10}$$

where k is Boltzmann's constant and T is the temperature. g_m and r_0 are the transconductance and output resistance of the MOS transistor, respectively. Due to the fact that gm can be changed by the drain current of the transistor, the noise of the proposed circuit indicated in Fig. 2 depends on the biasing current.

A noise analysis of the negative resistor was performed in SPICE. Therefore, in accordance with SPICE results, the noise contributions of each transistor to the total output voltage noise are given in Table II.

Table 2: Noise sources of the proposed negative resistor.

Transistors	The voltage noise (V^2/Hz)	Transistors	The voltage noise (V^2/Hz)
M_1	$6.72x10^{-18}$	M_9	$2.60x10^{-15}$
M_2	$2.24x10^{-18}$	M_{10}	$6.80x10^{-16}$
M_3	$1.08x10^{-19}$	M_{11}	$6.80x10^{-16}$
M_4	$0.67x10^{-19}$	M_{12}	$19.77x10^{-20}$
M_5	$62.83x10^{-18}$	M_{13}	$7.03x10^{-21}$
M_6	$71.17x10^{-18}$	M_{14}	$1.70x10^{-18}$
M_7	$21.38x10^{-21}$	M_{15}	$1.00x10^{-30}$
M_8	$21.38x10^{-21}$		
Total voltage noise		64.07 nV/√Hz	

The resistance value of the proposed circuit is -6.31 kΩ for I_0=45 µA. The total voltage noise for the proposed circuit which has -6.31 kΩ resistance value is 64.07 nV/√Hz. The main contributors to the total noise are the three transistors M_9, M_{10} and M_{11}. Total voltage noises can be obtained as 57.544 nV/√Hz, 63.003 nV/√Hz and 64.070 nV/√Hz for I_0=15 µA, I_0=30 µA and I_0=45 µA, respectively. In other words, the total voltage noise is strongly depends on transconductance as shown in Eq. (10).

The negative resistance having a wide tuning range is an important advantage for the analog circuit applications. The comparison of the performance parameters belongs to some resistors and the proposed negative resistor is displayed in Table III.

If the circuits are compared in terms of supply voltage, the proposed negative resistor requires a small supply voltage. As shown in Table III, the total harmonic distortion of the proposed circuit is lower than the others. Moreover, this circuit consumes low power of which has only 65 µW value. The total voltage noise has not been studied in other cited paper. However, the total voltage noise of the proposed circuit can be obtained as 64.07 nV/√Hz.

4 Conclusion

In this study, the self-cascode composite transistor based a linear current-controlled floating negative resistor has been presented. The circuit required low supply voltage as well as ±0.75 V consumes low power about 65 µW. In addition, the circuit has highly basic circuit structure. The behaviour of the proposed resistor is highly linear from -250 mV to +250 mV. The value of the proposed resistance can also be adjusted from 5.9 kΩ to 243 kΩ with perfect correspondence between the theoretical and simulation results by changing the value of the bias current. The total voltage noise and THD values of the proposed circuit have been calculated as 0.465 % and 64.07 nV/√Hz, respectively. Finally, we expect that such a tunable behaviour of the proposed negative resistor could highly be appropriate for the low voltage integrated circuit realizations, considering into the perfect resemblance between all the simulated and theoretical performances.

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Table 3: Comparison between this study and the others.

Parameters	This study	[3]	[13]	[4]	[5]
Supply voltage	± 0.75 V	± 3 V	± 1.5 V	± 1.5 V	± 2.5 V
Input range	± 250 mV	± 1 V	± 200 mV	± 30 mV	± 30 mV
Tuning range	5.9 kΩ - 243 kΩ	800 kΩ - 4 MΩ	60 kΩ - ∞	43Ω - 516kΩ	132 Ω-1.25 kΩ
Total harmonic distortion (THD)	0.465 % (at 1 MHz)	0.5 % (NA)	NA	0.747 % (at 1 MHz)	> 1 % (at 1 kHz)
Total voltage noise	64.07 nV/√Hz	NA	NA	NA	NA
Power dissipation	65 µW	NA	NA	0.9 mW	NA
Bandwidth	222.1 MHz	NA	NA	70.2 MHz	NA
Technology	CMOS (0.13 µm)	CMOS (0.35 µm)	CMOS	Bipolar	Bipolar
Positive resistance	Yes	Yes	Yes	Yes	Yes
Floating	Yes	Yes	Yes	Yes	Yes

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Series Active Power Filter for High-Voltage Synchronous Generators

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Abstract: In this paper, an approach for minimization of voltage harmonics in the output of synchronous generators (SG) is described. It is based on three single-phase series active power filters (SAPF) that are inserted close to the common point of SG through an injection transformer. A distinctive advantage of the proposed approach is the use of low-voltage components that can be used due to SAPF insertion point position. Another benefit of the injection transformer implementation is also the possibility to increase the turns ratio and therefore the same approach can be used also for high-voltage SG. The solution was experimentally verified on two synchronous generators of various nominal voltage and power ratings. Due to very promising results, the implementation of the approach in high-voltage applications requiring low harmonic distortion is fully justified.

Keywords: series active power filter, synchronous generator, harmonic distortion, magnetostriction, power supply, repetitive control, digital signal controller

Serijski aktivni močnostni filter za visokonapetostne sinhronske generatorje

Izvleček: V prispevku je predstavljen pristop za zmanjšanje harmonskega popačenja na izhodnih sponkah sinhronskih generatorjev (SG). Rešitev temelji na uporabi treh enofaznih serijskih aktivnih filtrov, ki so preko vmesnih transformatorjev vezani zaporedno s faznimi navitji sinhronskega generatorja. Posebna prednost predlagane metode je uporaba nizkonapetostnih komponent, saj je posamezni aktivni filter v sistem priključen na strani skupne nevtralne točke trifaznega navitja generatorja. Rešitev je primerna tudi za visokonapetostne generatorje, saj lahko zmanjšanje harmonskega popačenja dosežemo z obstoječimi nizkonapetostnimi komponentami aktivnega filtra ob ustrezno izbranem prestavnem razmerju vmesnega transformatorja. Zahvaljujoč zelo obetavnim eksperimentalnim rezultatom na dveh generatorjih različnih nazivnih napetosti in moči je predlagana zasnova nadvse primerna za uporabo v visokonapetostnih aplikacijah, kjer je zahtevano majhno harmonsko popačenje izhodne napetosti.

Ključne besede: serijski aktivni močnostni filter, sinhronski generator, harmonsko popačenje, magnetostrikcija, napajalni vir, repetitivna regulacija, digitalni signalni krmilnik

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1 Introduction

A typical set-up for testing various equipment at high voltage and grid frequency relies on the use of a stand-alone synchronous generator (SG) and in majority of cases also a variable matching transformer. This solution assures that measurements can be performed electrically isolated from the grid and independent from the variable grid states. Furthermore, this approach also enables us to modify the voltage through SG excitation and transformer turns ratio and – if required – also the frequency (e.g. 50 Hz or 60 Hz) of the supply source. Although at first sight this solution is the obvious choice since it provides for a constant voltage waveform, it has some drawbacks that are connected with the SG itself and its design. Namely, when we look closely at the SG voltage waveform, we can observe that it is not perfectly sinusoidal. The reason for the presence of higher harmonics in the SG output voltage lies in the construction of the machine. Due to the fact that excitation winding is distributed in the slots across the SG perimeter, the magnetic field distribution in the air gap is not sinusoidal. Further increase of voltage distortion is a result of a non constant permeability of the air gap, different pole shapes, appearance of local magnetic saturation and a non-concentrically

designed rotor. The presence of higher harmonics in SG voltage can represent quite a challenge in some applications where a device under test (DUT) undergoes a series of typical laboratory or final production-stage measurements. A typical example is testing of power transformers, where among other measurements also a noise measurement of DUT at no-load is performed. In this case, DUT is supplied with its nominal low-side voltage from the grid-independent source consisting of SG and a matching transformer. When the voltage is applied, a certain level of noise is to be expected in the vicinity of DUT [1]. Its level and frequency spectrum depends greatly on the frequency spectrum of the supplied voltage that is causing magnetostriction-related vibrations in the transformer steel core and its enclosure [2 - 7]. It is clearly obvious that comparison of results from noise measurements performed using different voltage sources is not justified.

In the following chapters, a practical solution that actively suppresses higher voltage harmonics is described in detail. Although it is composed of low-voltage components, it is intended to be used together with high-voltage synchronous generators for special measurements requiring an improved voltage waveform.

2 Principles of harmonics reduction

Since the harmonic content in the output voltage of SG is a matter of a magnetic design, the first option for harmonic reduction would of course be optimization of SG magnetic characteristics [8, 9]. However, as this measure is not always effective enough, harmonic reduction should be performed with additional circuitry that enables suppression of certain harmonics or a certain frequency range. In general, these solutions are known as power filters and can be divided into two groups depending on the components used. The first group – the passive filters group – relies only on passive components, where using a combination of resistors, inductors and capacitors, a desirable transfer function as in low power electronics can be achieved. As it is often very hard to design a passive power filter with sufficiently high impedance compared to the load impedance to achieve effective suppression of voltage harmonics, another group – active power filters – is more common in power electronics.

Active power filters are divided into two subgroups depending on the harmonics to be cancelled from the system. The first type is known as a parallel active power filter (PAPF) and the second as a series active power filter (SAPF). Since PAPF is actually a current source, it is used where current harmonics are to be cancelled from the system [10-12]. Their position in the system depends on the reason causing the presence of harmonics – they can be placed closer to the supply or closer to the load. In the latter case, PAPF is connected in parallel with the supply source in a way that a sum of the load current and the power filter current results in a fundamental harmonic only.

On the other hand, SAPF filters are actually high frequency voltage sources that are connected in series with the supply to eliminate voltage harmonics from the system.

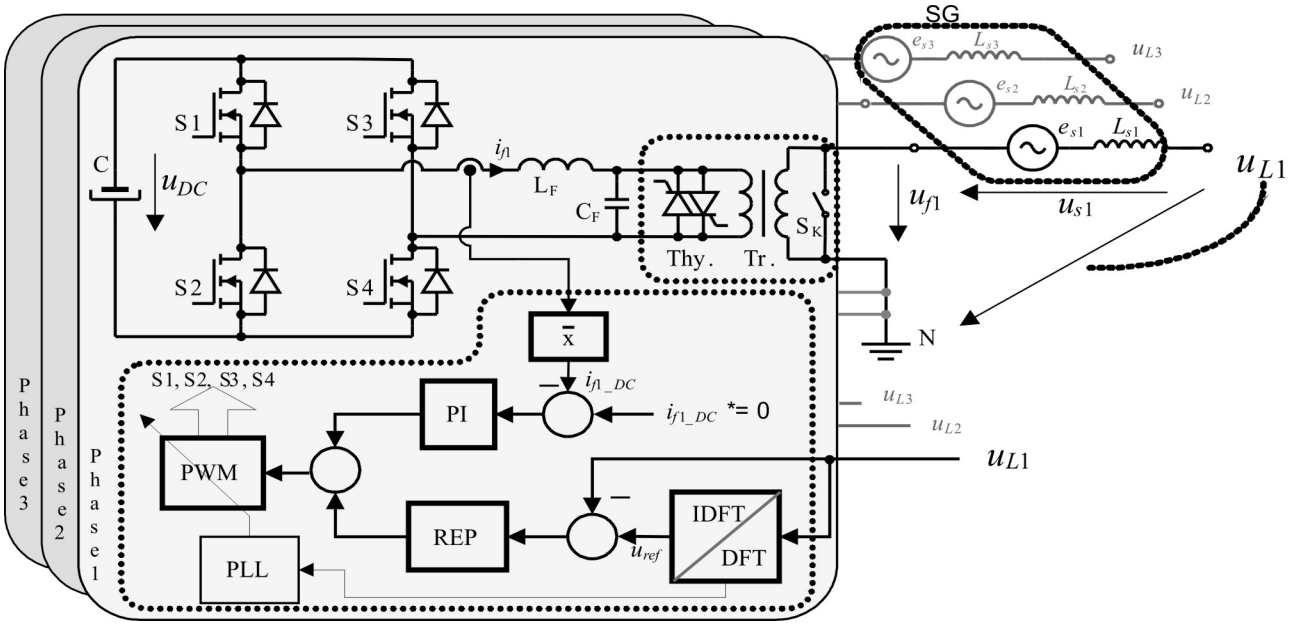

Figure 1: Diagram of the proposed system.

3 Proposed topology of SAPF

As the main objective of our research work was to cancel voltage harmonics from the SG voltage, we implemented a SAPF filter for that purpose [13]. A distinctive advantage of the SAPF, proposed in this paper, is its position. Namely, as it can be seen from Fig. 1, the SAPF position is close to the (normally grounded) common point of the SG three-phase windings. Consequently, being close to the ground potential, also insulation demands for filter components are significantly reduced. In that way, low voltage components that enable high frequency switching can be implemented.

3.1 Power stage of SAPF

The power stage of the proposed SAPF prototype consists of three subunits: a MOSFET transistor full bridge, an output low-pass LC filter for switching ripple suppression and an injection transformer. The latter enables an electrically isolated connection of high-frequency voltage to the SG voltage. When the SAPF is not active, anti-parallel thyristors (Thy.) on the primary side of the injection transformer and a power switch (S_K) on the secondary side are switched on. In this way, SAPF is bypassed and has no influence on the total system output voltage. When SAPF is active, both thyristors and the power switch are in their off state, so the voltage harmonics from SAPF can be transformed to the secondary side of the injection transformer.

3.2 Control algorithm

To be able to efficiently suppress higher harmonics from the SG spectrum irrespective of the SG operating point, an advanced repetitive control algorithm for SAPF is implemented. Basically, it can be divided into three functional control loops that are being executed by means of the supervising digital signal controller (DSC) TMS320F28335 and belonging input/output circuitry.

The first control loop is the voltage feedback loop. Among numerous approaches for reference voltage calculation [14 - 17], here, reference signal u_{ref} for the controller with repetitive action was calculated using the Discrete Fourier Transform (DFT) and Inverse Discrete Fourier Transform (IDFT). With DFT we derived A and B coefficients of the fundamental harmonic and then reconstructed it with IDFT. Since the control algorithm only requires the transform of the fundamental harmonic, a sliding DFT was used [18, 19] as it requires less computational power than the traditional DFT or FFT (Fast Fourier Transform). Its use is also beneficial since it can easily lock-in to the fundamental period in spite of its small frequency deviations or presence of higher harmonics in the synchronizing signal [14]. In such a way, the reference signal is perfectly synchronized with SG, thus preventing any active power being generated by SAPF. The preferred frequency span of the voltage controller was based on the SG voltage spectrum. In the final application, the controller frequency span was set to 5 kHz, while its sampling frequency was set to 51.2 kHz. In this way, 1024 samples per the fundamental period (50 Hz) were guaranteed. Yet, it should be noted that the voltage signal was actually acquired at a four-times higher frequency (204.8 kHz). This oversampling and the subsequent signal averaging improve the signal-to-noise ratio [20] and lower the requirements for an input anti-aliasing filter. Besides, the power stage PWM block was designed to run at twice the sampling frequency (102.4 kHz) thus minimizing the output LC filter size. The applied frequency relationships – affected by the built-in PWM timer - are shown in Fig. 2.

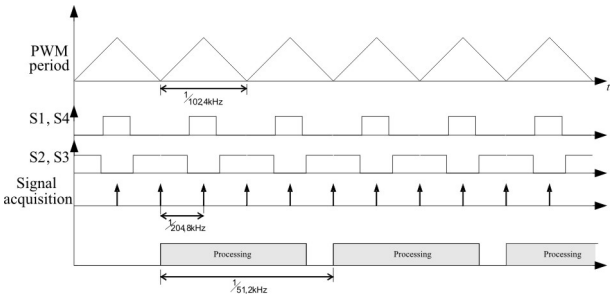

Figure 2: Timing diagram of sampling, switching and algorithm execution

Based on the reference signal u_{ref} and actual line voltage u_{L1} an error signal for the repetitive controller (REP) is obtained for each phase of the system. For a proper operation of the repetitive controller [21, 22], the line voltage sampling has to be synchronized with the period of the fundamental harmonic. For that purpose, a PLL (phase-locked loop) loop is implemented as a part of the control algorithm. Finally, the third control loop forces the SAPF DC current to be near zero and therefore prevents the saturation of the injection transformer.

4 Results and discussion

Firstly, the proposed prototype of SAPF was tested on a laboratory SG (P_n = 40 kVA, U_n = 400 V, n_n = 1500 min^{-1}). To determine what harmonic content is to be expected in the whole SG voltage range, a series of measurements was performed for different excitation levels and various loads. Based on experimental results, no significant change in the harmonic spectrum of the SG voltage was observed. As initially expected and then experimentally confirmed, the presence of harmonics

in the voltage spectrum is predominantly a matter of SG magnetic design. The SG waveform and frequency spectrum for one of the operation points at nearly half of the nominal voltage, are given in Fig. 3 and Fig. 4. The presence of voltage harmonics – especially beyond the frequency of 1 kHz – can be clearly observed from the voltage spectrum, resulting in a total harmonic distortion (THD) of 6.7 %.

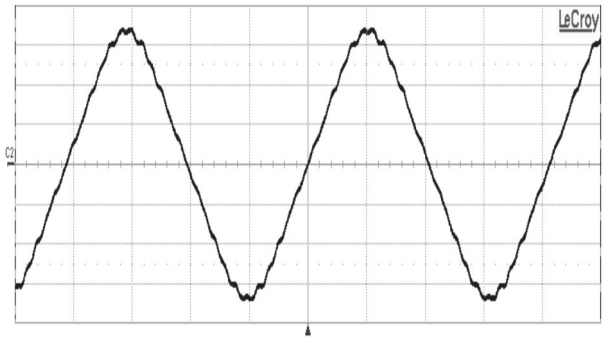

Figure 3: SG output voltage (k_u = 50 V/div, k_t = 5 ms/div).

Further tests were done with the SAPF inserted in the common point of the star connected SG windings as described in section 3. For the SAPF to be able to eliminate voltage harmonics from the SG spectrum efficiently, appropriate DC voltage should be applied to the transistor bridge inside the SAPF. Based on the harmonic spectrum measurements and SG nominal voltage, the DC link voltage was set to 60 V. With the SAPF active and for the same operating point as in Fig. 3, the overall system voltage waveform changed notably, as depicted in Fig. 5. A great improvement is also seen in the voltage harmonic spectrum (Fig. 6). Higher harmonics were efficiently suppressed, yielding in a THD of 0.29 %.

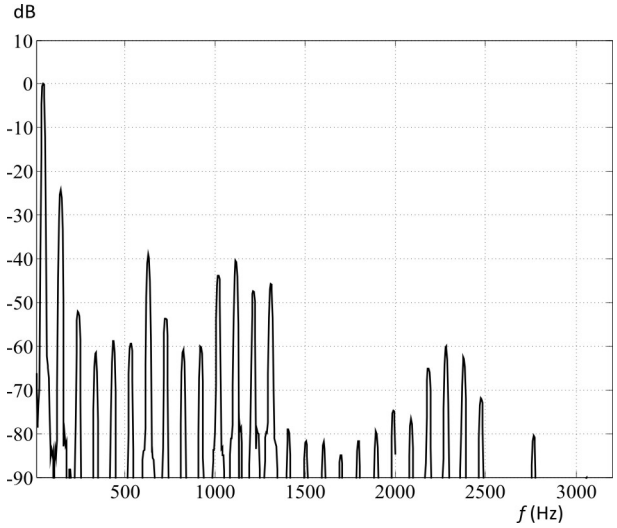

Figure 4: SG output voltage spectrum.

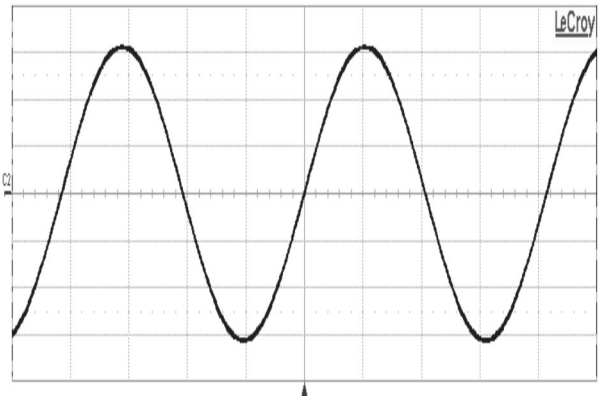

Figure 5: Total system voltage with SAPF active (k_u = 50 V/div, k_t = 5 ms/div).

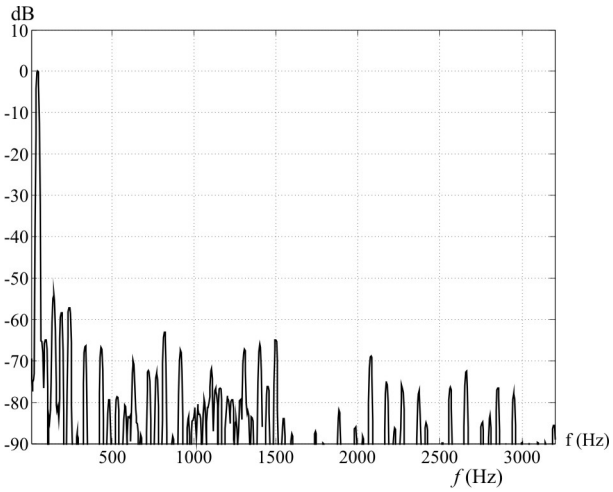

Figure 6: Total system voltage spectrum with SAPF active.

A second series of measurements was performed on the production site of a large producer of power transformers (Kolektor ETRA, Ljubljana, Slovenia). There, final quality control measurements of power transformers are done using a SG (U_n = 6 kV, P_n = 3.5 MVA) and a variable matching transformer in a similar way as described in chapter 1.

During the experiments, one of the power transformers (U_n = 6.3/20 kV, P_n = 8.5 MVA) from the production line was used as a DUT.

As the output voltage of the SG on the production site is substantially higher than the voltage of the laboratory SG, we performed an initial measurement of the SG output voltage and its spectrum in order to get an estimate value for the DC voltage of the SAPF. Similarly as with the previous SG, the output voltage (Fig. 7) is quite heavily distorted with higher harmonics (THD = 4.94 %) – especially around 2 kHz and 4 kHz, as can be observed from Fig. 8. In Fig. 9, also SG output current spectrum is given (THD = 8.75 %). A brief comparison of Fig. 8 and Fig. 9 reveals a close correlation

between the distorted SG voltage and the presence of harmonics in the load current that are consequently resulting in increased mechanical vibrations in the DUT core.

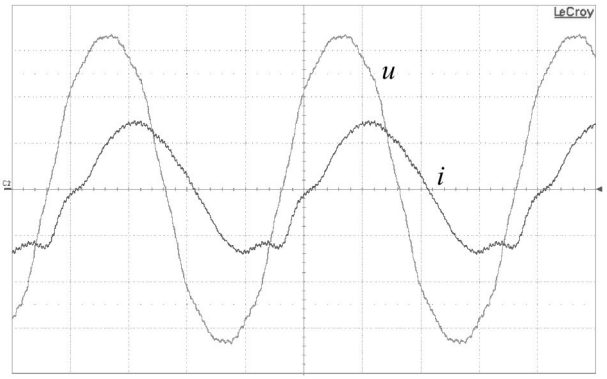

Figure 7: SG output voltage and load current (k_u = 1000 V/div, k_i = 5 A/div, k_t = 5 ms/div).

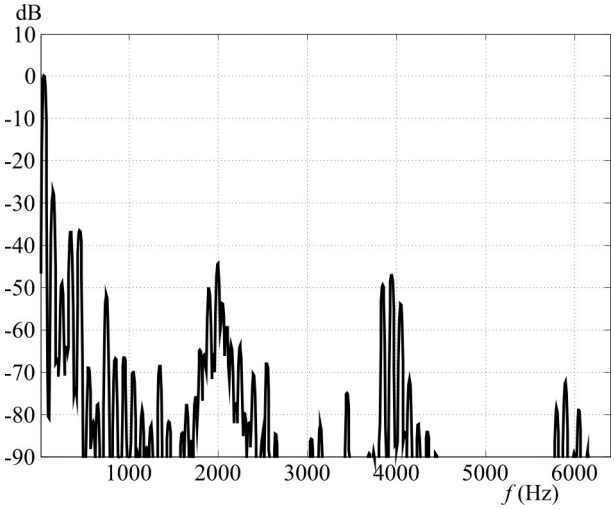

Figure 8: SG output voltage spectrum.

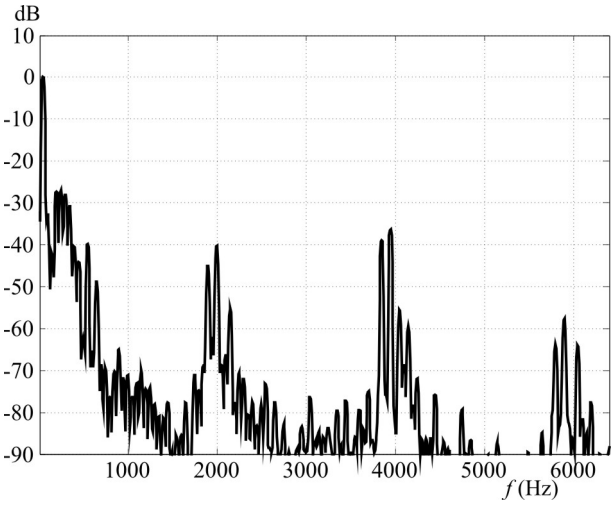

Figure 9:. SG output current spectrum.

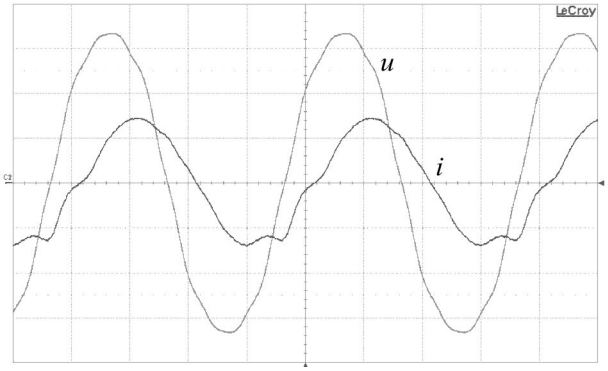

Figure 10: Total system output voltage and load current with SAPF active (k_u = 1000 V/div, k_i = 5 A/div, k_t = 5 ms/div).

Based upon the harmonic spectrum (Fig. 8) analysis, we estimated that the required DC link voltage of SAPF should be in the range of 600 V (for the installed injection transformer (Tr.) with turns ratio 1:1), which is substantially higher than the allowed maximum value of installed components. Namely, installed SAPF components - especially low voltage MOSFET transistors with high frequency switching capability - were selected in order to guarantee a sufficient precision for higher harmonics suppression. Since our focus during this stage was to eliminate only harmonics above the frequency of 1 kHz, the required superimposed voltage u_{f1} (Fig. 1) from SAPF could be achieved with a DC link voltage that is lower than the estimated 600 V for full harmonic reduction. Having that in mind, we set the DC link voltage to 90 V in this case, compared to 60 V that we used with the low voltage laboratory SG. Also, the main reference signal for the repetitive controller was calculated slightly different as in the case of the low voltage SG. Instead of calculating the reference voltage for suppressing all higher harmonics, here, the reference was calculated only for suppression of harmonics above the 9th. In that way, the resulting system output voltage (Fig. 10) was composed of a fundamental component and the 3rd, 5th, 7th and 9th harmonic component still present. Although there is no significant decrease in the voltage and current THD (voltage THD dropped from 4.94% to 4.83 % and curent THD from 8.75 % to 8.63 %), all harmonics above the 9th were efficiently suppressed as seen from the voltage (Fig. 11) and current spectrum (Fig. 12). Of course, if all harmonics are to be cancelled, firstly, the reference voltage calculation is to be modified back again and the DC link voltage or the injection transformer turns ratio should be increased accordingly to prevent SAPF PI controllers from saturation.

5 Conclusion

A low-voltage series active power filter was introduced for the minimization of harmonic distortion in the out-

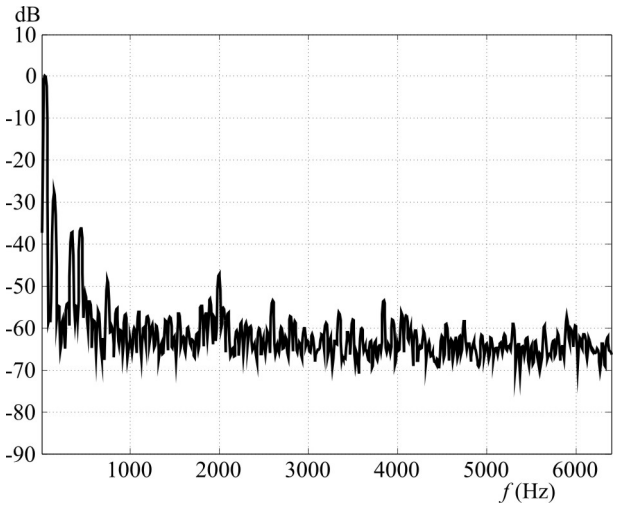

Figure 11: Total system output voltage spectrum with SAPF active.

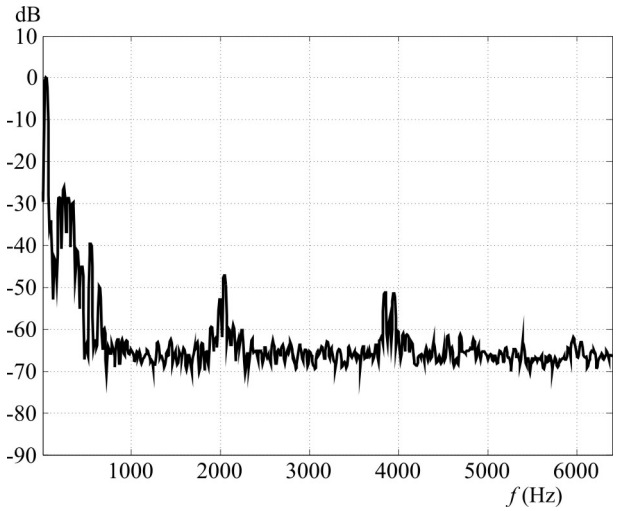

Figure 12: Output current spectrum with SAPF active

put voltage of synchronous generators. Instead of a more common three-phase solution, a single-phase topology was chosen due to a modular design, to simplify maintenance and finally, to achieve efficient harmonic suppression irrespective of voltage disproportions among individual phases. Due to the use of high-speed low-voltage MOSFET transistors in the SAPF full bridge and an advanced repetitive control algorithm, extremely low distortion of voltage can be achieved. Furthermore, due to sophisticated reference voltage calculation, various options for harmonics suppression can be achieved (i.e. full suppression, certain harmonic or a percentage of certain harmonic,…).

Our further work will be focused on implementation of the proposed topology for final production stage measurements of power transformers. A special research topic will be the correlation of the applied voltage with a certain level of harmonics and the produced noise level and frequency spectrum of the DUT.

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Model Checking using Spin and SpinRCP

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Abstract: Spin is one of the leading verification tools for the model checking of distributed systems. It is used over a broad spectrum of applications where systems can be represented as asynchronously running processes. This paper provides an overview of the concepts of model checking, the Spin model checker together with its input language Promela, and of the available graphical user interfaces to Spin. In order to offer Spin users an integrated development environment for Spin, we have developed a SpinRCP. We introduce its structure and demonstrate some of its features by considering a standard algorithm for leader election in a unidirectional ring.

Keywords: formal verification, model checking, modelling, simulation, Promela, Spin, SpinRCP

Preverjanje modelov z uporabo orodij Spin in SpinRCP

Izvleček: Spin je eno izmed vodilnih verifikacijskih orodij za preverjanje modelov porazdeljenih sistemov. Uporablja se za širok spekter aplikacij, pri katerih lahko sisteme predstavimo kot asinhrono izvajajoče se procese. V članku podajamo kratek pregled osnovnih pojmov o preverjanju modelov, preverjalniku modelov Spin, njegovem vhodnem jeziku Promela in razpoložljivih grafičnih uporabniških vmesnikih za Spin. Da bi uporabnikom orodja Spin ponudili integrirano razvojno okolje za Spin, smo razvili SpinRCP. Predstavljamo njegovo strukturo in prikažemo nekatere izmed njegovih značilnosti na primeru standardnega algoritma za izbiro vodje v enosmernem obroču.

Ključne besede: formalna verifikacija, preverjanje modelov, modeliranje, simulacija, Promela, Spin, SpinRCP

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1 Introduction

The constantly increasing sizes and complexities of contemporary ICT (Information and Communication Technology) systems as well as demands for reduction in costs and a shortening of time-to-market for a new product, confront designers with harder and harder tasks for ensuring the correct functioning of developed systems. Nowadays, ICT systems are becoming ubiquitous in our daily lives and we have to rely on their correctness. If any of them malfunction, it will be at least annoying for its user but in the case of safety-critical systems, such as for example systems in transport, medicine, industry, ecology, telecommunications, space exploration, and the military, each undiscovered error in the hardware or software may cause a lot of damage, threatening the health or even the lives of people. Let us recall some dramatic examples. Between 1985 and 1987 four cancer patients died and two were seriously injured following incorrect behaviour (100-times radiation overdosing) of the Therac-25 anti-tumour irradiating machine. The cause was a design error in the control software. On 4th June 1996, the Ariane 5 rocket changed trajectory and exploded 40 seconds after being launched on its first flight. The cause of failure was a variable overflow during the conversion of a 64-bit real number to a 16-bit integer. In 1997, a computer onboard the Mars Pathfinder had to be reset often due to an error in the algorithm for access of several processes to a common computer bus. A design error in the Intel Pentium floating point division algorithm in 1994 caused the loss of about 450 million dollars when replacing faulty processors. Therefore, the reliability of systems is a key issue in the system design process that takes up the greatest part of the design time and effort. A very promising approach towards ensuring the correctness of ICT systems is that of model checking. Model checking is a formal verification method that can automatically verify the desired behavioural properties of a given system through exhaustively exploring all states of a system's suitable model. One of the most successful model checkers is Spin [1, 2]. Although it was

originally designed as a tool for protocol verification, it is capable of model checking and simulating almost any system consisting of asynchronously running processes. Spin is a command line tool that accepts user commands from a command line and also outputs the results there. In order to ease Spin model checking, some graphical user interfaces have appeared for Spin. Two of them were developed at the Faculty of Electrical Engineering and Computer Science at the University of Maribor. In this paper we introduce the latest one called SpinRCP.

Section 2 introduces the basic concepts of model checking including its strengths and weaknesses. Section 3 provides a short overview of Spin and its input language called Promela. Section 4 gives an overview of the currently available graphical user interfaces for Spin. Section 5 introduces our new integrated development environment (IDE) for Spin called SpinRCP. The use of SpinRCP is demonstrated on the model of an algorithm for leader election in a unidirectional ring in Section 6. Section 7 draws together the concluding remarks.

2 Model checking

Model checking is an automated technique that, given the finite-state model of a system and a formal property, systematically checks whether this property holds for (a given state in) that model. A detailed explanation of the model checking technique can be found in [3]. A schematic view of model checking is shown in Fig. 1. We can distinguish between three different phases when applying model checking to a system: the modelling, running, and analysis phases.

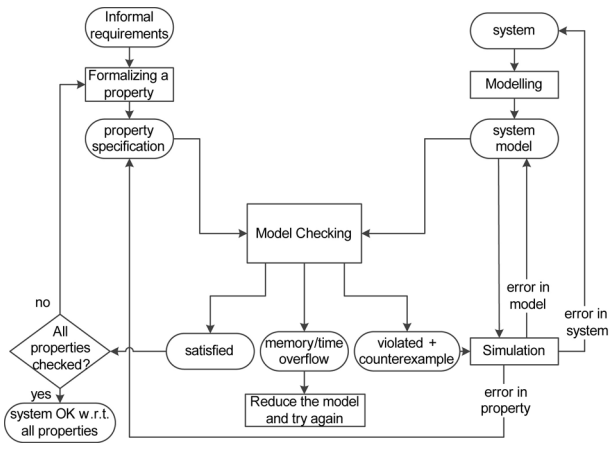

Figure 1: Schematic view of model checking.

In the *modelling phase*, a model of the system under consideration has to be obtained. Models describe the possible behaviours of systems in a precise and unambiguous manner. They are usually expressed as finite-state automata that consist of a finite set of states and a final set of transitions. Models can be created either manually or automatically using a model extraction tool. In both cases the model has to be described in a description language used by the model checker. Simple errors within the model can be found by simulation prior to the model checking. Such inexhaustive simulation can disclose errors in the model but it cannot guarantee that the model is error-free. In order to find any remaining subtle errors, we have to resort to rigorous verification using model checking. The informal requirements for the system's behaviour have to be formalised into precise and unambiguous properties using an adequate property specification language. A kind of temporal logic is most often used. The model checking process actually checks whether the system description *M* is a model of a temporal logic formula *P*. A temporal formula can express the behaviour of a system over time. It allows the specifying of relevant system properties regarding the following kinds: functional correctness (does the system do what it should?), safety ("something bad never happens"), liveness ("something good will eventually happen"), fairness (does an event occur infinitely often under certain conditions?), and real-time properties (does the system act in due time?).

In the *running phase* the user has to set various options, parameters, and directives for the model checker that should be used for verification. Then, the model checker automatically checks the validity of the property under examination in all states of the system model.

In the *analysis phase* the user has to evaluate the outcome of model checking performed within the previous phase. There are three possible outcomes: the specified property is either valid or violated in the given model, or the model turns out to be too large to fit in the available computer memory or the model checking run is unfinished within a reasonable amount of time. If the property is valid, the next property can be checked with a new run perhaps with different options, parameters, and/or directives. If the property is violated, a counterexample is generated that can be analysed by simulation. The counterexample guides the simulation run across a path where the property is violated. A thorough counterexample analysis can reveal the cause of the violation. It may be a *modelling error*, a *system design error*, or a *property error*. In the case of the modelling error, the model does not reflect the design of the system. The model has to be corrected and all the properties have to be checked again. In the case of the system design error, the system does not behave as required and has to be corrected. The last possible

cause is that the property does not reflect the informal requirement for the system behaviour. This implies a revision of the property and a new verification for this property. The designed system is verified with respect to the given properties if and only if all of them have been proven valid. Whenever the model is too large to be handled within the available amount of computer memory or within a reasonable time, the model has to be reduced using different abstractions.

Model checking has many strengths including the following ones: it is a general technique that is applicable to a wide range of systems (e.g., protocols, hardware, software), it allows partial verification (only the more relevant properties are checked), it is nothing harder to find less likely errors than the more likely ones, it provides a counterexample in case a property is invalidated, it is an automatic technique and software tools exist, or it is more and more accepted in the industry.

On the other hand, it also has some weaknesses: it is mainly appropriate for control-intensive applications and much less suitable for data-intensive applications, it is applicable only to final-state systems, it verifies a system model, and not the system itself, its results are only as good as the system model, it checks only given properties and provides no guarantee about the completeness of the results, it is faced with state-space explosion, or it cannot handle parameterised systems.

Despite these weaknesses it is a fact that model checking is an effective technique for exposing potential design errors and thus increases the quality of a system design.

3 Spin and Promela

This section provides a short introduction to the input language of Spin called Promela and the main features of Spin.

3.1 Short Introduction to Promela

Promela (**Pro**cess or **Pro**tocol **Me**ta **La**nguage) is a language for describing finite state automata. It is not intended to be an implementation language but a system description language that is aimed at facilitating the searches for good abstractions of systems' designs. The language is oriented towards the modelling of process coordination and synchronisation, and not to computation. The reason is simple. Promela is not a programming language but a verification modelling language. Promela language reference can be found in [1].

A Promela model consists of processes, variables, and channels. It corresponds to a finite state transition system, hence all objects in Promela are bounded. The processes are global objects, whilst the variables and channels may be declared either as global or local to a process. A new inline or block scope for variables has been introduced since Spin Version 6.

The processes are instantiations of proctype declarations and define parts of the system's behaviour. A proctype consists of a name, a list of formal parameters, local variable declarations, and a body. The body consists of a sequence of statements. A process executes concurrently with all other processes. It communicates with other processes using either global (shared) variables or channels. There may be several processes of the same type. Each process has its own local state that consists of a process counter (current location within the proctype) and the values of the local variables. Processes can be created within any process at any point of execution using the run statement. They can also be created by adding the keyword active in front of the proctype declaration. A so-called init process becomes active in the initial state of the system. It serves to initialise other processes and global variables.

Promela has nine basic (integer) variable types: bit or bool (1 bit), byte (8 bits), chan (8 bit), mtype (8 bit), pid (8 bit), short (16 bits), int (32 bits), unsigned ($1 \leq n < 32$ bits). More complex types (records) can be composed from the basic types with the keyword typedef.

Message channels in Promela are used to model the exchange of data between processes. Channels can be either asynchronous or synchronous (rendezvous). Asynchronous channels are queues or buffers, and can store a finite number of messages. Synchronous channels have a length of zero. Channel declaration is introduced by the type name chan followed by the channel name, length of the channel queue (channel capacity) and the structure of the messages, which can be stored in the channel as a comma-separated list of type names.

The body of a process consists of statements that execute sequentially. There are two kinds of statements: statements that never block and statements that may block. An expression is also a statement and is executable if it evaluates to non-zero but is blocked otherwise. No other statement within a process may be executed until the statement evaluates to true, which may result from a variable assignment or a received message, for example. Statements if and do consist of one or more option sequences. An option sequence begins with a guard, and if the guard evaluates to true, the option sequence is selected for execution. If more than one

guard is true, the selection of the statement to be executed is non-deterministic. If no choice is executable, the statement is blocked. The only difference between these two statements is that after the execution of the selected statement, a do statement repeats the choice selection but an if statement ends the execution. The always executable break statement exits a do loop.

There are four ways to express correctness properties in Promela: assertions, trace assertions, labels, and never claims. Assertions express invariants. If an invariant is false at the point where the assertion occurs, Spin reports an error. Trace assertions perform similarly to channels. Labels can be of type *accept*, *end*, and *progress*. They mark the states in a process and have a special meaning when Spin is run in verification mode. The accept state labels are normally used only in never claims that are mentioned below. The verifier can find all cycles that do pass through a state with an accept label. The end label marks a valid end state that is not at the end of a process' code (i.e., the closing curly brace in the corresponding proctype body). The progress label marks a statement in a Promela model that accomplishes something desirable and thus makes progress. The never claim expresses behaviour that should never occur. Usually, it is automatically generated from a linear temporal logic (LTL) formula.

3.2 Principles of Spin

Spin is one of the most often used and successful model checkers. It was written by Gerard J. Holzmann at Bell Labs [1, 2]. The software has been available freely since 1991, and continues to evolve. The latest version of Spin is Version 6.2.5 issued on 4th May 2013. Spin download distributions and a lot of additional tools and relevant information can be found at the Spin home page http://spinroot.com/. Spin beginners' tutorial and practically-oriented introduction to the principles of the Spin model checker are available in [4] and [5], respectively. The Spin model checker takes a Promela model as an input. Hence where its name is derived from. Spin is an acronym for **S**imple **P**romela **In**terpreter. In 2001, the Association for Computing Machinery (ACM) recognized Dr. Gerard Holzmann by a prestigious ACM Software System Award for Spin.

Let us suppose that a Promela model M has *n* processes, defined by proctype declarations. Spin first transforms them into finite state automata A1, A2, …, An. Then, it creates an asynchronous product of all automata. The states of this product automaton are called the state space or the reachability graph of the model. Next, consider that a property that has to be satisfied by a model, is expressed by an LTL formula *f*. Spin first generates a never claim for the negated formula ¬*f* and converts it into a corresponding Büchi automaton, B. Spin can check if M satisfies *f* by computing the global system automaton S

$$S = B \otimes \prod_{I=1}^{n} A_i$$

We use the operator ∏ to represent an asynchronous product of multiple component automata, and ⊗ to represent the synchronous product of two automata [1]. The automaton S is now analysed for its acceptance properties. If S has accepting ω-runs (i.e., a certain state in the set of its final states is visited infinitely often in the run), then formula *f* can be violated (and ¬*f* can be satisfied). If no accepting ω-runs are found, then the system is considered valid. In this way liveness properties are formulated. Informally, a liveness property says that "something good will eventually happen". Spin works the other way round. It tries to find a (infinite) loop in which the "good things do not happen". If there is no such loop, the property is satisfied. Another class of properties is safety properties (e.g., invariance, deadlock, livelock, unreachable states). Informally, a safety property says that "something bad never happens". Spin tries to find an execution path leading to the "bad" thing. If there is no such execution path, the property is satisfied.

For each model to be verified, Spin first generates a C verifier program, which can then be compiled to the executable verifier called pan. When it finds an error, a counterexample is generated, which can be used in a guided simulation that replays the execution path that violated the property. Random and interactive simulation is also available. They can be used for the sake of early detection of (simple) errors before verification.

Spin has several optimisation algorithms to make the verification process more effective (e.g., partial order reduction, statement merging, state compression, bitstate hashing, hash-compact) [1]. In addition, a slicing algorithm gives the user hints of what can be "thrown away" in a model description in order to reduce space and time consumption.

3.3 Spin Application Domains

Due to the nature of Promela, it can be used to model many different kinds of systems of asynchronously (and synchronously) communicating processes [6]. Thus, Spin that takes a Promela model as its input, has been used for a wide range of different applications: protocol design and verification, feature interaction, safety critical system verification, embedded and reactive system verification, hardware circuit modelling, hardware/software codesign, finding solutions for op-

timising problems, verifying contracts and guidelines, verifying business processes, modelling telephone switching systems, modelling multimedia presentations, modelling routers and network traffic, modelling operating system kernels, scheduling and plan execution, verifying bytecode, modelling genes, etc.

4 Graphical environments for Spin

The most basic way of using Spin is textual. A user enters the commands at the command line and Spin outputs are printed on standard output afterwards. Such an approach to model checking could be difficult and discouraging especially for newcomers who are not yet well acquainted with Spin commands. Of course, the availability of a user-friendly graphical interface to Spin is of a considerable benefit for skilled users as well. In order to accomplish these needs, several different graphical interfaces or environments for Spin have been developed. This section provides a brief overview of Xspin, jSpin, Eclipse Plug-in for Spin, iSpin, and EpiSpin. In the next section we present our SpinRCP.

4.1 Xspin

Xspin [1] was the first graphical interface to Spin. The interface runs independently from Spin itself. It generates the proper Spin commands in the background, based on user menu selections and button clicks, then obtains the Spin output and wherever possible attempts to generate a graphical representation of this output. Xspin interface was very suitable for dealing with small models, but coping with larger ones was much more difficult due to the lack of syntax colouring and code folding. In addition, the opening of a separate window for each task during investigation of a model was inconvenient.

Xspin was written in Tcl/Tk script language. The last version of Xspin was Xspin Version 5.2.5 from 17th April 2010. Since then it has no longer been supported. In Spin Version 6 it was superseded by iSpin.

4.2 jSpin

jSpin [7] is an alternative graphical user interface for the Spin model checker. It was developed by M. Ben-Ari primarily for pedagogical purposes. It is written in Java.

jSpin's interesting part is its SpinSpider component, which is very useful for demonstrating the properties of concurrent programming. As in the case of Xspin, syntax colouring and code folding are missing. In contrast to Xspin, message passing between communicating processes is displayed only in textual form.

4.3 Eclipse Plug-in for Spin

In [8, 9] we introduced a new approach for automatic model extraction and applied it in our tool called *sdl2pml*. It can generate a Promela model of a system specified in SDL. The tool was tested on the implementation of an ISDN User Adaptation (IUA) protocol, which is part of the SI3000 softswitch. The specification was developed by Iskratel d.o.o., which is the largest Slovenian telecommunication equipment developer. The generated Promela model is huge with its 79,281 lines of code. We didn't have any suitable Promela editor that would be suitable for such large models. Therefore, we decided to create an Eclipse Plug-in for Spin with a user-friendly Promela editor that includes syntax colouring and code folding and similar capabilities for running Spin syntax check, simulation and verification as Xspin [10, 11]. In order to ease analyses of extremely long Spin simulation trails (e.g., Spin trail of the simple call with the use of IUA protocol consists of 55,371 lines of text and contains 21 processes that communicate using 261 messages) we have developed a Spin Trail to Message Sequence Chart (MSC) tool called *st2msc* [12]. It converts a Spin simulation trail into a standard MSC textual representation according to standard Z.120 [13]. Professional telecommunication design tools such as ObjectGEODE can read this MSC representation and display message sequence charts in graphical form.

The Spin Plug-in is written in Java and uses numerous other plug-ins available within the Eclipse environment. It has proved to be very useful when working with large models but also has some shortcomings: an interactive simulation is not implemented, better filtering of the Spin simulation output trail is missing, and graphical display of MSCs is only possible with the use of external tools.

4.4 iSpin

iSpin [14] is the graphical user interface that has replaced Xspin since Spin Version 6.0.0. It was provided by the Spin author, G. J. Holzman, and is included in each new Spin release. Just like Xspin, iSpin is implemented using the Tcl programming language and the Tk graphical user interface toolkit.

iSpin is a good upgrade of Xspin and is much more user-friendly, because all operations display their results in different areas of a single window and don't open new windows as in the case of Xspin. iSpin is the only graphical user interface to Spin that supports a swarm verification run [15] that distributes verification loads amongst more computing cores or platforms. Syntax colouring and code folding would be welcome for the editing of large Promela models.

4.5 EpiSpin

EpiSpin [16], introduced by de Vos et. al., is an Eclipse plug-in for editing Promela models and starting Spin verification and simulation runs. It includes its own error checker that instantaneously feedsback on syntax and semantic errors, syntax highlighting, code folding, reference resolving, and a graphical tool for displaying the static relationships between channels, and processes and global variables. EpiSpin has been built using the Spoofax language workbench.

This tool is primarily oriented towards providing various editor services for editing Promela models and a dot graph that shows how model processes can communicate using channels and global variables.

5 SpinRCP IDE

Motivated with good responses to our Eclipse Plug-in for Spin and suggestions for the integration of the full functionality of the then graphical interface Xspin into Eclipse, we decided to develop an integrated development environment that will facilitate entering new or reviewing extracted Promela models from an existing software code, simple parameters choosing for individual operations on the model, running Spin verification and simulation, and keeping records of file versions [17]. This new environment will remove some disadvantages of Eclipse Plug-in for Spin, particularly the lack of interactive simulation implementation and the need for external tools to display MSCs graphically.

For the implementation of this environment we selected the Eclipse Rich Client Platform (RCP) technology. RCP is the minimum set of plug-ins needed to build a rich client application. It allows us to quickly build a professional-looking application, with native look-and-feel, on multiple platforms.

5.1 SpinRCP architecture

After launching the application, one single window entitled SpinRCP with its version number opens. Ac-

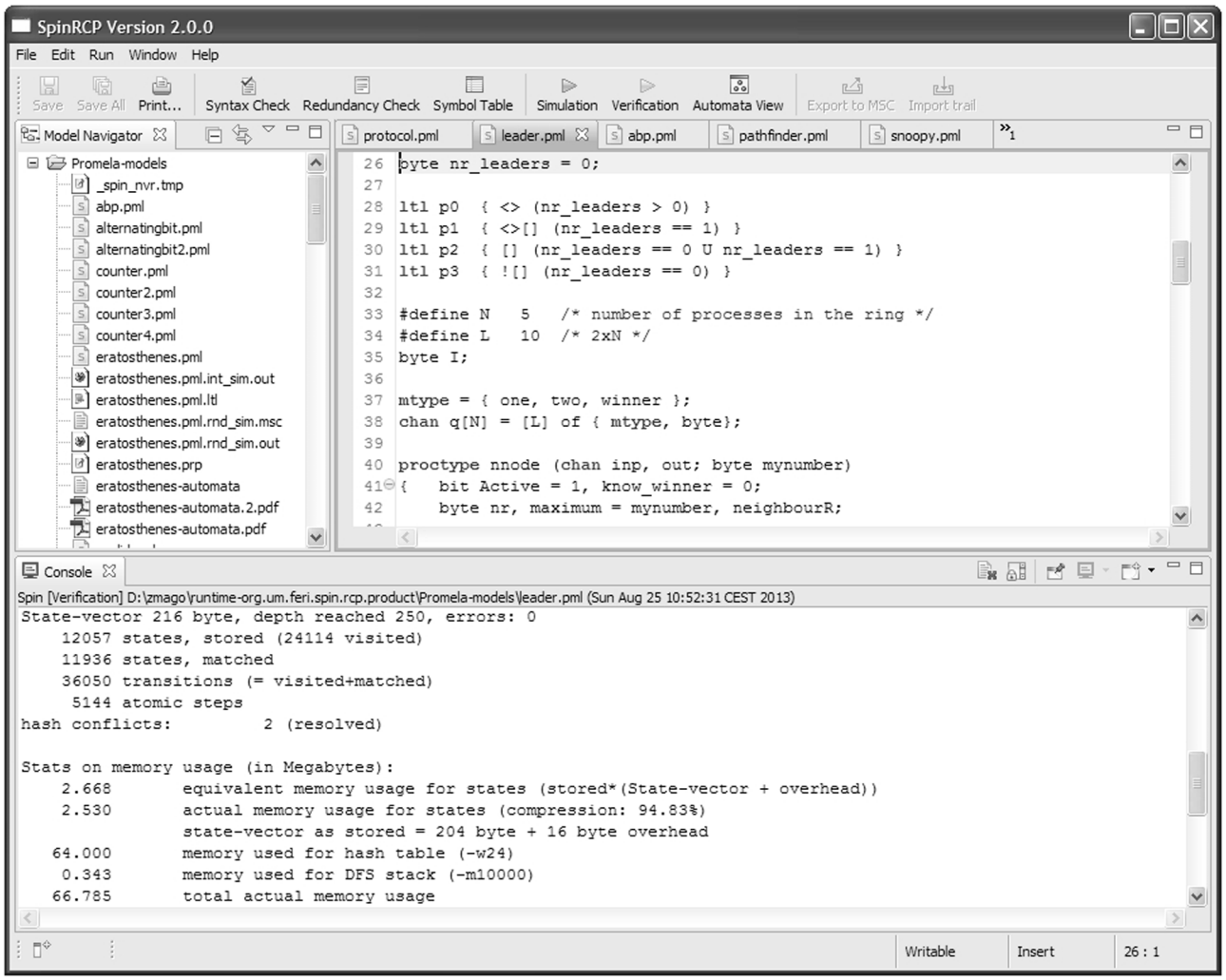

Figure 2: SpinRCP Workbench during verification.

cording to the terminology of Eclipse it is called a Workbench. A Workbench consists of perspectives, views and editors. A perspective is a group of views and editors in the Workbench window. A view and an editor are visual components within the Workbench. In SpinRCP, there are many different views (e.g., Model Navigator, Console, Simulation, Spin Trail To MSC, CVS Repositories, ...) and only two editors (Promela Editor as a special case of Text Editor and MSC Viewer as a special case of Graphical Editor). Some features are common to both views and editors. We use the term "part" to mean either a view or an editor. Parts can be active or inactive, but only one part can be active at any one time. The active part is the one where the title bar is highlighted. Using a simple drag-and-drop operation you can relocate and/or resize any part and thus reform the SpinRCP perspective at your will. The outlook of Workbench with SpinRCP perspective during verification is shown in Fig. 2. It consists of the Menu bar, the Tool bar, the Model Navigator View, the Promela Editor, and the Console View. Below we present in short these parts of the Workbench.

5.2 Menu bar

At the top of the Workbench there is a Menu bar with five menus already known from Eclipse: File (to open, save, or print a file, and exit the application), Edit (to undo or redo an editing action, to cut, copy, paste, or delete a selected text, and to search for and replace a specific text in the Promela Editor or the Console), Run (to run any of the SpinRCP tools), Window (to show any of the available views, to open, save, or reset a perspective, to set general or Spin preferences), Help (to obtain installation details about SpinRCP, to browse help contents including the possibility of printing the selected topics without or with all subtopics, allows locating local topics, remote documents, and other documents given a search query, gives context-sensitive help, and displays a list of key bindings).

5.3 Tool bar

Below the Menu bar is the Tool bar. The first three Tool bar icons (Save, Save All, and Print…) are shortcuts of the equally named operations from the File menu. They are followed by eight shortcut buttons for launching a specific SpinRCP action. Syntax Check uses Spin –a option for performing a thorough model syntax check and generates the source C program for a model-specific verifier. Redundancy Check uses Spin –A option to apply a property-based slicing algorithm for the model, which can detect eventual redundancies in the model and generate suggestions on how the model could be revised in order to use less memory. Symbol Table uses the Spin –d option to produce symbol table information for the Promela model. The information for each Promela object depends on its type. Simulation opens the Simulation preference page, where the user can select the type of simulation (random, guided, interactive) and some simulation parameters. Then the simulation view opens and the user can start the selected type of simulation. Verification opens the Verification preference page, where the user can select and/or enter many basic and advanced verification options and then verification starts. Automata View opens the Automata View preference page, where the user can select in which graphical format the automata should be displayed. Ten different file formats are currently available. SpinRCP uses options –o3 and –a to generate the verifier source C code, then compiles it to pan and runs pan using run-time option –D. This option generates state tables for each proctype and each never claim in the format accepted by the dot tool from Graphviz [18]. These state tables are redirected to a text file. Next, the dot tool transforms this text file to a set of files (one file for each proctype or never claim) with the previously selected graphical format. Then, a dialogue appears, where the proctype or the never claim to be displayed can be selected. Finally, a system program, assigned to a given file type is opened and the selected automaton is displayed. In the Simulation View, where the MSC Viewer is active, two other shortcut buttons are enabled – Export to MSC and Import trail. By clicking the first one the currently displayed MSC in the MSC Viewer is exported to a selected file with standard MSC textual representation according to standard Z.120 [13] using the st2msc tool introduced already in [12]. By clicking the second button the Spin simulation trail in a selected file is read-in and the MSC is displayed in the active MSC Viewer.

5.4 Model Navigator

The Model Navigator View is designed to create a new file, folder, or project resource, an untitled text file, or import resources from the local file system into an existing project. The resources on local disk are represented in a tree structure. If a user double-clicks a file, an appropriate internal editor or external program opens this file. For Promela files of type pml and simulation trail files of type out the Promela Editor and MSC Viewer Editor are default editors, respectively. On the SpinRCP General preference page either an internal editor or an external program can be associated for each file type. Using the Project wizard within the Model Navigator we have to generate a project, which is actually a place, where our models and other files, produced by the SpinRCP IDE, will be stored. Within a wizard for the creation of a new Promela model, a user has to select a project (that is a container where the model is to be stored) and enter the file name of type pml. The Promela Editor opens a new file with a given name and

automatically inserts an empty init process so that the user doesn't need to do it manually.

5.5 Promela Editor

We have developed the Promela Editor already for our Eclipse Plug-in for Spin [10, 11]. In SpinRCP it is almost unchanged. For ease of viewing and editing models the following features are available: syntax highlighting, code folding, content assist, and marking a place of a syntax error.

Syntax highlighting is a feature of Promela Editor that displays the text of the source file in different colours according to the category of terms. Highlighting does not affect the meaning of the text itself; it is only intended for human readers. The colours for different groups of reserved words, comments, and default text can be selected on the Promela Editor preference page. The default colours for text and comments are black and blue, respectively. According to the Promela language reference in [1], Promela reserved words can be grouped into seven sections: Meta Terms, Declarators, Control Flow Constructors, Basic Statements, Predefined Functions and Operators, Embedded C code, and Omissions. All the reserved words in a section will be displayed in the same colour. In each section a different colour can be set. By default, reserved words from all seven sections are displayed in the same (violet) colour. By default, the colours are enabled. They can also be disabled by deselecting the *Enable colours* checkbox.

Code folding allows the user to selectively hide or display sections of a currently-edited file. This allows the user to manage large amounts of text whilst viewing only those subsections of the text that are specifically relevant at any given time. Code folding is possible between an opening curly bracket "{" and closing curly bracket "}". This feature is commonly used to hide/display the bodies of large proctype declarations and is essential for studying the specifications in real systems.

Content assist or autocomplete is a functionality provided by SpinRCP that helps the user to write code faster. A user can just type in the first letter(s) of the reserved word and then press Ctrl+Space to be offered all the choices that match the entered letters that are valid for the current context. He/she simply selects the wanted word. This help is especially useful for a beginner who is not yet well acquainted with Promela syntax.

The Promela Editor uses a mechanism for marking syntax errors. If the Spin syntax checker detects a syntax error within Promela source code, SpinRCP parses its error message and finds out the line number where the error occurred. The Promela Editor marks this line with an error icon. A detail reason for the displayed syntax error is shown in the Console and in the Problems View.

Many instances of the Promela Editor containing Promela (or other) files can be opened simultaneously but only one editor can be active at any one time. The active editor is the one, the title of which is highlighted.

5.6 Console

Console is a view that is used for displaying the synthesised Spin commands and Spin textual outputs for all actions on the model. Below the console title bar a header line is displayed that consists of four strings: "Spin" – the parent application that is executing, the name of the action that is being performed (e.g., Verification, Random Simulation, etc.) in square brackets, the full path to the file containing the Promela model, over which the action is being performed, the exact date and time at which the action started.

All outputs for the same type of action (e.g., verification) and the same model are written to the same console. Thus, the number of created consoles at any time is equal to the sum of the number of different actions that have been performed on each model so far. Filtering of Spin outputs is helpful for a user who can now gather the results that are important to him/her much more easily. The contents of any console can also be cleared or copy-pasted in the whole or just within a selected area anywhere else for later use.

5.7 Preference pages

SpinRCP has several preference pages on which the user can set values to different kinds of variables. The following preference pages are available:

- General,
- Spin,
- Automata View,
- MSC Viewer,
- Promela Editor,
- Simulation,
- Verification.

In the General preference page a subset of the more common general preferences from Eclipse can be set (appearances of colours and fonts, editors file associations, different text editors' options, keys' bindings, perspectives, and workspace options, etc.).

Spin preference page (Fig. 3) is used to set paths to external tools. These paths have to be set before the first usage of SpinRCP. Spin is the main external tool for which the SpinRCP was developed at all. Therefore, it is mandatory to set the path to Spin. Since Spin gen-

erates a verifier for each model being checked as C source code, which has to be compiled to an executable code, we need an installed C compiler. We use gcc-4 from Cygwin environment and that is why we have set the path to gcc-4 C compiler. The conversion of a Spin textual simulation output trail to MSCs is done by the st2msc tool [12]. Therefore, the absolute path to the file st2msc.jar has to be set. Of course, the path to the Java Runtime Environment that runs st2msc.jar has to be set, too. A path to the Graphviz dot tool is necessary if we want to generate graphs of the processes and never claims. If the PATH environment variable of the computer system includes paths to Spin, C compiler, Java, and dot, we don't need to enter their absolute paths but just their names as shown in Fig. 3. Paths with spaces are also allowed. SpinRCP recognises such paths and encloses them in double quotes.

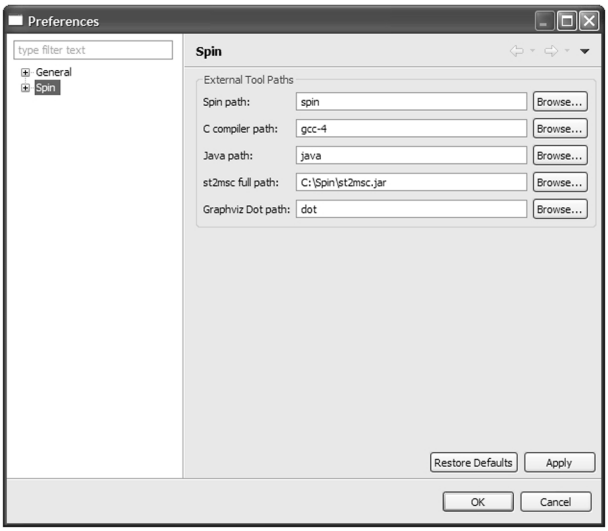

Figure 3: Spin preference page.

The Automata View preference page (Fig. 4) gives the user a choice to select a type of files that will contain the computed state transition system for all processes in the model and all never claims, and whether or not the automata view dialogue will be shown after graph creation. Currently the following file types are supported: bmp, dot, eps, fig, gif, jpg, pdf, png, svgz, and tif.

On the MSC Viewer preference page the MSC refresh interval can be set (default is 50 ms). In addition, it can also be set as to whether the message parameters will be shown in MSC diagrams or not.

The Promela Editor preference page is used to select colours for different categories of terms in Promela source file or disable colours.

The Simulation preference page (Fig. 5) offers the user the possibility of selecting the Spin simulation mode

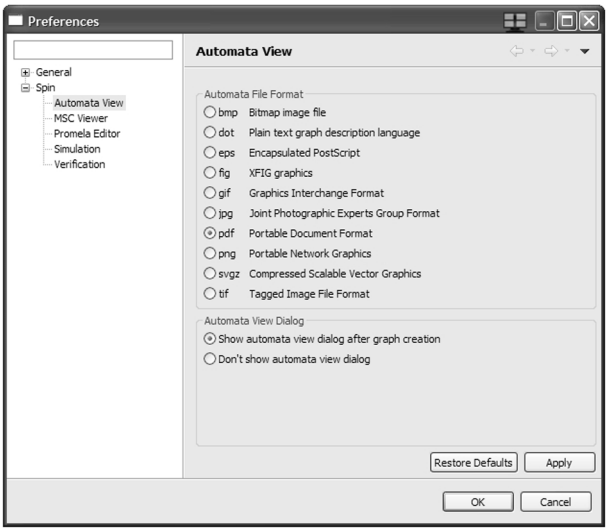

Figure 4: Automata View preference page

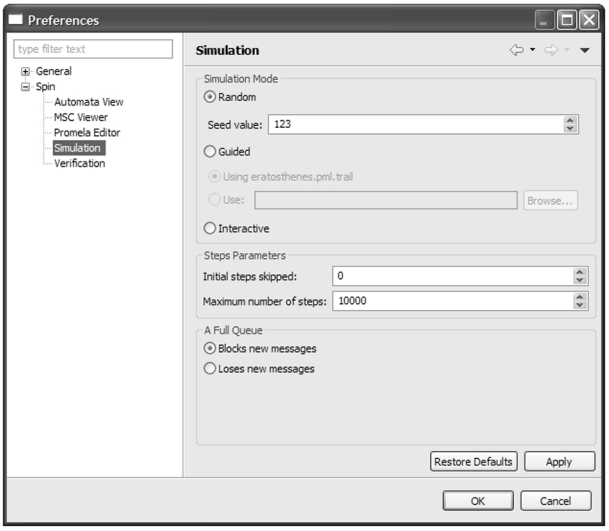

Figure 5: Simulation preference page.

(random, guided, or interactive). A seed value can be set for random simulation. Either the default Spin trail file with the extension .trail added to the original Promela source file or any other Spin trail file can be selected for guided simulation. The number of initial steps skipped (default 0), the maximum number of steps (default 10000), and how a full queue is simulated (either blocks or loses new messages), is also selected on this page.

The most complex preference page in SpinRCP is the Verification preference page (Fig. 6 and Fig. 7). In the upper part, the user can export current verification parameters (verification profile) to an xml file and import or reload a previously saved verification profile. Verification options are accessible below in two tabs: Basic Options and Advanced Options.

In the Basic Options tab (Fig. 6), a user can select a correctness property to be proved (either safety or liveness) with several additional options, the search mode (exhaustive, bitstate hashing or hash-compact), how a full queue behaves during verification (either blocks or loses new messages), the explicit use of user-entered compile-time and run-time parameters that supersede the clicked options and the elsewhere entered parameters, and how a never claim (if any) is specified. A never claim can be specified in four different ways. In the first one, which is a default, a never claim or an LTL formula is specified in the model itself. In the text field right to the label the name of the never claim/LTL formula to be checked against the model has to be written. Such an in-model never claim specification has been possible since Spin Version 6. The second method is to enter an LTL formula in the text field. The third one is to enter or select the file name, in which the single-line LTL formula is written. The last way to specify a never claim is to enter or select a file name with a contained never claim.

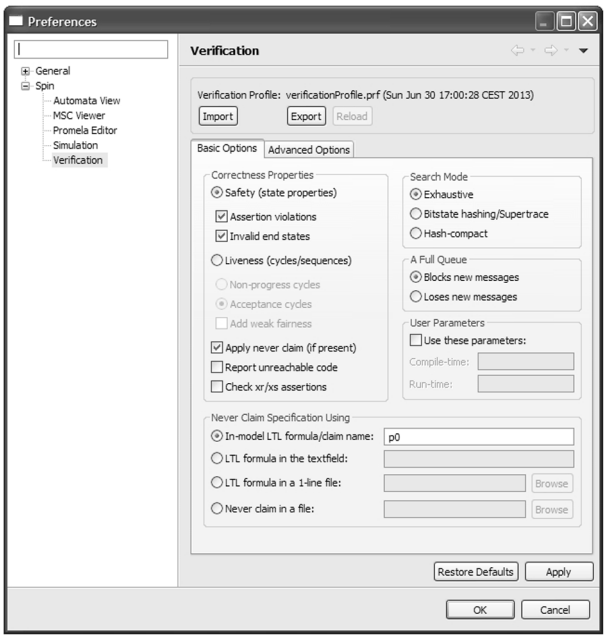

Figure 6: Basic options on the Verification preference page.

In the Advanced Options tab (Fig. 7) it is possible to enter several advanced verification parameters (the amount of the available physical memory in megabytes, the estimated state space size, the maximum search depth, number of hash-functions in bitstate mode, extra verifier generation options, extra compile-time directives, and extra run-time options) and select some error-trapping and verification run type options.

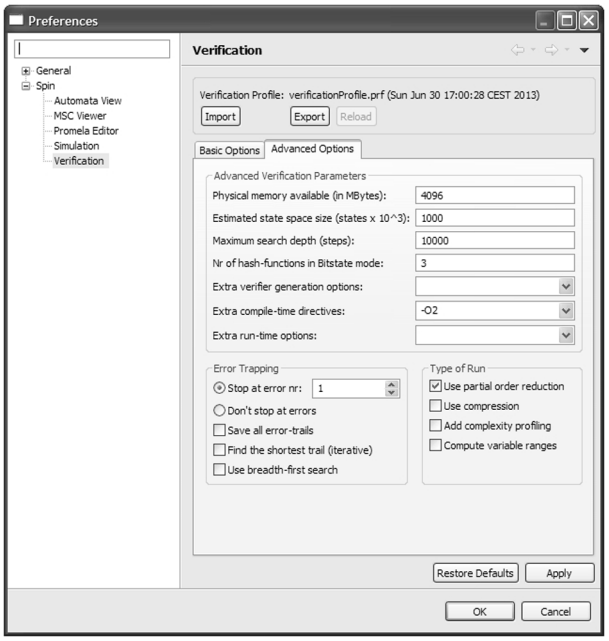

Figure 7: Advanced options on the Verification preference page.

5.8 MSC Viewer

The MSC Viewer is used for a graphical display of the Spin simulation output trail. Otherwise, as in the case of [10, 11], external (often commercial) tools would be needed to accomplish this (e.g., ObjectGEODE). The MSC Viewer is shown in the central part of Fig. 8. It works in two different modes. In the first one it displays an already generated simulation trail from a file of type out. This kind of MSC display can be achieved either by a double-click on an out file in the Model Navigator view or by a click on the Import trail button in the Tool bar when the Simulation View is active. The second mode of displaying the MSC is "on-the-fly" when the simulation is running. In this mode, two Java threads run in parallel: a Spin simulation thread and an MSC refreshing thread. The simulation thread executes the Spin simulation (random, guided, or interactive). Simulation output is parsed line by line and for each new parsed line the list of created processes and messages that have been sent and received up to this time is updated. In parallel, the MSC refreshing thread is refreshing the MSC displayed in MSC Viewer. If any new process or any new message has been added to the corresponding list since the last screen refresh, the MSC is changed accordingly. The MSC Viewer is implemented using the Graphical Editing Framework (GEF) that provides technology for creating rich graphical editors and views for the Eclipse Workbench UI.

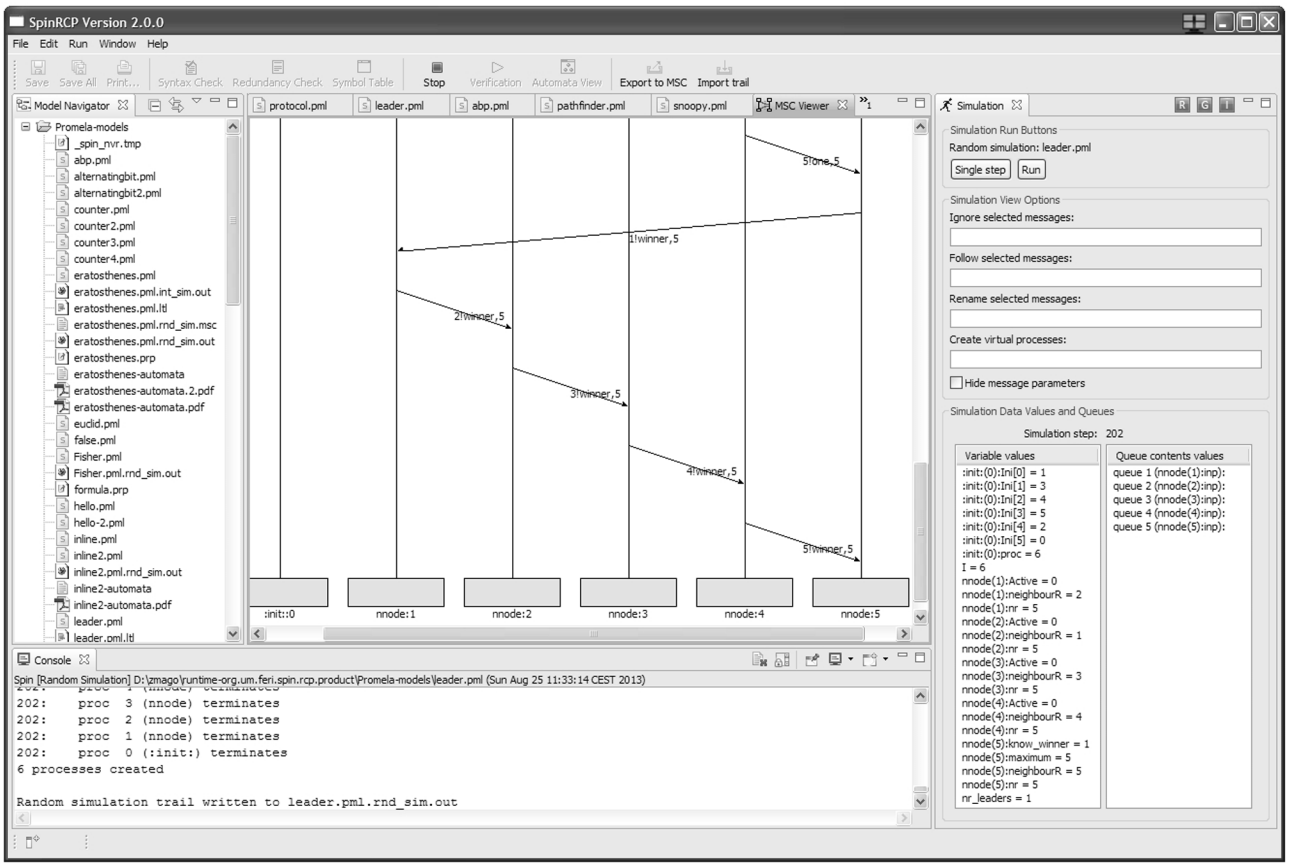

Figure 8: SpinRCP Workbench during simulation.

5.9 Simulation View

The Simulation View is shown after the Simulation button in the Tool bar has been pressed and the Simulation preference page confirmed (right side of Fig. 8). At the top of the view there is a label showing the previously-selected simulation type including the Promela model filename and two simulation buttons, Single Step and Run. By clicking the Single Step button, MSC is being drawn message by message (if any message is sent and received in the model at all). Clicking on the Run button periodically updates the MSC each time the MSC refresh interval expires as given on the MSC Viewer preference page.

Several options to adapt the display of MSCs are available below the simulation buttons. The user can do the following:

- select a subset of messages that will be ignored and not displayed in the MSC diagram,
- select a subset of messages that will be displayed in the MSC diagram,
- rename selected messages,
- join two or more processes into a new virtual process, and
- select whether to show or hide message parameters.

The first two options are very useful if we have to explore simulation traces of large models with many processes and a large number of messages, and can thus concentrate only on those that we are interested in. Selected messages are entered using their space-separated IDs. The need for renaming of messages appears when our sdl2pml tool [8, 9] has extracted a very large Promela model from an SDL code of a real product. Since Promela allows a maximum of 255 different message types, the sdl2pml tool presents messages using integers. It is very difficult to track a simulation trail if messages are represented by numbers instead of having sensible names. The renaming of messages helps, in that the MSC is more understandable. For example, to rename a message with ID 1 to one, the following command has to be entered: 1>one. To rename more messages within a single command, a space has to be entered for separating individual renamings. When we want to make an abstraction of the model, we can use a powerful feature of joining a group of processes into a virtual process. For example, the 1,2>onetwo command has to be entered in order to join processes with IDs 1 and 2 into a virtual process called onetwo. More virtual processes can be created within a single command using a space separator. The abstraction by joining processes results in a smaller number of processes in the MSC as well as in a smaller number of messages

displayed, as all messages within each group of joined processes are internal for the virtual process and therefore not shown. Parameter hiding is especially useful when reviewing simulation trails of real systems, where messages often contain many parameters that lead to less transparent diagrams.

The same set of simulation view options is also available in the Spin Trail to MSC View, which is intended for converting a Spin simulation output trail to the standard MSC text format according to [13] in the same manner that the Export to MSC command does. In addition, Spin Trail to MSC View displays a list of created processes and messages transmitted between them during the simulation run.

During the simulation run the variable values and queue contents values are updated in two separate tables at the bottom of the Simulation View. The current simulation step number is shown at the top of the tables.

6 Leader election example

Let us demonstrate some features of SpinRCP by considering a standard algorithm for leader election in a unidirectional ring. An efficient algorithm for solving this problem was published in [19]. The Promela model of this algorithm is taken from Spin Version 6 distribution.

The leader election algorithm, when given a circular arrangement of *N* uniquely numbered processes in a unidirectional ring, determines the maximum number in a distributive manner. Communication occurs only between neighbours around the ring. All processes have the same program. They differ only by having distinct numbers (known only to the owners) in their local memory.

We suppose that $N = 5$. The Promela model contains two proctype definitions: init and nnode. The init process first assigns a unique number for each of the five processes using non-deterministic choices. Then it creates five instances of a nnode process and assigns them their numbers. Next, the five nnode processes start to send and receive messages around the ring and process them according to the algorithm. A process terminates when it recognizes whether it is a leader (has the greatest number in a ring) or not.

A global variable nr_leaders is defined and initialised to zero in line 26. In lines 28 through to 31, four required properties for the algorithm are specified with the following LTL formulas:

```
p0: <> (nr_leaders > 0)
p1: <>[] (nr_leaders == 1)
p2: [] (nr_leaders == 0 U nr_leaders == 1)
p3: ![] (nr_leaders == 0)
```

Such in-model specification of LTL properties has been supported since Spin Version 6. They state "positive" properties. Spin performs the negation automatically.

After a successful syntax check, eventual redundancy check and/or listing of a model symbol table, it is useful to become more acquainted with the model. For this purpose we can first generate and display a graphical representation of a state transition system (an automaton) for each proctype and never claim in the model. By clicking the Automata View button in the Tool bar, the Automata View preference page (Fig. 4) opens and gives us the choice of selecting the type of files that will contain the automata. Let us suppose that we select the pdf file type (as in Fig. 4). Then the following sequence of commands is executed:

```
spin –o3 –a leader.pml
gcc-4 –o pan pan.c
pan –D | dot>leader-automata
dot –O –Tpdf leader-automata
```

The first command generates the verifier source code for the model leader.pml without statement merging, the second one compiles it, the third one writes state tables in dot-format to leader-automata file, and the last one creates a pdf file with the automaton for each proctype and never claim. Now a new selection dialogue is open and we can select, which automaton we want so see. Each selected automaton is opened in a system application that is assigned for a given file type. Let us suppose that we want to see the automata for nnode, p0, p1, and p2. To save space, all of them are placed together in Fig. 9.

In order to deepen understanding of the model and perhaps to find some early (simple) errors before verification, it is wise to perform random and/or interactive simulation. In random simulation, Spin decides by itself, as to which one of the executable statements will be chosen at the points of non-deterministic selections. In interactive simulation, these decisions have to be made by a user. Fig. 8 shows the content of the console, the MSC Editor window, and the Simulation View on completion of the random simulation of the leader.pml model. At the bottom of the *Variable values* table in the Simulation View it is evident that the nr_leaders variable is given the final value 1.

We may want to prove several interesting properties about this algorithm but one of the most important

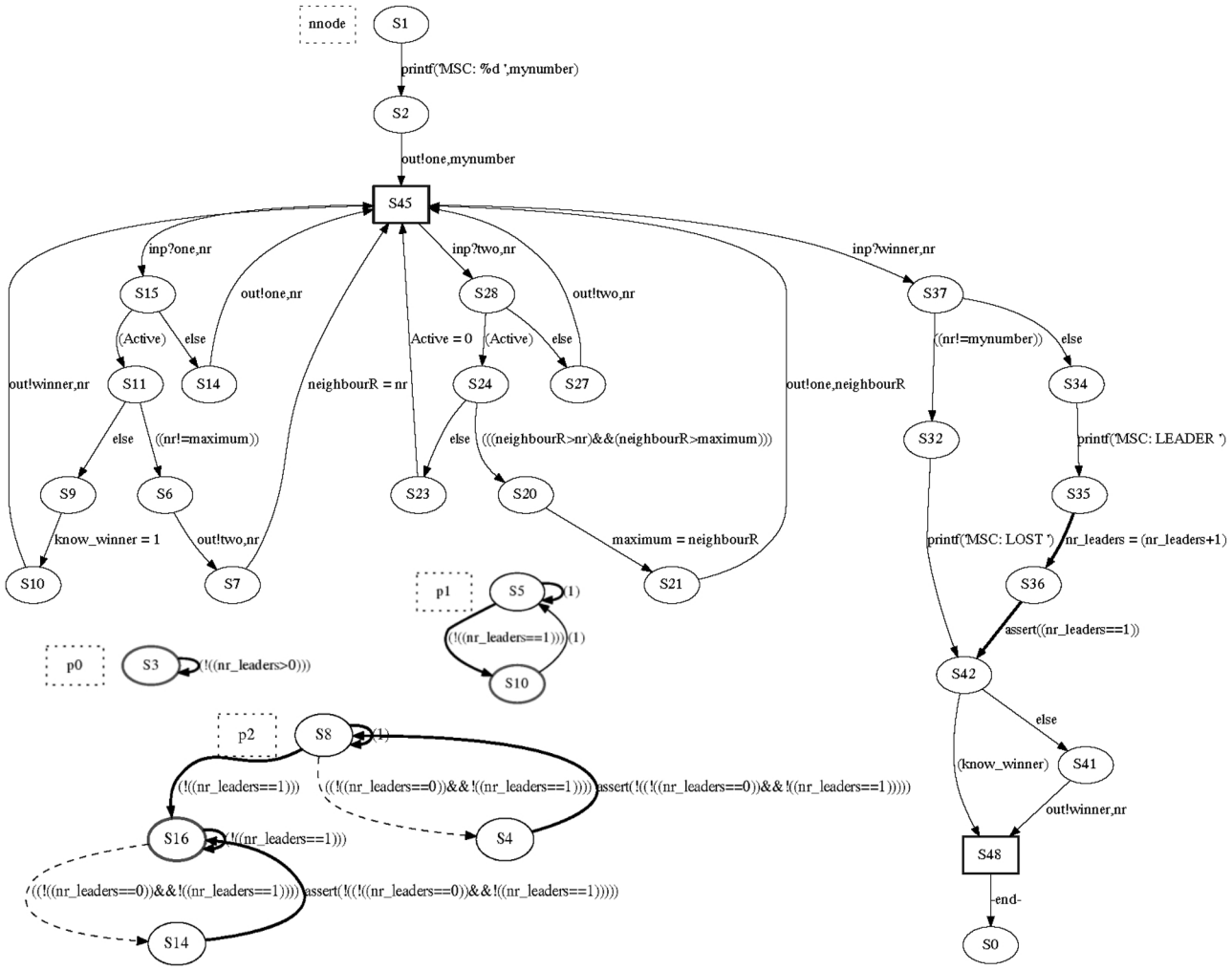

Figure 9: Automata for nnode, p0, p1, and p2.

seems to be the property that under no conditions should it be possible that more than one process declare to be the ring leader.

Firstly, let us check p0, i.e., that eventually the number of leaders is greater than 0. By clicking the Verification tool button, the Verification preference page (Fig. 6) is displayed. Since p0 specifies a liveness property, we must select the *Liveness* and *Acceptance cycles* radio buttons. Next, we select *Apply never claim* and as a manner of never claim specification select *In-model LTL formula/claim name*. Finally, we enter the name of the in-model LTL formula, p0, in the text field to the right of the label. As a result of verification, Spin returns that no error is found (i.e., the model fulfils the property p0) (see the Console in Fig. 2). But it is as yet unclear whether the algorithm will eventually always give one single leader. In order to verify this, we check if the model fulfils p1, i.e., if eventually the number of leaders will always be 1. Therefore, this time we enter p1 as the LTL formula name and run the verification again. Spin finds no errors, which means that the model fulfils p1. Now the only doubt about the correctness of the algorithm that still exists is whether the number of leaders goes from 0 to 1 directly with no intermediate numbers greater than 1. In order to find out the answer to this question, we check whether the system fulfils p2 as well, i.e., the number of leaders is always 0 until the number of leaders is 1. The new verification run succeeds and thus p2 is verified. p3 specifies that the number of leaders is not always zero. This means that eventually the number of leaders is not zero. Since this number cannot be negative, p3 means exactly the same as p0, and is thus already verified.

7 Conclusions

Using the Spin model checker on a huge model, automatically extracted from the SDL code of a real telecommunication industry product, encouraged us to develop an integrated development environment for Spin model checking called SpinRCP. SpinRCP is based on the Rich Client Platform technology. It is written in

Java as an Eclipse plug-in and then exported together with many other plug-ins as an Eclipse product. Therefore, it runs as a stand-alone RCP application on any platform without the need for an installed Eclipse but nevertheless has many of the useful Eclipse functionalities.

The whole application consists of 92 plug-ins. The Java source code for our plug-in called org.um.feri.spin.rcp is contained in 19 Java packages with a total of 84 files defining Java classes. The total amount of our source code is around 16,800 lines of Java code. The help contents for SpinRCP is implemented in a separate plug-in that contains more than 60 html files with descriptions of individual help topics and many xml configuration files. Currently, SpinRCP runs on 32- and 64-bit Windows operating systems. Platforms with other operating systems will be supported later. Once the website for SpinRCP is ready, it will be publicly announced.

Amongst the more important features of SpinRCP are the following ones: a user-friendly Promela editor with syntax colouring, code folding, keyword autocompletion, and syntax error marking, running Spin verification, random, guided, and interactive simulation, graphical MSC viewing, abstracting MSCs by joining some processes into an abstract process, conversion of Spin simulation output trail to a standard text file, which is readable by professional MSC viewers, displaying graphical automata representation of proctype definitions and never claims in a model.

There are still a lot of ideas for improvements and new features. Let us mention just some of them: better Spin simulation output filtering, stepping back in time during single step simulation, indication of the statement that is currently executed during a simulation run in the Promela source file, display of a process creation in the MSC Viewer, generation of state tables for proctype definitions and never claims, cleanup of temporary files, verification management, swarm support [15] for distributing a model checking task to more CPU cores or to a cloud of workstations, etc.

APPENDIX A

```
1   /*  Dolev, Klawe & Rodeh for leader election in
    unidirectional ring
2   *  `An O(n log n) unidirectional distributed algo-
    rithm for extrema
3   *  finding in a circle,' J. of Algs, Vol 3. (1982), pp.
    245-260
4
5   *  Randomized initialization added -- Feb 17, 1997
6   */
7
8   /* sample properties:
9   *  <>elected
10  *  <>[]oneLeader
11  *  []  (noLeader U oneLeader)
12  *  ![]  noLeader
13  *
14  *  ltl format specifies positive properties
15  *  that should be satisfied -- spin will
16  *  look for counter-examples to these properties
17  *  verify as:
18  *  spin -a leader.pml
19  *  cc -o pan pan.c
20  *  ./pan -N p0
21  *  ./pan -N p1
22  *  ./pan -N p2
23  *  ./pan -N p3
24  */
25
26  byte nr_leaders = 0;
27
28  ltl p0  { <> (nr_leaders > 0) }
29  ltl p1  { <>[] (nr_leaders == 1) }
30  ltl p2  { [] (nr_leaders == 0 U nr_leaders == 1) }
31  ltl p3  { ![] (nr_leaders == 0) }
32
33  #define N 5 /* number of processes in the ring */
34  #define L 10 /* 2xN */
35  byte l;
36
37  mtype = { one, two, winner };
38  chan q[N] = [L] of { mtype, byte};
39
40  proctype nnode (chan inp, out; byte mynumber)
41  { bit Active = 1, know_winner = 0;
42   byte nr, maximum = mynumber, neighbourR;
43
44   xr inp;
45   xs out;
46
47   printf(„MSC: %d\n“, mynumber);
48   out!one(mynumber);
49  end:  do
50     :: inp?one(nr) ->
51       if
52       :: Active ->
53         if
54         :: nr != maximum ->
55           out!two(nr);
56           neighbourR = nr
57         :: else ->
58           know_winner = 1;
59           out!winner,nr;
60         fi
61       :: else ->
62         out!one(nr)
```

```
63        fi
64
65      :: inp?two(nr) ->
66        if
67        :: Active ->
68          if
69          :: neighbourR > nr && neighbourR > maxi-
    mum ->
70            maximum = neighbourR;
71        out!one(neighbourR)
72          :: else ->
73            Active = 0
74          fi
75        :: else ->
76          out!two(nr)
77        fi
78      :: inp?winner,nr ->
79        if
80        :: nr != mynumber ->
81          printf(„MSC: LOST\n“);
82        :: else ->
83          printf(„MSC: LEADER\n“);
84          nr_leaders++;
85          assert(nr_leaders == 1)
86        fi;
87        if
88        :: know_winner
89        :: else -> out!winner,nr
90        fi;
91        break
92    od
93  }
94
95  init {
96    byte proc;
97    byte Ini[6];/* N<=6 randomize the process
    numbers */
98    atomic {
99
100     I = 1; /* pick a number to be assigned 1..N */
101     do
102     :: I <= N ->
103       if  /* non-deterministic choice */
104       :: Ini[0] == 0 && N >= 1 -> Ini[0] = I
105       :: Ini[1] == 0 && N >= 2 -> Ini[1] = I
106       :: Ini[2] == 0 && N >= 3 -> Ini[2] = I
107       :: Ini[3] == 0 && N >= 4 -> Ini[3] = I
108       :: Ini[4] == 0 && N >= 5 -> Ini[4] = I
109       :: Ini[5] == 0 && N >= 6 -> Ini[5] = I /* works
        for up to N=6 */
110       fi;
111       I++
112     :: I > N -> /* assigned all numbers 1..N */
113       break
114     od;
115
116     proc = 1;
117     do
118     :: proc <= N ->
119       run nnode (q[proc-1], q[proc%N], Ini[proc-1]);
120       proc++
121     :: proc > N ->
122       break
123     od
124   }
125 }
```

Acknowledgments

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Signal Processing for Integrated, High Performance, Low Noise Chemical/Biological Sensor Interface

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Abstract: The article presents miniature detection system and its associated signal processing electronics, which can detect and selectively recognize vapor traces of different materials including explosives. It is based on surface-functionalized COMB capacitive sensors and extremely low noise analog integrated electronic circuit, hard-wired digital signal processing and additional software running on the PC. The instrument is sensitive and selective, consumes minimum amount of energy, is very small (few mm3) and cheap to produce in large quantities, and is insensitive to mechanical influences. Using electronic detection system built of low noise analog front-end and hard-wired digital signal processing, it is possible to detect less than 3ppt of TNT molecules in the atmosphere (3 TNT molecules in 10^{12} molecules of the air) at 25 °C in 1 Hz bandwidth using very small volume and approx. 10 mA current from 5 V supply voltage. The sensor is implemented in modified MEMS process and analog electronics in 0.25 um CMOS technology.

Keywords: Chemical/Biological Sensor interface, Low noise signal processing, high performance integrated sensors

Signalno procesiranje za integriran, visokozmogljiv nizkošumni vmesnik za kemijske/biološke senzorje

Izvleček: Članek predstavlja miniaturni detekcijski sistem in pripadajoče integrirano elektronsko vezje, ki selektivno zaznava pare različnih materialov vključno s parami eksplozivov. Bazira na površinsko modificiranih COMB kapacitivnih senzorjih in nizkošumnem analognem integriranem vezju, skupaj z digitalnim procesorjem signalov in programsko opremo na PC računalniku. Instrument je zelo občutljiv, selektiven, porabi malo električne energije za svoje delovanje, je zelo majhen (nekaj mm3), je neobčutljiv na mehanične in temperaturne vplive in ga je mogoče ceneno proizvajati v velikih količinah. Z uporabo predstavljenega nizkošumnega procesiranje signalov je mogoče zaznati manj kot 3 TNT molekule v 10^{12} molekulah nosilnega plina ali v atmosferi pri 25 °C in v 1 Hz pasovne širine. Instrument ima majhen volumen ter porabi približno 10 mA toka pri napajanju 5 V. Senzor je izdelan v modificiranem MEMS procesu, analogni del elektronike pa v 0.25 um CMOS procesu.

Ključne besede: kemijski/biološki sezorski vmesniki, nizkošumno procesiranje signalov, visoko občutljivi integrirani senzorji

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1 Introduction

Detecting vapor traces of different materials including explosives in the atmosphere is a potentially powerful method to reveal the presence of different toxic materials, explosives and land mines. The principle of detection method is based on the fact that most materials, including explosive devices, constantly emit rather small, but detectable number of different molecules, constituting the material. Numerous detection systems on the market are capable of detecting vapor traces of explosives [1]. Their common limitations are rather large size, high power consumption, unreliable detection with false alarms, insufficient sensitivity and chemical selectivity or hypersensitivity to mechanical influences, long time needed for detection and extremely high price.

Currently, the most popular method for detection of vapor traces of target molecules is the chemo-mechanical sensor system based on cantilever bending, caused by adsorption of target molecules on asymmetrically modified surface. Bending is measured with optical

or electrical detection [2]. Optical cantilever position measurements are difficult; the apparatus is bulky and sensitive to the environmental influences like temperature, vibrations, pressure etc.; the integration and miniaturization is not possible. In this work, we present the detection system that measures the change of the capacitance caused by adsorption of target molecules to the surface of functionalized miniature MEMS capacitors with fixed COMB fingers; the environmental problems described above for the cantilever based sensors are completely eliminated. The adsorption of target molecules on functionalized surfaces of the fixed COMB capacitors causes the change of the dielectric constant of the monolayer between the plates of the capacitor. This extremely small change can be measured with extremely sensitive electronic measurement system described in this article.

The paper is organized as follows. In section 2, the principles of operation of the capacitive COMB sensor is shortly described to understand the requirements for the electronic measurement system. Section 3 deals with system design and modeling issues, while section 4 presents most important circuit design steps together with sensitivity estimates. Section 5 describes high level modeling and simulation results of the circuit which includes analog, mixed signal and digital modules. Section 6, presents responses of the detection system to the TNT and RDX vapors, the detection limits are calculated and compared to the estimates from the system level simulation results. Measured results are compared to the state of the art detection systems.

2 Sensor operation

The detection measurement system is composed of four differently functionalized differential COMB capacitive sensors (Fig. 1) connected to one channel of the low -noise analog electronic measurement system, followed by the DSP as presented on Fig. 2.

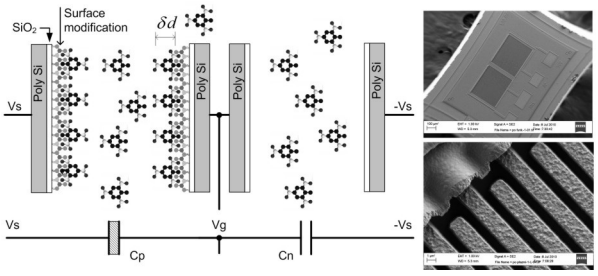

Figure 1: Comb capacitive sensor implemented in 1um MEMS process: (Left) COMB capacitance change due to adsorption of the target molecule in the air. (Right) SEM micrograph of a differential COMB capacitor and the detail of its structure.

The principle of sensor operation is presented on the left part of Fig. 1. Each sensor is composed of a pair of COMB capacitors implemented in modified MEMS technology (SEM micrograph is shown on the right side of Fig. 1), where the fingers are not released from the bottom oxide. Both capacitors are covered with approx. 15 nm of silicon dioxide [3]. One capacitor in each pair is chemically functionalized with different organosilanes (APS, APhS or UPS) [4] to [5], as shown symbolically on the left part of Fig. 1 (shaded symbol of functionalised capacitors). For example, C_p is modified while C_n is not. During operation, on average, approx. equal numbers of target molecules are present in the space between the plates of both capacitors. Other molecules are also present in the air around both sensors; again, the density of all the molecules is on average distributed equally between capacitors and the capacitance difference is the same. The target molecules adsorb preferentially [7] to the surface of the C_p and change the relative dielectric constant between the plates, while C_n remains the same. Using differential excitation signal V_s, connected to both capacitors, one can measure the difference of the two capacitances caused by adsorbed target molecules. Each capacitor consists of 50 fingers with length of 350um, height of 2um and the distance between the fingers of approximately 1.5um, thus forming two capacitors, each having a capacitance of approximately 0.4 pF with matching accuracy better than 5%, which is reduced by automatic calibration procedure before every measurement. At the moment, each differential sensor is produced and functionalized individually, while the modification layer is removed from one half of each differential pair using laser erosion procedure. In the near future, we plan to build an array of differently and selectively modified sensors on top of the ASIC chip to reduce the parasitic effects caused by bond-wires and parasitic capacitances and thus to increase the sensitivity.

3 Measurement system

Fig. 2 shows simplified block diagram of the sensor measurement system that includes low-noise analog signal processing electronics implemented in 0.25um CMOS process together with four differently modified sensors, one channel of remaining analog signal processing electronics (AFE) and the digital signal processing block (DSP) in the gray area of Fig. 2. The DSP is currently implemented on the FPGA but in the future it will be implemented on-chip. The system architecture is in fact a multi-frequency lock-in amplifier where necessary part of the signal processing happens in the block of analog signal processing (AFE) and the rest using digital signal processing (DSP). The AFE consists of minimum amount of necessary analog electronics to

convert extremely weak capacitive changes to the digital stream. The AFE is programmable in many ways, so it can be adapted to different signal levels, frequencies, sensors etc. Each sensor is driven by a high frequency differential square-wave signal V_{si} with slightly different and adjustable frequency and amplitude. The capacitors of the first sensor are driven with differential square-wave signal V_{s1} with frequency f_{s1}, the capacitors of the second sensor are driven with differential square-wave signal V_{s2} with frequency f_{s2} and so on. One channel of the analog front-end electronics (AFE) serves at the moment for four sensors and consists of: two low noise single-ended charge amplifiers, low noise BP filter, analog mixer, 4th order low pass filter, 2nd order $\Delta\Sigma$ modulator with one-bit internal quantizer and multi-bit DACs built as analog FIR filter. The excitation signals are delivered to the sensors as a four low noise analog differential signals. The signal at the output of the charge amplifier, when all four sensors are present, is composed of four spectral components and their odd harmonics. The amplitude of each spectral line corresponds to one sensor and is proportional to the difference of the corresponding differential sensors capacitance and the amplitude of the corresponding excitation signal (1). Different sensors are driven with square-waves with slightly different frequencies. The amplitude of each spectral component carries the information about the difference ΔC of each sensor. The starting capacitance difference of each sensor is adjusted to be small during automatic calibration procedure at the beginning of the measurements. After adsorption of target molecules, the capacitance changes so the amplitude of the main spectral component changes. At the moment, one measurement channel can process signals from four differential sensors that might be functionalized differently. The idea behind the array of the sensors is that differently modified sensors show different responses to the target and other molecules in the air, producing a "signature" of the responses, which could improve the selectivity and sensitivity of the sensor system.

The difference in charges from each capacitive pair is transformed into the voltage using low noise charge amplifier through the use of excitation signals connected to the sensors. The frequencies are selected well above the flicker noise corner of the charge amplifier that is in the range of several 100 kHz for modern CMOS process [8]. Each sensor pair is driven with a differential square wave signal V_{sj}, producing charge amplifier output signal with amplitude given in (1), where $\Delta C = C_p - C_n$, V_s is the excitation voltage amplitude and C_f is the feedback capacitance of each amplifier. To remove unwanted components, the signal V_{cho} is band-pass filtered, amplified and multiplied with coherent square-wave signal with frequency f_m generated in the DSP. The spectrum after the passive mixer is a reach composition of sums and differences of all fundamental spectral components and their odd harmonics. Since amplified and filtered signals at the output of the band-pass filter contain main spectral components and attenuated higher harmonics, the analog mixer generates the differences and sums of the main spectral component frequencies and many high frequency spectral components.

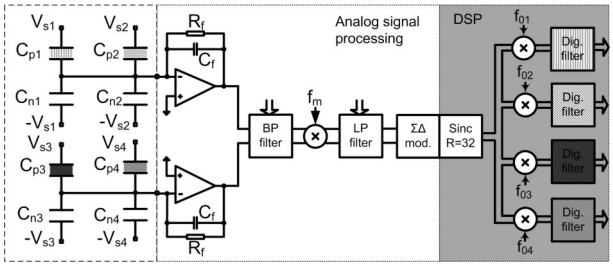

Figure 2: Block diagram of a complete sensor measurement system including 4 sensors, one measurement channel and corresponding DSP implemented in the FPGA.

The differences of the first harmonics happen at frequencies: $f_{oi} = f_{si} - f_m$ (i=1…4). They are amplified, while HF components with frequencies $f_{oi} = f_{si} + f_m$ (i=1…4) and other remains of higher harmonic signals mixing products are attenuated by programmable analog LP filter, which also adapts the level appropriate for the ADC. The frequencies f_{si} and f_m are selected in such a way that they are coherent [9], the components after mixing have different frequencies and the higher order products do not fall into the base-band. The composed signal is quantized using second order Σ-Δ modulator and a 3rd order sinc decimation filter with down-sampling ratio of 32. To speed up the detection process and avoid the problems of non-coherency, it is extremely important that all signals used for driving, mixing, down-sampling and timing of further filtering are strictly coherent, that is, the measurement period is a multiple of every signal period generated in the circuit and that their ratios are prime numbers [9]. To be able to generate coherent signals, the decimation ratio is small in the first decimation stage; the remains of the out-of-band signals and shaped quantization noise are further filtered in each channel after digital mixing with f_{oi} as suggested in the DSP block on the right side of the block diagram shown on Fig. 2. The spectrum at the output of the first sinc filter consists of four spectral components at frequencies f_{01} to f_{04}, with amplitudes proportional to the corresponding sensor capacitance difference and excitation signal amplitudes. This digital signal is than multiplied in four separated digital multipliers, each with a digital sine-wave with frequencies f_{01} to f_{04}, translating corresponding signals to the DC. Each DC digital signal is than separately filtered in the DSP

to remove all remains of high frequency components. Each DC result is proportional to the difference of differential capacitances of each sensor and the excitation signal amplitude. The digital signal processing at DC is possible without compromising the signal quality. The bandwidth is reduced to approx. 10Hz in corresponding LP digital filter. The remains of the second mixing process are highly attenuated by appropriate positions of poles and zeroes of the digital LP filters. The results of all channels are transferred to the PC where further filtering and decimation takes place, reducing the effective bandwidth of each channel down to 1Hz or even more if necessary. The results are stored for further processing and presented on the screen of the PC.

Excitation signals transfer the information from slowly varying sensor capacitances, due to slow adsorption-desorption process, to the trans-impedance charge amplifier at frequencies that are well above the corner frequency of the flicker noise. The whole measurement system looks like a modified lock-in amplifier [10] using double mixing architecture to sense and amplify the signals at high frequencies and thus to avoid 1/f noise and DC offset effects in analog modules. All signals are coherent and selected in such a way that the ratio of f_{dec1}/f_{oi} is even integer. They are derived from one master clock with frequency f_{clk}=*25MHz*. Possible selection of the excitation signal frequencies for 4 sensors are: f_{s1}=*208.3kHz*, f_{s2}=*183.8kHz*, f_{s3}=*201.6kHz* and f_{s4}=*189,3kHz*. Multiplying signals at the output of the BP filter with square-wave signal with frequency f_m=*195,3kHz* generates the differences and sums of the first harmonics and also other higher harmonics that are LP filtered. The main spectral components after mixing are at frequencies: f_{o1}=*13.02kHz*, f_{o2}=*11.5kHz*, f_{o3}=*6.3kHz* and f_{o4}=*5.9kHz*. This arrangement makes possible to use one analog channel and to avoid the DC offset and remaining 1/f noise effects in analog LP filters and the Σ-Δ modulator and makes possible to reduce the sampling frequency and thus reduced power consumption. It would also be possible to use HF chopping at each component at the expense of increased thermal noise effects, which means worse SnR and worse detection sensitivity. Since the adsorption-desorption process is slow process (in the range of several s), the offset voltage and 1/f noise would compromise the accuracy and the stability of the results if DC excitation signals would be used; the "DC" signal-processing happens in the DSP where no physical noise process can reduce the SnR of the results.

4 Circuit design

The decisive parameter regarding detection sensitivity of the measurement system is the S/N ratio at the charge amplifier output. Fig. 3 shows simplified model of the charge amplifier with most important noise contributions, together with simplified model of one sensor and associated parasitic capacitances. The circuit implementation details of the charge opamps and the feedback resistors R_f are not shown because of the lack of space. The feedback capacitance of the charge amplifier is C_f=*1.5pF*, while small signal resistance of the feedback resistor is very high R_f>*10GΩ*; the pole frequency of the charge amplifier is low enough not to influence the behavior of the spectral components and the noise contributions of the R_f is small enough around the lowest excitation signal frequency of *180kHz*. The R_f is built as electronically tunable linear MOS resistor [11] that can be adjusted to have a very high resistance (bigger than *10GΩ*). Each charge amplifier use differential, folded-cascode architecture with single ended output reaching input referred noise density of less than *15nV/√Hz* at *200 kHz*. Two single ended amplifiers are used to be able to keep the potential of the sensing capacitors fixed. BP filter uses fully differential opamp with similar characteristics; its input signal is a difference of both charge amplifier signals. From this point on, the analog signal processing is fully differential. The most important noise contributors are: Noise V_{ndop} is the opamp noise and is multiplied with noise gain $G_{ndop} \cong \left(1+\sum C_{vg}/C_f\right)$, where $\sum C_{vg}$ is the sum of all capacitors connected to the virtual ground of the opamp and C_f is the feedback capacitor of the charge amplifier; Input referred noise density of the BP filter is V_{ndBP}; the noise density of the feedback resistor V_{ndRf}, which is attenuated by its frequency transfer function $\left|H_{R_f}(\omega_s)\right|$; the noise density of the excitation signal sources V_{ndsp} and V_{ndsn} are multiplied by excitation signal gain $G_s \cong C_s/C_f$.

The SnR at the output of the charge amplifier can thus be calculated using (1) and (2).

$$V_{cho} \cong V_s \cdot \left(\Delta C/C_f\right) \tag{1}$$

$$V_{ndCho}^2(f_{oi}) \cong \left[V_{ndop}G_{nd,op}\right]^2 + V_{ndBP}^2 + 2\cdot\left[V_{ndS}G_s\right]^2 + \\ + kTR_f \cdot \left|H_{R_f}(\omega_{oi})\right|^2 \tag{2}$$

Equation (1) estimates the signal at the charge amplifier output while (2) estimates the noise power density at the output of the charge amplifier around frequency f_{oi} assuming thermal noise approximation. The pole frequency formed by C_f, R_f must be much lower than the signal frequency f_{oi} to avoid attenuation and phase shift of the main spectral components. In addition, noise contributions of the R_f at low frequency are highly attenuated by the noise transfer function $\left|H_{R_f}(\omega_s)\right|$. The total noise power density at the output of the charge amplifier around signal frequency f_{oi}

is composed of all contributions. The biggest contribution is the charge amplifier noise density V_{ndop} multiplied by associated gain $G_{nd,op}$. Usually, contributions of all other noise sources in a low-noise measurement system are selected in such a way that they are smaller or equal to the charge amplifier contribution because this is the most difficult and expensive to reduce. The estimate of the detectable capacitance difference of one sensor can be calculated using (3) assuming: SnR=6dB, noise bandwidth is 1Hz, noise density of the opamp $V_{ndop}(f_{oi}) \leq 15nV/\sqrt{Hz}$, excitation signal amplitude $V_s = 4V$, $C_f = 1.5pF$ and the sum of all capacitors connected to the virtual ground of the opamp is equal to $\sum C_{vg} = 2.5pF$. Factor four in (3) comes from analogue and digital mixers (each contributes approx. $\sqrt{2}$ [12]), while another factor 2 comes from the peak to rms conversion (factor $\sqrt{2}$) and noise contributions from all other sources including the excitation signal generators. One can estimate minimum detectable capacitance change of the modified COMB capacitor caused by the adsorption of target molecules using (3); it is assumed that adsorbed molecules do not change the dielectric constant of the modified capacitor significantly.

$$\delta C \cong (4/V_s) V_{ndop} \left(C_f + \sum C_{vg} \right) = 0.06 \left[aF/\sqrt{Hz} \right] \quad (3)$$

$$d_m \cong \left(d_0 \cdot \delta C / (C_0) \right) = 120 \ fm \quad (4)$$

Equation (4) gives the minimum detectable COMB capacitance distance change, which is $120\,fm$. This distance change is well below the thickness of the one layer of adsorbed target molecules, estimated to be approx. 0.5nm for the TNT [2].

5 System level modeling

The electronic measurement system was modeled using Matlab/Simulink. The concept, sensitivity, selectivity, and functionality of the analog and digital signal processing modules and sensors operation were checked. Most important non-ideal effects of the analog measurement channel modules were taken into considerations [14]: non-linearity, thermal noise, 1/f noise, kT/C noise, offset voltages, gains, gain bandwidth products, slew-rates, distortions, as well as a bit-true models of all DSP modules. The system level simulation results match very well to the circuit level simulation results and to the measurements of the real circuit.

The system level optimization and simulation is very efficient because of high level model. Fig. 4 shows simulated spectrum at the output of the Σ-Δ modulator for 2 sensors connected to the charge amplifier with capacitance difference of 1*fF* for the first pair and 0.1*fF* for the second pair. The detection levels from system simulation results are very close to the estimates given in (3) and to the measured results. On Fig. 4, two main spectral components could be observed, each of them corresponding to associated sensor capacitance difference. The amplitude of the main spectral component at 11kHz is proportional to the capacitance difference of 1*fF* with SnR1=62.7dB in 200Hz band, while the SnR2 is 20 dB smaller because of 10 times smaller capacitance difference. The result lead to the sensitivity of 0.037aF/√Hz (The noise contributions from the excitation signals are not included in the model, so the result is approx. √2 better than predicted by (3) and calculated from the measurements. High frequency components and shaped quantization noise are attenuated in the following decimation filters and DSP blocks, currently implemented on the FPGA. The digital part of the signal processing is also modeled in Simulink using bit-true models, so eventual finite word-length effects could be clearly observed. The Simulink models of the DSP blocks are used to synthesize the VHDL description of the DSP blocks directly from the models [15], while the analog part of the signal processing is designed "manually" using the information from the Simulink model as a specification for the circuit design parameters; in this way the total design time is drastically reduced, while increasing the reliability of the design.

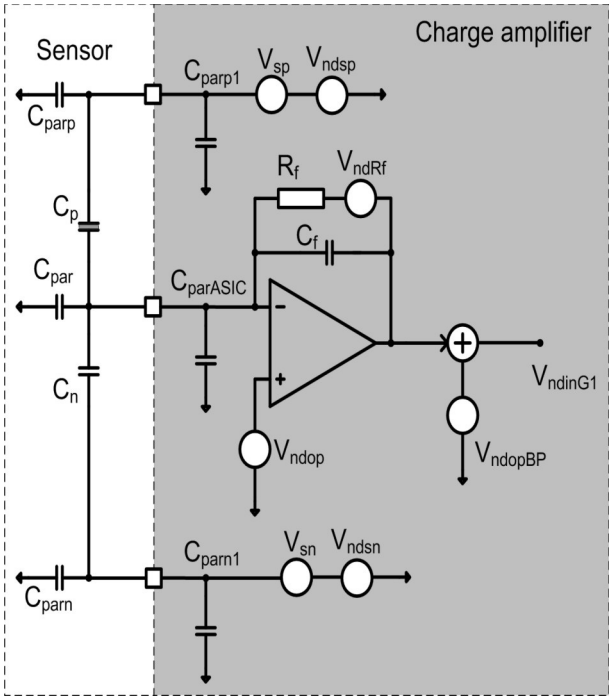

Figure 3: Noise sources of the input electronics of the AFE.

6 Measurements

For laboratory measurements the PCB with System in Package (SiP) demonstrator was built as shown on the right part of Fig. 5. It is composed of the ASIC (left part of Fig. 5) and four differently modified differential sensors. During experiments, the package is covered with metal cover that seals the sensors completely. The cover has 2 holes; the mixtures of gases is delivered from the gas generator via one hole and expelled through another. In laboratory experiments the gas coming to the sensor surface is switched between dry N_2 gas and N_2 contaminated with TNT vapor molecules. At room temperature, the density of target molecules relative to the N_2 molecules is in a range of X_{targ}=10^{-9} [2] dependent on the pressure, temperature etc.

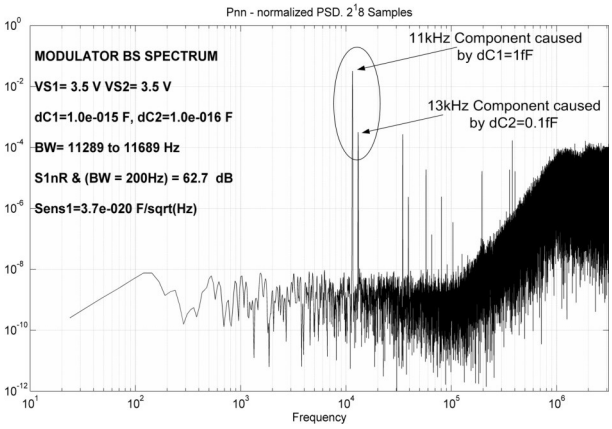

Figure 4: Spectrum at the output of the analog front-end for 2 sensors. Spectral line at 11 kHz is proportional to ΔC_1=1*fF*, while spectral line at 13kHz is caused by ΔC_2=0.1*fF* . Signal-to-noise ratio (SnR) is calculated for the main spectral line for 200Hz bandwidth, while Sensitivity Sens1 is valid for 1Hz band.

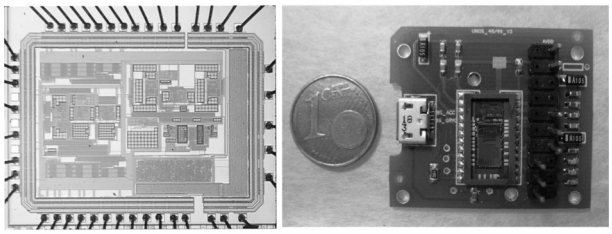

Figure 5: ASIC and SiP: (left) Photomicrograph of the ASIC in 0.25um BCD technology, (right): PCB with SiP (ASIC and 2 differential sensors).

Fig. 6 shows response of one measurement channel to the gas switched between N_2 and N_2 contaminated with TNT (estimated number of TNT molecules in the mixture is $0.5 \cdot X_{targ}$). From Fig. 6 it is possible to estimate the normalized sensitivity S_{TNT} in 1 Hz band using (5), where: ΔN is the difference between two readings, σ is the standard deviation of each reading (result), *BW=12Hz* (after DSP filtering).

$$S_{TNT} \cong \frac{0.5 \cdot X_{t\arg} \cdot \sigma}{\left(\Delta N_{TNT} \sqrt{BW}\right)} = \frac{3.5 \cdot 10^{-12}}{\sqrt{Hz}} \quad (5)$$

The lower level of the response on the y axis of Fig. 6 is proportional to the difference between capacitors after the calibration, while the change due to adsorbed molecules is proportional to ΔN . Long measurement times are produced by slow gas flow and big non-functional volume of the tubes. The sensitivity to the author's knowledge is still 2 to 3 orders of magnitude worse than the sensitivity of a dog's nose [3]. Currently, the selectivity measurements show that differently modified sensors provide different responses to the target and other molecules; this fact can be used to improve the selectivity. To the author's knowledge the system with comparable characteristics and using only available commercial technologies does not exists. Research papers regarding explosive vapor trace detection exists, for example [2], with comparable sensitivities but they use exotic technologies that are far away from possible industrialization.

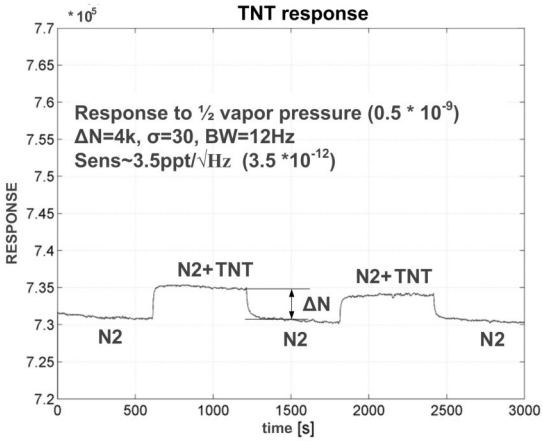

Figure 6: Measured response of the N_2 and N_2 +TNT switching.

The first experimental measurements were performed also in the air for RDX vapors. The results are presented on Figure 7. Four differently modified sensors (APS, APHS, UPS, Reference) were exposed to the vapors of RDX in the air using a tube with topped RDX material. The tube on the left bottom picture is closed than in the middle it is opened, and on the right it is closed again. The sensors measurement system shows the screen of the PC with different responses of differently modified sensors as a function of time. We can see that differently modified sensors show different results and

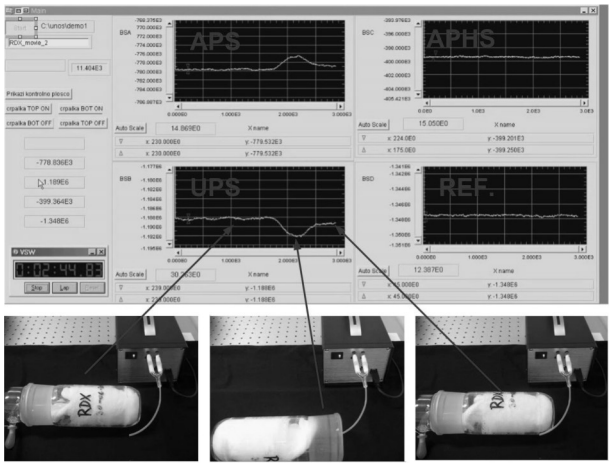

Figure 7: Measured responses of 4 differently modified sensors to RDX vapors in the air

no response is observed on reference sensor that is not modified at all.

7 Conclusions

Detecting vapor traces of different materials in the atmosphere is a potentially powerful method to reveal the presence of those materials. In this article, a miniature sensor detection system has been presented that is capable to detect vapors of different explosives. It is sensitive, selective, consumes a minimum amount of energy (10mA at 5 V), is very small and cheap to produce in large quantities and it is insensitive to mechanical influences. In laboratory environment, the response to TNT and RDX vapors has been measured. The detection levels for TNT of 3ppt and for RDX of 0.3ppthas been achieved. In the future, we plan to use large integrated array of differently modified sensors with improved individual sensitivities. This could lead to miniature, cheap and very selective detection system that could be massively deployed for detection of different hazardous molecules in the air. Measurement results in real environment are presented for RDX vapors. We have tested the sensitivity of the APS modified sensor to vapor traces of RDX with even better sensitivity than for TNT. Future work will be directed towards improving the sensitivity and the selectivity: changing the sensor geometry, reducing the analog channel noise and the parasitic capacitances of the ASIC and the sensors, increasing the number of differently modified sensors in the array and applying signature analysis algorithms to the results. We could come closer to dog's nose sensitivity and selectivity by one to two orders of magnitude using suggested modified MEMS COMB sensors and standard modern CMOS technology.

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On-line Testing and Recovery of Systems with Dynamic Partial Reconfiguration

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Abstract: The FPGA devices are increasingly being used in mission critical systems like security systems, banking systems, and avionics. The errors induced by high-energy radiation, also known as Single Event Upsets (SEUs), corrupt the configuration memory of the FPGA device and are a major concern for the system reliability and dependability. For this, error mitigation techniques like triple module redundancy and ECC codes are commonly employed techniques. However error mitigation techniques do not recover the system. The fault-free system can be recovered using reconfiguration of the FPGA device. Previous recovery methods employ processor cores as a reconfiguration controller consuming notable amount of device resources and introducing additional error detection and recovery latency. In this paper a low area overhead error recovery mechanism for SRAM based FPGA systems is presented. The error recovery mechanism is implemented as a state machine. The reliability of the developed solution was experimentally evaluated by fault emulation environment.

Keywords: FPGA, dynamic partial reconfiguration, self-recovery, fault emulation, single event upset

Sprotno preiskušanje in popravljanje sistemov z dinamično delno rekonfiguracijo

Izvleček: Programirljiva vezje FPGA se vedno bolj uporabljajo tudi v visoko zanesljivih sistemih, ki se uporabljajo v nadzornih sistemih, bančništvu in v letalski industriji. Napake, nastale zaradi visoko-energijskega sevanja, imenovane SEU, lahko spremenijo vsebino konfiguracijskega spomina vezja FPGA in predstavljajo eno večjih težav pri razvoju zanesljivih sistemov. Najpogosteje zanesljivost sistemov izboljšamo s pomočjo metod za zmanjševanje vpliva napak kot sta potrojitev modulov in uporaba kod za odpravljanje napak. Pomanjkljivost takih metod je v tem, da ne odpravijo same napake v sistemu. Napake v sistemu osnovanemu na vezjih FPGA lahko odpravimo z ponovnim konfiguriranjem vezja FPGA. Obstoječe metode popravljanje sistemov osnovanih na vezjih FPGA kot krmilnik rekonfiguracije uporabljajo procesorko jedro kar znatno poveča porabo logičnih blokov, poveča pa tudi latentnost pri odkrivanju ter odpravljanju napak. V članku je predstavljen mehanizem odpravljanja napak za sisteme osnovne na vezjih FPGA, ki uporabi relativno malo logičnih blokov. Mehanizem odpravljanja napak je izveden z avtomatom prehajanja stanj. Zanesljivost razvite metode je bila ovrednotena s pomočjo okolja za emulacijo napak v vezjih FPGA.

Ključne besede: dinamična delna rekonfiguracija, samopopravljivost, emulacija napak

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1 Introduction

SRAM-based FPGA devices are increasingly being used for implementing embedded applications used as a part of a mission-critical and reliable system. The main advantage of FPGAs is their high reconfigurability, which enables fast prototyping, flexible functionality through partial reconfiguration, on-site hardware upgrades, and on-site configuration recovery. Due to the increasing integration density FPGA devices are getting more susceptible to faulty behavior, caused by cosmic or artificial radiation [1-3]. Such faults are modeled as Single Event Upsets (SEUs). While radiation is a major concern in space [4], systems in avionics and on ground level are less exposed to it because of the planetary atmospheric and magnetic radiation shield. However, experiments [1-2,5] showed that with increased density of integrated circuits the neutron particles present in the atmosphere are also capable of producing SEU.

The Single Event Upset is a change of logic state caused by the radiation. It is a result of the free charge created by ionization in the node proximity. While such errors are typically transient they can cause a bit flip in the device memory.

SRAM FPGA devices are programmable logic devices using the SRAM memory for storing the configuration. While SRAM memory enables the effortless and rapid prototyping, they are especially vulnerable to SEUs. Thus it is imperative that FPGA based applications, where high reliability is required, include mechanisms that can easily and quickly detect and correct SEUs.

Many techniques have been developed to protect critical systems on SRAM FPGAs against SEU [6]. At the design level of the FPGA these techniques are classified as SEU mitigation techniques which prevent SEU to disturb the normal operation of the target design, and SEU recovery techniques that recover the original programmed information in the FPGA configuration memory after an upset.

Some SEU mitigation techniques use time redundancy but they are effective only against transient faults. The most common SEU mitigation techniques employ hardware redundancy like Triple Modular Redundancy (TMR) and Error Correcting Codes (ECC). In the case of TMR, design logic is triplicated and a voter is used to identify the correct value [7-10]. Since the voter is also vulnerable to upsets an improved TMR strategy for FPGA was developed [7]. The voters are triplicated and implemented using dedicated FPGA logic resources. TMR can be distributed over reconfigurable modules and when the voter detects a fault the faulty module can be recovered by a partial reconfiguration. A controller for managing the reconfiguration was proposed by [11].

Error Correction Codes (ECC) [12] are also used to mitigate the SEU in integrated circuits. Different ECC are used to protect systems against single and multiple SEUs. The most common ECC are Hamming codes and Reed-Solomon codes. ECC are mostly used to protect memories of the systems.

The SEU recovery techniques in SRAM FPGAs are also known as configuration scrubbing. The basic principle of this method is to use partial reconfiguration to recover SEUs within the FPGA configuration memory. Depending on which FPGA configuration interface is used to reconfigure the device, the scrubbing techniques are classified as external and internal. The external scrubbing techniques use external configuration ports (i.e. JTAG, SelectMap). They require an external radiation hardened scrubbing controller (processor [13], or FPGA [14]) and external radiation hardened memory to store the so called "Golden copy" of the FPGA configuration bits. The internal SEU recovery techniques use internal configuration interface to access the configuration memory of the FPGA. Scrubbing is also controlled internally and the controller usually consists of an embedded microprocessor [15-18].

The SEU detection-and-recovery mechanism should be fast in order to reduce the system-error latency. Besides, since it is implemented with similar FPGA resources as the target application, the mechanism itself is subject to SEUs. It is therefore imperative that its hardware overhead is as small as possible.

This paper summarizes the results of the development of a novel internal SEU detection-and-recovery mechanism [19]. This approach outperforms existing recovery mechanisms in terms of speed as well as in minimizing the hardware overhead. It can be implemented using different error mitigation techniques to achieve required degree of the system reliability. The error recovery mechanism with accompanying error mitigation techniques are evaluated using a specially designed fault-emulation environment that allows the injection of faults into specified FPGA resources. The obtained failure-in-time (FIT) estimations can be used to select appropriate solution.

2 Single event upsets in SRAM FPGA

FPGA device is an integrated circuit that consists of an array of logic blocks, interconnection networks, and configuration memory. The configuration memory controls the behavior of each logic block as well as the connections in the interconnection networks. Changing the content of the configuration memory different logic circuits can be implemented on such array.

In the Xilinx FPGA the configuration memory is organized as a matrix of configuration frames. More detailed structure of the FPGA configuration matrix is depicted in Figure 1. A configuration frame is the smallest reconfigurable part of a FPGA device. The size of the configuration frame in Xilinx Virtex 4 and Virtex 5 FPGA family is 41 words or 1312 bits. The whole column of configuration frames in the configuration matrix corresponds to a single type of the FPGA resources: Configuration Logic Blocks (CLBs), Block RAMs (BRAMs), and DSPs. The number of configuration columns of each type of the FPGA resources varies with the family and size of the FPGA device.

The frame is identified by the frame address. The frame address is composed of top/bottom bit, major address identifying the column, the row, and the minor address identifying the frame within the row.

The configuration memory of the SRAM based FPGA is susceptible to the SEUs. The SEU can cause the change in a bit of the configuration frame that corresponds to a particular FPGA resource. It may correspond to internal memory of the FPGA device (BRAM), or to the

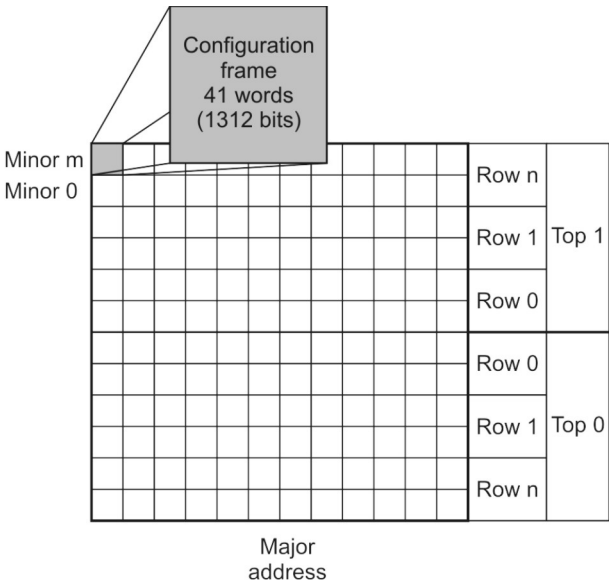

Figure 1: FPGA configuration matrix structure

DSP block (e.g. multiplier), or to the Configurable Logic Block (CLB), comprising Look-Up Tables (LUT) and flip-flops, or to the internal routing.

The changed configuration bit may manifest as an altered device. However the user design does not occupy whole FPGA and even when the affected bit corresponds to the used resource its effect might be masked. The configuration bits that correspond to the used FPGA resources are considered potentially critical.

A SEU can also affect other non-configurable parts of the FPGA device like Power-On-Reset circuit (POR), SelectMap or Internal Configuration Port (ICAP), Digital Clock Managers (DCMs), or global signals (Global Wire Enable, Global 3-State, etc.). Such faults can cause regional or device wide failure. These SEUs are referred as Single Event Functional Interrupts (SEFI) [18].

3 Error-recovery mechanism

The errors in the FPGA configuration memory can be recovered by the reconfiguration. The straightforward approach is to reconfigure the whole device however such approach requires long configuration time and is inefficient. The alternative is to reconfigure only the affected portion of the configuration using partial reconfiguration. The reconfiguration can be implemented using external reconfiguration port (either SelectMap or JTAG) and controller, or using internal configuration port (ICAP) and internal reconfiguration controller. The fault-free configuration can be stored externally in the nonvolatile memory or the reconfiguration content can be determined if the error location is known.

3.1 Error detection and recovery method

In Xilinx Virtex 4 and Virtex 5 FPGA families each configuration frame contains an Error Correction Code (ECC) signature. ECC signature consists of 12 parity bits that can locate single bit fault within the frame and detect double bit faults. The error within the frame can be determined by comparing the stored ECC signature with the newly calculated ECC. The comparison is called the syndrome value. First 11 bits of a syndrome value identify the location of a single erroneous bit within the frame while the last bit indicates the presence of a double error in the frame.

Xilinx Virtex 4 and Virtex 5 FPGA families have an embedded ECC circuit that calculates a frame syndrome value during the read-back of the frame. The Table 1 summarizes possible syndrome values and the corresponding error status.

Table 1: Syndrome value to error status mapping.

Syndrome bit 11	Syndrome bits 10 to 0	Error status
S[11]=0	S[10:0]=0	No error
S[11]=0	S[10:0]>0	Single bit error S[10:0] location
S[11]=1	S[10:0]=0	Single bit error in last parity bit
S[11]=1	S[10:0]>0	Double bit error

The error in the FPGA configuration memory can be detected by continuously reading configuration frames and monitoring the syndrome value. When the syndrome value is non-zero there are two possibilities:

1. Single fault is detected and the original frame content can be restored using syndrome value.
2. Double fault is detected and the original frame cannot be restored. To recover the affected device the frame must be restored using externally stored fault free configuration.

3.2 Error recovery mechanism implementation

Proposed error recovery mechanism consists of an Internal configurations Port (ICAP), a frame ECC device, one dual-port Block RAM (BRAM) and control logic. Its architecture is depicted in Figure 2.

The FPGA device can be reconfigured by applying configuration commands in the configuration registers of the device. The ICAP device has a direct access to these registers and it is used for both reading and writing the content of the configuration frames.

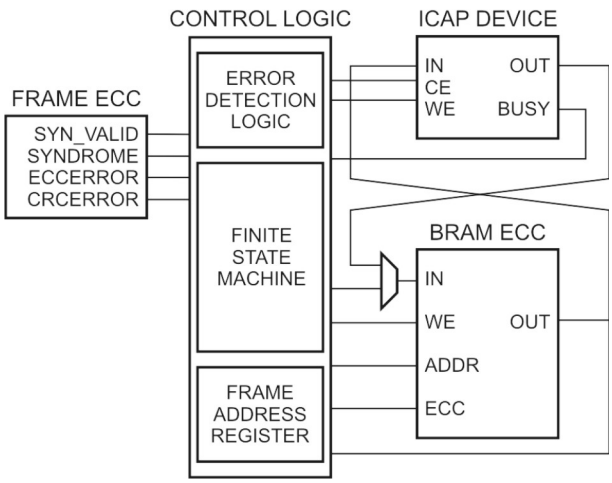

Figure 2: The error recovery mechanism architecture

The command sequences for both reading and writing of configuration frame are predefined and stored in the Block RAM. During the iteration an address of the current frame is determined and inserted in the read command sequence. The sequence is then transferred to the configuration registers by using ICAP device.

The frame ECC device is used to detect and locate configuration errors within the frame content. It works in parallel with the ICAP device during the read operation. While ICAP device reads the frame content the frame ECC device calculates the syndrome value.

The internal Block RAM is used to store the configuration command sequences as well as the content of the current configuration frame, which is used for error recovery if the frame is faulty. Since BRAMs are also susceptible to SEUs, strengthen BRAM configuration with internal ECC option is used.

The control logic monitors error detection process and triggers the frame reconfiguration, if an error is detected. When double error is detected an external alarm is triggered. External alarm can be used for external reconfiguration of the device. The control logic consists of a Finite State Machine (FSM), a frame address register, and error detection logic. The frame address register holds major address, top/bottom bit, row, and minor address and its value is updated when frame address is needed. The error detection logic examines the syndrome value, and corrects the frame content in the BRAM and triggers the reconfiguration if an error occurred.

3.3 Error recovery mechanism operation

The operation of the error recovery mechanism is controlled by a Finite State Machine (FSM) depicted in Figure 3.

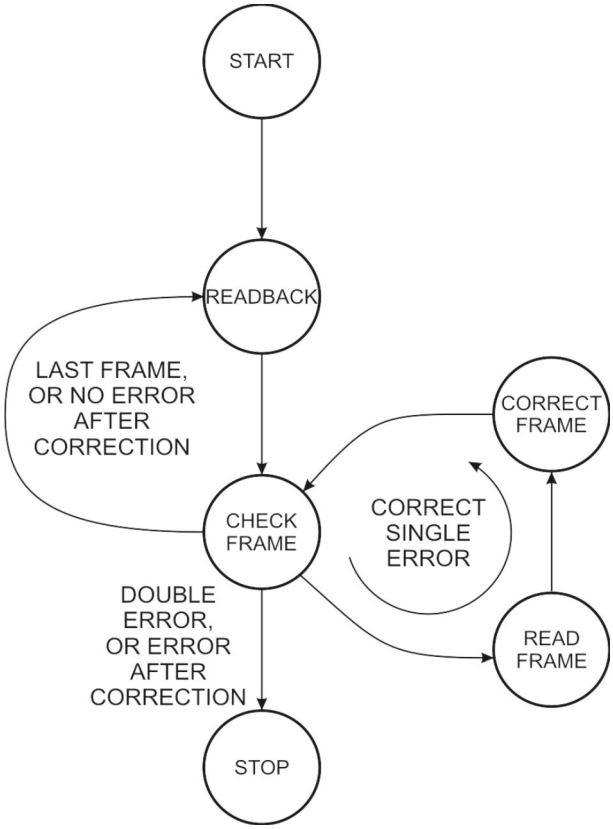

Figure 3: The error recovery state machine diagram

The recovery process starts in the state Start, where internal registers and signals are initialized.

In the state Readback the reading of the current frame register is initiated by issuing the readback commands with current frame address.

In the state Check Frame the syndrome value of current configuration frame, determined by the frame ECC device is inspected by the error detection logic. SYNDROMEVALID signal indicate the completion of the frame check operations. There are several options depending on the syndrome value:

1. The syndrome value is zero. This indicates that current frame is fault free. If the current frame is the last frame of the FPGA device, the register is initiated to the first frame, otherwise the frame address is incremented to the next frame address. The next frame read is started in Readback state.
2. If a single error is detected the erroneous frame is read in the state Read and its content stored in the BRAM. According to the syndrome value the frame is reconfigured with the corrected content in BRAM in the Correct frame state. Additional Check Frame is initiated. In the case of two consecutive failures of the same state, the mechanism switches to Stop state where an alarm is triggered.

3. In the case of double faults the error is detected but cannot be corrected. The mechanism switches to the state Stop, where an alarm is triggered.

In the case of multiple errors the operation of the mechanism is unreliable. However the probability of multiple errors in the same configuration frame is negligible.

4 Hardware implementation comparison

The internal error recovery mechanism was implemented using Virtex 4 and Virtex 5 FPGA families. The hardware overhead as well as the error recovery time of our error recovering mechanism was compared with other reported mechanisms.

The implementation in Virtex 4 FPGA family was compared with the error recovering mechanism described by Heiner *et al.* [16]. The comparison is presented in Table 2.

Table 2: Virtex 4 implementation comparison

Virtex 4 XC4VLX15	Our mechanism	Heiner et al. [16]
Slice	176	736
Flip-flops	118	680
BRAM	2	2
Worst-case Error detection time	1.477ms	~1.5ms
Worst case Error correction time	2us	~24.0ms
Worst-case Error recovery time	1.479ms	~25.5ms

The controller of their error correction mechanism is 8 bit PicoBlaze microprocessor. While PicoBlaze microprocessor requires relatively little FPGA resources, it is still significantly bigger than our FSM controller. On the other hand a microprocessor offers additional features, like easier monitoring and debugging through communication devices. While such features ease the development of the system, they require additional FPGA resources which in turn reduce the reliability of the recovery mechanism.

The error detection is performed using a device readback and achieve comparable error detection time, however they do not have the address of the erroneous frame. Therefore, when an error occurs, they have to perform an additional frame by frame check to determine the location of the error. This leads to a large error correction time.

The Virtex 5 implementation was compared to the Xilinx error recovery mechanism described by Chapman [17]. The results are shown in Table 3.

Table 2: Virtex 4 implementation comparison

Virtex 5 XC5VLX30	Our mechanism	Chapman [17]
Slice	72	172
Flip-flops	115	321
BRAM	1	1
Worst-case Error detection time	2.261ms	2.261ms
Worst case Error correction time	2µs	125µs
Worst-case Error recovery time	2.263ms	2.386ms

The controller of the Xilinx error correction mechanism is 8 bit PicoBlaze microprocessor and occupies about three times more FPGA resources than our mechanism.

Virtex 5 devices have an additional dedicated device readback CRC which can perform a continuous readback of the FPGA device. The recovery mechanism [17] employs readback CRC device to detect errors and the error-detection time is the same as error-detection time of our recovery mechanism. However the error correction time is four times longer since it is controlled by 8-bit PicoBlaze processor in contrast to our 32-bit architecture.

5 Fault-emulation experiment

In order to assess the reliability of the proposed recovery mechanism an error emulation environment was developed. Bit-flip errors are injected into the configuration memory of the targeted bit of the FPGA configuration. This is achieved by dynamic partial reconfiguration with a circuit similar to our error-recovery mechanism. It is additionally connected to the external computer, which controls the placement of the bit-flip error and gathers information of the error recovery. This error injection approach enabled us to inject configuration faults at a precise location within the FPGA configuration memory.

The fault emulation experiment was performed by placing both fault injection circuit and error recovery mechanism in the target FPGA device. Additional measures have been taken in order to prevent simultaneous access to the FPGA reconfiguration registers. The hardware structure of the fault emulation and error recovery mechanism assessment is given in Figure 4. The computer behaves as a fault emulation controller,

external memory, and external reconfiguration device. It also acts as an external watchdog timer for the error recovery mechanism.

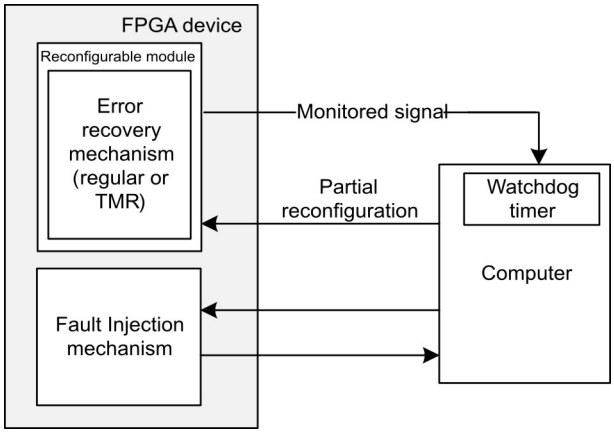

Figure 4: The error recovery mechanism architecture

Faults are injected only into the configuration memory of the FPGA device which corresponds to the error recovery mechanisms. Errors in other parts of the configuration memory do not affect the operation of the error recovery mechanism and are corrected during configuration memory recovery cycle. Furthermore only single recovery cycle is performed since the error should be detected and repaired in first cycle.

The fault emulation process starts by configuring the FPGA device with fault injection mechanism and fault-free error-recovery mechanism, which is being stopped. Then following steps are performed for each fault from the fault list:

- Fault is injected into error-recovery mechanism configuration memory via fault injection circuit.
- The error-recovery mechanism is started and it stops after its repair cycle finishes. Depending on how injected fault affects the performance of the error-recovery mechanism, there are following situations:
  - The error-recovery mechanism performs correctly and the error is corrected. This is detected by external watchdog timer, which is reset. The fault injection mechanism verifies that the fault was corrected. The computer logs the result and the fault emulation proceeds with the next fault from the fault list.
  - The error-recovery mechanism fails, but the failure is detected by the watchdog timer. Error-recovery mechanism did not complete the recovery cycle and the watchdog timer was not reset. Such failures are still manageable by the error-recovery mechanism if an external watchdog timer is added. The computer logs the result and reconfigures the error-recovery mechanism using stored partial configuration image. The fault emulation proceeds with the next fault from the fault list.
  - The error-recovery mechanism fails, however the failure is not detected by the watchdog timer. This indicated that error-recovery mechanism completed the recovery cycle and reset the watchdog timer, but it didn't correct the failure. The situation is detected by fault-injection mechanism and logged by the computer. The computer reconfigures the error-recovery mechanism from stored partial configuration image since the error-recovery mechanism could introduce additional fault into its configuration. The fault emulation proceeds with the next fault from the fault list.

5.1 Fault-emulation results

Fault emulation experiment was performed on Virtex 5 XC5VLX110T device. In the fault-emulation experiment 181056 faults were injected into 138 configuration frames occupied by error-recovery mechanism. Only 9177 faults affected the operation of the error-recovery mechanism. 719 of undetected faults can be further detected and corrected by an external watchdog timer and external reconfiguration device. These faults were further classified by their corresponding type of the FPGA resource. The results of the fault-emulation are presented in Table 4.

Table 4: Fault-emulation results of an error-recovery mechanism implemented on Virtex 5 FPGA device

181056 injected faults	Unrecoverable Errors	Detected by watchdog
Routing	7180	554
LUT content	1429	122
CLB configuration	509	37
BRAM configuration	59	6
Whole mechanism	9177	719

5.2 Reliability estimation

The reliability of Xilinx devices in the atmospheric conditions is being investigated by an ongoing Rosetta experiment [2]. Current reliability estimation of Xilinx FPGA devices can be found in Xilinx device reliability report [20]. The SEU induced error rate is given in terms of Failure In Time (FIT) or Mean Time Between Two Failures (MTBF). The FIT is the number of failures that can be expected in 10^9 hours of operation.

Our experimental results were determined for Virtex 5 FPGA device. The nominal failure rate for Virtex 5 devices is 162 FIT/Mb according to [20]. According to experi-

ments shown in [21] the failure rate of the application can be estimated by the multiplication of the percentage of the critical bits acquired with fault emulation with the failure rate of the whole device.

Table 5: SEU reliability estimation for applications on Virtex 5 XC5VLX110T device

XC5VLX110T device	Number of critical bits	FIT (SEU/109 h)
Whole device	31.1 Mb	5039.8
Average design	3.42 Mb	554.4
Error-recovery mechanism	9177 b	1.49
Error-recovery With watchdog	719 b	0.12

Table 5 summarizes the reliability estimation of different design scenarios. The whole FPGA configuration of Virtex 5 XC5VLX110T device has over 5000 FIT. However an average design uses only portion of FPGA resources and only part of their corresponding configuration bits are critical to its operation. In the estimation 11% configuration bits are considered to be critical for the average application [22].

The fault-emulation experiment determined that 9177 configuration bits are critical which in turn gives a reliability estimation of 1.49 FIT. Applying an external watchdog timer with accompanying external reconfiguration device the reliability estimation is decreased to 0.12 FIT which is equivalent to MTBF of approximately 1 million years.

6 Conclusions

An error recovery mechanism for SRAM based FPGAs was developed. It is controlled by a finite state machine architecture providing the smallest reported hardware overhead and minimal recovery latency. It can be further hardened by the use of external watch dog timer.

The efficiency and performance of the proposed mechanism was evaluated by the fault evaluation environment.

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Different Switchover-strategies for Load Balancing in Future Aircraft

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Abstract: Saving weight in aircraft is the major challenge to reduce fuel consumption and decrease the running costs. The electrical distribution system in aircraft is oversized and shows potential for optimization. An inflexible point-to-point supply of loads is the state-of-the-art technology in aircraft nowadays. Because the wiring is rigid, it is not possible to connect loads to different power feeders when the aircraft is in flight. New technologies are required for handling the increasing demand for electricity on board aircraft. Two concepts — phase balancing and feeder balancing — which lead to an energy-efficient power supply network, are introduced. Both methods use intelligent switching nodes with power semiconductor devices, such as MOSFETs. The power transistors are chosen in such a way that they are slightly above the limits for forward current, blocking voltage and switching frequency. The number of switching operations that produce overvoltages and overcurrents in the electrical grid increases if the concepts that have been presented are used. To ensure that the transistors operate in their safe operating area, snubber circuits are used. Since the switching nodes bring in additional weight, these snubbers have to be designed in such a way that they are sufficiently light. Based on an analytical examination of switching ohmic-inductive and ohmic-capacitive loads, different switching strategies for reducing the negative switching effects are introduced. Computer simulation results are presented and evaluated.

Keywords: Feeder Balancing, More Electric Aircraft, Phase Balancing, Switching strategy

Različne preklopne strategije uravnoteženja bremena v letalih prihodnosti

Izvleček: Prihranek pri teži je največji izziv pri varčevanju z gorivom in zniževanju stroškov v letalu. Električen sistem v letalu je predimenzioniran in ponuja možnosti optimizacije. Trenutno stanje tehnike v letalstvu je napajanje bremena po sistemu od točke do točke. Zaradi togega ožičenja posameznega bremena med letom ni mogoče napajati z različnimi viri, zato so potrebe nove tehnologije, ki bodo sposobne dovajati vedno večje potrebe po energiji. Predstavljena sta dva koncepta – balansiranje faze in balansiranje vira –, ki vodita v energijsko učinkovit napajalni sistem. Obe metodi uporabljata preklopne vozle z močnostnimi polprevodniškimi elementi, kot je MOSFET. Močnostni tranzistorji so dimenzionirani le nekoliko nad mejnimi prevodnimi tokovi, blokirnimi napetostmi in preklopnimi frekvencami. Pri uporabi predstavljenih konceptov se poveča število preklopnih operacij, ki povzročajo prenapetosti in nad tokove. Za zagotavljanje delovanja tranzistorjev v varnem območju delovanja se uporabljajo blažilna vezja. Ker preklopna vozlišča prinašajo dodatno težo je potrebno blažilna vezja izvesti s čim manjšo težo. Na osnovi analitičnih raziskav ohmsko induktivnih in ohmsko kapacitivnih bremen so predstavljene različne preklopne strategije za zmanjševanje negativnih preklopnih vplivov. Predstavljene in ovrednotene so računalniške simulacije.

Ključne besede: balansiranje vira, električna letala, balansiranje faze, preklopne strategije

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1 Introduction

The trend in aviation technology is to substitute hydraulic, pneumatic and mechanical systems with electrical ones. This, however, increases the demand for electrical power on board aircraft and is called 'More Electric Aircraft' [1]. Additionally, the consumption of electrical energy rises as passenger comfort increases. In order to handle the higher demand for power, while keeping the weight of the aircraft low, the electrical power supply system has to be optimized. This can be done by implementing a high-voltage-DC bus and a multifunctional fuel cell system [2]. Electrical load analyses have shown the possibility of reducing the weight in the electrical distribution system [16].

The Institute of Electrical Power Systems of Helmut Schmidt University is conducting research on 'Flexible and energy-efficient aircraft power supply systems'. In this project, new aircraft architectures for feeder and phase balancing are being developed. These methods are aimed at optimizing the current power supply systems. The phase balancing method intends to reduce the return current and leads to a smaller electric structure network (ESN) in new aircraft fuselage made of carbon fibre-reinforced materials (CFRP). The feeder balancing method symmetrises the currents flowing through the power feeders so as to reduce the diameters of cables. Both methods use intelligent switching nodes. At these nodes, the loads can respectively be connected to different phases and power feeders. Therefore, a solid state power controller (SSPC) can be used. An SSPC combines semiconductor and microcontroller technology and works as a monitoring and protection device [3]. State-of-the-art SSPCs prevent overcurrents and overvoltages by controlling the slope of the gate voltage [4]. As a result, the transistors function in the linear mode instead of the switching mode. This method increases losses, which are normally accepted, because switching does not occur very often. However, because switching operations increase in aircraft when maintaining a symmetrised system, the effects of switching have to be analysed. Special components can be added in order to protect the switching node, reducing the negative effects. These can be TVS diodes and snubber circuits.

Another option is a software-controlled solution controlling the switching moments. The switching nodes can be equipped with voltage and current measurement devices, which enable them to follow a specific switching strategy. Assuming that the loads can be represented as a series connection of a resistor and an energy storage device, an analytical examination has been carried out to devise different switching strategies with the aim of reducing overvoltages and overcurrents. Therefore, the quality of the power supply remains high. Different switching strategies have been simulated and compared.

2 Modern concepts using switching nodes

The standard bus voltage of commercial aircraft is 115 V (line-to-ground) in a three-phase system. Electrical generators transmit the power to the primary electrical power distribution centre (PEPDC). The PEPDC supplies flight-critical and consumer loads via secondary power distribution boxes (SPDB). SPDB are connected to loads with currents smaller than 15 A. Most of the power feeders in aircraft are made of aluminium. The return path for the electric current does not use cables, but instead uses the conductive fuselage. Since the fuselage is made of aluminium, the voltage drop is very low. Two methods, aimed at increasing the performance of the electrical grid, are (1) phase balancing and (2) feeder balancing. If a route fails, these methods provide enough opportunities for supplying a load from another cable. This redundancy can increase the availability of the consumer loads and make the electrical grid more tolerant of failure. It is assumed that only cabin and cargo loads are switchable loads, because these loads are non-critical flights loads.

2.1 Phase balancing

Phase balancing is aimed at reducing an asymmetric load of a three-phase feeder. This method becomes advantageous when aircraft manufacturers start to use CFRP materials instead of aluminium for the fuselage of aircraft. CFRP has a lower conductivity than aluminium, which makes it necessary to integrate a conductive ESN into the fuselage for the return current. If there is an asymmetry in a three-phase system, the return current increases, which enhance the voltage drops over the structure [5]. The single-phase loads in the SPDBs can be equipped with threefold-switches, allowing the loads to be connected to either one of the three phases (A, B or C) of a feeder. Through this new approach, the loads can be reallocated in real-time during the flight, allowing for minimization of the return current flowing through the ESN of the aircraft. The reallocation of the cabin and cargo loads is a mixed-integer non-linear optimization problem. It can be solved for instance using genetic algorithm. The objective function of the optimization problem should aim at achieving a symmetric three-phase system. This can be achieved by an objective function "minimize the sum of the negative and zero sequence components". To receive a symmetric three-phase system with a small return current, loads have to be reallocated and switched from one phase to another one. Since switching effects in aircraft increase, because of the application of phase and/or feeder balancing, optimal switching strategies have to be developed to minimize negative switching effects.

During the changeover to another phase, the load is not supplied for a short period, depending on the switching strategy. Aircraft loads have to handle a time of several milliseconds without an energy supply. Nevertheless, the changeover time ought to be small. Because the generators which supply different areas of the aircraft can have different frequencies, computation of phase balancing is limited to each generator of the aircraft to ensure that different grids are not connected. Fig. 1 shows a three-phase generator and exemplary

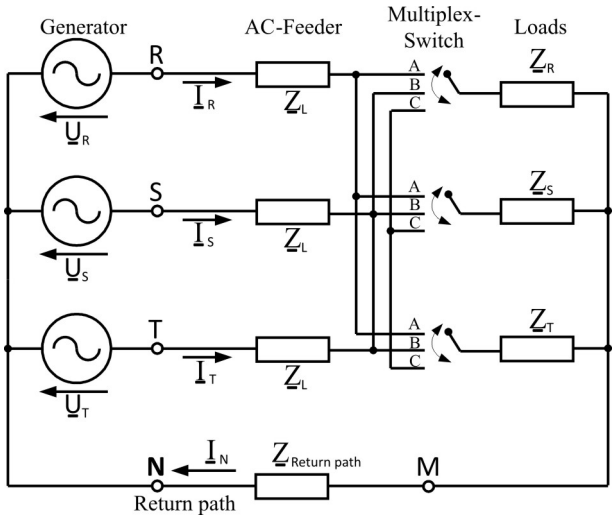

Figure 1: Using threefold-switches for phase balancing of power feeders

three single-phase loads each with a threefold-switch. Every phase of a three-phase feeder has to be connected to each threefold-switch to allow phase balancing. Phase balancing is a large combinatorial optimization problem and non-linear. Because the loads are locally distributed in the aircraft the objective function cannot just assume a virtual ground point where all loads are connected to. This would only lead to a small return current in the front of the aircraft where all currents are added up. Within the ESN higher return current can appear. In order to ensure that phase balancing is not increasing the return current in some locations of the ESN, the actual structure of the ESN has to be taken into account. Fig. 2 shows a more realistic structure of the ESN. It also shows that a threefold switch can supply several loads. In many cases these loads are connected to different grounding point inside the aircraft. Knowing the load currents, phase shifts and the grounding points allows a more effective phase balancing.

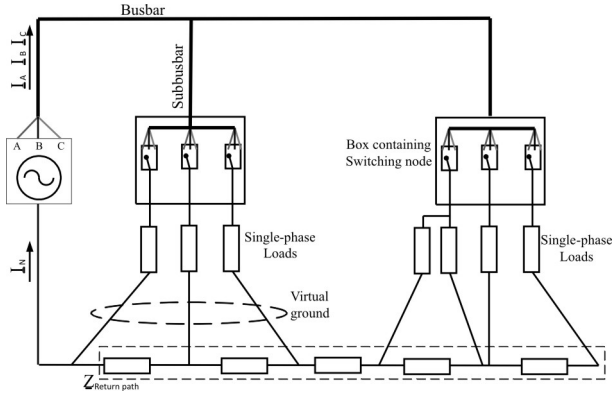

Figure 2: Phase Balancing concept considering the actual structure of loads, switches and the return structure

2.2 Feeder balancing

Because of the high availability, a SPDB is supplied from more than one feeder. The loads in conventional aircraft are allocated with a rigid wiring based on the findings of electrical load analysis. The size of the feeders has to be determined based on the maximum current appearing on the feeder during the flights. Measurements have proved that the power demand of loads vary through the different feeders and that most of the time, the different feeders do not conduct the same current. This non-concurrence facilitates a high optimization potential for feeder balancing. Feeder balancing allows a reduction in the feeder diameter and this saves weight. This is accomplished by switching loads between different feeders (see Fig. 3) to receive a symmetric feeder network, making unused feeder capacities unnecessary [5]. For realizing this in practice, intelligent switching nodes are implemented in aircraft. Such implementation, with the ability to lead all feeders to the single loads, allows for a high granularity. A drawback is the high number of multiplex switches that are needed and the additional cable length. A possible compromise can be reached between the switching options and the additional cable length by leading all passing feeders to the switching node. The feeder balancing concept can be transferred to the DC network of an aircraft.

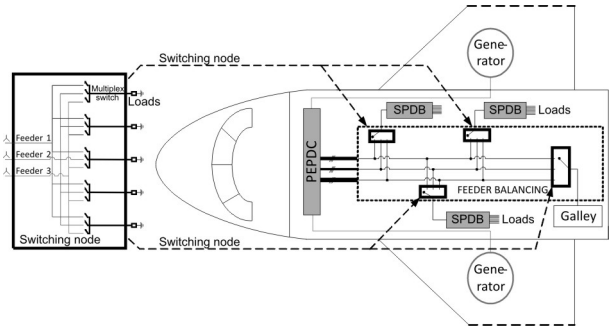

Figure 3: Implementation of switching nodes for smart feeder balancing on board aircraft

Table 1 shows an example electric load analysis of two poorly utilized power feeders reaching their individual maximum current of 25 A and 20 A in different flight phases. If feeder balancing is used and it is assumed that both feeder currents can be distributed equally on the two feeders the highest appearing current will be reduced to 15 A.

3 Switching operations in aircraft ac-electrical grid

In the analytical examination of switching operations, it is assumed that loads can be idealized by a connection

Table 1: Example of poorly utilized power feeder showing potential for current reduction with feeder balancing

Ground / Flight phase	Ground operations	Climb	Cruise	Descent	Highest current
Feeder 1 Cabin	2 A	5 A	25 A	5 A	25 A
Feeder 2 Cargo	20 A	5 A	5 A	5 A	20 A
Average current	11 A	5 A	15 A	5 A	15 A

in series of either an ohmic resistance R with an inductor L, or an ohmic resistance with a capacitor C. Based on this assumption, the formula for the transition voltages and currents have been explained and switching strategies have been developed. After this, the different strategies have been tested via simulation on different kinds of loads. Only loads connected to SPDBs are considered. Heavy inductive loads are directly supplied from the PEPDC. Motors in aircraft with a variable frequency use frequency-variable drives

3.1 Analytical examination

Switching ideal ohmic resistors does not produce any over-voltages or overcurrents. However, this changes when energy storage devices are present. Because switching operations change the energy level of electrical circuits, they cause a transition from the old to the new state. Switching a DC voltage at a capacitor leads to overcurrents when it is turned on if the input voltage is different from the capacitor voltage. Turning a DC current off at an inductive load leads to overvoltages. Switching of a sinusoidal AC voltage, as on board aircraft, has additional effects. The mathematical derivation of the transition current after the turn-on moment is described in detail in [6]. The basic circuit with the two load types is illustrated in Fig. 4. The load can be switched to either phase A or B, depending on the gate signals (Gate A and Gate B). Activating both gate signals would lead to a short circuit.

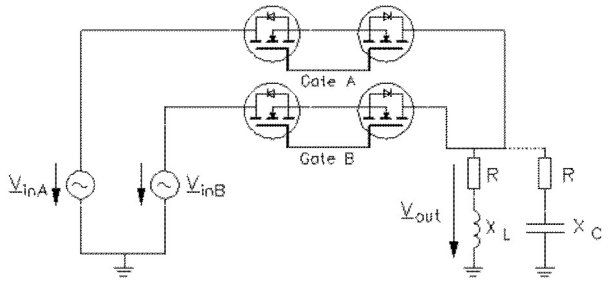

Figure 4: Basic circuit for simulation allowing single-phase loads to be connected to either phase A or phase B of a feeder

3.1.1 Switching operations at ohmic-inductive loads

In contrast to switching a DC voltage, the transition process depends on the instantaneous value of the AC voltage at the moment of switching. When we consider a simple circuit with an inductor and a resistor, it leads to findings which can also be used for current-dependent inductors like transformers or chokes with an iron core [7]. The voltage produced by a generator is given by the formula:

$$v = \hat{v} \cdot \sin(\omega t + \varphi_0)$$

in which $\hat{v}$ is the peak voltage and ω is the angular frequency. The switching operations start at the time t=0. The initial phase φ_0 determines the height of the voltage at the moment of switching. If φ_0 =0, then the voltage is switching at its zero-point. The switching operation is carried out at the maximum value of the voltage if φ_0 =90°. The current required after it is switched on can be calculated using the convolution integral and Laplace-Transformation:

$$i(t) = \frac{\hat{v}}{\sqrt{R^2 + \omega^2 L^2}\left[\sin\omega t + \varphi_0 - \varphi) - \sin(\varphi_0 - \varphi) \cdot e^{\frac{t}{\tau}}\right]}$$

with the time constant $\tau = \frac{L}{R}$ and the phase shift $\varphi = \frac{\arctan\ \omega L}{R}$. The examination of this formula shows that the alternating current component is superposed with a decreasing direct current component. The height of this DC component depends on the initial phase φ_0. The highest current appears when the zero-point of the voltage is switched in. The current can become at the most twice as high as the nominal current. If it is switched in such a way that $\varphi_0 = \varphi$, then the steady state is immediately reached.

Switching an inductive load off, leads to high overvoltages, which can be calculated by Lenz's law:

$$|V_{OUT}| = L\frac{d_i}{d_t}$$

3.1.2 Switching operations at ohmic-capacitive loads

Capacitive loads in an aircraft can be, for example, super-capacitors, DC-DC and DC-AC converters. When it is turned on, a discharged capacitor acts like a short circuit, whereas the current is only limited by the ohmic component. Assuming the voltageis switched on at t=0 to an ohmic-capacitive load, the transition current is:

$$i(t) = \frac{\hat{v}}{R^2 + \frac{1}{(\omega \cdot C)^2}} \cdot \left[\cos(\omega t + \varphi_0 - \varphi) + \frac{1}{R\omega C} \sin(\varphi_0 - \varphi) \cdot e^{\frac{t}{\tau}} \right]$$

with the time-constant τ = RC and the phase shift φ =artcan(RωC). The DC component in the current resulting from switching capacitive loads is a negligible factor. A capacitive load producing a high DC component has, at the same time, a high damping, which leads to a low current [6]. At the moment when it is turned on, the discharged capacitor acts like a short circuit and the current is:

$$i(t=0) = \frac{\hat{v}}{R} \sin \varphi_0$$

This formula considers a discharged capacitor. During the changeover operations for phase or feeder balancing, the loads can be loaded. Depending on the initial phase, a voltage difference occurs between the load voltage and the input voltage. In the worst case, the voltage difference is twice as high as the input voltage. This leads to high inrush currents.

3.1.3 Worst-case scenario

Without using a switching strategy, the power switches and all protection devices have to be designed to withstand the overvoltages and overcurrents that appear when the switching operation is at its worst. To illustrate the different transition processes and to test different switching strategies, a simulation model has been built. The simulation results show the changeover from phase A to phase B. The resultant figures show in the upper part the input voltage V_{inA} and the 120° delayed input voltage V_{inB}. The corresponding gate signals Gate A and Gate B have also been plotted to illustrate the switching moments. The lower part of the figure illustrates the switching effects by showing the output voltage V_{OUT} and the current I. To compare the different switching strategies, the same parameters are used for the current and power factor. Fig. 5 shows the simulation result of a worst-case scenario with an ohmic-inductive load. The load is supplied by phase A and turned off when V_{inA}=80 V at the time t=3.6 ms. The resetting is carried out at the moment the voltage V_{inB} is zero at t=5.9 ms. The output voltage shows an overvoltage of several kilovolts at t=3.6 ms and an overcurrent with a peak value of 33 A at time =7 ms.

The arbitrary switching of a capacitive load could lead to a moment when it is turned off with a high voltage and is reset on another phase with a greatly different voltage. This leads to a high inrush current, which is a multiple of the nominal current.

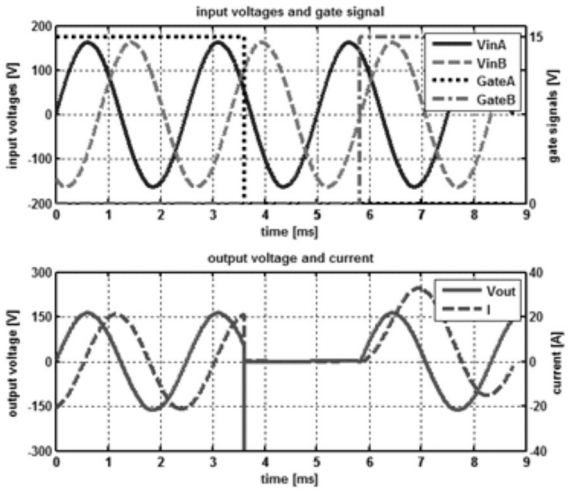

Figure 5: Worst-case switching (ohmic-inductive load)

3.2 Protection circuit of solid state switches

For switching applications in aircraft, MOSFET power switches are normally used. They have an intrinsic body diode, enabling them to only block positive voltages between their drain and source pins. Therefore, two MOSFETs can be connected in series with a common source potential so that this behaves like a bidirectional switch (Fig. 6) [15]. To deal with high currents and high voltages, such bidirectional switches are often connected in series respectively in parallel. In addition, a protection circuit has to be applied.

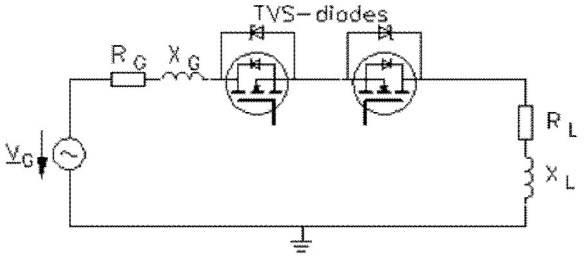

Figure 6: Protection with TVS diodes

3.2.1 Solid state power controllers

In modern aircraft, the power line to commercial loads is protected by SSPCs [5] [8]. These SSPCs use semiconductor technologies and microcontrollers. They can be remote-controlled and programmed for different tripvalues. The SSPCs could be redesigned as multiplex switches for implementing phase and feeder balancing. Semiconductor devices are designed to handle currents and voltages tight to the operation values to save money and because devices with high breakdown voltages and forward current have a higher on-state voltage and a lower switching frequency. To protect

semiconductor switches against overvoltages and overcurrents, protection circuitry is used. Normally, this circuit has to be designed to withstand the worst-case values. The use of switching strategies can reduce the protection circuitry that is needed. Also, the size of the cooling unit can be decreased.

3.2.2 Protection against overvoltages

The easiest way to protect the switch against overvoltage is to connect a TVS or a Zener diode parallel to the switch (see Fig. 6). TVS operates in a manner similar to Zener diodes, but are especially designed to be fast. If the voltage in operation is higher than the permitted voltage, the diode becomes conductive and reduces the overvoltage. In Fig. 7 (right), it can be seen that a gate side protection circuit named active clamping is applied. In case illegal overvoltage occurs, the Zener diode gets conductive and the MOSFET is switched on to reduce the overvoltage. Another possible way of ensuring protection is to implement a snubber circuit with ohmic and capacitive resistance, as shown in Fig. 7 (left). Overvoltages during the switching process charge the capacitor and are reduced.

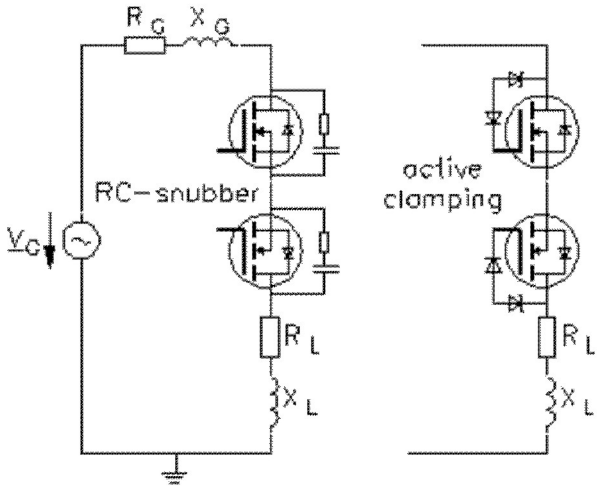

Figure 7: Protection with RC snubber (left) and active clamping (right)

3.2.3 Protection against overcurrents

Overcurrents can occur on board aircraft if a high capacitive load is switched on. If the overcurrent is at the level of the fault current, the installed MOSFETs have to be protected. Although MOSFETs are known as short-circuit-proof solid state devices, they have to be switched off as fast as possible in case a fault occurs [9].

In practice, the fault current is detected by current sensors, such as instrument shunts or current transformers, and results in a switch-off signal, which is rapidly transmitted to the driver unit of the MOSFET. This method is called the direct protection method because the overcurrent is measured directly by the use of current sensors implemented in the source path of the MOSFET. Another method, called the indirect method, observes the drain-source voltage of the MOSFET while it is switched on. If the measured voltage exceeds a permitted level, a signal for switching it off is sent to the driver of the MOSFET. The fault current should be eliminated within 10 μs in order to ensure that the MOSFET is not destroyed [10].

All the protection options have in common the fact that they need additional passive electrical elements, which result in higher cost and increased weight for the aircraft. With a better understanding of the switching process and the resulting switching strategies, both the cost and weight factor can be considerably reduced. In the following section, new switching strategies and control algorithms of the MOSFET-gate have been introduced.

3.2.4 Considerations of power quality

For aircraft applications, high power quality requirements have to be fulfilled by electrical equipment. [11] specifies the requirements and test procedures for the electrical characteristics of the Airbus A350 AC and DC equipment. The stated balancing concepts with active load switching may lead to additional system perturbations, depending on the load type and the switching rate. For 115/230 VAC equipment, different requirements are defined in [11] for steady-state and transient characteristics. Because of the stated switching strategies for different load types, additional system perturbations, caused by transients during the load switching, such as voltage spikes and voltage harmonic distortion, are kept low and should not exceed the limits defined in [11]. However, depending on the switching rate as well as the amount and power of the switched loads, the balancing concepts may affect the power quality due to modulation of voltage. In order to keep this effect low, the maximum permitted switching rate of the balancing concepts should not be higher than 25 Hz (40 ms) [12].

3.3 New switching strategies

In order to produce as few overvoltages and overcurrents as possible as a result of switching, different algorithms can be used, which act on the gate driver of the MOSFETs [13]. To illustrate the effects, the types of load have a power factor of 0.2 and a phase shift of 78.47°. The steady-state current through the load is 15 A.

3.3.1 Zero-switching strategy

SSPCs can be designed in such a way that they can measure the input voltage, the output voltage and the current [14]. A possible strategy, which is often used, is to turn on the switch when the input voltage is zero and to turn it off when the current is zero. This procedure is referred to as the Zero-switching strategy. For this strategy, no output-voltage sensor is needed. If the SSPC receives a signal to switch a load to another feeder, it waits until the next zero-point of the current is reached and switches it off at that moment. The load is connected to a different feeder at the moment when the new feeder voltage is zero. In case the load is a discharged capacitor, the inrush current will be zero because the voltage difference would be lacking. If the load is inductive, an overcurrent occurs (Fig. 5). Because the inductive loads are turned on in the voltage zero-point, the highest DC component of the current is produced. It is ensured that no overvoltages appear when it is turned off in case the load is inductive. In case the load is highly capacitive, the capacitor will be loaded to a voltage level different from zero. If this occurs and the capacitor does not unload itself fast enough while switching over to another phase, when it is turned on during the voltage zero point, it leads to a high inrush current. Fig. 8 shows the operation chart of this strategy.

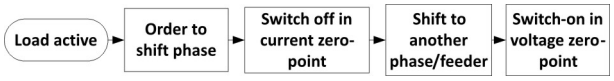

Figure 8: Zero-switching strategy

Fig. 9 shows a high inrush current because of the fact that the ohmic-capacitive load was disconnected from phase A at a high voltage and reconnected to phase B when the voltage V_{inB} is zero. With high capacitive loads, the switching off at the current zero-point leads to a maximal loading of the capacitor and leads to high inrush currents. At high power factors greater than 0.9, the negative effects are repressed through the ohmic parts.

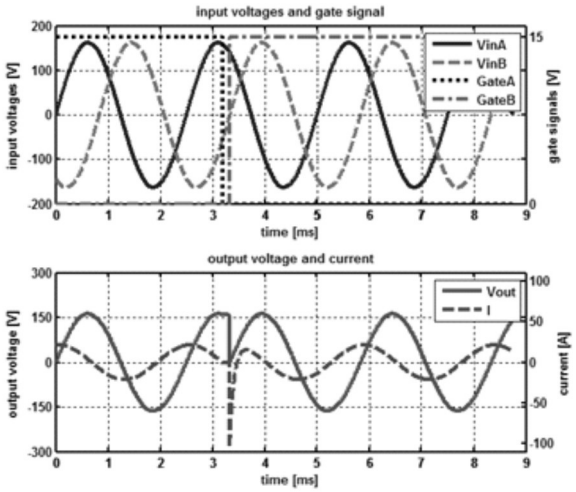

Figure 9: Zero-switching strategy at ohmic-capacitive loads

3.3.2 Vout-switching strategy

To avoid the disadvantage caused by the high capacitive turn-on current, the moment when it is turned on can be executed when the input voltage is equal to the output voltage. Thus, the voltage difference between the input and output sites of the SSPC is zero. Therefore, the output voltage has to be tracked by the SSPC. Since not just the zero-point has to be detected but the exact output voltage has to be measured as well, the requirements from the voltage sensors are higher. This procedure is referred to as the Vout-switching strategy. Even if the capacitor is being discharged during the time when the switch-over occurs, the inrush current will still be zero. With this strategy, the overvoltages that are produced by inductors when they are turned off and the overcurrents produced by capacitors when they are turned on can be avoided. But overcurrents similar to the Zero-switching strategy can appear when ohmic-inductive loads are switched. Fig. 10 illustrates the operation chart of this strategy.

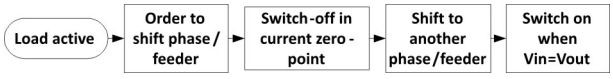

Figure 10: Vout-switching strategy

With ohmic-inductive loads, the behaviour and simulation results of the Vout-switching strategy are the same as for the Zero-switching strategy. Fig. 11 shows the

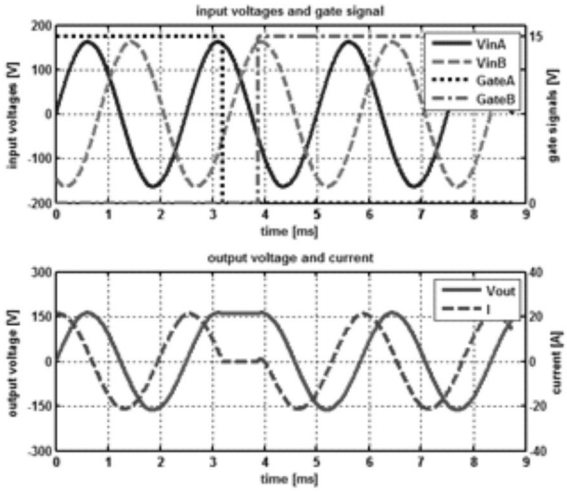

Figure 11: Vout-switching strategy at ohmic-capacitive loads

simulation results with the Vout-switching strategy at capacitive loads.

3.3.3 Phi-switching strategy

Because different strategies are optimal for different kind of loads, one way could be to determine if the load is inductive or capacitive and adapt the switching strategy. Therefore, the current and the input and output voltages have to be tracked, to determine the phase shift. This allows different switching strategies for different load types. The phase shift can be determined using a microcontroller. Because the phase shift is used, this procedure is referred to as the Phi-switching strategy. The Phi-switching strategy is illustrated in Fig. 12.

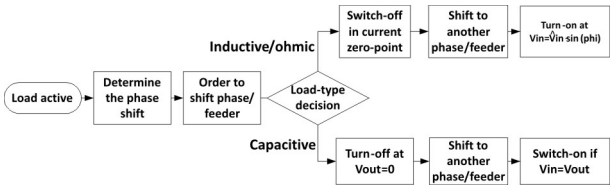

Figure 12: Phi-switching strategy

It is assumed that the load is activated and the stationary current is measured. Depending on the kind of load—whether it is inductive or capacitive—different strategies are used. If the load is inductive, the current will lag behind the voltage and the turn-off will occur at the zero point of the current to prevent high overvoltages. The turn-on on a different phase respectively feeder is executed when the input voltage is:

$$V_{in} = \hat{V}_{in} \cdot \sin(\varphi)$$

This avoids the DC part in the current and immediately leads to the stationary current without an overcurrent. In a built multiplex-switch prototype the phase shift was not determined; instead the voltage of the input is tracked and saved in the moment the current equals zero. This voltage equals $\hat{V}_{in} \cdot \sin(\varphi)$.

At ohmic-capacitive load behaviour, it is turned off at the voltage zero-point and turned on when the input voltage equals the output voltage. In most cases, this will occur at zero voltage. But because the construction of the loads is not known, other cases are possible.

Fig. 13 illustrates the simulation result using the Phi-switching strategy with an ohmic-inductive load. It can be seen that the load is turned off in the current zero point, after 1 ms the voltage of phase B equals $\hat{V}_{in} \cdot \sin(\varphi)$ and the load is activated, leading to an immediately stationary current without an overcurrent. All negative effects can be minimized with this strategy. Loads with rectifier or power factor correction (PFC)

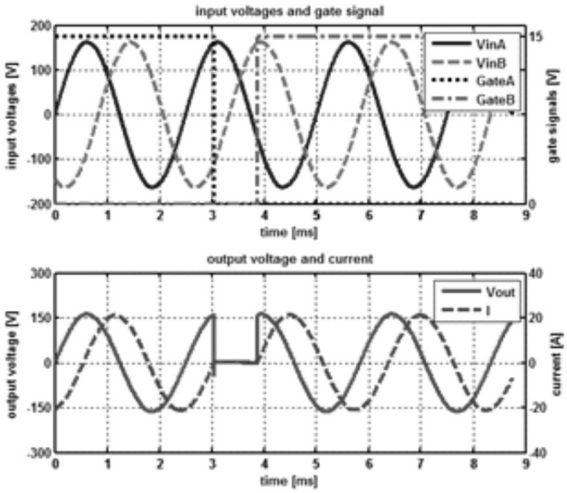

Figure 13: Phi-switching strategy at ohmic-inductive loads

prevent that loads are feeding into the grid. Behind the rectifier is a capacitor to stabilize the voltage, meaning the output voltage meter of the solid-state power controller cannot detect a zero-crossing of the voltage. Therefore, the phi-switching strategy has to be adapted: if the microcontroller of the SSPC does not detected of zero-crossing of the output voltage within one period, the SSPC is turned off immediately independent of the actual current or input voltage.

3.4 Results

Aircraft manufacturers prescribe that loads have to follow certain specifications, such as the high of the inrush current and the maximum allowed phase shift of inductive and capacitive loads, depending on the power consumption. That includes the claim to withstand time periods of several milliseconds without energy supply. To protect the solid state power controllers, snubber circuits are used. Other papers like [4] suggest using the semiconductor switch in linear mode when it is turned on while switching high capacitive loads. Therefore, the maximum capacitance has to be calculated to ensure the transistor stays in its safe operating area (SOA). The data of the SOA is deposited in a look-up table in the microcontroller of the SSPC. The gate voltage is controlled by the microcontroller for controlling the slope of the current. During this time, the losses over the MOSFET increase. In contrast to this strategy, all the switching strategies presented in this paper ensure that the MOSFETs operate in switching mode.

The inductance of the generator is not determinative, since in aircraft hundreds of loads are connected to the generators through several busbars which have two or three branches. That is why the type of load is the most important factor for the switch-over strategy. The

Table 2: Characteristics of the different switching strategies

	Without switching strategy	Zero-switching strategy	Vout-switching strategy	Phi-switching strategy
Turn-on moment	arbitrary	Vin=0 V	Vin=Vout	$\varphi \geq 0: V_{in} = \hat{v} \cdot \sin(\varphi)$ $\varphi \langle 0: V_{in} = V_{out}$
Turn-off moment	arbitrary	I=0 A	I=0 A	$\varphi \geq 0: I = 0 \cdot A$ $\varphi \langle 0: V_{in} = 0$
Overvoltage at turn-off by ohmic-inductive loads	Yes	No	No	No
Overcurrent at turn-on by ohmic-capacitive loads	Yes	Yes	No	No
Overcurrent at turn-on by ohmic-inductive loads	Yes	Yes	Yes	No

way suggested here for reducing transition effects is to control the switching moments. Without a switching strategy, the turn-on and turn-off moments are arbitrary. The time the load is not supplied can be minimized, since only a short dead-time has to be included to ensure the former conducting MOSFET is turned off completely. The Zero-switching strategy prevents high overvoltages when inductive loads are switched off. The Vout-switching strategy also avoids high inrush current when capacitive loads are turned on. Therefore, an additional output voltage sensor is necessary. The Phi-switching strategy claims the highest demands on accuracy of the voltage and current sensing. Table 1 summarizes the characteristics and the effects of the different switching strategies. Simulation with parallel loads and models of real loads gives similar results. With parallel ohmic-capacitive loads, depending on their time constant, the absolute value of the load voltage decreases during the changeover time. This reduces the inrush current for the Zero-switching strategy. Since the output voltage is tracked by the Vout-switching strategy, the results stay the same. The Phi-switching strategy in this case cannot prevent the overcurrent when it is turned on at ohmic-inductive loads.

Switching operations should be minimized to ensure that the DC current components are decayed in order not to perpetuate them. For aircraft using phase and feeder balancing in the future, it is recommended that the Phi-switching strategy is used.

4 Conclusion

The two methods introduced—phase and feeder balancing—aim at optimizing the distribution networks in aircraft by the use of intelligent switching nodes. Phase balancing minimizes the return current leading to a smaller ESN in future CFRP-aircraft. Feeder balancing uses the non-concurrence of the feeder load to symmetrise the feeders which makes it possible to reduce the power feeder diameters. The intelligent switching nodes using the two methods contain modern power semiconductors, such as MOSFETs, to execute the switching operations.

When the switching operations increase, the implemented power semiconductor switches are extremely stressed by negative switching effects like overvoltages and overcurrents. In order to reduce these negative effects, different switching strategies have been presented. Because of the simulation result, it is recommended to use the Phi-switching strategy. In general, to protect the switches from overvoltages, TVS diodes, RC snubbers or active clamping can be used. For protection from overcurrent, the direct method observing the current or the indirect method observing the drain source voltage can be adopted. Together with the proposed switching strategies, the protection circuit can be designed to be smaller and leads to a lighter implementation of the intelligent switching nodes in modern aircraft.

The analytical examinations as well as the simulations are based on the assumption of ideal devices. Effects such as saturation of iron cores of transformers are not considered. To test and evaluate the feasibility of the different switching strategies, a multiply switch has been built. The experimental results show the feasibility of the different strategies.

In modern aircraft, the power factor is limited and depends on the load power. The higher the load power consumption, the higher the power factor. This reduces

the need for a switching strategy because the negative effects are low. However, some loads which do not fulfil these requirements can still be integrated into the aircraft. On the other hand, the switching strategy could lead to more generous power factor limits. By using an intelligent switching strategy instead of switching arbitrarily, it leads to a smaller layout of the semiconductor and snubber circuits.

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The Copper Losses of Gapped Inductors with Litz-Wire Windings

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Abstract: In this paper, an analytical procedure is presented, how to predict the AC resistance of litz-wire windings considering air gap fringing fields. For this purpose, an equivalent complex permeability model is derived for hexagonally packed wires. It is shown, how the real as well as the imaginary part of the complex permeability can be determined with the copper filling factor as a parameter. An analytical 2D model is deduced to describe the air gap fringing fields of gapped inductors. Accordingly, the proximity losses of the litz-wire winding are determined correctly and the AC resistance of practical inductors can be predicted over a wide frequency range with high accuracy. This offers the opportunity to optimize such components. Finally, the influence of various parameters on the copper losses is investigated and verified by means of experimental data drawn from impedance measurements. The novelty of the approach presented in this paper is given by the fact that an exact 2D analytical solution is conducted to describe the air gap fringing field. Furthermore, the distance between air gap(s) and winding can be considered as a degree of freedom as well as the number of single gaps to realize a distributed air gap.

Keywords: Inductors, air gaps, eddy currents, electromagnetic analysis, analytical models.

Bakrove izgube na tuljavah z režo pri uporabi navitij s pletenico

Izvleček: Članek obravnava analitičen postopek napovedovanja AC upornosti navitja s pletenico. V ta namen je bil razvit model ekvivalentne kompleksne permeabilnosti heksagonalno zavitih žic. Prikazano je, kako se lahko, s pomočjo polnilnega faktorja bakra, določi realen in imaginaren del kompleksne permeabilnosti. Izveden je 2D model opisovanja polja v navitjih z zračno režo. Pravilno so določene izgube bližine v navitju s pletenico. Prav tako je mogoče z visoko natančnostjo določiti AC upornosti v širokem frekvenčnem območju, kar omogoča optimizacijo komponent. V zaključki je, s pomočjo meritev impedance, preučevan vpliv številnih parametrov na izgube v bakru. Novost predstavljene metodologije je natančna 2D analitična rešitev stresanega polja v zračni reži.

Ključne besede: tuljava, zračna reža, vrtinčasti tok, elektromagnetna analiza, analitični model

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1 Introduction

High frequency (HF) litz-wire is generally used to avoid strong eddy current losses due to the fringing fields of adjacent air gaps. If the radius *a* of the insulated strands is smaller than the skin depth

$$\delta = \frac{1}{\sqrt{\pi f \sigma \mu_0}} \tag{1}$$

the well known skin effect can be neglected and a homogeneous distribution of the conducted current is expected. Nevertheless, considerably high losses can still be generated due to the fact that all of the strands are influenced by external magnetic fields generated by adjacent strands, windings and air gaps as well (proximity effect).

When designing HF inductors and integrated magnetic components, these effects have to be predicted with high accuracy. Especially air gap fringing fields can lead to much higher losses than expected. As a disadvantage, these losses develop in a small region around the air gap. Due to the poor thermal conductivity of insulated litz-wire, heat cannot be dissipated outside and insulation failures are the consequence.

In recent work (e.g. [1, 2]), eddy current losses of round and rectangular wires have been investigated. These results were extended to bundles of wires [3] and litz-

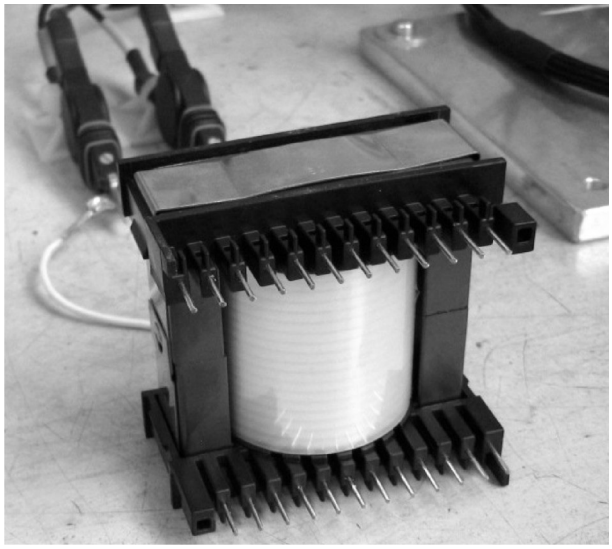


Figure 1: Inductor under test: ETD59/31/22–N87, air gap length l_g=5 mm, number of turns N=72 (litz-wire 7x35x0.1 mm).

wire windings [4, 5]. Nevertheless, numerical simulations as well as analytical solutions (e.g. by the modal decomposition of the boundary value problem) come to their limits when the great number of litz-wire strands has to be taken into account. To provide a solution, equivalent complex permeability models [6 - 9] were derived for the winding area and linked either with FEM simulation or rough (usually 1D) estimations of the penetrating magnetic field.

The novelty of the approach presented in this paper is given by the fact that an exact 2D analytical solution is conducted to describe the air gap fringing field. Furthermore, the distance s between air gap(s) and winding can be considered as a degree of freedom as well as the number of single gaps N_g to realize a distributed air gap (Fig 2).

2 Calculation

2.1 Equivalent Complex Permeability Model

If a round wire is situated in a homogeneous high frequency external magnetic field, eddy currents are generated which again effect the external magnetic field. The shape of this external field part is comparable to a magnetic dipole field. Analogously to the theory of magnetism, a multitude of such dipoles can be expressed by an isotropic complex permeability $\mu = \mu' - \mathrm{j}\mu''$ (Fig. 3). The real part $\mu'(f)$ describes the shielding behavior of the litz-wire region as a function of the frequency f. The imaginary part $\mu''(f)$ is related

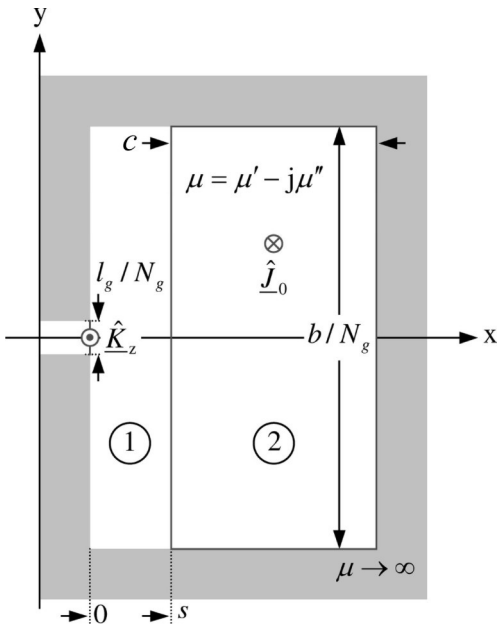


Figure 2: Basic configuration of the winding window (distributed air gap with N_g parts of length l_g/N_g).

to the eddy current losses. To determine $\mu(f)$ of hexagonally packed litz-wire strands, finite element simulation is used.

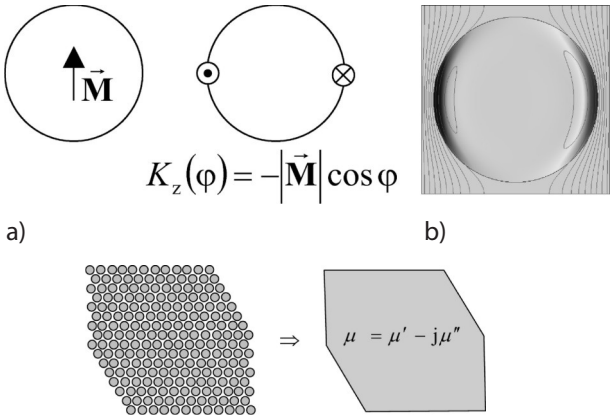
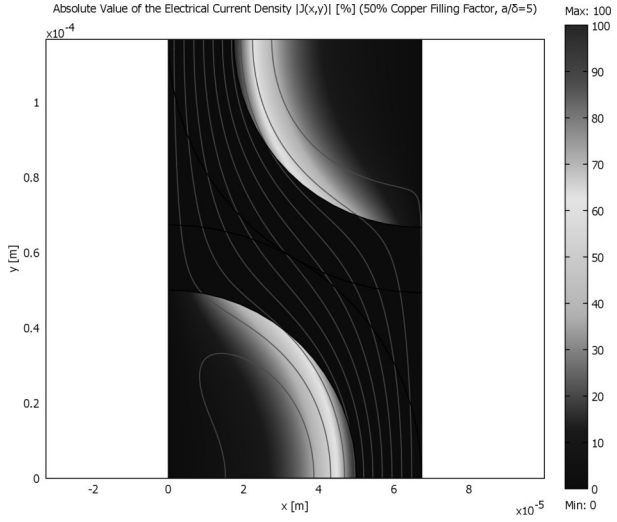


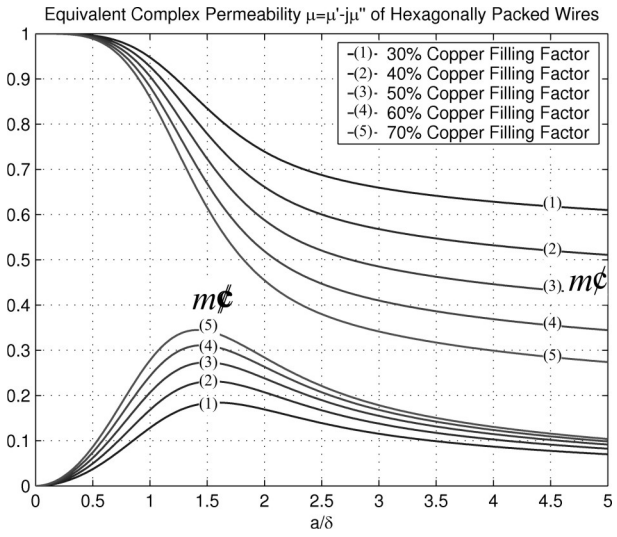
Figure 3: Equivalent current shell of a cylinder with homogeneous magnetization (a), eddy current distribution in a round wire excited by an external magnetic field (b), equivalent complex permeability model for hexagonally packed wires (c).

Fig. 4a shows the FEM simulation of the elementary cell. The picture depicts the absolute value of the electrical current density in a per-cent scale for 50 % copper filling factor and a relation between strand-radius a and skin depth of $a/\delta = 5$.

The real and imaginary parts of the equivalent complex permeability can be determined based on the relations



a)



b)

Figure 4: Simulation (a) of the elementary cell of hexagonally packed wires to obtain the equivalent complex permeability $\mu=\mu'-j\mu''$ (b).

$$\mu = \mu' - \mathrm{j}\mu'' = \mu'\left[1 - \mathrm{j}\tan(\varphi_m)\right] \tag{2a}$$

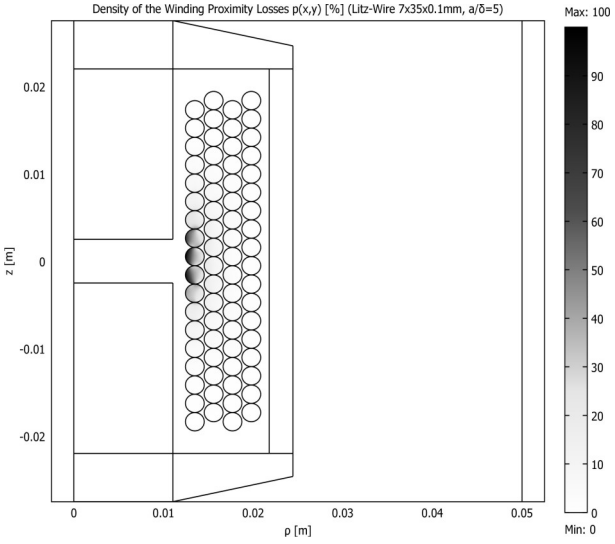
$$\tan(\varphi_m) = \frac{p_m}{2\omega w_m} \tag{2b}$$

$$\mu' = \frac{\overline{B}^2}{4w_m\left[\tan^2(\varphi_m)+1\right]} \tag{2c}$$

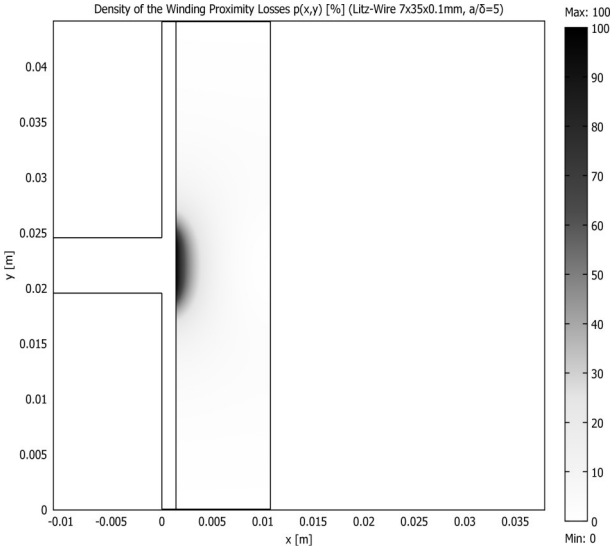
where $\tan(\varphi_m)$ denotes the loss tangent, p_m the mean power loss (per volume) and w_m the mean stored magnetic energy (per volume). In Fig. 4b the results are presented with different values of the copper filling factor as a parameter.

2.1 Analytical Calculation of the Winding Proximity Losses

With the equivalent complex permeability presented above, the calculation of the winding proximity losses can be referred to a magnetostatic problem. The basic configuration is depicted by Fig. 2. Therein, *b* denotes the width of the core's winding window and *c* the thickness of the litz-wire winding.



a)



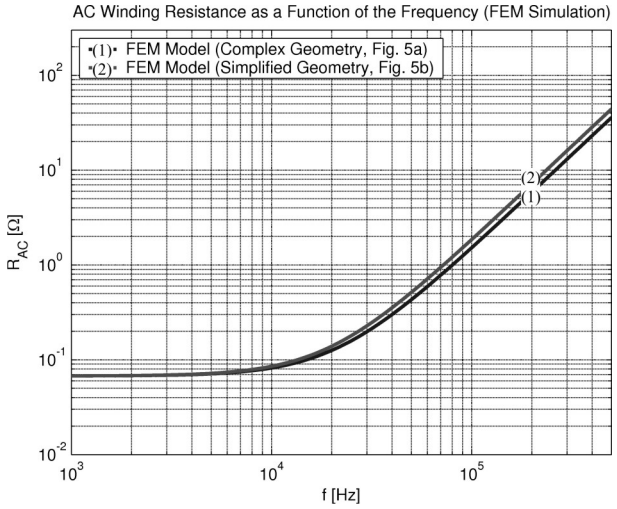
b)

Figure 5: Simulated proximity loss density of the litz-wire region due to the air gap fringing field for complex (a) as well as simplified (b) geometry ($a/\delta = 5$).

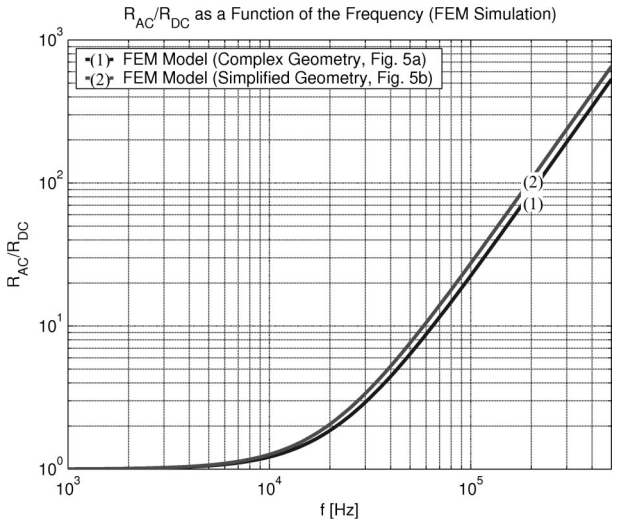
To begin with, it is verified, if the geometry of the winding window can be restricted to the relatively simple configuration shown in Fig. 2 with acceptable error. Therefore, FEM simulations are conducted to investigate the influence of the underlying geometry on the

calculated AC winding resistance. Fig. 5 depicts both alternatives. In Fig. 5a the complex axially symmetric model with distinct litz-wire windings is shown (each with copper filling factor 0.6). In Fig. 5b the plane 2D restricted model is figured out. Therein, the spacing between the round windings is considered by the total copper filling factor (here 0.38) of the winding area.

The color bar in Fig. 5 is related to the simulated proximity loss density of the litz-wire region (per cent scale). Using FEM, the total proximity losses can be determined via integration. By superposition of DC (RMS), skin and proximity losses, the AC resistance is calculated and illustrated by Fig. 6a. In Fig. 6b the relation R_{AC}/R_{DC} is shown. From these results, it can be seen that the basic geometry can be restricted according Fig. 2 with acceptable error.



a)



b)

Figure 6: AC resistance (a) and relation R_{AC}/R_{DC} (b) for complex (Fig. 5a) and simplified geometry (Fig. 5b).

The two-dimensional solution is based on the (complex) magnetic vector-potential $\underline{\hat{\mathbf{A}}} = \vec{\mathbf{e}}_z \underline{\hat{A}}_z(\mathrm{x},\mathrm{y})$, which has to fulfill the vectorial partial differential equation

$$\nabla \times \left(\nabla \times \underline{\hat{\mathbf{A}}} \right) = \begin{cases} \vec{\mathbf{0}} & \text{region 1} \\ & \text{in} \\ -\mu \underline{\hat{J}}_0 \, \vec{\mathbf{e}}_z & \text{region 2} \end{cases} . \quad (3)$$

After R-separation [10, 11] of the according scalar differential equation and restriction by the different boundary conditions, for region 1 and 2 in Fig. 2, the two solutions

$$\underline{\hat{A}}_{z1}(\mathrm{x},\mathrm{y}) = \underline{\hat{A}}_0 + \underline{\hat{B}}_0 \mathrm{x} + + \sum_{n=1}^{+\infty} \left[\underline{\hat{A}}_n \frac{\cosh(\lambda_n \mathrm{x})}{\cosh(\lambda_n s)} + \underline{\hat{B}}_n \frac{\sinh(\lambda_n \mathrm{x})}{\sinh(\lambda_n s)} \right] \cos(\lambda_n \mathrm{y}) \quad (4a)$$

$$\underline{\hat{A}}_{z2}(\mathrm{x},\mathrm{y}) = \frac{1}{2} \mu \underline{\hat{J}}_0 \left[\mathrm{x} - (s+c) \right]^2 + + \sum_{n=1}^{+\infty} \underline{\hat{E}}_n \frac{\cosh\left\{ \lambda_n \left[\mathrm{x} - (s+c) \right] \right\}}{\cosh\left\{ \lambda_n \left[s - (s+c) \right] \right\}} \cos(\lambda_n \mathrm{y}) \quad (4b)$$

are found. With the eigenvalues $\lambda_n = 2\pi \, n \, N_g / b$ and the parameters

$$\underline{\hat{B}}_0 = -\mu_0 \underline{\hat{J}}_0 \, c$$

$$\underline{\hat{A}}_0 = \frac{1}{2} \mu \underline{\hat{J}}_0 c^2 - \underline{\hat{B}}_0 s$$

$$\underline{\hat{B}}_n = -\frac{\mu_0}{\lambda_n} \underline{\hat{J}}_0 \frac{bc}{l_g} \frac{2}{\pi n} \sin\left(\frac{\pi n l_g}{b} \right) \sinh(\lambda_n s)$$

$$\underline{\hat{E}}_n = \underline{\hat{B}}_n \left[1 - \tanh^{-2}(\lambda_n s) \right] \left(1 + \frac{\mu_0}{\mu} \frac{\tanh\{\lambda_n c\}}{\tanh(\lambda_n s)} \right)^{-1}$$

$$\underline{\hat{A}}_n = \underline{\hat{E}}_n - \underline{\hat{B}}_n$$

the proximity losses of the winding area 2 in Fig. 2 can be calculated using Poynting's theorem.

3 Results

Accordingly, the winding proximity losses per length *l* are given by

$$\frac{\overline{P}_v^{(Prox)}}{l} = \frac{N_g \omega}{2\mu_0} \mathrm{Im} \left\{ \frac{b}{N_g} \underline{\hat{A}}_0 \underline{\hat{B}}_0^{\,*} + \sum_{n=1}^{+\infty} \pi \, n \frac{\underline{\hat{A}}_n}{\cosh(\lambda_n s)} \frac{\underline{\hat{B}}_n^{\,*}}{\sinh(\lambda_n s)} \right\} \quad (5)$$

3.1 Calculation of the Total Copper Losses

If the winding with current $i(t) = \hat{i}\cos(\omega t)$ consists of *N* turns of litz-wire, each with *M* strands of diameter *d*, the DC (RMS) losses can be described by

$$\frac{\overline{P}_v^{(RMS)}}{l} = \frac{1}{2}\frac{N}{\sigma M \pi\left(\frac{d}{2}\right)^2}\hat{i}^2 \tag{6}$$

The copper losses due to the skin effect now are directly calculated from the RMS losses:

$$\frac{\overline{P}_v^{(Skin)}}{l} = \left[\frac{d}{4\delta}\mathrm{Re}\left\{(1+\mathrm{j})\frac{\mathrm{I}_0\left[(1+\mathrm{j})\frac{d}{2\delta}\right]}{\mathrm{I}_1\left[(1+\mathrm{j})\frac{d}{2\delta}\right]}\right\} - 1\right]\frac{\overline{P}_v^{(RMS)}}{l} \tag{7}$$

The total copper losses are finally given by the superposition of all loss mechanisms:

$$\frac{\overline{P}_v}{l} = \frac{\overline{P}_v^{(RMS)}}{l} + \frac{\overline{P}_v^{(Skin)}}{l} + \frac{\overline{P}_v^{(Prox)}}{l} \tag{8}$$

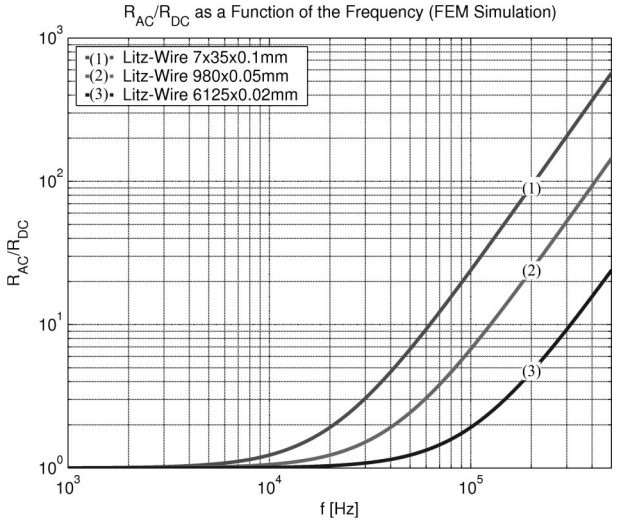
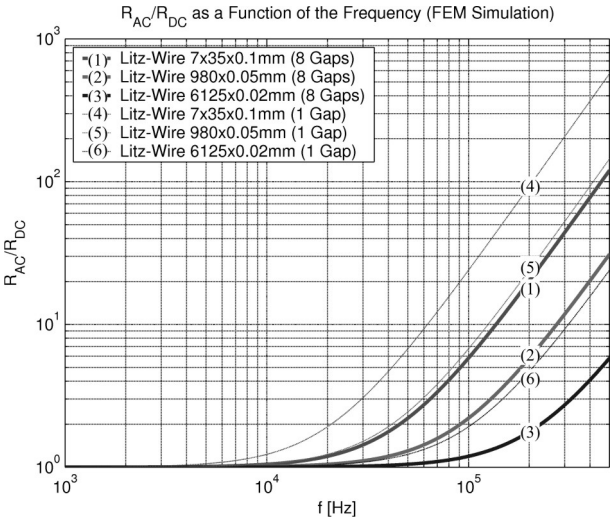


Figure 7: Relation R_{AC}/R_{DC} for different types of litz-wire.

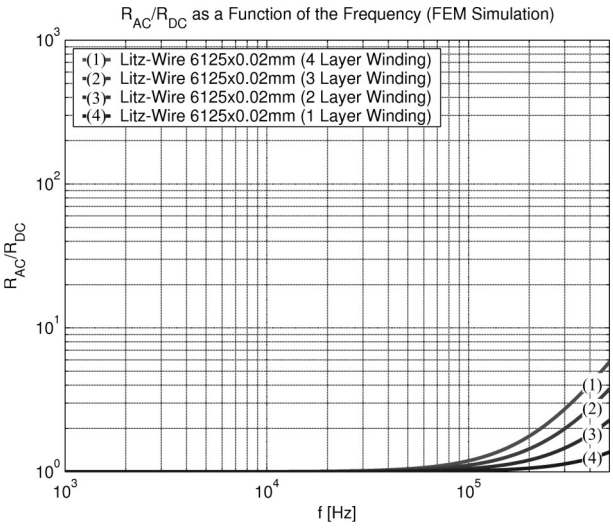
Fig. 7 depicts the relation $\overline{P}_v / \overline{P}_v^{(RMS)} = R_{AC}/R_{DC}$ for different types of litz-wire (R_{DC} is kept constant in all cases). It can be noticed that the AC resistances are increasing much earlier than estimated by the skin depth (1). E.g. for 0.1 mm strand-diameter, we reach $a/\delta \approx 1$ at ~1.75 MHz – in contrast the AC resistance starts to increase around 10 kHz(!).

This is a direct consequence of the fact that proximity losses are predominant here. The diagram shows that frequency could be around five times higher at constant copper losses using 0.02 mm strand diameter instead of 0.1 mm (sinusoidal current).

4 Inductor Optimization: Minimization of Copper Losses



a)



b)

Figure 8:. Relation R_{AC}/R_{DC} (a) for different types of litz-wire and a distributed air gap of 8 single gaps (thick lines), R_{AC}/R_{DC} for different numbers of layers (b).

To reduce the copper losses, the choice of thinner strand diameters may not be the most cost effective way. In many cases, the realization of a distributed air gap could be an alternative [12]. In Fig. 8a the original 5 mm central air gap is split into 8 single air gaps, each of length 0.385 mm. To give a fair comparison, the inductance of the choke is kept constant. It is found that

the advantage of the distributed air gap here is close to the gain of choosing the next thinner strand diameter (thin lines). The influence of the number of layers on the relation R_{AC}/R_{DC} is presented in Fig. 8b. Using a one-layer-winding (see Fig. 11) and the suggested litz-wire 6125x0.02 mm, a 500 kHz resonant power inductor can be realized with copper losses comparable to the DC case.

a) b)

Figure 9: High frequency equivalent circuit model (a) of the inductor, Wayne-Kerr 3260-B impedance analyzer (b) used for measurements.

5 Experimental Verification

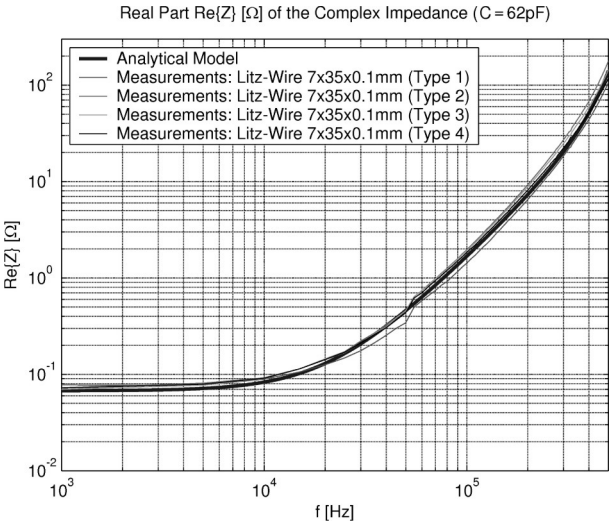


Figure 10: Comparison between simulated and measured results for different types of 7x35x0.1 mm litz-wire (parameter: twist pitch length).

In Fig. 10 the simulation results are compared with measured data. Four different types of litz-wire are used for measurements – each with different twist pitch length. To describe the parasitic effects of the inductor, a constant parallel capacitance C ≈ 62 pF is assumed (see equivalent circuit model in Fig. 9a). The Wayne-Kerr 3260-B impedance analyzer which was used for measurements is shown in Fig. 9b. The (measured) series resistance R_S and series inductance L_S are finally given by the expressions

$$R_s = \mathrm{Re}\{\underline{Z}\} = \frac{R}{\left(1-\omega^2 LC\right)^2 + \left(\omega RC\right)^2} \tag{9a}$$

$$L_s = \omega^{-1} \cdot \mathrm{Im}\{\underline{Z}\} = \frac{L - \omega^2 L^2 C - R^2 C}{\left(1-\omega^2 LC\right)^2 + \left(\omega RC\right)^2} \tag{9b}$$

Fig. 10 illustrates the high accuracy of the model. It is found that the proximity losses are more or less independent from the twist pitch length of the litz-wire. Consequently, the model becomes more general and the only relevant parameters to describe an arbitrary litz-wire are the strand diameter and the copper filling factor.

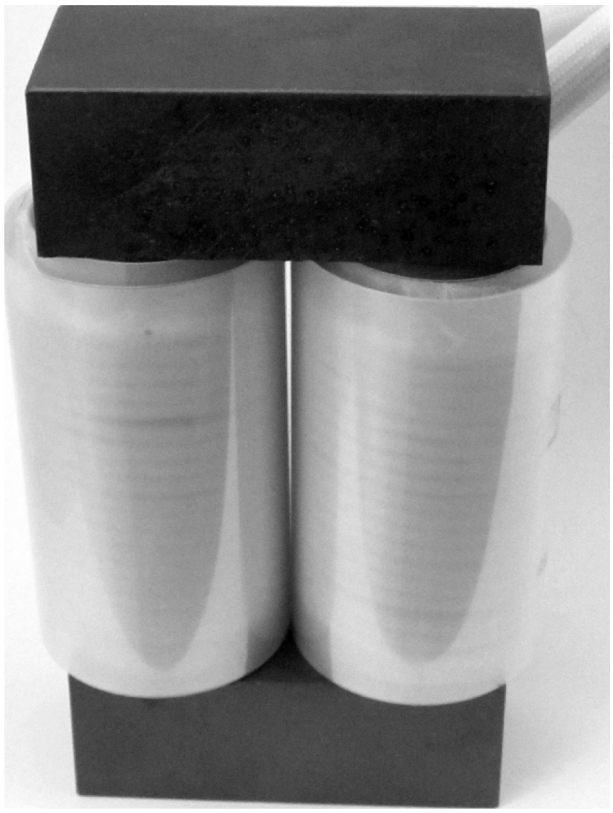


Figure 11: Optimized inductor with distributed air gap and one-layer-winding

6 Conclusion

Promising experimental results show that the litz-wire model allows a precise prediction of the winding AC resistance even if strong air gap fringing fields penetrate the winding. The strand-diameter and the copper filling factor are identified as the only necessary parameters to describe practical litz-wires. This offers the opportunity to optimize these components. If the winding window and the copper cross section are fixed, the strand diameter and the number of gaps (if a distributed air gap can be realized) remain as degrees of freedom.

Otherwise, also the number of layers can be taken into account. In most cases, the main goal of the optimization process is to minimize the AC resistance for a given amount of copper. To exemplify the major dependencies, various parameter studies are shown in the paper based on the example inductor and different types of litz-wire.

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