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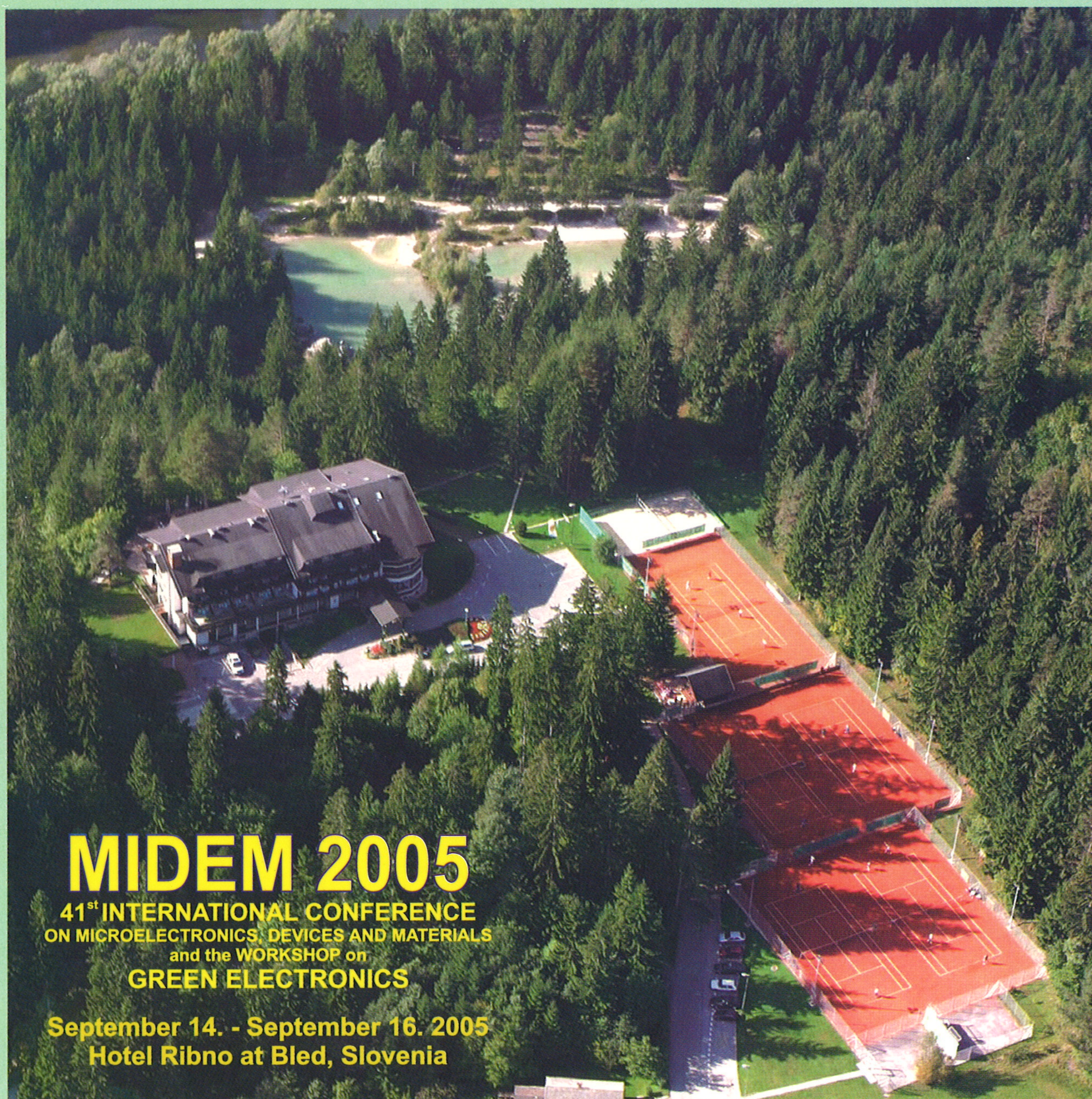

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VSEBINA CONTENT

Obnovitev članstva v strokovnem društvu MIDEM in iz tega izhajajoče ugodnosti in obveznosti

Spoštovani,

V svojem več desetletij dolgem obstoju in delovanju smo si prizadevali narediti društvo privlačno in koristno vsem članom.Z delovanjem društva ste se srečali tudi vi in se odločili, da se v društvo včlanite. Življenske poti, zaposlitev in strokovno zanimanje pa se z leti spreminjajo, najrazličnejši dogodki, izzivi in odločitve so vas morda usmerili v povsem druga področja in vaš interes za delovanje ali članstvo v društvu se je z leti močno spremenil, morda izginil. Morda pa vas aktivnosti društva kljub temu še vedno zanimajo, če ne drugače, kot spomin na prijetne čase, ki smo jih skupaj preživeli. Spremenili so se tudi naslovi in način komuniciranja.

Ker je seznam članstva postal dolg, očitno pa je, da mnogi nekdanji člani nimajo več interesa za sodelovanje v društvu, se je Izvršilni odbor društva odločil, da stanje članstva uredi in **vas zato prosi, da izpolnite in nam pošljete obrazec priložen na koncu revije.**

Naj vas ponovno spomnimo na ugodnosti, ki izhajajo iz vašega članstva. Kot član strokovnega društva prejemate revijo »Informacije MIDEM«, povabljeni ste na strokovne konference, kjer lahko predstavite svoje raziskovalne in razvojne dosežke ali srečate stare znance in nove, povabljene predavatelje s področja, ki vas zanima. O svojih dosežkih in problemih lahko poročate v strokovni reviji, ki ima ugleden IMPACT faktor.S svojimi predlogi lahko usmerjate delovanje društva.

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ULTRASONIC TRANSDUCERS FOR HIGH RESOLUTION IMAGING : FROM PIEZOELECTRIC STRUCTURES TO MEDICAL DIAGNOSTICS

[1] Marc Lethiecq, [2] Franck Levassort and [2] Louis-Pascal Tran-Huu-Hue

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INVITED PAPER

MIDEM 2005 CONFERENCE

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Key words: diagnostics, imaging, high resolution imaging, transducers, piezoelectric transducers

Abstract: The fields of medical diagnostics, namely for examination of skin, eye and blood vessels, of medical research on small animals, of cosmetics and also of non destructive testing of small parts all require very high resolution imaging techniques. Ultrasonic waves, at frequencies between 20 and 100 MHz, allow the observation of structures of several mm size with resolutions in the micrometers range. For this, specific systems including ultrasonic transducers, transmit/receive electronics and image processing and display need to be developed, since classical ultrasonic systems operate only in the 1-15 MHz range. The electroacoustic performance of transducers is one (if not the) key element of such systems. Parameters such as the centre frequency, the relative bandwidth and the loop sensitivity need to be optimised and adjusted for each application. They define both the axial resolution of the images produced and the depth of penetration, and also influence the contrast. To obtain high lateral resolution, the transducers must be focused, which implies either using a focusing lens or shaping the transducer surface. The paper describes current work on piezoelectric materials and structures, namely thick films, developed specifically for these applications. Material properties measured on different samples including thin plates, thick films on several substrates, machined bulk ceramics are presented and compared. The design of transducers using those materials identified as potentially most efficient is discussed, as well as transducer fabrication and performance.

Ultrazvočni pretvorniki za slikanje z visoko ločljivostjo : od piezoelektričnih struktur do medicinske diagnostike

Kjučne besede: diagnostika, slikanje, slikanje z visoko ločljivostjo, pretvorniki, piezo električni pretvorniki

Izvleček: Medicinska diagnostika, npr. pregled kože, oči in žil, preiskave malih živalih, raziskave v kozmetiki, kot tudi neporušno testiranje majhnih sestavnih delov, zahteva tehnike slikanja z visoko ločljivostjo. Ultrazvočni valovi s frekvenco med 20 in 100 MHz omogočajo opazovanje struktur velikosti nekaj milimetrov z mikrometrsko ločljivostjo. V ta namen je potrebno razviti posebne podsisteme, kot so ultrazvočni pretvorniki, oddajno/sprejemna elektronika, prikazovalniki in obdelava slik, saj klasični ultrazvočni sistemi delujejo le v območju 1-15MHz. Elektroakustične lastnosti pretvornikov so ključnega pomena za delovanje takih sistemov. Parametri, kot so sredinska frekvenca, relativna širina pasu in občutljivost morajo biti optimizirani in nastavljeni za vsako uporabo posebej. Le-ti definirajo osno ločljivost posnetih slik, globino prodiranja ultrazvoka in vplivajo na kontrast. Za doseganje visoke lateralne ločljivosti, moramo uporabiti bodisi zbiralno lečo ali ustrezno oblikovati površino pretvornika.

V prispevku opisujemo razvoj piezoelektričnih materialov in debeloplastnih struktur za uporabo v ultrazvočni medicinski diagnostiki. Predstavljamo in primerjamo lastnosti materialov in plastnih struktur na različnih podlagah. Komentiramo načrtovanje, izdelavo in delovanje ultrazvočnih pretvornikov, narejenih iz materialov z največjim piezoelektričnim odzivom.

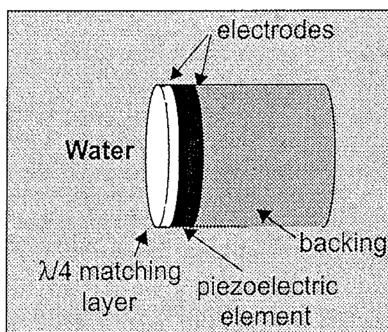
1. Introduction

High frequency ultrasound devices have been developing in many fields such as electronic filters and resonators, material characterisation (acoustic microscopes), non-destructive testing and medical diagnostics. This paper will deal with ultrasonic transducers which are designed for imaging applications, and in particular for medical diagnosis in organs such as skin, eye and blood vessels, as well as for non-destructive evaluation and small animal examinations. This field has generated a great deal of research as well as commercial products, attested by many publications in both specialised and general scientific journals /1-4/. The frequency range starts around 20 MHz, and extends up to 100 MHz. The paper will first present general transducer requirements, then specific piezoelectric materials developed for high frequency will be reviewed and finally transducer fabrication and performance will be discussed (modelling and characterisation).

2. Transducer requirements

The classical single-element transducer is composed of a piezoelectric plate or disc poled along the thickness direction, whose thickness defines the resonance frequency of the device (Figure 1). The piezoelectric element (typ-

ically a ferroelectric ceramic), has an acoustic impedance (*i.e.* around 33 MRa) much higher than biological tissues (close to that of water, *i.e.* 1.5 MRa). This large difference leads to poor acoustic matching and low axial resolution. Consequently, other layers are added to this active layer. First, on its rear face, a thick layer is bonded (backing) /5/. It serves as a mechanical support for the active element, but acoustic energy flows by the rear face. The closer the backing acoustical impedance is to that of the active layer, the more energy is lost. The consequence is a lower sensitivity but a higher axial resolution. The attenuation coefficient and the thickness of the backing layer must be sufficient so that no energy can be radiated back to the active layer, which would produce parasitic echoes. Secondly, on the front (*i.e.* between the piezoceramic and the propagation medium), a matching layer is used. Its design is optimised in order to increase the transfer of energy from the active layer to the tissues /6/ /7/. The thickness of this matching layer is generally around a quarter-wavelength at the resonance frequency, and its acoustical impedance is intermediate between those of the piezoceramic and tissues. The use of a matching layer thus improves the sensitivity of the transducer. Moreover, since the acoustical energy can better flow towards the tissues, the duration of acoustical resonance in the active layer is decreased. Consequently, the matching layer also improves axial resolution. Influence of these two elements on the impulse and frequency responses transducers is shown in Figure 1 and a trade-off has to be found for each application. The active layer is typically a PZT-based material, while matching layers and backings are polymer-based.



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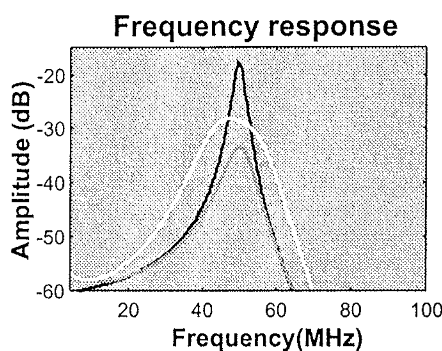

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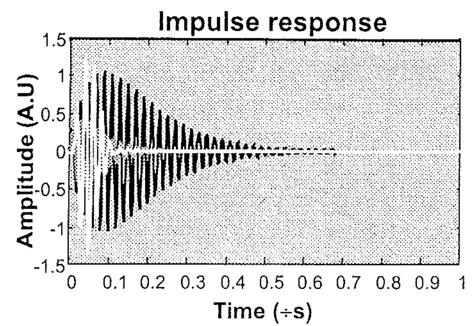


(c)

Figure 1: *(a) Classical diagram of a single-element transducer.*
(b) and (c) Frequency and impulse responses of: black line: piezoelectric element (water on front face and air on rear face), grey line: piezoelectric element+backing, white line: with matching layer.

The radiation pattern of a focused single-element transducer is defined by the size of the active element (D) and the focal distance (F) (Figure 2). In the case where a lens is used for focusing, (F) can be deduced from the lens curvature (R_C) and the sound wave velocities in the lens and propagation media (Figure 3).

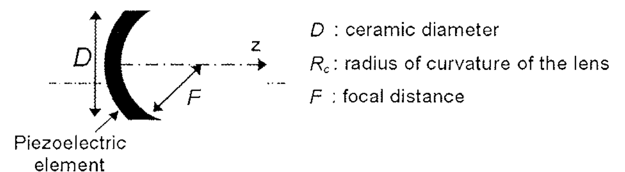


Figure 2: *Shape-focused transducer.*

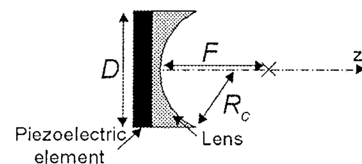


Figure 3: *Lens-focused transducer.*

Lateral resolution is linked to the width of the acoustic beam and is optimum at the focal distance. Approximate expressions of this lateral resolution ($R_{lateral}$), depth of field (DOF) and axial resolution (R_{axial}) for a spherical shape transducer are defined (eq. 1). The ratio between the focal distance and the diameter of the piezoelectric element, called the f-number ($f_{\#}$), allows to define the trade-off between lateral resolution and depth of field. λ is the wavelength at nominal frequency and BWR_{-6dB} is the relative bandwidth at -6dB.

$$f_{\#} = \frac{F}{D}, \qquad R_{lateral} \approx \lambda \times f_{\#},$$

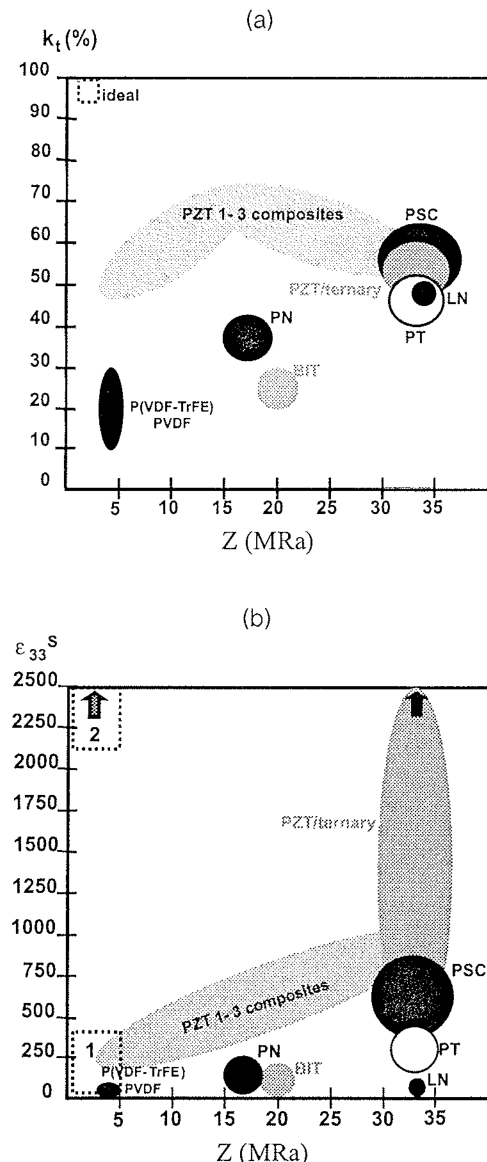
$$DOF \approx 7\lambda \times f_{\#}^2, \qquad R_{axial} \approx \frac{\lambda}{2BWR_{-6dB}} \qquad (1)$$

The resolutions and depth of field can change of several orders of magnitude according to frequency. High frequencies lead to high resolutions but, due to increase of attenuation in tissues, the depth of penetration in the explored medium is reduced. The acoustical properties of the explored medium as well as of the driving electronics also influence imaging performance /4//8/.

For typical fixed values for medical imaging as the centre frequency at 50 MHz (i.e. a f-number of 2.5, a focal distance at 7.5 mm, a relative bandwidth (-6dB) at 60%), the corresponding diameter D is at 3 mm, the thickness of the piezoelectric element (ceramic) is around 45 μm, the axial and lateral resolutions are respectively around 30 and 75 μm, and the depth of field around 1.3 mm. These resolutions correspond to those generally required for skin imaging.

3. Piezoelectric materials

For the piezoelectric material, in particular for medical applications, two of the most important material parameters are the effective electromechanical coupling coefficient k_{eff} of the main vibration mode used and the acoustic impedance Z_{ac}. The k_{eff} factor represents the piezoelectric activity of the material in the considered mode of vibration, in other words the capability of the material to convert electrical energy into acoustical energy (or vice-versa) in a short time; it should of course be as high as possible. This factor depends not only on the material properties but also on the geometry of the active element. In medical imaging applications, all vibration modes are longitudinal, *i.e.* the displacements are in the poling direction which defines the thickness dimension. For large plates or discs (thickness much lower than lateral dimensions), the thickness coupling factor k_t is used. For bars or pillars (thickness higher than lateral dimensions), the factor is k_{33}. For the intermediate case of an array element (one small and one large lateral dimensions with a thickness value between them), k'_{33} factor is defined /9/. The value of the dielectric constant also has an important role on the electrical matching. Figure 4 represents values of the thickness mode coupling factor (k_t) versus the acoustic impedance (Z_{ac}) for a wide range of available piezoelectric materials. It can be observed that no material allows to obtain both high coupling and low acoustic impedance (ideal area on Figure 4). The best trade-off must be found among these materials. For almost all medical transducers applications, PZT piezoceramics are used because of their high coupling factor, even if their acoustic impedance is high, since this can be compensated for by using acoustic matching layers in the transducer structure. For a given application, properties such as dielectric constant and grain size allow to choose a specific material reference. A large range of properties can be found from relatively low (a few hundred) to very high (a few thousand) relative dielectric constants with grain sizes from one to ten micrometers. For large area devices such as single element transducer, a moderate dielectric constant allows good electrical matching to cables and electronics (which are typically at 50 to 80 ohms) (area 1), while array elements require much higher dielectric constants (area 2).

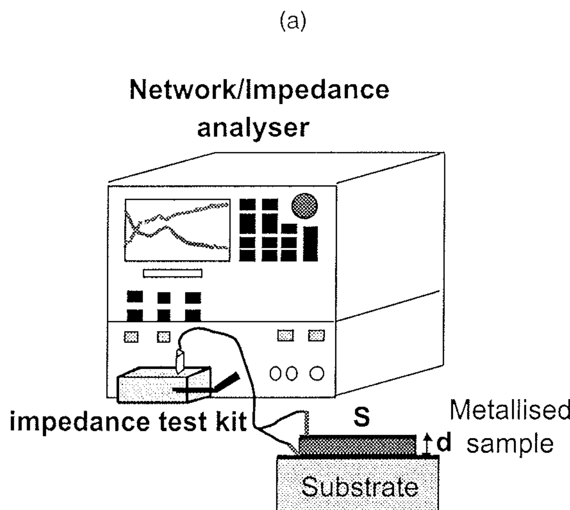


PZT: Lead zirconate titanate, **PT**: Lead titanate, **PN**: Lead metaniobate, **BIT** : Bismuth titanate, **PSC** : Piezoelectric single crystals, **LN** : Lithium Niobate, **PZT 1-3 composites** : PZT and polymer

Figure 4: (a) Electromechanical coupling factor in thickness mode (k_t) and (b) Dielectric constant at constant strain versus acoustical impedance for a wide range of piezoelectric materials.

Measurements of the complex electrical impedance as a function of frequency allow the dielectric, mechanical and electromechanical properties to be obtained by a fitting process /9-11/. The set-up is composed of a network analyser with its impedance test kit and a spring clip fixture to make electrical contacts with the electroded piezoelectric material (Figure 5(a)). These contacts have a great importance in particular at high frequency, since to stay in free resonator condition, their sizes must be very small in comparison with the size of the measured sample and the forces applied must not disturb the resonance mode. Figure 5(b) shows the typical resonance of a PZT disk made by tape-casting which has an antiresonant frequency around 50 MHz. At high frequency, the piezoelectric element is often deposited on a substrate during the fabrication process (Figure 5(a)) and the experimental electrical impedance depends on this substrate. With an electrical equivalent circuit, such as KLM which is well adapted to multilayer structures (electrodes, piezoelectric layer and substrate), and knowing all the acoustic properties of electrodes and substrate, the fitting process allows to obtain the properties of the piezoelectric layer (Figure 4 (c))/12/ /13/.

(a)



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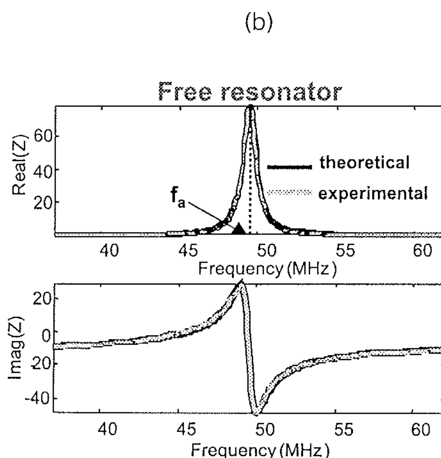

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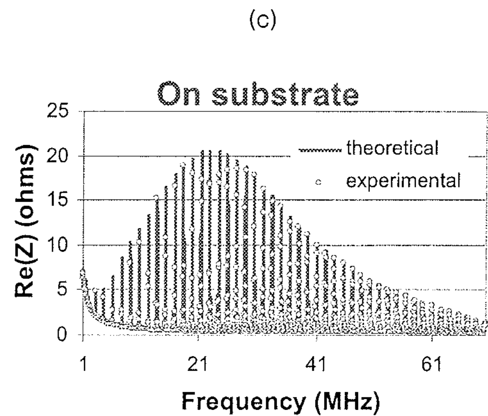

Figure 5: (a) experimental set-up for electrical impedance measurements, (b) experimental and theoretical complex impedance (fit) of high frequency piezoelectric disk in free resonator conditions, (c) experimental and theoretical impedance (real part) (fit) of high frequency piezoelectric thick film on alumina substrate.

Typical parameters characterised are the following:

- Resonant (f_r) and antiresonant (f_a) frequencies which correspond respectively to maximum of real admittance and real impedance;
- The thickness coupling factor (vibration corresponding to a thickness mode) can be calculated with

$$k_t = \sqrt{\frac{\pi}{2}\frac{f_r}{f_a}\cot\left(\frac{\pi}{2}\frac{f_r}{f_a}\right)} \qquad (2)$$

- The longitudinal wave velocity $v = 2df_a$ (d: thickness of the piezoelectric sample) (3)
- Dielectric constant ε is obtain from the capacitance C_0 after resonance and dimensions;
- Mechanical quality factor (or mechanical losses δ_m)

$$Q_m = \frac{f_a}{\Delta f} \qquad (4)$$

  where Df corresponds to the frequency width at half the maximum resistance;
- Dielectric losses appear as an offset on resistance curves, the measurement can be made at twice the anti-resonant frequency and they can change with frequency.

Piezopolymers such as PVDF or copolymers /14/ /15/ can be purchased as films with thickness of one to a few tens of microns which can be directly used for high frequency applications. Their coupling factors are relatively low (between 15 and 30%) and relative clamped dielectric constant is low (around 5). These two last properties tend to give a relatively low sensitivity and the electric matching is difficult. But their acoustic impedance is low and close to that of tissues (between 4 and 5 MRa), so acoustic matching is not indispensable (Table 1).

Table 1: Main properties of a P(VDF-TrFE) piezoelectric copolymer film.

material	$\varepsilon_{33}^S/\varepsilon_0$	v_l (m/s)	k_t (%)	δ_e (%)	δ_m (%)	Z (MRa)	ref
P(VDF-TrFE)	4.1	2380	29	6.9	4.0	4.6	[16]

$\varepsilon_{33}^S/\varepsilon_0$: clamped dielectric constant; v_l: longitudinal wave velocity; k_t: thickness coupling factor; δ_e: dielectric losses; δ_m: mechanical losses; **Z**: acoustic impedance;

The second main and determinant advantage is the flexibility of the film which allows a direct focusing and avoids the addition of a lens (Figure 6). Even with a relatively low (k_t), these materials are widely used for high frequency transducer fabrication in the range of from 20 MHz to over 100 MHz.

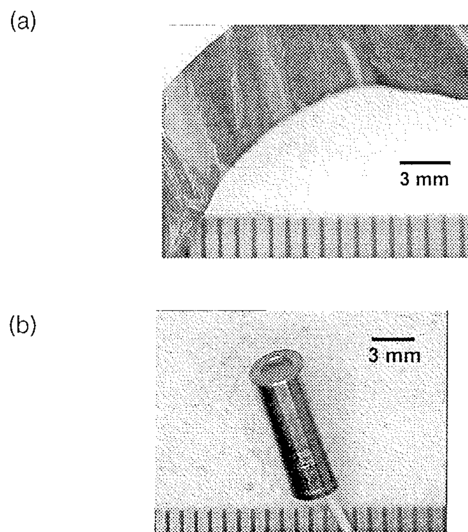

Figure 6: (a) Copolymer sheet and (b) high frequency copolymer based transducer.

Ceramic thick films are a very promising alternative. Many processes are possible and have been developed /17/ such as screen-printing, tape-casting, spin or dip coating processes and spray techniques /15/ /18/ /19/ /20/ /21/ to make piezoelectric thick films (few tens of microns). The three first ones are widely used techniques, in particular for imaging applications. In each case, the samples (generally circular shape) are made directly in final shape and avoid machining, namely lapping, which can represent a critical step where micro-cracks or breakdown can appear. The tapes can be used to manufacture thin self-supported disks as shown on Figure 7.

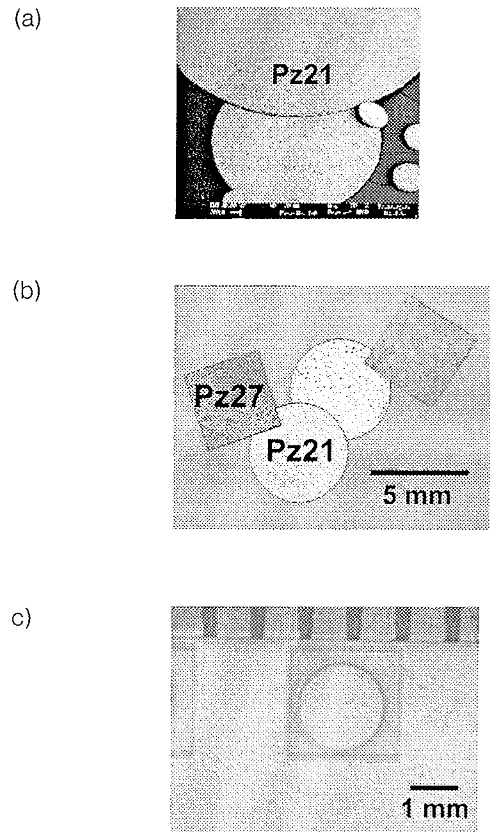

Figure 7: Tape-casted self supported disk photographs. (a) (b) from Ferroperm piezoceramics (Denmark), (c) from Laboratoire de Céramique (EPFL, Switzerland)

Table 2 summarises several representative characteristics of self-supported samples where properties are slightly lower than those of bulk ceramics (in particular k_t) but their actual performance allow to integrate these elements in transducers which deliver satisfying properties.

Table 2: Properties of self supporting samples made by tape-casting.

Materials	$\varepsilon_{33}^S/\varepsilon_0$	k_t (%)	f_a (MHz)	ρ (kg/m^3)	δ_m (%)	ref
Pz21 (PNNZT)	1920	43	33.9	7420	4.7	[22]
Pz29 (PZT)	1035	35.5	34.1	6900	6.0	[22]
PZT	675	43	46	-	3.6	[23]

$\varepsilon_{33}^S/\varepsilon_0$: clamped dielectric constant; k_t: thickness coupling factor; f_a : antiresonant frequency; ρ: density; δ_m: mechanical losses.

The substrates used for the deposited thick films can be used in two ways. First, the substrate can be chosen to be used directly as a backing for the transducer /24/. Many conditions are necessary for this in terms of sintering temperature (for the thick films) and acoustical properties for the transducer. Porous PZT can be a good choice (Figure 8(a)). This method leads to an integrated device. Secondly, the substrate can be chosen only as an intermediate material. For example, The PZT thick film is deposited on an aluminium substrate (Figure 8(b)) /25/. On the other side, epoxy resin loaded with Ag powder is added as the future backing. Finally, the Al substrate is etched and a new electrode is deposited on the front face of the thick film. This method allows to optimise the choice of these two materials for the future transducer. For these two cases, properties of the piezoelectric thick films are given in Table 3 where the performance obtained can be relatively high, but the reproducibility remains an important problem to be solved. Moreover, the choice of the bottom electrode material and thickness can also greatly influence the final properties.

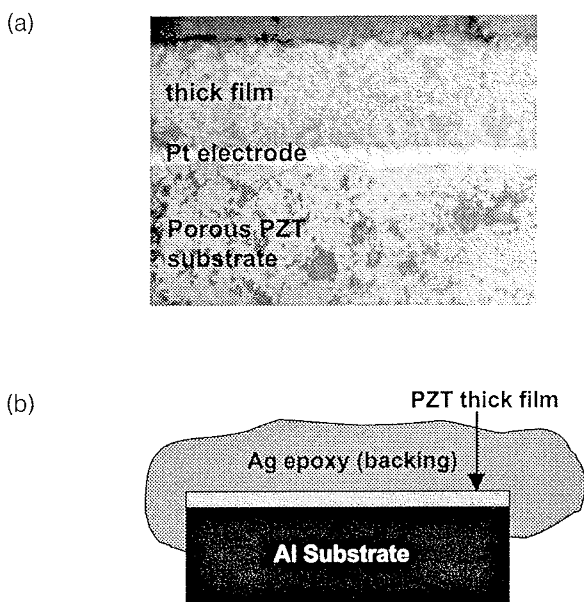

Figure 8: (a) Cross section of optical microscope photograph of screen-printed PZT thick film on Porous PZT substrate from JSI - Slovenia, (b) screen-printing with intermediate substrate.

Different types of piezocomposites have also been developed for high frequency applications /26-41/ , namely 1-3 connectivity including fibres and hollow spheres, as well as curved films.

4. Transducer fabrication and performance

4.1. Transducer fabrication

A fabrication technique, described by Lockwood *et al.* /42/, has allowed to increase significantly the sensitivity of focused transducers, for centre frequencies around 50 MHz, compared to the more classical polymer-based devices. This method has been applied to both ceramic and single crystals. First, bulk ceramic is bonded on a malleable substrate (typically conductive epoxy layer). Ceramic is then lapped to required thickness (generally few tens of microns). The third step is the lapping of the substrate generally to around 100 microns and machining of the structure to final diameter. The two-layer composite is then heated and pressed into a spherically shaped well. The diameter of the well is the focal distance of the transducer. The shell is cooled and removed from the well. Finally, an attenuating backing is added. Two possibilities exist for focusing. The first is the use of a spherically-shaped active element (Figure 9(a)), the second is the addition of lens (Figure 9(b)).

4.2. Transducer performance: overview of published results

The two next Tables (Tables 4 and 5) give an overview of published results on high frequency transducers using materials and/or process described in previous sections. Table 4 specifies essentially the characteristics (fabrication process, dimensions or material used) while Table 5 gives the corresponding performance such as bandwidth and sensitivity /44/ /33/ /45/ /25/ (if authors give these values). Concerning the sensitivity, the comparison between values is not always possible since the definition used by different authors is not identical.

Table 3: Properties of screen-printed samples on different substrates.

material	process	substrate	e (μm)	$\varepsilon_{33}^S/\varepsilon_0$	v_l (m/s)	k_t (%)	δ_e (%)	δ_m (%)	Z (MRa)	ref
PZT/PGO	Screen-printing	PZT	35.5	334	3240	47	4.7	4.8	-	[24]
PZT/PGO	Screen-printing	Al_2O_3	39	342	3940	39.7	2.0	1.5	-	[24]
PZT	Spin coating	Al	20	220	3950	24.4	-	-	21.8	[25]

e_{33}^S/ε_0: clamped dielectric constant; v_l: longitudinal wave velocity; k_t: thickness coupling factor; δ_e: dielectric losses; δ_m: mechanical losses; **Z**: acoustic impedance.

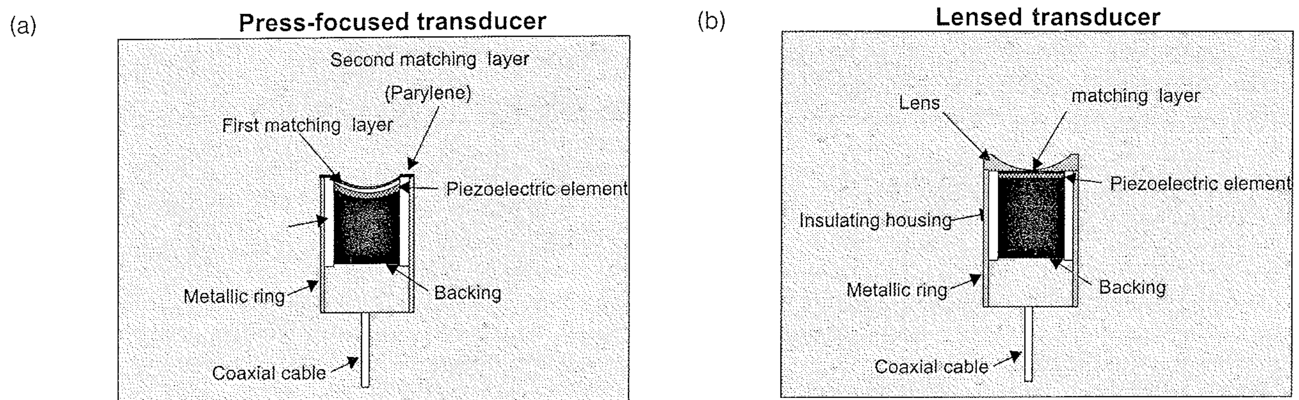

Figure 9: Cross-sections of schematic representation of press&lens-focused transducers.

Table 4: Overview of published results on high frequency transducers (part 1).

Material	e (μm)	f_c(MHz)	shaping	$F_\#$/F (mm)	Z_b(MRa)-material	Z_{m1}(MRa)-material	Z_{m2}(MRa)-material
P(VDF-TrFE) [16]	17	34	prefocused	2.7/6	15 – Ag epoxy	no	no
PVDF[33]	9	48.1	prefocused	2-3/-	3.15 –pure epoxy	no	no
$LiNbO_3$ crystal [44]	-	78	prefocused	2/-	5.9 – Ag epoxy	7.3 – Ag epoxy	2.6 - parylene
$LiNbO_3$ crystal [33]	60	44.5	Lens (epoxy)	2-3/-	5.9 – Ag epoxy	7.3 – Ag epoxy	no
$LiNbO_3$ crystal [45]	-	200	prefocused	1.15/0.8	4.3 – Ag epoxy	no	no
PT ceramic [33]	32	45.1	prefocused	2-3/-	5.9 – Ag epoxy	3- parylene	no
Fiber composite [34]	32	31	prefocused	-/17.5	Porous polymer	no	no
PT hollow sphere [41]	70-90	39.8	-	-/1.43	6 - Ag epoxy	parylene	no
PZT thick film [25]	-	72	prefocused	-/2.8	Ag epoxy	no	no

e: thickness of the piezoelectric material; f_c : transducer centre frequency; **F**: focal distance; $F_\#$: f-number; Z_b: acoustic impedance of the backing- corresponding material; Z_{m1} and Z_{m2}: acoustic impedances of the first and second matching layers - corresponding material;

In these nine high frequency transducers, a wide range of centre frequencies is observed (between 31 and 200 MHz). The press-focused process is essentially used. A majority of transducers have been designed to have a f-number between 2 and 3. With PT hollow sphere, this f-number is lower. For backing material, epoxy loaded with silver particles is mainly used. For matching layers, technology takes a very important place and generally only one matching layer is added. These matching layers are often in parylene which allows uniform and repeatable deposition of controlled-thickness layers.

In accordance with properties of piezoelectric materials, $LiNbO_3$ and PT based single-element transducers deliver best performance corresponding to a good trade-off between resolution and sensitivity. Press-focused process delivers better performance than lens-focused process /44/. Attenuation due to various lens thickness decreases

Table 5: Overview of published results of high frequency transducers (part 2).

Material	D (mm)	tuning	BW (%)	AR (μm)	LR (μm)	IL (dB)
P(VDF-TrFE) [16]	2.2	no	70	51	-	-
PVDF [33]	3	no	118	-	-	-45.6
$LibO_3$ crystal [44]	3	yes	73	-	-	-13.5
$LiNbO_3$ crystal [33]	3	yes	74	-	-	-21.3
$LiNbO_3$ crystal [45]	0.7	-	22	12	14	-18
PT ceramic [33]	3	yes	47	-	-	-23.7
Fiber composite [34]	5	no	118	-	-	-29.3
PT hollow sphere [41]	2	no	33	-	-	-20.1
PZT thick film [25]	1	no	52	20	295	-46

D: Aperture; **tuning**: addition or not of a self inductor and a transformer; **BW**: bandwidth at -6dB; **AR**: axial resolution (-6dB); **LR**: lateral resolution (-6dB); **IL**: Insertion loss.

the sensitivity (around -6dB for $LiNbO_3$ transducers /44/) even if bandwidth is slightly increased.. Finally, the transducer ($LiNbO_3$ based) with two matching layers (Ag epoxy and parylene) gives, as expected, the highest performance.

4.3 Comparison of transducer performance.

Electroacoustic behaviour of transducers includes electrical input impedance that will govern energy transfer between the imaging system and the transducer, pulse-echo response whose amplitude is linked to sensitivity and duration to axial resolution, and frequency response equal to the Fourier transform of pulse-echo response, which defines centre frequency and bandwidth. All these curves can be predicted with the assumption of single axis vibration, using equivalent electrical circuits such as KLM /10/ /46/ or others /47/. All transducer layers are taken into account as well as electrical elements such as electrical matching and cables. Finite element methods are also available /48/ /49/ in cases where no assumptions can be made on acoustic modes. Acoustic radiation patterns allow to define lateral resolution, which is high when lateral beam dimensions are low, and acoustic noise level (the off-axis power level measured in dB using the on-axis power level as a reference). The appearance of side lobes tends to increase acoustic noise level. Lateral resolution is responsible for image sharpness and low parasitic lobe levels ensure the absence of artefacts in the lateral direction. Radiation pattern calculations can be performed by applying Huygen's principle (*i.e.* the transducer surface is assumed to be a series of point-sources, and the pressure radiated at any point is the sum of pressures radiated by each of the point-sources /50/). For simple geometry (circular, annular or rectangular transducers), analytical results have been derived (impulse diffraction theories), and allow more efficient calculations /51/ /52/. Five different piezoelectric materials have been retained for comparison: P(VDF-TrFE) copolymer, $LiNbO_3$ single crystal, lead titanate ($PbTiO_3$) ceramic, soft PZT ceramic and finally PMN-PT single crystal. For these simulations, three parameters have been fixed: the transducer centre frequency (50 MHz), the active area of the piezoelectric element (diameter of 3 mm) and the length of the 50 ohms coaxial cable (1.5 m). One matching layer is considered. A self inductor and a transformer are also taken into account. Table 6 gives all the parameters of piezoelectric materials used for the simulations (values from literature).

The optimisation of transducer performance allows to determine the characteristics /43, 53-56/ of the matching layer (acoustical impedance and thickness), backing (acoustical impedance), value of the self inductor and ratio of the transformer. The performance results are specified in Table 7. These simulations do not take into account focusing by a lens. Impulse responses are represented in Figure 10. Due to low k_t, the P(VDF-TrFE) based transducer delivers a low sensitivity. The results for the $PbTiO_3$, soft PZT and single crystal (PMN-PT) are similar. The electrical matching allows to compensate for the difference in dielectric constants. The $LiNbO_3$ single crystal delivers a similar bandwidth but a lower sensitivity since the dielectric constant is much lower than that of the three previous materials.

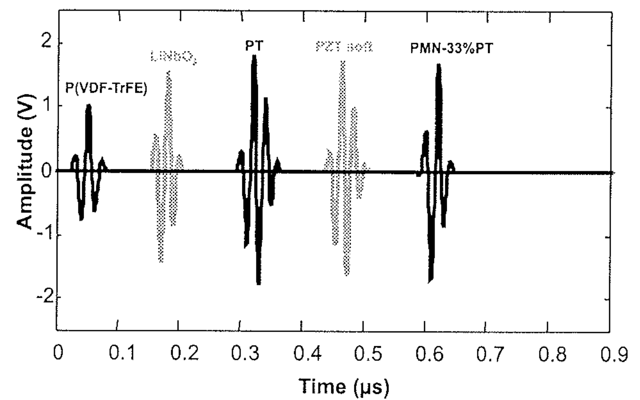

Figure 10: Electroacoustic responses of the five simulated transducers.

5. Conclusion

PZT-based thick films are very promising for high frequency ultrasonic transducer applications since their electromechanical properties are high and they are compatible with backing materials. Their performance has been demonstrated in non focused configurations, and current work aims at obtaining curved films in order to focus the beam without use of a lens.

Table 6: Piezoelectric material parameters for high frequency transducer simulations.

Material	k_t (%)	$\varepsilon_{33}^S/\varepsilon_0$	ρ (kg/m^3)	v_l (m/s)	δ_e (%)	δ_m (%)	Z (MRa)
P(VDF-TrFE) [16]	33	4.1	1932	2380	6.9	4.0	**4.6**
$LiNbO_3$ crystal [33]	**49**	28	4640	7340	0.1	0.01	34.1
PT ceramic [33]	**49**	**200**	6900	5200	0.9	0.83	35.9
PZT soft ceramic [57]	50	800	7900	4390	2.5	2.7	34.7
PMN-33%PT [58]	**62**	712	8060	4645	-	-	37.4

k_t: thickness coupling factor; $\varepsilon_{33}^S/\varepsilon_0$: clamped dielectric constant; ρ: density; v_l: longitudinal wave velocity; δ_e: dielectric losses; δ_m: mechanical losses; **Z**: acoustic impedance.

Table 7: Design and performance parameters of high frequency single element transducers.

Material	e (μm)	Z_b(MRa)	Z_{m1}(MRa)	e_{m1}(xλ/4)	tuning	BW(%)	IL(dB)
P(VDF-TrFE)	22.4	1.2	2	1.5	Yes	71	26
$LiNbO_3$ crystal	69.6	4.5	4	1.2	Yes	70	23.4
PT ceramic	51.0	4.3	4.3	1.2	Yes	53	19.7
PZT soft ceramic	43.1	4	4.2	1.2	Yes	54	20.6
PMN-33%PT	44.3	2.7	4	1.0	Yes	68	22

e: thickness of the piezoelectric material; Z_b and Z_{m1}: acoustic impedances of the backing and matching layer; e_{m1}: thickness of the matching layer normalised by a quarter-wavelength; **tuning**: addition or not of a self inductor and a transformer; **BW**: bandwidth at -6dB; **IL**: Insertion loss

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DECISION DIAGRAMS AND DIGITAL TEST

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Abstract: *The most important question in testing today's complex digital systems is: how to improve the testing quality at continuously increasing complexities of systems? Two main trends can be observed: defect-orientation to increase the quality of testing, and high-level modelling to reduce the complexity problems of diagnostic analysis. Both trends can be joined in the hierarchical approach. Decision Diagrams (DD) serve as a good tool for hierarchical modelling and diagnostic analysis of digital systems. Traditional Binary Decision Diagrams are well known for working with logic level. New generalizations of BDDs in a form of High-Level DDs and Vector DDs as efficient tools for test generation and fault simulation of complex digital systems are discussed in the paper. Finally, two examples of hierarchical test generation tools based on DDs together with corresponding experimental results are given.*

Odločitveni diagrami in digitalno testiranje

Kjučne besede: testiranje, testiranje digitalnih sistemov, odločitveni diagrami, hierarhično modeliranje, odločitveni diagrami na višjem nivoju, vektorski odločitveni diagrami

Izvleček: Eno najpomembnejših današnjih vprašanj pri testiranju digitalnih sistemov je, kako izboljšati zanesljivost testiranja ob stalnem naraščanju kompleksnosti sistemov ? Opažamo dvae glavni smeri : eno, ki je usmerjena k odkrivanju napak in drugo, ki obsega modeliranje na višjem nivoju, kar zmanjša zapletenost diagnostične analize. Obe smeri lahko združimo v hierarhični pristop. Odločitveni diagrami (DD) služijo kot dobro orodje za hierarhično modeliranje in diagnostično analizo digitalnih sistemov. Tradicionalni binarni odločitveni diagrami (BDD) so dobro poznani pri delu z logičnimi nivoji. V prispevku obravnavamo nove posplošitve BDD v obliki DD na višjem nivoju in vektorske DD kot učinkovita orodja za tvorbo testov in simulacijo napak pri kompleksnih digitalnih sistemih. Na koncu podamo dva primera orodja za tvorbo hierarhičnih testov na osnovi DD skupaj z ustreznimi eksperimentalnimi rezultati

1. Introduction

Test generation for digital systems encompasses three activities: selecting a description method, developing a fault model and generating tests to detect the faults covered by the fault model. The efficiency of test generation (quality, speed) is highly depending on the description method and fault models which have been chosen.

As the complexity of digital systems continues to increase, the gate level test generation methods have become obsolete. Other approaches based mainly on higher level functional and behavioral methods are gaining more popularity /1-3/. However, the trend towards higher level modelling moves us even more away from the real life of defects and, hence, from accuracy of testing. To handle adequately defects in deep-submicron technologies, new fault models and defect-oriented test methods should be used. On the other hand, the defect-orientation is increasing even more the complexity. To get out from the deadlock, the two opposite trends - high-level modelling and defect-orientation - should be combined into hierarchical approaches. The advantage of hierarchical approaches compared to high-level functional modelling lies in the possibility of constructing test plans on higher levels, and modelling faults on more detailed lower levels.

The drawback of traditional multi-level and hierarchical approaches to digital test lies in the need of different dedicated languages and models for different levels. Uniform methods for hierarchical diagnostic modelling of digital systems can be developed by using Decision Diagrams (DD) /4-9/. Binary DDs (BDD) have found already very broad applications in design and test on the logic level /4-5/. A special class of BDDs, Structurally Synthesized BDDs (SSBDD) can be used to represent gate-level structural faults directly in the graph model /6,7/. Recent research has shown that generalization of BDDs for higher levels provides a uniform model for both gate and RT level or even behavioral level test generation /8,9/.

The disadvantage of the traditional hierarchical test approaches is the use of gate-level stuck-at fault (SAF) model. It has been shown that high SAF coverage cannot quarantee, high quality of testing /10/. The types of faults that can be observed in a real gate depend not only on the logic function of the gate, but also on its physical design. These facts are well known but usually, they have been ignored in engineering practice. In earlier works on layout-based test techniques /11,12/ a whole circuit having hundreds of gates was analysed as a single block. Such an approach is computationally expensive and highly impractical as a method of generating tests for real VLSI designs.

In this paper, we present, first, in Section 2 a method for mapping faults from lower levels to higher levels. For this purpose the concept of functional fault model is used. Thereafter, for hierarchical diagnostic modelling of digital systems, DDs are presented. In Section 3 SSBDDs are described for logic level test generation, and in Section 4 the use of higher level DDs for test generation is discussed. Some experimental data are presented in Section 5 to illustrate the efficiency of the described hierarchical approach. Section 6 concludes the paper.

2. Functional fault model in hierarchical test

Consider a Boolean function $y = f(x_1, x_2, ..., x_n)$ implemented by an embedded component C in a digital circuit. Introduce a Boolean variable d for representing a given physical defect in the component, which may affect the value y by converting the Boolean function f into another faulty function $y = f^d(x_1, x_2, ..., x_n)$. Introduce for the block C a generic parametric function

$$y^* = f^*(x_1, x_2, ..., x_n d) = \bar{d} f \vee d f^d \tag{1}$$

as a function of the defect variable d, which describes the behavior of the component simultaneously for both possible fault-free and faulty cases. The solutions of the Boolean differential equation

$$W^d = \frac{\partial y^*}{\partial d} = 1 \tag{2}$$

describe the conditions which activate the defect d on a line y. The parametric modeling of a given defect d by equations (1) and (2) allows us to use the constraints W^d = 1, either in defect-oriented fault simulation to check if the condition (2) is fulfilled (i.e. if the defect d is tested by the given pattern), or in defect-oriented test generation to solve the equation (2) for testing the defect d. The conditions W^d allow to map physical defects to logic level. The constraint W^d = 1 defines how a lower level fault d should be activated at a higher level to a given node y.

Table 1: Activating conditions for different defects

No	Defect	Conditions W^r
1	SAF $x_k \equiv 0$	$x_k = 1$
2	SAF $x_k \equiv 1$	$x_k = 0$
3	Short between x_k and x_l	$x_k = 1, x_l = 0$
4	Exchange of lines x_k and x_l	$x_k = 1, x_l = 0$, or $x_k = 0, x_l = 1$
5	Delay fault on the line x_k	$x_k = 1, x'_k = 0$, or $x_k = 0, x'_k = 1$

Table 2: Library defect table for a complex gate AND2,2/NOR2

i	Fault d_i	Erroneous function f^{di}	Input patterns t_j															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	B/C	not((B*C)*(A+D))				1								1	1	1		
2	B/D	not((B*D)*(A+C))				1								1	1		1	
3	B/N9	B*(not(A))	1	1	1					1	1	1	1					
4	B/Q	B*(not(C*D))	1	1	1						1	1	1		1	1	1	
5	B/VDD	not(A+(C*D))									1	1	1					
6	B/VSS	not(C*D)													1	1	1	
7	A/C	not((A*C)*(B+D))				1				1					1	1		
8	A/D	not((A*D)*(B+C))				1				1					1		1	
9	A/N9	A*(not(B))	1	1	1		1	1	1					1				
10	A/Q	A*(not(C*D))	1	1	1		1	1	1						1	1	1	
11	A/VDD	not(B+(C*D))					1	1	1									
12	C/N9	not(A+B+D)+(C*(not((A*B)+D)))		1			1	1			1	1						
13	C/Q	C*(not(A*B))	1	1		1	1	1		1	1	1		1				
14	C/VSS	not(A*B)				1				1				1				
15	D/N9	not(A+B+C)+(D*(not((A*B)+C)))			1		1		1		1		1					
16	D/Q	D*(not(A*B))	1		1	1	1		1	1	1		1	1				
17	N9/Q	not((A*B)+(B*C*D)+(A*C*D))				1												
18	N9/VDD	not((C*D)+(A*B*D)+(A*B*C))													1			
19	Q/VDD	SA1 at Q				1				1				1	1	1	1	1
20	Q/VSS	SA0 at Q	1	1	1		1	1	1		1	1	1					

Some examples of the conditions W^d for different type of defects (where SAF is a particular extreme case) are given in Table 1 (here x_k is the observable variable, and x'_k is the variable observed at the previous time moment).

The event of erroneous value of y can be described as $dy = 1$, where dy means Boolean differential. A functional fault representing a defect d can be described as a couple (dy, W^d): at the presence of the physical level defect d, we will have an higher level erroneous signal $dy = 1$ if the condition $W^d = 1$ is fulfilled.

The functional fault model (dy, W^d) allows to use for test generation for any physical defect d traditional stuck-at fault test generators. To generate a test for a defect d, a test pattern should be generated for the stuck-at fault $y \equiv (1 \oplus y(W^d))$ at the additional condition $W^d = 1$. Here $y(W^d)$ is the expected value of y determined by the condition $W^d = 1$.

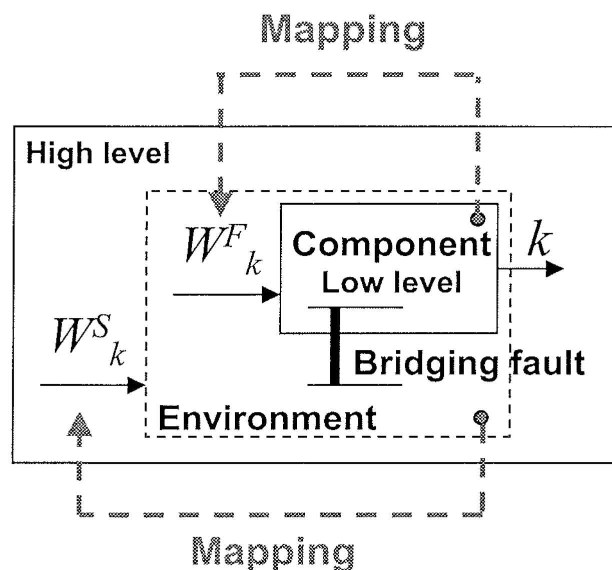

Figure 1: Mapping faults from lower level to higher level

In the described approach we have to characterize all possible defects in all library cells, and represent the results as defect tables or as optimized sets of defect activating conditions $W^F = \{W^{d,i}\}$. The defect characterization may be computationally expensive, but it is performed only once for every library cell. An example of the fault table for the complex gate AND2,2/NOR2 with a function y = ¬(AB Ú CD) is presented in Table 2 /13/.

The defect lists W^F_k of library components C_k embedded in the circuit can be extended by additional physical defect lists W^S_k in the close network environment of the component C_k to take into account also the wrong behaviour of C_k influenced by the outside environment (bridging faults, crosstalkings etc.). For these defects additional characterization should be carried out by a similar way as for the library cells.

3. Diagnostic modelling of digital systems by BDDs

Decision Diagrams (DD) can serve as a basis for a uniform approach to test generation for mixed-level representations of systems, similarly as we use the Boolean algebra for the plain logic level. In the following it is shown how the traditional logic level test methods can be implemented on Binary Decision Diagrams (BDD) /6,7,14/ as a special class of DDs, and then we generalize the procedures developed for BDDs for a general class of DDs /6,16,17/ to handle the test generation problems at higher levels of systems.

Structurally synthesized BDDs. In 1959 C.Y.Lee introduced a method for representing digital circuits by Binary Decision Programs /18/. In 1976 /14/ and in 1977 /15/ independently the BDDs were introduced for test generation purposes. Today the theory of BDDs is developing quickly /4,5,19/.

In /7,14/ structurally synthesized BDDs (SSBDD) as a special class of BDDs was introduced to represent the topology of gate-level circuits in terms of signal paths. Unlike "traditional" BDDs /4,18/, SSBDDs directly support test generation for gate-level structural faults without explicitly representing the faults. The advantage of SSBDDs is that the library of *D*-cubes for components is not needed for structural path activization. That's why SSBDD based test generation procedures do not depend on whether the circuit

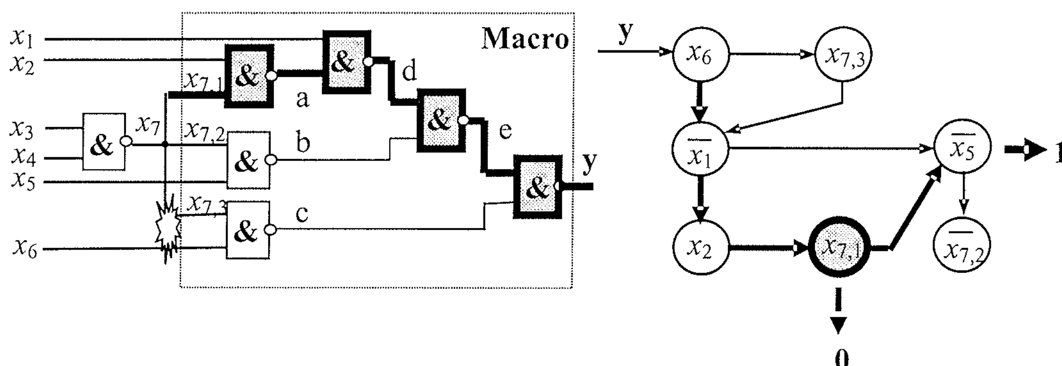

Figure 2: Combinational macro and his SSBDD

is represented on the gate level or on the higher macro-level whereas the macro means an arbitrary single-output subcircuit of the whole circuit. Moreover, the test generation procedures developed for SSBDDs can be easily generalized for higher level DDs to handle digital systems represented at higher levels /6,16,17/.

The BDD that represents a Boolean function is a directed noncyclic graph with a single root node, where all nonterminal nodes are labelled by Boolean variables (arguments of the function) and have always exactly two successor-nodes whereas the terminal nodes are labelled by constants 0 or 1. For all nonterminal nodes, a one-to-one correspondence exists between the values of the label variable of the node and the successors of the node. The correspondence is determined by the Boolean function to be represented by the graph.

Denote the variable which labels a node m in a BDD by $x(m)$. We say that a value of the node variable activates the node output edge. According to the value of $x(m)$, one of two output edges of m will be activated. If $x(m) = 1$ we say 1-edge is activated, or if $x(m) = 0$ we say 0-edge is activated. A path is activated if all the edges that form this path are activated. The BDD is activated to 0 (or 1) if there exists an activated path which includes both the root node and the terminal node labelled by the constant 0 (or 1).

Definition 3.1. A BDD G_y with nodes labelled by variables $x_1, x_2, ..., x_n$, represents a Boolean function $y = f(X) = f(x_1, x_2, ..., x_n)$, if for each pattern of X, the BDD will be activated to the value which is equal to y for the same pattern.

Important property of SSBDDs. SSBDDs differently from traditional BDDs have the following property: each node m in a G_y which describes a tree-like subnetwork N_y of the gate-level circuit N, represents a signal path $l(m)$ in N_y. There is an one-to-one correspondence between the nodes m in a G_y and the paths $l(m)$ in the corresponding circuit N_y.

An example of a combinational circuit with a tree-like macro and SSBDD for the macro is presented in Figure 2. For simplicity, the values of variables on edges of the SSBDD are omitted (by convention, the 1-edge is always directed to the right, and the 0-edge is always directed downwards). Also, terminal nodes with constants 0 and 1 are omitted (leaving the SSBDD to the right corresponds always to $y = 1$, and down - to $y = 0$). Each node is marked by an input variable of the macro. A node with the label x_m in the SSBDD represents the signal path through the macro which begins with the input variable x_m. The node variable is inverted when the path consists of odd number of inverters, and not inverted when the number of inverters is even. For example, the node $x_{7,1}$ of SSBDD represents the signal path with even number of inverters starting with the line $x_{7,1}$ through the nodes a,d,e to the output y in the macro (the bold lines in the circuit). The node [illegible] in the SSBDD has inverted variable since the corresponding path x_1,d,e,y consists of odd number of inverters. The fan-out node x_7 in the circuit has three branches, and each branch $x_{7,i}$ ($i = 1,2,3$) is the beginning of a path which is represented by the node $x_{7,i}$ in the SSBDD.

From the above described property of the SSBDD, automatic fault collapsing results. Assume a node m with label variable $x(m)$ represents a signal path $l(m)$ in a circuit. Suppose the path $l(m)$ goes through n gates. Then, instead of $2n$ faults of the path $l(m)$ in the circuit, only 2 faults related to the node variable $x(m)$ should be tested when using the SSBDD model.

Test generation with SSBDDs. Consider a combinational circuit as a network of gates, which is partitioned into interconnected tree-like subcircuits (macros). This is a new higher level (macro-level) representation of the same circuit. Each macro is represented by a SSBDD where each node corresponds to an input of the macro. In the tree-like subcircuits only the stuck-at faults at inputs should be tested. This corresponds to testing all the nodes in each SSBDD. Test generation for a node m in SSBDD, which represents a function $y = f(X)$ of a macro, is carried out by the following procedure /19,23/.

Algorithm 1.

1) A path l_m from the root node of SSBDD to the node m is activated.
2) Two paths $l_{m,e}$ consistent with l_m, where $e \in \{0,1\}$, from the neighbors m^e of m to the corresponding terminal nodes $m^{T,e}$ are activated.
3) For generating a test for a particular stuck-at-e fault $x(m) \equiv e$, $e \in \{0,1\}$, the opposite assignment for $x(m)$ is needed: $x(m) = \bar{e}$.
4) All the values assigned to node variables build the local test pattern $T(X,y)$ (input pattern of the macro) for testing the node m in G_y.

The paths in the SSBDD activated by *Algorithm 1* are illustrated in Figure 3.

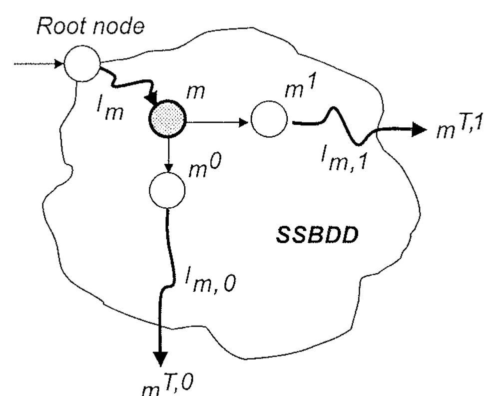

Figure 3: Test generation for the node m *with SSBDD*

To create the final test pattern in terms of primary inputs of the circuit (network of macros) for the given fault in an

embedded macro, fault propagation and line justification through the network of macros are needed. The fault propagation through a macro from the input x to its output y is carried out similarly to the test generation for the node m labelled by x in the corresponding SSBDD G_y as explained in *Algorithm 1*. Line justification for the task $y = e$ is carried out by activating a path in the graph G_y from the root node to the terminal node $m^{T,e}$.

Example 1. Consider test generation for the bridging defect between lines x_6 and x_7 of the circuit in Figure 2. This defect can be described by a functional fault model (dx_7, $\bar{x}_6 x_7 = 1$), which corresponds to the AND-type bridging model. To generate a test for the short we can generate a test for the stuck-at-1 fault ($x_{7,1} \equiv 1$) of the internal line $x_{7,1}$ (input of the macro) in the circuit at aditional conditions $x_6 = 0$, $x_7 = 1$. Using SSBDD we have to generate by *Algorithm 1* a test for the node $x_{7,1}$ in the SSBDD in Figure 2 at the preconditions $x_6 = 0$, $x_7 = 1$. Activating the path l_m through the nodes x_6, $\bar{x}_1$, and x_2 gives new additional assignments $x_1 = 1$, and $x_2 = 1$. Activating the path $l_{m,1}$ through the node $\bar{x}_5$ gives $x_5 = 0$. The path $l_{m,0}$ is activated "automatically", since the 0-edge from the node $x_{7,1}$ is connected directly to the terminal node $m^{T,0}$. The paths, activated by the generated test pattern $x_1x_2x_5x_6x_7 = 11001$, are shown by bold lines in Figure 2.

4. Using high-level DDs for diagnostic modelling

Test generation and fault simulation methods developed for SSBDDs have the advantage compared to other logic level methods that they can be easily generalized to handle the test generation and fault simulation problems at higher system levels /6,16,17/.

In general case (beyond the Boolean algebra and BDDs) a decision diagram can be defined as a non-cyclic directed graph $G = (M, \Gamma, X)$ with a set of nodes M, a set of variables X, and a relation Γ in M /6/. The nodes $m \in M$ are labelled by variables $x(m) \in X$ (constants or algebraic expressions of $x \in X$). For each value from a set of predefined values of a non-terminal node variable $x(m)$, there exists a corresponding output edge from the node m into a successor node $m' \in \Gamma(m)$. Consider a situation where all variables are fixed to some value. By these values, for each non-terminal node m a certain output edge is chosen, which is connected to a successor node. Let us call these connections between nodes - *activated edges*, and the chains of them - *activated paths*. For each combination of values of variables of X, there exists always a *full activated path* from the root node to a terminal node. This relation describes a mapping from a Cartesian product of the sets of values for variables in all nodes to the joint set of values for variables (or expressions) in terminal nodes. Therefore, by DDs it is possible to represent arbitrary digital functions $Y=F(X)$, where Y is the variable whose value will be calculated by the DD and X is the vector of all variables in nodes of the DD.

Depending on the class of the system (or its representation level), we may have DDs, where nodes have different interpretations and relationships to the system structure. In register transfer level (RTL) descriptions, we usually partition the system into control and data parts. State and output variables of the control part serve as addresses and control words, the variables in the data part serve as data words. High-level data word variables allow to describe RTL functions in data parts. When using DDs for describing complex digital systems, first we have to represent the system by a suitable set of interconnected components (combinational or sequential subcircuits). Then, we have to describe the components by their functions which can be represented as DDs.

As an example, in Figure 4 a RTL data-path and his compressed DD is presented /20/. The DD is created by superposition /6,21/ of elementary DDs for the components of the circuit. The word variables R_1, R_2 and R_3 represent

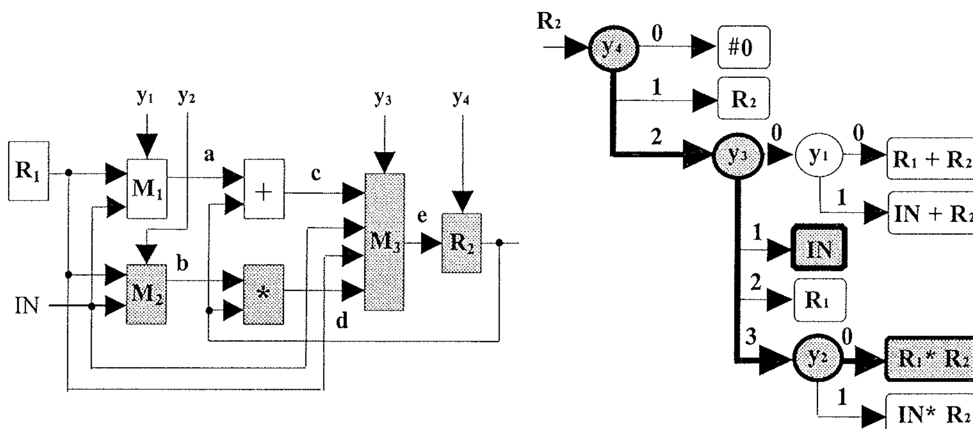

Figure 4: Register-transfer level data-path system

registers, IN representss the input bus, the integer variables y_1, y_2, y_3, and y_4 represent the control signals. M_1, M_2 and M_3 are multiplexers, and the functions $R_1 + R_2$ and $R_1 * R_2$ represent the adder and multiplier, correspondingly. The whole DD describes the behaviour of the input logic of the register R_2.

In test pattern simulation, a path is traced in the graph, guided by the values of input variables until a terminal node is reached, similarly as in the case of SSBDDs. In this example, the result of simulating the vector y_1, y_2, y_3, y_4, R_1, R_2, IN = 0,0,3,2,10,6,12 is $R_2 = R_1*R_2 = 60$ (bold arrows mark the path activated by the control pattern). Instead of simulating all the components in the circuit, on the DD only 3 control variables are visited during simulation, and only a single data manipulation $R_2 = R_1*R_2$ is carried out.

Each node in DD represents a subcircuit of the system. To test a node means to test the corresponding subcircuit. The paths to be activated during test generation in high-level DDs are illustrated in Figure 5.

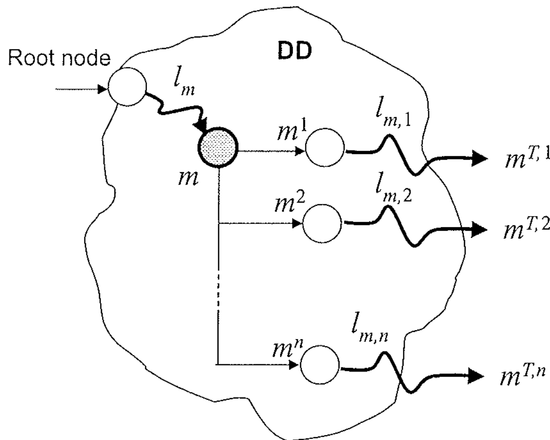

Figure 5: Test generation with high-level Decision Diagrams

We differentiate two testing types used for systems: *scanning test* (for testing terminal nodes in DDs, i.e. for testing the data path), and *conformity test* (for testing nonterminal nodes, i.e. for testing the control path).

Procedure 1. Scanning test. To generate a scanning test for a terminal node $m^{T,i}$ in the DD G_y, the path $l(m^{T,i})$ from the root node to $m^{T,i}$ is to be activated, and the test patterns for testing the function $z(m^{T,i})$ should be generated (according to the hierarchical approach, these patterns can be generated on the lower level representation of $z(m)$, and they can be regarded as a set of additional conditions W^F according to the functional fault model to map the faults from logic level to RT level).

Procedure 2. Conformity test. To generate a conformity test for a node m in G_y, the following paths are to be activated: 1) $l(m)$, and 2) for all the values of $i = 1,2,\ldots,n$: $l(m,i)$, and the proper data are to be found by solving the inequality $x(m^{T,1}) \neq x(m^{T,2}) \neq \ldots \neq x(m^{T,n})$ where $i = 1,2,\ldots,n$, and $x(m^{T,i})$ are the algebraic expressions of the terminal nodes.

To generate a scanning test for the node $R_1 * R_2$ of the DD in Figure 4, a path $l(R_1*R_2) = (y_4, y_3, y_2, R_1*R_2)$ is to be activated, and the data vetors (local test patterns) $DATA = (R_{1,1},R_{2,1};\ R_{1,2},R_{2,2};\ \ldots\ R_{1,m},R_{2,m})$ for testing the multiplier are to be generated at low level by any ATPG. The scanning test consists in cyclically run sequence: FOR all $(a,b) \in DATA$: /Load: $R_1 = a$; Load: $R_2 = b$; Apply: $y_2 = 0$, $y_3 = 3$, $y_4 = 2$; Read R_2/.

To generate a conformity test for the node $m = y_3$, the following paths are activated $l(m) = (y_4, y_3)$, $l(m,1) = (y_3, y_1, R_1+R_2)$, $l(m,2) = (y_3, IN)$, $l(m,3) = (y_3, R_1)$, $l(m,4) = (y_3, y_2, R_1*R_2)$ that produces a test control vector y_1, y_2, y_3, y_4 = 0,0,D,2. The test data vector $DATA = (R^*_1, R^*_2, IN^*)$ is found by solving the inequality $(R_1+R_2) \neq IN \neq R_1 \neq (R_1*R_2)$. The conformity test consists in cyclically run sequence: FOR all $D \in \{0,1,2,3\}$: /Load: $R_1 = R^*_1$; Load: $R_2 = R^*_2$; Apply: $y_1 = 0$, $y_2 = 0$, $y_3 = D$, $y_4 = 2$; $IN = IN^*$; Read R_2/.

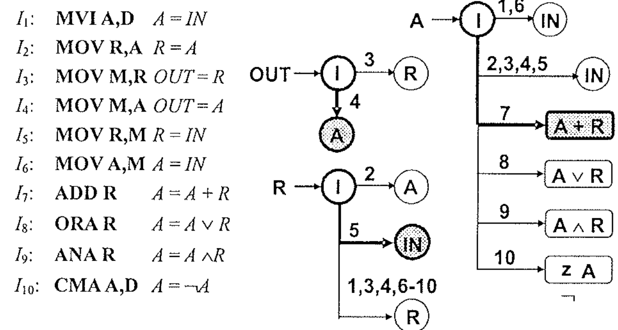

Figure 6: Decision Diagrams for a hypothetical microprocessor

An example of a hypothetical microprocessor is presented in Figure 5 given by a instruction set and three DDs G_A, G_R, G_{OUT}, for representing the behaviour, correspondingly, of accumulator A, register R and output logic. Since the model consists of several DDs representing a network of modules, the following tasks are solved for test generation: fault manifestation, fault propagation and line justification.

To generate a scanning test for the node $A+R$ in G_A, a path $l(A+R) = (I, A+R)$ in G_A is activated, which produces a test pattern $I = I_7$. The test data vector $DATA = (A_{1,1},R_{2,1};\ A_{1,2},R_{2,2};\ \ldots\ A_{1,m},R_{2,m})$ for testing the adder are generated by a low level ATPG. These operations correspond to the fault manifestation procedure, i.e. for solving a set of conditions $W^d = 1$ to map the low-level defects of the adder to the behavior level errors in the register A. For propagating the faults from A to OUT, a scanning test for the node A in G_{OUT} is generated. As the result, the path $l(A) = (I, A)$ in G_{OUT} is activated, which produces a test pattern $I = I_4$. For justification of the data variables A and R, the paths $l(IN)$ =

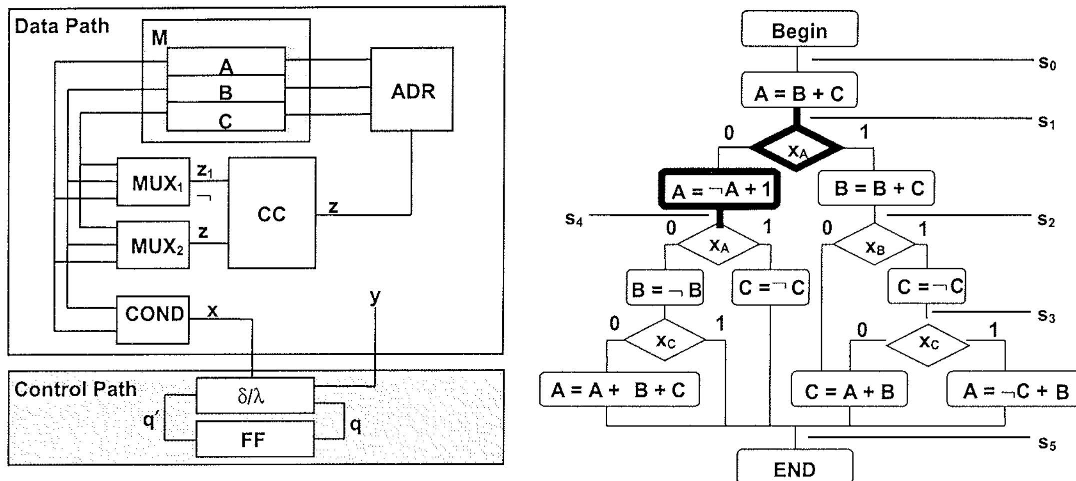

Figure 7: A digital system with a behavioral description

(I, IN), correspondingly, in G_A and G_R are to be activated which produce symbolic test vectors ($I = I_1$, $IN = a$) and ($I = I_5$, $IN = r$). The scanning test consists in cyclically run sequence: FOR all $(a,r) \in DATA$: /I_5: **MOV R,M** (Load $R = r$); I_1: **MVI A,D** (Load $A = a$); I_7: **ADD R** ($A = a + b$); I_4: **MOV M,A** (Read A)/.

Consider a digital system with a behavioral description in Figure 6. The system consists of control and data parts. The FSM of the control part of the system is given by the output function $y = \lambda\,(q', x)$ and the next-state function $q = \delta\,(q', x)$, where y is an integer output vector variable, which represents a microinstruction with four control fields $y = (y_M, y_z, y_{z,1}, y_{z,2})$, $x = (x_A, x_C)$ is a Boolean input vector variable, and q is the integer state variable. The value j of the state variable corresponds to the state s_j of the FSM. The apostrophe refers to the value from the previous clock cycle.

The data path consists of the memory block M with three registers A, B, C together with the addressing block ADR, represented by three DDs: $A = G_A\,(y_M, z)$, $B = G_B\,(y_M, z)$, $C = G_C\,(y_M, z)$; of the data manipulation block CC where $z = G_z\,(y_z, z_1, z_2)$; and of two multiplexers $z_1 = G_{z,1}\,(y_{z,1}, M)$ and $z_2 = G_{z,2}\,(y_{z,2}, M)$. The block COND performs the calculation of the condition function $x = G_x\,(A, C)$.

By superpositioning the DDs /21/ we can represent the system by only four DDs G_q, G_A, G_B, and G_C in Figure 7a.

Consider now the possibility of joining a set of DDs into a single DD. In Figure 7b the DDs G_A, G_B, G_C and G_q are joined into a single Vector Decision Diagram (VDD) $M = A.B.C.q = G_M\,(q', A, B, C, i)$ which produces a new concise model of the system. For calculating the values to different components of the vector variable M, we introduce a new type of node in VDD called *addressing node* labeled by an addressing variable i. The VDDs offer the capability to efficiently represent the array variables (corresponding to register blocks and memories) for calculating and updating their values. VDDs are particularly efficient for representing functional memories with complex input logic - with shared and dedicated parts for different memory locations. In general case, all the registers of the data path can be combined in the model as a single memory block.

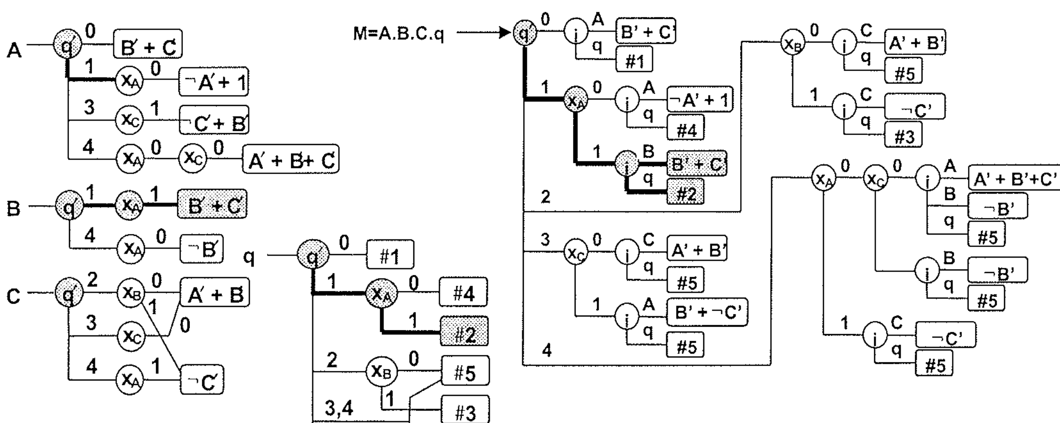

Figure 8. Representing the digital system in Figure 7 by high-level Decision Diagrams

Using VDDs allows significally to increase the speed of simulation. For example, in G_M in Figure 7b for the input vector $q' = 4$, $x_A = 0$, $x_C = 0$, the nodes q' and x_A, are traversed for calculating both new values of A and B only once, whereas in case of separate DDs in Figure 7a the nodes q' and x_A should be traversed for all the graphs: for calculating separately A, B, C, and q.

5. Experimental results

Table 3 presents the results of investigating the defect-oriented hierarchical test generation based on using of physical defect tables for library cells and logic macro level test generation. Experiments were carried out with a new defect-oriented Automated Test Pattern Generator (ATPG) DOT /22/ for detecting the AND-short defects in the 0.8μm CMOS technology. We used circuits resynthesized from the Verilog versions of the ISCAS85 suite as benchmarks for tests. The circuits were synthesised by SYNOPSYS Design Compiler. Column 2 in Table 3 shows the total number of defects in the defect tables summed over all the gates belonging to the netlist. Column 3 reflects the number of gate level redundant defects. These are defects that cannot be covered by any gate input (GI) vector of the gate. In column 4 circuit level redundant defects are counted. These are defects that cannot be tested as the circuit structure does not allow to generate a test for any of the GI vectors covering the defect. This redundancy is proved by the DOT tool. Column 8 shows the percentage of defects covered by DOT, while column 5 shows the ability of logic level SAF-oriented ATPG to cover the physical defects. The next coverage measure shows the SAF-oriented test efficiency. In this value, both, gate level redundancy of defects (column 6) and circuit level redundancy of defects (column 7) are taken into account.

The experiments prove that relying on 100 % SAF test coverage would not necessarily guarantee a good coverage of physical defects. In many situations the achieved coverage remained well below what can be achievable with the defect-oriented tool. For example, for circuit c2670 the defect coverage 98,29% obtained by SAF tests was more than 1.7 % lower than the result of the proposed tool. An interesting remark is, that up to nearly 25% of the defects were proved redundant by the DOT and can therefore not be detected by any voltage test. 75% defect coverage for c880 by 100% SAF-test gives not much confidence for this test. Only using DOT allows to prove that most of the undetected defects are redundant, and that the real test efficiency of this SAF-test is actually 99,66% giving finally a good confidence to the test.

Table 4: Comparison of ATPGs

Circuit	Faults	HITEC [1]		GATEST [3]		DECIDER [9,23]	
		F.C. %	Time s	F.C. %	Time s	F.C., %	Time, s
gcd	454	81.1	170	**91.0**	75	89.9	**14**
sosq	1938	77.3	728	79.9	739	**80.0**	**79**
mult	2036	65.9	1243	69.2	822	**74.1**	**50**
ellipf	5388	87.9	2090	94.7	6229	**95.0**	**1198**
risc	6434	52.8	49020	96.0	2459	**96,5**	**151**
diffeq	10008	96.2	13320	96.4	3000	**96.5**	**296**
average F.C.:		76.9		87.9		**88.6**	

The experiments of the hierarchical DD-based ATPG DECIDER /9,23/ developed at the Tallinn Technical University were run on a 366 MHz SUN UltraSPARC 60 server with 512 MB RAM under SOLARIS 2.8 operating system. At present, DECIDER contains gate-level EDIF interface which is capable of reading designs of CAD systems CADENCE, MENTOR GRAPHICS, VIEWLOGIC, SYNOPSYS, etc. In Table 4, comparison of test generation results of three ATPG tools are presented on six hierarchical benchmarks. The tools used for comparison include HITEC /1/, which is a logic-level deterministic ATPG and GATEST /3/ as a genetic-algorithm based tool.

Actual stuck-at-fault coverages of the test sequences generated by all the tools were measured by the same fault simulation software. The experimental results show the high speed of the ATPG DECIDER which is explained by the DD-based hierarchical approach used in test generation.

Table 3: Experiments of defect oriented test generation on logic level

Circuit	Number of defects			Defect coverage			
	All defects	Redundant defects		100% stuck-at fault ATPG			DOT
		Gates	System				
1	2	3	4	5	6	7	8
c432	1519	226	0	78,6	99,05	99,05	100,00
c880	3380	499	5	**75,0**	99,50	99,66	100,00
c2670	6090	703	61	79,1	98,29	**98,29**	100,00
c3540	7660	985	74	80,1	98,52	99,76	99,97
c5315	14794	1546	260	82,4	97,73	99,93	100,00
c6288	24433	4005	41	77,0	99,81	100,00	100,00

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6. Conclusions

Two main trends can be observed today in the field of digital test: defect-orientation to increase the quality of testing, and high-level modelling to reduce the complexity problems of diagnostic analysis. However, on the other hand, counting physical defects increases the complexity, and high-level modelling reduces the accuracy. Hierarchical approaches can solve this antagonism. Decision diagrams discussed in the paper contribute as a good tool for hierarchical modelling and diagnostic analysis of digital systems. The new innovative forms of DDs, structurally synthesized binary decision diagrams, high-level and vector decision diagrams have been discussed. From simulation point of view, they provide a compact and efficient representations of digital systems. High-level DDs is a new model, and there are a lot of possibilities for further research, for additional improvements and optimization.

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WEEE, RoHS, AND WHAT YOU MUST DO TO GET READY FOR LEAD-FREE ELECTRONICS

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Key words: Lead-free, implementation, manufacturing, reliability, compliance, WEEE, RoHS.

Abstract: The transition to lead-free electronics requires surmounting a host of technical, socio-political and economical issues. This paper discusses key concerns in lead-free product development, and provides guidelines to help equipment manufacturers efficiently implement a transition to lead-free electronics. The guidelines address key questions confronting the industry, including those related to lead-free compliance, lead-free part and supplier selection, lead-free manufacturing, and lead-free training and education.

WEEE, RoHS in kaj vse morate storiti, da se pripravite na elektroniko brez svinca

Kjučne besede: komponente brez svinca, tehnologija brez svinca, zanesljivost, WEEE, RoHS

Izvleček: Prehod na elektroniko brez svinca pomeni premagati kopico tehničnih, sociopolitičnih in ekonomskih ovir. V prispevku obravnavamo nekatere ključne zadeve pri razvoju izdelkov brez svinca ter predlagamo vodila, ki naj pomagajo proizvajalcem opreme pri prehodu na elektroniko brez svinca. Poudarek je predvsem na izobraževanju in šolanju za izdelavo elektronike brez svinca, proizvodnji brez svinca, izboru komponent brez svinca, izboru dobaviteljev in končno skladnosti z ustreznimi standardi.

Introduction

An expedient transition to lead-free electronics has become necessary for most electronics industry sectors, considering the European directives /1, 2/, other possible legislative requirements, and market forces /3, 4/. In fact, the consequences of not meeting the European July 2006 deadline for transition to lead-free electronics may translate into global market losses.

Considering that lead-based electronics have been in use for over 40 years, the adoption of lead-free technology represents a dramatic change. In less than ten years, the industry is being asked to adopt different electronic soldering materials, component termination metallurgies and printed circuit board finishes. This challenge is accompanied by the need to re-qualify component-board assembly and rework processes, as well as implement test, inspection and documentation procedures. In addition, lead-free technology is associated with increased materials, design and manufacturing costs[1]. The use of lead-free materials and processes has also prompted new reliability concerns /3/, as a result of different alloy metallurgies and higher assembly process temperatures relative to tin-lead soldering.

This paper discusses key concerns in lead-free product development, and provides guidance to efficiently implement a lead-free transition process that accounts for the company's market share, associated exemptions, technological feasibility, product reliability requirements, and cost. Lead-free compliance, part and supplier selection, manufacturing, and education and training are addressed.

The guidelines are presented in the form of answers to key questions, that are crucial to electronics manufacturers who are interested in migrating to lead-free products, to those companies that will purchase lead-free parts or sub-assemblies, and to those companies, which will support (maintain) traditional products.

1. What is the value for us to provide a lead-free product to our customer(s)?

Both legislative pressures resulting from the European Union (EU)'s proposed ban and the enacted Japanese take-back legislation, and marketing policies from electronics companies, are the driving forces behind lead-free solder adoption.

[1] *The cost of implementing the RoHS directive in the EU has been estimated to be US $ 20Bn /5/. Intel Corporation's efforts to remove lead from its chips have been estimated to cost the company over US$ 100 million so far /6/.*

An analysis of individual companies' strategies and consumer reaction within the electronics industry shows that to date, the main benefit of migrating to lead-free electronics has been increased market share through product differentiation, in terms of product environmental friendliness /4/. Consumers are thus holding corporations responsible for a quality of life that goes beyond the value of their product or service. As product, sub-assembly, component, and board manufacturers wish to be considered environmentally conscious, they are voluntarily migrating to lead-free technology prior to the implementation of legislation. However, once the European legislation becomes effective (July 1, 2006), migrating to lead-free electronics will become a requirement for equipment manufacturers who wish to maintain their market in that region.

As an increasing number of electronic suppliers transit to lead-free technology, the limited availability of lead-based items will become an additional driver to change to lead-free electronics, as manufacturers wish to ensure that their products remain reliable, repairable, and affordable. Considering that most of the electronics supply chain is migrating to lead-free technology, equipment manufacturers who are not prepared for this transition will be left behind technologically, and may ultimately incur substantial costs.

The difficulty for manufacturers to manage their design, manufacturing process, inventory, and logistics to a different set of regulations for each region and customer, may prompt them to extend lead-free product compliance to regions outside the EU. This strategy has been adopted by Hewlett Packard, who plans to extend lead-free compliance on a world-wide basis for non-exempted applications /7/.

A recent survey estimates that 68% of original equipment manufacturers (OEMs) are being requested to comply with the customer's corporate environmental policy /8/. Large OEMs and electronic manufacturing service (EMS) providers have responded more rapidly to the market's demand for lead-free products than mid- and small-sized ones /8/. Major OEMs who have successfully introduced lead-free products include Fujitsu, Hitachi, Matsushita, NEC, Philips, Sony and Toshiba in the consumer sector, which was the first industry to implement lead-free electronics; Dell, HP, IBM, NEC and Toshiba in the computer/server industry; and Ericsson, Infineon, and Motorola in the telecommunication sector.

A survey conducted on 53 component suppliers indicates that 44% of the component suppliers interviewed is already manufacturing compliant parts, and that 94% are designing RoHS-compliant parts /9/. It has been estimated that 69% of component manufacturers expect to be fully compliant by July 2006 /10/.

2. How do we certify lead-free compliance with the regulatory authorities?

An overview of current legislation pertaining to lead-free electronics is available in /4/. As the European Restriction of Use of Hazardous Substances (RoHS) directive /2/ is currently the only legislation that restricts the use of lead in electronic products, the guidelines provided in this section focus on compliance to this directive regarding the usage of lead[2]. However, manufacturers who plan to commercialize products in the EU after July 1, 2006, or in regions affected by other environmental regulations, will also need to ensure compliance with any other legislative or regulatory environmental constraints that may apply to their products[3].

As per the European Commission /11/, the concentration of lead in electrical and electronic products commercialized in Europe after July 1, 2006 should be less than 0.1% by weight in homogeneous materials[4]. The product categories and applications of lead currently exempted from the legislation are listed in the annex of the RoHS directive. The rationale behind the RoHS exemptions and their potential impact on the electronics industry are discussed in /4/. As of now, exemptions include: medical devices and monitoring and control instruments; oil and gas electronics if they are equipment for control and monitoring /12/; batteries used in electrical and electronic equipment, but these will be collected with the equipment once it becomes waste, on the basis of the WEEE directive; and

[2] *In addition to lead, the RoHS directive /2/ also prohibits the use of cadmium, mercury, hexavalent chromium, and two halide-containing flame retardants, namely polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), in non-exempted electronic products.*

[3] *Other environmental regulations applicable to electronic products are limited in scope to product take-back, reuse, and recycling. These regulations include The European Waste from Electrical and Electronic Equipment (WEEE) legislation /1/, the Japanese Household Electric Appliances Recycling Law /16/, and other laws enacted by China and certain states in the United States. China's Ministry of Information Industry's (MII) draft regulation, "Management Methods for the Prevention and Control of Pollution from Electronics Information Products," bans the use of lead, cadmium, mercury, hexavalent chromium, PBB and PBDE in electronic information products. This regulation is scheduled to take effect on July 1, 2006. Japan has had voluntary green initiatives in place for many years, and South Korea's electronic companies have adopted a voluntary program to comply with RoHS /17/.*

[4] *A homogeneous material is defined as a material that cannot be mechanically disjointed into different materials. The terms 'homogeneous' and 'mechanically disjointed' can be explained as "of uniform composition throughout" and "separated by mechanical actions such as unscrewing, cutting, crushing, grinding, and abrasive processes", respectively /11/.*

applications of lead listed in the annex of the RoHS directive /2/. As avionics and automotive electronics have not been specifically mentioned among the categories of electronics covered by the WEEE and RoHS legislations /2, 13/, they can be considered to be outside their scope. However, automotive electronics are covered by the scope of the End-of-life Vehicle (ELV) legislation /14/, which establishes a framework to ensure that vehicles are designed and manufactured in a way that optimizes opportunities for reuse, recycling and recovery. There are also bans for certain substances, but lead used in solders for automotive electronics is specifically exempt /15/.

In December 2004 and March 2005, the Technical Adaptation Committee (TAC) of the RoHS directive voted in favor of a draft Commission decision to add new exemptions, and modify existing ones. The additional applications of lead proposed were: lead in solders to complete a viable electrical connection between semiconductor die and carrier with IC flip chip packages (i.e., flip chip solder joint interconnections), lead used in compliant pin connector systems, lead as a coating material for the thermal conduction module c-ring, lead in solders consisting of more than two elements for the connection between the pins and the package of microprocessors with a lead content of more than 80% and less than 85% by weight, and lead in optical and filter glass /18, 19/. However, the European Parliament raised concerns regarding the legitimacy of the proposed exemptions, and requested the Commission to re-examine its draft decision /20/. Other exemptions /21/ have been requested by various industry stakeholders, which are to be reviewed by the TAC.

In the following sections, guidelines are provided to help establish a company's strategy to comply with the lead-free RoHS regulation, and verify product compliance to this regulation[5].

2.1 Company's Compliance Strategy

The company's strategy (i.e., legal policies) to comply with the RoHS regulation /2/ should be established both at corporate and division level, and documented in the form of a position statement that can be distributed to customers and suppliers. An example of a corporate RoHS compliance position statement is given in /7/.

A company's position regarding the RoHS directive should define what product(s) are to become compliant, the date which these product(s) are commercialized, and regions in which they are introduced if compliance is extended to regions outside the EU. The manufacturer should identify whether any of its products and their applications are exempt from the RoHS legislation. If necessary, clarification should be obtained from the regulatory body on how exemptions may apply to the company's specific products and applications. If the company is planning to use any of the RoHS exemptions, these should be specified in the company's position statement.

Exemptions are likely to remain the only option as long as substitution of a lead-based material by a lead-free one is not technically feasible from a process, reliability or cost viewpoint. For example, the use of high melting temperature (greater than 300°C) lead-based solder, such as Pb-3Sn, in flip chip BGA (FCBGA) applications prevents remelting of the bumps during lead-free reflow soldering. Alternative bumping metallurgies such as electroless nickel/gold and gold, or epoxy bumps, have poor self-alignment properties and higher cost. Other examples of almost unavoidable exemptions include lead in piezoelectric crystal devices (e.g., oscillators, filters) for microwave telecommunication applications, and lead in die attach solders for power applications. Regardless of exemptions, certain manufacturers in exempted industries (e.g., medical electronics, avionics, military electronics) that purchase commercial-off-the-shelf (COTS) electronic parts, which are the subject of the legislation, may be driven to use lead-free technologies, due to part availability and cost considerations /4/. The desire of component manufacturers and other elements of the supply chain is to operate a single line of products, rather than dual lead-free and lead-based production /22, 23/. Furthermore, the exemptions will be subjected to periodic review by the EU legislative bodies, with the intent to progressively eliminate them /23/.

2.2 Certification of Compliance

Once the legislation becomes effective, equipment manufacturers will have complete responsibility for compliance with the RoHS directive. Although no approach has been specified in the EU directives to report compliance with the legislation, at this time it is recommended that OEMs adopt the self-certification approach, for which the majority of the EU member states have indicated their preference /24/. Precedents for self-certification in the EU include the CE mark. Lead-free compliance self-certification should be supported by 'compliance' documentation from the suppliers, certifying that the procured materials, parts and subassemblies not exempted by the legislation meet the requirements of the RoHS directive, in terms of the maximum concentration of lead. Guidance to verify the compliance of procured items is provided in Section 2.2.1.

[5] *Legislative requirements pertaining to lead-free electronics should be regularly monitored for revisions. New and revised standards applicable to lead-free assembly process, qualification test, and inspection should also be identified (Section 17). A map of which products (and their quantity) are being sold into which regions should be established. The regulatory body, regulation/standard and its effective date, that the products must comply with, as well as corresponding regulatory requirements (e.g., banned materials, associated threshold limits including the level at which it should be measured, recycling requirements, and reporting methods) should be identified.*

A market surveillance will be conducted by national enforcement authorities to verify producers' compliance with EU regulations. Upon request of the enforcement authority, producers will be required to demonstrate compliance by providing satisfactory evidence. Inspections will be conducted, involving product chemical composition analysis (see Section 2.2.2).

At this time, the WEEE legislation itself only states that penalties applicable to breaches of the national provisions of the directives should be "effective, proportionate and dissuasive" /1/, but EU member states will determine the actual penalties. Regardless, non-compliance could lead to a decrease in market share and reputation.

2.2.1 Verification of compliance for procured materials, parts, and sub-assemblies

To ensure that the final product is lead-free, assurance should be obtained from all related material, part and sub-assemblies suppliers that their products do not contain lead with a concentration above the RoHS restricted level (0.1% by weight). Manufacturers will be required to maintain a record of their suppliers' compliance documentation, that can be shown to the enforcement authorities in the course of an inspection. The declaration obtained from the supplier will constitute a legal documentation.

No format or time frame for producing such compliance documentation has been specified. At this time, it is recommended that OEMs issue a formal letter to suppliers and assemblers, requesting self-certification on the basis of chemical composition analysis of the supplied material and/or parts. It should be noted that the transmitting material safety data sheet is not sufficient, because elements with content levels below 1% by weight are not shown. Examples of lead-free/RoHS compliance statements from electronic part manufacturers include /25-30/.

The self-certification request issued to the supplier should be supplied along with the company's RoHS position statement, and a list of requirements and restrictions for the procured material, part, or sub-assemblies, including the threshold concentration value of lead. The lead-free certification request may be included as part of a material declaration questionnaire (also referred to as green procurement survey or supply chain questionnaire) that manufacturers may already issue to their suppliers, to verify lead-based product compliance to other regulatory requirements /31/. An example of environmental requirements set by an equipment manufacturer for its procured materials, parts and sub-assemblies is provided in /32/. Suppliers may use different units for defining the concentration of hazardous substances (e.g., part per million, percentage by weight, percentage by mass). Caution should be taken when examining lead content data, because the lead concentration threshold set by the RoHS legislation is expressed by weight. The verification documentation obtained from suppliers and assemblers should be re-obtained or re-signed whenever there is a change in materials used in supplied parts or end products, process, or regulatory requirements.

For all procured lead-free items, a lead-free compliance notation/record should be included in the material management system or database that the company may already employ to convey material chemical data for lead-based products. This will permit the lead-free compliance of the procured items to be verifiable throughout the enterprise (e.g., design, production and logistic departments) and supply chain.

If no appropriate compliance documentation is available from the supplier, equipment manufacturers should consider an alternative supplier with lead-free capability, or conduct a chemical analysis of the procured part. Chemical analysis methods and providers of lead-free compliance assessment services are listed in Sections 2.2.2 and 3, respectively.

2.2.2 Chemical analysis

Conducting a chemical analysis of the procured materials, parts and sub-assemblies may be necessary to ensure compliance with legislative requirements, when the legal compliance documentation is not available from the supplier(s). Lead can be found in many electronic packaging materials, namely: solders, component terminal finishes (i.e., lead finish for leaded packages or solder ball for area array packages and flip chip interconnections), separable connector terminations, PCB pad surface finishes, solder-based die attach materials, as an alloying element in aluminum-based die-casting materials, polyvinyl chloride (PVC), PVC wiring, balance weights for large Titan motors, paints, plastic additives, tinned cables, resin stabilizers and additives, optical materials, and ferroelectrics.

Two standards have been published on assessing the lead content of electronic products. EIA/ECCB-952 /33/ describes the required elements of a plan to assess the lead content of a product, in terms of high-level requirements and areas of concern that must be addressed by the process. /34/ defines test procedures to assess the lead content of polymeric and metallic materials, and electronic parts and assemblies[6].

[6] *Analysis procedures include the use of Energy Dispersive X-Ray Fluorescence (EDXRF) or Wavelength Dispersive X-Ray Fluorescence (WDXRF) for material/part qualitative and quantitative screening. The use of inductively coupled plasma-atomic emission spectroscopy (ICP-AES), inductively coupled plasma-mass spectrometry (ICP-MS), or atomic absorption spectroscopy (AAS) may be used to confirm the lead content /34/. These experimental methods are discussed in /35/, along with Energy Dispersive X-Ray analysis, Spark Emission and DC Arc Emission Spectroscopy, Glow Discharge Optical Emission Microscopy, and Polarography.*

Considering the level of expertise required for compositional analysis of electronic assemblies (e.g., in terms of potential limitations of the experimental method and equipment, instrument calibration), manufacturers should consider subcontracting such analysis to specialized providers (see Section 3).

Databases such as offered by i2 /36/ and Underwriters Laboratories /37/, which contain information of the chemical content of certain electronic materials and components, may help identify non-compliant electronic parts, lead-free alternatives and their suppliers. i2's database provides material composition data at component level, including RoHS-restricted substances. UL's database covers plastic materials and is expected to expand in the near future to include information on restricted substances. However, parts and materials change, and it is critical that guarantees for accuracy and compliance be obtained.

3. Which companies can test electronic materials, parts and sub-assemblies for lead-free compliance?

Material, part, sub-assembly and product compliance analysis can be subcontracted to third parties such as material analysis companies with lead-free compliance assessment capabilities. The cost of chemical analysis services typically varies from US 500 dollars for standard elemental composition analysis by energy dispersive x-ray spectroscopy (EDS) or XRF spectroscopy, up to a few thousand US dollars for highly sensitive analysis techniques such as mass spectrometry. Although no particular provider of chemical analysis services is advocated, examples include /38-42/.

4. How should we get started with the design of lead-free products?

All materials and parts in final product, which may contain RoHS restricted substances in the Bill of Materials (BoM), should be identified. The BoM may represent a single product or assembly, or a family of products. As outlined in Section 2.2.2, identification of such materials and parts may require material analysis. Any impacted parts and products should be documented in a database.

Non RoHS-compliant materials and parts should be replaced with RoHS compliant alternatives that are selected based on availability, manufacturability, reliability and cost considerations. Manufacturability considerations include compatibility between lead-free materials used as component terminations, PCB pad finishes and solders; material and part compatibility with the lead-free manufacturing processes (reflow, wave, rework), and component terminal and PCB pad solderability. Potential reliability concerns specific to lead-free materials and processes include component moisture and thermal sensitivity, excessive intermetallic growth, tin whiskering, electro-chemical migration, solder joint manufacturing defects (e.g., poor wetting, fillet lifting, voiding, cold joint), and material/process incompatibilities in assemblies combining lead-free and lead-based metallurgies.

When outsourcing manufacturing, the part selection process should be co-ordinated with the assembly house to ensure compatibility of the procured parts with the manufacturing processes. Examples of EMS providers with lead-free capability include /43-46/.

5. How do we assess our suppliers' ability to offer lead-free parts and assemblies?

The capability of part, design and manufacturing service providers should be assessed based on the same criteria as those employed for providers of lead-based products. In addition, evidence of the provider lead-free capability should be obtained, particularly when considering less established providers. Such evidence should include lead-free/RoHS compliance certification for the procured parts (Section 2.2), and proof of a qualified lead-free manufacturing process for EMS providers. Lead-free part suppliers and EMS providers can be evaluated based on the following criteria.

Inspections of in-coming materials and parts should be performed, to ensure conformance of the procured items to quality and reliability requirements applicable to lead-free technology and/or lead-based products. Requirements for lead-free components and boards are outlined in Sections 6 and 7, respectively.

Component moisture and/or thermal sensitivity (see Section 6.2) should be addressed using standardized or recognized storage, packing, handling and transportation procedures and using qualified lead-free reflow, rework/repair processes.

Assembled boards should meet standardized quality and reliability criteria (e.g., requirements defined by and tested in accordance with global standards such as IPC, IEC, and JEDEC, or regional standards, such as JPCA and JEITA in Japan). The board assembler should demonstrate willingness to co-operate with the equipment manufacturer, as well as component, board and solder suppliers, to successfully design and produce reliable lead-free products.

Appropriate lead-free product designations (e.g., part number change, date code differentiation, marking) should be employed to trace lead-free materials, parts and assemblies throughout the supply chain. Product change notices (PCNs) and alerts should be provided by the supplier, to notify equipment manufacturers of the replacement of lead-based items by lead-free ones (see Section 16).

The offering, availability and scheduling of assembled lead-free parts and systems, including lead-times for a given production volume, should be compatible with the equipment manufacturer's plans for lead-free products. Any possible change in cost due to a material change should be monitored.

The manufacturing house personnel, including operators, technicians, process engineers, and managers should receive appropriate and up-to-date lead-free education and training, and have access to suitable information resources (see Section 18).

6. Is there anything unique that we need to do when selecting lead-free components?

The main considerations for lead-free component selection (including IC, passive and optoelectronic components, and connectors) include terminal finish, moisture and thermal sensitivity, material and process compatibility, and part tracing.

6.1 Part terminal finish

At present, pure tin (matte finish) is the most widely adopted finish material for leadframe components, followed by nickel-palladium-gold leadframe pre-plating /3/. Other lead-free leadframe finishes include tin-bismuth, tin-copper, and tin-silver.

For array components, tin-silver-copper solder ball metallurgy has been widely adopted.

For connectors, tin-copper (Sn97.3-Cu0.7) and tin-silver-copper (e.g., Sn-Ag3~4-Cu0.5~0.7) finishes can be employed as replacements of tin-lead solder contact finishes. These lead-free alloys exhibit better hardness and resistance to fretting corrosion than tin-lead /47, 48/. For cost-driven applications, pure matte tin may be used.

Tin whiskers are hair-shaped crystals that can grow spontaneously on the plating surface, and could cause electrical short circuits across part terminals, such as connectors. The whisker tolerance level of the specific product and application considered should be identified. For long-duration or high-reliability applications (e.g., medical, avionics, space, and defense applications), the risk tolerance may be sufficiently low as to warrant consideration of mitigation strategies /3/. Standard JESD22A-121 /49/, released this year, specifies test methods to assess the propensity for whisker's growth on tin and tin alloy surface finishes. iNEMI has submitted tin whisker acceptance test requirements /50/ for review to JEDEC and IPC. iNEMI has also proposed mitigations approaches that include the use of thick tin coating (with thickness greater than 8 ěm) or nickel under-plating (with thickness greater than 1.27 ěm) over copper base metal, and recommends avoiding the use of pure bright tin plating without a mitigation strategy /51/. The effectiveness of various mitigation strategies is discussed in /3, 52/. Examples of non-standard vendor tin whisker qualification tests are given in /53, 54/.

Nickel-palladium or nickel-palladium-gold leadframe component finishes are not prone to whisker growth /51/. However, there are also potential disadvantages associated with the use of these finishes /3/, including cost, solderability, and susceptibility to creep corrosion /55, 56/.

An example of procurement guidelines set by an equipment manufacturer for lead-free components is given in /57/. In this example, the equipment manufacturer specifies its preferred termination finishes, and a number of requirements for tin-based finishes, including plating process control, plating characteristics known or suspected to influence whisker growth, and tin whisker qualification tests.

6.2 Component moisture and thermal sensitivity

Components may be more prone to mechanical damage (e.g. delamination, cracking, popcorning) when exposed to lead-free reflow soldering temperature profiles compared with standard tin-lead reflow.

Organic IC packages. The moisture sensitivity of organic IC packages is characterized in terms of component floor life when stored in a PCB assembly environment, outside moisture-proof packaging. For lead-free assembly, package moisture sensitivity, as defined per IPC/JEDEC J-STD-020C /58/ classification, should not exceed moisture sensitivity level (MSL) 3. The IPC/JEDEC MSL rating of a plastic component has been found to decrease by up to one or two ratings for every 10°C increase in peak reflow temperature /3/. For example, an MSL 1-rated component at a tin-lead assembly temperature of 220°C would become MSL 2 or MSL 3 at a lead-free assembly temperature of 240°C. Qualification tests performed by component suppliers should include moisture sensitivity level tests. Equipment manufacturers also need to ensure that the time out of moisture-proof packaging is appropriately monitored throughout the supply chain, by component manufacturers, distributors and contract manufacturers. Baking moisture sensitive components (125°C, 24 hours) before lead-free reflow soldering may be a good precaution.

Component temperature rating requirements for lead-free assembly and rework depend upon package volume and thickness, and are specified in standards IPC/JEDEC J-STD-020C /58/ and JEITA ED-4701-301A /59/. Large, thin organic packages (e.g., BGAs, TQFPs, CSPs) are generally more prone to hygrothermal stress-induced failures. Small volume, thin SMD packages (i.e., with small thermal mass) reach higher body temperatures during reflow soldering to boards that have been profiled for larger packages. Therefore, it should be verified that such components are rated at the appropriate temperature specified by the standard. Equipment manufacturers need to ensure that component vendors following JEDEC J-STD-

020 use the latest version of the standard, in which temperature rating requirements have been revised compared with J-STD-020B. Other standards relating to the handling and assembly of moisture and/or thermally sensitive components include IPC/JEDEC J-STD-033C /60/ and Mil-Std 202G Method 210F /61/.

Passive components. For passive components such as chip capacitors and resistors, it should be verified that the component temperature rating is sufficient for lead-free soldering. In addition, the allowable PCB flexure specified by the component supplier may need to be considered, as passive ceramic components may be more susceptible to mechanical damage (e.g., cracking) due to higher soldering temperature than for tin-lead soldering, and possibly due to different solder joint metallurgies. Large chip components (1210 in size and above) tend to be more exposed to flexure-induced damage than smaller components.

Optoelectronic components. Optoelectronic components, such as light emitting diodes (LEDs), are very temperature-sensitive and could suffer optical property degradation or mechanical damage when exposed to lead-free reflow soldering profiles. Temperature-sensitive devices may require a separate assembly process that is performed after standard reflow of other components. Thermally-sensitive devices may be assembled using either press-fit, hot bar soldering, laser soldering, hand soldering and/or a conductive adhesive attachment method. Wave soldering may be suitable for devices having intrusive leads. Assembly should be performed based on the component manufacturer assembly guidelines.

Connectors. The majority of connector housings are made of plastic materials, and can be prone to hygrothermal stress-induced defects such as popcorning, similarly to IC plastic packages. It should be verified with the manufacturer that the connector is rated to a sufficiently high temperature for lead-free assembly.

6.3 Material and process compatibilities

Due to part availability and cost considerations, equipment manufacturers may be constrained or tempted to combine lead-free and lead-containing materials and parts in PCB assemblies. The use of lead-free and lead-based material combinations could potentially affect solder joint reliability, and examples of such situations are given below, both for forward and backward assembly incompatibility. Forward compatibility refers to a component with lead-based terminations soldered using lead-free solder and a lead-free temperature profile. Forward incompatibility issues can arise due to unavailability of a lead-free component in the transition period. Backward compatibility refers to a component with lead-free terminations soldered with tin-lead solder and a tin-lead temperature profile. Exempted products may be exposed to backward incompatibility issues when lead-based components become unavailable. When possible, the following situations should be avoided.

6.3.1 Forward incompatibility

Lead in lead-based component termination (leadframe or solder ball) can interact with bismuth-containing lead-free solder (e.g., Sn-Bi, Sn-Ag-Bi, Sn-Zn-Bi, Sn-Ag-Cu-Bi) during assembly, to form a low-melting point phase (Sn-51Bi-32Pb, melting point = 96°C) which can cause cracking in solder joints /62/.

Lead-containing component termination with lead-free Sn-Ag-Cu or Sn-Ag solder can result in poor solder joint mechanical reliability, due to the formation of a Sn-Pb-Ag eutectic (62Sn-36Pb-2Ag, melting point = 179°C) during the cooling phase of the assembly process. This phase has different microstructural characteristics compared with the bulk of the solder joint, and can cause solder joint fillet lifting in through-hole joints /63/.

6.3.2 Backward incompatibility

BGA packages with Sn-Ag-Cu solder balls assembled to a PCB using a conventional tin-lead soldering temperature profile may result in the formation of "cold joints". A hybrid soldering process, which uses higher reflow temperatures compared with standard tin-lead reflow, may be required to melt the balls.

Tin-lead hot air solder leveling (HASL) PCB pad finish can cause solder joint fillet lifting in through-hole lead-free nickel-palladium-gold coated components soldered with lead-free Sn-Ag solder /3/. This is due to the formation of 62Sn-36Pb-2Ag eutectic during the cooling phase of the assembly process.

Tin-lead HASL PCB pad finish with lead-free Sn-Ag-Cu solder can result in weak joints with voiding. This has been attributed to depletion of tin from the pad coating, which results in the formation of a weak lead-rich phase /64/.

6.4 Solderability and reliability

Conformance to standardized solderability criteria (per IPC/EIA-J-STD-002B /65/) and reliability criteria, already applicable to lead-based components, should be ensured. However, caution should be exercised, as the wettability of most lead-free solders is not as good as that of eutectic tin-lead solder, causing potential quality and reliability issues. The shelf life of the lead-free component finish, which impacts on solderability, should be obtained from the supplier.

There are two known trends with regard to the thermo-mechanical reliability of lead-free solder joint interconnections in temperature cycling conditions. Lead-free solder joint thermo-mechanical fatigue durability is expected to be equivalent or better relative to tin-lead eutectic joints (considering the same package and board) at small levels of mechanical loading (i.e., small thermal expansion mismatch between the component and board, which generally applies to plastic packages, and moderate thermal cycling). Conversely, lead-free solder joint thermo-mechanical fatigue durability may be lower relative to tin-lead eu-

tectic joints (considering the same package and board) at high levels of mechanical loading (i.e., high thermal expansion mismatch between the component and board, which generally applies to ceramic leadless and ceramic ball grid array packages, and severe thermal cycling).

The use of reliability qualification tests should be considered to assess joint thermo-mechanical reliability for the specific product and application environment. Further information on lead-free electronics reliability can be found in /3/.

7. Is there anything unique that we need to do when designing or selecting lead-free circuit boards or circuit assemblies?

Considerations for lead-free board design include PCB pad finish and laminate material selection.

7.1 PCB pad finish

The primary lead-free alternatives to tin-lead HASL are immersion silver, immersion tin, electroless nickel/immersion gold (ENIG), and organic solderability preservative (OSP). Unlike for lead-free component termination finishes, there is a history of use for lead-free board finishes. PCB finish selection is based upon the finish wetting characteristics with lead-free solders, shelf life, pad planarity, and cost. Reported concerns associated with each finish are summarized below.

Immersion tin used in PCBs subjected to multiple reflow temperature profiles can be prone to Sn-Cu intermetallic formation, resulting in a degradation of pad solderability. Immersion silver is known to generally better survive multiple reflows than immersion tin due to the lower growth rate of Sn-Ag intermetallics compared with Sn-Cu intermetallics, but silver migration may pose a reliability risk for certain applications.

Due to the thinness of OSP and immersion silver finishes, these coatings may be more prone to mechanical damage (e.g., surface scratches) during board handling operations, that could expose the underlying metal and thus impact pad solderability.

ENIG is considered a multifunctional (applicable to soldering, aluminum wire bonding, press fit connections and contact surface), corrosion resistant surface finish, but can be prone to "black pad" defects /66/. Black pads are characterized by separation of the solder joint from the surface of the electroless nickel underplate. This is commonly attributed to excessive phosphorous contamination of the electroless nickel.

The shelf life of all finishes impacts solderability, and should therefore be obtained from the supplier. Immersion tin and immersion silver are more cost-effective relative to ENIG.

7.2 PCB laminate material

PCB laminate material selection should follow the same criteria as for lead-based products, with some exceptions. It should be ensured that the laminate can withstand multiple reflows and rework at the appropriate lead-free processing temperature without thermo-mechanical damage. Although FR-4 laminates with glass transition temperatures of approximately 140°C may be suitable, applications exposed to high temperature environments (e.g., under-the-hood, oil well applications) may require materials with higher glass transition temperature, such as high-glass transition temperature FR-4 (e.g., 170°C). Potential concerns associated with assembly at lead-free soldering temperature profiles include increased board warpage, which could cause planarity problems with large components /67/, increased through-plane thermal expansion, which could affect plated-through hole (PTH) reliability, or possibly delamination of the metallization /68, 69/. According to /68/, one-third of the U.S. industry has switched to higher glass transition temperature materials (e.g., 170°C) for a greater margin in rework.

The laminate material should not contain polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE). These halide-containing flame retardants are prohibited by the RoHS legislation. Furthermore, the laminate moisture absorption properties should be verified with the supplier, as well as any specific storage conditions/ duration or pre-baking that may be required before assembly.

7.3 PCB layout

In general PCB design rules for lead-free soldering are same as tin-lead soldering. However, because of inferior lead-free solder wettability and less superheat (temperature above the liquidus) during reflow, there will be differences in optimized layout between lead-free and lead-based designs. The following guidelines for PCB layout for lead-free soldered product may be considered.

It is a good practice to design the PCB to achieve even spread of high and low thermal mass components (to minimize temperature gradients and peak temperature).

PCB design may also need to accommodate hand soldering of some thermally sensitive components (due to higher reflow temperature associated with lead-free soldering).

In some designs, insufficient component spacing can result in secondary reflow of adjacent leadframe components during lead-free rework operations of BGA/CSP components, particularly in high-density component-board assemblies. Typically, the minimum component spacing between BGA/CSP and leadframe components should be 150 mils /3/.

In some applications, pad width may have to be reduced to minimize the exposed pad (without solder coverage) due to the reduced spreading (wetting) of lead-free solder.

The product designer should consult with PCB manufacturer and assembler to minimize manufacturing concerns

8. Is there anything unique that we need to do when selecting lead-free solder alloys?

The International Tin Research Institute (ITRI), International National Electronics Manufacturing Initiative (iNEMI), European Consortium BRITE-EURAM and Japan Electronics and Information Technology Industries Association (JEITA) recommend Sn-Ag-Cu eutectics as the most promising lead-free solder metallurgies[7], endorsing Sn-4.0Ag-0.5Cu, which is the most widely-characterized alloy /3/, as well as Sn-3.0Ag-0.5Cu (JEITA's recommendation), Sn-3.9Ag-0.6Cu (iNEMI's recommendation), and Sn-3.8Ag-0.7Cu (BRITE-EURAM's and Soldertec's recommendations) /70/.

Both for reflow and wave soldering, Sn-3Ag-0.5Cu (liquidus temperature, 217-220°C) currently appears to be the leading candidate adopted by the industry, due to cost considerations. 99.3Sn-0.7Cu (liquidus temperature, 227°C) is a low cost alternative for wave soldering, recommended by iNEMI /71/.

Equipment manufacturers should verify the licensing agreements of the lead-free solder supplier, and verify that the solder supplier is aware of any potential patent issues in the country of manufacture as well as country of sale or customer re-sale. Typically, royalty cost account for 2 to 8 % of the solder paste cost. If the procured lead-free solder is not properly licensed, the alloy composition should be obtained, and an explanation of why the solder supplier believes no license is necessary should be sought. In addition, the equipment manufacturer should verify whether their company has a worldwide intellectual property (IP) non-infringement warranty and indemnity in place with the solder supplier or assembly house, as appropriate. Such warranty should be application-specific, and may help the equipment manufacturer to recover damages in the event of patent infringement issues. However, an indemnity is not an alternative to due diligence. Firstly, an indemnity would not protect the equipment manufacturer from being sued. Secondly, the equipment manufacturer would never be fully compensated for the damage caused to customer relationships by missed shipments. Furthermore, small sub-contractors or solder suppliers may not have the financial strength to honor the indemnity.

9. Is there anything unique that we need to do when selecting fluxes?

The industry is migrating to no-clean flux systems for both cost and environmental reasons. Because tin-silver-copper pastes have lower wettability than tin-lead ones on copper, no-clean flux systems using slightly more aggressive wetting agents than conventional commercial fluxes (employed with lead-based solders) may be required. Such fluxes tend to leave a higher amount of residues on the board after reflow, compared with conventional fluxes. This may cause reduced surface insulation resistance and increase the risk of electrochemical migration. In addition, the flux residues are harder than those formed with tin-lead soldering due to higher reflow temperatures, which can cause probing difficulties due to increased electrical contact resistance.

Although water-soluble flux systems eliminate potential surface insulation resistance and electrochemical migration issues, little progress has been made to develop such formulations due to lack of industry demand. On the other hand, solder paste manufacturers are actively working on the development of improved no-clean solder pastes.

Japanese end-users have successfully implemented lead-free wave soldering with Sn0.7Cu, Sn3.5Ag, and Sn-Ag-Cu alloys using rosin-based no-clean fluxes. In North America and Europe, the preference is to use volatile organic compound (VOC) no-clean fluxes.

10. How do we modify the approved vendor and part lists for the lead-free supply chain?

Once the lead-free part and corresponding vendor are approved, this information should be updated in the company's material and vendor database or management system, in the same manner as for lead-based products.

A monitoring scheme of supplier PCNs and supplier alerts of the replacement of lead-based parts by lead-free ones should be established. The PCN-alert database service, and Government-Industry Data Exchange Program (GIDEP) are examples of alert databases.

11. How do we mitigate supply interruptions related to the bill of materials?

It is expected that lead-based products may become unavailable as electronic suppliers transit to lead-free technology. Consequently, manufacturers of exempted applications (e.g., medical electronics) that develop non-RoHS compliant products may be exposed to the discontinuation of parts, making design, production and maintenance risky. The potential issues associated with assembling lead-free parts to a PCB using tin-lead solder and processes were summarized in Section 6.3.

[7] *An overview of lead-free soldering alloys and their characteristics (including constitutive properties, durability, and cost), suppliers and users is provided in /3/, with corresponding solder joint characteristics (including metallurgical reactions, mechanical properties, electromigration- and current carrying capability).*

Manufacturers relying on lead-based technologies must monitor PCNs, and identify whether their suppliers have any plans to discontinue the production of lead-based products. If this is the case, the time line for the discontinuation should be obtained.

Life time buy practices are a possible solution to resolve supply interruptions. However, potential disadvantages of such practices include significant on-time expenditure, increased inventory on the balance sheet, the requirement for proper storage space (with appropriate temperature, humidity, and handling conditions), and the potential for future unplanned requirements (e.g., significant changes in product technology or upgrades).

12. What are the storage and handling requirements for lead-free parts and sub-assemblies?

The shelf life and specific storage and handling requirements of the procured items should be obtained from the suppliers. Finish shelf life (e.g., PCB pad-, component- and connector termination finishes) will impact solderability.

The moisture and thermal sensitivity of leaded and lead-free components and board laminates is different. Handling, packing, and shipping requirements for moisture/ reflow sensitive surface mount devices are specified by JEDEC standard J-STD-033C /60/.

If thin immersion silver or OSP pad finishes are used, care must be taken to avoid surface defects or scratches.

Lead-free solder paste should be stored in a container with appropriate labeling and identification to distinguish it from tin-lead solder paste. The solder paste should be stored in the refrigerator between 35 and 45°F and should be used on a first-in/first-out (FIFO) inventory control basis. The shelf life of tin-silver-copper solder pastes at the recommended storage temperature (35 to 45°F) may be reduced from the typical six months expected for tin-lead solder paste, to three to four months. The materials used in fluxes developed for use with tin-lead solder paste may attack the higher tin-containing lead-free solder powder (>95% tin by weight) more than standard tin-lead solder powder (63% tin by weight), hence reduce the shelf life of the lead-free paste. Solder paste manufacturers are in the process of developing flux chemistry formulations to improve the shelf life of lead-free pastes. The solder paste should be maintained at room temperature for four hours before opening the container /3/.

In addition, the storage and handling scheme of electronic parts should prevent the mixing of lead-free and lead-based items. This can be achieved through appropriate part identification, as detailed in Section 16.

13. How should we perform lead-free component-board assembly?

The following guidelines for surface mount and through-hole assembly are adapted from /3/.

13.1 Reflow Soldering

Surface-mount assembly consists of three steps: screen printing, pick and place, and reflow. Only qualified lead-free materials should be available on the production floor. In addition, it should be ensured that the materials selected for assembly are free of other impurities that may impact on manufacturability and/or reliability.

Stencil printing. Studies conducted by many companies have shown that the same type of stencil printer can be used for lead-free solder paste as for tin-lead solder. The stencil design guidelines are identical to those for tin-lead systems. As noted in Section 7.3, there is currently no change in PCB pad design guidelines for soldering lead-free components. The print volume (transfer rate) of lead-free paste has been found comparable to that of lead-tin paste /3/. The same printing settings can be applied to lead-free solder pastes as for tin-lead. Settings include printing speed, squeegee pressure, on or off contact, separation speed, separation distance, and cleaning frequency. For the screen-printing process, high squeegee pressure and low printing speed have been found to yield better printing results for tin-silver-copper paste /3/. The stencil release rate has a minimal effect on the printability of lead-free solder pastes. Typical settings tested for lead-free pastes are: squeegee blade pressure (16-inch blade length) = 18 kg, printing speed = 10-20 mm/s, snap-off rate = 1mm/s /3/.

Pick and place. No change is required to pick-and-place machines to accommodate lead-free components.

Reflow oven equipment. Most eight-to ten-zone convection reflow ovens are capable of lead-free soldering. Ten-zone ovens enable a more precise control of spatial temperature variations across large boards. Currently-available ten-zone convection ovens have a 325 to 350°C temperature rating. Typical oven settings would normally not exceed 300°C in the reflow zones, and are capable of heating the boards and components to the temperature range (240°C to 250°C) required for lead-free soldering of most products. If necessary, higher temperature can be achieved by lowering the conveyor speed. The use of a nitrogen atmosphere may contribute to improve the wetting of the lead-free parts, and to reduce the amount of no-clean flux residue deposits on probe surfaces for In Circuit Testing /3/. However, nitrogen can increase tombstoning (solder joint lifting) /71/.

Reflow temperature profile. Typical reflow profile parameters for lead-free tin-silver-copper paste (melting point = 217°C) are: ramp rate = 1-2°C/sec or less than 3°C/ sec; soak time and temperature range = 100 seconds at

170-217°C; reflow peak temperature = minimum solder joint peak temperature (235°C to 245°C); reflow time above 217°C for tin-silver-copper = 45-75 sec or less than 90 seconds; cooling rate higher than 2°C/sec if possible, or lower than 6°C/sec. An example of lead-free reflow process qualification is given in /72/.

13.2 Wave Soldering

As the wave soldering process window for Sn-3Ag-0.5Cu solder is narrower than for tin-lead wave solder, more precise process control is required. Using the correct process parameters, lead-free wave soldering can be achieved successfully.

Atmosphere. The use of a nitrogen atmosphere typically enables soldering temperature to be reduced by 10°C, improves the process window, and yields a more reliable joint, but at a higher cost compared with air.

Equipment. Wave soldering machines used for lead-free assembly may require longer contact time to achieve the desired wetting, due to the lower wettability of lead-free solders relative to tin-lead ones. Once the equipment is modified or upgraded for lead-free processing, a tin-lead process can no more be employed. The wave soldering machine must have an adequate preheating capacity to maintain thermal shock to the assembly when it enters the solder wave to within 100°C.

The solder pot needs to be drained, cleaned, and refilled with lead-free solders. The surface coatings on the pot pump assembly and nozzle can be a major issue when handling multiple tin-based chemistries. When normally filled with wet solder, the pot is protected from reaction with the atmosphere. With too frequent drainage of wet solder and re-filling with new solder, the solder pot is highly stressed from high to low temperature and vice versa. Improper cleaning or incorrect cleaners can cause further damage to the anti-rust and anti-corrosion material layer on the surface. Furthermore, high tin-containing solder alloys require the pot coating to be non-reactive, as stainless steel components in the wave solder pots are attacked (corroded) by lead-free alloys over time. Similarly, the compatibility of the lead-free solder paste with the pump impellor and solder bath nozzles should be verified.

Wave soldering machines for which the pot show signs of poor performance and aging when used for tin-lead assembly should not be considered for lead-free production. New solder pots, pump assemblies, and lead-free compatible flow ducts should be used where appropriate. If required, the wave soldering machine supplier should be contacted for a lead-free upgrade of the equipment.

For existing wave soldering machines that are still relatively new, it is advisable to modify the pump assembly, nozzle, and flow duct of each chip wave and Lambda wave by applying a coating to protect the equipment from erosion. Typical lead-free upgrade package components include: first wave (chip wave), pump assembly, nozzle (with coated layer), flow duct, and secondary wave (Lambda main wave).

Certain wave machines with stainless steel pots cannot be upgraded for lead-free wave soldering due to the need for solder pot replacement. The jacking stand for the stainless steel pot may not support the new cast iron pot and needs to be changed. Recently, wave solder equipment manufacturers have been offering lead-free compatible parts as standard options.

Process parameters. For lead-free wave soldering with Sn0.7Cu, the peak temperature registered on the bottom of the board is 255°C, whereas the peak temperature recorded on the top side is 198.8°C. The dwell time in the main contour wave (Lambda) is 3.5 seconds and the total time above the liquidus temperature (227°C 217-220°C) is 9.7 seconds.

Solderability, wettability. As most lead-free solders have a higher melting temperature than eutectic tin-lead solder (e.g., 217 to 227°C versus 183°C), oxidation of high-tin solders can become a greater issue. A higher rate of dross (a metallic oxide) formation can be observed on the surface of molten lead-free solder in the presence of air, compared with tin-lead solder. Although the rate of dross formation varies depending upon the lead-free solder used, this result in degradation of solder performance. Conventional no-clean fluxes may dissipate or become inactive before reaching the peak solder temperature. Solderability studies of lead-free alloy and component finish in both air and nitrogen have concluded that lead-free solder has lower solderability than tin-lead solder, especially when weaker no-clean VOC-free fluxes are used. In addition, the necessary removal of dross, which adheres to the solder pot surfaces as it cools, causes product interruption and additional labor cost. Studies have also shown that solderability is considerably improved when processing takes place in an inert (nitrogen) atmosphere.

The required process temperatures for good wetting can be reduced with the use of nitrogen, thereby reducing the potential damage to temperature-sensitive components. Nitrogen atmosphere may be necessary, especially with complex boards with varying finishes and thermal requirements. The oxygen levels in nitrogen atmosphere should generally be kept below 350 SCFH when using no-clean VOC-free fluxes, to minimize soldering defects and maximize wetting.

For thick PCBs (such as 14-layer boards), the hole fill capability is not as good using lead-free solders as for tin-lead solders. Solutions such as press-fit connectors or selective soldering technology are being investigated for such situations.

Lead contamination may cause fillet lifting at high temperature. Therefore, tin-lead HASL boards should not be used with lead-free wave solder. Lead-free coated components

should be used wherever possible. In addition, the cooling rate/profile needs to be well controlled. Lead contamination resulting from the processing of lead-based parts using lead-free wave soldering equipment can be regarded as "intentionally added" substances.

14. How should we perform lead-free repair and rework?

Rework is conducted for defective components using either hand soldering irons for leadframe and chip termination components, or BGA/CSP rework equipment for BGA/CSP components. Challenges in reworking lead-free soldering assemblies include: spacing between BGA/CSP and leadframe components to avoid secondary reflow of leadframe components during BGA/CSP rework, selection of lead-free rework materials which should be able to cater to both surface-mount and wave-assembly operations, rework process temperature profile to minimize the risk of internal delamination or popcorning in moisture-sensitive plastic components.

Rework on lead-free assemblies can be performed with existing rework equipment, both for hand soldering rework and BGA/CSP rework. However, modifications to existing equipment may be required, as detailed below for the temperature setting of hand soldering equipment. It should be ensured that tools for rework and repair are identified as lead-free. In addition, the rework station should be separately located (although most of the rework equipment for tin-lead can still be used for the lead-free solders).

Lead-free rework is conducted at higher temperatures (typically, 30°C higher) than for tin-lead solder. As previously noted, the typical minimum keep-out spacing for BGA/CSP components from leadframe components is 150 mils (3.81 mm). This distance is necessary to avoid localized secondary reflow of adjacent components during rework operations.

Flux and solder selection are critical. For BGA/CSP rework, the solder paste should be the same as that used for assembly. The recommended lead-free wire for hand soldering rework is Sn3.5Ag, due to its long history of use. Sn3Ag0.5Cu and Sn0.7Cu are the preferred lead-free wave solder alloys.

The hand soldering equipment temperature settings may need to be raised by one or two settings to accommodate the higher melting temperature of the lead-free solder wire (221°C for Sn3.5Ag, versus 183°C for tin-lead). Alternatively, the same settings may be used as for tin-lead, but the hand soldering equipment tip should be left on the reworked part (solder pad and component lead) for a longer time than for tin-lead solder before applying the solder wire to ensure reflow. Whether this may cause the solder tip to wear out more quickly needs to be verified.

Further information on the rework of lead-free assemblies is provided in /3/.

15. How should we perform lead-free inspection and testing?

The purpose of inspection is to detect manufacturing nonconformities, both by visual assessment of the appearance of solder joints (e.g., bridging, insufficient solder, misalignment, opens, non-wetting) using optical microscopes, and by automated inspection using X-Ray imaging and in-circuit testing. Currently, the same inspection equipment is employed for lead-free and tin-lead joints. However, retraining of the inspectors and operators may be required due to differences in inspection criteria between lead-free and tin-lead joints.

Acceptance guidelines for lead-free solder joints at optical inspection. The criteria for inspecting visual defects are typically set by industry standards such as IPC-A-610D /73/, which has been revised to incorporate visual inspection criteria for lead-free solder joints. This revision is due to differences in solder joint visual appearance between lead-tin and lead-free joints (due to the differences in the solidification behavior), which are characterized by dullness, reduced surface smoothness, lower wettability and potentially more cratering compared with tin-lead joints. Although dull or shiny joints are acceptable, reduced wetting is not.

At this time, pre-existing cracks can be induced by thermal and/or mechanical fatigue of the solder joints from reliability testing. This method can be used in conjunction with electrical continuity measurements to determine open or partially open solder joints and their distribution for a specific component.

Acceptance guidelines for lead-free solder joints at automated inspection. Current automated optical inspection criteria, which have been optimized for lead-based assemblies, are not suitable for lead-free assemblies due to differences in solder joint visual appearance. However, using a proper reference standard, the inspection system can be programmed to categorize good, marginal, or poor quality lead-free or tin-lead joints. This is possible as most of the combinations of solder alloys and surface finishes have an impact on the appearance of solder joints that can be characterized. Therefore, automated optical inspection (AOI) settings require to be adjusted depending on the solder alloy-surface finish combination being inspected.

Regarding automated X-Ray inspection, the coefficient of X-ray absorption of lead-free alloys is reduced relative to that of tin-lead alloys, which can alter X-ray images. Calibration coupons can be employed to program the X-ray system for lead-free joint inspection.

Acceptance guidelines for in circuit test of lead-free assemblies. There are no differences in functional testing between lead-free and tin-lead soldered boards.

16. How do we trace lead-free materials, parts and sub-assemblies from lead-based ones?

The change-over to lead-free manufacturing requires that lead-free materials, parts, sub-assemblies and final product can be distinguished from the corresponding lead-based ones. This is important for production, as well as rework and repair of field returns and recycling. Lead-free products can be identified by their part number or serial number, lead-free marking applied on both parts and sub-assemblies within the product, as well as on the outer packaging, the effective date of designation change, PCNs, traceable documentation systems, and staff training.

It is recommended that all lead-free materials, components and boards should have new (unique) supplier part numbers (PNs) assigned to distinguish them from tin-lead ones /74, 75/. Suffix or prefix additions to existing P/N structures are acceptable. A survey conducted by Avnet and Technology Forecasters in November 2004 estimates that only 52% of component suppliers are planning to issue new part numbers for lead-free parts, and that 42% plan not to change part numbers, and instead to identify lead-free components using designation printed on component packaging (37%), date of manufacture (31%), or marking on the components (27%) /9/.

Standards for marking lead-free parts and assemblies include JEDEC JESD-97 /76/, JEITA ETR-7021 /77/, and IPC-1066 /78/. These standards permit the type of lead-free materials contained in the part to be identified, and for JESD-97 and IPC-1066, the part process compatibility (maximum process temperature) to be assessed by the end-user. Equipment manufacturers should familiarize themselves with these marking methods, and should identify the effective date of change in part designation.

However, many electronic manufacturers use non-standard marking methods, and consequently the same part may be designated using different marking schemes in different countries. If the lead-free part supplier uses a non-standard marking scheme, it should be ensured that part identification meets the following requirements:

(i) All components of sufficient size should have their termination composition identifiable (with reference to a datasheet). On smaller components, where no marking is possible, the innermost packaging material should specify the termination finish composition.

(ii) The inner packaging (tray, tube, and reel) of all components should be marked with traceable information that indicates that no lead is present in the components.

(iii) No lead-free markings are required on the outer packaging boxes as long as suppliers can track their lead-free products versus their lead-containing ones and ensure that only one type of part is being delivered to the customer.

(iv) Part datasheets should indicate the termination solder composition, maximum part temperature rating, recommended and absolute reflow profile limits, and moisture sensitivity rating. If this information is not provided in the datasheet, a reference to where it can be located should be included.

Manufacturers should monitor PCNs issued by their part suppliers when transitioning to lead-free electronics. As per JESD46-B /79/, all changes on existing parts should be documented by a PCN issued by the part manufacturer to notify their customers of product transition to lead-free. An example of PCN issued by a component manufacturer is available in /80/. Any changes related to lead-free components should be considered major changes. Sample devices and qualification data should be available to customers at the time the PCN is issued or the new product is introduced.

All manufacturers who provide notification that they will be producing lead-free products should provide a product roadmap to their customers indicating the planned changes and timeframe for availability. 75% of the component suppliers surveyed in /9/ stated that they will deliver compliant parts with the same lead times as for current parts. Only 2% indicated that lead times will increase for lead-free parts /9/. More than half (53%) of the component suppliers surveyed did not expect to increase prices for compliant parts, which is likely to be associated with high production volumes, while 35% of suppliers expected a potential price increase /9/. However, the production of exempted parts in reduced quantities has also prompted concerns with the pricing of such parts /17/.

Any discontinuances of existing parts must be published to the customers, per standard JESD48-A /81/. Based on the survey previously mentioned /9/, many component suppliers do not plan to totally discontinue lead-containing products, as they anticipate a continuing demand for leaded products from exempted sectors. Component suppliers who plan to discontinue non-compliant parts typically intend to give customers a six-week to 24-month time frame to return non-compliant products after a PCN or end of life announcement is issued /9/.

Finally, it is recommended that manufacturers conduct the shipment and use of tin-lead coated leadframes and chip termination components to depletion, followed by the introduction of lead-free coated components.

17. What are the standards applicable to lead-free assembly processes, qualification and inspection?

The release of new and revised standards applicable to lead-free assembly process, qualification and inspection should be monitored, as these operations may have an impact on the design.

IPC is currently revising or has recently revised standards /49, 58, 60, 65, 73, 82-86/ to address lead free assembly. Standards /65, 82-86/ relate to solderability requirements and testing of electronic parts and boards, and requirements for soldering materials. IPC-A-610D /73/ has been revised to incorporate visual inspection criteria for lead-free solder joints.

J-STD-020C /58/, JEITA ED-4701-301A /59/, J-STD-033C /60/ and Mil-Std 202G Method 210F /61/ relate to component moisture and thermal sensitivity classification, and the handling, packing and assembly of moisture sensitive components.

JESD22A-121 /49/ specifies procedures for measuring whisker growth on tin-based finishes.

Other standards applicable to lead-free assembly process, qualification and inspection, include /87-89/. PCB qualification standards /90-93/ address lead-free PCB finishes. Common lead-free platings and coatings are also covered in PCB design /94-97/ and multichip module design /98/ standards.

18. What education, training and information resources are available to help in the successful implementation of lead-free product development?

Providers of education, training and information resources on lead-free electronics include research organizations /38, 99-101/, consulting companies /38, 102-104/, contract manufacturers /105/, vendors of electronic manufacturing products /106, 107/, and component/equipment manufacturers such as /108/. Such providers cover topics ranging from lead-free legislation, implementation, material and part selection, design, manufacturing, to lead-free reliability.

Closure

Key issues in the assembly of lead-free electronics that have not been fully resolved include component moisture and thermal sensitivity, solder joint manufacturing defects, backward and forward compatibility, and lead-free part traceability throughout the supply the chain.

The current state-of-knowledge on lead-free manufacturing and reliability is not as extensive as for lead-based electronics, which has a 40-year legacy. Although the electronics industry is aware of potential reliability risks specific to lead-free technologies, including excessive intermetallic growth, tin whiskering, and electrochemical migration, the long-term reliability of lead-free assemblies remains to be quantified. There is a need for studies addressing this concern, covering the range of available solder metallurgies, component terminal metallurgies and PCB pad finishes. Since the majority of studies on lead-free solder joint reliability have focused on single loading conditions (e.g, temperature cycling, high temperature aging), combined loading conditions (e.g., temperature cycling and vibration) need to receive more attention.

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QUALITY LABORATORY FOR INVESTIGATION OF LEAD-FREE MATERIALS AND PROCESSES

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Key words: quality laboratory, testing quality and reliability, solderability testing, lead-free coating, lead-free soldered joints

Abstract: The main technological objective of the GreenRoSE project is to provide European SMEs of the electronics sector with the knowledge and tools to produce electronic equipment free of hazardous substances, with defined quality and reliability. For the realization of the objectives the Advanced Interconnections Technology Laboratory for substitution technology assessment and quality tests has been set up in ITR, ISSP and Cynel. The main testing equipment of the Quality Laboratory in ITR is as follows: solderability testers, rotary dip tester, ionograph , sirometer, digital Viscometer, AOI, resistivity 4 point resistance meter, climatic chamber, stereoscopic and metallurgical microscopes, system for microstructures metallographic preparation of the samples, UV laser system, convection oven and double-wave soldering machine.

The range of investigations that can be carried out in ITR Quality Laboratory concerns: quality investigation of materials and components for assembly processes, quality evaluation of soldering technologies parameters, quality investigation of solder joints as well as climatic tests performance of soldering materials, PCBs and solder joints.

ITR has designed test boards for solderability measurements of PCBs with lead-free coating, characterisation of the immersion tin coating and estimation of solder joints quality produced in reflow and wave soldering processes.

Laboratorij za raziskavo in študij materialov in procesov brez svinca

Kjučne besede: laboratorij, testiranje kakovosti in zanesljivosti, testiranje spajkljivosti, prevleke brez svinca, spajkani stiki brez svinca

Izvleček: Glavni tehnološki cilj projekta GreenRoSE je zagotoviti Evropskim proizvajalcem elektronike znanje in orodje za proizvodnjo naprav brez škodljivih snovi, s predpisano kakovostjo in zanesljivostjo. Za uresničitev tega cilja smo ustanovili ustrezne tehnološke laboratorije na Poljskem (ITR, Cynel) in v Latviji (ISSP). V laboratoriju ITR imamo na razpolago sledečo testno opremo : merilnik spajkljivosti, merilnik omakanja, ionograf, sirometer, digitalni viskozimeter, AOI, štiri-točkovni merilnik upornosti, klimatsko komoro, stereoskopske in metalurške mikroskope, sisteme za mikrostrukturno in metalurško pripravo vzorcev, UV laserski sistem, temperaturno komoro in napravo za valno spajkanje.

V tem laboratoriju lahko opravimo naslednje raziskave : preiskave kakovosti materialov in komponent za montažo, preiskave kakovosti tehnologij spajkanja, preiskave kakovosti zaspajkanih stikov, kakor tudi obnašanje materialov, tiskanin in spajkanih stikov v klimatski komori.

ITR je razvil testne plošče za meritve spajkljivosti tiskanin s prevlekami brez svinca, za vrednotenje spajkanja s potapljanjem ter za oceno kakovosti spajkanih stikov pri različnih načinih spajkanja.

1. Introduction

The main technological objective of the GreenRoSE project is to provide European SMEs of the electronics sector with the knowledge and tools to produce electronic equipment free of hazardous substances (in particular lead and halogen compounds).

For technology assessment and quality tests the Advanced Interconnections Technology Laboratory has been set up. The laboratory has contributed to research identified in WorkPackages and specifically to develop techniques and standards for quality and reliability testing. This laboratory will also support the needs of SME Core Group partners throughout the project and provide a support platform for wider exploitation of the new technologies both during and after the project.

The Quality Laboratory has been set up at ITR and Cynel, Poland as well as at ISSP, Latvia.

2. Description of the quality laboratory

The Quality Laboratory in ITR is equipped with the following equipment:

- Solderability testers MK-6A, General Electic Co. and Menisco ST 60/LT 6000, Metronelec
- Rotary dip tester, ITR
- Ionograph Omega Meter 600R, Alpha Metals

- Sirometer Model 300, Alpha Metals
- Brookfield Digital Viscometer DV-II ,
- AOI CAMTEC 2V50 system, PCB-MB Material Anlagen Service
- Resistivity 4 point resistance meter model 34420A, Agilent Technology
- Climatic chamber C-70/200, CTS
- Stereoscopic Zoom Microscope Nikon SMZ1500 (Zoom range 7X - 112,5X)
- Metallurgical Microscope Nikon Eclipse L150 (Zoom:100X,200X,500X,1000X)
- System for microstructures metallographic preparation of the samples
- UV Laser system.
- Convection oven VIP70A, BTU
- Double-Wave soldering machine ERSA ETZ 250

Solderability testers

Two types of computerized wetting balance machines for solderability measurements are available in the Laboratory at ITR. First one Menisco ST60 is a fully automatic (Fig.1). The Menisco ST60 can be used for incoming quality control of materials, preassembly testing after extended component storage, soldering process parameter selection and optimization, flux efficiency determination, solder alloy, and solder paste quality checking and monitoring. The second solderability tester Mk6A makes possible to measure surface tension or interfacial tension of alloys and solderability of components by Wetting Globule Method.

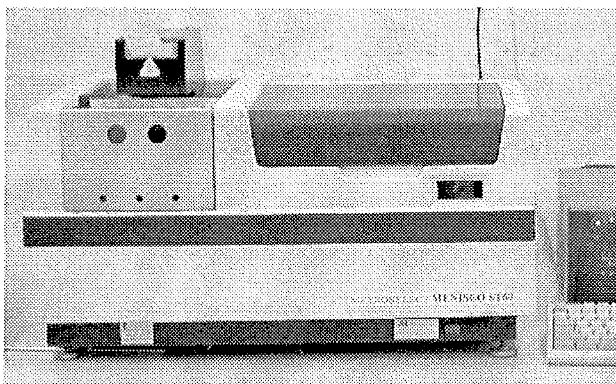


Figure 1. Solderability tester Menisco ST60

Rotary dip tester TL-14

Rotary dip tester TL-14 is recommended for solderability testing of plated through holes, surface conductors and attachment lands. It simulates wave soldering process.

Ionograph Omega Meter 600R

Omega Meter Systems allows quantitative measurements of ionic contamination on printed circuit boards and printed wiring assemblies resulting from varied technological processes.

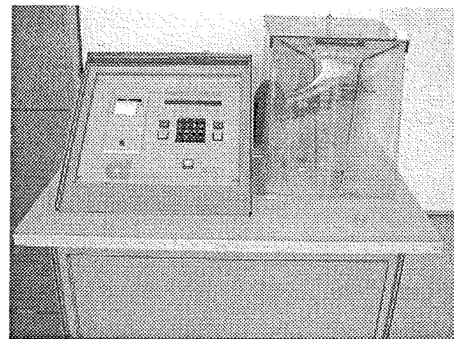


Figure 2. Ionograph Omega Meter 600R

Resistivity 4 point resistance meter

Agilent 34401A Multimiter can be used to measure resistance in the ranges: 100Ω, 1KΩ, 100 KΩ, 1MΩ, 10 MΩ and 100MΩ with maximum resolution of 100 μΩ.

Sirometer Model 300 and Climatic chamber CTS - 70/200

Sirometer allows measuring the insulating material's resistance and electro-migration to the flow of current between conductors (Fig.3a). Surface insulation resistance (SIR) and electro-migration (EM) testing are used in a number way to characterize residues or determine the effect of residues on the performance of printed circuit boards. Sirometer co-operates with the climatic chamber CTS -70/200 in our laboratory. Characteristics of the climatic chamber are presented below:

- Temperature range + 10°C to +95°C
- Humidity range 10% to 98% rel. humidity
- At dew. point range I +7°C to +89.5°C
- Dew. point range II -5°C to +7°C
- Temperature fluctuation: ± 0.1 to ± 0.3 K temporary

Brookfield Digital Viscometer DV-II

The Brookfield digital viscometer, Model DV-II is a laboratory Viscometer which can be utilized with all Brookfield accessories (Fig.3b). It allows to measure rheological properties of solder pastes, conductive adhesives and other materials.

Microscopes

The Stereoscopic Zoom Microscope Nikon SMZ1500 with zoom range 7X - 112,5X and provides very good optical performance (Fig.4a).

The Metallurgical Microscope Nikon Eclipse L150 (Zoom: 100X, 200X, 500X, 1000X) can be used for inspection and measurements. CF160 infinity enables the microscope images to be crisp and clear with high contrast and minimal flare (also under dark field microscopy) (Fig.4b).

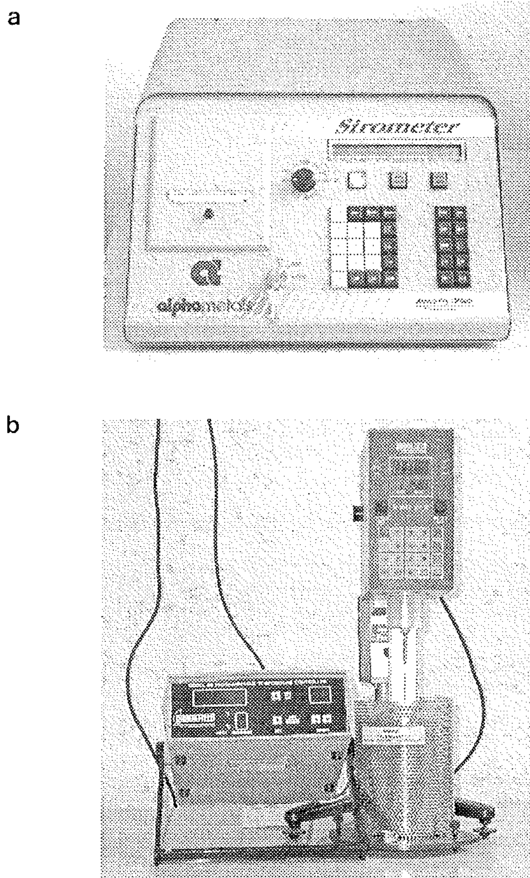


Figure 3. Sirometer Model 300 (a), Brookfield digital viscometer DV-II (b).

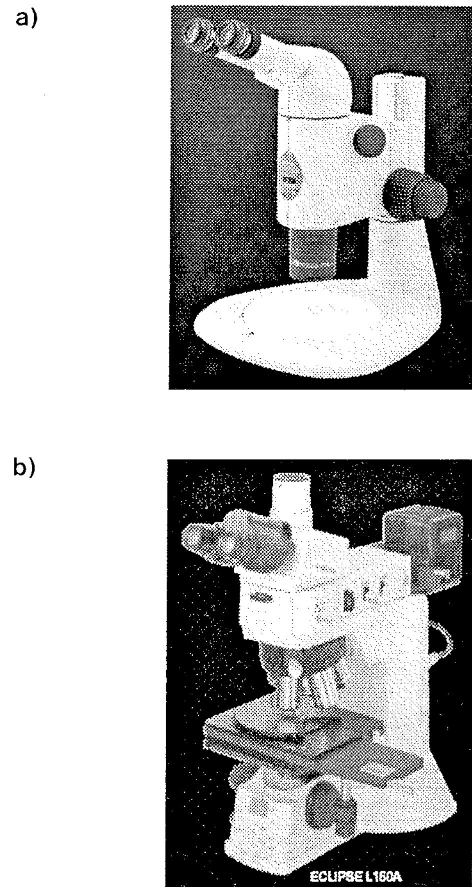


Figure 4. Stereoscopic Zoom Microscope (a). Metallurgical Microscope (b).

System for preparation of the metallographic specimens

System for preparation of metallographic specimens consists of a cut-off machine Mecatome 255/300, a polishing machine Mecapol P262 and an automatic and manual cut-off machine Mecatome 255/300.

The specimens are used for quality evaluation of the laminate system, plated-through holes (PTHs), copper foils, plating, and/or coatings in PWB production and also for quality of solder joints.

Automatic Optical Inspection CAMTEC 2V50 (AOI)

Camtec 2V50 provides an optimal tool for use in the visual inspection of printed circuit through the entire manufacturing process as well as after paste print, component placement and reflow process.

UV Laser system

High power diode-pumped, repetitively q-switched UV:YAG laser system. The machine is used for drilling micro-via and structuring conductors, channels as well as cutting various shapes in many different organic and metallic materials. UV laser system is also used for very precision measurements of distance in the aim to control the quality of manufactured PCBs.

Convection oven VIP70A

VIP 70A is a convection oven with 5-Zone independent control air configuration. Windows-based operating software provides user-friendly control, advanced profiling, data collection, programmable event sequencing and host communication. It has edge rail conveyor and fixed and retractable center board supports eliminate sagging associated with thin boards.

Double wave soldering machine ERSA ETZ 250

Double wave soldering machine ERSA ETZ 250 enables analyzing and controlling soldering processes of mixed assemblies with SMD and Through-Hole components. It is completely adopted for lead-free soldering. The machine has got two flux systems (spray and foam) what makes possible to investigate the whole spectrum of fluxes.

3. Test boards for quality assessment of materials and solder joints

ITR has also offered test boards for quality assessment of materials and solder joints (Fig.5a-e, Fig.6 and Fig.7). All test boards can be manufactured in ITR and SMEs (GreenRoSE partners). Assembly processes can be done at pilot line in Semicon and ITR.

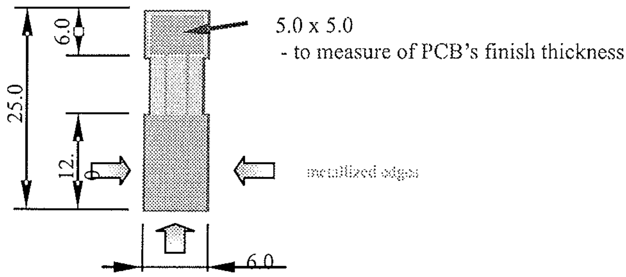
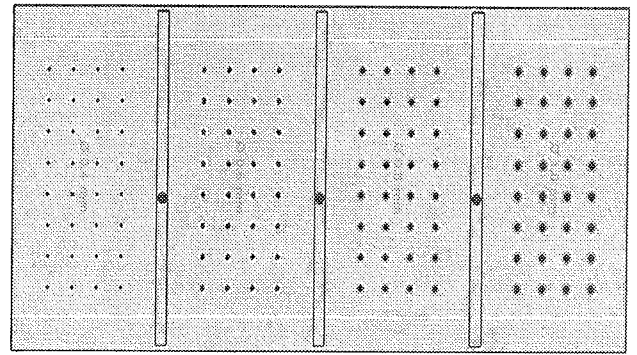


Figure 5a. Test board for wettability test using the meniscograph method, tin thickness measurement and assessment of tin porosity.



d)

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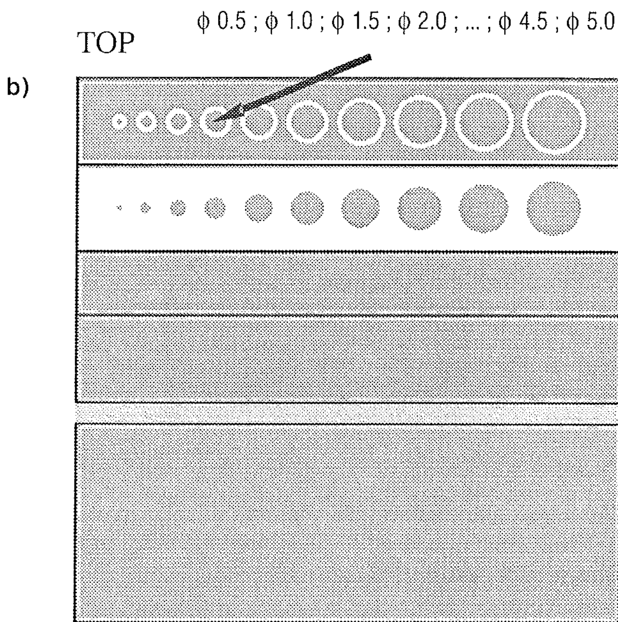


c)

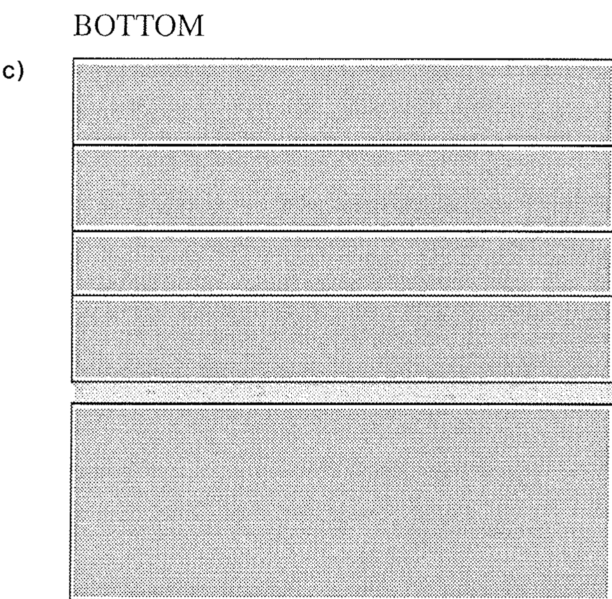


Figure 5b and 5c. Test board: for spread tests in reflow soldering process (b) and for PTH wettability test carried out by rotary-dip test (c).

e)

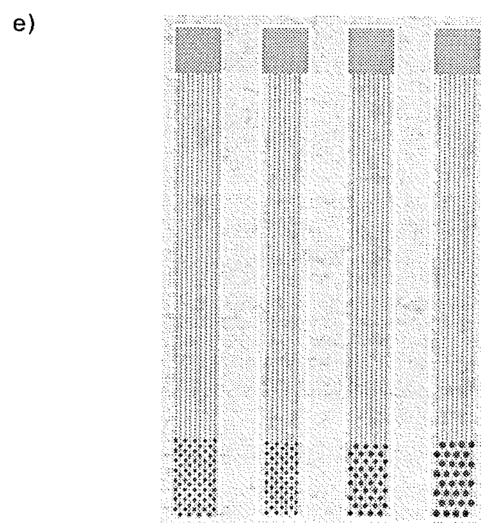


Figure 5d and 5e. Test board for: tin thickness measurement in PTH - diameters: ϕ 0.4; ϕ 0.6; ϕ 0.8 and ϕ 1.0 mm (d) estimation of solder mask compatibility with the tin immersion process and soldering processes (e).

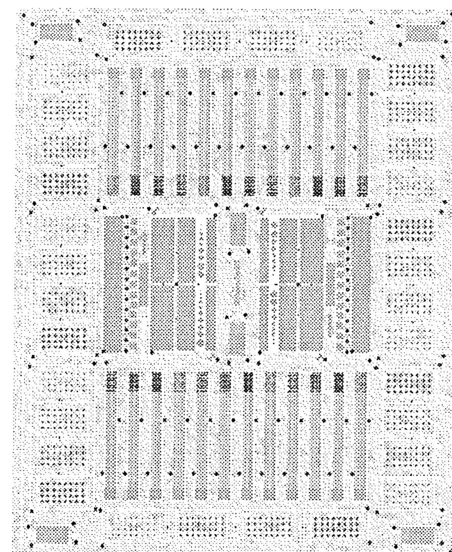
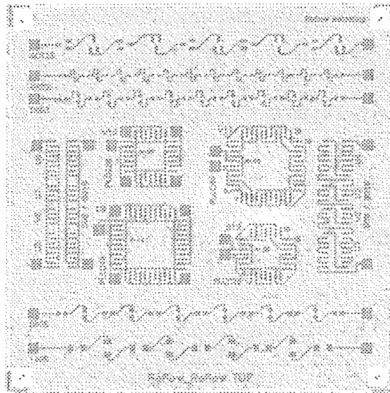


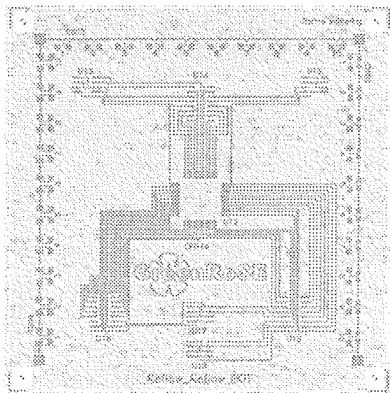
Figure 6. The set of test boards

Reflow soldering

TOP

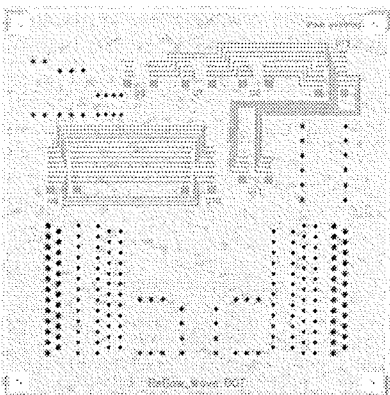


BOTTOM



Wave soldering

TOP



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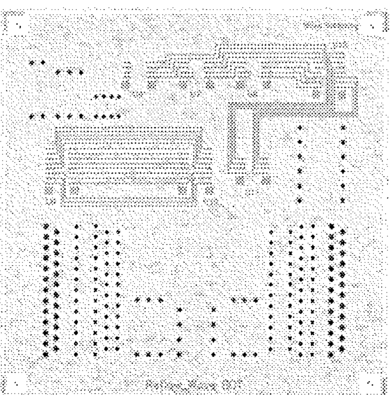


Figure 7.Test boards for soldering processes.

4. ITR Quality Lab investigation range

The range of investigations that can be carried out in ITR Quality Laboratory concerns the following issues:

1. Quality investigation of materials for assembly processes, included:
   - Solder alloys for wave soldering process:
     surface tension and surface interfacial tension of alloys, solderability
   - Solder wires for hand soldering process:
     dimensional tolerance, flux content, flux efficacy test, copper corrosion test, surface insulation resistance comb test and electrical migration test of flux residues, ionisable surface contaminants
   - Solder pastes:
     viscosity, wetting, slump, solder ball, tack, metal content by weight, solder shapes- granularity, copper corrosion, ionic residue, surface insulation resistance comb test and electrical migration test of flux residues.
   - Fluxes:
     activity, acid value, non-volatile matter, halogen determination, tack test, spread test, copper corrosion, ionic flux residues, ionic residue, surface insulation resistance comb test and electrical migration test of flux residues.
2. Quality investigation of components for assembly processes, included:
   - Printed circuit boards:
     Visual and dimensional examination, plating thickness /microsection/ and immersion tin thickness, solderability of pads and through holes, solder mask compatibility of soldering process, tin whiskers, ionic contamination, surface insulation resistance, electrical tests, changes in resistance and delamination after thermal shock.
   - Electronic components:
     solderability of electronic components.
3. Quality evaluation of soldering technology parameters, included:
   - Wave soldering process:
     time-temperature profile selection, flux selection, checking of fluxing process.
   - Reflow soldering process:
     solder paste selection, stencils laser made, solder paste inspection, time-temperature profile choice.
4. Quality investigation of solder joints, included:
   - Evaluation of solder joints quality:
     Visual inspection of solder joints, solder joint failures qualification, electrical and mechanical measurements of solder joints,
   - Solder joint cross sections evaluation for:
     explanation of solder joint failures, investigation of intermetallic compounds.
5. Climatic tests performance of soldering materials, PCBs and solder joints.

4.1. Catalogue of available services for quality testing

In the Quality Laboratory four groups of tests are available:

- test group for lead-free materials applied in printed-circuit board assemblies,
- test group for printed circuit boards with lead-free finish,
- test group for lead-free components for surface mount technology and through- hole technology,
- test group for lead-free printed-circuit board assemblies.

The tests are performed according to the required international standards.

5. Examples of the performed tests

5.1. The Wetting Balance measurement

For solderability measurement of PCBs with different finishes the wetting balance method was used. The maximal wetting force Pmax, wetting time τ_Z, time to obtain 2/3 maximal theoretical force $P_{maxTeor.}$ and wetting angle θ after 2 and 3 s were measured using Meniscograph Solderability Tester MENISCO ST 60 (Fig.1).

Table 1. Solderability requirements

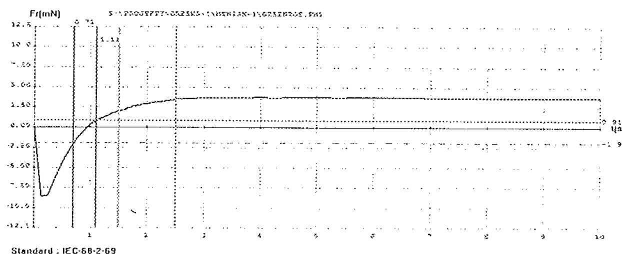
Standard	Criteria	Requirement
J - STD 003 [2]	Wetting time τ_z [s]	≤ 2 s
	Max wetting force P_{max} [mN/m]	≥ 120 mN/m
	Contact angle θ [°] after 3 s	$\leq 55°$

The following experimental procedure was established:

- Atmosphere: air,
- Test coupon: 18μm Cu double-clad FR-4 with Sn, OSP and Ag coatings, thickness = 1.5 mm (Fig.5a),
- Alloy SAC407,
- Flux: VOC- LP11/AC, TN/4A and MPWC, ITR and VOC -free - 330 Alpha, 1075-EXR46 Indium and Koki,
- Immersion depth: was 3 mm,
- Immersion time: 10 s,
- Immersion speed: 21 mm/s,
- Test temperatures: 250°C.

The test boards have been tested in the state "as delivered", after aging: dry heat - 4h at 155°C, after humidity (24h at 125°C + 96h at 30°C 70% RH) and 1 x reflow process.

Examples of boards with very good solderability and bad solderability are presented in figures 8 and 9, respectively.



a)

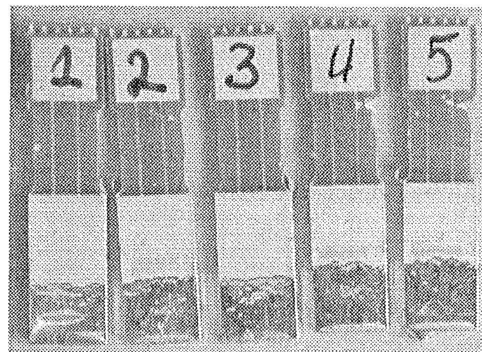


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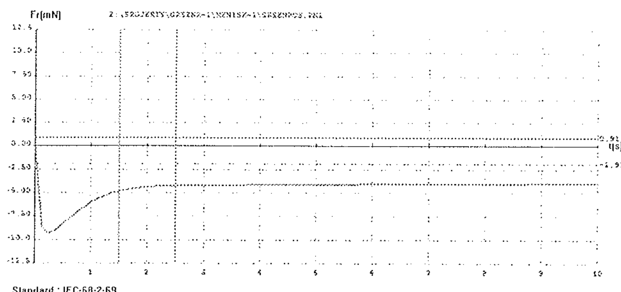
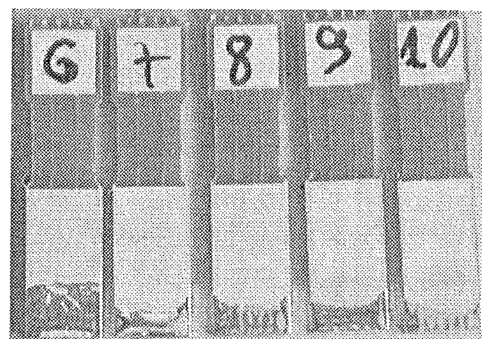
Figure 8. An average wetting curves for test board with Sn that passed the requirements (a) and example of the test board (b).



a)



b)

Figure 9. An average wetting curves for test board with Sn that did not pass the requirements (a) and example of the test board (b).

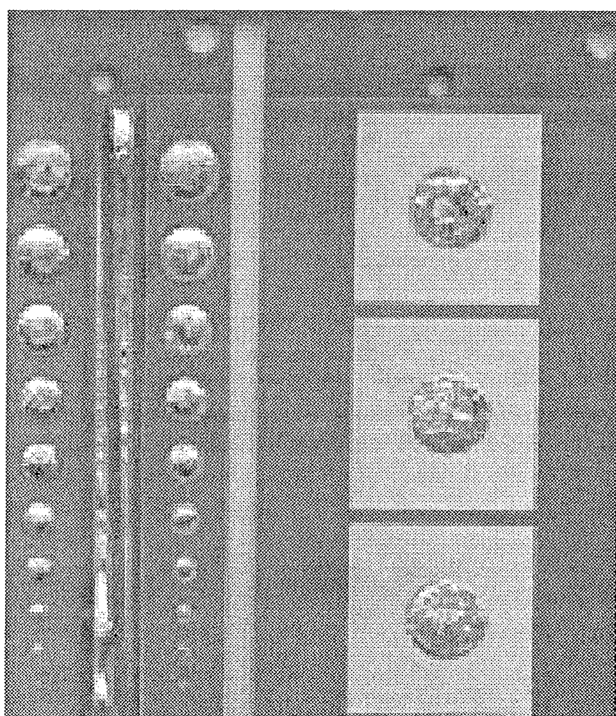
5.2. The reflow wettability test

Wettability tests of lead-free solder pastes on PCBs with led-free coatings have been carried out on the base of the Standard ANSI/J-STD-005 /3/. After applying solder paste

by stencil the specimen is placed on the surface of the soldering bath at the temperature 250°C for 20 s.

Requirement: class "A" - When examined visually at 10X, the solder shall uniformly wet surface and there should be no evidence of dewetting or non-wetting of the copper and there shall be no solder spatter around the printed dots. (Defects: B- non-wetting, C- dewetting, D- spattering).

An example of the testing equipment is shown in Fig.10. Examples of good and bed wettability of lead-free solder pastes on PCBs with led-free coatings are presented in Fig.11.



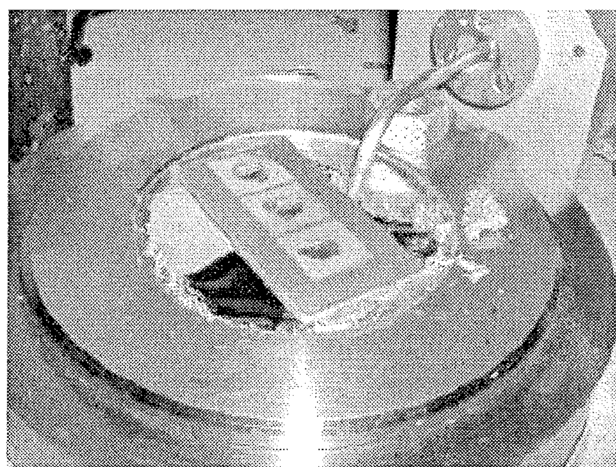
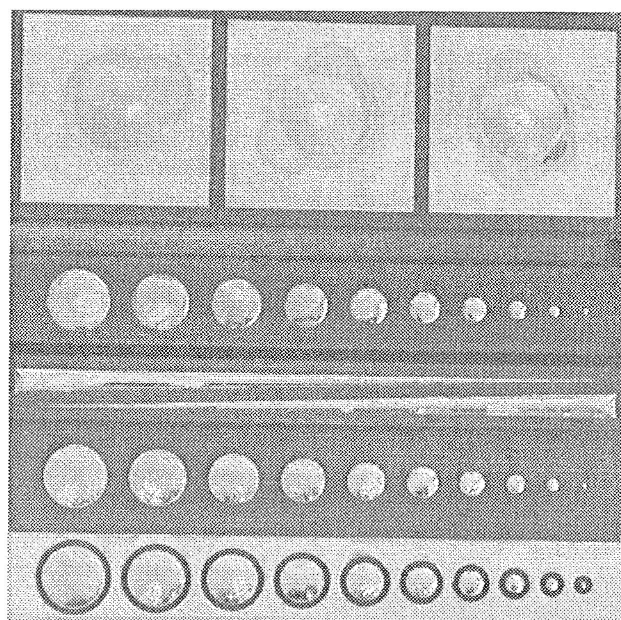
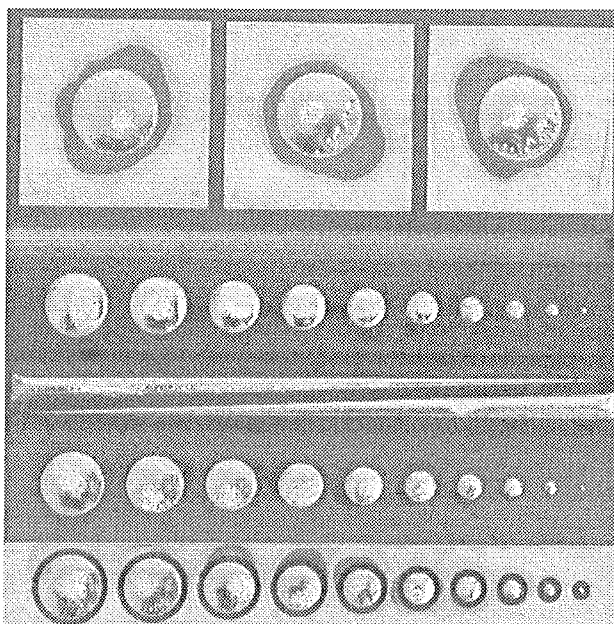


Figure 10. Example of the testing equipment.



a)



b)

Figure 11. Example of good (a) and (b) bad wettability of solder paste on tin coating.

6. Conclusion

The Quality Laboratory in ITR is equipped with modern measuring and controlling devices and technology equipment which allow performing quality investigation of materials and components, quality evaluation of soldering processes and solder joints as well as climatic tests.

The necessary materials and services for the quality test can be supplied by the following Partners: Eldos, SEMICON and RWT. Eldos can manufacture test boards; Cynel can deliver some lead-free alloys. The assembly processes can be done in Semicon, RWT and ITR. Other quality investigation can be carried out in the laboratory of other GreenRoSE's research Partners: ISSE, Cynel Unipress, ITRI, TUB, IVF, IJS and HIPOT R&D.

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8. Acknowledgment

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ACCELERATED RELIABILITY TESTS OF LEAD - FREE SOLDERED JOINTS

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Key words: reliability tests, accelerated tests, tests of lead-free soldered joints, mechanical shear strength, fatigue strength

Abstract: Important condition for implementation of lead - free technology, according to the RoHS directive of European Community, is the warranty of good quality and reliability of electrical joints executed in new, environment - friendly technology. Especially for small electronic enterprises it is difficult to prove that the product reliability is not lower than before the change. One of the solutions is application of appropriate accelerated test methods. Typical tests applied in Warsaw University of Technology for reliability assessment of solder joints are investigations of mechanical shearing strength at appropriate temperature and fatigue strength in cycling processes. For investigation of fatigue strength are applied different accelerating factors (temperature changes and thermal shocks, cycling of electrical charge and mechanical cycling). The principles and discussion of appropriate test methods are presented.. Some preliminary results show that mechanical fatigue tests may be used for accelerated comparative reliability investigations for certain classes of electronic products.

Pospešeni testi zanesljivosti spajkanih stikov brez svinca

Kjučne besede: testi zanesljivosti, pospešeni testi, testi stikov spajkanih brez svinca, mehanska natezna trdnost, utrujenost materiala

Izvleček: Pomemben pogoj pri upeljavi tehnologije brez svinca v skladu z RoHS direktivo Evropske skupnosti, je zagotovilo dobre kakovosti in zanesljivosti stikov izdelanih z novo, okolju prijazno tehnologijo. Še posebej majhnim podjetjem je težko dokazati, da zanesljivost izdelka ni manjša kot pred spremembo. Ena od rešitev je uporaba ustreznih pospešenih testnih metod. Na Varšavski tehnični univerzi izvajamo tipične teste za določanje zanesljivosti spajkanih stikov, kot so raziskave mehanske natezne trdnosti pri določeni temperaturi in utrujenosti materiala pri cikliranju. Pri raziskavi utrujenosti uporabljamo različne pospeševalne faktorje (temperaturne spremembe in termične šoke, cikliranje električnega naboja, mehansko cikliranje). V prispevku pokažemo principe in opišemo ustrezne testne metode. Nekateri uvodni rezultati kažejo, da teste mehanske utrujenosti lahko uporabimo pri pospešenih primerjalnih raziskavah zanesljivosti za določene razrede elektronskih izdelkov.

1. Introduction

Each producer of electrical and electronic equipment must prove that the product reliability is not lower than before the change. One of the solutions is application of appropriate test strategy and accelerated test methods.

By planning and selection of type and parameters for reliability tests of lead - free soldered joints are considered general relations between data sets concerning design, technology and manufacturing factors (solder data, soldering process characteristics and soldered joints characteristics), applied test parameters and required functions determining definition of the failure, shown on fig 1. As failure criteria are chosen the measured changes of electrical resistance /1/ and extent of the cracks formation.

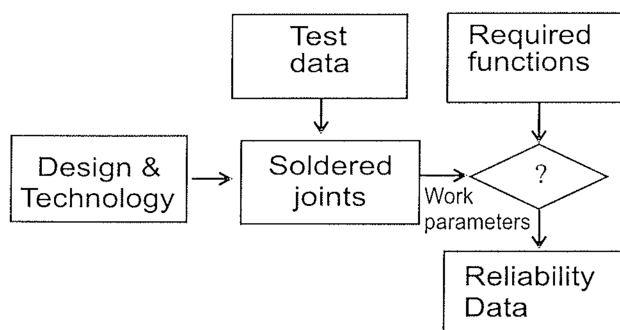


Figure 1: Scheme of data sets for reliability testing.

Preliminary results showed that thermal cycling, thermal shocks cycling and mechanical fatigue tests may be used for accelerated comparative reliability investigations for certain classes of electronic products.

2. Design, technology and manufacturing factors

2.1. Impact of design and technology on reliability issues

The data concerning design (especially applied materials and surface finishes), manufacturing factors and quality

inspection characteristics influencing the properties of lead - free joints shall be determined.

Essential data of design and technology can be divided in following groups:

- soldered materials and surface finishes
- solder and flux data (type, composition, melting temperature, surface energy)
- quality and solderability data of soldered materials
- surface treatment before soldering (e.g. plasma treatment)
- composition and properties of flux and solder paste
- soldering process characteristics (soldering temperature, soldering time, temperature profile, soldering atmosphere, etc.)
- soldered joints characteristics (shape, dimensions, mechanical properties, temperature resistance and quality data determined by visual inspection) of the joints soldered with new alloys.

At present alternative solders are principally based on Sn - Cu, Sn - Ag and Sn - Ag - Cu eutectic alloys. Compared to eutectic SnPb38 solder with melting temperature 183 °C these alloys show some principal differences and strong dependence on the solder composition..

Higher melting temperature (227 °C for SnCu0,7 , 221°C for SnAg3,5 and 217°C for SnAg3,8Cu0,7) is critical for soldering of electronic components with soldering temperature resistance 250°C. The Cu content in wave soldering must be sharply controlled. Temperature window (fig.2) is smaller and new solutions of heating equipment (solder wave, reflow ovens) must be applied.

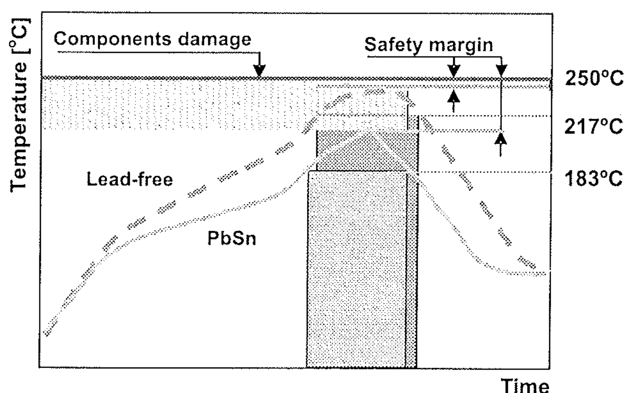


Figure2: Temperature window for SnPb and lead-free reflow soldering

Higher surface energy, smaller wetting force and longer wetting time of lead - free solders are unfriendly for joints quality and soldering productivity. New methods and new parametric data of soldering ability testing are necessary. In many cases these problems must be solved by soldering in nitrogen (N_2) atmosphere. New solutions of soldering equipment are also needed.

The creep rates by deformations of new solders are up - to 100 times lower than by Sn-Pb solders /2/ /3/. This property must be considered by development appropriate fatigue test methods and calculation of accelerating factors.

Poor soldering ability, low creep rate and higher melting temperature are influencing on the thermal and mechanical fatigue resistance. Modification of fatigue test methods and test data will be also necessary.

2.2. Test samples of solder joints

As samples of solder joints for reliability tests can be used:

- Electronic equipment
- Electronic modules
- Test samples

By choice of test models following criteria are applied:

- Representation of investigated product
- Charge conditions
- Simplicity of failures detection
- Measurements ability

3. Working and test conditions

3.1. Working conditions and degradation processes

The real working conditions of soldered joints are the base for selection of appropriate test methods. Soldered joints in electronic modules are subjected to a variety of mechanical and thermal charges as:

- thermal shock during soldering and cooling,
- mechanical charges during manufacturing process,
- thermal stress during storing and transportation,
- mechanical vibrations and shocks during transportation and operation,
- high and low temperatures during transportation and operation
- variation of temperature and thermal shocks during transportation and operation.
- electrical operating power changes

These charges influence following degradation processes:

- relaxation of mechanical and thermal stresses,
- corrosion of the solder, soldered parts an insulating parts,
- diffusion processes,
- whiskers growing
- fatigue and wear,

The solders are specific materials working at temperature near melting point. Especially for the objects working at increased and constant temperature, investigation of diffusion processes, metallurgical transformations as growth

of the grains, decrease of the strength and corrosion are very important. The creep strain rate $\acute{\varepsilon}$ in certain limits can be determined from Arrhenius law /4/:

$$\acute{\varepsilon}_c = A\,\sigma^n e^{-(Q/RgT)}$$

where (for eutectic solder): $A = 1{,}84.10^{-4}\ (MPa)^{-n}$ - experimentally determined constant, n = 5,2 (experimentally determined), Q = 50KJ/mol - activation energy, Rg = $8{,}313.10^{-3}$ KJ/molK, T - absolute temperature.

The Arrhenius Law can be applied for assessment of relaxation of mechanical stresses, corrosion and diffusion processes.

Simplified model of linear deformations and stresses, with disregarded flexion of the PCB is shown on the figure 3. The length initial of the component not soldered is L_0. After heating of the component or heating of both: component and PCB by different thermal coefficients or mechanical deformation of the PCB the length of the component increase to L_1.

Total increase of the component length in relation to the PCB will be ΔL:

$$\Delta L = \Delta T_C \alpha_C - \Delta T_B \alpha_B + \Delta L_M$$

where: ΔT_C, ΔT_B - temperature changes of the component and PCB respectively, α_C, α_B - thermal expansion coefficients, ΔL_M - mechanical deformation.

However, the length of soldered component will be only L_2 because of compression by the force F_C causing the diminution ΔL_C. At the same time the deformation of the PCB and solder joints under the stretching force F_B will be ΔL_B.

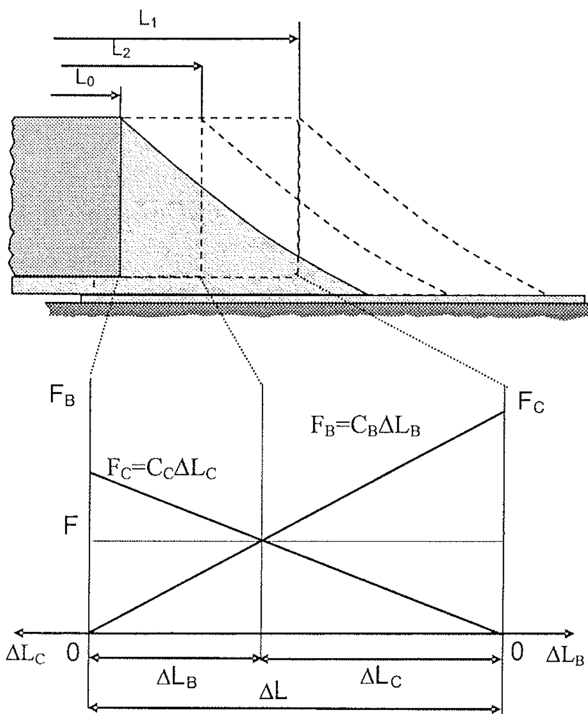


Figure 3: - *Linear deformations of the component - solder - PCB system*

Mechanical charge of the soldered joints (e.g. compression of the component and stretching of the PC board) can be determined from the balance condition:

$$F_C = F_B = \Delta L_C c_C = \Delta L_B c_B = F$$

where: c_C and c_B are the rigidity of the component and PCB with solder joints respectively, and finally:

$$F = \Delta L c_C c_B / (c_C + c_B).$$

It is only approximate value because of simplifications applied and omission of nonlinearity, creep phenomena and plastic deformations.

Good instrument for preliminary studies and selection of test conditions is the finite element modelling of the mechanical system created by soldered component. Example of mechanical deformations of chip resistor 1206 and Flip Chip soldered joints after PCB flexion are shown on fig. 4. FEM models are helpful for understanding of the damaging process and determining the test conditions and optimal shape of the soldered parts.

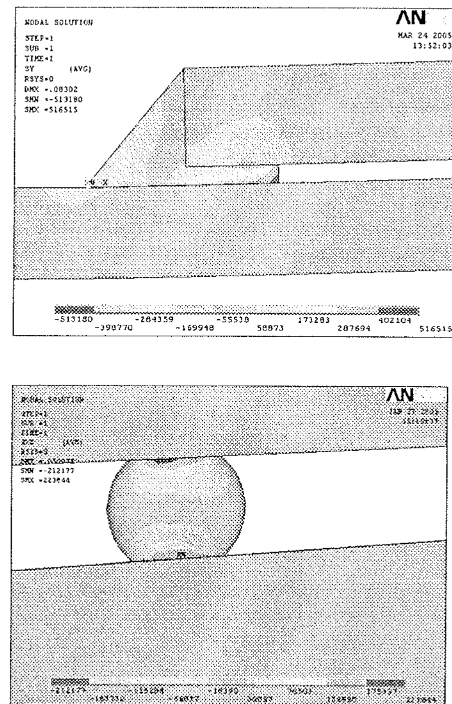


Figure 4: FEM model of the chip resistor and Flip Chip soldered joints

3.2. Accelerated Test Methods

The main accelerating factors by investigation of life time are applications of appropriate range of test temperature and mechanical load of soldered components and PCB in following tests:

- dry heat (for acceleration of physical and chemical processes)
- temperature cycling

- thermal shocks
- mechanical cycling
- electrical power cycling
- thermo mechanical charges.

3.3. Thermal cycling and thermal shock tests

The changes of temperature (fig.5) are the source of stress - relaxation enhanced creep and fatigue of the solder joints and thermo-mechanically induced failures /5/. The mean number of cycles to failure and acceleration factor can be determined by use of experimentally determined models and appropriate empirical relationships.

The rapid temperature changes result in large transient thermal gradients resulting in warping of the surface of the assembly. The test is appropriate for comparative reliability investigations, especially for the products working in thermal shock conditions, e.g. automotive under hood.

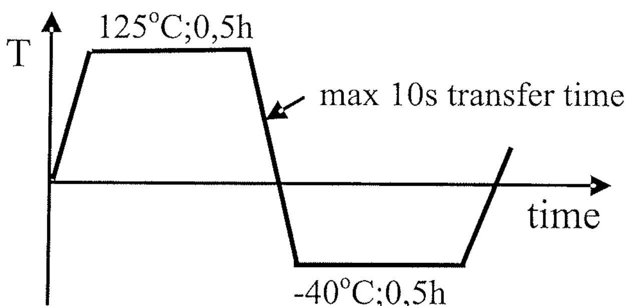


Figure 5: Thermal shock cycle

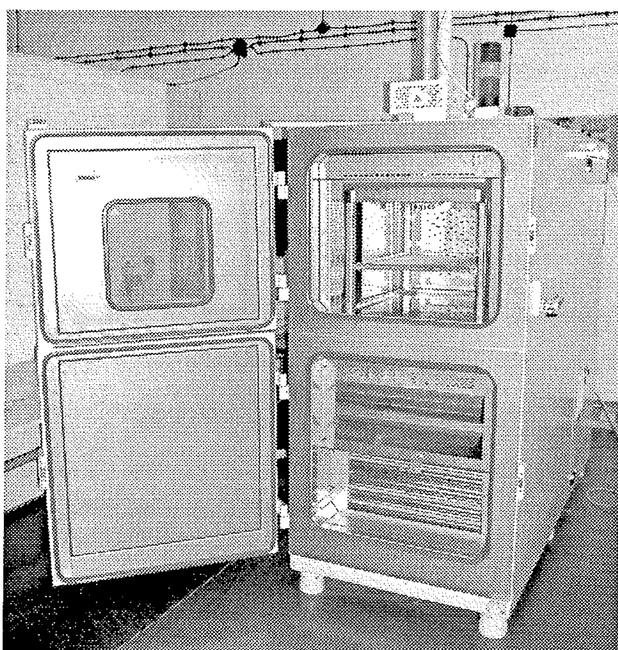


Figure 6: Two Zone Temperature shock chamber

It is performed in dual chamber test equipment (fig.6). By appropriate programming and sample configuration in two zones (heat zone and cold zone) the compatible temperature gradient can be achieved. The costs of the test are relatively high. Because of cost problems broad application of the thermal shock tests by implementation of the lead - free technology in small enterprises seems to be limited.

3.4. Electrical power cycling

By power cycle tests are generated deformations caused by changes of the power from on to off conditions of real component (mainly resistor) soldered on the PCB. The power cycling may more accurately replicate field use conditions than temperature cycle testing, as well both temperature and power cycle tests can be applied simultaneously.

3.5. Mechanical cycling

The deformations and stresses shown on fig. 4 can be obtained by stretching, warping or bending of the PCB. Different schemes of mechanical load are shown on fig 7.

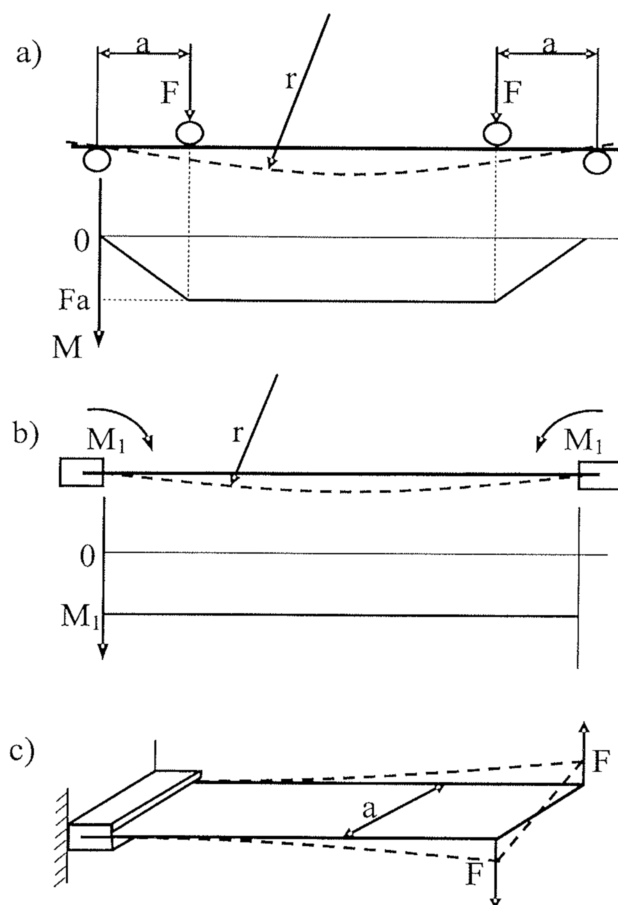


Figure 7: Charge systems of the PCB by mechanical tests; a) bending by force F , b) bending by moment M, c) warping with moment Fa

Very useful is the flexing system shown on the scheme 7b because of constant moment M and flexion radius r and uniform charge conditions for all components soldered on whole surface of the PCB. Preferably the PCB can be bent

cyclic in one or two directions. By mechanical cycling tests is induced the solder creep fatigue phenomena. The necessary test acceleration factor can be obtained by selection of appropriate strain range.

3.6. Mechanical fatigue test stand

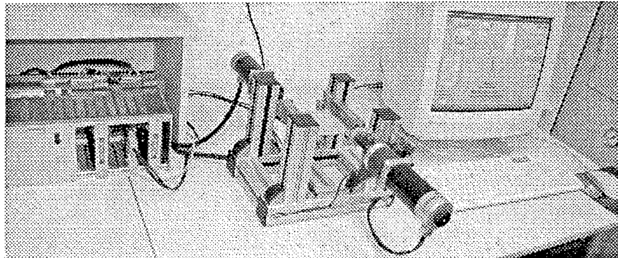


Figure 8: Mechanical fatigue test stand

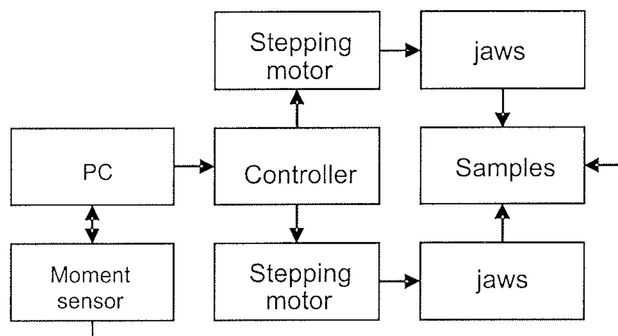


Figure 9: scheme of mechanical test stand

General view of laboratory stand for mechanical fatigue tests is shown on the fig.8. Block scheme is shown on fig.9. The stand consist of bending jaws, two servomotors, and motor controller.

The main parameters of mechanical cycling: bending velocity, time intervals t_1, t_2, t_3, t_4, bending angle α and bending moment M (fig.10) are controlled by PC.

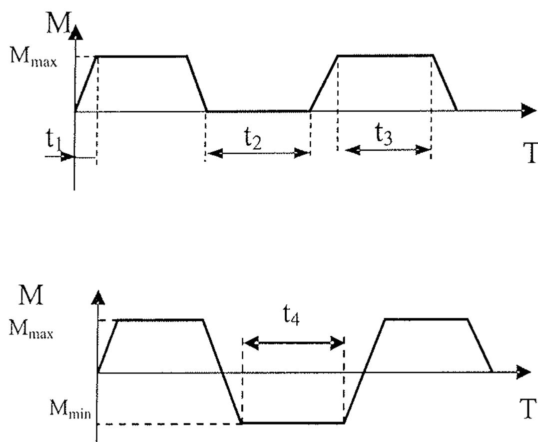


Figure 10: Mechanical testing schedule; a)one - side, b) two - side flexion

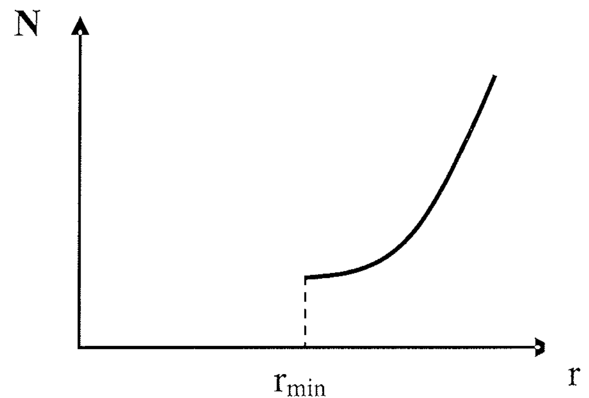
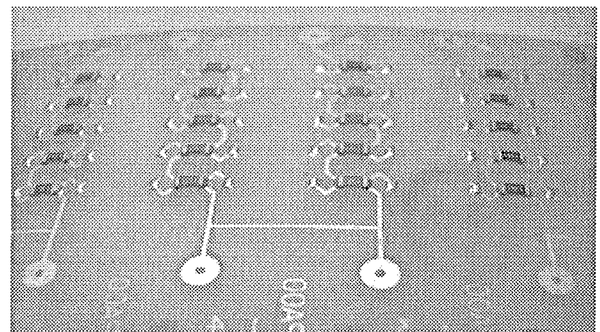


Figure 11: Number of cycles N to failure as a function of bending radius r (preliminary data for PbSn soldered 1206 resistor)

Preliminary tests, performed for SnPb eutectic solder, showed that mechanical bending cycling has in relation to thermal cycling following advantages:

- uniform charge of all components on the test board,
- large range of acceleration factor can be achieved by appropriate choice of the bending radius (fig.11),
- verification of materials and manufacturing process parameters relative test results can be achieved in short time,
- good accessibility of tested joints for verification and measurements (fig.12),
- low cost of testing equipment and necessary energy,
- environmental compatibility.



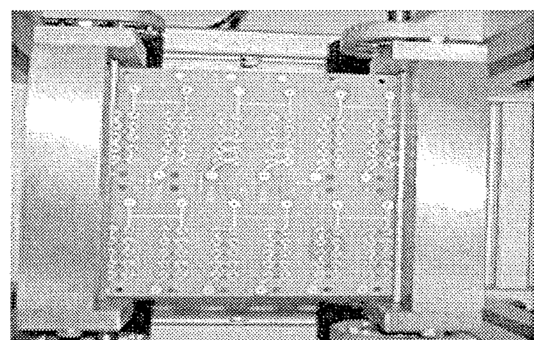


Figure 12: PCB sample fixed in the jaws

4. Required functions and failure criteria

Choice of required functions and parameters is very important for determining of the failure criteria and failure definition. In certain solutions the interconnections can be evaluated visually during the test, however precise definition of such failures and their detection during the tests is problematic. Application of electrical parameters (resistance, impedance, noise) as the failure criteria is more objective. The most important parameter is the value and stability of electrical conductance of all soldered joints. Good criterion is the stability of electrical resistance. During the tests performed in Warsaw University of Technology the resistance changes more than 10 moms were defined as failures /1/. The resistance increase 20% was also admitted as failure definition in IPC-9701.

5. Failures data collection and analysis

Failures of occurred during thermal shock and mechanical cycling are shown on fig.13a and 13b. By mechanical cycling smaller number of cycles is necessary.

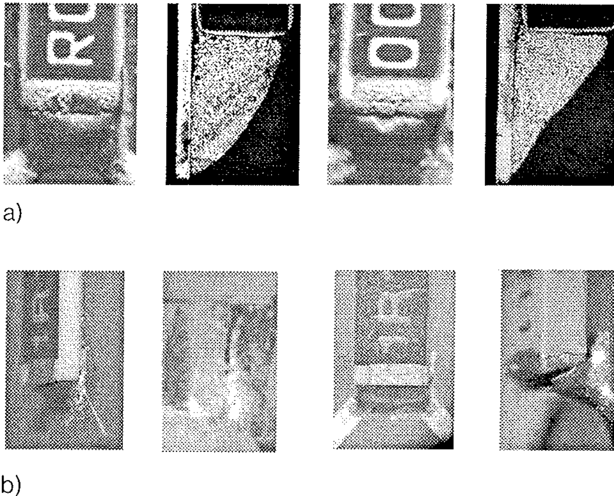


Figure 13: Failures of solder joints; a)after 2000 thermal shocks, b)after 100 mechanical cycles

Dependent of the results of the tests the failures data can be expressed in following forms;

- Absence or presence of failures
- Time to first failure
- Number of failures as time function
- Cumulative distribution function F(t)
- True reliability R(t) = 1 - F(t)
- Density function
- Mean time to failure (MTTF)
- Failure rate λ
- Graphical presentation
- Confidence intervals
- Statistical distribution (exponential, Weibull,..)

Some examples are shown on figures 14, 15 and 16.

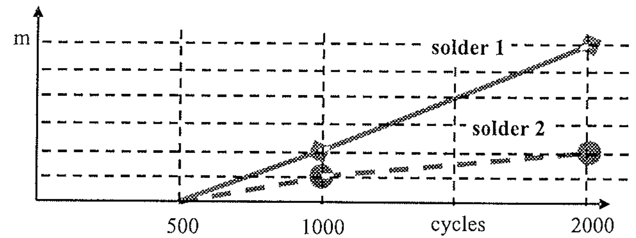


Figure 14: Number of failures m after thermal cycling of soldered joints for 400 joints

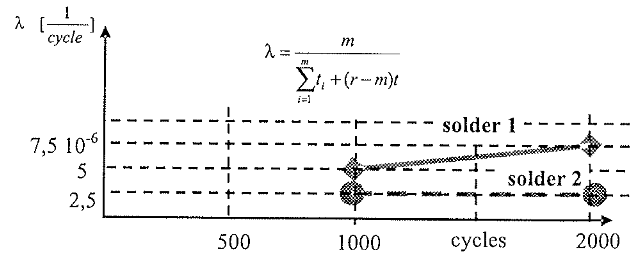


Figure 15: Failure rate λ calculated for the test sample 400 joints

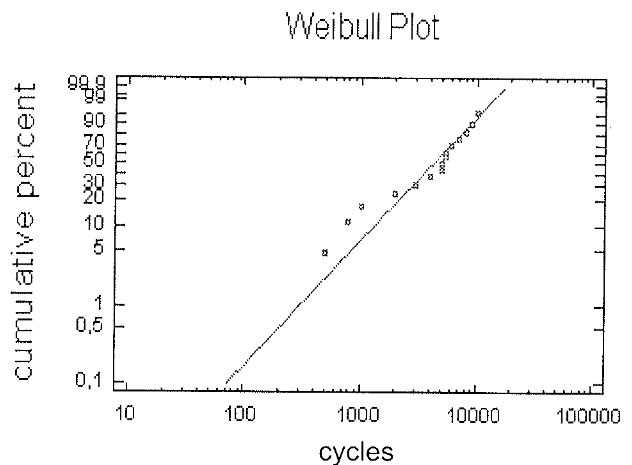


Figure 16: Presentation of failure data on Weibull plot

6. Conclusions

Reliability of soldered joints is the critical problem by implementation of lead - free technology. Up to date the reliability data of electronic products after removal of hazardous substances are unsatisfactory.

This paper showed preliminary results of investigations and analysis of thermal and mechanical cycling method for testing of solder joints. Preliminary test showed that applica-

tion of only mechanical cycling as routine verification by small producers of electronic equipment will be very useful, however further detailed investigations, comparison with thermal cycling and electrical cycling tests, determination the test parameters and analysis of obtained results for different solders are necessary.

Developed laboratory stand enables further investigations, concerning test life correlations for SnPb and lead free soldered joints achieved in accelerated tests realized by different methods, and determination of application area for mechanical cycling method.

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ADHESIVE JOINING OR LEAD-FREE SOLDERING?

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Key words: electrically conductive adhesive, lead-free solder, adhesive joint, soldered joint

Abstract: Low-cost tin-lead solders have been used as interconnecting and surface coating materials in electronics for many decades. These alloys have good electrical and mechanical properties, reasonably low melting point, and good reliability, but they are not nature-friendly. As a result of an effort to eliminate the use of lead-containing solders there have been started different regulation and legislation activities in many countries. Some of them are presented in this paper. There are two basic ways of no-lead replacement: lead-free solders and electrically conductive adhesives. Basic types of lead-free solders and electrically conductive adhesives are presented. Selected methods for testing of quality of soldered and adhesive joints are mentioned, and results of measurements of selected types of lead free solders and conductive adhesives are mentioned, too. It has been found that quality of soldered joints is higher than quality of adhesive ones.

Lepljenje ali spajkanje brez svinca?

Kjučne besede: električno prevodna lepila, spajka brez svinca, lepljen stik, spajkan stik

Izvleček: Cenene spajke na osnovi svinca uporabljamo v elektroniki za povezave in spajkanje že nekaj desetletij. Te zlitine imajo dobre električne in mehanske lastnosti, dokaj nizko temperaturo tališča, so zanesljive, vendar niso okolju prijazne. V mnogih državah so zaradi tega z uvedbo zakonskih uredb zaceli z odpravo uporabe spajk s svincem. Nekatere uredbe predstavimo v tem prispevku. V osnovi obstajata dva načina odprave spajk s svincem: uporaba spajk brez svinca in uporaba električno prevodnih lepil. V prispevku predstavimo obe alternativi skupaj z izbranimi metodami in rezultati preizkušanja kvalitete spajkanih in lepljenih stikov. Ugotovili smo, da je kvaliteta spajkanih stikov boljša od kvalitete lepljenih stikov.

1. Introduction

Driving forces affecting development of new joining materials in electronics are as follows:

- Performance of joints realized using these materials.
- Minimization of impact of joining materials and processes on environment.

Soldering technology based on the use of tin-lead solders has become the most frequent method of conductive joining in electronics. Soldered joints have good electrical and mechanical properties, high reliability, and the price of tin-lead solders is not too high.

On the other hand, lead has been involved among 17 chemicals, which impose the greatest threat to human health. Although the consumption of lead for production of solders for electrical and electronic applications is very low in comparison with consumption of this metal in some other applications (accumulators, paints), producers selling electronic products to the European Union and China, but also in many other countries, pay great effort to be compliant with WEEE/RoHS directives in order to stay on the Single Market. To be compliant means that they will have to convert their soldering technologies from tin-lead soldering to lead-free soldering or adhesive joining starting from July 1, 2006.

A step from tin-lead to lead-free soldering is not easy for manufacturers. It means that they have to convert from the very good known technology toward to the technology, which is connected with many question marks still yet, and which is under continuous development. Replacement of tin-lead soldering by adhesive joining is also connected with many problems: adhesive joining needs different surface finishes of the pads and leads than soldering, temperature profiles requested for soldering and for curing of adhesives are different, the price of adhesives is higher in comparison with the price of tin-lead solders.

There are many other questions connected with the no-lead replacement of tin-lead solders. Which of many lead-free solders will dominate, how the higher temperature of lead-free soldering will influence reliability of electronic components, which types of fluxes will be optimal, if properties of joints soldered by lead-free alloys will be equivalent to that of existing tin-lead solders, others.

Many questions must also be answered for adhesive technology, which has some advantages and some disadvantages in comparison with soldering. The main advantage

is the low curing temperature of adhesives, which is substantially lower in comparison with the soldering one. The curing temperature is usually in the range of 110 °C to 140 °C, the time of curing is usually 30 to 120 min. However, there are also adhesives, which are cured at the room temperature for a longer time, e.g. for 48 hours. Significant advantage of adhesives is a possibility to prepare them with isotropic or anisotropic electrical conductivity. Electrical conductivity of isotropically conductive adhesives is uniform in all directions just like electrical conductivity of solders. Anisotropically conductive adhesives have high conductivity in z direction and very low electrical conductivity in other directions. The main disadvantages of electrically conductive adhesives are their low endurance against moisture, lower thermomechanical endurance in comparison with solders, and high price, which mostly depends on the price of silver on the world market (conductive fillers in adhesive formulations provide silver usually, although gold, nickel, copper, carbon and palladium have also been tested in some formulations).

2. Regulation and legislation activities in different countries

There are many activities directed to ban lead from electronic production in different countries /1/.

- **EU**: Activities inside the EU are under the umbrella of the European Parliament and the Council of the European Union.
    - In 1998 the EU introduced a draft directive called the Waste from Electrical and Electronic Equipment Directive (WEEE).
    - In 2000 EU Commission has officially adopted the proposal as two separate but associated draft directives for submission to the European Parliament - WEEE and RoHS (Restriction on Hazardous Substances) /6, 7/.
    - In April 2001 the Environmental Committee of the European Parliament adopted a number of amendments and advanced their progress through the EU legislative process /14/.
    - In May 2001the European Parliament and the Council of the European Union have voted to adopt proposals to amend the date for the hazardous material ban in the WEEE/RoHS draft to 2006.
    - In 2002 the Council of Ministers of European countries has discussed and approved the WEEE/RoHS drafts including the target date 2006. The list of hazardous materials has been reviewed in 2003 and is opened. The Directive, prohibits the use of lead (and five other substances - mercury, cadmium, hexavalent chromium, polybrominated biphenyls, and certain polybrominated diphenyl ethers) in electronics starting from July 1, 2006 /5/.
    - Some European countries are paying great effort to apply these documents into practice as fast as possible, e.g. United Kingdom and Ireland /8, 9/.
- **USA**: There is no existing or pending federal restriction or prohibition on the use of lead in electronics components and productions. On the other hand there are many activities in this field on lower levels:
    - The U.S. Environmental Protection Agency (EPA), under the Resource Conservation and Recovery Act (RCRA) regulates the disposal of lead containing wastes /2/.
    - Manufacturers that process 100 or more pounds of lead are required to file annual Toxic Release Inventory (TRI) reports /3/.
    - The Occupational Safety and Health Administration (OSHA) regulate workers exposure to lead /4/.
    - Legislation focused on waste electronics is under development in many states.
- **Japan**: There are no known laws, pending or otherwise, in Japan, calling for reduction or elimination of lead in electronics. However, it has been proposed a recycling legislation in 1998. This legislation has called for reduction of the use of lead by 1/2 to the year 2000 and by 2/3 to the year 2005. There have also been approved Home Electronics Recycling Law (2001) and a law that requires the recycling of personal computers in (2003) /10/.
- **China**: There are no known laws in China, calling for reduction or elimination of lead in electronics, but such laws are under preparation /11/.
- **South Korea**: With respect the effort to be successful on the EU market, 340 companies representing 95 % of electronic industry have voluntary started to accept EU RoHS Directive. South Korea also enacted law making electronics manufacturers and importers responsible for recycling their products. /12/.

This short outline presents some selected activities only in the field of regulation and legislation related to restriction or elimination of lead in electrical and electronic products and production processes.

It is significant that many big producers use "green" production processes (e.g. Samsung Group has announced a "green" semiconductor product already in 2001, Nortel Networks is very active in this field in the Europe, Motorola and Lucent Technologies in USA, Matsushita (Panasonic) and Sony in Japan). There are also many initiatives coming from independent corporations and electronic industry organizations, such as Department of Trade and Industry (DTI) in the Europe, Japanese Institute of Electronic Packaging (JIEP), National Centre for Manufacturing Science (NCMS) and National Institute of Standards and Technology (NIST) in USA.

3. Criteria for selection of lead-free alloys and electrically conductive adhesives

The replacement of lead soldering by no-lead soldering of adhesive joining is not simple. At first, it has been necessary to appoint criteria for selection of proper materials. These criteria have been appointed with respect to material parameters and to technological parameters as well. The criteria make decision, if it is possible to use a lead-free alloy or electrically conductive adhesive as a substitution of tin-lead solder, possible.

3.1 Criteria resulted from basic material parameters

Materials used for conductive joining in electronics must have primarily high electrical conductivity, bond strength and high thermomechanical endurance. However, they must satisfy also other criteria.

These criteria /2/ comprises the liquidus temperature, pasty range, wettability, area of covering (the test is based on the measurement of coverage of copper test piece by solder), drossing (the test is based on the measurement of amount of oxide formed in air on a surface of molten solder after a fix duration at soldering temperature), TMF (lifetime at a given failure rate compared to that of (eutectic) Sn/37Pb, for a specific configuration of a board and solder joint), coefficient of thermal expansion, creep, yield strength and elongation. According to these criteria 79 alloys as candidates for substitution of tin-lead solders have been chosen /13/.

Criteria for selection of electrically conductive adhesives as a substitution of tin-lead solders are TMF, coefficient of thermal expansion, creep, yield strength and elongation.

3.2 Criteria resulted from basic technological parameters

Criteria resulted from basic technological parameters are related to possibility of transformation of contemporary soldering technology for tin-lead soldering to lead-free technology. These criteria are not related to adhesive joining.

The most significant criteria are as follows /13/:

- The melting temperature has to be similar to that of eutectic tin-lead solder. The reason of this request is evident. If the temperatures of tin-lead and lead-free soldering will not be too different, contemporary soldering equipment would be usable without significant changes. It would also not be necessary to increase temperature resistance of some electronic components.
- Narrow plastic range.
- Capability of being fabricated into contemporary physical forms of solder, such as wire, preforms, ribbon, spheres, powder, and paste. This condition is again related to the possibility of the use of contemporary soldering equipment without bigger changes.
- Adequate wetting properties and viscosity.
- Good wettability of leads and pads.
- Acceptably low dross formation when used in wave soldering. This is one of basic conditions for trouble-free wave soldering.
- For paste, adequate shelf life and performance.

4. Viable lead free alloys and electrically condutctive adhesives

4.1 Lead-Free Alloys

Many lead-free alloys, which satisfy criteria for selection mentioned above, have been investigated /15, 16/. However, with respect to the electrical, mechanical and other properties and especially with respect to the price of alloys, only few of them have been recommended for the practical use in common applications. Properties of the alloys are usually compared with the properties of eutectic 63Sn-37Pb solder or with 62Sn 36Pb 2Ag solder. Favorites differ from region to region.

In the Europe the consortium BRITE-EURAM has recommended the use of alloy 95.5Sn 3.8Ag 0.7Cu as the all-purpose solder. Other potential alloys are 96.5Sn 3.5Ag, 9.3Sn 0.7Cu, Sn Pb Bi and Sn Ag Sb.

In the U.S. the National Manufacturing Initiative (NEMI) has recommended alloy 99.3Sn 0.7Cu for wave soldering and alloys 96.5Sn 3.5Ag and 95.5Sn 3.9Ag 0.6Cu for reflow soldering. Other favorite alloys are 96.5Sn 3.5Ag 4.8Bi and 58Bi 42Sn.

In Japan the Japanese Electronic Industry Development Association (JEIDA) has recommended alloys 96.5Sn 3Ag 0.5Cu and 89Sn 8Zn 3Bi for wave soldering, medium and high temperature reflow and 42Sn 57Bi 1Ag for low temperature reflow /16, 17/.

4.2 Electrically conductive adhesives

Electrically conductive adhesives (ECA) are composites consisting of polymer insulating matrix (binder) and electrically conductive filler /18/. There are two basic types of ECAs: adhesives with isotropic electrical conductivity (ICAs) and adhesives with anisotropic electrical conductivity (ACAs, z-axis adhesives). ACAs are usually, in film or paste form, interposed between opposite surfaces which would be joined and application of heat and pressure causes conductive particles to be trapped between these surfaces. This way an adhesive joint is realized. ACAs are of two basic types: preprocessing anisotropic and postprocessing anisotropic /19/.

Both thermoplastic and thermosetting materials are used for adhesive matrix of ECA. The main advantage of ECAs

with thermoplastic matrix is easy rework or repair of adhesive joints, main disadvantage is low thermal resistance, the joints must not be heated near to the temperature of the glass transition of adhesive.

Thermosetting resins are cross-linked by curing. Shrink of adhesive caused by the cure reaction, causes compressive force inside the adhesive, which increases of electrical conductivity of a joint. Different materials are used as thermosetting adhesives: acrylic resins for applications under 100 °C, epoxy resins for temperatures to 200 °C, and polyimide and silicone resins for applications up to 300 °C. Rework or repair of adhesive joints fabricated of thermosetting adhesives is difficult /20/.

Fillers of ECAs are of different materials. Particles have different shapes. Typical material of filler is silver, but other materials such as gold, nickel, copper or palladium can also be used. Some ACAs have the particles with nonconductive core of glass or plastic material coated with a conductive layer.

The particles have different forms. They are usually spherical with diameter of 3 to 15 µm, sometimes flakes or grains are used. Particles of different forms can be combined, e.g. filler can consist of 40 % balls and 60 % flakes.

5. Measurements of basic electrical and mechanical properties of soldered and adhesive joints

Basic parameters, which are usually measured on soldered and adhesive joints, are: the electrical resistance, the tensile strength, the shear strength, and the thermomechanical resistance. The changes of these parameters after different types of climatic load are also investigated. As for the adhesive joints, their resistance against DC current or current pulses is also examined.

It has been found /21/ that the electrical resistance of the joints has substantially lower sensitivity to changes in joining material than nonlinearity of the current vs. voltage characteristics of the joint. The measurement of nonlinearity is significant for adhesive joints especially, where it makes a deeper analysis of changes in adhesive, caused by its aging, possible.

The theory of nonlinearity, based on an assumption that nonlinearity of the current vs. voltage characteristic is dominantly influenced by thermal movement of vacancies inside the material, has been derived by Zhigalsky /22/. It has been found that this theory, which has been derived for description of nonlinearity of thin metallic films, is also usable for description of nonlinearity of electrically conductive adhesives /23/. The relationship between the voltage U_3 of third harmonics and the temperature T can be described by the equation:

$$U_3 = \Psi \exp\left(-\frac{\Phi}{T}\right) \qquad (1)$$

Here Ψ and Φ depend on the joining material, on the thermal resistance of the joint, on the thickness of the layer between a lead of a component and a pad, on the thermal dilatation of the layer and on other parameters.

Other theory of nonlinearity is based on an assumption that nonlinearity of the current vs. voltage characteristic is dominantly caused by potential barriers inside the material /24/. According to this theory, the current I_T flowing through the material can be described by the equation:

$$I_T = 2N_T A \exp\left(-\frac{e\phi_I}{kT}\right)\left[\frac{eU}{kT} + \frac{e^3U^3}{3!(kT)^3} + \frac{e^5U^5}{5!(kT)^5} + \ldots\right] \qquad (2)$$

Here N_T ... total number of barriers, A ... material constant, e ... charge of an electron, ϕ_I ... high of the potential barrier, k ... Boltzman constant, T ... temperature, U ... voltage across the joint.

The measurement of the resistance of the joint is mostly carried out in four-point arrangement by the use of an ohmmeter for the measurement of low resistances.

Different types of equipment are used for the measurement of nonlinearity. One possible arrangement of such equipment, based on evaluation of inter-modulation distortion generated by nonlinearity of a measured component, is shown in Fig. 1.

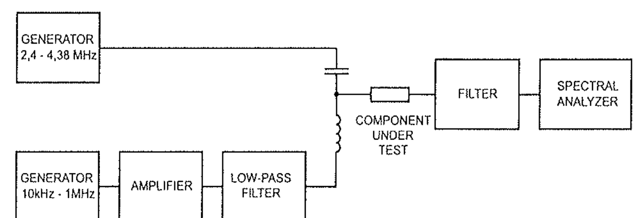

Fig. 1 Schematic diagram of equipment for measurement of nonlinearity of current vs. voltage characteristic

Mechanical properties of soldered and adhesive joints, usually their tensile strength and shear strength, are examined by a pull off test of a component mounted on a testboard using soldering or adhesive joining. Different types of breakers are used for these measurements.

Thermomechanical fatigue is investigated, too.

6. Experiments

Adhesive and soldered joints have been realized by assembly of SMT resistors of the type 1206 with "zero" resistance (jumpers) on a testing PCB (FR4, Cu). The pads have been cleaned by a standard way; no additional sur-

face finish has been used. Seven resistors have been mounted on one board. The testing board (see Fig. 2) makes two point or four-point measurements of the resistances of the joints possible.

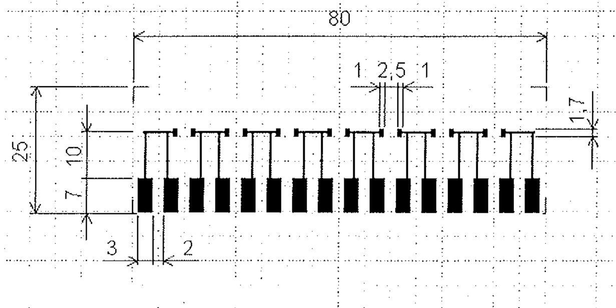

Fig. 2 Testing board (dimensions are in mm)

Adhesive joints have been realized using three one component and three two-component types of adhesives (epoxy resin, Ag filler). The difference among the adhesives has also been in types of particles of the filler (balls, flakes, combination balls/flakes 80/20).

Lead-free solders have been of the types 96.5Sn 3.5Ag and 95Sn 5Ag.

Properties of adhesive joints and the joints soldered with no-lead solder have been compared with the properties of the joints soldered with the solder 62Sn-36Pb-2Ag.

Climatic load has been realized at a climatic chamber. Three types of climatic load have been used: aging at the temperature of 120 °C, aging at the temperature of 80 °C and the humidity of 80 % RH, aging at the humidity of 100 % RH. The time of aging has been 300, 500, 700 and 1000 hours.

Influence of a static mechanical load has also been investigated: the test boards assembled with the "zero" resistors using soldering or adhesive joining have been mounted in a fixture, where they have been compassed. The compassed testing board with the mounted resistors is schematically shown in Fig. 3. Dimensions of the resistor are marked in Fig 4.

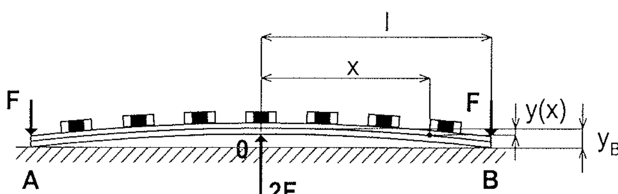

Fig. 3 Compassed testing board with the assembled resistors

The joints have been loaded with different load according to their location with regard to the midpoint of the board. It has been derived that the shear force F_S and the shear stress d_S in the soldered or adhesive joints of the resistor

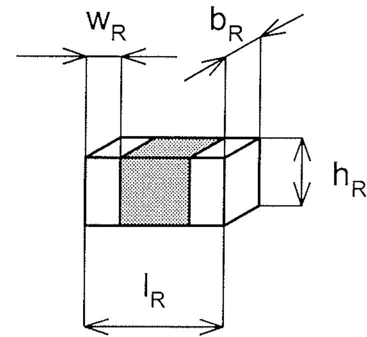

Fig. 4 Dimensions of the resistor

located in the middle of the testing board can be calculated according to the equations:

$$F_S = \frac{E_R S_J \Delta l_R}{l_R} \tag{3}$$

$$\delta_S = \frac{F_S}{S_J} \tag{4}$$

Here E_R ... Young's modulus of elasticity of the body of the resistor, S_J ... contact area of the resistor on the pad, Δl_R ... elongation of the resistor after compassing of the board, l_R ... length of the resistor. The calculated value of the shear force in joints of the resistor located in the middle of the test board is 52.5 N.

Tensile force F_T and tensile stress τ in the joints of the middle resistor can be described by the equations:

$$F_T = \frac{3 E_R J_{ZR}}{l_R^3} y_R \tag{5}$$

$$\tau = \frac{F_T}{S_J} \tag{6}$$

Where J_{ZR} ... cross section module of a body of the resistor, y_R ... deflection of the end points of the resistor against its middle point.

The calculated value of F_T is 2.42 N. The comparison of the calculated shear and tensile forces influencing the soldered or adhesive joints of the middle resistor shows that the shear force dominates. Derivation of equations (3) ... (6) has been presented elsewhere /25/. Similar equations like (3) ... (6) can be derived for every resistor on the board.

7. Results of experiments

Changes of properties of soldered and adhesive joints caused by climatic ageing have been published elsewhere /26/. An example of results of climatic aging of one type of soldered joints is shown in Fig. 5.

Properties of mechanically loaded joints have been published in /21/. An example of changes of the resistance and nonlinearity of adhesive joints loaded with the static mechanical load and aged at the temperature of 120 °C, is

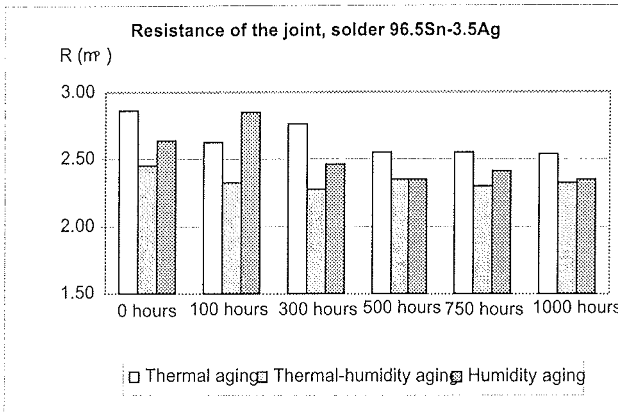

Fig. 5 Climatic aging of soldered joints

shown in Fig. 6 and Fig. 7. Pay attention to changes of the resistance and nonlinearity of the joints. Whereas the changes of the resistance are in the range of 4 to 35 mΩ, the changes of nonlinearity are in the range of 10^{-7} to 2.10^{-4}. Nonlinearity is substantially more sensitive to the changes in material than the resistance of the joint.

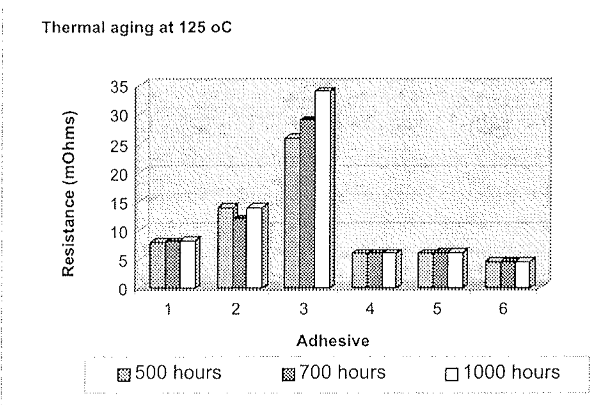

Fig. 6 Resistance of adhesive joints fabricated of 6 different types of adhesives with epoxy resin matrix and Ag filler (1 ... 3: two-component adhesives, 4 ... 6: one-component adhesives). The joints have been loaded with the static mechanical load (F_S = 52.5 N, F_T = 2.42 N) and aged at the temperature of 125 °C.

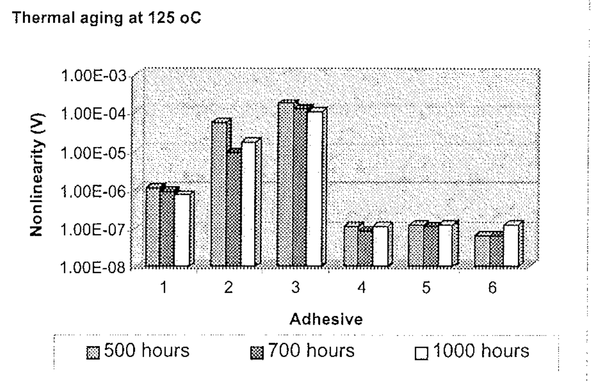

Fig. 7 Nonlinearity of adhesive joints fabricated of 6 different types of adhesives with epoxy resin matrix and Ag filler (1 ... 3: two-component adhesives, 4 ... 6:one-component adhesives). The joints have been loaded with the static mechanical load (F_S = 52.5 N, F_T = 2.42 N) and aged at the temperature of 125 °C.

Results of experiments, focused on investigation of influence of current pulses on properties of adhesive joints, have been presented in /27/.

Comprehensive results of our experiments with 6 types of electrically conductive adhesives and two types of lead-free solders are presented in Tab. 1 to Tab.4. Incomplete results have also been published in /21, 25, 27/.

8. Conclusions

Situation in the field of replacement of tin-lead solders by nature-friendly joining materials such as no-lead solders and

Tab. 1 The resistances of the joints

Joining material	Resistances of the joints
2-component adhesives	4 to 15 mΩ
1-component adhesives	8 to 30 mΩ
Lead-free solder	1 to 3 mΩ
Tin-lead eutectic solder	1 to 2 mΩ

Tab. 2 Changes of the resistances of the joints after the climatic load (1000 hours)

Joining material	Thermal aging (125 °C)	Thermal-humidity aging (80 °C/80 % RH)	Humidity aging (100 % RH)
2-component adhesives	Low (5 to 10 %)	Middle (20 to 40 %)	High (50 to 100 %)
1-component adhesives	Low (5 to 20 %)	High (50 to 100 %)	High (50 to 100 %)
Lead-free solder	Lower than 5 %	Lower than 5 %	Lower than 5 %
Tin-lead eutectic solder	Lower than 5 %	Lower than 5 %	Lower than 5 %

conductive adhesives has been discussed. The most promising lead-free alloys have been mentioned. Methods of investigation of properties of soldered and adhesive joints have been presented together with examples of some results.

Tab. 3 Nonlinearity of the joints

Joining material	Nonlinearity of the joints
2-component adhesives	0.06 to 10 μV
1-component adhesives	0.8 to100 μV
Lead-free solder	~ 0.1 μV
Tin-lead eutectic solder	~ 0.1 μV

The values presented in tables have been found for the soldered and adhesive joints fabricated by assembly of the resistors with "zero" resistance of the type 1206 on the testing PCBs. Other results can be found by the use of other types of components.

It has been found that the investigated electrical, as well as mechanical, properties of the adhesive joints are worse than the properties of the soldered joints. The adhesive joints are also less resistant to the climatic load than the soldered ones.

Such results have been assumed. In general, metal alloys are more resistant to climatic aging than composites based on epoxy resin.

It is possible to claim that quality of the joints soldered by no-lead and tin-lead solders is comparable. Quality of the adhesive joints is lower. On the other hand, electrically conductive adhesives are unsubstitutable in such applications, where it is necessary to create a conductive joint without a heat shock. Especially ACAs have promising prospective in electronics packaging.

9. Acknowledgments

The work has been supported by the research project MSM6840770021 "Diagnostics of Materials".

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Tab. 4 Changes of nonlinearity of the joints after the climatic load (1000 hours)

Joining material	Thermal aging (125 °C)	Thermal-humidity aging (80 °C/80 % RH)	Humidity aging (100 % RH)
2-component adhesives	Middle (20 to 50 %)	High (50 to 250 %)	Very high (>250 %)
1-component adhesives	High (50 to 250 %)	Very high (>250 %)	High (50 to 250 %)
Lead-free solder	Low (5 to 20 %)	Very low (<5 %)	Very low (<5 %)
Tin-lead eutectic solder	Very low (<5 %)	Very low (<5 %)	Very low (<5 %)

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DIRECTIVES WEEE/ROHS: FROM EARLY INFORMATION TO THE SLOVENIAN IMPLEMENTATION

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Key words: WEEE, RoHS, hazardous substances, collective reasearch projects

Abstract: EU Directives: 2002/95/EC on the restriction of use of certain hazardous substances in electrical and electronic eqiupment (RoHS) and 2002/96/EC on waste of the electrical and electronic equipment (WEEE) have a major influence on technology and market conditions to which companies in electrical and electronic engineering industry is faced to.

Process leading to substantial changes in companies imposed by directives: from collecting early information at the stage when draft directive was prepared, providing information and awareness raising campaign with special view on SME, following with exchange of information and best practice between associations on EU level and establishing working groups RoHS and WEEE, cooperation with authorities in Slovenia and also participation in collective research project in 6.FP is described.

Direktivi WEEE/RoHS: od začetne informacije do Slovenske implementacije

Kjučne besede: WEEE, RoHS, nevarne snovi, skupni raziskovalni projekti

Izvleček: Direktivi EU 2002/95/EC glede omejitve uporabe določenih nevarnih snovi v električni in elektronski opremi (RoHS) in 2002/96/EC glede odpadne električne in elektronske opreme (WEEE) imata velik vpliv na tehnologijo in razmere na trgu, s katerimi se soočajo podjetja, ki delujejo na področju elektronike.

V prispevku opisujem proces, ki je pripeljal do velikih sprememb v podjetjih, ki jih direktive prizadevajo: od zbiranja podatkov v času, ko sta direktivi bili še v poskusni fazi, ko sta podajali osnovne informacije in dvigovali raven zavesti v podjetjih, preko izmenjave informacij in najboljše prakse med združbami na nivoju Evropske skupnosti z uvedbo delovnih skupin RoHS in WEEE in nato sodelovanje s Slovenskimi oblastmi in soudeležbo v skupnem raziskovalnem projektu v okviru 6.FP

1. Introduction

Environment protection and sustainable development in manufacturing industry has been in EU of the major concern for a long time. Not only pollution through production processes but also other aspects like water consumption in production, energy efficiency of product in its regular use has led to changes in EU policies and subsequently in regulatory framework. Dynamic emergence of new electrical and electronic products in broad area of use in every days life has brought to a large amount of used products which became waste at the end of their useful life. Large stream of electrical and electronic waste and the presence of dangerous substances in this equipment which demand proper treatment has bought to an EU legislative initiative for a WEEE and RoHS directive.

Slovenia has a strong electrical and electronics industry with final as well as intermediate products which are exported traditionally to EU market and through this inevitably influenced by the processes mentioned. The WEEE/RoHS legislative process on EU level as well as somewhat simultaneous efforts of the EU industry and research institutions have been closely followed by Electronic and Electrical Engineering Association (EEEA) of Chamber of Commerce and Industry (CCI) Slovenia from 1999.

The WEEE legislative process has been considered as a case of multiple impact to our industry: collecting early information on future legislation, collecting and dissemination of information on research efforts on potential new substances to replace the banned ones in EE equipment and also aspects on design of new products, taking into account the WEEE directive.

2. WEEE & RoHS Awareness raising and implementation process

2.1. Collecting early information: EU legislative initiative and reaction of industry

After having conducted a study on specific streams of waste, which has shown substantial growth of the electrical and electronic waste stream in the near future and actual consequences of often improper treatment of such waste - from collection to the disposal phase, legislative process for WEEE directive has included the hazardous substances. The importance of the simultaneous reduction of hazardous substances in EEE has been one of the reason that this area also was initially included in WEEE. The initial WEEE legislative initiative has somewhat boosted the intensity of research and industry efforts in searching for new substances. One of the first contact with information of the research results on lead-free solder and lead-free soldering problems has been for EEEA in Productronica Fair in Munich 2000. Simultaneously the legislative process in EU was followed by EEEA through the work of task force for the WEEE at ORGALIME , Liaison group of the European mechanical, electrical, electronic and metalworking industries as one of the strongest EU industry federation. At that time, in first quarter of 2000, the process was aiming to reach the Commission proposal of WEEE to the Council and the Parliament. Details on producer responsibilities regarding financing, cost and collection, historical waste and collection targets were discussed. It was proposed by the industry that design and substances issues should be legislated under article 95 of the EU Treaty as not to distort internal market, which resulted later to the separate RoHS directive. Contacts and discussions had been held with Japan and American industry representatives in EU regarding ban of hazardous substances, where some Japanese companies have established ambitious plan to completely phase out lead from their products by 2002.

At this time the discussions on the possibility of developing "new approach" framework directive on environmental requirements which could include provisions on eco-design, processing, energy efficiency and maybe the use of certain substances and materials in products; the idea has than led to the today`s already adopted "eco design of energy using products (EuP) directive".

2.2. EE Forum 2001 in Ljubljana: Information and awareness raising events for electrical and electronic industry

Although companies which have contacts with providers of certain materials and substances have already had some knowledge on the lead- free efforts, the need for emidiate start of providing information both on technology issues as well as on future legislative aspects and obligations for producers (suppliers of the EE equipment) was considered priority. The opportunity for an event promoting the issues on WEEE and RoHS has been taken in October 2001. A series of round table discussions under the title "EE Forum" during the fair "Sodobna elektronika 2001" in Ljubljana were organised by EEEA of CCI with the support of "Ljubljanski sejem". The WEEE and RoHS issues as central theme were discussed with experts from industry and representatives from responsible ministry. Specifically, the discussion was focused on the experience in the applying lead-free technology so far in industry, further to some outstanding issues and also experiences in the collection and recycling schemes of household and some other electronic equipment already existing in some EU member states. Similar EE Forum was organised in October 2003 in the framework of the same fair, where discussion was already focused to the implementation of already adopted Directives WEEE and RoHS.

At this time in 2003 a large scale discussions on WEEE and RoHS implementation issues on national level with companies, industry associations, national administration as well as in industry federations the EU level has taken place. The aim was to prepare guidelines for the WEEE implementation and take back system according to the provisions in WEEE and at the same time for its efficient and rationale functioning. Also RoHS issues regarding exemptions and other outstanding issues essential for economic operators were analysed. EEEA has acted as an observer in the process and while, gathering information, identifying at the same time the stakeholders and its role.

2.3. Establishment of Working Group WEEE and RoHS in CCI: Awareness raising, sharing good practices and transposition process in RS

In 2003 collection of information from Task Force (TF) WEEE and RoHS at Orgalime was intensified by EEEA in parallel with the ongoing process in EU which aim was to provide guidelines on understanding of specific provisions in both directives and their implementation on the industry level. Explanatory fiches were developed by task force at Orgalime engaging numerous experts from industry and association professionals in the Member states. Cooperation with European sector committees representing household appliances producers (CECED) and ICT industry (EICTA) and others was established. The issues considered were for example: the scope of the directives and the definition of producer (which are the same in both directives), further the specific issues in RoHS like maximum concentration values of restricted substances, exemptions to RoHS and other. The examination of the exemptions listed in the annex of the RoHS directive were analysed for which the procedure through TAC (technical adaptation committee) was foreseen in the directive itself and provided for adaptation to scientific and technical progress in the field of alternatives to hazardous substances. Several

proposals for new exemptions were presented and than presented to the Commission.

The awareness raising campaign on implementation process by EEEA in Slovenia has started with information leaflets to member companies in second half of the 2003 with seminars which finally led to the establishment of working group (WG) WEEE and RoHS at CCI. Companies from EE industry, distributors and retailers, importers have joined WG where also researchers from institutes (IJS) and the officials from responsible of the Ministry for environment, spatial planning and energy (MOPE) took part. The aims of the WG WEEE and ROHS in CCI were: exchange of information coming from above mentioned sources, than follow up of the explanatory fishes, discussion of proposed guidelines for implementation and also practical issues regarding preparation to compliance with directives. On top of that, close cooperation in the transposition and implementation process of both directives with authorities in Slovenia was established.

Several WG meetings took place in 2004 from March onwards, resulting to discussions on the draft proposals for WEEE and RoHS in September 2004, where positions of the industry and other economic operators where formed and presented to legislators.

Two meetings between economic operators and ministry officials discussing the outstanding implementation issues on WEEE were organised by the CCI. Two further meetings in CCI of WG WEEE and RoHS with MOPE discussing RoHS implementation have lead to important changes in the initial draft of the ministerial decree regarding RoHS compliance assessment and surveillance. After transfer the responsibility for RoHS to the National Chemicals Bureau good cooperation was established.

This has resulted into regular exchange of information between Bureau and WG in periodical meetings, which are organised to follow up the developments regarding practical implementation, new developments on EU level regarding annexes to RoHS.

2.4. Participation in GrenRose project and further activities of WG WEEE/Rohs in Slovenia

The EEEA of CCI took part in 6.FP collaborative research multinational project GreenRose, where EEEA has - as an industrial association of SMEs the role to disseminate the knowledge and support to implement results of the research efforts in technology and processes with substitutions to hazardous substances among its SME members. Good cooperation is established with IJS both in the promotion of RoHS themes as well as in the work of WG WEEE RoHS.

While the date of the ban 1. 7. 2006 for products containing hazardous substances for the placement on the market is approaching quickly, the practical issues regarding the changes to new products without hazardous substances in supply chain between companies are still to be solved. After officially established maximum concentration values of the banned substances by EU Commission lately, the conformity assessment issues with RoHS provisions are in the focus of interest and also the proposals for new exemptions. In many cases the proposals for exemptions are based on practical issues (specific ICT components which are in use but will not be available in lead free technology) and- if not adopted - could harm competitiveness of important segment of industrial SME. One of the most important issue in national level is to build up the guidelines for B2B communication in supply chain on the components and materials which are to comply with RoHS provisions.

Environmental friendly product design and substitution of hazardous substances in electronic and electrical equipment is one of the main purpose of the lately adopted directive establishing framework for eco-design of energy using products (EuP) promoting life cycle approach in designing new products and represent a step towards integrated product policy. EEEA of CCI is already actively involved in promoting methodology for product design within the EU project "Awareness raising campaign for electrical and electronic SME " with Fraunhofer IZM Institut Berlin. A successful workshop with large number of participants was organised in CCI in Ljubljana in May 2005.

3. Conclusion

Implementation of EU legislation which has a strong influence on technology and production processes as well as directly to the market access for SME in industry, is demanding task for industrial associations.

Having the opportunity to follow the WEEE and RoHS legislative process and consequently its technology implications: in research area, on technology, production processes and on competitiveness of SME, has enabled EEEA to understand the mechanism of the whole process, role of stakeholders in it, and above all the role of associations and tasks to be accomplished. Understanding of the EU legislation process and active participation in it, is essential for building association competence in the implementation phase on the member state level as well as supporting SMEs in solving problems and other practical issues.

Summarising the stages in the process with the relative tasks and activities the following points could be considered as important and/essential:

- collecting early information on legislative initiatives on EU Commission level (possible participation in "regulatory Impact assessment procedure " is crucial)
- EU federations are important source of information, giving opportunity to share the views and positions, also to actively influence the process both in preparing positions to proposals within Commission service activities as well as in the parliamentary process and

other decision making levels or bodies (EU Council, COREPER...) Active response and expert support from companies is also important for credible participation in the process.

- Gathering "early information" and exchange of information though the adoption process of directives on EU level is important for the competence needed in the implementation phase on national level later on.
- Cooperation with national authorities in both phases (EU adoption process and implementation) should be based on partnership and shared responsibility.
- building - up competence is connected with acquisition of specific knowledge (e.g. like in the case of RoHS where new research activities are essential part of the implementation), at the same time the exchange of good practices, bringing together all relevant stakeholders are essential in such cases where new technology is involved.

New developments in EU industrial policy promoted by EU Commission is strongly connected with research and technology development in much faster rate that before. Sustainable development policy is of highest importance and means for industry searching for new products, where environmental issues are essential. This is proven by many regulatory concepts, one of them is framework directive known as "eco_design of energy using products" which is providing new challenges for electrical and electronics industry, perhaps also on a global scale.

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RAZUMNI HIŠNI POMOČNIK

Uporaba teorije o razumnih agentih za izvedbo inteligentne hišne naprave

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Kjučne besede: modalna logika, večmodalna logika, usmerjeno vedênje, agent, razumni agent, BDI-model, BDI arhitektura, praktično razmišljanje, ciljna usmerjenost, ciljno usmerjeni agenti, inteligentni hišni pomočnik, povezane naprave, porazdeljeni sistemi, interoperabilnost, večagentni sistemi.

Izvleček: Vsebina članka temelji na teoriji in izvedbi razumnega agenta in njeni možni uporabi na področju inteligentnih hišnih naprav. Najprej opisujemo nekaj glavnih značilnosti agentov kot samostojnih računalniških sistemov, agentnih skupnosti in komunikacijo med agenti, ter nekatere glavne motive za uporabo te tehnologije na področju inteligentnih hišnih naprav. V nadaljevanju povzemamo teorijo o namenskem ali usmerjenem vedęnju in modalno logiko kot primerno orodje za opis miselnih stanj agentov. Iz te logike izhaja večmodalna, BDI-logika, ki predstavlja osnovni formalizem za obravnavo BDI-modela razumnega agenta. Jedro članka je posvečeno razumnim agentom, ki so zgrajeni na osnovi BDI-modela, to je modela prepričanja, želje in namena (*BDI* - *B*elief, *D*esire, *I*ntention). Nato podajamo kratek pregled metodologij in razvojnih orodij za načrtovanje agentov in agentih sistemov. Posebej predstavljamo razvojni orodji JADE kot hrbtenični sistem agente skupnosti in Jadex kot stroj za razmišljanje, ki temelji na teoriji BDI-modela. Na koncu opisujemo še možno izvedbo razumnega hišnega pomočnika (RHP) in njegov posebni primerek razumnega pomočnika pranja (RPP). Sistem je izveden kot agentna skupnost, sestavljena iz procesnega agenta, ki skrbi za izvajanje ciljnega hišnega procesa (recimo RPP), ter njegovih agentnih pomočnikov - nadzorovanih agentov, ki opravljajo posamezna opravila v okviru ciljnega procesa - recimo pranja perila. V članku želimo pokazati, da lahko samostojne in povezane hišne naprave obravnavamo kot večagentne sisteme.

Intelligent Home Assistant

Theory of Rational Agent Application for Intelligent Home Appliance Implementation

Key words: modal logic, multimodal logic, intentional attitude, agent, rational agent, BDI model, BDI architecture, practical reasoning, goal oriented agents, intelligent home assistant, connected appliances, distributed systems, interoperability, multiagent systems.

Abstract: This paper focuses on the theory and implementation of rational agents, and their possible application in the area of intelligent home appliances. We firstly describe some essential features of agents as autonomous computer systems, agent societies and inter-agent communication, and also some ground reasons to use this technology in the area of intelligent home appliances. Then, we present a short overview of intentional notion and modal logic, used as an appropriate formalization of the agent's mental state description. A derivation of this logic is multi-modal BDI logic which basically formalizes the description of the BDI model of rational agents. The central part of our article discusses rational agents based on the BDI model - the model of *B*elief, *D*esire, and *I*ntention. We continue with a short description of agent design methodologies and development tools. A special attention is paid to JADE, an agent development tool, which is applied as the middleware layer for agent society, and Jadex serving as a BDI reasoning engine. In the final part, our paper reveals a possible application of the Rational Home Assistant, and the Rational Washing Assistant as a special instance. The system is implemented as agent society, and uses a processing agent for performing the target home process, and his assistants - supervised agents that perform different task of the target process, such as laundry washing. In the conclusion, we argue that the autonomous and connected appliances can be treated as multi-agent systems.

1. Uvod

Agentni sistemi in tehnologije spadajo na področje, ki bo po nekaterih virih pomembno vplivalo na razvoj naslednjih računalniških generacij. Postajajo popularni za reševanje širokega področja kompleksnih problemov ali za nadzor kompleksnih sistemov, porazdeljenih sistemov, sistemov s spremenljivim okoljem, sistemov, kjer se programska oprema integrira v izvajalnem času, in podobno. V Gorenju menimo, da je to zelo obetavna in primerna tehnologija bodočnosti za načrtovanje povezanih naprav in porazdeljenih sistemov, primernih za realizacijo inteligentnega doma. V našem primeru gre za naprave bele tehnike, kot so pralni stroj, sušilec perila, hladilnik, zamrzovalnik, kuhalnik in pečica. Te naprave postajajo s pomočjo elektronskih sklopov, ki so zasnovani z novimi visokointegriranimi polprevodniškimi tehnologijami, in vgrajenimi zmogljivimi mikrokrmilniki vse bolj učinkovite. Takšna strojna oprema pomeni temelj za uvedbo programskih rešitev, ki zahtevajo visoko stopnjo zmogljivosti. V aparate bele tehnike bomo kmalu pričeli vgrajevati upravljalno-krmilne enote, ki bodo zasnovane tudi na 32-bitnih arhitekturah RISC in to z močno in aplikaciji primerno periferijo. Tako bomo razvili naprave z visokim nivojem inteligence, medsebojno pa jih bomo povezali v inteligentne sisteme povezanih hišnih aparatov. Prepričani smo, da je omenjena agentna tehnologija povsem primerna in perspektivna za takšne naloge. Najbolj nas zanima, kako z danimi računalniškimi tehnologijami doseči *inteligentnost naprav* in kako v sistemih *povezanih naprav* zagotoviti *interoperabilnost*.

Ukvarjali se bomo torej z določenim razredom računalniških sistemov, ki jih poznamo kot *agente* in jih lahko še natančneje opredelimo kot razumne agente. O računalniških agentih govorimo zato, ker lahko izvajajo *neodvisna ali avtonomna dejanja*, s katerimi dosegajo svoje cilje, za katere smo jih načrtovali. Grobo rečeno, sposobni so se odločati sami zase o tem, kaj naj napravijo v določeni situaciji. Imenujemo jih *razumni agenti*, ker se lahko *dobro (razumno) odločajo* o tem, kaj bodo storili. Izbirajo vedno najboljša možna dejanja.

Danes že lahko srečamo razumne agente na mnogih področjih in v mnogih aplikacijah. Zelo znana je Nasina misija *'Deep Space'* (DS1) /McBurney - 2005/. Agentna tehnologija je na primer čedalje bolj uporabna v elektronskem poslovanju preko interneta, pri upravljanju in nadzoru zračnega prometa, v telekomunikacijskih omrežjih, poslovnih procesih in medicinskih storitvah /Rao - 1995/, /Wooldridge - 1998/, /McBurney - 2005/. Zelo znan je (agentni) sistem za nadzor zračnega prometa OASIS na letališču v Sydneyu /Rao - 1995/.

Za preučevanje agentno usmerjenih sistemov se pojavljajo številni različni pristopi -/Bratman, 1988/, /Doyle, 1992/, /Rao in Georgeff, 1992/, /Shoham, 1993/. Zelo znana arhitektura za izvedbo razumnega agenta je BDI-arhitektura, ki vsebuje miselna vedęnja, kot so prepričanje, želja in namen (Belief, Desire, Intention). Ta vedênja predstavljajo agentove informacijsko in motivacijsko komponento ter komponento preudarjanja. Miselna vedênja določajo obnašanje sistema in lahko postanejo kritična, kadar hočemo doseči ustrezni in optimalni učinek sistema, če pri tem sistemski viri omejujejo proces preudarjanja /Bratman, 1987; Kinny in Georgeff, 1991/.

Za formalizacijo agentov se pojavljajo različni logični okviri. S pomočjo ustrezne logike lahko predstavimo lastnosti razumnih BDI-agentov in razmišljamo o njih na jasen, nedvoumen in dobro definiran način. Najbolj znana logična formalizma za obravnavo razumnih agentov sta logika KARO /Meyer - 2005/ in LORA, ki sta jo razvila Anand Rao in Georgeff v /Rao - 1991/ in /Rao - 1992/. KARO je kratica za Knowledge, Actions, Results in Opportunities (znanje, dejanja, rezultati, priložnosti), LORA pa za: Logics Of Rational Agents (logika o razumnih agentih).

Agent je računalniški sistem, ki je sposoben opraviti prilagodljiva in avtonomna dejanja v dinamičnem, nepredvidljivem in odprtem okolju. Agentne tehnologije so naravne razširitve obstoječih komponentno zasnovanih pristopov in imajo potencial, da bodo v veliki meri vplivale na življenje in delo vseh nas. Temu ustrezno je to področje eno najbolj dinamičnih in vznemirljivih v današnji računalniški znanosti /Luck - 2003/.

Računalniški agenti so nameščeni v stalno spreminjajočem se okolju /Wooldridge - 1997/. Agenti zaznavajo okolje. Imajo samo delno, mogoče napačno informacijo o okolju in so sposobni izvajati omejene napovedi o tem, kaj bo v prihodnosti veljalo. Lahko delujejo na okolje zato, da ga spremenijo, vendar imajo v najboljšem primeru samo delni nadzor nad rezultati svojih dejanj. Koncept takšnega agenta je prikazan na sliki 1.

Slika 1: Agent in njegovo okolje.

Agent mora mogoče izvajati nasprotujoče si naloge. Ima na voljo več različnih odločitev. Od njega zahtevamo, da se odloča pravočasno in da se zna pravočasno odzvati na okolje - deluje v realnem času. Poznamo štiri ključne lastnosti agentov, ki delujejo v večagentnem okolju. To so: avtonomnost, socialnost, odzivnost in usmerjeno delovanje. Razumnim agentom, ki delujejo v sodobnih okoljih, običajno pripisujemo še naslednje lastnosti: mobilnost, verodostojnost, dobronamernost, razumnost in prilagodljivost (učenje). Te lastnosti opredeljujejo razumne agente kot inteligentne sisteme. Pri načrtovanju večagentnih sistemov se običajno ukvarjamo z agentnimi sistemi na dveh nivojih. Na *mikro nivoju* se ukvarjamo z vprašanji, kako načrtujemo agente z zgornjimi lastnostmi. To je področje arhitekture razumnih agentov. Na *makro nivoju* pa obravnavamo področje skupnosti agentov. To je področje porazdeljene umetne inteligence. Ti dve področji sta med seboj tesno povezani.

Članek je zasnovan tako, da v drugem poglavju pokaže uporabnost modalne logike v teoriji vedênja. Tretje poglavje je posvečeno razumnim agentom in njihovi BDI-arhitekturi. V četrtem poglavju predstavimo orodja za načrtovanje agentov in njihovih skupnosti, v petem pa razvijemo idejo o inteligentnem hišnem pomočniku. Šesto poglavje sklene naš prispevek.

2. Teorija vedenja in modalna logika

Zgoraj navedene lastnosti agentov opredeljujemo kot šibko notacijo. Strožja notacija agentnosti se ukvarja z lastnostmi, ki jih pripisujemo ljudem; to so: znanje, mišljenje, nameni, želje ipd. Agentom pripisujemo mišljenjska (mentalna) stanja, ki jih sicer pripisujemo ljudem. Želimo načrtovati in zgraditi sistem naprav, porazdeljenih sistemov in naprav, povezanih v inteligentni dom. Sistem naj bo namenski ali usmerjeni, vodijo pa ga stanja mišljenja agentov. Izraz namenski ali usmerjeni sistem (lahko tudi intencijski sistem) je skoval filozof Dennett /Denett - 1987/. Razložimo ga lahko s primerom naslednjih dveh stavkov, ki opredeljujeta dejavnosti človeka: "Dragica je vzela s sabo

dežnik, ker je *menila*, da bo deževalo." in "Konrad trdo dela, ker *hoče* pripraviti doktorsko disertacijo." Ta dva stavka izražata človeško miselnost, na osnovi katere je obnašanje človeka predvidljivo, hkrati pa razlaga njegovo obnašanje z atributi vedênja, kot so mišljenje, hotenje, upanje, strah itd. Oblike vedênja, ki so opisane s takšno obliko človeške miselnosti, se imenujejo namenski ali usmerjeni pojmi ali nameni. Sistem, ki opisuje stvari, za katere lahko predvidimo obnašanje z metodo pripisovanja mišljenja, želja in razumnega obnašanja, pa imenujemo namenski ali usmerjeni sistem. Pripisovanje pojmov, kot so *mišljenje, prosta volja, nameni, zavedanje, sposobnost* ali *hotenje,* stroju je legitimno, če to izraža informacije o stroju na enak način, kot pa jih izraža o človeku /Wooldridge - 1995, McCarthy - 1978/. Takšno pripisovanje lastnosti je uporabno, kadar pomaga pri razumevanju zgradbe stroja, njegovega obnašanja v preteklosti in prihodnosti, ali pa če pomaga pri njegovih izboljšavah. Namenski ali usmerjeni pojmi so abstrakcijska orodja, ki nam ponujajo primeren in vsakdanji način za opisovanje, razlago in napovedovanje obnašanja v kompleksnih sistemih. Agent je sistem, ki ga najbolj primerno opišemo z njegovo usmerjeno držo. V ta namen opredelimo dve kategoriji vedênja: *informacijsko vedênje* (mišljenje in znanje) in *usmerjeno vedênje* (želje, namen, dolžnosti, zavezanost).

Formalno osnovo za obravnavanje usmerjenega vedęnja agentov predstavlja modalna logika in njena razširitev v večmodalno logiko. V navadni izjavni ali predikatni logiki so izjave v kateremkoli modelu ali resnične ali neresnične. V naravnem okolju pa ločimo različne vrste ali oblike resnic, kot na primer: "*biti nujno res*"; "*vedeti, da je res*"; "*verjeti, da je res*" in "*bo res v prihodnosti*". Takšne situacije opisujemo s pomočjo modalne logike, kjer imamo poleg operatorjev navadne izjavne logike še operator nujnosti ($\Box$ - škatla) in slučajnosti ($\Diamond$ - karo). Izjave v osnovni modalni logiki so definirane v naslednji Backus Naurjevi obliki (BNF):

$$\varphi \equiv |\bot|T|p|\neg\varphi|\varphi\vee\varphi|\varphi\wedge\varphi|\varphi\rightarrow\varphi\;|\;\varphi\leftrightarrow\varphi\;|\Box\varphi\;|\Diamond\varphi.$$

Med operatorjema $\Box$ in $\Diamond$ velja naslednja relacija: $\Box\varphi \leftrightarrow \neg\Diamond\neg\varphi$. To preberemo takole: *'Škatla φ je isto kot ne karo ne φ'.* (nujno res je enako kot ni mogoče, da ni res). Ostale izjavne oblike so dovolj jasne in jih ne bomo posebej razlagali. Primer iz realnega sveta bi lahko na osnovi zgornjega opisa izbrali takole: *'Nujno je da bo jutri deževalo.'* $\leftrightarrow$ *'Ni res, da je mogoče, da jutri ne bo deževalo.'* Modalna logika na drugačen način izraža lastnosti sveta. Razvili so jo filozofi, ki jih je zanimala razlika med *nujno resnico* in *slučajno resnico.* Ključna oseba pri snovanju modalne logike je bil C. I. Lewis /Hajdinjak - 2004/, idejo uporabljati modalno logiko za sklepanje o znanju pa je uvedel Jaako Hintikka /Hintikka - 1975/. *Nujna resnica* predstavlja nekaj, kar ne more biti drugače, *slučajna resnica* pa je nekaj, kar bi verjetno lahko bilo drugače. V modalni logiki je zelo pomembna izjava **K:** $\Box(\varphi \rightarrow \psi) \wedge \Box\varphi \rightarrow \Box\psi$. Včasih jo zapišemo tudi na ekvivalenten način v obliki $\Box(\varphi \rightarrow \psi) \rightarrow \Box\varphi \rightarrow \Box\psi$. Ta izjava se v večini knjig imenuje **K** ali Kripkejev aksiom, in sicer v čast logika S. Kripkeja, ki je uvedel tako imenovano semantiko možnih svetov. Pomembne so še naslednje izjavne oblike **T**: $\Box\varphi \rightarrow \varphi$, kar je refleksija, **D**: $\Box\varphi \rightarrow \Diamond\varphi$, čemur pravimo serija, **4**: $\Box\varphi \rightarrow \Box\Box\varphi$, kar imenujemo tranzitivnost in **5**: $\Diamond\varphi \rightarrow \Box\Diamond\varphi$, ki nakazuje evklidnost. Poznamo različne logične modele, kjer velja različna kombinacija teh izjavnih oblik. Pri obravnavi teorije o razumnih agentih sta pomembna dva modela, in sicer KD45 ali logika prepričanja in KT45 ali epistemska logika ali logika znanja. V epistemski logiki običajno uporabljamo namesto operatorja $\Box$ operator K oziroma K_i. Izjavna oblika $K_i\varphi$ pomeni, da agent i ve, da φ velja. Operator slučajnosti $\Diamond$ pa zapišemo kot $\neg K_i \neg$ ali včasih tudi M_i.

Kombinacija prvostopenjske izjavne logike in modalne logike z večjim številom modalnih operatorjev sestavlja večmodalno logiko, s pomočjo katere lahko obravnavamo razumne agente. V ta namen so bile vpeljane različne večmodalne logike. Najbolj znani sta logiki KARO, ki poleg prepričanja uporablja še znanje /van der Hoek - 2002/ in logika LORA - logika o razumnih agentih, ki je zelo lepo razložena v /Wooldridge - 1998/. V LORI lahko na primer zapišemo $\exists i \cdot$ (Bel *i Sončno(ljubljana)),* kar pomeni, da obstaja agent i, ki je prepričan, da je v Ljubljani sončno vreme. Podobno lahko zapišemo, da je *vsakdo* prepričan, da je v Ljubljani sončno: $\forall i \cdot$ (Bel *i Sončno(ljubljana)).* Poleg operatorja *Bel* za prepričanje uporabljamo v LORI še operatorja *Des* za željo in *Int* za namen. LORO sestavljata poleg prvostopenjske komponente in BDI-komponente še časovna komponenta in komponenta dejanj. Zapišemo lahko, recimo, tudi izjavo: $Int\ i\ \varphi \Rightarrow Bel\ i\ \Diamond\varphi$ (če *i* namerava φ, potem je *i* prepričan, da je φ mogoč), ki ustreza značilnemu odnosu med nameni in željami.

3. Razumni agenti in BDI-arhitektura

Pripisovanje usmerjenih pojmov, kot so mišljenje, prosta volja, nameni, zavedanje, sposobnost ali hotenje, stroju je torej legitimno, če to izraža enake informacije o stroju, kot jih izraža o človeku. Te lastnosti pripišemo stroju kot razumnemu agentu, ki deluje na osnovi BDI-modela, to je modela "*prepričanj, želja in namenov*". Obnašanje človeka vsekakor najbolje modelira *tehnika razumnih agentov*, ki s pomočjo logične formalizacije prepričanj, želja in namenov tehniko usmerjanja k cilju izboljša. V /Laza - 2003/ so obravnavani preudarni agenti, ki se morajo odzivati na dogodke. Ti se dogajajo v okolju. Prevzemati morajo pobudo glede na svoje cilje, sodelovati morajo z drugimi agenti (ali ljudmi) in uporabljati predhodne izkušnje za doseganje zastavljenih ciljev. Inteligentni razumni agenti so obravnavani v /Pokhar - 2005/ kot primer modeliranja sveta s pomočjo agentov, ki premorejo- lastna miselna stanja. Agent deluje razumno. S tem doseže svoje cilje, če le ima znanje o svetu in sposobnost, da izvaja planirana dejanja. Wooldridge meni, da si lahko agente predstavljamo kot sisteme, ki so nameščeni in vključeni v neko okolje - agenti niso sistemi, ki ne bi imeli okolja /Wooldridge - 2000/. Agenti torej naj zaznavajo svoje okolje in imajo nabor možnih

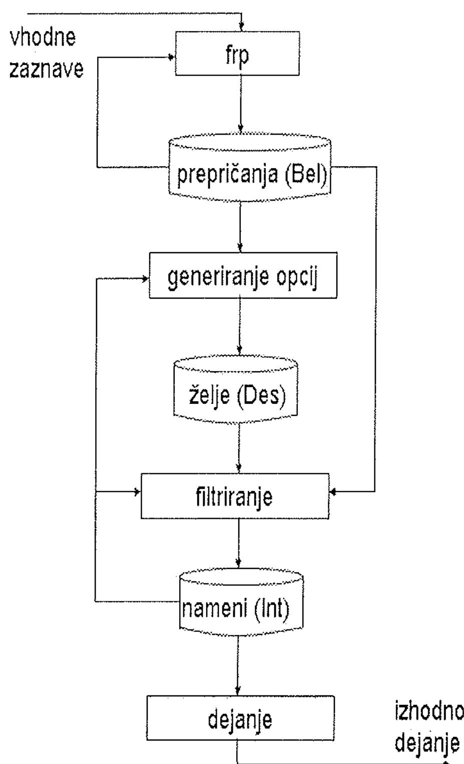
dejanj, katera lahko izvajajo tako, da vplivajo na okolje (slika 1). Razumni agent izvaja dejanja, ki na osnovi njegovega znanja o okolju, v katerem deluje, povečujejo njegove možnosti za uspeh. Dejanja razumnega agenta so odvisna od agentovih predhodnih izkušenj, agentovih informacijah o okolju, dejanj, ki jih ima agent na razpolago, in ocene koristi in možnosti za uspeh teh dejanj.

3. 1. BDI-model

Georgeff pravi, da postaja BDI-model verjetno najbolj znan in preučevan model razumnega agenta s praktičnim razmišljanjem /Georgeff - 1999/. Obstaja veliko število razlogov za ta uspeh, vendar je mogoče najbolj pomembno, da ta model kombinira ugledni filozofski model praktičnega razmišljanja, ki ga je razvil Bratman /Bratman - 1987/, številne izvedbe BDI-modela kot so originalna Bratmanova arhitektura IRMA (Intelligent Resource-bounded Machine Architecture) /Bratman - 1988/ in najbolj znana izvedba BDI-modela v sistemu PRS (PRS - Procedural Reasoning Machine) /Georgeff - 1987/) ter več uspešnih aplikacij, vključno s slavno diagnozo napak vesoljskega taksija in sistem zračnega upravljanja OASIS /Rao - 1995/, in končno elegantno abstraktno logično semantiko - teorijo, ki jo zelo strogo formalizira družina BDI-logik. Na kratko bomo opisali generični BDI-model in enostavno izvedbo BDI-agenta - njegovo programsko komponento.

3. 2. Generični BDI-model

Generični BDI-model je narisan na sliki 2.



Slika 2: Generični BDI-model.

V nadaljevanju predstavlja zapis *γ(T)* moč množice tipa *T*, *x* pa predstavlja kartezijski produkt. Določimo lahko glavne komponente agentove nadzorne zanke v generičnem modelu s slike 2. Proces, s katerim agent posodablja prepričanje, je formalno modeliran s *funkcijo revizije prepričanja - frp : γ(Bel) x zaznave → γ(Bel).* Trenutno prepričanje in trenutne zaznave določajo novo množico prepričanj. Funkcijo *preudarjanja* agenta razdelimo na dve ločeni funkcionalni komponenti: *generiranje opcij* - pri tem agent generira množico možnih alternativ, in *filtriranje* - pri tem agent izbira med kompetitivnimi alternativami. Formalno -funkcijo za generiranja *opcij* zapišemo kot: *opcije: γ(Bel) x γ(Int) → γ(Des).* Da bi agent izbiral konkurenčne opcije, uporablja funkcijo *filtriranja,* ki jo zapišemo takole: *filter : γ(Bel) x γ(Des) x γ(Int) → γ(Int).* Dejansko je to proces preudarjanja, ki ga izvaja agent. Agentovo razmišljanje o sredstvih za doseganje ciljev podaja planska funkcija: *plan: γ(Bel) x γ(Int) -> Plan.* Pri izvedbi agenta moramo zagotoviti pravočasno posodabljanje prepričanja, ponovnega tehtanja opcij in ponovnega planiranja.

3. 3. Izvedba razumnega agenta

Na osnovi razlage iz podpoglavja 3.2 lahko opredelimo tako imenovano *programsko komponento* razumnega agenta BDI, oziroma način, kako lahko agenta zgradimo. Na sliki 3 vidimo osnovno nadzorno zanko agenta. Agent neprenehoma izvaja postopek, v katerem opazuje svet, se odloča, kateri bo naslednji namen, ki ga bo poskušal udejanjiti. Določi neke vrste plan za doseganje postavljenega cilja in potem ta plan izvaja.

1. **while true do**
2. agent opazuje svet;
3. agent posodablja notranji model sveta;
4. agent preudarja o tem, katere namene naj udejanji v naslednjem koraku;
5. agent razmišlja o sredstvih za doseganje ciljev in zasnuje načrt za udejanjanje namena;
6. agent izvaja načrt;
7. **end while;**

Slika 3: Splošna nadzorna zanka agenta.

Osnovno izvajalno zanko s slike 3 lahko razgradimo na detajlnejše agentove posege, s čimer pridemo do mnogo realnejšega algoritma. Prikazuje ga slika 4.

1. B := B_0; /* B_0 so začetna prepričanja */
2. I := I_0; /* I_0 so začetni nameni */
3. **while true do**
4. pridobi naslednjo zaznavo ρ;
5. B := frp(B, ρ);
6. D := opcija (B,I);
7. I := filter(B, D, I);
8. π := plan(B,I);
9. **while not** (prazen(π) **or** uspešen(I, B) **or** nemogoč(I, B)) **do**

```
10.         α := glava (π);
11.         izvaja(α);
12.         π := konec(π);
13.         pridobi naslednjo zaznavo ρ;
14.         B := frp(B, ρ);
15.         if pretehta(I,B) then
16.               D := opcije(B,I);
17.               I := filter(B, D, I);
18.         end-if
19.         if not smiseln(π, I, B) then
20.               π := plan(B, I)
21.         end-if
22.     end-while
23. end-while
```

Pomen posameznih oznak:

- *B* je spremenljivka, ki vsebuje agentovo trenutno prepričanje.
- *D* je spremenljivka, ki vsebuje agentovo trenutno željo.
- *I* je spremenljivka, ki vsebuje agentov trenutni namen.
- *ρ, ρl*, ... predstavljajo zaznave.
- *Plan* je množica, ki jo sestavljajo predpogoji in izhodni pogoji.
- Telo plana je dejanski recept za izvedbo plana.
- Če je π plan, potem lahko z njim opravimo naslednje operacije:
- *pred(π), izhod(π), telo(π),*
- *prazen(π), izvaja(π),*
- *glava(π), konec(π),*
- *smiseln(π, I, B).*
- *frp* - funkcija revizije prepričanja.

Slika 4: Nadzorna zgradba previdnega in smotrno zavezanega agenta.

V zunanji izvajalni zanki agent zaznava okolje in posodablja prepričanje, generira želje oziroma cilje in izbira konkurenčne opcije s pomočjo funkcije *filter*. Iz prepričanja generira plan za doseganje namenov. Pogoji za izvajanje notranje zanke so trije: izvaja se, dokler ni plan prazen, uspešen ali nemogoč. Ti pogoji določajo previdnega in smotrno zavezanega agenta. V notranji zanki agent ponovno posodablja prepričanje, pretehta opcije in ponovno planira. Te posege mora opravljati v ustreznih, pravočasnih časovnih intervalih. Na tem modelu in algoritmu temelji razvojno orodje jadex za agentne sisteme, ki ga opisujemo v naslednjem poglavju.

4. Orodja za načrtovanje agentov in agentih skupnosti

4. 1. Metodologije za agentno orientirano načrtovanje programske opreme

S pomočjo agentno orientiranega pristopa lahko načrtujemo fleksibilne sisteme z zamotanim in s popolnim vedênjem. Načrtovanje večagentih sistemov vključuje zamotane postopke in več nivojev načrtovanja. Danes so na voljo agentno orientirana razvojna orodja, ki omogočajo, da si to tehnologijo prisvaja tudi industrija. Rezultati so obetavni in to usmerja tudi nas pri študiju agentne tehnologije kot alternative poti za načrtovanje inteligentnih naprav - razumnih hišnih pomočnikov. Združenje AOSE (Agent Oriented Software Engineering) - agentno orientirano načrtovanje programske opreme - združuje dejavnosti s področja metodologij načrtovanja programske opreme, razvojnih orodij in programskih jezikov za področje agentno orientiranih sistemov. Posvetovanja AAMAS (Autonomous Agents and Multiagent Systems) obravnavajo zelo široka področje agentih sistemov.

Običajno predstavljajo predlagane metodologije razširitev obstoječih objektno orientiranih metodologij, ki vključujejo koncepte agentnega načrtovanja /Massonet - 2002/. Vse te metodologije imajo naslednje skupne pristope in postopke za načrtovanje večagentnega okolja, kakor jih navajamo v nadaljevanju.

Organizacija: Organizacija agente skupnosti predstavlja skupnost agentov, ki sodelujejo za skupne namene. To je virtualna zgradba, ker nima vgrajenega posebnega nadzornega sistema, ki bi tej zgradbi ustrezal. Storitve zagotavlja in skupaj dosega skupnost agentov, ki organizacijo sestavljajo. Njena zgradba se izraža skozi moč povezav med sestavnimi deli in pa vedęnjskimi in koordinacijskimi mehanizmi sodelovanja med njimi.

Vloga: Vloga določa zunanje značilnosti agenta v določenem kontekstu njegove obravnave. Agent lahko igra večje število vlog, pa tudi večje število agentov lahko igra isto vlogo.

Cilji: Cilje lahko enačimo z željami agenta. Za vsakega agenta določimo njegove cilje in delne cilje.

Vhodne zaznave in izhodna dejanja: Vhodne zaznave in izhodna dejanja predstavljajo agentov stik s svetom oziroma okoljem. Stanje sveta zaznavajo vhodne zaznave, z njimi agent posodablja svoje znanje in prepričanje. Izhodna dejanja temeljijo na nivoju agentovega znanja in prepričanja; z njimi agent deluje na okolje. Zaznave in dejanja se izvajajo kot plani agenta.

Sodelovanje z drugimi agenti: Agenti v večagentnem sistemu sodelujejo med sabo tako, da si izmenjujejo sporočila. Uporabljamo dogovorjene protokole. V našem primeru uporabimo platformo JADE /Bellifemine - 1999/, ki izkorišča komunikacijski standard FIPA.

V literaturi so obravnavane predvsem naslednje metodologije za načrtovanje agentov in agentih sistemov, ki združujejo zgornje pristope: Prometheus, MaSE, Tropos, AUML, GAIA /Shehory - 2005/.

4. 2. Programska orodja za programiranje agentih sistemov

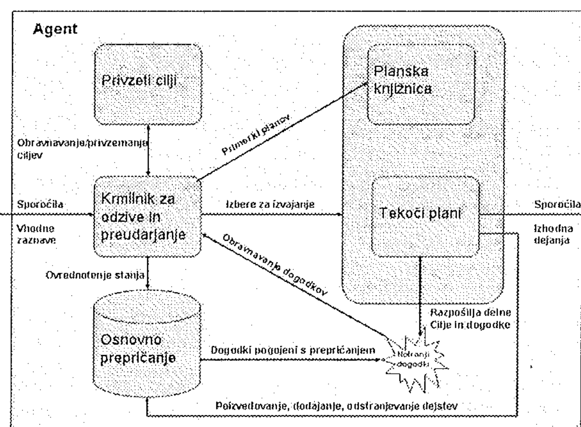
Obstaja vrsta orodij za razvoj agentno orientiranih sistemov, od razvojnih okolij do programskih jezikov /Dastani - 2005/.

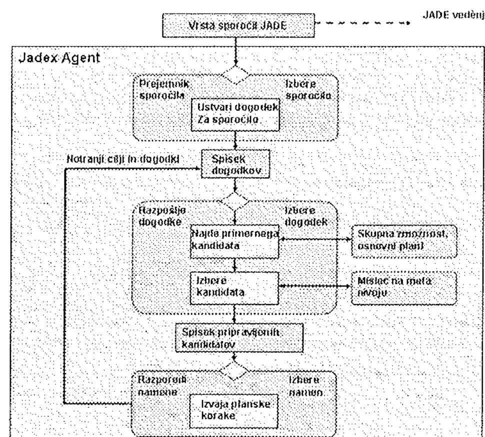
Naštejmo jih nekaj, medtem ko nekoliko natančneje opisujemo JADE in jadex, ki ju kasneje uporabimo za izvedbo agentne skupnosti "večagenti pomočnik pranja": programski jeziki 3APL, AgentSpeak, JASON in programska okolja JACK, JADE, jadex.

4. 3. JADE in jadex

Jadex označujemo tudi kot BDI-stroj za razmišljanje /Dastani - 2005/. BDI-model je zelo primeren za opisovanje agentovih mišljenjskih stanj /Braubach - 2004/. Želje (cilji) agenta predstavljajo njegovo motivacijsko držo in so glavni vir agentovih dejanj. Predstavitev ciljev in rokovanje z njimi igra torej osrednjo vlogo pri ciljno orientiranih analizah in tehnikah modeliranja, kot je jadex. Jadex je vgrajen (ali nadgrajen) na platformo JADE. Zasnovan je torej na BDI-modelu in integrira agentne teorije, ki so objektno orientirane in opisane z jezikom XML. Eksplicitna predstavitev ciljev dovoljuje razmišljanje in upravljanje s cilji. Platforma JADE /Bellifemine - 1999/ se osredotoči na vpeljavo referenčnega modela FIPA, ki predstavlja zahtevano komunikacijsko infrastrukturo in platformo za storitve, kot je na primer upravljanje z agenti, ter množico razvojnih in testnih orodij. Namenoma pušča odprte številne stvari, ki se tičejo notranjega koncepta agenta, in s tem nudi enostavni, opravilno zasnovani model, v okviru katerega lahko razvijalec zasnuje kakršnokoli obnašanje agenta. Zaradi tega je zelo primeren za izvedbo stroja za razmišljanje. Medtem ko je JADE agentna platforma, pripravljena za stik z zunanjostjo, ki vključuje komunikacijo in agentovo upravljanje, lahko stroj za razmišljanje obvladuje notranjost agenta. Obnašanje razumnega agenta, zasnovanega na BDI-modelu, določajo torej prepričanja, plani in cilji. Te tri komponente so združene v skupnost, ta pa opredeljuje skupne sposobnosti sistema, ki jih lahko potem modularno izkoristimo. Abstraktna jadexova arhitektura ter njegov abstraktni model sta narisana na sliki 5. Jadex temelji na generičnem BDI-modelu razumnega agenta, ki smo ga opisali v poglavju 3. Navzven predstavlja jadex črno škatlo, ki sprejema in oddaja sporočila. Na ta način zaznava okolje in vanj posega s svojimi dejanji. Vsakemu sporočilu sledi notranji dogodek, ki ga prestreže in obravnava krmilnik dogodkov. Ta skrbi za odzivno in preudarno vrednotenje dogodkov. Nove dogodke lahko prožijo tudi cilji in posebni pogoji notranjega prepričanja agentov. Krmilnik za odzive in preudarjanje izbira na osnovi ovrednotenih dogodkov plane, ki se izvajajo. Ti lahko dosegajo in posodabljajo osnovno prepričanje, pošiljajo sporočila drugim agentom, kreirajo nove cilje ali delne cilje in prožijo notranje dogodke. Mehanizem odzivanja in preudarjanja je v splošnem enak za vse agente. Vedênje posameznega agenta torej določajo samo njegova prepričanja, cilji in plani, ki si jih v nadaljevanju poglejmo malo podrobneje.

Prepričanja: Prepričanje odseva osvojena znanja in je shranjeno, da je dosegljivo vsem planom. Agenti lahko poizvedujejo po prepričanjih. Jadex ne vsiljuje logične predstavitve prepričanja. Namesto tega lahko uporabimo običajne javine objekte, ki opisujejo temeljna prepričanja. Objekti torej shranjujejo dejstva ali množice dejstev, ta pa so opisana z dogovorjenimi podatkovnimi strukturami. Podatke, ki ustrezajo prepričanjem, lahko posodabljamo pod vplivom novih dejstev, tako da jih spreminjamo, dodamo ali odstranimo. Po njih lahko poizvedujemo s pomočjo objektnega jezika za oblikovanje poizvedb (OQL - Object Query Language). Prepričanja lahko uporabimo kot vhodne podatke za misleči stroj tako, da določimo stanja prepričanj kot predpogoje za plane ali kot pogoje za dosego ciljev. Stroj nadzoruje spremembe prepričanj in samodejno prireja cilje in plane.





Slika 5: Jadexova abstraktna arhitektura in njegov izvajalni model.

Cilji: Jadex zasleduje splošno idejo, ki pravi, da so cilji dejanske in trenutne želje agenta. Kateremukoli cilju, ki ga ima, agent neposredno priredi primerna dejanja. Cilju sledi, dokler je agent aktiven ali pa se deaktivira oziroma ga zastavljeni cilj ne zanima več. Za razliko od večine drugih sistemov jadex ne predpostavlja, da morajo biti cilji med sabo skladni. Da lahko razlikujemo med ravnokar privzetimi cilji (to je želenimi) in pa zasledovanimi cilji, uvajamo življenjsko dobo cilja, ki jo sestavljajo stanja cilja: *opcija, aktiven* in *začasno odložen.* Kadar postane cilj privzet, postane opcija, ki se doda agentovi zgradbi, želja. Mehanizem preudarjanja je odgovoren za prehode stanj na poti do vseh privzetih ciljev.

Plani: Miselni stroj upravlja vse dogodke, kot so sprejem sporočil ali aktiviranje ciljev, tako da izvaja primerne plane. Jadex uporablja plansko knjižnico, ki vsebuje agentove plane. Vsak plan ima glavo, ki določa okoliščine, pod katerimi se plan izbere, in telo plana, ki določa dejanja za izvajanje. Najpomembnejši del glave plana so cilji in/ali dogodki, ki upravljajo plan. V planih je določeno, katera agentova izhodna dejanja je treba izvajati in katere vhodne vrednosti je treba zaznavati.

5. Razumni hišni pomočnik kot večagentni sistem

Razumni agent zna izbirati najboljša možna dejanja. Porazdeljene in povezane inteligentne naprave lahko pri tem sodelujejo in skupaj izbirajo dejanja, ki najbolje vodijo do skupne koristi. Pokazati želimo, da je interoperabilnost ne samo koristna, ampak že kar nujna pri vodenju takega porazdeljenega sistema. Pomembni pogoj za interoperabilnost naprav je združljivost, ki je dosežena s standardiziranimi pristopi pri načrtovanju. V tem poglavju želimo torej predstaviti možno izvedbo razumnega agenta s pomočjo razvojnega orodja JADE, ki zagotavlja interoperabilnost porazdeljenih naprav kot agentnih sistemov. Jadex, ki je stroj za razmišljanje, pa prispeva nivo, ki je nameščen nad hrbtenično infrastrukturo JADE in ponuja načrtovanje agentov, zasnovanih na BDI-modelu. Omogoča načrtovanje ciljno orientiranih agentov, ki z mehanizmi preudarjanja izbirajo najboljša možna dejanja in se torej odločajo razumno. S takšno platformo lahko načrtujemo inteligentne sisteme. Orodje dodatno omogoča še, da programiramo v javi. S tem imamo v rokah pomembne razvojne načrtovalske mehanizme za razširitve naših agentov. S pomočjo takšne platforme bomo predstavili enostavni primer razumnega hišnega pomočnika pranja, zgrajenega v obliki agentne skupnosti. Programiranje agentnih sistemov ni preprosto opravilo, saj moramo načrtovati številne usklajene sisteme (agente), njihovo miselno zgradbo - prepričanja in cilje ter njihove medsebojne odnose (objektni poizvedovalni jezik), njihova dejanja - plane (java), sodelovanje in komunikacijo z drugimi agenti (FIPA, JADE). Želimo torej prikazati možno izvedbo razumnega agenta s pomočjo BDI-arhitekture in večagenti sistem kot agentno skupnost v realnem okolju hišne naprave. V našem primeru je to pralni stroj, ki ga upravlja razumni pomočnik pranja (RPP), vgrajen v okolje pralnega stroja. Na osnovi dogovora -dialoga z uporabnikom poskrbi za pranje perila v skladu z uporabnikovimi željami in v skladu z navodili za pranje izbranega in vloženega perila. RPP zna iz vgrajene planske knjižnice izbrati najboljši možni plan za pranje vloženega perila, pri čemer upošteva uporabnikove želje tako, da doseže zastavljene cilje na najboljši možni način.

5. 1. Opredelitev lastnosti razumnega pomočnika pranja kot večagentnega sistema

Odločili smo se torej, da izdelamo RPP kot posebni primerek razumnega hišnega pomočnika. Vendar pa je RPP samo eden izmed agentov, ki sestavljajo večagentnega pomočnika pranja (VAPP). RPP je nadzorni agent z najvišjo stopnjo *samostojnosti* in dejansko določa obnašanje celotnega sistema. Njegovi pomočniki, ki se obnašajo kot *nadzorovani agenti*, opravljajo določena pomožna opravila (opredeljujemo jih v naslednjem podpoglavju) in imajo različne stopnje samostojnosti. Imenujemo jih lahko tudi agenti delavci, saj so zadolženi za čisto rutinska opravila. RPP zna planirati sam zase in za nadzorovane agente. Nadzorovani agenti imajo določene plane, ki jih sami zase ne znajo posodobiti. Okolje VAPP naseljujejo naslednji agenti: *RPP*, *Agent_Termostat*, *Agent_Za_Vodo*, *Agent_Za_Meritev_Čiste_vode*, *Agent_Za_Prašek_ Mehčalo*, *Agent_Za_Vrata_Stroja*, *Agent_Za_Motor*, *Agent_Za_Vlaganje_Perila*, *Agent_GUI*. Njihove lastnosti opredeljujemo v naslednjem podpoglavju. Lastnosti celotnega okolja VAPP in posameznih agentov v agentni skupnosti lahko opišemo izhajajoč iz lastnosti agentov v večagentnem okolju, kakor smo jih navedli v poglavju 1. Okolje VAPP in njegov nadzorni agent RPP se morata obnašati *dobronamerno* in *verodostojno*, kar pomeni, da RPP uporabniku ne bo dovolil izbrati parametrov pranja izven priporočenega obsega in bo v primeru, da eden izmed članov skupnosti odpove, še vedno optimalno opravil svoje delo, če bo to mogoče. Sicer pa bo zaključil pranje na najboljši možni način. Agent se mora znajti tudi v nepredvidenih situacijah in poiskati razumne rešitve. Glede na postavljene želje se bo obnašal *razumno*, kar pomeni, da bo izbral najbolj obetavna dejanja z namenom, da doseže postavljene cilje. Vedno bo znal poiskati razumne rešitve. Glede na uporabnikove želje bo RPP posodabljal svoje prepričanje in se s tem *učil*. RPP bo znal na osnovi dogovora z uporabnikom *samostojno* opraviti svoje naloge in doseči končno stanje, ki pomeni kvalitetno in po željah uporabnika oprano perilo. RPP se mora do drugih agentov v svojem okolju znati obnašati *socialno*, kar dosežemo s komunikacijo po predpisih agentnega komunikacijskega protokola FIPA. Lahko tudi rečemo, da RPP deluje *usmerjeno*, saj zasleduje samo en cilj, to je kvalitetno oprano perilo. *Agent_GUI* in *Agent_Za_Vlaganje_Perila* sta delno samostojna, delno pa tudi nadzorovana agenta te skupnosti. Usmerja ju sicer RPP, vendar pa se dogovarjata z uporabnikom oziroma spremljata proces vlaganja perila samostojno in se pri tem tudi učita.

VAPP, ki ga upravlja RPP, ima vse lastnosti inteligentnega agentnega sistema. Takšen agentni sistem lahko realiziramo z enotno ali na s porazdeljeno strojno opremo.

5. 2. Organizacijska zgradba večagentnega pomočnika pranja

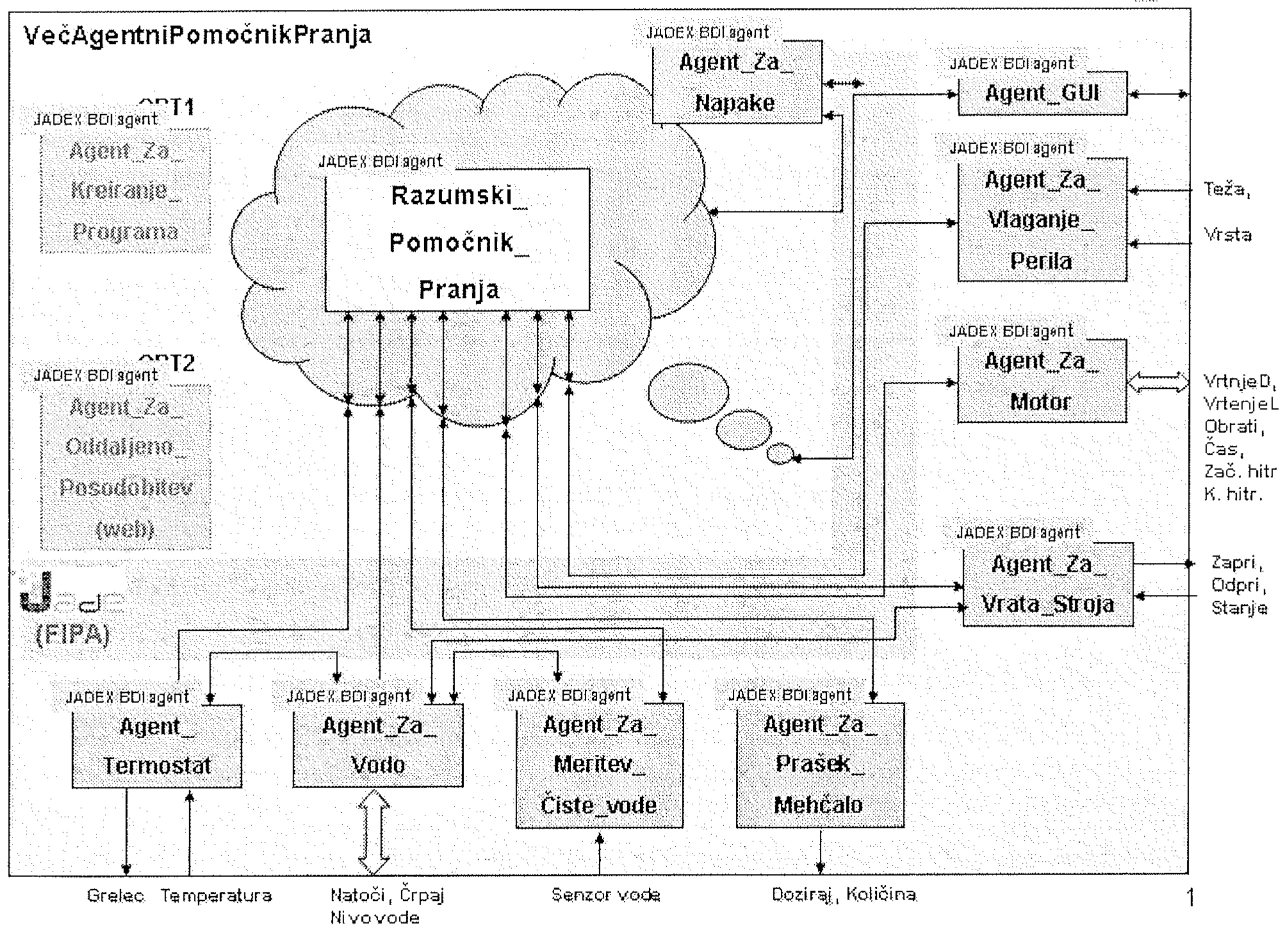
Zgradba oziroma organizacija VAPP je prikazana na sliki 6. Njegovo jedro predstavlja RPP, ki smiselno usmerja delovanje našega hišnega pomočnika, in pa večje število agentov, ki v procesu pranja samostojno izvajajo posamezna opravila pod nadzorom RPP. Gre za delna opravila pri pranju: *Agent_Termostat* je agentni podsistem za uravnavanje temperature vode v bobnu, *Agent_Za_Vodo* skrbi za pris-

otnost določene količine vode v bobnu, *Agent_Za_Meritev_Čiste_vode* meri nivo motnosti vode med pranjem, *Agent_Za_Prašek_Mehčalo* dozira potrebno količino praška ali mehčala, *Agent_Za_Vrata_Stroja* zaklene vrata bobna, ko se poteka pranje, *Agent_Za_Motor* vrti boben, *Agent_Za_Vlaganje_Perila* spremlja vlaganje perila, *Agent_GUI* pa omogoča pogovor med RPP in uporabnikom. Vsi ti nadzorovani agenti komunicirajo z RPP s pomočjo platforme JADE, dogovarjati pa se znajo tudi med sabo. RPP torej udejanja svoj plan in vpliva na okolje s posredovanjem nadzorovanih agentov. Ti so povezani s fizičnim svetom in z drugimi agenti, kar pomeni, da zaznavajo fizični svet pralnega stroja in izvajajo dejanja. Agent termostat na primer zaznava temperaturo vode in s pomočjo grelca vzdržuje zahtevano temperaturo. S prepričanjem nadzorovanih agentov lahko delno upravlja RPP, saj se sami običajno ne učijo, ker opravljajo "rutinska dela", ki so imajo v naprej določen plan. Poleg RPP imata samo *Agent_Za_Vlaganje_Perila* in *Agent_GUI* lastno prepričanje, ki si ga lahko sama posodabljata in se tako učita.

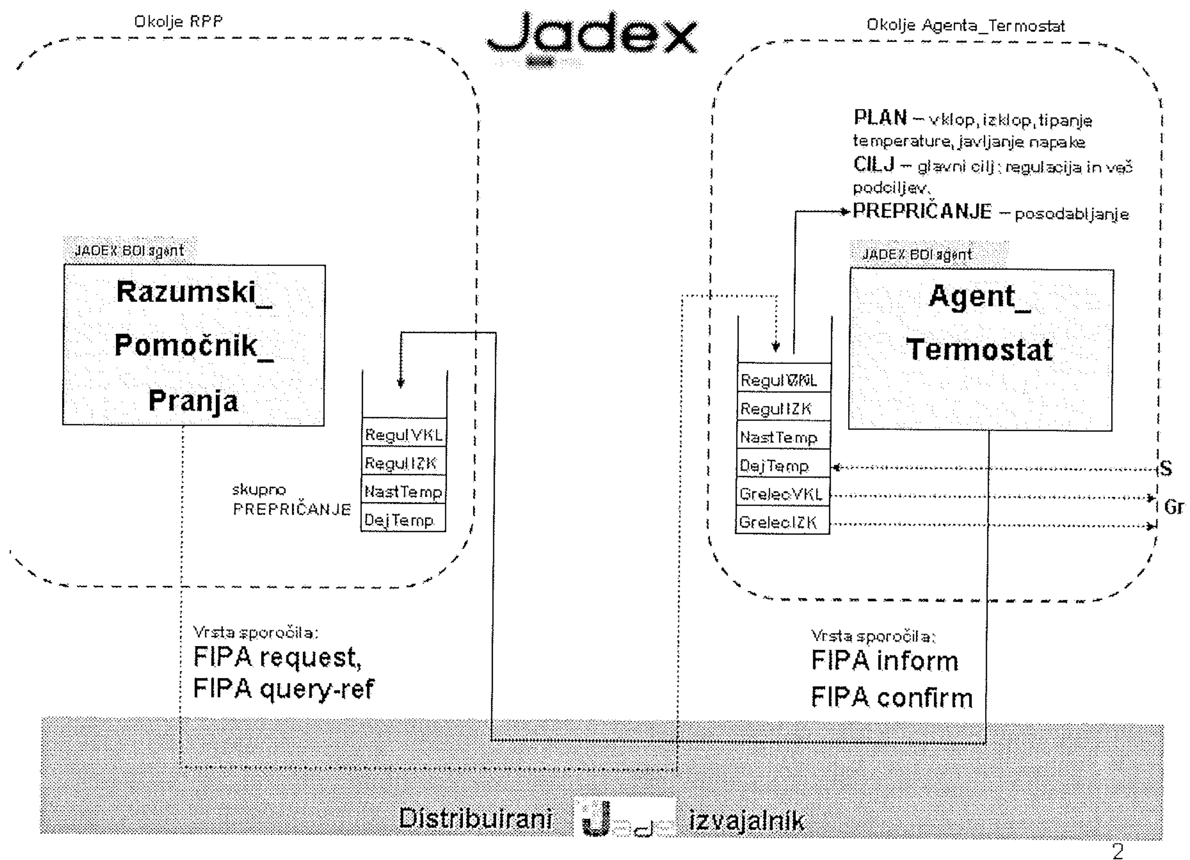
Na sliki 7 je narisana povezava med RPP ter agentom *Agent_Termostat*. Agenta RPP in *Agent_Termostat* sta med sabo povezana preko porazdeljenega izvajalnika JADE. RPP lahko pošlje v sistem za ogrevanje vode dve vrsti FIPA-sporočil. Eno je tipa "FIPA request", s katerim RPP posreduje ukaze, na primer 'vklopiinsegrej 34'. Ta ukaz vklopi proces segrevanja vode in regulacijo na zahtevani temperaturi. Drugi ukaz je tipa "FIPA query-ref"; ta pošlje poizvedbo o stanju naslovljenega agenta. *Agent_Termostat* lahko odgovori na dva načina: z informacijskim sporočilom tipa "FIPA inform" ali s potrditvijo odziva na ukaz, tj. s sporočilom tipa "FIPA confirm".

5. 2. Načrtovanje agenta *Agent_Termostat*

Agent_Termostat predstavlja sistem za ogrevanje vode v VAPP in je poseben primerek nadzorovanega agenta. To ni enostavni odzivni agent, ki bi skrbel samo za vklop in izklop gretja vode, ampak tvori podsistem za ogrevanje vode v napravi - pralnem stroju. Opis postopkov načrtovanja ostalih agentov, med njimi tudi RPP, zaradi obsežnosti tukaj izpuščamo. V skladu z metodologijo načrtovanja agentne programske opreme Prometheus določimo najprej vlogo agenta *Agent_Termostat*, ki jo igra v okviru agentne skupnosti hišnega pomočnika, ki ga nadzira RPP. Ta vloga je zapisana v tabeli 1.



Slika 6: Organizacija večagentnega pomočnika pranja.



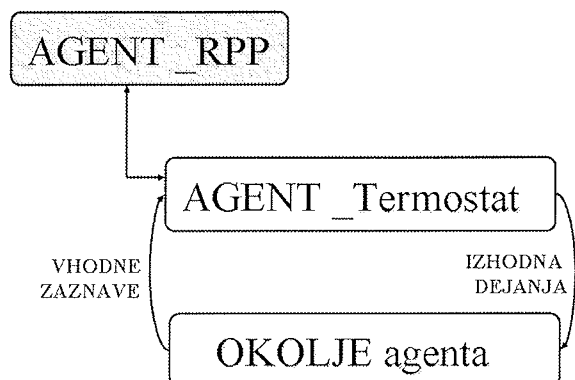
Slika 7: Zasnova agenta za segrevanje vode - Agent_Termostat.

Tabela 1: Vloga agenta Agent_Termostat.

_Agent_Termostat_ zaznava okolico:	
- Zaznava temperaturo vode	Temperaturni senzor meri temperature. Strojna oprema pretvori temperaturo v obliko, ki jo *Agent_Termostat* lahko izmeri.
- Poizve za nivo vode	Dejansko *Agent_Za_Vodo* posreduje informacij o o nivoju vode preko sistema JADE.
- Zaznava moč grelca	Zaznava delovanje grelca – moč na grelcu.
- Sprejema ukaze od RPP	Vklop, izklop, nastavljena temperatura.
_Agent_Termostat_ vpliva na okolico:	
- Vklopi ali izklopi grelec	Grelec vklopi, če je temperatura nižja od nastavljene spodnje meje. Izklopi ga, ko je temperature višja od nastavljene zgornje meje.
- Javi napako	Javi napako grelca, nivoja vode ali tipala za temperaturo tako, da obvesti agenta *Agent_Za_Napake,* ta pa vzpostavi stik z zunanjim, posebnim agentom *Agent_Servis*, ki je zadolžen za izpeljavo vzdrževanja dodeljenih mu naprav.
- Javi stanje v RPP	Javlja svoje stanje agentu v RPP.
_Agent_Termostat_ izvaja naslednje plane:	
Vzdržuje stanje "pripravljen".	
Sprejema ukaze od RPP in mu posreduje stanje sistema za ogrevanje.	
Pri *Agentu_Za_Vodo* preveri nivo vode.	
Vklopi grelec in segreje vodo na zahtevano temperaturo.	
Izvaja regulacijo temperature.	
Javi napako agentu *Agent_Za_Napake* in preide v stanje pripravljen.	
Izklopi regulacijo in preide v stanje pripravljen.	

Agent_Termostat je glede na stopnjo njegove avtonomije torej nadzorovani agent. Nadzoruje ga RPP. Na osnovi splošne zgradbe za razumnega agenta iz poglavja 3, slika 3, lahko narišemo njegovo zunanjo simbolično zgradbo na sliki 8.

Sistemu za ogrevanje vode oziroma agentu *Agent_Termostat* določimo cilje in njegovo notranjo zgradbo. To zgradbo kaže slika 9. Povezanost in pomen postavljenih ciljev sta s sliko dovolj pojasnjena, zato ju ne opisujemo posebej.



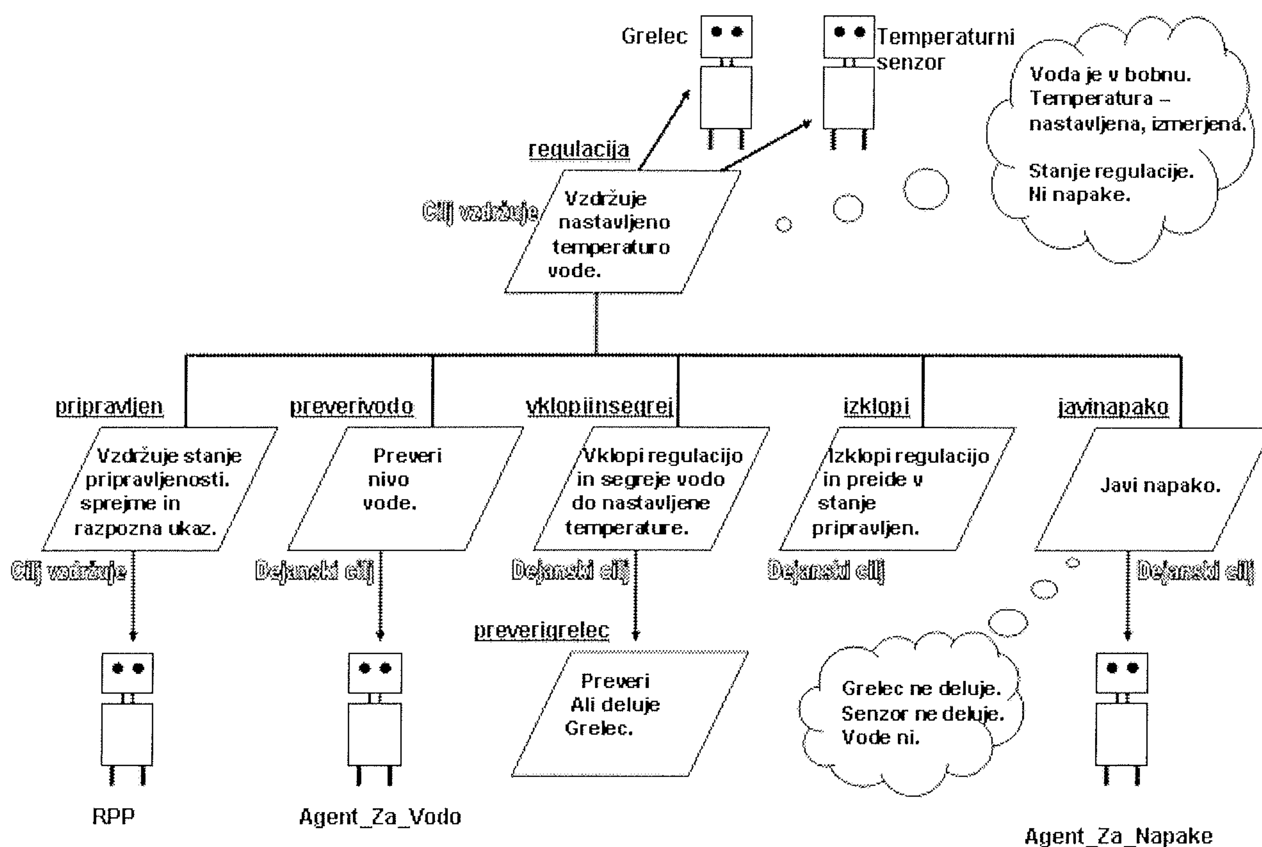
Slika 8: Simbolična zgradba agenta Agent_Termostat.

Izhajajoč iz vloge agenta in njegovih ciljev lahko določimo miselno zgradbo agenta, ki jo opredeljujejo relacije med njegovimi prepričanji, željami in nameni. Ta notranja zgradba, ki skrbi za ogrevanje vode v pralnem stroju, je prirejena razvojnemu orodju za načrtovanje agentov in agentih skupnosti Jadex. Narisana je na sliki 10. Cilji se v jadexu interpretirajo kot želje, plani pa kot nameni agenta. *Agent_Termostat* ima določena naslednja stanja: *Pripravljen, Regulacija, ČakaNaVodo in Napaka.* Agent izvaja plane, ki dosegajo delne cilje ali posodabljajo prepričanje, ki torej vplivajo na njegovo notranjo stanje mišljenja ali na BDI- zgradbo. Plani lahko vključujejo neposredno izvedbo določenih dejanj, lahko pa nanje vplivajo le posredno, tako da postavljajo delne cilje ali posodabljajo prepričanja. Na ta način agent prehaja v nove možne svetove tako da si lahko njegovo delovanje predstavljamo kot obnašanje dinamičnega sistema, katerega stanja se menjajo, kakor določa diagram v obliki drevesa. Posamezno drevo prehajanja stanj pomeni le enega izmed možnih svetov, v katerem se znajde agent. Prestopi med svetovi in s tem tudi iz enega v drugo drevo stanj so odvisni od spreminjanja prepričanj ter prilagajanja želja in poti za njihovo uresničenje.

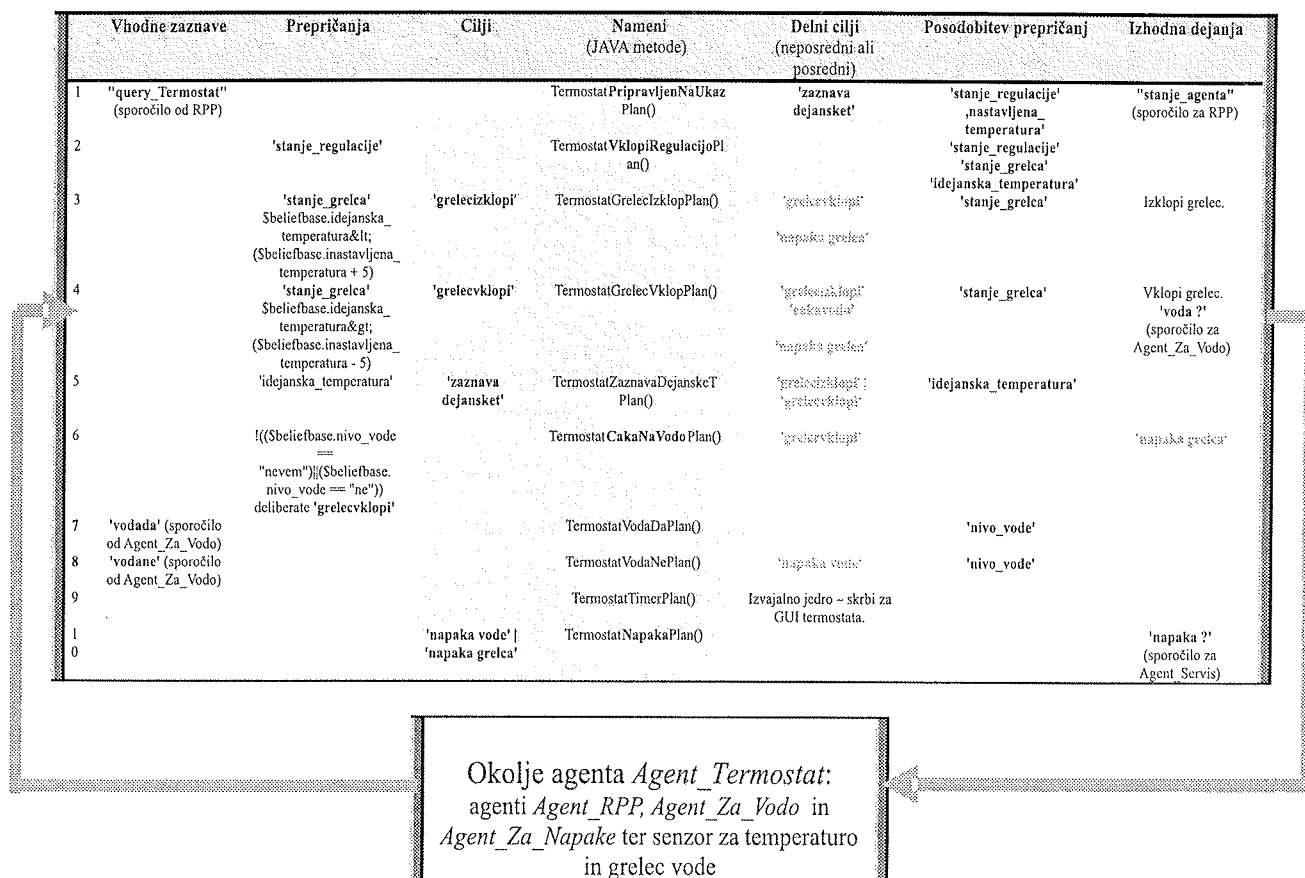
Opišimo nekaj primerov s slike 10:

Zunanja zaznava v prvi vrstici je v obliki sporočila, prejetega od agenta *Agent_RPP*. To sporočilo proži nov plan »Termostat**VklopiRegulacijo**Plan()«, pri čemer je njegova izvedba odvisna od prepričanja '**stanje_regulacije**'. To lahko obravnavamo kot dejanje, ki agenta postavi iz stanja *Pripravljen* v stanje *Regulacija*.

V tretji in četrti vrstici sta pogoja ($T_d < T_n - 5$) oziroma ($T_d > T_n + 5$), ki generirata cilja '**grelecvklopi**' oziroma '**grelecizklopi**' in s tem povzročita dejanje, ki vklopi ali izklopi grelec. Tako namreč poteka regulacija temperature vode



Slika 9: Struktura ciljev agenta Agent_Termostat *in njihova medsebojna povezanost.*



	Vhodne zaznave	Prepričanja	Cilji	Nameni (JAVA metode)	Delni cilji (neposredni ali posredni)	Posodobitev prepričanj	Izhodna dejanja
1	"query_Termostat" (sporočilo od RPP)			TermostatPripravljenNaUkazPlan()	'zaznava dejansket'	'stanje_regulacije' ,nastavljena_temperatura'	"stanje_agenta" (sporočilo za RPP)
2		'stanje_regulacije'		TermostatVklopiRegulacijoPlan()		'stanje_regulacije' 'stanje_grelca' 'idejanska_temperatura'	
3		'stanje_grelca' $beliefbase.idejanska_temperatura< ($beliefbase.inastavljena_temperatura + 5)	'grelecizklopi'	TermostatGrelecIzklopPlan()	'grelecvklopi' 'napaka grelca'	'stanje_grelca'	Izklopi grelec.
4		'stanje_grelca' $beliefbase.idejanska_temperatura> ($beliefbase.inastavljena_temperatura - 5)	'grelecvklopi'	TermostatGrelecVklopPlan()	'grelecizklopi' 'cakavodo' 'napaka grelca'	'stanje_grelca'	Vklopi grelec. 'voda ?' (sporočilo za Agent_Za_Vodo)
5		'idejanska_temperatura'	'zaznava dejansket'	TermostatZaznavaDejanskeTPlan()	'grelecizklopi' | 'grelecvklopi'	'idejanska_temperatura'	
6		!(($beliefbase.nivo_vode == "nevem")\|\|($beliefbase.nivo_vode == "ne")) deliberate 'grelecvklopi'		TermostatCakaNaVodoPlan()	'grelecvklopi'		'napaka grelca'
7	'vodada' (sporočilo od Agent_Za_Vodo)			TermostatVodaDaPlan()		'nivo_vode'	
8	'vodane' (sporočilo od Agent_Za_Vodo)			TermostatVodaNePlan()	'napaka vode'	'nivo_vode'	
9				TermostatTimerPlan()	Izvajalno jedro – skrbi za GUI termostata.		
10			'napaka vode' | 'napaka grelca'	TermostatNapakaPlan()			'napaka ?' (sporočilo za Agent_Servis)

Slika 10: Notranja miselna zgradba agenta Agent_Termostat *v okolju VAPP.*

(T_d). Doseči mora nastavljeno temperaturo (T_n) in skrbeti, da se ne spreminja več, kot določa histereza 5°C. Zaporedje ciljev '**grelecvklopi**' in '**grelecizklopi**' se ponavlja, dokler RPP ne pošlje sporočila '**izklopi**'. Agent vzdržuje stanje *Regulacija.*

Zelo zanimiva je tudi situacija v šesti vrstici, kjer prepričanje '**nivo_vode**' = "ne vem" ali "ne" vodi v stanje *CakaNaVodo.* Dokler v bobnu ni vode, agent preudarja, ali naj vklopi grelec ali ne. Dokler ni vode, grelca seveda ne sme vklopiti.

RPP smo programirali v Borlandovem razvojnem okolju Jbuilder, v katerega smo inštalirali JADE in razvojno okolje za agentne sisteme jadex. Na ta način smo dobili zelo učinkovit sistem za načrtovanje in razvoj porazdeljenih večagentnih sistemov z agenti, ki so zgrajeni na osnovi BDI-modela. S preprostim primerom modeliranja inteligentne hišne naprave v obliki agentnega sistema smo želeli pokazati, kako je možno uporabiti perspektivno večagentno tehnologijo tudi pri snovanju porazdeljenih inteligentnih sistemov in povezanih hišnih naprav.

6. Zaključek

Raziskujemo agente in večagentne sisteme kot novo tehnologijo, s pomočjo katere bomo izdelali inteligentne hišne pomočnike. To so lahko agenti, kot je opisani razumni pomočnik pranja, ali pa tudi kuhanja ali hlajenja, ter njihova večagentna skupnost, v kateri sobivajo.

Najprej smo na kratko povzeli lastnosti večagentih sistemov in poudarili, da sta na področju porazdeljenih računalniških sistemov najpomembnejša medsebojna komunikacija in skupno ter porazdeljeno znanje agentov. Nadaljevali smo z obravnavo teorije namenskega ali usmerjenega vedenja in modalne logike ter njenega pomena za načrtovanje (razumnih) agentov in agentih sistemov. Njena logična razširitev je večmodalna logika, ki nam omogoča, da razmišljamo o razumnem agentu, ki temelji na BDI-modelu, to je modelu prepričanj, želja in namenov, ki so predstavljeni s tremi modalnostmi (Bel, Des in Int). Pomen logike za obravnavo agentov, na primer LORE, ki je sicer v članku nismo podrobneje predstavili, je predvsem v tem, da lahko z njeno pomočjo sistematično razmišljamo o lastnostih razumnih agentov. Opisali pa smo generični BDI-model in lastnosti ter programsko izvedbo razumnega agenta. Oboje služi kot temelj v večini agentih razvojnih orodij, ki jih v članku omenjamo. Področje agentnih sistemov je podprto s številnimi metodologijami načrtovanja, razvojnimi sistemi, orodji in programskimi jeziki. Med njimi smo nekoliko natančneje pregledali JADE in razvojni sistem Jadex, ki smo ju potem tudi uporabili za izvedbo večagentnega pomočnika pranja. Ideje, ki so nas pri tem vodile, smo osvetlili v zadnjem poglavju.

S primerom, ki ga obravnavamo v zadnjem poglavju, smo pokazali, kako lahko načrtujemo inteligentne hišne naprave kot večagentne sisteme. S tem smo postavili osnovo za nadaljnje raziskovalno delo, ko bomo na osnovi takšne arhitekture raziskovali miselno zgradbo Razumnega Hišnega Pomočnika in kot njegove posebne primerke - Razumnega Pomočnika Pranja, Razumnega Pomočnika Kuhanja in Razumnega Pomočnika Hlajenja. Obravnavali jih bomo kot posamezne razumne agente in kot pomočnike, ki delujejo kot samostojni ali nadzorovani agenti in opravljajo neko določeno hišno opravilo, se lahko učijo, vodijo dialog med človekom in strojem v čimbolj naravnem jeziku, ki si ga izpopolnjujejo, ter znajo sodelovati z drugimi hišnimi pomočniki v agentni skupnosti, ki jo bomo zgradili in preizkusili ter ovrednotili.

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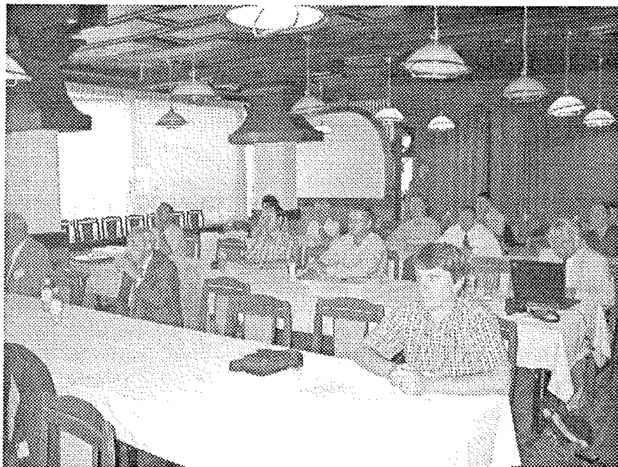
Prispelo (Arrived): 23. 11. 2005; Sprejeto (Accepted): 08. 12. 2005

Konferenca MIDEM 2005 - pročilo
MIDEM 2005 Conference - report

41. Mednarodna konferenca o mikroelektroniki, elektronskih sestavnih delih in materialih - MIDEM 2005

14.09.2005 - 16.09.20045, Hotel RIBNO pri BLEDU

Enainštirideseta mednarodna konferenca o mikroelektroniki, elektronskih sestavnih delih in materialih - MIDEM 2005 (41st International Conference on Microelectronics, Devices and Materials) nadaljuje tradicijo mednarodnih konferenc MIDEM, ki jih vsako leto prireja MIDEM - Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale.



Na konferenci je bilo predstavljenih 47 rednih in osem vabljenih predavanj v petih sekcijah in delavnici na temo ZELENA ELEKTRONIKA.

Na konferenci so bili predstavljeni najnovejši dosežki na naslednjih področjih:

- optoelektronika
- fizika polprevodniških komponent, modeliranje in tehnologija
- keramika, kovine, kompoziti in filmi
- elektronika
- integrirana vezja

Letošnje leto smo v okviru konference že osmič zapored organizirali delavnico, ki vsako leto obravnava posebej izbrano tematiko. V okviru delavnice šest do osem vabljenih predavateljev predstavi izbrano tematiko z različnih aspektov in tako poda poslušalcem popolno dragoceno informacijo. V rednem delu delavnice pa so predvidene predstavitve konkretnih rezultatov in dela udeležencev s tega področja.

Letos smo organizirali delavnico z naslovom : "Zelena elektronika" (Workshop on "Green Electronics"), v okviru kat-

ere smo poskušali osvetliti problematiko prehoda na neosvinčeno tehnologijo izdelave elektronskih komponent in elektronike v skladu z Evrospko zakonodajo in RoHS direktivo.

Letošnji vabljeni referati so bili naslednji:

M.Lethiecq, F.Levassort, L.P. Tran-Huu-Hue
Ultrasonic Transducers for High Resolution Imaging: From Piezoelectric Structures to Medical Diagnostics

R.Ubar
Decision Diagrams and Digital Test

V.Eveloy, S.Ganesan, Y.Fukuda, J.Wu, M.G.Pecht
WEEE, RoHS, And What You Must Do To Get Ready for Lead-Free Electronics

G.Koziol
Quality Laboratory for Investigation of Lead-free Materials and Processes

Z.Drozd, J.Bronowski, J.Drozd, M.Szwech
Accelerated Reliability Tests of Lead-free Soldered Joints

K.Bukat
Results of Lead-free Soldering Experiments on Pilot Line

P.Mach, A.Duraj
Adhesive Joining or Lead-free Soldering ?

J.Renko
Directives WEEE/RoHS: From Early Information to the Slovenian Implementation

Izdali smo zbornik referatov v obsegu okoli 23 ap (približno 372 strani), ki je podobno urejen kot vsa prejšnja leta.

Nekaj statističnih podatkov:
Število udeležencev: 74, iz tujine 9
Število referatov v zborniku: 53, iz tujine 10
Število predstavljenih referatov: 50, iz tujine 8

V okviru konference smo v sredo zvečer, 15.09.05, obiskali razstavo Slovenskih impresionistov v Pristavi pri Bledu.

SEZNAM UDELEŽENCEV KONFERENCE MIDEM 2005, Hotel RIBNO, BLED

ŠT.	IME IN PRIIMEK	ORGANIZACIJA	DRŽAVA
1	WERNER RECZEK	INFINEON, Villach	A
2	WERNER SATTLEGGER	INFINEON, Villach	A
3	PAVEL MACH	CTO PRAGUE	CZECH. REP.
4	RAIMUND UBAR	TALLINN UNIVERSITY OF TECHNOLOGY	EST
5	MARC LETHIECQ	FRANCOIS-RABELAIS UNIVERSITY, Tours	F
6	GRAZYNA KOZIOL	TELE AND RADIO RESEARCH INSTITUTE, Warszawa	POL
7	KRYSTINA BUKAT	TELE AND RADIO RESEARCH INSTITUTE, Warszawa	POL
8	ZDZISLAW DROZD	WARSAW UNIVERSITY OF TECHNOLOGY	POL
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10	ALEKSANDER SEŠEK	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
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19	DRAGO STRLE	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
20	DUŠAN RAIČ	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
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22	JANEZ TRONTELJ	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
23	JANEZ TRONTELJ ML.	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
24	JERNEJ GOLJAVŠČEK	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
25	JOŽE DEDIČ	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
26	JURIJ PODRŽAJ	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
27	KRISTJAN BAŠA	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
28	LEON PAVLOVIČ	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
29	MARIJAN MAČEK	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO

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35	SLAVKO AMON	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
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37	VOJAN ROZMAN	FAKULTETA ZA ELEKTROTEHNIKO, LJ.	SLO
38	DEAN KOROŠAK	FAKULTETA ZA GRADBENIŠTVO, MB	SLO
39	DANIJEL HRIBERŠEK	GORENJE, VELENJE	SLO
40	JANEZ RENKO	GZS, LJUBLJANA	SLO
41	DARKO BELAVIČ	HIPOT-HYB, ŠENTJERNEJ	SLO
42	MARINA SANTO ZARNIK	HIPOT-HYB, ŠENTJERNEJ	SLO
43	JANETA FAJFAR PLUT	HYB, ŠENTJERNEJ	SLO
44	KOSTA KOVAČIČ	IDS, LJUBLJANA	SLO
45	IRENA ŠKULJ	IMT, LJUBLJANA	SLO
46	MATJAŽ GODEC	IMT, LJUBLJANA	SLO
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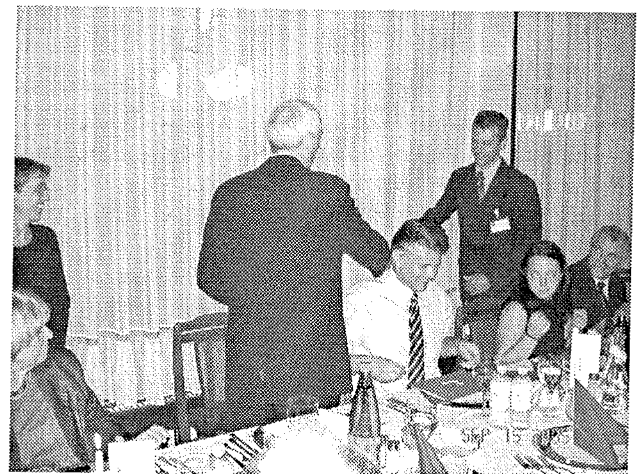
48	ANTON ZALAR	INSTITUT JOŽEF STEFAN, LJ.	SLO
49	BARBARA MALIČ	INSTITUT JOŽEF STEFAN, LJ.	SLO
50	BRUNO CVIKL	INSTITUT JOŽEF STEFAN, LJ.	SLO
51	DUBRAVKA ROČAK	INSTITUT JOŽEF STEFAN, LJ.	SLO
52	FRANC NOVAK	INSTITUT JOŽEF STEFAN, LJ.	SLO
53	GORAN DRAŽIČ	INSTITUT JOŽEF STEFAN, LJ.	SLO
54	JANEZ KOVAČ	INSTITUT JOŽEF STEFAN, LJ.	SLO
55	MARIUSZ WEGRZYN	INSTITUT JOŽEF STEFAN, LJ.	SLO
56	MARKO HROVAT	INSTITUT JOŽEF STEFAN, LJ.	SLO
57	MATJAŽ KOŽELJ	INSTITUT JOŽEF STEFAN, LJ.	SLO
58	SLAVKO BERNIK	INSTITUT JOŽEF STEFAN, LJ.	SLO
59	SREČKO MAČEK	INSTITUT JOŽEF STEFAN, LJ.	SLO
60	UROŠ CVELBAR	INSTITUT JOŽEF STEFAN, LJ.	SLO
61	DIANA KAIČ	ISKRA EMS, ŠENTJERNEJ	SLO
62	MARIJA ZUPAN	ISKRA TEL, KRANJ	SLO
63	MATEJA POTOČNIK	ISKRA TEL, KRANJ	SLO
64	MATIJA MILOSTNIK	ISKRA TEL, KRANJ	SLO
65	SREČKO ZUPANČIČ	ISKRA TEL, KRANJ	SLO
66	BREDA KODEK	ISKRAEMECO, KRANJ	SLO
67	JOŽEF PERNE	ISKRAEMECO, KRANJ	SLO
68	UROŠ BIZJAK	ISKRAEMECO, KRANJ	SLO
69	VJEKOSLAV DELIMAR	ISKRAEMECO, KRANJ	SLO
70	FRANC KOPLAN	MAGNETI, LJUBLJANA	SLO
71	MATJAŽ PIVK	METREL, HORJUL	SLO
72	IZTOK ŠORLI	MIDEM, LJUBLJANA	SLO
73	MILAN TASEVSKI	SIPO, LJUBLJANA	SLO
74	MIKE PECHT	CE UMC, MARYLAND	USA

Predsednik društva dr.Slavko Amon je podelil priznanja društva MIDEM

Med konferenčno večerjo je predsednik društva MIDEM, prof.dr.Slavko Amon, podelil priznanja posameznikom, ki so v preteklih letih na kakršenkoli način zaznamovali in podprli delo društva ter močno prispevali k razvoju njegove dejavnosti.



Prejemniki priznanj posamezniki so:

Prof.dr.Marija Kosec, Igor Pompe, Dr.Iztok Šorli in prof.dr.Marko Topič

NOVICE
NEWS

New process could speed up move to 45nm mode

Scientists working at semiconductor research consortium Sematech have identified a dual damascene method for interconnect integration that could achieve an aggressive industry target for ultra low-k dielectric materials used in semiconductor manufacturing.

The two-level metal, dual damascene process uses two Zirkon interlayer dielectric (ILD) films from Rohm and Haas Electronic Materials to demonstrate a copper/ultra low-k (ULK) integration with a k-effective (keff) value of 2.5, the target set out by the International Technology Roadmap for Semiconductors (ITRS) for the 45nm technology generation. By using ULK dielectric films and newly developed flows, the process achieves a lower k-effective result.

"The dual damascene integration that our team developed offers a potential solution for blocking precursor penetration and minimising process-induced damage typically observed with ULK dielectrics containing interconnected pores," said Ward Engbrecht, a Sematech copper low-k integration project engineer.

Ultra low-k films are porous materials that are much less dense than organosilicate glasses, the starting material for advanced interconnect technology dielectrics. ULK is critical to advanced semiconductor manufacturing because it will allow metal lines to be packed closer together on a chip with less capacitance-driven delay, which slows chip performance. However, as previously noted by Sematech, the integrated ULK must be evaluated according to keffective, which is the overall k-value of a dielectric material and its associated layers after processing.

Throughout the late 1990s and early 2000s, the semiconductor industry drove toward developing materials with progressively decreasing k-values, but process-induced damage to these materials is becoming increasingly problematic as the industry approaches the 45nm node, which is slated to enter production in 2010. Focusing on the challenges associated with dual damascene processing (in which metal lines and vias are laid down in a single step), the Sematech approach deposits the dielectric films by spin-on-deposition to form a matrix-porogen system that can be integrated as a dense material through chemical mechanical planarisation, Rohm and Haas's ILD process. The porogen then can be removed in a thermally-assisted ultraviolet cure process to create a system with a keff value of approximately 2.5. (This late removal of porogen avoids many issues associated with conventional processing of porous dielectrics).

"The key to achieving a keff value of 2.5 in this integration approach is the use of ultra low-k materials throughout the integration scheme except for the dielectric barriers and the minimisation of process induced damage," said Klaus Pfeifer, Sematechs program manager for copper low-k integration.

"Our results show a process that has real promise as a solution for k-effective at 45nm," said Sitaram Arkalgud, Sematechs interconnect director. "We will continue to refine our approach with an eye to reliability and eventual high-volume manufacturing."

Infineon alliance with Russia's KNC

Based on the agreement, the companies will foremost promote wirebond packaging technology in Russia and the Commonwealth of Independent States (CIS).

Infineon will make available its expertise in production methods for smart card chip packages and will transfer two conventional assembly lines to KNCs semiconductor production facility, Mikron, in Zelenograd, Russia. KNC on its part will integrate Infineons chips in its future smart cards for use in such applications as SIM cards in mobile phones. Financial details of the collaboration and of the supply agreement were not disclosed.

"Our partnership with world leaders in semiconductors and system solutions and using the newest technological developments will enable us to effectively develop modern chip packaging technologies at KNC," said Alexander Goncharuk, KNCs CEO after the agreements signing ceremony. "Cooperation with Infineon is our next step in the field of microelectronics. We are actively developing Russian and CIS smart cards markets which require state-of-the-art technologies."

Andreas Liebheit, vice president at Infineons Chip Card and Security ICs business unit, said: "The Russian SIM card market, both strong in volumes as well as fast in migration to high-value SIM cards, needs dedicated local engagement and this cooperation with KNC is most promising as they are the strongest Russian supplier in the telecom industry

"This is why Infineon concentrates its work together with KNC in this field as a first step; however, we plan to enlarge this co-operation to other applications, such as payment and health care and social insurance cards!

New video technology to spur new products

In press conferences at four cities around the world Texas Instruments (TI) announced a new digital video platform that they hope create a flurry of new products using digital video technology. Unlike past economic growth spurts there is no killer application on the horizon and the semiconductor industry is looking for activities that will increase consumer spending in electronics.

Rich Templeton, president and CEO of'TI introduced DaVinci, advanced semiconductor technology for next generations of digital video products. DaVinci technology is a DSP-based solution tailored for digital video applications that provides video equipment manufacturers with integrated processors, software and tools to simplify the design process and accelerate innovation. DaVinci will allow digital video designers to choose a signal processor tailored for their needs and then select from a menu of production ready software, reducing time to market and increasing innovation by an order of magnitude. For consumers, these advancements will potentially result in new generations of digital video products that go far beyond today's capabilities. For example, consumers will no longer have to correct colour and lighting problems on a digital photo using their PC; those corrections will be done automatically by the camera. Instead of multiple systems, one TV set-top box will allow consumers to play and/or record, as well as video conference with friends simultaneously. Taking this technology one step further, consumers with a video security system will be able to identify a visitor at the front door, unlock it and open it via their TV remote.

TI expects to announce DaVinci-basecl processor samples, software and development tools by year-end 2005. DaVinci-enabled solutions are in the pipeline for products such as digital cameras, automotive infotainment products, portable media players, set-top boxes and video security systems.

IBM and AMD extend research alliance until 2011

Major US chip makers AMD and IBM have broadened the scope of their technology alliance. The expanded alliance now includes early exploratory research of new transistor, interconnect, lithography, and die-to-package connection technologies through to 2011.

The agreement marks the first time a member of a technology development alliance will work directly with IBM's Research Division on R&D, electronic materials and basic feasibility studies three-to-five years before commercialisation.

Furthermore, the extended duration of the alliance makes it one of the longest IBM currently has with any of its semiconductor alliance associates.

Early exploratory research is a critical part of microprocessor Research and development. This collaboration will enable both companies to identify and investigate future technology challenges earlier, allowing solutions to be found and fundamental technology choices to be made sooner.

"The industry-leading performance, power-efficiency and function of our AMD64 processors is made possible through a constant, uninterrupted cycle of improvements to our integrated circuit process technologies," said Craig Sander, corporate vice president of technology development at AMD.

"By expanding our successful IBM alliance, we can significantly increase our level of early-stage research, focusing on technologies for the 32nm and 22nm technology generations. By influencing and participating in this research, AMD can better align its process technologies with the needs of our products scheduled to be introduced late in this decade and beyond."

Bernie Meyerson, IBM vice president and chief technologist, said: "This agreement is a perfect example of IBM's strategy of collaborative Innovation.

"Working closely with our key development associates like AMD, we are able to bring advanced technology to market faster and more economically, providing added benefit to our customers."

Research and development as part of the alliance will take place in IBM's Watson Research Center in New York, the newly announced Center for Semiconductor Research at Albany NanoTech, and at IBM's 300mm manufacturing facility in East Fishkill.

Slow light could speed up electronic devices

Researchers from IBM have created a tiny device that could pave the way for far faster communication between electronic components through the use of light rather than electricity.

The company's scientists have managed to slow light down to less than 1/300th of its usual speed by directing it down a carefully designed channel of perforated silicon called a "photonic crystal waveguide".

The unique design of the device allows the light's speed to be varied over a wide range simply by applying an electrical voltage to the waveguide.

Researchers have known for some years how to slow light to a crawl under laboratory conditions, but actively controlling the light speed on a silicon chip, using standard silicon with standard micro- and nanoelectronic fabrication technology, is a first.

The device's small size, use of standard semiconductor materials, and ability to more closely control this "slow light" could make the technology useful for building ultra-compact optical communications circuits that are practical for integration into computer systems.

The inability to move information quickly around within electronic systems is one of the biggest bottlenecks in electronic design today. This work by IBM could help solve the problem.

AMD's FAB 36 opens in Dresden

AMD has opened its latest 300mm wafer fab in Dresden in a ceremony attended by Semiconductor leaders and the cream of Germany's political world, demonstrating the strong relationship the company has with the Saxony region.

With the production ramp in Fab 36 progressing on schedule, the company intends to make 90nm production shipments in the first quarter of 2006 and begin 65nm production by the end of 2006. AMD has set a goal to be substantially converted to 65nm in Fab 36 by mid-2007.

"The on-schedule, on-plan opening of Fab 36 is the latest achievement in AMD's growing track record of execution on our manufacturing strategies and goals," said Hector Ruiz, chairman of the board, president and chief executive officer of AMD. "In AMD Fab 30, using our patented Automated Precision Manufacturing (ARM) capabilities, we have had tremendous success in rapidly transitioning to new technology generations and quickly achieving mature yields."

Capacity gained through the use of larger 300mm wafers, combined with the speed and efficiencies enabled by ARM, plays a fundamental role in the company's growth plans for the next several years. Now in its third generation, ARM consists of hundreds of AMD patented and patent-pending technologies that dynamically and automatically optimize fab operations. This unique automated decision-making capability has allowed AMD to accelerate its responsiveness to customer needs, more quickly transition to new technologies, improve quality and operate at increasing levels of efficiency.

AMD's presence in Dresden has been a tremendous mutual success for the company, the Free State of Saxony, Germany and the European Union.

AMD's investment in the region, one of the largest foreign investments in Germany within the last decade, has created approximately 7,000 direct and indirect jobs in Saxony and the surrounding regions. It has been instrumental in establishing Dresden as the thriving centre for semiconductor innovation in the EU.

Soitec and SEZ collaborate on SOI

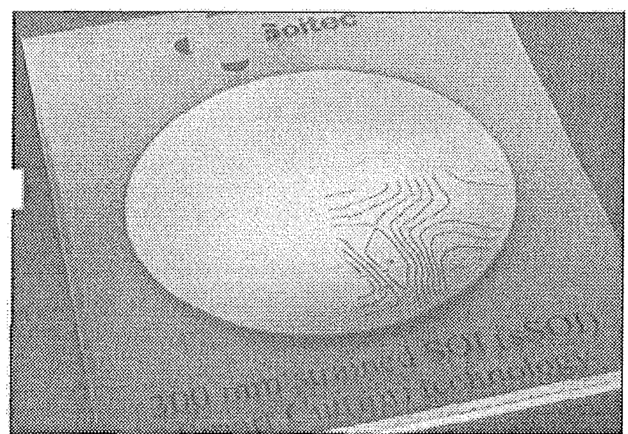
Soitec Group and SEZ have announced they have initiated a joint development program (JDP) intended to speed the industrialization of next-generation strained silicon-on-insulator (sSOI) substrates. Under the terms of the JDP, the two companies will leverage Soitecs engineered substrates and SEZs single-water, wet-processing technology to develop new wet-etch processes designed to optimize total germanium removal in sSOI manufacturing.

Company officials report that effective and complete removal of germanium is a key step in the sSOI manufacturing process as silicon germanium (SiGe) must be used to produce the silicon-layer strain that is essential to sSOIs functionality. Ultimately, it is the combined power of this strained silicon layer and the SOI substrates that allow chipmakers to harness the powerful performance and power dissipation benefits afforded by sSOI substrates.

Key to this, single-wafer processing has emerged as a promising solution for enabling selective control during the germanium etching process-removing only the desired material without damaging underlying material layers.

According to Carlos Mazure, Soitecs chief technology officer, "This joint work is another step in Soitecs strategy to build infrastructure that will ensure future generations of sSOI substrates. SEZs single-wafer technology offers benefits for selective etch of SiGe that allows more efficient germanium removal."

"We are pleased to be entering into this collaborative effort with Soitec," stated Dr. Gerald Wagner, director of process development for SEZ. "SEZ is continually involved in research and development surrounding new materials and process solutions. Working with Soitec will enable us to access their extensive expertise in sSOI and other advanced substrates. We plan to develop a new process application that may prove essential to producing sSOI."



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