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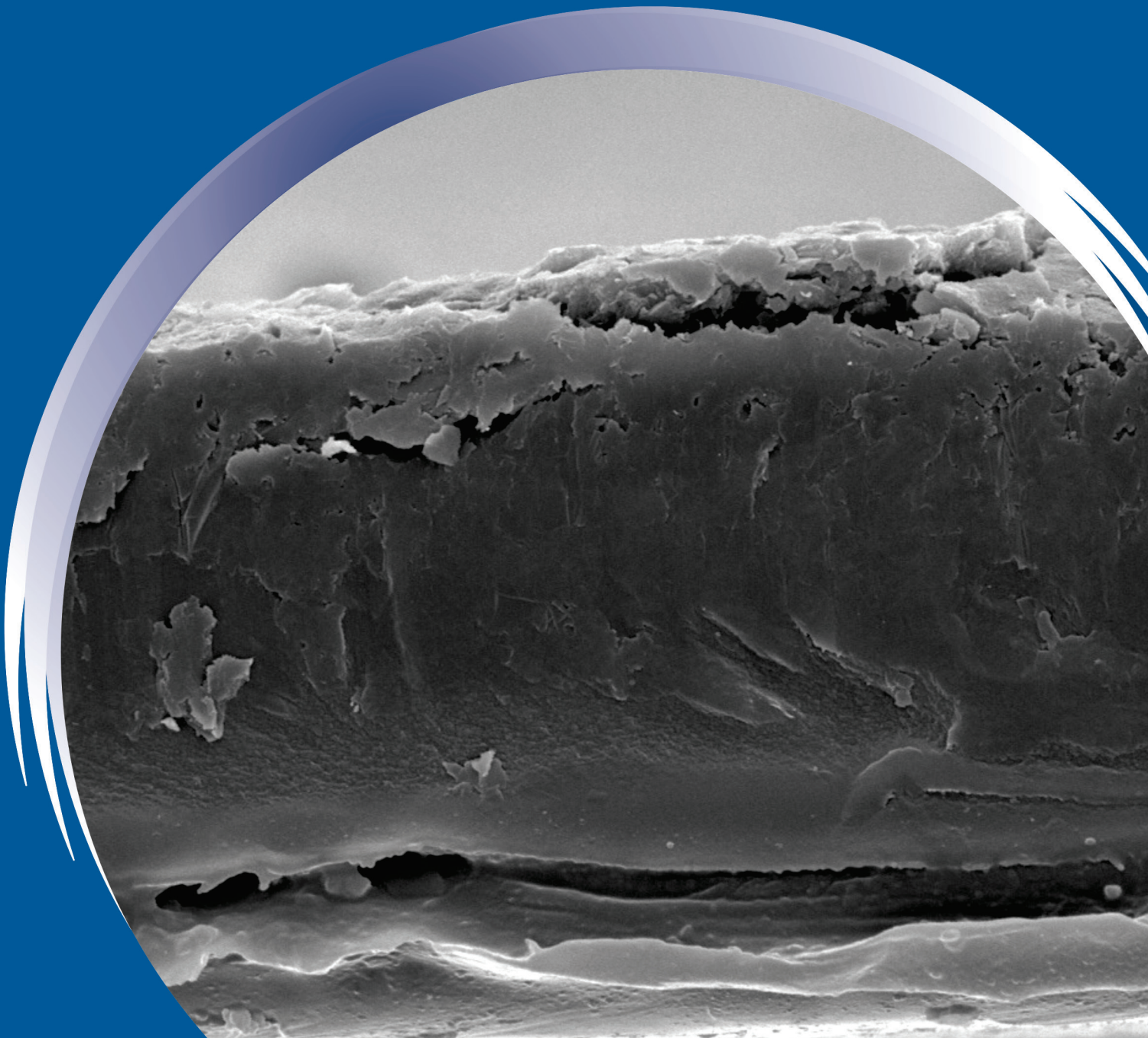

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Content | Vsebina

Original scientific paper | Izvirni znanstveni članki

Editorial | Uvodnik

Dear Reader,

This issue brings 6 original scientific papers and the Call for paper at the 53rd MIDEM conference that the MIDEM Society organizes in late September/early October every year. The conference will be organized at the largest research institute in Slovenia, the Jozef Stefan Institute in Ljubljana. Among highlights of the conference will be the Workshop on Materials for Energy Conversion and their Applications: Electrocalorics and Thermoelectrics. The organizers invite you to join us at the inspiring invited talks and full three-day programme. Readers of the journal will get a chance to read selected papers from the conference in coming Issue 4 in December.

The landscape of academic journals started to change since 2002, when the Budapest Open Access Initiative has been released. Fifteen years later we can state that it did not change dramatically, but brought new players – publishers, policy makers, charitable foundations, scholarly collaboration networks and additional authors and reviewers. European Commission urges that dissemination of knowledge generated with EU funding needs to follow open access. All peer-reviewed scientific publications relating to the projects funded within Horizon 2020 programme must be published as green or gold open access. Member states follow and Slovenia is no exception. Science Europe committed to playing a role in accomplishing the transition to Open Access in an efficient and sustainable way. It recommends that scientific institutions disclose payments of Open Access publication fees by participating in the 'Open APC Initiative'. This will help create a more transparent cost structure in the Open Access publication market and stimulate competition.

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Original scientific paper

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Investigations on the Influence of Selected Factors on Thermal Parameters of Impulse-Transformers

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Abstract: In the paper the results of experimental investigations illustrating the influence of the selected factors on parameters of the thermal model of the transformer are presented. The form of this model and the applied method of measurements of the transformer structural components' self and mutual transient thermal impedances are described. The influence of the selection of material of the core, its geometrical dimensions, spatial orientation, shape of the core, frequency of the primary winding current in the transformer and power lost in this element on the considered thermal parameters of the transformer are discussed. An analytical formula describing the dependence of the considered transient thermal impedances on the internal temperature of the windings is proposed and verified experimentally.

Keywords: thermal parameters;selfheating; impulse-transformers

Vplivi izbranih parametrov na termične parametre impulznih transformatorjev

Izvleček: Članek prikazuje rezultate eksperimentalnih raziskav vplivov izbranih faktorjev na parameter termičnega modela transformatorja. Opisan je model, uporabljene merilne metode in vzajemne tranzientne termične impedance. V smislu termičnih parametrov so obravnavni: izbira materiala jedra, geometrija, orientiranost, frekvenca toka primarnega navitja in izgube. Predlagana in eksperimentalno preverjena je analitična enačba odvisnosti tranzientne termične impedance od temperature navitja.

Ključne besede: termični parametri; lastno segrevanje; impulzni transformator

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1 Introduction

Impulse-transformers are commonly used in switched-mode power electronic converters [1, 2, 3, 4]. The considered elements have a simple construction - they consist of the ferromagnetic core and windings. The properties of both these components influence temperature, the change of which causes changes of the value of technical parameters of the core and windings [4, 5]. Particularly, when the core temperature is higher than the Curie temperature, magnetic permeability of the ferromagnetic core decreases to the value near permeability of free air, and the transformer practically does not transfer energy from the input to the output. In turn, the excess of the admissible temperature of windings can cause destruction of isolation of winding wires [4, 5], leading to the short-circuit of turns.

The temperatures of the core and windings of the transformer during its operation are higher than the ambient temperature as a result of self-heating in the core and in the winding [5-14], as well as mutual thermal coupling between them. Calculating values of temperature of structural components of the transformer demands using the thermal model. Such a model can have the form of the detailed model, making it possible to calculate time-space distribution of temperature in the considered element [9-12, 15], or the compact model - making possible calculations of waveforms of temperature of this element [6, 13, 14] or the selected structural components of the transformer [5, 7]. In the paper [13] many results of calculations of temperature distribution in a planar transformer obtained with the use of the finite element method (FEM) are presented. In these calculations uniform distributions of the pow-

er dissipated in the core and in the windings were assumed. The results of measurements shown in this paper prove that this assumption is fulfilled.

In the case of the use of the compact thermal model it is indispensable to measure the transformer's self and mutual transient thermal impedances. Thermal models presented in papers [5, 6, 7, 8, 13] are linear models, i.e. transient thermal impedances in these models neither depend on constructional factors nor on the power lost in the transformer. Yet, in papers [16, 17, 18] (for instance) it was shown that thermal parameters of semiconductor devices strongly depended, among other things, on the power dissipated in them, the type of the case, or the manner of mounting the considered device. It can be expected that a similar influence will be observed in the case of magnetic elements, to which the transformer belongs.

In the paper the method to measure thermal parameters existing in the thermal model of the transformer and the results of measurements of these parameters illustrating the influence of the selected factors on efficiency of transformers cooling are presented. Transformers with ring cores considered in the present paper are characterized by uniform distribution of the magnetic force and magnetic flux density, similarly as transformers considered in paper [13]. Therefore, distribution of power density in the core is also uniform.

In Section 2 the form of the thermal model of the transformer is presented and the transformer's self and mutual transient thermal impedances are defined. Section 3 contains a description of the measuring method to measure the transformer's self and mutual transient thermal impedances. In Section 4 the results of measurements of thermal parameters of the selected constructions of transformers are presented and the analytical formula describing the influence of the dissipated power on the considered parameters is proposed and experimentally verified.

2 Thermal Model of Transformer

The thermal model describes the dependence of the internal temperature of the electronic component on the power emitted in it. In the case of commonly used compact thermal models this dependence can be described by means of the convolution integral [19, 20, 21]. As it is shown, among other things, in papers [5, 7, 22], in order to describe correctly thermal properties of magnetic elements it is indispensable to take into account both self-heating in the core and in windings, as well as mutual thermal coupling between them. Hence, the temperature of k-th winding can be described by the following formula

$$T_{wk}(t) = T_a + \sum_{j=1}^{n} \int_0^t Z'_{thwkj}(t) \cdot p_j(t-\tau) d\tau + \\ + \int_0^t Z'_{thck}(t) \cdot p_c(t-\tau) d\tau \tag{1}$$

where T_a denotes the ambient temperature, k represents the name of the winding, $p_k(t)$ denotes the power dissipated in k-th winding of the transformer and $Z'_{thwkj}(t)$ represents the time derivative of the devices' self (for k = j) or mutual (for k ≠ j) transient thermal impedance between the windings of the transformer, n – the number of windings, $Z'_{thck}(t)$ – the time derivative of mutual transient thermal impedance between the core and the k-th winding, whereas $p_c(t)$ is the power dissipated in the core.

In turn, the temperature of the core is given by the following formula

$$T_c(t) = T_a + \sum_{j=1}^{n} \int_0^t Z'_{thcj}(t) \cdot p_j(t-\tau) d\tau + \\ + \int_0^t Z'_{thc}(t) \cdot p_c(t-\tau) d\tau \tag{2}$$

where $Z'_{thc}(t)$ is the time derivative of the core's self transient thermal impedance.

The core's self or mutual transient thermal impedance can be modelled using the classical formula [19, 23, 24]

$$Z_{th}(t) = R_{th} \cdot \left[1 - \sum_{k=1}^{N} a_k \cdot \exp\left(-\frac{t}{\tau_{thk}} \right) \right] \tag{3}$$

where R_{th} is thermal resistance, τ_{thk} denotes k-th thermal time constant, a_k is the ratio factor corresponding to this time constant, whereas N is the number of thermal time constants.

The presented thermal model, given by equations (1 – 3) of the transformer can be described as the RC electrical analog, like the linear thermal model presented in [5]. In the real situation, where the parameters existing in Eq. (3) depend on the value of the dissipated power, the nonlinear thermal model is needed. The simple form of this model for the electronic device non-coupled thermally with any other device is proposed in [17]. In this model, the controlled voltage and current sources are used instead of RC elements.

3 Method to Measure Thermal Parameters of the Transformer

The transformer's self and mutual transient thermal impedances of the selected magnetic devices were measured with the use of the method described in papers [25, 26]. This method is realised by means of the measurement set presented in Fig.1.

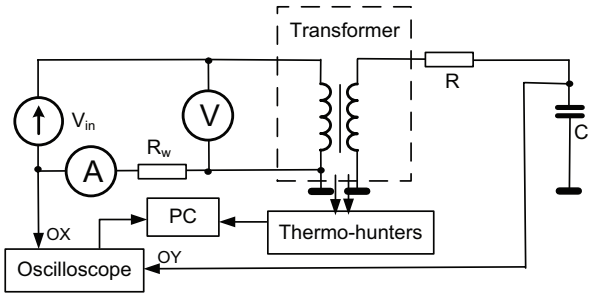


Figure 1: Measurement set for measuring thermal parameters of the transformer [26]

The measurements are realised in two steps. The first step needs stimulations of the primary winding with a current step and the measurement of waveforms of the windings temperature and the core temperature by means of thermo-hunters (pyrometers with IR sensors) until the thermally steady-state is achieved. In the considered measurement set the thermo-hunters of the type PT-3S by Optex are used [27]. The range of the measured temperature is from 0 to 200 °C and the resolution is equal to 0.1°C. These thermo-hunters are situated in the distance of 25 mm from the measured transformer. The area, on which the temperature is measured, has the form of a circle with the diameter 2.5 mm. During measurements it was assumed that emissivity of all components of the considered transformers has the constant value equal to 0.95. This value is close to typical values of emissivity of materials used to construct transformers.

As it results from the Authors' investigations presented in [26], in the area of a transformer, in which the windings are located, practically uniform distribution of the temperature is observed. Similarly, temperature distribution of the core is quasi-uniform. Therefore, averaging the temperature value in a circle of the diameter equal to 2.5 mm does not cause a visible measurement error.

The waveforms of the core temperatures $T_C(t)$ and of the winding temperature $T_W(t)$ while heating the transformer are registered by the computer PC coupled with two thermo-hunters. By means of the voltmeter and the ammeter the values of the voltage on the primary winding V_1 and the current of this winding I_1 are measured at the steady-state. The results of these measurements are used to calculate transient thermal impedance of the winding $Z_{thW}(t)$ and mutual transient thermal impedance between the core and the windings $Z_{thWC}(t)$ with the following formulas

$$Z_{thW}(t) = \frac{T_W(t) - T_a}{V_1 \cdot I_1} \tag{4}$$

$$Z_{thWC}(t) = \frac{T_C(t) - T_a}{V_1 \cdot I_1} \tag{5}$$

where T_a is the ambient temperature.

In the second step, the primary winding of the transformer is stimulated by a sinusoidal signal of frequency f_s, whereas the temperature of the core is measured by the thermo-hunter. When the steady state is obtained, the hysteresis loop of the magnetising characteristic B(H) of the core is measured using the oscilloscope and next - transmitted to the computer (PC).

The waveforms of the magnetic force H(t) and flux density B(t) are calculated using the following formulas

$$B(t) = \frac{R \cdot C \cdot u_C(t)}{z_2 \cdot S_{Fe}} \tag{6}$$

$$H(t) = \frac{z_1 \cdot i_1(t)}{l_{Fe}} \tag{7}$$

in which R and C denote resistance of the resistor and capacitance of the capacitor used in Fig.1, respectively, z_1 and z_2 are numbers of turns in primary and secondary windings, respectively, S_{Fe} – the cross-section area of the core, l_{Fe} – magnetic path in the core, u_C – voltage on the capacitor C, whereas i_1 – the current of the primary winding.

The area S_H of the obtained hysteresis loop B(H) is given by following formula

$$S_H = \oint B dH \tag{8}$$

This integral is calculated using the Excel software and the method of numerical integration. The used values of frequency f_s are in the range from 1 kHz to 100 kHz. Next, in the moment t = 0 the power supply of the primary winding is switched off and waveforms of the core temperature $T_C(t)$ are measured until the steady state is obtained. The transient thermal impedance of the core $Z_{thC}(t)$ is calculated using the following formula

$$Z_{thC}(t)=\frac{T_C(t=0)-T_C(t)}{V_C\cdot f_s\cdot S_H} \tag{9}$$

where V_C represents volume of the core. In Eq. (9) only the power dissipated in the core is taken into account, whereas the power dissipated in the windings is omitted. This is justified, if the value of the power dissipated in primary and secondary windings is much smaller than the power dissipated in the core. Such conditions are fulfilled when

$$S_H\cdot f\cdot V_C >> I_1^2\cdot R_1+I_2^2\cdot R_2 \tag{10}$$

where I_1 and I_2 are RMS values of primary and secondary windings currents, whereas R_1 and R_2 are resistances of these windings.

4 Investigation Results

Using the method presented in Section 3, measurements of thermal parameters of transformers containing ferromagnetic cores made of the powdered iron (RTP), the ferrite (RTF) and the nanocrystalline cores (RTN) were performed.

The first series of measurements was performed for ring cores of the dimensions RTP 26.9x14x11 made of material T106-26, RTN-26x16x12 made of material M-070, RTF-25x15x10 made of material F-867, called in the further part of this paper small ring cores. The second series of measurements was made for cores made of the same ferromagnetic materials, but of the bigger dimensions: RTP 39.9x24.1x14.5 made of material T157-26, RTF 40x24x16 made of material F-867, called in the further part of this paper large ring cores and for the pot core B65701 -T1000-A48 of the diameter 30 mm and heights 19 mm made of material N48. In Table 1 the values of basic parameters of the considered ferromagnetic materials are collected. In this table B_{sat} denotes saturation flux density at the magnetic field strength H_{sat}, H_C is the coercive field strength, T_C – Curie temperature, whereas P_V – relative core losses.

In marking ring cores each number means the outside diameter, the inside diameter and the height of the core expressed in millimetres, respectively. The view of the ring core with its dimensions is shown in Fig. 2, whereas the view of the pot core is shown in Fig. 3. The temperature of windings of the transformer with the pot core can be measured using a hole in this core.

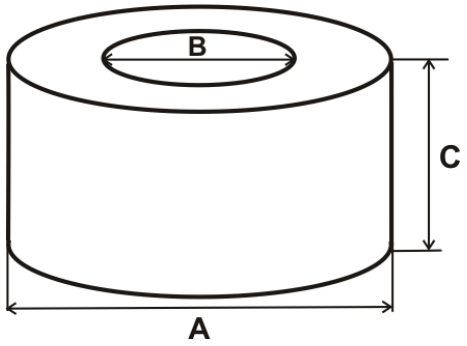


Figure 2: View of the ring core with its dimensions

On small ring cores two windings containing 22 turns were wound with copper wire in the enamel of the diameter 0.8 mm. In turn, on large ring cores two windings containing 30 turns of copper wire in the enamel of the diameter 0.8 mm were wound. The transformer with the pot core contains two windings made with the same wire consisting of 22 turns. The views of transformers with the ring core and with the pot core are shown in Fig. 4 and Fig. 5, respectively.

As it is visible, the distance between turns in each winding is not constant. The temperature of these windings is measured for the area in which this distance is the smallest and much smaller the measuring spot of the used thermo-hunter.

In the following figures the results of measurements of self and mutual transient thermal impedances $Z_{th}(t)$ of the selected constructions of impulse transformers (solid lines) and approximation of these curves (dashed lines) with Eq. (3) are presented. The values of parameters of the model described with the equation (3) are estimated with the use of the method proposed in [5]. The value of R_{th} is estimated by averaging the wave-

Table 1: Values of basic parameters of the considered ferromagnetic materials

parameter	T106-26 and T157-26	M-070	F-867	N48
manufacturer	Micrometals	Magnetec	Feryster	Epcos
B_{sat} [T]	1.38	1.2	0.5	0.42
H_{sat} [A/m]	19.9x103	590	966	1200
H_C [A/m]	440	9	75	26
T_C [°C]	750	600	215	170
P_V [kW/m^3]	180 @f=100 kHz	800 @f=100 kHz	400 @f=100 kHz	-

form of the considered transient thermal impedance in the steady state (typically for the last 100 seconds), whereas the values of the parameters a_i and thermal time constants t_{thi} are determined by the least square method. Starting from the longest thermal time constant through approximation based on the formula [5]

$$y_i(t) = \ln\left(1 - \frac{Z_{th}(t)}{R_{th}} - \sum_{j=1}^{i-1} a_j \cdot \exp\left(-\frac{t}{\tau_{thj}}\right)\right) \quad (11)$$

the linear function given by

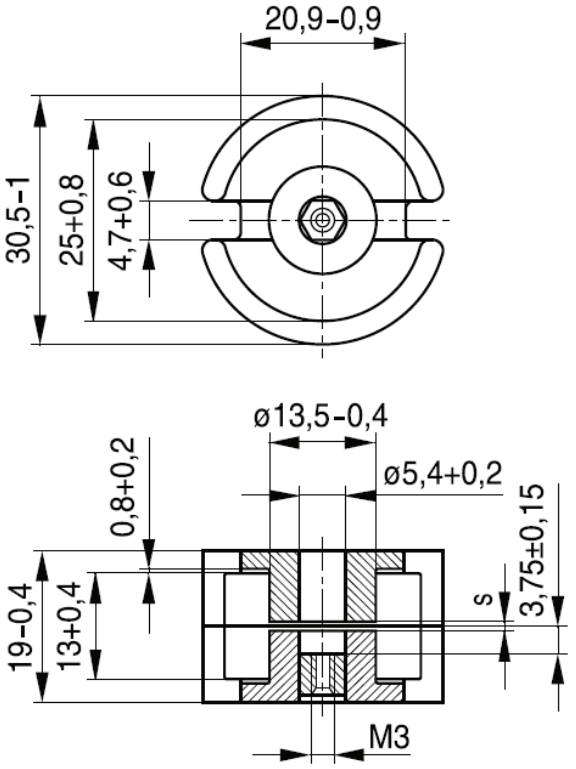


Figure 3: Cross-sections of the pot core B65701 -T1000-A48 with its dimensions

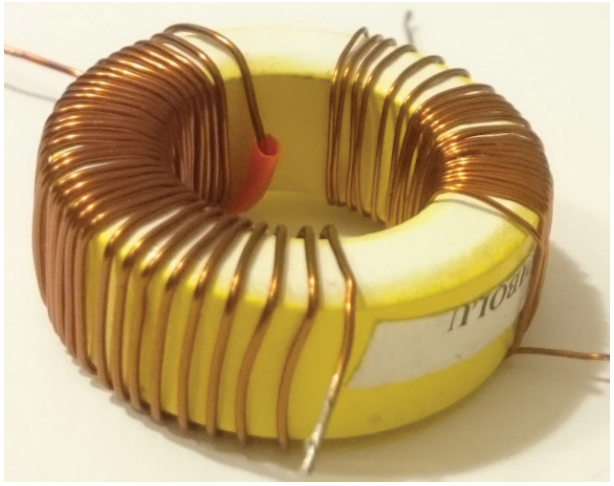


Figure 4: View of the transformer with the ring core

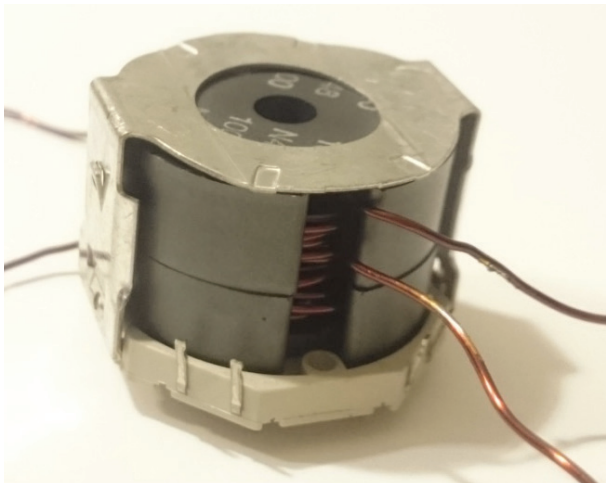


Figure 5: View of the transformer with the pot core

$$y_i(t) = -\frac{t}{\tau_{thi}} + \ln(a_i) \quad (12)$$

is used.

Attention is focused on the parameters describing self-heating phenomenon in the core ($Z_{thC}(t)$) and in the winding ($Z_{thW}(t)$), as well as mutual thermal coupling between the core and the windings ($Z_{thWC}(t)$). The mutual thermal couplings between the windings are not taken into account.

The values of parameters R_{th}, a_i, τ_{thi} approximating the selected waveforms of the investigated transformers' self and mutual transient thermal impedances are collected in Tables 2 - 5.

Table 2: Parameters values of transient thermal impedances in transformers with the small ring core RTP situated horizontally

parameter	$Z_{thW}(t)$	$Z_{thWC}(t)$	$Z_{thC}(t)$
R_{th} [K/W]	22.15	18.12	25.39
a_1	0.664	0.758	0.925
a_2	0.206	0.242	0.068
a_3	0.13		0.007
τ_{th1} [s]	661.2	710.5	702.1
τ_{th2} [s]	134.1	259	283
τ_{th3} [s]	10		12.8

Table 3: Parameters values of transient thermal impedances in transformers with the big ring core RTP

orientation	horizontally		vertically	
parameter	$Z_{thW}(t)$	$Z_{thWC}(t)$	$Z_{thW}(t)$	$Z_{thWC}(t)$
R_{th} [K/W]	13.5	11.1	11.1	9.01
a_1	0.6	0.774	0.742	1
a_2	0.192	0.226	0.118	
a_3	0.148		0.09	
a_4	0.06		0.05	
τ_{th1} [s]	1062.5	1078.4	680.1	654.9
τ_{th2} [s]	470.5	459.4	114.8	
τ_{th3} [s]	30.9		19.4	
τ_{th4} [s]	5.64		14.7	

Table 4: Parameters values of transient thermal impedances in transformers with the small ring core RTF

parameter	$Z_{thW}(t)$	$Z_{thWC}(t)$	$Z_{thC}(t)$
R_{th} [K/W]	24.88	14.26	11.98
a_1	0.651	1	0.92
a_2	0.255		0.08
a_3	0.094		
τ_{th1} [s]	474.1	449.5	483.4
τ_{th2} [s]	126.8		53.1
τ_{th3} [s]	9		

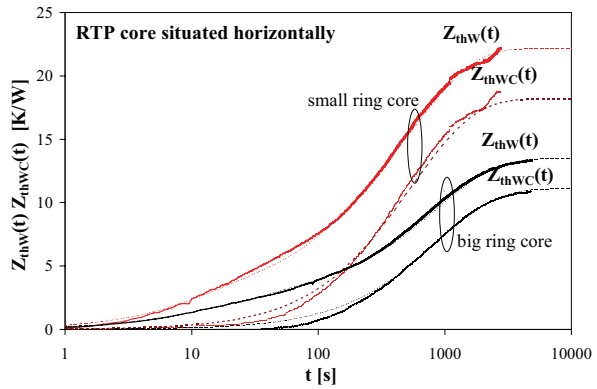
Table 5: Parameters values of transient thermal impedances in transformers with the big ring core RTF

orientation	horizontally		vertically	
parameter	$Z_{thW}(t)$	$Z_{thWC}(t)$	$Z_{thW}(t)$	$Z_{thWC}(t)$
R_{th} [K/W]	14	7.59	13.42	6
a_1	0.595	1	0.605	1
a_2	0.225		0.275	
a_3	0.13		0.118	
a_4	0.05		0.002	
τ_{th1} [s]	918	1050.5	792.8	800
τ_{th2} [s]	224.8		152.8	
τ_{th3} [s]	23.5		11.18	
τ_{th4} [s]	5.67		5.67	

Comparing the data collected in the mentioned tables one can observe that the description of the considered transient thermal impedances demands the use of a different number of thermal time constants τ_{thi}. In the case of large ring cores RTP and RTF up to 4 thermal time constants appear in the description $Z_{thW}(t)$, while in the description $Z_{thWC}(t)$ for both ferrite cores RTF - just only one thermal time constant. In all the considered cases the prevailing meaning has the longest thermal time constant τ_{th1}. The corresponding to it weight- coefficient a_1 assumes the values in the range from 0.595 to 1. In turn, the values τ_{h1} are in the range from 471 s (for the small ring core RTF) to 1078 s for the large ring core RTP.

The presented below results of investigations illustrate the influence of geometrical dimensions of the core (Fig.6), its spatial orientation (Fig. 7), shape of the core (Fig. 8), current of the primary winding (Fig. 9), material the core is made of (Fig. 10) and frequency of the current on the primary winding (Fig. 7) on waveforms of the transformers' self and mutual transient thermal impedances.

In Fig. 6 the measured and modelled with the Eq. (3) waveforms of transient thermal impedance of the winding $Z_{thW}(t)$ and mutual transient thermal impedance between the winding and the core $Z_{thWC}(t)$ for transformers containing ring cores RTP (Fig.6a) or ring cores RTF (Fig. 6b) of different dimensions are presented. The measurements were performed at the stimulation of the primary winding with the direct current of the value equal to 9 A.



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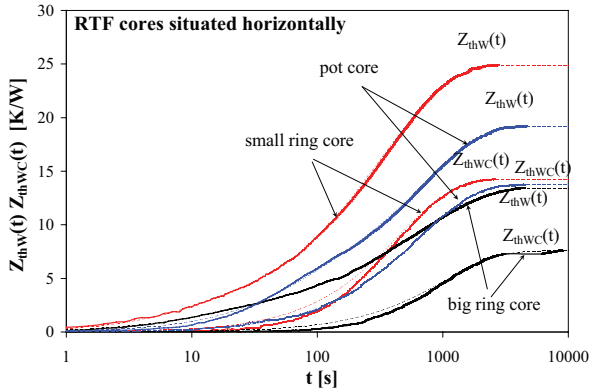
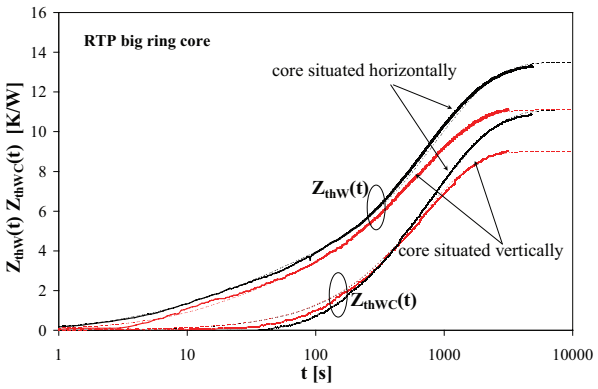


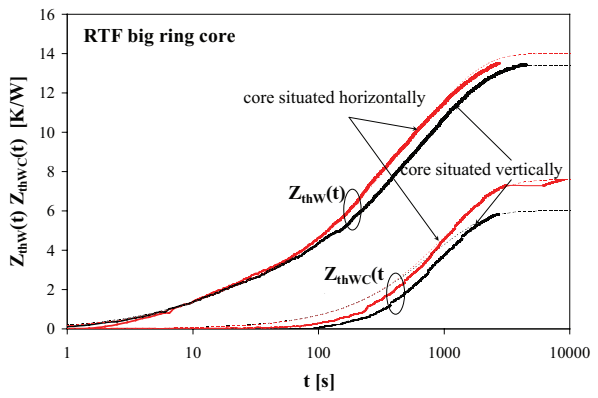
b)

Figure 6: Measured (solid lines) and modelled (dashed lines) waveforms of transient thermal impedances in transformers with ring cores RTP (and) and RTF (b) of different dimensions at the stimulation with the direct current of the primary winding and the horizontal orientation of the core

As one can notice in Fig. 6, the process of heating the core and the winding of the transformer with the considered cores runs slowly. The time indispensable to obtain the steady state exceeds 3000 s for the small ring core, 4000 s - for the pot core and 5000s - for the large ring core. The value of transient thermal impedances $Z_{thW}(t)$ is about 40% greater for the transformer with the small ring core RTP than for the transformer with the large ring core RTP (Fig. 6a). In the case of the transformer with the core RTF (Fig. 6a) one obtained greater by about 10% values of the considered parameter for transformers with ring cores made of the same material, while the transformer with the pot core shows average values of the time needed to settle the course between the values of this parameter corresponding to different measurements of ring cores. Waveforms of mutual transient thermal impedance between the winding and the core $Z_{thWC}(t)$ are late in relation to waveforms $Z_{thW}(t)$ by more than 20 s, and values $Z_{thWC}(t)$ at the steady-state are smaller than the value $Z_{thW}(t)$ at the steady-state. For transformers with cores RTP this difference is about 15%, and in the case of transformers with cores RTF these differences are bigger and are



a)



b)

Figure 7: Measured (solid lines) and modelled (dashed lines) waveforms of transient thermal impedances in the transformer with the core RTP (and) and RTF (b) at the stimulation with the direct current in the vertical and horizontal orientation of transformers

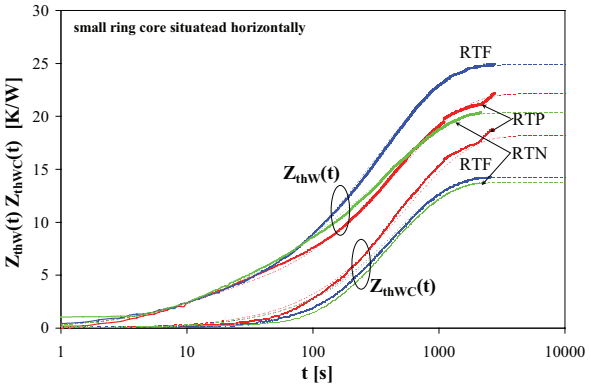
about 50% for ring cores and about 30% for the sot core. For all the considered waveforms the very good agreement between the results of measurements and the calculations performed with the use of the considered model is obtained.

In Fig. 7 waveforms $Z_{thW}(t)$ and $Z_{thWC}(t)$ for transformers with large ring cores RTP (Fig. 7a) and RTF (Fig.7b) placed both horizontally and vertically at the stimulation of the primary winding with the direct current of the value 9 A are presented.

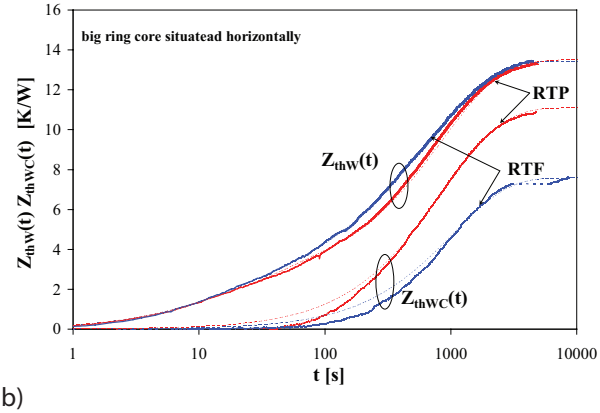
As one should expect the waveforms $Z_{thW}(t)$ and $Z_{thWC}(t)$ obtained in horizontal orientations lie above the waveforms obtained for the transformers situated vertically. It is the result of more efficient convection of heat for elements situated vertically, similarly to the situation with transistors mounted on any heat-sink situated vertically [9]. The vertical orientation of the considered elements quickens the perpendicular air flow along the sides of these elements, because the length of these sides is greater at this arrangement of the investigated element. The values of the considered transient thermal impedances in the steady-state in the horizontal and vertical orientation differ from each other by about 15% for the transformer with the core RTP and by about 10% for the transformer with the core RTF. It is visible that the considered model approximates well the measured waveforms $Z_{thW}(t)$, whereas it is possible to observe divergences between the measured and approximated waveforms $Z_{thWC}(t)$, especially for small values of time t.

In Fig.8 the influence of the selection of material of the ferromagnetic core on waveforms $Z_{thW}(t)$ and $Z_{thWC}(t)$ of transformers containing the small (Fig. 8a) or large (Fig. 8b) ring core is illustrated. The measurements were performed at the stimulation of the primary winding with the direct current of the value 9A.

As it can be noticed in Fig.8a, heat removal from the transformer containing the ferrite core (RTF) is the least efficient, while transformers with the powder core (RTP) and nanocrystalline core (RTN) have almost identical waveforms $Z_{thW}(t)$. It is worth noticing that dissipation of power of the same value in the winding causes a considerably higher temperature increase of the core RTP than the remaining cores, considered in this paper. This results from the greater value of thermal conductance of this material, which causes more efficient removal of heat generated in the winding through the core. Therefore, in the transformer with this core considerably smaller differences appear between temperatures of the winding and of the core than for the remaining considered transformers. The qualitatively similar results were obtained for transformers containing the large ring core. In this case, increases of the



a)



b)

Figure 8: Measured (solid lines) and modelled (dashed lines) waveforms of transient thermal impedances of transformers with the small (a) or large (b) ring core made of different materials

winding and the core temperatures of the transformer with the core RTP differ only just by about 20%, and for the transformer with the core RTF – up to about 60%.

In Fig. 9 the influence of the current flowing through the primary winding of the transformer on waveforms of transient thermal impedance of the winding and mutual thermal impedance between the winding and the core was illustrated. The measurements were performed for the transformer with the large ring core RTP situated horizontally for the current equal 7.35A and 9.1A, respectively.

As one can notice, with the current of the primary winding of the value 9.1A the values $Z_{thW}(t)$ and $Z_{thWC}(t)$ are by about 8% smaller than with the current equal to 7.35A. The improvement of efficiency of cooling with an increase of the current of the winding results from an increase in the value of the power dissipated in this element, which causes a temperature rise of the winding. In turn, the temperature rise of the winding causes an increase in efficiency of heat convection.

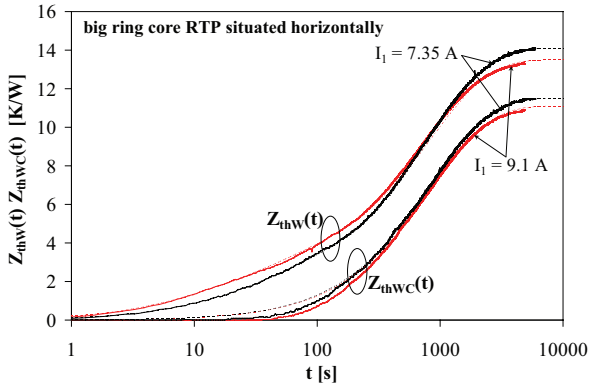


Figure 9: Measured (solid lines) and modelled (dashed lines) waveforms of transient thermal impedances of transformers with the large ring core RTP at the stimulation with the direct current of different values

Fig. 10 illustrates the influence of the shape of the waveforms $Z_{thC}(t)$ of the transformer with the core RTF at the stimulation of the primary winding with the sinusoidal signal. In this case the power dissipated in the winding is negligible in relation to the power dissipated in the core.

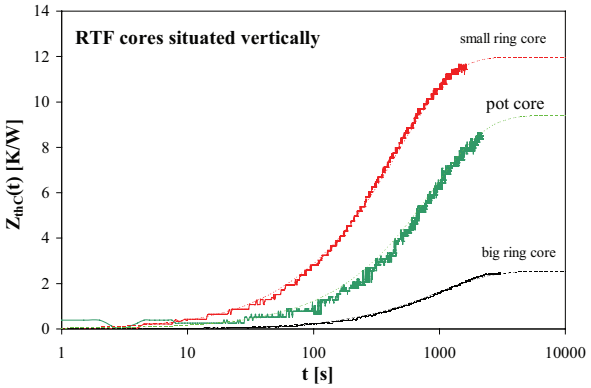


Figure 10: Measured (solid lines) and modelled (dashed lines) waveforms of transient thermal impedance of the core of transformers with the core RTF at the stimulation with the sinusoidal current

In Fig. 10 distinct differentiation of the obtained waveforms $Z_{thC}(t)$ is visible. The large ring core assures the most efficient cooling and the small ring core - the least efficient. The average values $Z_{thC}(t)$ are obtained for the transformer with the pot core. The obtained values of the considered transient thermal impedance differ from each other even four times.

In Fig. 11 the influence of frequency of the signal stimulating the primary winding of the transformer with the large ring core RTP on the waveforms $Z_{thC}(t)$ and $Z_{thCW}(t)$ is illustrated. Investigations were made for the transformer placed horizontally at two values of frequency equal to 25kHz and 75kHz, respectively. It is visible that an increase

of frequency of the stimulating signal from 25 kHz to 75 kHz causes an increase in the value of transient thermal impedances $Z_{thC}(t)$ and $Z_{thCW}(t)$ by about 10%.

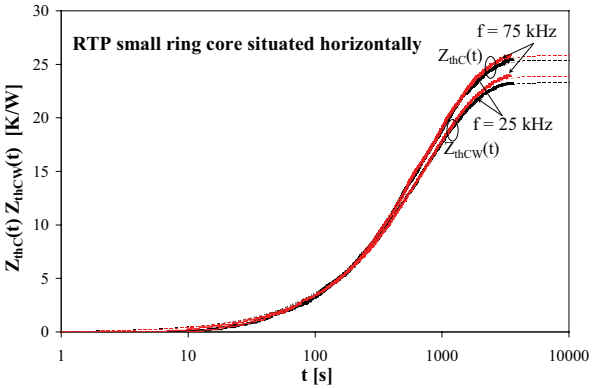


Figure 11: Measured (solid lines) and modelled (dashed lines) waveforms of transient thermal impedance of the core and mutual transient thermal impedance between the core and the winding of the transformer with the small ring core RTP at the stimulation with the sinusoidal current of frequency equal to 25kHz and 75kHz

The observed differences between waveforms of the considered thermal parameters can be caused not only by changes of the value of frequency, but also with changes of the power dissipated in the core at these frequencies (1 W at f = 25 kHz and 0.8 W at f = 75 kHz). Similarly, as this was shown in Figs. 9, an increase in the value of the power dissipated in the considered element causes a decrease in the value of thermal parameters of the transformer.

As one can notice in Figs. 6 - 11 for all the considered constructions of transformers and for all the considered cooling conditions the good agreement between the results of measurements and calculations performed with the use of Eq. (3) was obtained. However, as it is results among other things, from papers [16, 17] thermal resistance existing in this model is a decreasing function of the power dissipated in the modelled element. The decreasing dependence of thermal resistance on the dissipated power is a result of improved cooling of the transformer component with an increase in their temperature. As it is commonly known efficiency of convection and radiation increases with an increase in temperature of the heat source. Therefore, the dependence of thermal resistance on internal temperature of the heating source (the core or the winding) can be approximated with the function of the form:

$$R_{th} = R_{th0} + R_{th1} \cdot \exp\left(-\frac{T - T_0}{a_p}\right) \qquad (13)$$

where T denotes temperature of the considered component of the transformer, whereas R_{th0}, R_{th1}, T_0 and a_p are the model parameters.

The correctness of the presented description was verified experimentally. For example, in Fig.12 calculated (lines) and measured (points) dependences of thermal resistance of the winding R_{thW} and mutual thermal resistance between the winding and the core R_{thWC} on the dissipated power in the winding of the transformer with the big ring RTP core are shown. Solid lines correspond to the transformer placed horizontally, and dashed lines - to the transformer situated vertically.

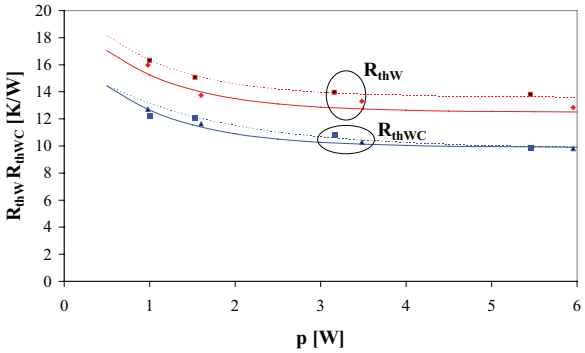


Figure 12: Measured (points) and modelled (lines) dependences of thermal resistance of the winding and mutual thermal resistance between the winding and the core on the dissipated power for the transformer with the big ring core RTP at the stimulation with the dc current

As it is visible, both the considered dependences are monotonically decreasing functions. The good agreement between the results of calculations and measurements is obtained. This proves that the proposed descriptions of the dependences $R_{thW}(p)$ and $R_{thWC}(p)$ are useful.

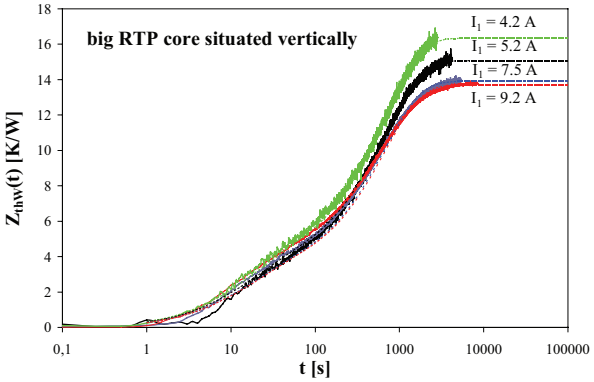


Figure 13: Measured (solid lines) and modelled (dashed lines) waveforms of self transient thermal impedance of the winding of the transformer with the big ring core RTP situated vertically at the stimulation with the direct current of different values

The considered dependences were used to model waveforms of transient thermal impedances of the impulse transformer. In this model only the value of thermal resistance is a function of the dissipated power given by Eq. (7), whereas the values of parameters a_i and τ_{thi} existing in Eq. (3) are constant for the considered transformer. For example, in Fig.13 the waveforms of measured (solid lines) and calculated (dashed lines) transient thermal impedance of the winding of the transformer with the big RTP core are presented at different values of the power dissipated in the primary winding. As it is visible, the good agreement between the results of calculations and measurements is obtained.

The difference between the temperature inside the core and on its surface is caused only by a non-zero value of thermal conductance of material used to make the core. Of course, the temperature inside the core is the highest, when power losses in the core dominate. In turn, the temperature rise of the core as a result of thermal coupling between this core and the windings is higher on the surface of the core than in the middle of it. Therefore, it is difficult to formulate the universal dependence between the temperature inside the core and on its surface. It is possible only to estimate the difference between temperatures of the surface and the middle of the core assuming that the only mechanism of heat transfer is conduction, generation of heat appears in the infinitely thin ring situated in the middle of the core, and heat flux density has uniform distribution. With these assumptions, for the ring core of the outside diameter equal to 5 cm, the inside diameter equal to 3 cm and the height equal to 1 cm, made of powdered iron at the power dissipated in the core of the value equal to 1 W the maximum temperature difference between the middle of the core and its surface amounts to 14 K.

5 Conclusions

In the paper the method to measure transient thermal impedances in the transformer and the results of measurements, illustrating the influence of the selected factors on waveforms of these thermal parameters, are presented. The research done by the Authors proves that efficiency of cooling the structural components of the transformer can be characterised by means of parameters of the compact thermal model and that the waveforms of the considered thermal parameters change depending on many factors.

For example, an increase in the value of the power dissipated in the winding by more than 30% causes a decrease of the waveforms $Z_{thW}(t)$ by several percent. In turn, enlargement of the diameter of the ring core by about 60% is effective with deterioration of thermal resistance by even about 50% and with extension of the indispensable time to obtain the steady state even by about 60%. For comparatively large sizes of the investigated elements, the time indispensable to obtain the thermally steady state reaches even 2 hours. The change of spatial orientation of the transformer (horizontal or vertical orientation) causes a change of the considered parameters by even about 20%.

The essential meaning has also the material, the core is made of, because its thermal conductance influences the measured waveforms $Z_{thW}(t)$ and $Z_{thWC}(t)$ in an essential manner. The least differences between waveforms of the mentioned thermal parameters, not exceeding 20%, were observed for transformers with cores RTP (characterised by high thermal conductance), and the greatest (by even above 50%) - for cores RTF.

The analytic description of dependences of self and mutual thermal resistances of the transformer on the power dissipated in it is proposed. It was shown experimentally that the use of this dependence in the classical literature model of transient thermal impedance assured correct modelling of waveforms of transient thermal impedances of the transformer over a wide range changes of the current of the primary winding.

It is worth noticing that the classical literature description of transient thermal impedance with the proposed description of thermal resistance enables very good approximation of the measured waveforms of transient thermal impedance of the winding for all the considered transformers. One observes, however, essential differences between the measured and approximated waveforms of mutual transient thermal impedances between the winding and the core and transient thermal impedances of the core for transformers containing ferrite or nanocrystalline cores. In the mentioned above transformers a large delay of the process of heating the core appears, which reaches even 100 s. The correct modelling of this delay demands correction in the thermal model of the transformer, which is at present an objective of the Authors investigations.

The results of investigations presented in this paper can be useful for constructors of impulse-transformers and constructors of switched-mode power supplies containing these transformers. These results will be of service also to the Authors as experimental material, indispensable to formulate the non-linear electro-thermal model of the impulse-transformer. In this model the influence of internal temperature of the core and the windings, of dimensions of the core and its spatial orientation on thermal parameters of the transformer will take into account.

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Small Signal Modeling of Scaled Double-Gate MOSFET for GHz Applications

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Abstract: The limits on scaling suggest the technology advancement for the solid-state devices. The double-gate (DG) MOSFET has emerged as an alternative device structure due to the certain significant advantages, i.e. increase in mobility, ideal sub-threshold slope, higher drain current, reduced power consumption and screening of source end of the channel by drain electric field (due to proximity to the channel of the second gate, which reduces the short channel effects). In this work, we have analyzed the double-gate MOSFET (undoped body because the doping rapidly varies the threshold voltage). The analytical expressions has been derived on the basis of surface potential model, which has been further used to yield the potential distribution, drain current, conductance and trans-capacitance. This illustrate the volume inversion effect is quite significant in this device upto the certain range of dimensions. In addition to this, we have analyzed the performance of symmetric DG MOSFET based on the circuit design prospective using S-parameters.

Keywords: Short channel effect; Double-gate MOSFET; S-parameters, RF devices; Microelectronics; VLSI.

Modeliranje majhnih signalov na pomanjšanem MOSFET z dvemi vrati za GHz aplikacije

Izvleček: Meje pomanjševanja zahtevajo napredno tehnologijo polprevodniških elementov. MODFET z dvojnimi vrati se kaže kot alternativen element zaradi očitnih prednosti, kot so: večja mobilnost, idealen naklon pod pragom, višji ponorni tok, znižana poraba in spremljanje izvorne strani kanala z električnim poljem ponora (zaradi bližine drugega kanala, kar zmanjšuje vplive kratkih kanalov). V delu smo analizirali MOSFET z dvemi vrati (nedopiran, saj dopiranje vpliva na pragovno napetost). Analitičen izraz je bil pridobljen na osnovi modela površinskega potenciala in je bil nadalje uporabljen za določanje porazdelitve potenciala, ponornega toka ter prevodnosti in trans kapacitivnosti. Volumski inverzijski vplivi so pomembno do določenih dimenzij. Dodatno smo raziskali učinkovitost simetričnega MOSFET z dvemi vrati na osnovi načrtovanja veza z S parametri.

Ključne besede: kratki kanal; MOSFET z dvemi vrati; S parameteri, RF elementi; mikroelektronika; VLSI.

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1 Introduction

The MOSFETs are basic cells for the integrated circuits but the demand to increase the switching speed, packing density and reduction in power consumptions are the reasons to extend the work in the direction of miniaturization as suggested by ITRS [1]. Initially, the scaling was the basic tool for miniaturization, however with the advancement in scaling, certain undesirable effects restrict the performance of the device such as short channel effects (SCE) [2, 3]. This motivated to move onto the new device structures. Therefore, *Balestra et. al*. [4] have proposed the first double-gate (DG) MOSFET with significant volume inversion effect. Currently, the DG MOSFET is a subject of intense very large scale integration (VLSI) research and a replacement for conventional bulk MOSFET beyond the *45-nm* technology [5]. It can be scaled to the shortest possible channel length for a given oxide thickness and more electrostatically robust than the earlier reported MOSFETs due to the dual-gate shielding and the reduced SCE [6].

Fossum et. al. [7] have analyzed the higher processing speed of DG MOSFET as compared to that of the single-gate MOSFET which further encouraged *Solomon et. al.* [8] to confer the advantages of the two gates over one gate. Fig. 1 shows the schematic of a DG MOSFET and the Fig. 2 presents the two major DG MOSFET structures:

Symmetric type with both gates of identical work-functions where both the surface's channels turn on at the same gate voltage [9] and *Asymmetric type* with either different work function of the gates or different gate oxide thicknesses where only one channel turns ON at the threshold voltage [10, 11].

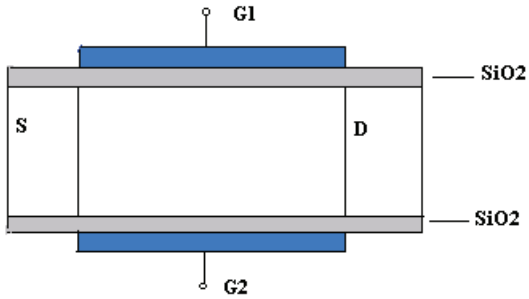

Figure 1: The schematic of double-gate MOSFET.

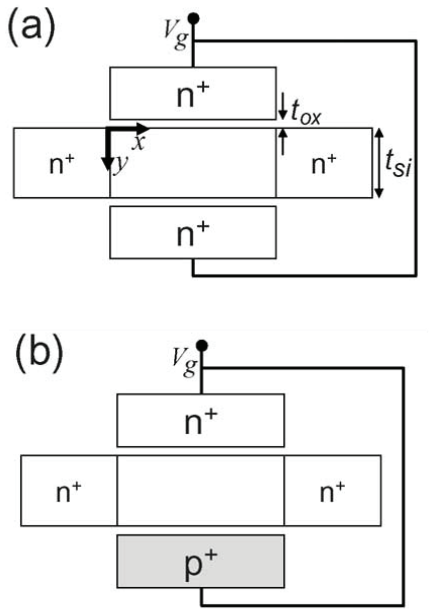

Figure 2: (a) Symmetric Double-gate MOSFET, (b) asymmetric Double-gate MOSFET [11].

Taur et. al. [12] have derived the analytical model based on the charge sheet approximation which is applicable to all operating regions such as cutoff, linear and saturation. Lu et. al. [13] also have developed a design based on the *Poisson theory* and the current continuity equation without charge sheet approximation and accounting the volume inversion concept. The drain current, terminal charges and the capacitances are further developed based on the numerical iterations. However, both the authors [12, 13] discussed the asymmetric DG MOSFET which is more sensitive as compared to the symmetric, to Silicon body thickness which further varies the threshold voltage. Yu et. al. [14] have proposed an algorithm and the PSP model for approximation of the surface potential of both the single-gate (SG) MOSFET and DG MOSFET. The model can cover all the operating regions without the use of fitting parameters or charge sheet approximation. However, this algorithm is really complex for implementation.

In addition to this, *Conde and Sanchez* [15] have developed a unified model for symmetric, asymmetric DG MOSFET and bulk MOSFET by using the mix-formulation of the charge and surface potential approaches. The mathematical expression derived for the drain current depends on the Silicon body thickness. However, the assumption is made that for the symmetric DG MOSFET, the electric field vanishes at the mid-point of the front and back surfaces but for the asymmetric DG MOSFET, the electric field is present. In addition to this, for the conventional MOSFET the charge coupling factor is zero and charge sheet approximation has not been used in ref. [15]. The state of the art of compact models for undoped DG MOSFET using the 1-D *Poisson equation* with the introduction of the SCE has been discussed in detail in ref. [16]. The threshold voltage based model for undoped DG MOSFET was also explored in ref. [17] and discusses the feasibility and the advantages of DG MOSFET over the conventional MOSFET. In ref. [18], an analytical expression for electric potential of the symmetric and asymmetric DG MOSFET with undoped body has been derived by considering the mobile charge in the *Poisson equation* and it has been illustrated that the *ON-state* currents differ slightly from each other when the Silicon thickness is significantly small. *Cakici and Roy* [19] have discussed a circuit perspective with the effect of connected gates or independent gates DG MOSFET, and illustrated that the significantly high noise immunity at low dynamic power dissipation can be achieved by the independently operating gates (as it increases the gate to gate coupling). In addition to this, it also affects the delay, leakage power and process variations. Moreover, with the use of independent-gates technology, the dynamic threshold voltage control is feasible. *Singh and Jiang* [20] showed that with the help of asymmetric DG MOSFET high performance and low power circuits are feasible in the nanometer regime. Therefore, this structure can be used in phase locked loop where the requirement is high speed, low voltage and low power operation [21]. Further, the other application of symmetric DG MOSFET is as a fast switching device [22]. Recently,

Srivastava et. al. [22-24] have analyzed the DG MOSFET and cylindrical surrounding double-gate (CSDG) MOSFET for the application as a double pole four throw switch.

In this research work, we have analyzed the performance of the symmetric DG MOSFET based on the potential distribution, sheet charge, drain current, terminal charges and trans-capacitance. Further, the trans-capacitances are used for the circuit simulation. The work has been organized as follows. Section 2 has discussion about the symmetric DG MOSFET with its design philosophy and working operation. Section 3 deals with the analysis and the simulation model. Section 4 explores the simulation results of the symmetric DG MOSFETs. Finally, the Section 5 concludes the work and recommends the future aspects.

2 Symmetric Double-Gate MOSFET

The planar DG MOSFET is an extension of the single-gate MOSFET which consist two gates designated as front-gate and back-gate, and a sandwiched ultra thin Silicon layer between these gates [25]. The additional gate significantly increases the electrostatic gate control over the channel and these gates are effective in shielding the drain electric field lines from reaching the source to reduce the potential barrier as well as reducing the short channel effects (SCE). Due to undoped / lightly doped body, the problem of random dopant fluctuation is also negligible. Moreover, both the gates contribute to inversion carriers, which have high drive capability and two channels for the current flow are formed (when these two gates simultaneously control the charge). Also, due to the very thin Silicon film, a better coupling between front-gate and back-gate exists, which affects the terminal characteristics of the MOSFET.

Double-gate silicon-on-insulator transistor with volume inversion has been analyzed by Balestra et. al. [26]. The basics of the fabrication processes are helpful in the fabrication of DG MOSFETs [27]. Yesayan et. al. [28] have included the effect of interface traps in nanowire and double-gate junction-less devices through a charge-based model that has been developed previously. *Roy et. al.* [29] have accurately handled both *Fermi–Dirac statistics* and *bias-dependent diffusivity* regarding core compact model for undoped, high mobility, and low density of states materials in a double-gate device architecture. Taur et. al. [13, 30] have presented an analytic potential model for long-channel symmetric and asymmetric double-gate MOSFETs. This design has been derived from the solution of *Poisson's* and current continuity equation without the charge-sheet approximation. This results in the analytic expressions of the drain-current, terminal charges, and capacitances for long channel DG MOSFETs continuous in all operation regions (linear, saturation, and sub-threshold), making it suitable for compact modelling. The extension of the DG MOSFET is as cylindrical surrounding-gate MOSFET has been analyzed by Sood et. al. [31].

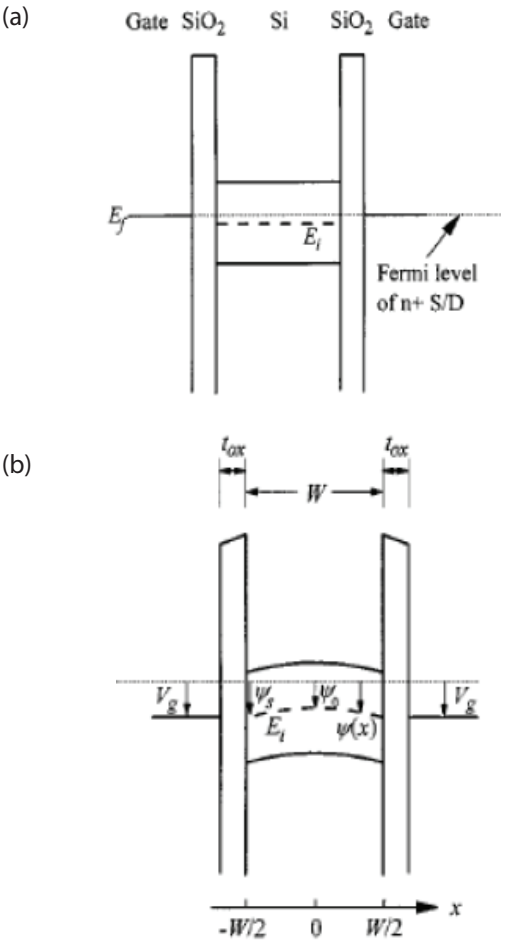

Figure 3: The band model of the symmetric DG MOSFET a) $V_{gs} = 0\ V$ b) $V_{gs} = V_{th}$ [9].

For the symmetric double-gate device structure, at the zero gate voltage the Silicon bands are flat for the mid-gap gate work function as shown in Fig. 3(a). However, at $V_g = V_{th}$, the edge of conduction band (Silicon body) near the surface bents as in Fig. 3(b) and approaches the conduction band edge of the n^+ source/drain. However, the conduction bands in both surfaces, under both gates, are bent by the similar value as the work functions of two gates are identical. At ON-state, two conductive channels (under both the gates) are formed for the symmetric double-gate device, unless the Silicon body is not very thin [12].

3 Analysis of Parameters

To analyze the various parameters, we have first analyzed the *1-D Poisson's equation* in the Cartesian coordinate system with gradual channel approximation which is given as [32]:

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\varepsilon_{Si}} e^{q(\psi - V)/kT} \tag{1}$$

where, q and ε_{si} are the electron charge and dielectric permittivity of Silicon respectively. The n_i, k, and T are the intrinsic concentration of Silicon, the Boltzmann constant, and working room temperature, respectively. The V represents the quasi-Fermi potential $V = 0$ at source side and $V = V_{ds}$ at drain side. We have considered the n^+ DG MOSFET, therefore the holes density is negligible and the Silicon film is undoped or lightly doped that is:

$$n_b << n_i e^{q(\Psi - V)/kT} \tag{2}$$

where, n_b is the doping concentration. However, integrating the Equation (1) twice, we can get the potential distribution equation as a function of '*x*' which is position in the Silicon body thickness. In the symmetric DG MOSFET, the electric field is zero at $x = 0$ that is the center of the Silicon body thickness.

3.1 Surface Potential

The surface potential (ψ_s) for DG MOSFET is:

$$\psi_s = \psi_o - \frac{2kT}{q}\left\{\log\left[\cos\left(\sqrt{\frac{q^2 n_i}{2kT\varepsilon_{Si}}} e^{q(\psi_o - V)/2kT} x\right)\right]\right\} \tag{3}$$

The boundary condition for symmetric DG MOSFET:

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(V_{gs} - \Delta\phi_i - \psi_s\right) = \pm\varepsilon_{Si}\left.\frac{d\psi}{dx}\right|_{x=\pm w/2} \tag{4}$$

where, ε_{ox}, V_{gs} and t_{ox} are the permittivity of oxide, gate voltage and oxide thickness respectively. After boundary conditions are satisfied, the center potential is given by:

$$\psi_s = V + \frac{2kT}{q}\left\{\ln\left[\frac{2}{at_{Si}} Sin^{-1}\frac{q\varepsilon_{ox}(V_{gs} - \psi_s)}{2\varepsilon_{Si}kTa} e^{-q(\psi_s - V)/2kT}\right.\right. \tag{5}$$

where, t_{si} is the Silicon body thickness. The surface potential is given by:

$$Sin\left(\frac{at_{Si}}{2}\sqrt{1-\left(\frac{qC_{ox}(V_{gs}-\psi)}{2kTa\varepsilon_{Si}} e^{-q(\psi-V)/2kT}\right)^2} * e^{q(\psi-V)/2kT}\right) = \tag{6}$$
$$= \frac{qC_{ox}(V_{gs}-\psi)}{2kTa\varepsilon_{Si}} e^{-q(\psi-V)/2kT}$$

where,

$$a = \sqrt{\frac{q^2 n_i}{2kT\varepsilon_{Si}}} \tag{7}$$

3.2 Drain Current

By following the dual integral [33], the drain current can be written as:

$$\begin{aligned} I_{ds} &= \frac{2\mu W}{L}\int_0^{V_{ds}} Q(V)dV \\ &= \frac{2\mu R}{L}\int_{\psi_{ss}}^{\psi_{sL}} Q(\psi_s)\frac{dV}{d\psi_s}d\psi_s \end{aligned} \tag{8}$$

where *Q* represents the inversion charge. Therefore, the drain current becomes:

$$I_{ds} = \frac{2\mu C_{ox}W}{L}\left[\frac{2kT}{q}\left(V_g - (\psi_{sL} - \psi_{ss})\right) - \frac{1}{4}\left(V_g - (\psi_{sL} - \psi_{ss})\right)^2 + \right.$$
$$\left. + \frac{8\varepsilon_{Si}k^2T^2}{q^2WC_{ox}}\ln\left(\frac{C_{ox}\left(V_g - \psi_{sL}\right) + \frac{4\varepsilon_{Si}kT}{qW}}{C_{ox}\left(V_g - \psi_{ss}\right) + \frac{4\varepsilon_{Si}kT}{qW}}\right)\right] \tag{9}$$

where, ψ_{ss} and ψ_{sL} are the potential at source side ($V = 0$) and potential at drain side ($V = V_{ds}$) which can be found through Equation (6).

3.3 Terminal Charges

For the modeling of total inversion charge, Ward Dutton charge partition method [24] has been used where the total inversion charge given by $Q = C_{ox}\left(v_{gs} - \psi_s\right)$ is partitioned into source charge (Q_s), drain charge (Q_d), and gate charge (Q_g) such as [34]:

$$Q_g = \int_0^L Q(y)dy,\ Q_d = \int_0^L \frac{y}{L}Q(y)dy,\ Q_s = \int_0^L\left(1 - \frac{y}{L}\right)Q(y)dy \tag{10}$$

We are modeling the charges based on the surface potential, therefore transforming y to ψ_s in all the equations and then performing the integration analytically which yields the expressions for the terminal charges.

3.4 Trans-Capacitance

Based on the expressions of the terminal charges, the capacitances of the double-gate MOSFET such as gate to source (C_{gs}), gate to drain (C_{gd}), and source to drain

(C_{sd}) can be written as:

$$C_{gs} = \frac{\partial Q_g}{\partial \psi_{ss}} \frac{\partial \psi_{ss}}{\partial V_s} \quad C_{gd} = \frac{\partial Q_g}{\partial \psi_{sL}} \frac{\partial \psi_{sL}}{\partial V_d} \quad C_{ds} = \frac{\partial Q_s}{\partial \psi_{sL}} \frac{\partial \psi_{sL}}{\partial V_d} \quad (11)$$

where the values of charges Q_s, Q_d, and Q_g are given in Equation (10). These capacitances were used in circuit simulations. The DG MOSFET with same potential applied to both gates is a combination of two single-gate MOSFETs connected in parallel.

3.5 Small Signal Model

The small signal equivalent circuit as shown in Fig. 4 has been analyzed. This equivalent circuit has been derived from the formation of capacitance and resistance at the junctions and the body of the double-gate MOSFET. Based on the intrinsic parameters of the device, the *Y-parameters* can be derived. However, scattering parameters can be obtained by applying the normal conversion based on the *Y-parameters* [35, 36].

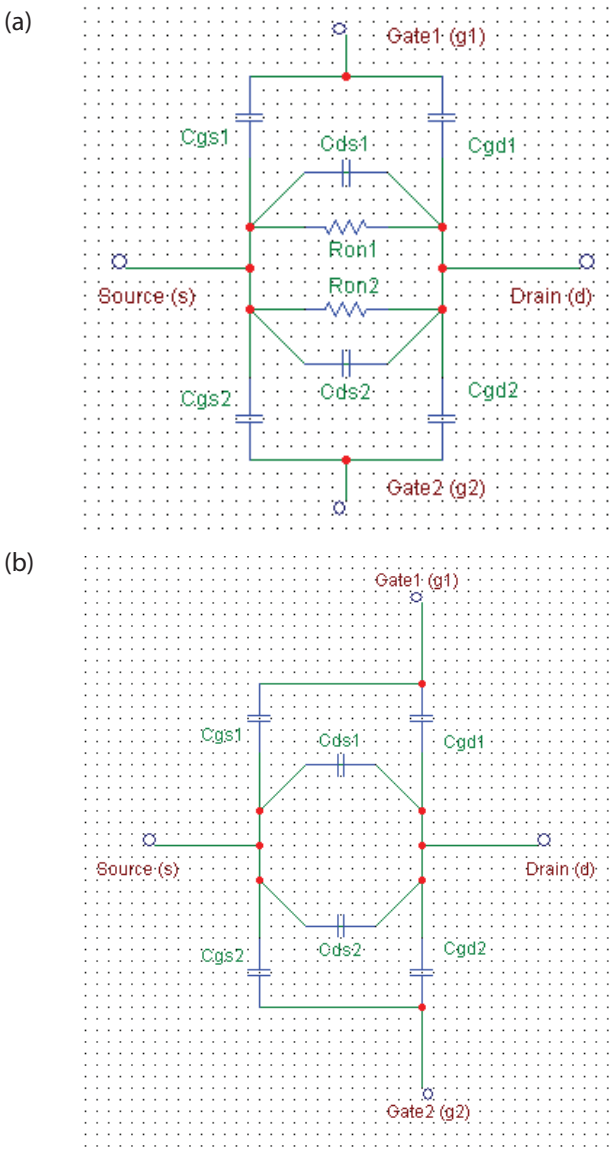

Figure 4: Small signal modeling of DG MOSFET at (a) Switch-ON state, and (b) Switch-OFF state.

4 Results and Its Analysis

We have presented the simulion results for symmetric DG MOSFET based on the electric potential, electron density, drain current, conductance, terminal charges and transcapacitance. In addition to this, the S-parmeter and gain analysis has also been performed.

4.1 Volume Inversion Analysis

The volume inversion effect is quite significant when the gate-source voltage is less than that of the threshold voltage. With the increase in gate voltage, the potential increases at the surface as the channel is formed on the surface and the minimum electric potential lies at center of the body $x = 0$, due to the screening of the center of the Silicon body by the charges on the surface as shown in Fig. 5. In addition to this, the significant effect can be seen for the $V_{gs} = 0.412\ V$ and $V_{gs} = 0.845\ V$.

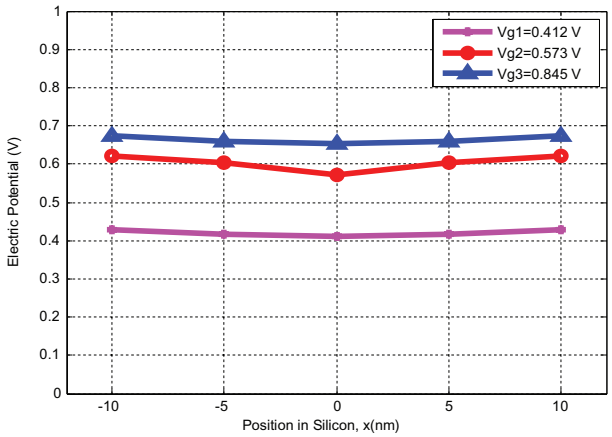

Figure 5: Electric potential variation with Silicon body thickness (nm).

The volume inversion effect is significant up to threshold voltage, $V_{th} = 0.4\ V$ but as the gate voltage crosses the threshold voltage the surface and the center potentials are decoupled. The center potential saturates at a specific value of potential as the arcsine argument in the Equation (5) cannot grow beyond $\pi/2$ but the surface potential keeps on increasing. It is illustrated through the Fig. 6 that the surface potential variation above the threshold voltage is independent of the Silicon body thickness. The input and output charecterstics of the DG MOSFET as shown in Fig. 7(a) and Fig.

7(b) are similar to that of the conventional MOSFET. The response of drain to source voltage over the drain current with various values of V_{gs} shown in Fig. 7(b) reveals the two operating regions (i. e. linear and saturation regions). By extrapolating these curves and finding the intersection with the x-axis the corresponding values of threshold voltage can be obtained (V_{th} = *0.6 V* and V_{th} = *0.7 V* for V_{ds} = *0.5 V* and V_{ds} = *1 V*, repectively).

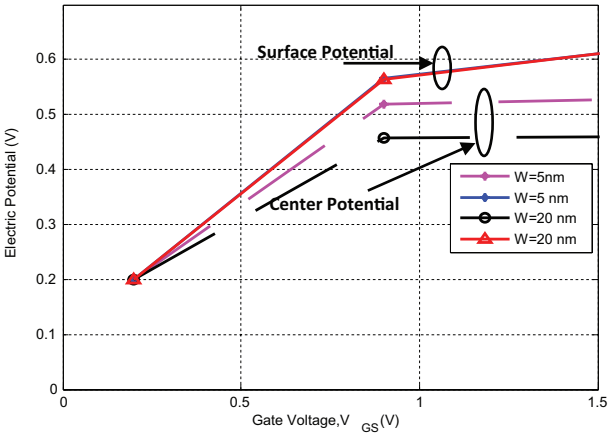

Figure 6: Electric potential variation with gate to source volatage.

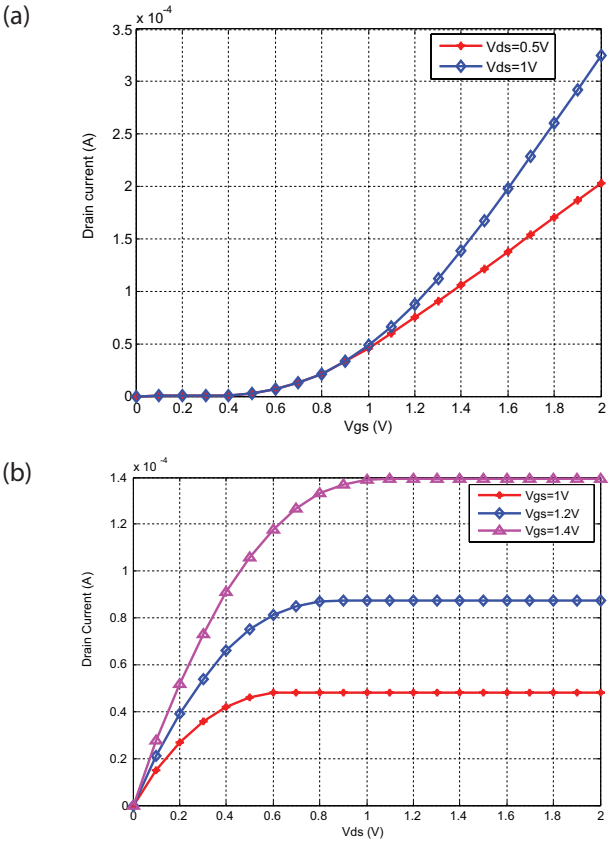

Figure 7: Drain current variation of DG MOSFET for t_{ox} = *2 nm*, *W = 30 nm* and *L = 90 nm* at various (a) gate to source voltage and (b) drain to source voltage.

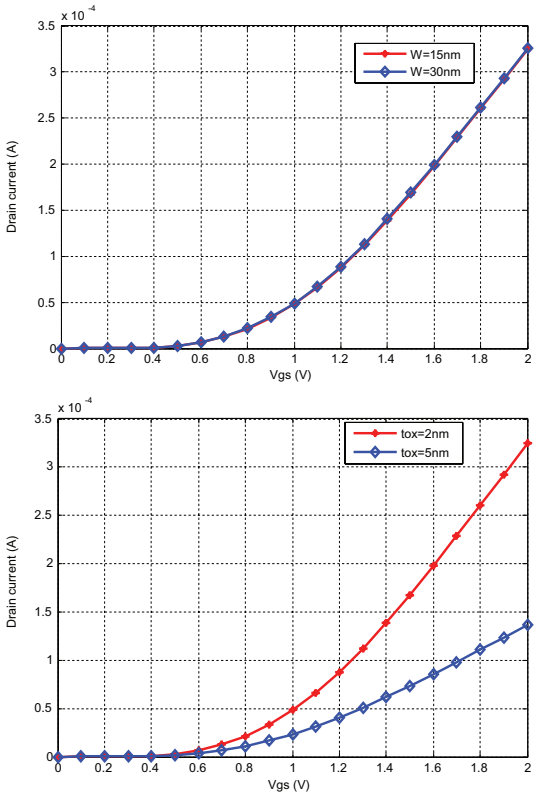

Figure 8: Response of drain current for various gate to source voltage at V_{ds} = *1 V* and *L = 90 nm* for (a) *fixed* t_{ox} = *2 nm* and (b) fixed width *W = 30 nm*.

4.2 Drain current analysis

The drain current is independent of the device width, however, its dependence over the oxide thickness is quite significant as shown in Fig. 8. It is well illustrated in Fig. 8(b) that the charge formation on the surface increases with the reduction in the oxide thickness, hence results in the increased device current.

4.3 Conductance and Transconductance Analysis

Fig. 9 shows the effect of oxide thickness on the conductance and transconductance for *W = 30 nm* and *L = 90 nm*. As the drain to source voltage increases for chosen oxide thickness, the conductance of the device decreases and reduces to zero as the pinch-off point is achieved as shown in Fig. 9(a). In addition to this, with the decrease of oxide thickness, the conductance of the device increases. In Fig. 9(b) as the gate voltage reaches the threshold voltage the transconductance increases with increasing V_{gs}. However, transconductance $G_m = {}^{\partial I_{ds}}/_{\partial V_{gs}}$, depends on C_{ox} as in Equation (9) through I_{ds}. Therefore with the increase of oxide thickness (which reduces the C_{ox}), the transconductance decreases. This concludes the significant enhancement in the overall gain of the device.

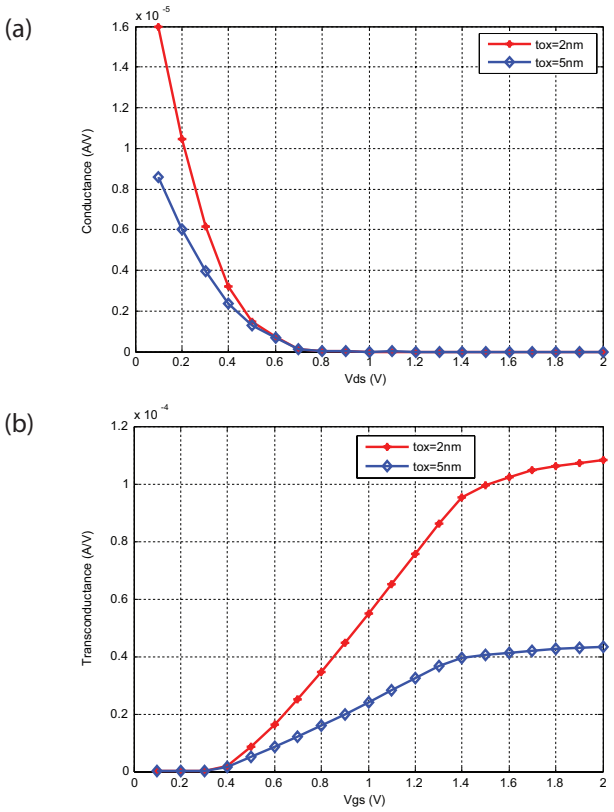

Figure 9: Effect of oxide thickness on the (a) conductance at $V_{gs} = 1\ V$ and (b) trans-conductance at $V_{ds} = 1\ V$.

4.4 Trans-Capacitance and Terminal Charge Analysis

Fig. 10(a) and Fig. 10(b) illustrate the trans-capacitance and the variation of terminal charges with V_{ds} for specific value of the oxide thickness. As the oxide thickness increases, the charge storage capacity decreases which further results in the decrease in capacitance of the device. However, the gate to drain capacitance (C_{gd}) and the source to drain capacitance (C_{sd}) do not depend on drain voltage after the saturation is achieved. Fig. 10(c) and Fig. 10(d), where $t_{ox} = 2\ nm$, $W = 20\ nm$ shows the variation with width of device (W). When comparing Fig. 10(a) and Fig.10(b) with these, it can be seen that as the width reduces the terminal charges the trans-capacitances are also reduces due to smaller device area. It is illustrated by Fig. 10(b) and Fig. 10(d) that the source charge always saturates to the value of *6/10* of the gate charge and drain charge saturates to *4/10* of the gate charge.

4.5 S-Parameters Analysis

Fig. 11 shows the S-parameters computed analytically using equivalent circuit of DG MOSFET with $t_{ox} = 2\ nm$, $W = 40\ nm$, $L = 1\ \mu m$, $V_{gs} = 1\ V$ and $V_{ds} = 0.9\ V$. The S_{11} represents the input reflection coefficient and it has been illustrated that the S_{11} reduces for high frequency,

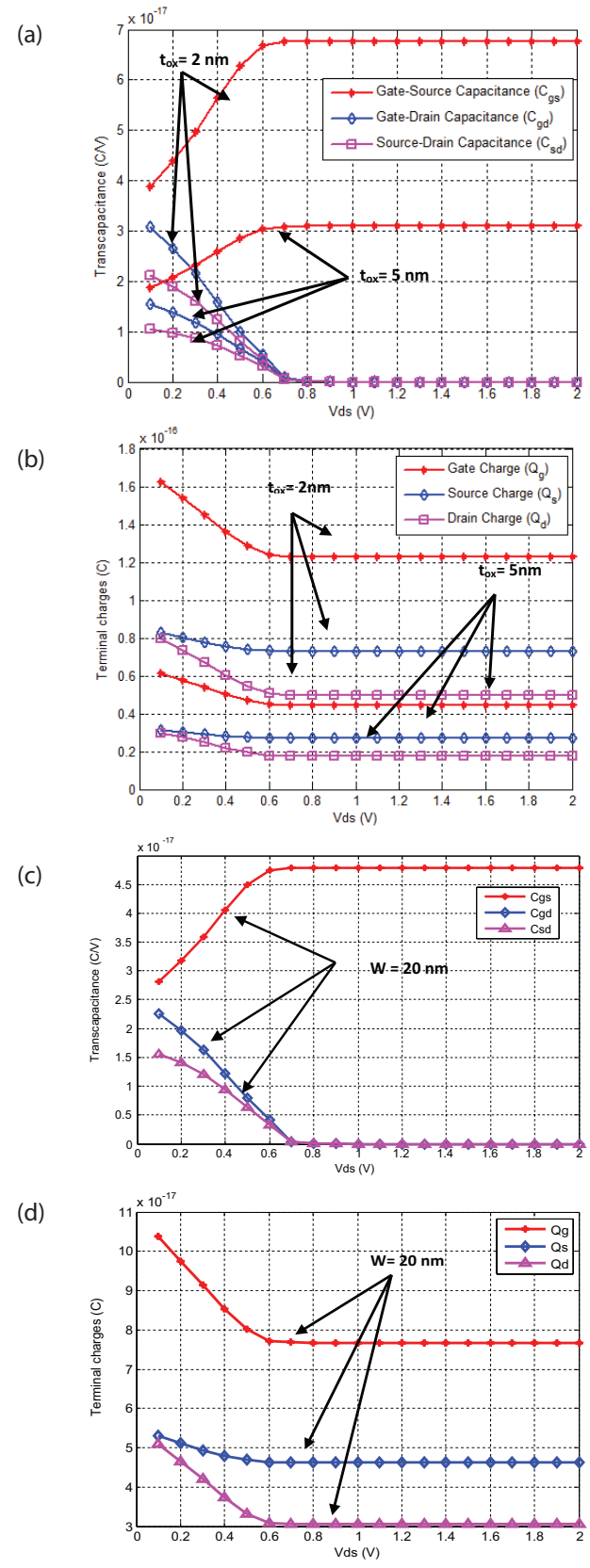

Figure 10: (a) Trans-capacitance, (b) terminal charges for $W = 30\ nm$ and $L = 90\ nm$, (c) Trans-capacitance, and (d) terminal charges for $W = 20\ nm$, $t_{ox} = 2\ nm$ and $L = 90\ nm$, at $V_{gs} = 1\ V$.

which is an advantage as the return loss is reduced for the device. The S_{21} represents the amount of power transferred from the input port to the output port and it also illustrates that as the frequency increases the S_{21} parameter remains constant which implies constant forward gain at higher frequencies.

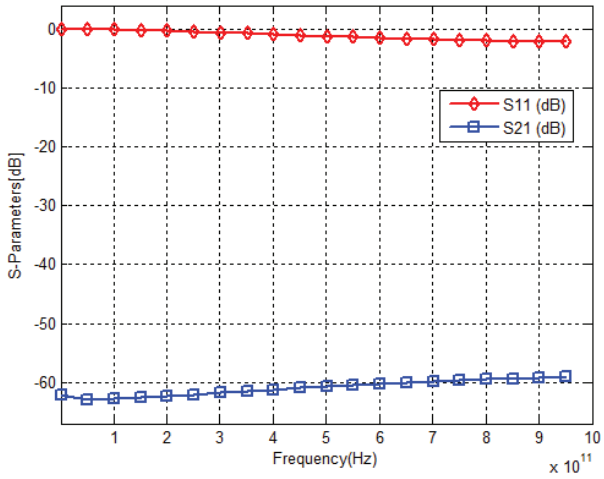

Figure 11: S-parameters over a range of high frequencies.

4.6 Power Gain Analysis

Fig. 12 represents the power gain achieved by the DG MOSFET over the range of frequencies. The unilateral power gain is the gain achieved when the input and the output port are matched simultaneously and the feedback is neutralized by adding a feedback network. As the frequency increases, this gain decreases exponentially and the decrease is smaller at high frequency due to the dual gate controllability. By extrapolating the curve for the gain of *1 dB*, the maximum frequency of oscillation can be inferred from the Fig. 12 to be around *254 GHz*. The gain achieved (when the two ports are simultaneously matched) is known as maximum stable power gain. It is predicted by the Fig. 12 that as the frequency increases the input-output mismatch decreases. In addition to this, the gain always remains above *0 dB* which suggests a major figure-of-merit for low noise amplifiers. The maximum unilateral transducer power gain is the ratio of power delivered to load to the power available at the source when the neutralization is provided which further enhances the maximum power transfer. All these gains are stable with the frequency only due to the dual gate controllability as suggested by Fig. 12. Therefore, the DG MOSFET with the analyzed dimensions is useful for high frequency applications.

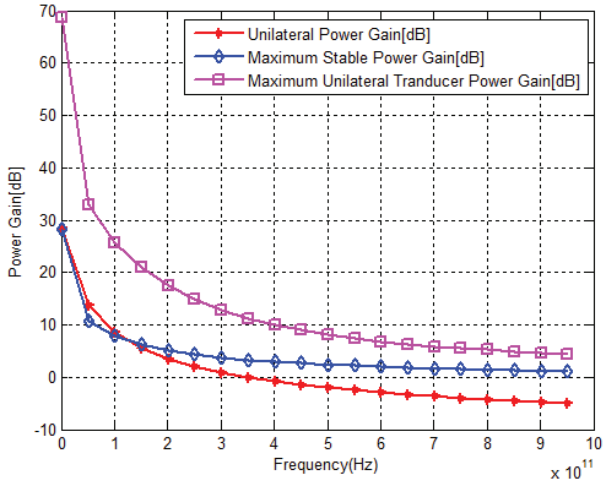

Figure 12: Response of the power gain at various frequencies for the DG MOSFET.

5 Conclusions and Future Recommendations

In this work, the analytical modeling of symmetric DG MOSFET with undoped Silicon body has been presented. The results reveals that for the symmetric DG MOSFET the electric potential varies in proportion with the gate voltage and the minimum potential lies at the center of the Silicon body due to the symmetric nature of device. In addition to this, the volume inversion effect is also significant and the surface potential variation beyond the threshold voltage is independent of the Silicon body thickness.

The *I-V* and *C-V* model are also reproduced and it is seen that the drain current in strong inversion region is invariant to width of device. Moreover, the intrinsic model has been proposed from where the high frequency characteristics in terms the S-parameters and gain are obtained. The results show that the DG MOSFET is useful for high frequency applications. However, with the optimization of the device structural parameters, the performance can be improved, which will be reported in future communication.

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DOE Study of Epitaxial Layer Thickness and Resistivity Effects on P-i-N Diode for beyond 300 V of Reverse Voltage Applications

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Abstract: A discrete power switching device used in the applications of computer and telecommunications requires operating less than 300 V during reverse bias, but for the use of motor control, robotics, and power distribution, it requires operating at beyond 300 V. With the current design structure, the P-i-N diode device can only operate at 250 V. To widen the operating range of the P-i-N power switching avalanche diode that can be operated more than 300 V, we studied the effects of the epitaxial layer thickness (WD) and resistivity (ρ) during forward and reverse biasing by performing a process simulation as well as the confirmation on the two level factorials of design of experiment (DOE) of physical wafers. The result shows that, the changes of the WD of 42 µm and ρ of 32 ohm·cm on a P-i-N diode can increase the reverse breakdown voltage (VR) performance beyond 300 V during reverse bias.

Keywords: Forward voltage; Breakdown voltage; Power device

Načrtovanje eksperimenta vplivov debeline in upornosti epitaksijske plasti P-i-N diode pri reverznih napetostih nad 300 V

Izvleček: Diskretni močnostni stikalni element za uporabo v računalnikih in telekomunikacijah zahteva delovanja pri zaporni napetosti pod 300 V. Pri krmiljenju motorjev, v robotiki ali pri močnostnih aplikacijah pa zahteva delovanje v zaporni smeri preko 300 V. Trenutna struktura P-i-N diode lahko deluje le do 250. Za višje napetosti je potrebna močnostna plazovita P-i-N dioda, na kateri smo preučevali vplive debeline epitaksijske plasti in upornosti pri prevodni in zaporni napetosti. Analiza sloni na simulaciji procesa dvonivojske faktorizacije načrtovanja eksperimenta silicijeve rezine. Rezultati izkazujejo, da sprememba debeline za 42 µm in upornosti za 32 ohm·cm zviša prebojno napetost preko 300 V.

Ključne besede: Forward voltage; Breakdown voltage; Power device

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1 Introduction

Diode is a simple semiconductor device with two terminals, allowing only unidirectional current to flow. It is created with the presence of p-type and n-type semiconductor materials in intimate contact on an atomic scale, yielding the P-N junction in between [1]. The formation of P-N junction occurred by diffusion of acceptor impurities (p-type dopant) into an n-type silicon crystal or vice versa. A depletion region formed instantaneously across a P-N junction and it is easily to be described when the junction is in thermal equilibrium or in a steady state: in both of these cases, the properties of the system does not vary in time; thus, it is known as dynamic equilibrium [2, 3]. Figure 1 (a) shows the diode 2D structure and electrical field distribution of P-N diode. For high power applications, an ideal power diode should be able of conducting high forward bias current (I_F) during forward bias voltage (V_F) of ~0.7 V and supporting high reverse breakdown voltage (V_R) in the range of 50 to 200 V [4, 5].

During reverse bias, P-N diode experiences the avalanche breakdown. To achieve the avalanching, besides the requirement of a large field, it also requires a sufficient distance to allow the electron to accelerate, hence gain enough kinetic energy, and lead to an avalanche of multiple hole-electron pair's creation [6]. In other words, to ensure the high V_R, a thick n-type substrate bulk is required for a vertical structure of simple P-N junction diode. For a vertical structure of P-N junction diode, a very thick wafer substrate bulk can be used to fulfill the requirement of a power diode. However, thicker substrate exhibits several drawbacks, which are 1) greater weight and 2) higher production cost.

Alternatively, higher V_R and I_F can be achieved by using the P-i-N diode structure with a thinner substrate. The P-i-N diode was one of the very first semiconductor devices developed for power circuit application [4, 7]. This evolution came from a conventional P-N junction diode with the addition of an extra intrinsic layer deposited between p-type and n-type regions. Figure 1 (b) (i) illustrates the P-i-N diode structure in 2D structure and electrical field distribution of P-i-N diode. In P-i-N diode, the reverse breakdown voltage is dependence on the depletion region formed with a P-N junction structure. The voltage is primary determined within the N-type drift region. Thus low doping concentration for the N-type drift region is more beneficial in order to hold the carrier from flowing between P- and N-region. The silicon P-i-N diode is designed to support large voltages, which rely upon the high level injection of minority carrier in the N-type drift region [8]. Therefore, to support a large voltage in the reverse breakdown voltage mode, an appropriate choice of doping concentration and thickness of the N-drift region needs to be made. Nevertheless, a narrower drift region is preferable because it can contain smaller amount of stored charges during the on-state operation, enabling faster turn-off.

Material substitution is one way to achieve narrower drift region thickness [9]. For example, by using silicon carbide, narrower drift region can be attained when compared to silicon devices. This is due to much larger electric field can be supported in silicon carbide. As a result, it favors a faster switching speed with reduced reverse recovery current and very high breakdown voltage can be achieved [10]. However, the high cost is a major concern, and silicon P-i-N diode still can be modified and continue to play an important role in the application, especially in medium range of breakdown voltage.

This can be explained based on expression as shown in Equation (2). The expression for V_R in this P-i-N diode can be derived by using higher critical electric field (E_C) [11, 12] Based on Figure 1 (b) (ii), E_C is the critical electric field and W_D is depletion region thickness during reverse bias. Since P-i-N diode operates in a thickness-limited mode, which is controlled by the thickness of N- region epitaxial layer, the W_D can be referred to as the thickness of the N- epitaxial layer in i-region. The V_R can be calculated as the area of the trapezium (Figure 1 (b) (ii)) as in Equation (2).

$$V_R = \frac{1}{2}\left(E_C + E_1 \right) W_D \tag{2}$$

By using the Equation (2) for the variation in the electric field with distance:

$$E_1 = E_C - \frac{q\, N_D}{\epsilon_S}\, W_D \tag{3}$$

and substituting Equation (3) in Equation (2), the V_R for the punch through diode is obtained as in Equation (4):

$$V_R = E_C W_D - \frac{q\, N_D W_D^{\,2}}{2\,\epsilon_S} \tag{4}$$

The V_R can be affected by the variable thickness of the N- region (W_D) and the doping concentration of the N-

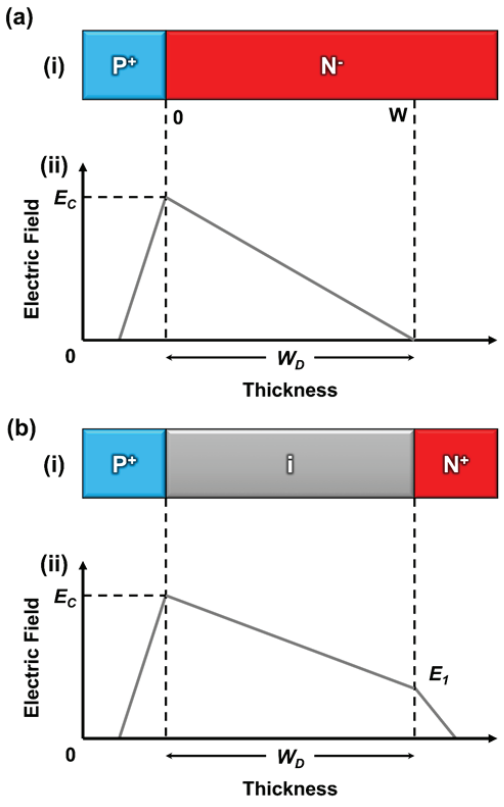


Figure 1: Comparison of ideal (a) P-N junction and (b) P-i-N diode in terms of (i) 2D structure and (ii)electrical field distribution.

epitaxial layer (N_D). The N_D can be translated into the resistivity of the N- layer [11],. The increase of the N_D results in lower resistivity.

In this paper, P-i-N diode with high resistivity N region (N- region) is used to replace the intrinsic layer. For this purpose, a commercially available 250 V P-i-N power switching diode was used to evaluate effects of N- epitaxial layer thickness (W_D) and resistivity (ρ) as the intrinsic layer effect to the P-i-N power switching diode on the performance of current-voltage (I-V) characteristic in terms of diode's V_R. The aim of this study is to have a diode that can withstand beyond 250 V for motor control, robotics and power distribution applications. The N- region is deposited on top of the wafer substrate through epitaxial process.

2 Methodology

In this work, the simulation of the P-i-N diode is performed using technology computer-aided design (TCAD) simulation software i.e. Sentaurus WorkBench, as well as the fabrication and characterization of the P-i-N diode. The P-i-N power switching diode diffuses a circular shaped boron (P+ anode junction) into an N- type epitaxial layer on a low bulk resistance N+ substrate. Another N+ diffused isolation region at the perimeter of the anode junction to reduces leakage current. The backside of the wafer is sputtered with platinum (Pt) and gold (Au). The process followed by a quick drive-in cycle for both elements, from the bulk all the way through the epitaxial layer and the P+ anode junction. Pt improves the life time cycle, reducing the reverse recovery time (t_{rr}) [13]. Au increases the epitaxial layer's t_{rr} resistance, which increases the resistance of drastic oscillation of the signal. Thus, it produces a wider P-N junction depletion region and reducing the capacitance. Figure 2 illustrates the cross-section design of the P-i-N power switching diode.

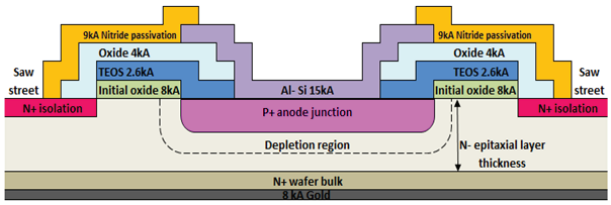


Figure 2: Cross-section structure of P-i-N power switching diode.

2.1 Numerical Simulation

The V_R of P-i-N power switching diode operates in W_D limited mode of the epitaxial layer. The first approach is to alter the W_D by adjusting the depth of the P+ anode junction through diffusion with boron as demonstrated in Figure 2. By reducing the junction diffusion drive time, a shallower anode junction is formed. With this approach, the W_D is increased [14]. However, this method has several weaknesses. The anode junction diffusion process is difficult to control, which leads to process variation. The inconsistent process temperature of diffusion furnace results in lower V_R at the edges compared to the centre of the wafers, as wafer edges tend to have a higher process temperature compared to the wafer centre [14]. Another drawback is the diffusion process is performed under a high temperature, thus caused the up diffusion from the heavily doped N+ bulk substrate. This resulted in a less favourable higher V_F [14].

The second approach is to adjust the epitaxial layer profile (W_D and ρ) of the substrate [14]. With the zero punch through structure of the P-i-N diode, as observed from the Equation (4), the W_D and N_D are dominant factors, which increase the V_R. The second approach is more favourable due to better control of wafer fabrication process.

A series of simulation and DOE is performed to show the effects of the W_D and N_D on the I-V characteristic using TCAD simulation software. The applications of TCAD simulation include technology and design rule development, as well as the extraction of compact models for manufacturability [15]. Initially, a half diode cross-section structure is designed by using SProcess. After the half diode is created, reflecting boundary conditions is applied to generate a full simulation diode model symmetrically.

For the SProcess step, a layer of phosphorus dopant (N- epitaxial) thickness is grown on top of the N+ bulk silicon substrate, which is initially doped with arsenic. The silicon substrate orientation of <100> is used. The dopant parameter is defined as @epidose@ and W_D parameter is defined as @epiThick@. With the parameters are defined in general, several W_D and doping concentrations are utilized in the simulation (Table 1) to evaluate the output response of the I-V characteristic.

Table 1: Simulation thickness and concentration dosage of N- layer.

Split	Epitaxial Layer Thickness, @epiThick@ (μm)	Epitaxial Layer Dopant Concentration, @epidose@ (cm^{-3})
a	42	1.68×10^{14}
b	42	1.58×10^{14}
c	42	1.48×10^{14}
d	42	1.36×10^{14}

e	34	1.68×10^{14}
f	34	1.58×10^{14}
g	34	1.48×10^{14}
h	34	1.36×10^{14}

The selection of the 34 µm and 42 µm thickness of W_D in simulation is due to lower and upper specification on the existing diode device epitaxial layer evaluation shown as group C in Figure 5, which will be explained in Section 2.2. The various dopant concentrations of N- epitaxial layer are selected to measure the electrical output response impact in simulation. By adjusting the phosphorus dopant concentration at the N- epitaxy layer via implantation, the ρ can be controlled, since the dopant concentration is inversely proportional with resistivity [16].

Subsequently, a 1 µm thickness of oxide layer is deposited, followed by opening of the anode area with the photolithography and etching process for electrode deposition. Next, boron is implanted with a dosage of 5×10^{15} cm^{-3}, anode junction drive in temperature and time for 1200 °C and 240 mins, respectively. After the anode junction is formed, the oxide layer is stripped off and then re-deposited with the same thickness. This re-deposited oxide layer is to react as the pattern oxide, followed by a 2 µm thickness of front metal Al layer, which act as the ohmic contact and a 1 µm thickness of Si_3N_4 nitride layer, which act as the passivation layer. All of these three layers are formed with photolithography and etching process. The final device structure is shown in Figure 3.

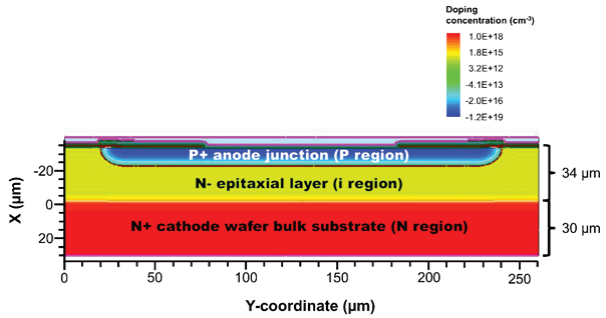


Figure 3: P-i-N diode structure with doping profile distribution.

2.2 Design of experiment and process split

Based on the simulated results, the devices are fabricated with a four corners matrix DOE to investigate the effects of W_D and ρ in order to achieve V_R above 300 V. In the fabrication process, the epitaxial layer is grown and diffused with dopant material on the wafer bulk as shown in Figure 4.

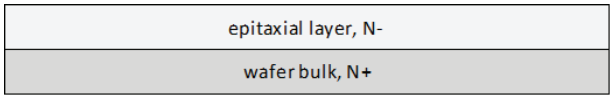


Figure 4: Wafer starting material with deposited epitaxial layer.

The DOE of the four corners matrix that includes the W_D and ρ is detailed in Table 2. As mentioned previously, the epitaxial layer dopant concentration and ρ are inter-related. The relationship between resistivity and phosphorus doping concentration has been studied for doped silicon as in [16]. Four corners matrix are groups of epitaxial layer covering the lower and upper specifications. It is used in the evaluation of the P-i-N diode performance when operating at the corners (lower or upper end) of epitaxial specifications as compared to the centre. Illustrations of total 5 groups with two level factorial DOE are shown in Figure 5 consisting of group A, B, C, D and E. The two factors (epitaxial layer thickness and resistivity) in low, centre and high condition. Design of experiments (DOE) is a systematic approach

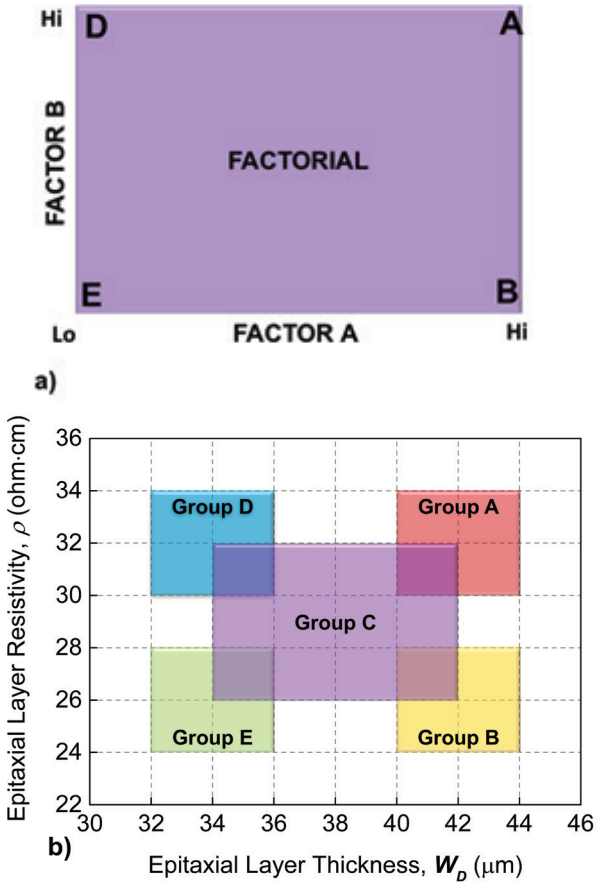


Figure 5: a) Two level factorials of DOE, Factor A and B refer to epitaxial layer thickness and epitaxial layer resistivity respectively. b) The location of four corners and centre of the evaluation samples consists of group A, B, C, D and E.

in engineering problem-solving that applies principles and techniques from the data collection stage. The output response from the data collection includes forward voltage, reverse breakdown voltage and reverse leakage current. The focus on the study is to increase the V_R during reverse bias without changing much of the V_F and I_R.

A total of 15 wafers lot are fabricated with the same P-i-N diode design at process corners with low/high W_D and low/high ρ. Afterward, the wafers are fabricated and electrically characterized. Electrical results of V_F, V_R, and reverse leakage current (I_R) are the main parameters of interest and then analysed with statistical software (for profiler study). The predicted profiler study is done to determine the dominant factor that affects the electrical performance and the optimal epitaxial profile. To ensure the repeatability of the result, each of the splits is repeated 3 times for the wafer fabrication and characterization.

3 Results and discussions

3.1 Simulation results

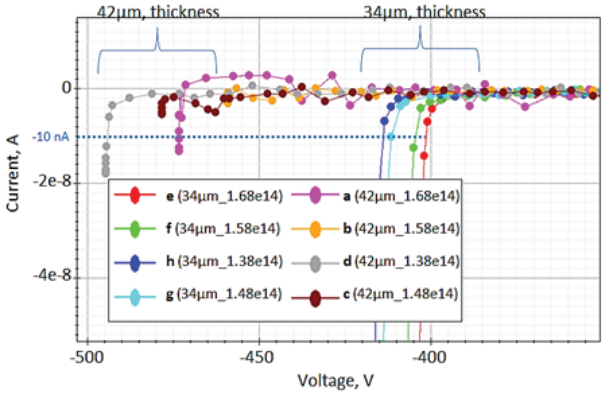
Figure 6 shows (a) reverse bias and (b) forward bias of the simulated I-V characteristics for different W_D and concentration of the N- epitaxial layer as tabulated in Table 1. In Figure 6 (a), a clear significant difference of the V_R with difference of W_D (i.e. 34 and 42 µm) is observed. At 10 nA (shown as dotted line), the 34 µm of W_D, results in lower V_R ranging from -400 V to -415 V. In contrast the 42 µm of W_D shows a higher V_R ranging from 460 V to 490 V. The increase of the W_D leads to an increment of the stored charges available and makes the diode to behave like a resistor [17]. According to Ohm's law and with the same current, the resistance is increased as a result of the increase in voltage. On the other hand, the increase of the dopant concentration N_D, from 1.38×10^{14} cm^{-3} to 1.68×10^{14} cm^{-3}, results in slight decrease of V_R. This shows that the W_D is more dominance factor affecting the V_R performance. Nevertheless, both impacts are in agreement with Equation (4) as previously explained.

Figure 6 (b) shows the forward bias results of the simulated diode. One can see that, significant impact is only related to the different W_D (i.e. 34 µm and 42 µm), while no variation can be observed for different dopant concentration. In comparison between 34 µm and 42 µm of W_D, 1) at low current of 200 mA (shown in the blue dotted line) regardless of the dopant concentration difference, V_F values of 870 mV and 880 mV, respectively. At low I_F biasing, the difference of the W_D results in a small change of V_F with the range of 10 mV difference. 2) The difference in V_F output response becomes widen

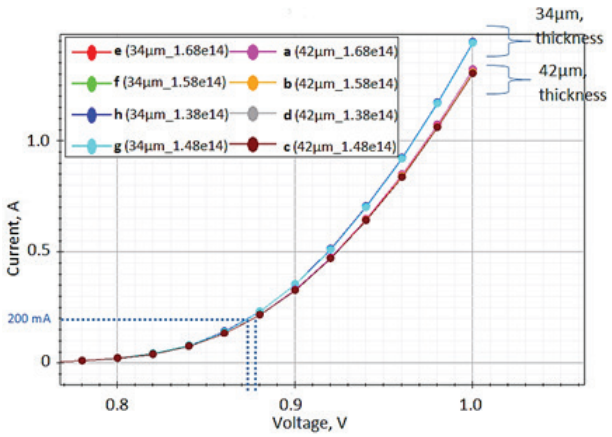
Table 2: Substrate 4 corner split table

Wafer#	Group	Description (Thickness/ Resistivity)	Target Thickness (µm)	Phosphorus dopant concentration (cm^{-3})	Conversion of dopant concentration to Resistivity (ohm·cm)	Target resistivity value (ohm·cm)	Exact Thickness value (µm)	Exact resistivity value (ohm·cm)
1	A	High / High	42	1.36×10^{14}	32.8	32	42.6	33.223
2	D	Low / High	34	1.36×10^{14}	32.8	32	34.34	30.093
3	C	Center / Center	38	1.58×10^{14}	28.2	29	37.95	28.742
4	A	High / High	42	1.36×10^{14}	32.8	32	42.6	33.223
5	D	Low / High	34	1.36×10^{14}	32.8	32	34.34	30.093
6	B	High / Low	42	1.68×10^{14}	26.6	26	42.15	26.524
7	E	Low / Low	34	1.68×10^{14}	26.6	26	33.85	25.723
8	C	Center / Center	38	1.58×10^{14}	28.2	29	37.89	28.742
9	B	High / Low	42	1.68×10^{14}	26.6	26	42.15	26.524
10	E	Low / Low	34	1.68×10^{14}	26.6	26	33.85	25.723
11	A	High / High	42	1.36×10^{14}	32.8	32	42.6	33.223
12	C	Center / Center	38	1.58×10^{14}	28.2	29	37.95	28.742
13	D	Low / High	34	1.36×10^{14}	32.8	32	34.34	30.093
14	E	Low / Low	34	1.68×10^{14}	26.6	26	33.85	25.723
15	B	High / Low	42	1.68×10^{14}	26.6	26	42.15	26.524

between various W_D with the increase of the I_F. This can be explained, when a P-i-N diode is forward biased, where holes and electrons are injected from the P and N regions into the i-region, which is represented as W_D. These charges do not recombine immediately. Instead, a finite quantity of charge always remains stored and results in a lowering of the ρ. So, the increase of I_F leads the decrease of the forward series resistance (R_S) [18]. The W_D plays a greater role to change the V_F with low resistivity.



(a)



(b)

Figure 6: I-V characteristics under (a) reverse bias and (b) forward bias for different W_D and dopant concentrations.

From the simulation, by changing the W_D and dopant concentration of the epitaxial layer, the V_R shows more significant difference compared to V_F. The reason being the P-i-N diode exhibiting reverse capacitance characteristics during reverse bias where dopant concentration and the W_D shows a more responsive curve. While forward biasing, P-i-N diode exhibits the forward series resistance characteristics where the difference of the W_D plays a greater role when the I_F is increased to a certain level [18], [19]. The phenomenon of the less responsive output on the forward bias is preferable as the focus on the study is to increase the V_R during reverse bias without changing the V_F.

With the confirmation of the theory through the TCAD simulation software, a wafer fabrication DOE has been conducted to validate the results by taking into account of the process variation and material variation.

3.2 DOE wafer results

From the DOE experimental results, in addition to V_R and V_F, and I_R are also considered. The statistical analysis, i.e. JMP profiler is used to analyse the effect of the W_D and ρ as shown in Figure 7. The line curve can be analysed by separating the two groups, which are W_D and ρ versus electrical responses. The x-axis of the chart represents the W_D, the ρ and the desirability of the responses. The curvature of the line in desirability row indicates how impactful the two factors (W_D and ρ) to the electrical output response of the device. The y-axis represents the electrical output response of V_R, V_F and I_R.

In Figure 7, W_D plays a dominant factor compared to the ρ in V_R and V_F. This is due to the V_R and V_F show more responsive curve on W_D compared to ρ. In other words, a greater gradient is observed in W_D line curve when compared to the ρ. However, the I_R change on both W_D and ρ is not significant (in nano-ampere range).

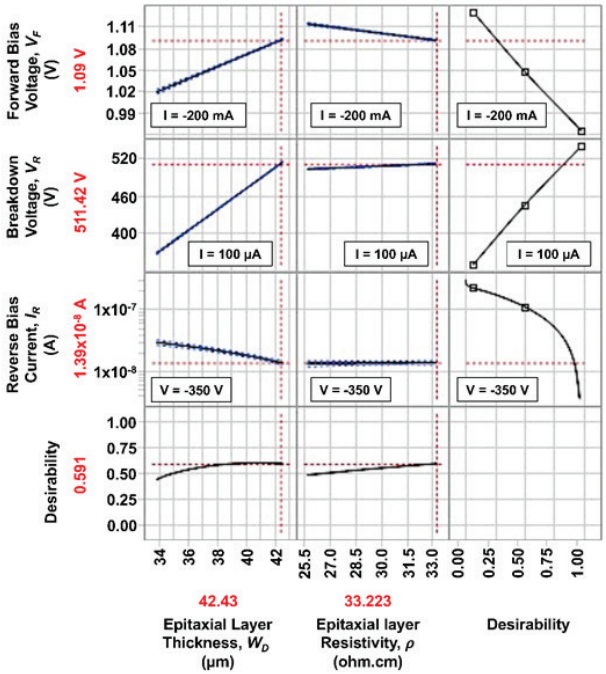


Figure 7: Statistical data on the impact of W_D and ρ on the fabricated devices.

As expected, by changing the W_D (34 µm to 42 µm), a significant difference on electrical performance for both V_F at 200 mA and V_R at 100 µA can be observed. This is related to the increase of the W_D results in the

V_R and V_F is also increased. Interesting to note that, an increase of V_F around 10 mV can be observed in Figure 7, is similar to the result obtained in simulation Figure 6 (b). With W_D increased from 34 µm to 42 µm, at 100 µA, the V_R shows almost similar response between simulations versus actual DOE. The voltage different between simulation and actual DOE is around 20 V is due to the uniformity of the boron pre deposition process.

In Figure 7, based on the statistical analysis JMP software, the V_R shows a significant improvement from 300 V to more than 500 V when replaced with W_D of 42.43 µm and the ρ of 33.22 ohm.cm.

From the DOE evaluation, both W_D and ρ in group A shows the optimum condition to achieved the desired device performance. The target W_D is 42 µm with window of 40–44 µm and the target ρ is 32 ohm·cm with window of 30–34 ohm·cm. The tolerance of ±4 µm of W_D and ±2 ohm·cm window are the narrowest tolerance, limited by process fabrication for this device. The small tolerance is preferable to reduce the process variation. With the fixed epitaxial layer substrate profile window, a total of 3 qualification lots with 5 wafers each have been fabricated in different time frames to monitor the process variation. All V_R and V_F are monitored at

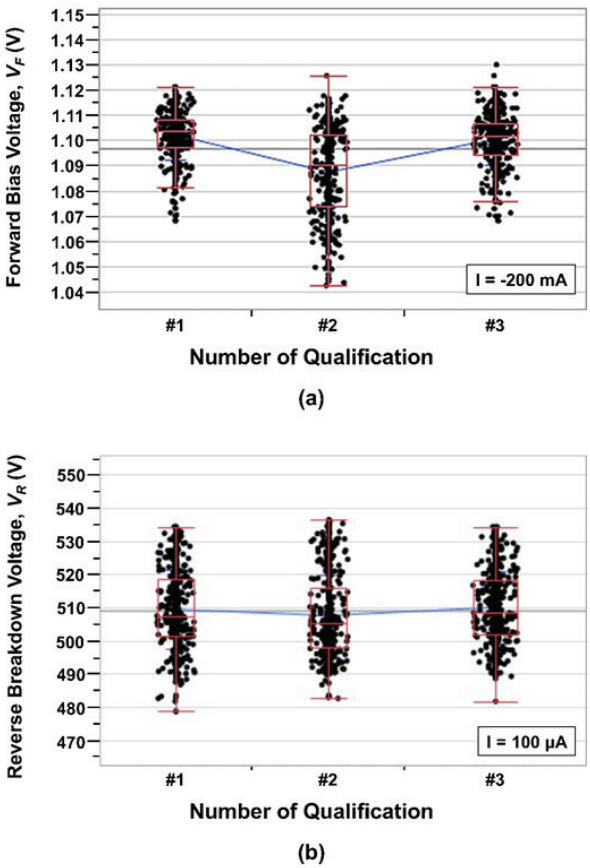


Figure 8: Qualification lot electrical distribution when (a) V_F at 200mA and (b) V_R at 100 µA.

wafer level electrical test. Based on the 3 qualification lots result shown in Figure 8, V_R and V_F electrical test result distribution are well within the specifications. The V_F distributions are less than 1.5 V and V_R distribution are above 450 V.

4 Conclusion

In summary, through the understanding of device behaviour and process TCAD simulation performance, the W_D plays a major role to increase the V_R when compared to the ρ. Further, the simulated result is validated through fabricated devices. To achieve beyond 300 V of V_R, the W_D is 42 µm and the target ρ is 32 ohm·cm.

A statistical analysis based on the electrical data was carried out to determine the best wafer substrate window. Subsequently, a validation process using 3 qualification lots is done. The V_R shows a significant improvement from 300 V to more than 500 V when replaced with the W_D of 42 µm and the epitaxial resistivity of 32 ohm·cm. The implementations of the new epitaxial specification have been successfully used to expand the product portfolio of this 300V P-i-N power switching diode that can be used in motor control, robotics and power distribution.

5 Acknowledgments

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2D Simulation Study of p-type TFTs with Chemically Deposited Poly-PbS Active Channel

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Abstract: In this work, the two-dimensional (2D) numerical simulation of p-type poly-PbS TFT electrical characteristics are performed using a physically based device simulator Atlas/Silvaco. The analytical expressions of defect density models for acceptor- and donor-like traps are defined for poly-PbS thin film material deposited with chemical bath deposition technique. The parameters of defect density model are optimized based on Levenberg-Marquardt algorithm to fit simulated and experimental results of TFTs. It is shown that the spatially uniform density of defect states method used for trapped charge evaluation in Atlas gives good agreement between simulated and experimental characteristics. An important presence of deep (Gaussian) acceptor- and donor-like density of states in poly-PbS band gap is confirmed. By controlling cation (donor-like) and anion (acceptor-like) vacancies of poly-PbS films could improved the performance of p-type TFTs.

Keywords: thin film transistor, simulation, density of states, optimization, defects, chemical bath deposition

2D simulacija TFT tipa p s kemijsko nanešenim aktivnim poli-PbS kanalom

Izvleček: Dvodimenzonalne simulacije električnih karakteristik TFT tipa p s poli-PbS so opravljene s simulatorjem Atlas/Silvaco. Analitični izrazi modelov stanj defektov za akceptorje in donorje so določeni za poli-PbS material, ki je nanešen s pomočjo tehnike kemijske kopeli. Parametri modela so optimizirani s pomočjo Levenberg-Marquardt algoritma tako, da se simulacije ujemajo z eksperimentalnimi meritvami. Izkazalo se je, da se rezultati prostorsko enotne metode v Atlas-u dobro ujemajo z eksperimentalnimi rezultati. Dokazana je bila pomembnost prisotnosti globoke Gausove porazdelitve defektov. Učinkovitost TFT-ja se lahko izboljša s kontroliranim vnosom vrzeli donorskega oziroma akceptorskega tipa.

Ključne besede: tankoplastni tranzistor, simulacije, gostota stanj, optimizacija, defekti

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1 Introduction

Thin film transistors (TFTs) are a growing technology in the flexible and large area of electronic fields, and recently they have been investigated mainly because of their low cost of production. Also, this technology is interesting due to the recent increase in the area of displays and its use to develop high-speed devices switching pixels, electroluminescent displays, active matrix displays, image sensors, and identification systems [1, 2].

There is a variety of thin film mature technologies in the market such as hydrogenated amorphous silicon TFTs (a-Si:H TFTs), polycrystalline TFTs (particularly low temperature), and organic TFTs (OTFTs). These technologies have advantages and disadvantages. For example, although a-Si:H TFTs have good uniformity, they have the disadvantages of insuficient mobility for driving a large screen LCD at a high speed, a large threshold voltage (V_{TH}) instability due to the desorption of hydrogen, and the absence of p-type semiconductor material for

Metal-Oxide-Semiconductor (MOS) technology. Furthermore, poly-TFTs have high mobility, but they have a drawback in that V_{TH} largely varies due to a process for crystallizing an active layer by annealing. Also, OTFTs have effcient p-type semiconductor materials, but they have the disadvantages that there is not a solution for n-type semiconductor material, they have V_{TH} in stability due to the oxidation of organic materials [3], and the organic molecules need to be aligned well at the interface or formed into large, low-defect grains, which is no trivial work.

Because some disadvantages are present in TFTs technology, researchers are looking for different options that can replace commercial materials and contribute to a better physical understanding of new materials for flexible electronics. The most important advantage of low temperature poly-TFTs technology is that it does not need expensive equipment of vacuum and high temperature processes, but printing or chemical bath deposition (CBD) techniques can still be used. In addition, CBD chalcogenide films are attractive for poly-TFTs for large area electronics given their simple fabrication, low temperature, and compatibility with most substrates. Moreover, chalcogenides materials are suitable candidates for their implementation in poly-TFTs because they have good electrical and morphological properties.

In particular, lead sulfide (PbS) chalcogenide is an important binary IV-VI semiconductor material with a direct narrow band gap [4]. It is also widely used in MOS transistors and optical devices [5], and it is one of the most widely studied semiconductos over the last decades [6, 7]. Recently, a p-type poly-TFT fabricated with PbS as semiconductor deposited by CBD technique was reported [8]. Using this technique, PbS thin films with photosensitive polycrystalline p-type conductivity can be obtained at room temperature.

Nevertheless, the CBD technique introduces structural defects (traps) during the deposition process, and numerous important electrical parameters of the TFTs are strongly affected by the density of defect states [9]. Besides, a model to predict and optimize the electrical characteristics of PbS poly-TFTs based on CBD technique is needed, so undoubtedly, device simulation tools are necessary to model and simulate a PbS poly-TFT. This work implements the 2D simulation of p-type poly-TFTs electrical characteristics using Atlas/Silvaco simulation models for Density of Defect (Trap) States (DDS).

2 Simulation of a p-type poly-PbS TFT

The simulated poly-PbS TFT is shown in Fig. 1, which has the same configuration of the fabricated device. It was fabricated in a bottom gate contact configuration by following these steps. First, 100 nm of Chromium (Cr) were deposited on the substrate. Second, the Cr film was patterned to define the gate contact. Third, 90 nm of hafnium oxide ($Hf\,O_2$) were deposited as gate dielectric. Then the PbS thin film was deposited by the CBD technique. After that, PbS and HfO_2 films were patterned and etched. Finally, 100 nm of gold (Au) were deposited and patterned to form the source and drain contacts. This process yields devices with channel widths (W) of 40, 80, and 160 μm and channel lengths (L) of 20, 40 and 80 μm. The detailed fabrication information of the p-type poly-PbS TFTs can be found in the literature [8]. However, in this work only the results of a TFT with W = 40 μm and L = 20 μm are reported. Also, the geometrical and technological parameters of simulated poly-TFT are listed in Table 1.

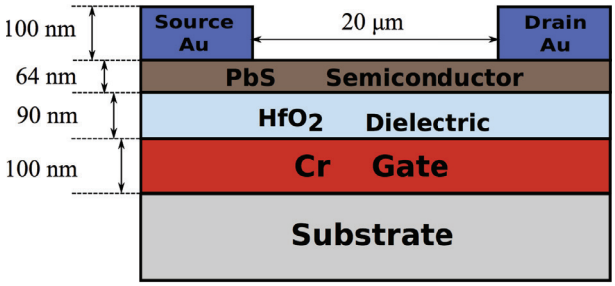

Figure 1: Cross section of PbS TFT simulated whit W=40 and L=20 μm. We used Cr as gate metal, $Hf\,O_2$ as dielectric, and Au as source - drain contacts.

2.1. Simulation Method

In this study the spatially uniform DDS method was adopted [10, 11]. It considers a polycrystalline PbS film as a homogenous material with an effective density of trapping states, which are uniformly distributed throughout the semiconductor layer of PbS. The advantage of this method is that it avoids complex mesh definitions of multigrain structures, which require the knowledge of the grain size. If the transistor has a long channel (>10μm), this method will be effective for simulations of poly-TFTs due to the large number of grains and grain boundaries. For instance, the thin PbS films used in the device fabrication have an average grain size of (~ 22nm) [8]. It results in the closely spaced grain boundary regions with increased defect densities and domination of carrier dynamics in the intergrain regions over the intragrain monocrystalline effects in the carrier transport. For this reason, the thin film of poly-PbS can be considered as a homogenous material with approximately uniformly distributed defect states.

Table 1: Device Parameters used in Simulation.

Parameter	Value
Channel length L (μm)	20
Channel width W (μm)	40
Gate oxide thickness t_{ox} (nm)	90
PbS thickness (nm)	64
Energy gap at 300 K (eV)	0.37
Dielectric constant	175
Low field hole mobility (experimental) (cm^2 /Vs)	0.09
Low field hole mobility (optimized) (cm^2 /Vs)	0.064
Gate workfunction ϕ_{ms} (eV)	4.4
Density of acceptor-like tail states N_{TA} (cm^{-3}/eV)	$1.74x10^{21}$
Density of donor-like tail states N_{TD} (cm^{-3}/eV)	$2.38x10^{17}$
Density of acceptor-like Gaussian states N_{GA} (cm^{-3}/eV)	$4.35x10^{18}$
Density of donor-like Gaussian states N_{GD} (cm^{-3}/eV)	$2.04x10^{18}$
Decay energy for acceptor-like tail states W_{TA} (eV)	0.0041
Decay energy for donor-like tail states W_{TD} (eV)	0.0104
Decay energy for acceptor-like Gaussian W_{GA} (eV)	0.0054
Decay energy for donor-like Gaussian W_{GD} (eV)	0.0040
Energy of Gaussian for acceptor-like states E_{GA} (eV)	0.20
Energy of Gaussian for donor-like states E_{GD} (eV)	0.20

2.2. Optimization Method

In the context of nonlinear least squares data fitting, the objective is to estimate a set of parameters $\theta=\{\theta_1,\ldots,\theta_m\}$ which minimizes the residual between the measured or experimental data *y*(*x*) and the predicted data $f(x;\theta)$

$$F(\theta)=\frac{1}{2}\sum_{i=1}^{n}\left(y_i-f(x_i;\theta)\right)^2$$

In particular the eval function $f(x;\theta)$ correspond to the numerical solution of the partial differential equation (PDE) of the simulator Atlas/Silvaco. The above equation can be generalized for multiple curve responses case; however, a simple notation was kept for simplicity. T he numerical determination of the set of parameters θ which minimizes F(θ) corresponds to the iterative Levenberg-Marquardt (LM) algorithm

$$\left(J^TJ+\lambda I\right)\delta\theta=-J^Tr \quad (1)$$

where *J* is the Jacobian matrix of derivatives of the residuals with respect to the parameters θ, the residual vector is *r*, the matrix identity is *I*, and the adaptive damping parameter is λ. The above procedure is a standard numerical scheme used to perform nonlinear data fitting, where the convergence properties relationship with the steepest descent and Gauss-Newton method are understood [12].

The Silvacos manuals do not explain how they code the LM algorithm; however, it is understandable that they employ finite dfferences schemes to approximate the partial derivatives on the Jacobian matrix. Besides, in modern computer simulators, each numerical solver are coded independently, this is the case on the Atlas/Silvaco tool, where the communication between the LM algorithm and the PDEs solver is achieved through files. Furthermore, at each time that the calculation of Jacobian or the residual evaluation is needed, it is required to solve numerically the PDEs, where the parameters are taken from a given data file. So, this procedure is general, and allows the interchange of numerical solvers without modify the rest of the programs.

3 Trap Density in poly-PbS Thin Film

A poly-PbS film consists of a number of small crystalline grains with boundaries. As mentioned before, this kind of materials contains a large number of defect states within the band gap of the material. Compared with the crystalline TFT, a much higher density of trap charge in poly-PbS dominates the Poisson's equation even when these devices work under the above threshold region [13]. In narrow gap materials, as PbS, the defects arise from variation in bond lengths, grain boundaries, dangling bonds (vacancies) and other microscopic point defects. The trap states exist within the crystal grains, but many are located at the front and back oxide interfaces and the grain boundaries [14]. Moreover, experimental methods reveal that the Gaussian (deep level) gap state exhibits distinctly a peak structure in some amorphous and polycrystalline oxide semiconductor [15].

Each kind of defect plays an important role in many electrical properties in semiconductors, serving as a scattering and/or a recombination center during transport. But also the vacancies, for example, acting as largely uncontrolled dopants and having the effect

on electron and hole mobilities [16]. Therefore, in order that the performance of TFTs based on chalcogenides thin films by CBD technique could be improved, the study of the native defects in the deposited thin films is undisputed.

3.1. Density of States Model

The total DDS distribution of trapping states $g(E_t)$ in the polycrystalline PbS films is taken to be composed of four bands: two tail bands (a donor-like valence band, $g_{TD}(E_t)$ and an acceptor-like conduction band, $g_{TA}(E_t)$), and two deep Gaussian level bands (one acceptor-like, $g_{GA}(E_t)$ and the other donor-like, $g_{GD}(E_t)$) by

$$g(E_t) = g_{TD}(E_t) + g_{TA}(E_t) + g_{GA}(E_t) + g_{GD}(E_t) \quad (2)$$

$$g_{TA}(E_t) = N_{TA} exp\left(\frac{E_t - E_c}{W_{TA}}\right) \quad (3)$$

$$g_{TD}(E_t) = N_{TD} exp\left(\frac{E_v - E_t}{W_{TD}}\right) \quad (4)$$

$$g_{GA}(E_t) = N_{GA} exp\left[-\left(\frac{E_{GA} - E_t}{W_{GA}}\right)^2\right] \quad (5)$$

$$g_{GD}(E_t) = N_{GD} exp\left[-\left(\frac{E_t - E_{GD}}{W_{GD}}\right)^2\right] \quad (6)$$

where E_t is the energy of trap, Ec is the conduction band energy, Ev the valence band energy and, the subscripts (T, G, A, D) stand for tail, Gaussian (deep level), acceptor- and donor-like trap states, respectively.

The donor-like traps are positively charged (cation vacancy); therefore, they can only capture electrons. They are positive when unoccupied by an electron, but they are neutral when occupied. On the other hand, acceptor-like traps are negatively charged (anion vacancy); therefore, they can only emit an electron. They are negative when occupied, but they are neutral when unoccupied. The capture and emission processes are predicted by Atlas simulator using the Shockley-Read-Hall (SRH) recombination model.

In the steady-state, the probability of occupation of a trap level at energy E_t for the tail and deep states is given by Fermi-Dirac (FD) occupation function [17]. The total trap charge $Q_T = q(n_T - p_T)$ is evaluated in Atlas by following these steps. First, the density of ionized acceptor- and donor-like states is simply the product of $g(E_t)$ and the FD occupation function. Then this product is integrated to obtain the density of carriers (n_T and p_T) over all possible energies within a band gap. Finally, the total trap charge Q_T obtained is subtracted from the right hand side of Poisson's equation. Q_T is also used to modify the standard SHR model in order to account for electrons and holes being emitted and captured by the acceptor and donor-like traps.

4 Simulation Results

The 2D numerical simulations of p-type PbS poly-TFT device were performed with Atlas/Silvaco simulator. The iterative Marquart algorithm (1) was used to determine the parameters N_{TA}, N_{TD}, N_{GA}, N_{GD}, W_{TA}, W_{TD}, W_{GA} and W_{GD} of the DDS model (2)-(6) numerically. So, it was necessary to propose the initial, maximum and minimum values of each parameter. These values were proposed according to the data reported by some authors that analyze the electronic properties of nanocrystalline PbS films where the DDS is extracted from experimental data [18, 19, 20]. As a result, the set of parameters, which best fit the experimental drain current (I_{DS}) of p-type TFT as function of both drain-source voltage V_{DS} and gate-source voltage V_{GS} were obtained and are listed in Table 1.

The example of simulated and measured I_{DS} - V_{DS} output characteristics after the optimization of DDS model are displayed on Fig. 2. Having in mind the large tolerances in physical and geometrical parameters of experimental devices obtained from fabrication process, a good agreement between simulated and measured results is achieved in Fig. 2. The optimized simulation results indicate that the spatially uniform DDS method with simplified mesh generation is suitable choice for numerical simulations of long channel and thin film poly-PbS TFTs.

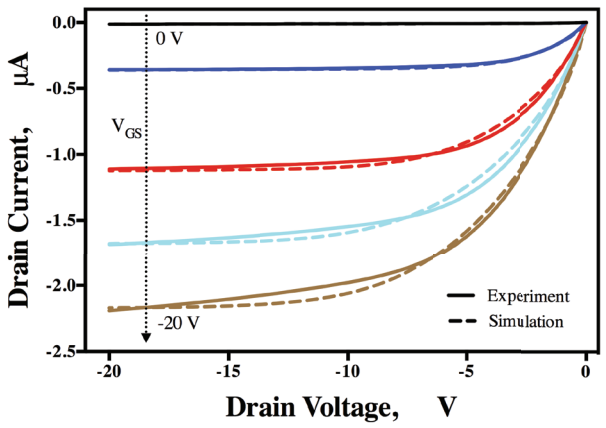

Figure 2: Simulated and experimental I_{DS}-V_{DS} characteristics of poly-PbS TFT device.

The optimized tail and deep density distributions of acceptor- and donor- like trap states for the simulated poly-PbS TFT are depicted in Fig. 3. As can be seen the density profile of defects across the forbidden gap of poly-PbS has a shape of two tail band edges and two deep levels near the midgap. The exponential band tails stem from the structural disorder in the lattice while the deep defect bands arise from impurities. Deep defects are very important for narrow band gap semiconductors [21]. The impurities and native point defects (vacancies and interstitials) are largely associated to deep traps. The deep levels can capture holes or electrons and hence acts as an electron/hole trap, which clearly affects the device performance. Fig. 3 shows that Gaussian (deep) defect bands of poly-PbS film have a peak structure, which agree with the study presented in [15].

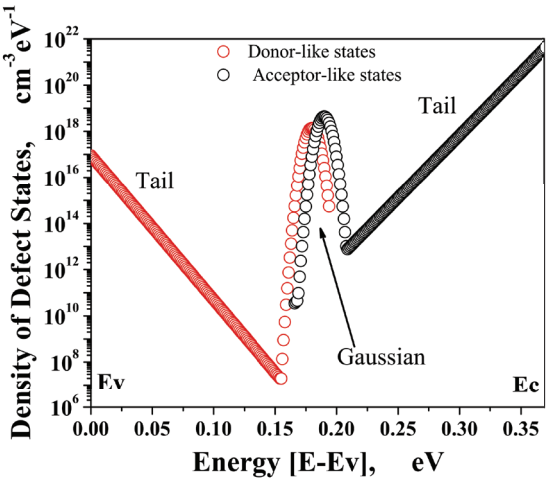

Figure 3: Optimized tail and Gaussian density distributions of acceptor- and donor-like trap states in poly-PbS TFT.

The energy-band diagram for p-type PbS MOS structure under thermal equilibrium V_{GS} = 0 (a) and accumulation regime V_{GS} < 0 (b) is shown in Fig. 4. If V_{GS} = 0 the semiconductor Fermi level E_F is near valence band and from Fig. 3 can be seen that the charge neutrality level (CNL) (the crossing point at which acceptor- and donor-like densities of states are equal) is located near midgap. For V_{GS} < 0, the bands bend upwards, drawing CNL away from E_F as shown in Fig. 4(b). As can be seen E_F lies below CNL, and ionized empty deep donor-like states build up a large positive interface charge. That is, the FD function of deep donor-like trap, which means the probability that the trap is not occupied by an electron, is increased as negative V_{GS} increases. Moreover, theorical results of [22] predict that S vacancies (acceptor-like traps) act as n-type PbS, whereas Pb vacancies (donor-like traps) act as p-type PbS.

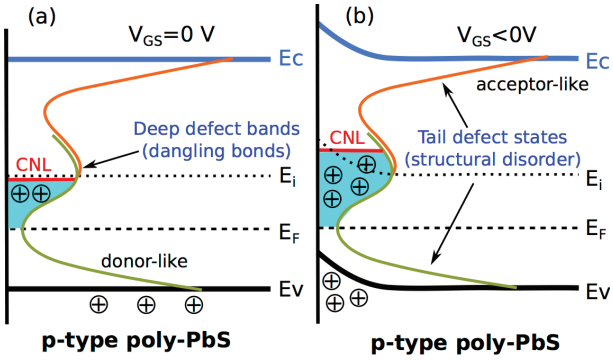

Figure 4: Energy band diagram drawn in scale for p-type PbS MOS structure (a) for $V_G = 0V$ and (b) for $V_G < 0$ (accumulation regime). Here, only the semiconductor and the interface with the oxide insulator are shown.

In Fig. 5 we display the simulated hole mobility (μ_p) as a function of transverse electric field ($E_\perp$) and V_{DS} (inset). We can notice that μ_p shows a strong dependence on $E_\perp$ and it is considerably lower than the mobility of crystalline TFTs. This behavior can be explained by considering that for a small negative *VGS* most of the charges are trapped. When V_{GS} becomes more negative, eventually more trap states become ionized (see Fig. 4). In this situation the effect of traps vanishes and the mobility remains almost constant with negative V_{GS}. The inset of Fig. 5 shows μ_p as a function of V_{DS} at different V_{GS} (-5V, -10V, -15V and -20V). It can be seen that μ_p has the correct behavior and it is well predicted by Atlas simulator. Both experimental and optimized (simulation) low field hole mobilities (μ_{p0}) are shown in Table 1.

In Fig. 4 is shown that tail donor-like states are located under E_F. So, they are occupied by an electron, and they are neutral; similarly, tail acceptor-like states are located above the E_F. So, they are unoccupied, and they are also neutral. So, in p-type PbS TFTs deep density states play an important role in charge transport [23]. For this reason, only the effect of different values of Gaussian density states on the transfer characteristics of the poly-PbS TFT simulated are shown in Figs. 6 and 7. As mentioned before, under low negative V_{GS}, most of the induced charge is trapped in deep states, the dominant term in Poisson equation is the density of traps n_{deep} and p_{deep}. Therefore, the sub-threshold characteristic of poly-PbS TFT can be improved by reducing both density of deep states and film thickness.

As the deep acceptor-like traps were increased, the states of electron capture (minority carriers) are increased and they cause less leakage current (see Fig. 6). Nevertheless, no significant change was observed in transfer characteristics of TFT when the deep acceptor-like traps were reduced. Accordingly, the effect of acceptor-like traps is less important in a p-type poly-PbS

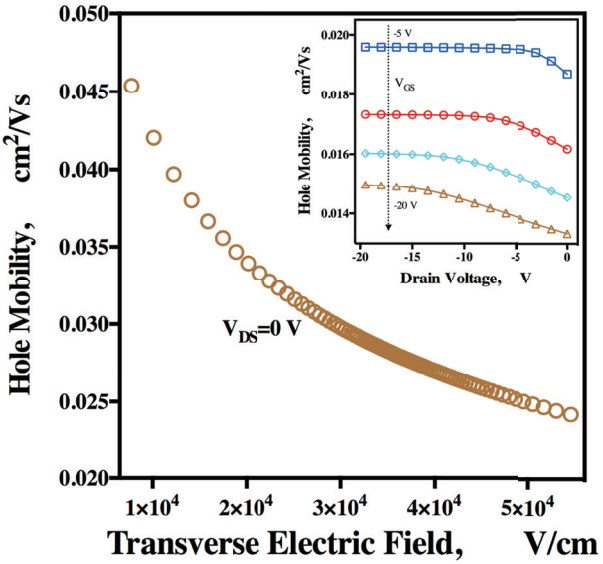

Figure 5: Hole mobility as a function of transverse electric field obtained from Atlas simulator. The inset compares the dependence of V_{DS} on hole mobility at different values of V_{GS}.

TFT in the accumulation regime. On the other hand, larger deep donor-like traps means larger positive ionized states. Notice that this situation states both less holes and less mobility in the channel (see Fig. 7). Furthermore, the total current of poly-PbS TFT is reduced. Whether the deep donor-like traps are reduced, the total current is increased, yet the V_{TH} shifts to positive values. Moreover, although the experimental and simulated value of V_{TH} is positive, it should be negative (accumulation regime). A similar conclusion about the effect of deep traps on V_{TH} behavior is presented in [24] for TFTs with cadmium sulfide (CdS) films, as

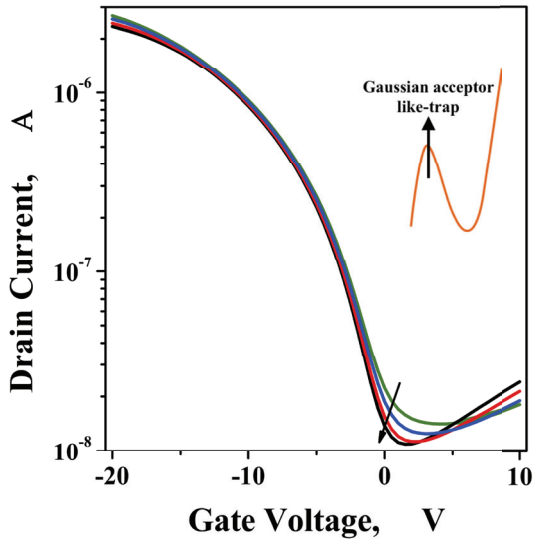

Figure 6: Transfer characteristics of the poly PbS TFT simulated as a function of V_{GS} for different values of deep acceptor-like traps (increased).

active channel, deposited by CBD technique. Because the deep traps affect the device performance by either doping the PbS film or acting as trap sites, both acceptor- and donor-like traps should be controlled in order to improve the p-type poly-PbS TFT electrical characteristics.

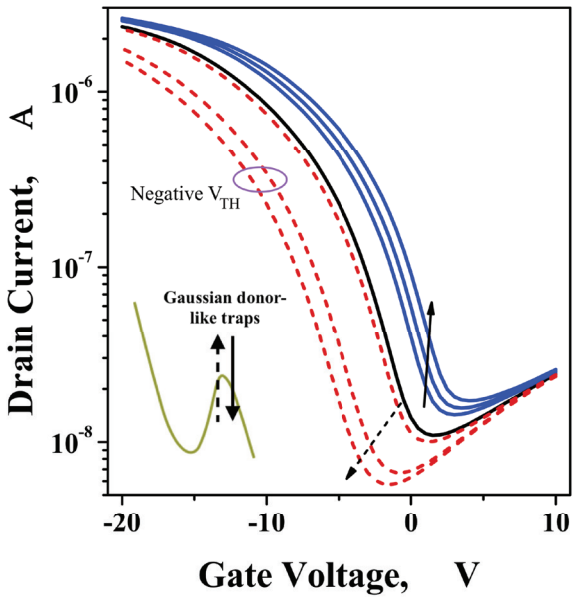

Figure 7: Transfer characteristics of the poly PbS TFT simulated as a function of V_{GS} for different values of deep donor-like traps (increased and reduced).

Fig. 3 shown that the point defects act as deep traps states situated at different energy depths within the forbidden gap, thereby influencing the principal parameters of poly-PbS TFTs (V_{TH} , mobility, I_{on} /I_{off} ratio and mobile charge density). It is demonstrated that after thermal annealing the electrical properties of thin films deposited by CBD are improved [8, 24]. This is attributed to the change in larger grain size, lattice parameter and crystalline structure along with a reduction of defects. Nevertheless, some defects are still present in the thin film and longer annealing times might be necessary to eliminate the vacancies or interstitials. In addition, a significant amount of S or Pb (anion or cation) vacancies could be created in the PbS films as function of the environment used during the synthesis, sulfur-poor or lead-poor. Also, the velocity of ions in a solution should be considered in order to control the S and Pb vacancies in the thin films deposited by CBD technique.

5 Conclusions

To sum up, the p-type PbS poly-TFT's electrical characteristics can be predicted with physically based two-dimensional device simulator Atlas using the embedded

density of defect models. The spatially uniform density of defect states method used for trapped charge evaluation and the parameter optimization of density defect model give a good agreement between simulated and experimental characteristics. Also, it is clear that the deep density of states in poly-PbS band gap affects the electrical characteristics of p-type TFTs. The high density of deep donor-like states (cation vacancies) found to be degrading device performance while it is not a concern for deep acceptor-like states (anion vacancies). The cation vacancies act as a deep electron donor, which affect the p-type device performance. To optimize the design of p-type PbS poly-TFTs both anion and cation vacancies should be controlled. These findings are important for the better understanding of TFTs based on calchogenides materials deposited by chemical bath deposition technique.

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Testing and Characterization of Multilayer Force Sensing Resistors Fabricated on Flexible Substrate

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Abstract: This paper presents design, fabrication and characterization of force sensing resistors (FSRs) which can be used in many applicable devices in medicine, rehabilitation, robotics, dentistry, etc. They consist of printed interdigitated electrodes on flexible substrate, an adhesive spacer and a carbon based sensing layer. Four types of FSRs were fabricated with different designs of active area. Measurement setup for testing and characterization has been developed in laboratory conditions and represents a device for precise implementation of a controlled force on FSRs. The characteristics of FSRs - the resistance as a function of applied force and temperature as well as the voltage as a function of applied force are presented. The obtained resistances were in the range of tens of Ohms for a wide range of applied force (1 N – 65 N).

Keywords: Electronic component; Materials; Force Sensing Resistor (FSR); Flexible substrate; Characterization

Preizkušanje in karakterizacija večslojnih uporovnih senzorjev sile izdelanih na fleksibilnih substratih

Izvleček: Članek predstavlja dizajn, izdelavo in karakterizacijo uporovnih senzorjev sile (FSR), ki se jih lahko uporabi v številnih aplikacijah v medicini, robotiki, zobozdravstvu… Sestaljeni so iz tiskanih prepletenih elektrod na fleksibilnem substratu, lepljivim distančnikom in senzorsko plastjo na osnovi ogljika. Izdelani so bili štirje tipi senzorjev glede na obliko aktivne plasti. Vzpostavljeno je bilo merilno in karakterizacijsko orodje v laboratorijskem okolju, ki omogoča natančno implementacijo kontrolirane sile na FSR. Prikazane so karakteristike FSR – upornost kot funkcija sile in temperature ter napetost kot funkcija sile. Upornosti so v razredu ohmov za široki razpon uporabljenih sil (1 N – 65 N).

Ključne besede: elektronske komponente; materiali; uporovni senzor sile; fleksibilen substrat; karakterizacija

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1 Introduction

Force and position sensing are an integral part to a wide range of measurements. Force sensing resistors (FSRs) have been used in a number of force sensing applications in many fields, such as medicine, rehabilitation, robotics, etc. [1-3]. FSRs are devices that allow measuring static and dynamic forces applied to a contact surface. Their range of responses is basically depending on the variation of its electric resistance. The FSR is usually a flat, flexible device that exhibits decreasing electrical resistance with increasing force applied normal to its surface. Some of the most popular commercial types of FSRs are: FSR Interlink Electronics [4], FlexiForce-Tekscan [5] and PS3-LuSense [6] sensors. A commercial FSR encompasses of two layers, namely a conductive surface and the printed electrodes. Both are facing each other which allow a contact between two surfaces. This results in the conductive layer of the printed electrodes short circuit to reduce the electric resistance upon force pressure. Usually, the resistance dropped from 1 MΩ to 10 KΩ for the applied force is in the range from 1 N to 10 N. FSRs are available in a few different shapes such as round, square and strip and their small thickness and mechanical flexibility allow them extensive applicability. Force sensors are widely used in the robotic field, particularly for robot interaction control application. A study has been conducted in [7] to utilize the Tekscan Flexiforce and the Interlink FSR sensors in robotic and

biomechanical applications. Two different set of experiments (the hardness detector system and the force-position control system) were carried out in [8] to test the effectiveness of the Flexiforce and Interlink sensors. Characteristics of three types of force-sensing resistors (Interlink FSR - Standard 402, FlexiForce - A201, LuSense PS3 - Standard 151) were identified in [9] for usage in a refreshable and portable E-Braille device that can assist the blind and visually impaired persons. An effective technique that improves reliability and accuracy of measuring compression force using FSRs (Interlink Electronics) was presented in [10], for biomedical and industrial design applications where measurement of finger and hand force are needed. In the paper [11], authors reported FSRs that are adequate to be part of wearable components. Authors focused on the sensing technologies that are compliant with the integration inside garments or other kinds of clothing (i.e., shoes, backpacks). Two different force sensitive resistors: FSR 406 (produced by Interlink Electronics) and A401 (from Tekscan) were evaluated in [12], while demonstrating gaits of healthy individuals through their loading behaviour. The flexible tactile force sensors presented in [13], were fabricated using a moulding process of a composite material, which is a mixture of two components: conductive ink and silicon elastomer, expressing good linearity and repeatability. A system with force sensors (Tekscan FlexiForce), which are placed on the hands rather than on objects, allowed improvements in versatility and spatial resolution to be made in measuring forces developed by human hand, was presented in [14]. The system has been successfully used to measure forces involved in a range of everyday tasks such as driving a vehicle, lifting a sauce pan, or hitting a golf ball. A wearable arm device that equipped with a monitoring system for post-stroke rehabilitation was designed and proposed in [15]. The device was equipped with an Interlink FSR sensor along with other sensors such as flex sensor and accelerometer. In the paper [16], FSRs were used to detect the transitions between five main phases of gait for the control of electrical stimulation while walking with several children with cerebral palsy. The paper [17] described testing of a bite force sensor based on force sensing resistor. The sensor surfaces were manufactured in silicone material that had mechanical properties similar to those of tough foodstuffs. The instrument has such clinical merits, as to favor its use in experimental clinical studies on the biomechanics of prosthetic applications. An electrolarynx which can change intensity as well as frequency simultaneously during conversation was described in [18]. A specialized FSR sensor was used to make possible controlling frequency and intensity simultaneously by applying pressure to the button. This system can be used as one of the rehabilitation methods for laryngectomees. From above-mentioned review of open literature it can be concluded that there are a huge interest for application of FSRs and consequently their custom-made innovative design.

This paper proposes various designs of FSRs on mechanically flexible substrate which can be exposed to a wide range of applied force (up to 65 N). The four types of FSRs were fabricated on the foil (Kapton film), with very low value of resistance in a wide range of applied forces. In-house measurement setup tool has been developed for determining characteristics of these FSRs. Comparison of their performances was performed with reference to resistance vs. applied force curve as well as changing these graphs with increasing the operating temperature which is very important from application point of view.

The article is organized as follows. Section 2 describes design and fabrication procedure of the proposed FSRs as well as measurement setup tool used for characterization of the manufactured force sensing resistors. Discussion of obtained results is presented in Section 3. The concluding remarks are given in Section 4.

2 Experimental

2.1 FSRs design and fabrication

In this paper, four different designs of force sensing resistor were proposed, as can be seen in Fig. 1. First two structures are round and they have different shapes of interdigitated electrodes, while the third structure has square shape active area (Fig. 1c). The fourth structure has 4-zones active area, and just first zone has been used for testing, shown in Fig. 1d.

Table 1: Dimensions of 4 different types of FSRs

	1st type of FSR	2nd type of FSR	3rd type of FSR	4th type of FSR
Active area diameter/surface (mm)	12.7	12.7	24 x 24	18 x 18
Length of structure with terminals (mm)	51.4	51.4	63.4	38.83
Width of interdigitated electrodes (mm)	0.4	0.2	0.4	0.36
Distance between interdigitated electrodes (mm)	0.4	0.5	0.3	0.27

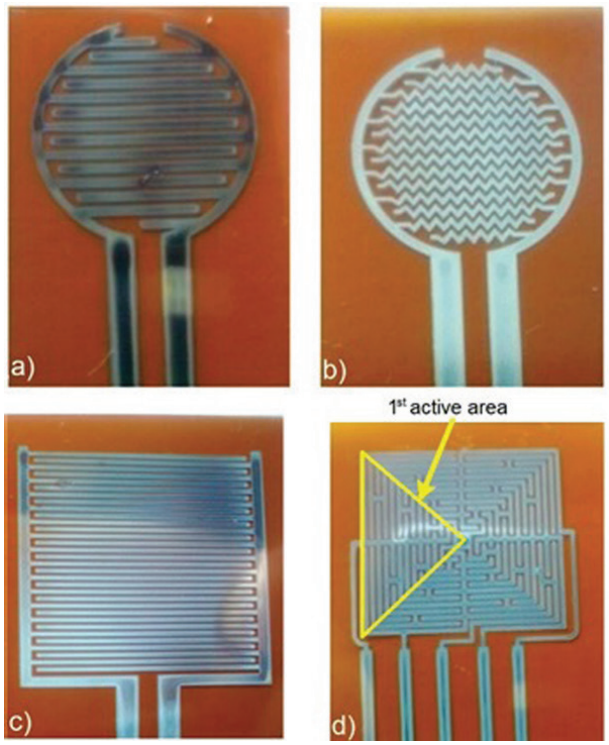


Figure 1: Four different structures after sintering: a) 1st type of FSR, b) 2nd type of FSR, c) 3rd type of FSR and d) 4th type of FSR, respectively

Dimensions of four types of fabricated sensors are shown in Table 1. All FSRs were manufactured by inkjet printing using Dimatix deposition material printer - DMP3000 [19] and RK Control printing proofer - RK K [20].

The first layer of the sensor was fabricated by printing of commercially available SunChemical silver nanoparticle ink with 20 wt% - Jet Silver U5714 [21]. Thickness of polymide film for active area was 75 µm. The resolution of the inkjet process using DMP-3000 printer is mainly governed by the nozzle diameter (approximately the droplet diameter) and the statistical variation of the droplet flight and spreading on the substrate. In case of printing with silver nanoparticle ink the minimum droplet diameter was around 36 µm, and drop spacing was 18 µm (from center to center) obtained by changing the printhead angle. Silver interdigitated electrodes for the first FSR's layer were printed and sintered at 240 °C for 30 min. The second sensor's layer was fabricated by printing of carbon ink using RK K printing proofer on 50 µm GTS polyimide film [22]. Carbon ink has been printed in several layers (three) on GTS film, shown in Fig. 2a. After fabrication both layers have been attached using two component epoxy glue, which has been mounted around the edges of the active area, shown in Fig. 2b. When the two substrates are pressed together, the microscopic protrusions on the FSR ink surface shorten across the interdigitated fingers of the facing surface. At low forces, only the highest protrusions make contact, while at higher forces, there are more and more contact points between the two substrates. The result is that the resistance between the electro conductive segments is inversely proportional to the applied force. The contact wires were mounted using silver paste, for testing purpose, at the ends of silver conductive lines and after finishing these steps, the four types of fabricated FSRs can be seen in Fig. 2c.

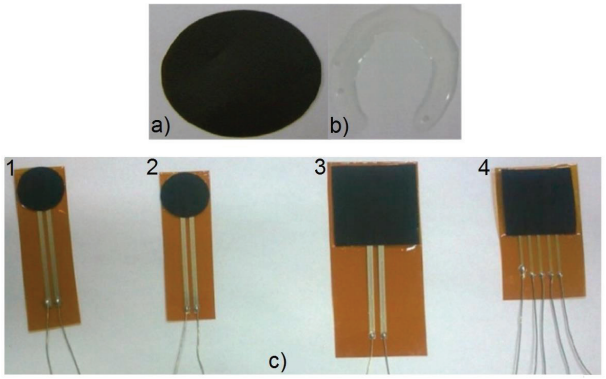


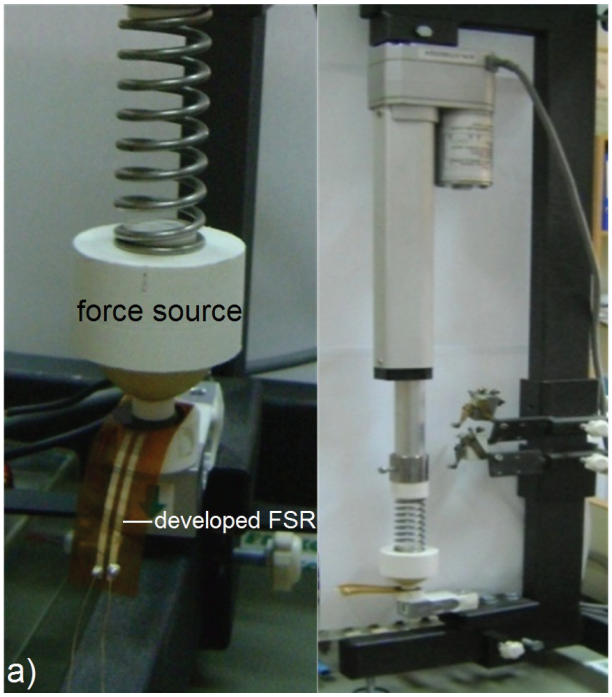
Figure 2: a) Printed carbon ink, b) mounted two component epoxy glue and c) four types of FSR sensors after manufacturing, respectively

2.2 Characterization techniques

The following instruments have been used for materials characterization: (1) for structural characterization - scanning electron microscope (SEM), JOEL JSM 6460 LV scanning microscope with EDS; (2) for mechanical characterization - nanoindentation, Nanoindenter G200, which uses the Berkovich diamond indenter with a face angle of 65.27°.

2.3 Measurement setup

The force sensing resistors testing were performed using an innovative in-house developed measurement setup shown in Fig. 3. It consists of a rigid frame, linear electric actuator with position feedback, spring, actuator sensor holder and reference force sensor. The complete system also includes digital electronic system control and operator control software (user friendly in-house developed software tool, entitled Forcer) shown in Fig. 4, which allows position change and changing of applied force [23]. Resistance and voltage of fabricated sensors were measured using multimeter (shown in Fig. 3b). For the purpose of measurements a voltage source was used (Fig. 3b). Force used for measurements was applied to the fixed part or all over the active part of the sensor.



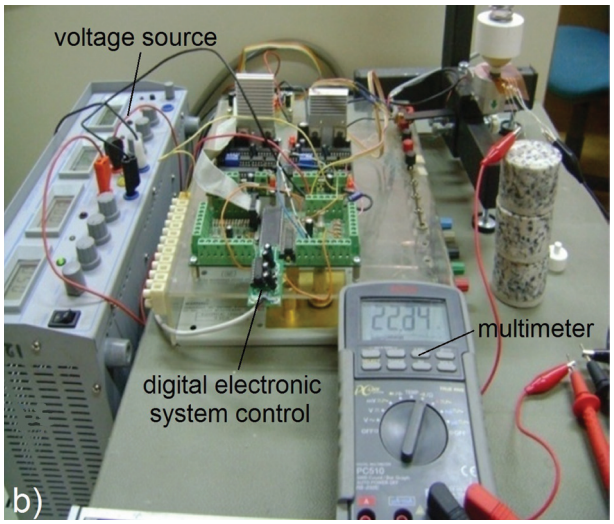


Figure 3: a) Positioning FSR and b) complete measurement setup

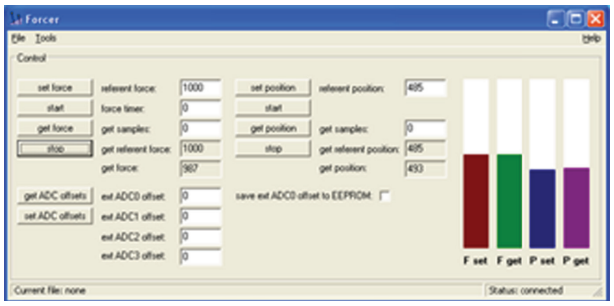


Figure 4: In-house developed software tool for controlling the measurement process.

For resistance as a function of force, measurement set-up described at the beginning of this section was used, and for voltage as a function of force, as addition to the setup, a voltage divider circuit which was connected to fabricated FSR, shown in Fig. 5, was used. The measuring resistor, R_M, is chosen to maximize the desired force sensitivity range and to limit current. For resistance as a function of temperature heat source was used to reach the desired temperature and an IR camera was used to monitor temperature variations.

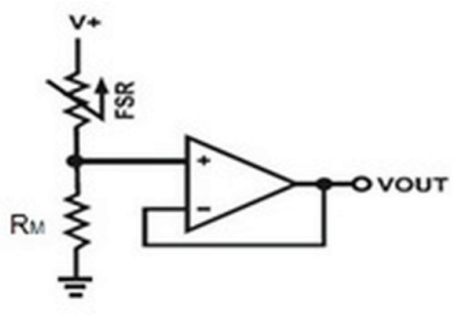
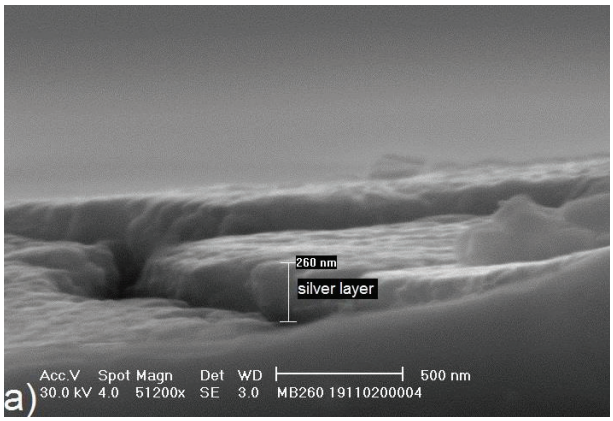


Figure 5: FSR voltage divider circuit



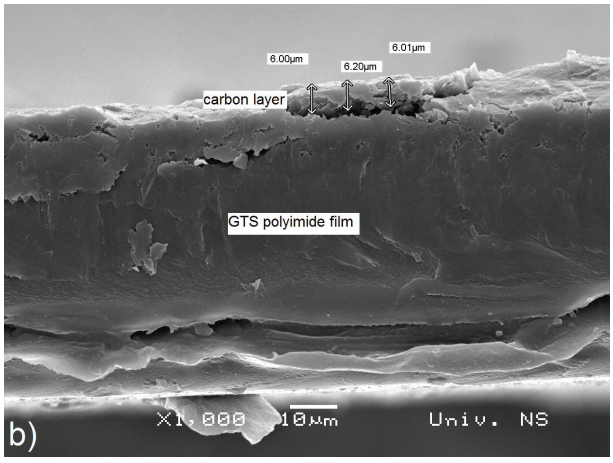


Figure 6: SEM micrographs of a) silver interdigitated electrodes, b) carbon layer

3 Results and discussion

3.1 SEM results

With the aim to determine the exact thickness of silver conductive layer as well as carbon layer, scanning electron microscopy (SEM) was conducted. SEM micrographs are presented in Fig. 6. It can be seen from this figure that thickness of silver layer was around 260 nm, whereas the thickness of carbon layer was around 6 µm.

3.2 Mechanical characterization results

Bearing in mind that FSRs will be exposed to different mechanical stress during the practical application, their mechanical characterization was performed by means of nanoindentation. We used an Agilent Nano indenter G200 to investigate mechanical properties of sintered silver layers as well as carbon layers. Multiple indentation (at least 10 indentations were made) tests provide measurement repeatability for the mechanical properties of analyzed samples/layers. Nanoindentation tests were conducted with a Berkovich diamond indenter, which ensures a precise control over the indentation process. Fig. 7a shows load-displacement curves measured on the silver layer, whereas Fig. 7b presents load-displacement curves measured on the carbon layer.

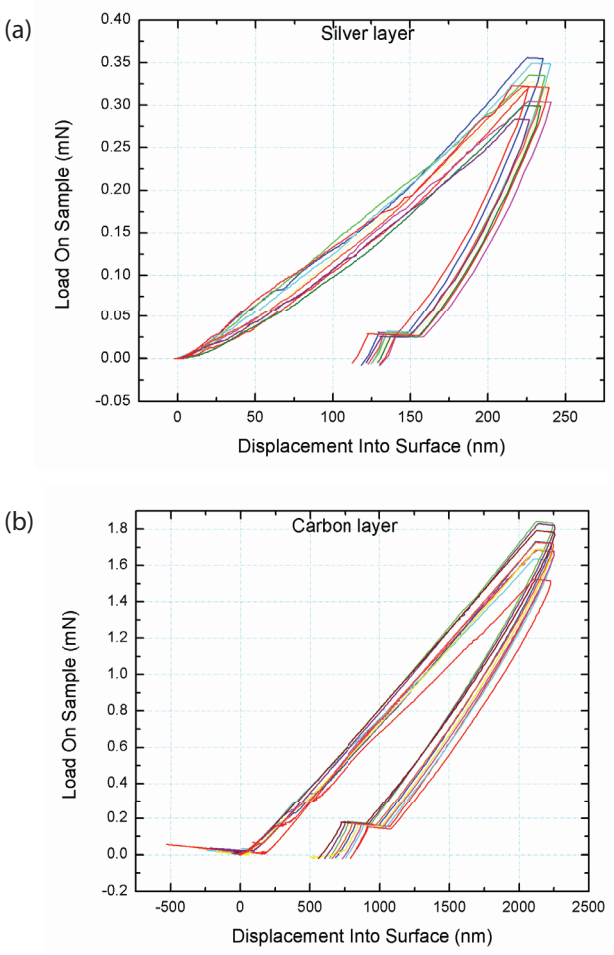


Figure 7: Load-displacement curves for a) silver interdigitated electrodes, b) carbon layer

It can be seen from Fig. 7a that maximum load on silver layer was at 0.35 mN and corresponding maximum depth of penetration was around 240 nm, which confirm that we did not reach the substrate (the thickness of this layer is around 250 nm). Fig. 7b presents load-displacement response for carbon layer for a maximum load of about 1.8 mN and the penetration depth was about 2.25 µm (which is around one third of the thickness of this layer). These force-displacement curves confirm repeatability of obtained results.

3.3 Resistance/Voltage vs. force results

A typical FSR's characteristic represents dependence of resistance vs. force, thus we analyzed firstly this behaviour of the proposed sensors. The resistance as a function of force characteristic for four types of FSRs, at room temperature, is depicted in Fig. 8. Three areas of different sensor behaviour can be distinguished. The first area is leftmost area in which the resistance is high and the sensitivity is also very high. This area has nonlinear properties of a dead lash at the beginning of the area characterized by a breaking force that introduces the sensor in the high sensitivity area. The component abruptly switches into the second – the regular area, which is commonly used for sensing. In this area the conductance fairly linearly depends on the applied force (force difference). Finally, when excessive force is applied, the component starts to saturate. The transition to the saturation is not abrupt, but rather gradual [24]. Fig. 8 shows that resistance of sensor decreases

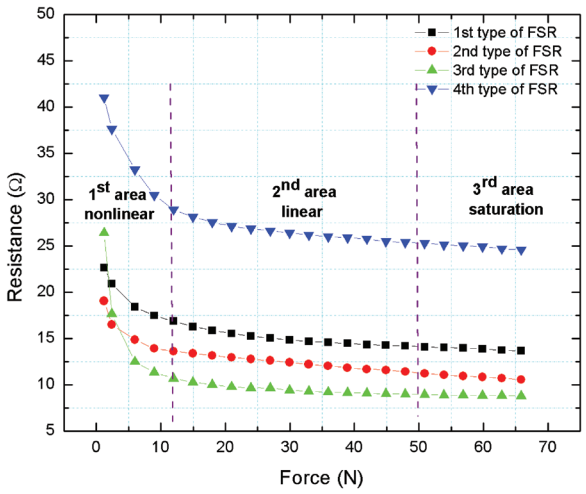


Figure 8: Resistance as a function of force for four types of FSRs

with an increase in force, and it can be observed for all types of analyzed FSRs.

The force range was from 1.19 N to 65.7 N and the same range was used for all four types of FSRs. This force was implemented on FSRs by means of in-house developed system, presented in Fig. 3. In Fig. 8 is visible that the third type of FSR, which has the largest active area, has lowest resistance, 8.81 Ω when applying maximal force, while the fourth type of FSR, with smallest analyzed active area, has resistance of 24.81 Ω when applying the same force. For practical application point of view and connecting with electronic circuits, it is important to have voltage-force characteristics. FSRs are usually configured in voltage divider circuits for simple resistance-to-voltage conversion, as already shown in Fig. 5. Voltage change due to change in force for several values of R_M resistor (depicted in Fig. 5), which allows voltage change in the whole range, is presented in Fig. 9 and 10. Moreover, Fig. 11 depicts voltage as a function of applied force for proposed types of FSRs, for constant values of R_M equal to 18 Ω.

The voltage increases with the increase of applied force, which can be seen using voltage divider equation:

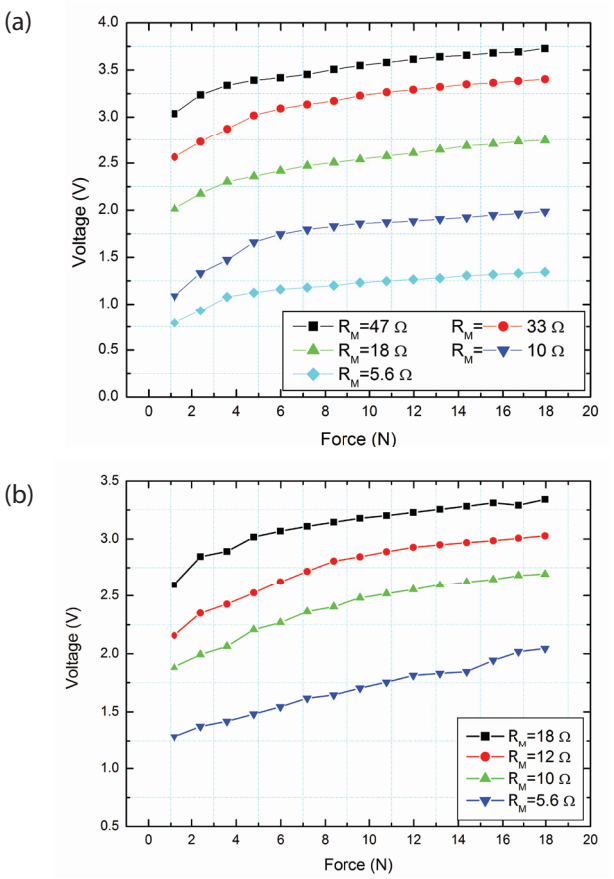


Figure 9: Voltage as a function of force characteristics for: (a) 1st type of FSR, (b) 2nd type of FSR

$$V_{out} = \frac{V_+}{1 + \frac{R_{FSR}}{R_M}} \quad (1)$$

where V_{out} is output voltage, V_+ bias voltage, R_{FSR} resistance of FSR, and R_M measuring resistor. The resistance of FSR decreases with increasing force. Applying that in (1), V_{out} increases with R_{FSR} decrease, which can be seen in Figs 9 - 11. This is valid for all four types of the

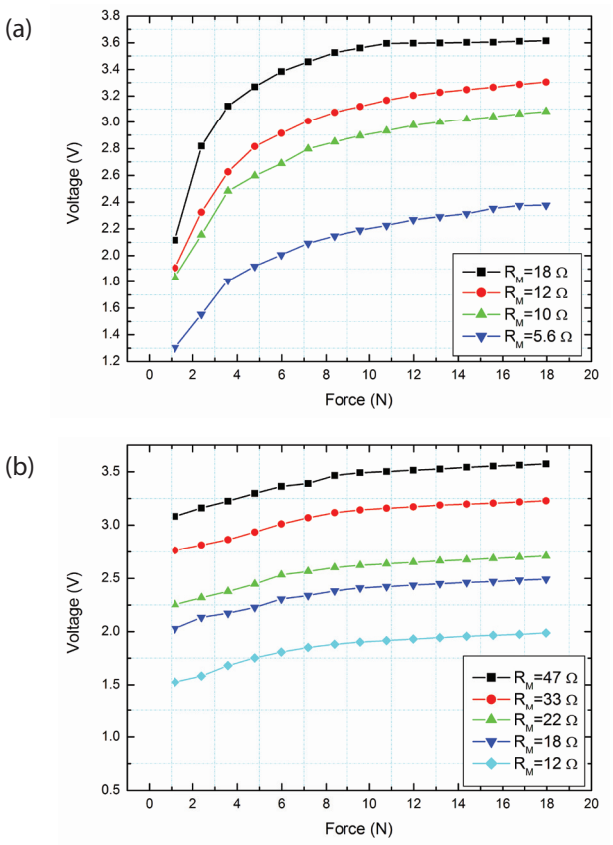


Figure 10: Voltage as a function of force characteristics for: (a) 3rd type of FSR, (b) 4th type of FSR

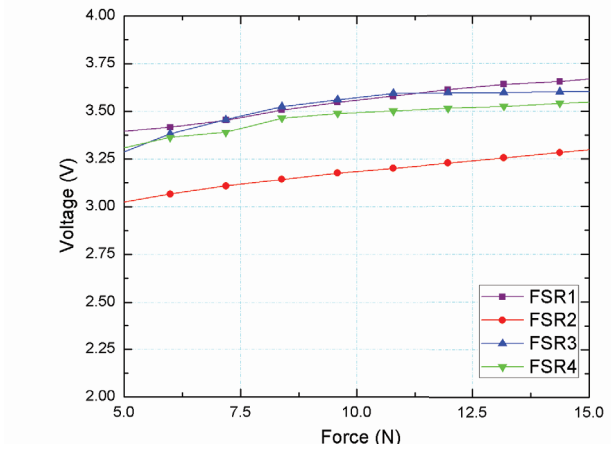


Figure 11: Voltage as a function of force for four types of FSRs and for R_M = 18 Ω in linear sensors' regime

proposed sensors. From Fig. 11, it can be seen that voltage range is from 3 V to 3.5 V, which is very appropriate range for further connection to read-out electronics or displays. Using (1) it can be also calculated which value of R_{FSR} will be obtained for already measured voltage shown in Figs 9 and 10. This will confirm validity of resistance values shown in Fig. 8. R_{FSR} can be calculated from the following equation:

$$R_{FSR} = R_M \left(\frac{V_+}{V_{out}} \right) - R_M \tag{2}$$

where $V_+ = 5$ V.

In Fig. 11 can be seen that applied force was from 5 N to 15 N, since at larger forces changes in voltage are negligible due to small change of R_{FSR}. Fig. 11 shows that the output of the sensor varies linearly with the force applied. The 2nd type of FSR demonstrated the best linearity, in a wide range of applied forces. This FSR has our novel design and can not be found commercially.
FSRs may also find their application in systems with higher temperature than room temperature. Because of that, we analyzed the behaviour of the proposed FSRs at elevated temperature. Fig. 12 shows that resistance of FSRs increases with an increase in temperature. Temperature was changed in the range from 30 °C to 90 °C, while applied force was constant with value of around 12 N (which belongs to a linear range). This increase of resistance can be explained using following equation for R(T) at room temperature:

$$R(T) = R(T_0)\left(1 + \alpha_0 \Delta T\right) \tag{3}$$

where α_0 is temperature coefficient, $R(T_0)$ is resistance at room temperature, and $\Delta T = T - T_0$ is difference between actual and room temperature. As α_0 for silver is 0.0061 °C^{-1} and for carbon -0.0005 °C^{-1}, using (3) it can be seen

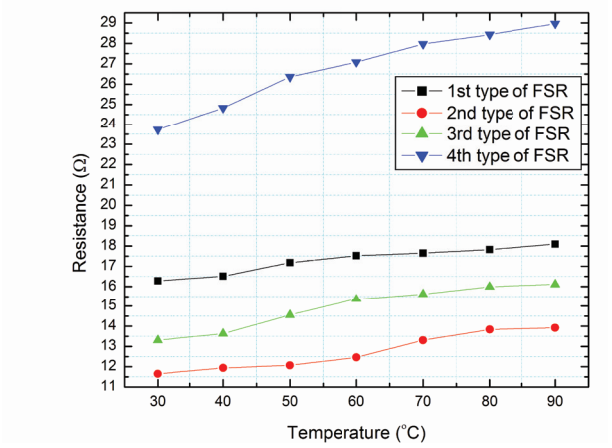


Figure 12: Voltage as a function of force for four types of FSRs and for $R_M = 18\ \Omega$

that with an increase in temperature, value of R(T) also increases. This increase in resistance can be observed for all four types of FSRs (Fig. 12). It can be seen that the smallest variation of resistance with changing temperature demonstrated the first and second types of FSRs which have the lower total active area, comparing with the third and the fourth design of proposed FSRs. In addition to this, α_0 for all four fabricated FSRs has been calculated and results are presented in Table 2.

Table 2: Temperature coefficient α_0 for characterized FSRs

	α_0 (°C^{-1})
1st type of FSR	0.0019
2nd type of FRS	0.0032
3rd type of FSR	0.0035
4th type of FSR	0.0037

The obtained results are directly connected with sensors structure. When pressed or touched, the FSR ink carbon based structures act as a short between the conductive traces from the contact area, resulting in a resistance that depends on the applied force. When the two substrates are pressed together, the microscopic protrusions on the FSR ink surface shorten across the interdigital fingers of the facing surface. At low forces, only the tallest protrusions make contact, while at higher forces, here are more and more contact points between the two substrates. As a consequence, the resistance between the electro conductive lines is inversely proportional to the applied force, as presented in Fig. 8. The voltage is directly proportional with applied force, in accordance with equation (1), and as it is demonstrated in Figs 9-11. Our results revealed that presented cost-effective FSRs are reliable and have a good sensing property for measuring force. The proper design of FSRs, which this paper has proposed (even unconventionally), is very important when dealing with different shape of objects, in order to be able to detect adequately applied force.

4 Conclusion

In this paper four types of flexible FSRs, fabricated in low-cost and easily accessible ink-jet and screen printing technologies, with different design of active area were tested. Each of four FSRs shows that measured resistance of FSR decreases with an increase in applied force, that voltage increases with an increase in force and that resistance increases with an increase in temperature. Measured values of resistance were in the range of 8.81 - 24.81 Ω and voltage was in range from 0.79 V to 3.73 V, while applied force from around

1 N up to maximum of 65 N. Obtained results showed that sensor with largest active area has lowest resistance when applying maximal force, while sensor with smallest active area has largest value of resistance at the same applied force. The novelty of this paper can be summarized as follows: (1) innovative design of second type of FSRs which showed the best linearity and the smallest resistance variation at elevated temperature comparing to other designs which can be usually found off-the-shelf; (2) together with flexibility and thin structure of the sensor this brings a very wide possibilities of sensors applications in many delicate and important fields such as prosthetic medicine, dentistry, rehabilitation, robotics, etc.; (3) comparison of the complete set of performances of four different types of FSRs performed for the first time; (4) presented FSRs can be exposed to a wide range of applied forces up to 65 N; and (5) completely novel in-house developed system for experimental testing of FSRs has been presented.

5 Acknowledgement

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A seven-core fibre for fluorescence spectroscopy

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Abstract: Fibre-optic fluorescent probes need special filtering; this allows them to reject the strong excitation light while transmitting the weak fluorescent light to the detector. In this paper, a seven-core fibre with optically coupled cores is proposed for fluorescent probes. Using core-to-core mode coupling for filtration instead of mounting conventional filters would decrease the number of necessary parts and the size of the probe, making it suitable for spectroscopic applications. The proposed probe was assembled with the central core being used to transmit and couple the excitation radiation to the outer six cores. Using all the cores for delivering the excitation light from the source to the sample reduces the risk of sample being photochemically damaged compared to excitation by a single-core fibre. Fluorescence emission feedback radiation at a higher wavelength can be collected in the outer six cores, and then the fluorescence signal can be coupled from these cores to the central core. The results from the numerical simulations of the 3D full-vectorial model show two cases corresponding to peak transmission at wavelengths of 410 nm and 480 nm. Therefore, the selectivity of the wavelength ensures that the light directed into the central core will pass through it and reach the end of the probe, except for certain wavelengths, where it will couple and appear at the end of the other cores.

Keywords: multi-core fibre (MCF); fluorescent probe; wavelength filtering devices; spectral filtering

Sedem-jedrno vlakno za fluorescenčno spektroskopijo

Izvleček: Fluorescenčne sonde iz optičnega vlakna potrebujejo posebno filtriranje, ki omogoča zavračanje močne vzbujevalne svetlobe medtem ko na detektor prepušča šibko fluorescenčno svetlobo. V tem prispevku je za fluorescenčno sondo predlagano sedem-jedrno vlakno z optično sklopljenimi jedri. Uporaba rodovnega sklapljanja iz jedra na jedro za filtracijo namesto montaže običajnih filtrov zmanjša število potrebnih sestavnih delov in velikost sonde, ki je primerna za uporabo v spektroskopiji. Predlagana sonda je sestavljen iz osrednjega jedra, ki se uporablja za oddajanje in sklapljanje vzbujevalnega sevanja na zunanjih šest jeder. Uporaba vseh jeder v primerjavi z enim samim jedrom vlakna za dostavo vzbujevalne svetlobe od vira do vzorca zmanjša tveganje za fotokemično poškodovanje vzorca. Povratno sevanje fluorescenčne oddaje, na višjih valovnih dolžinah, se lahko zbira v zunanjih šestih jedrih od koder je nato sklopljeno v osrednje jedro. Rezultati numeričnih simulacij s tridimenzionalnim popolnoma vektorskim modelom prikazujejo dva primera, ki ustrezata največji propustnosti pri valovnih dolžinah 415 nm in 480 nm. Pri tem selektivnost valovne dolžine omogoča da bo svetloba usmerjena v osrednje jedro prehajala skozenj in dosegla konec sonde, medtem ko se nekatere valovne dolžine sklopijo in pojavljajo na koncu drugih jeder.

Ključne besede: večjedrno vlakno, fluorescenčna sonda, naprave za filtriranje valovnih dolžin, spektralno filtriranje

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1 Introduction

Optical fibres have been used in many sensing applications [1-2]. Fluorescence-based optical-fibre sensors are of special interest because of their various applications in non-invasive, in-vitro/in-vivo detection systems, drug discovery, the analysis of biomolecules for disease diagnostics, environmental monitoring, three-dimensional, in-situ analyses of living organisms, and the investigation of tissues [3-6].

Fluorescence measurement techniques with free beam optics have many optical components, such as an off-axis parabolic reflector and dichroic beam splitters. This bulky optical arrangement requires a precise optical alignment. Fluorescence-based optical fibre measurement techniques are more convenient compared to fluorescence-based, free-beam optics techniques due to their flexibility, immunity to external electromagnetic interference, cost-effectiveness, compactness, small

size, remote-monitoring capability, long-range operation and their ability to operate in harsh environments. Several configurations of fibre probes for fluorescence spectroscopic systems have been employed. The first configuration consists of a single-fibre probe: the same fibre is used to deliver the excitation radiation to the sample and to collect the emitted radiation.

In the second configuration one fibre is used to transmit the excitation radiation to the sample and a second fibre is used to collect and guide the emission radiation to the detection system. Using separate fibres eliminates the need for fibre splitters, but decreases the chances of capturing the emission photons, as only a small portion of the excited fluorescence can be collected.

In the third configuration fluorescence measurements are made with fibre bundles, where half of the fibres carry the excitation radiation, while the other half return the emission radiation [7, 8]. There are also other designs that include a central excitation fibre surrounded by a number of collection fibres located in one or more rings known as collection rings [9].

In the fourth configuration, probes based on a multicore-coupled structure have been proposed [10]. Multi-core fibres (MCFs) have many advantages over fibre bundles, such as an increased stability, as each core will undergo the same environmental changes, like temperature increases, vibrations and pressure changes. The overall size is also reduced; this is because multiple cores can be designed in a fibre with the same width as a single-core fibre. The core separations throughout the fibre are constant, compared to fibre bundles made by inserting multiple single-core fibres into a capillary, and adding extra functionality to MCFs is easier and more readily repeatable than for a fibre bundle. It also offers new opportunities. The first opportunity is the sinusoidal spectral response due to the coupling between the cores, which allows correlating the property being measured with either the intensity changes or the spectral shifts over the section of the sinusoidal. They have been widely used in a variety of different applications, such as fibre sensors [11], spatial division multiplexing [12], microwave photonics [13], fibre lasers [14], and amplifiers [15].

Our objective is to introduce a new type of optical fibre, with novel capabilities for fluorescence detection, as shown in Fig. 1. One advantage of our proposed MCF probe is the use of core-to-core coupling for filtration instead of external conventional filters. Fluorescence-based, optical-fibre probes with conventional external filters require proper fixations and careful positioning. Another limiting factor that applies to the filters is the outer diameter of such probes. For these reasons, the replacement of the conventional external filters with another, alternative filtering is still of interest [16, 17]. The integration of fibre Bragg gratings into the fibre cores has already been suggested [18, 19]. The challenge is, however, to optimize the filtering characteristics of the MCF filter in order to match the excitation/emission wavelength fingerprint of any selected fluorophore. Therefore, MCF filters with different structures resulting in appropriate optical properties have to be designed and the optical filtering characteristics must be determined to enable the fabrication of the optimal filter for the detection of a selected fluorophore.

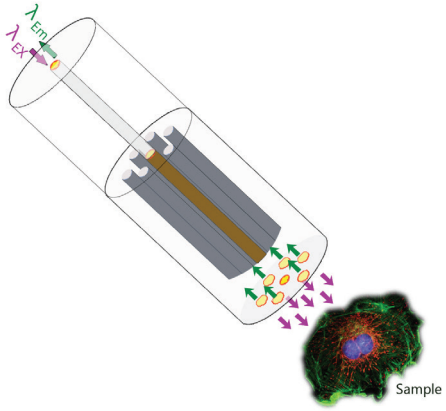

Figure 1: Seven-core fibre for sending the excitation light to the fluorophore and collecting the emitted fluorescence light.

Here, we focus on the design of a seven-core fibre with coupled cores that we intend to use as a probe for fluorescence spectroscopy. The paper is structured as follows. In Section 2 the fundamentals of the seven-core fibre structure are presented on the basis of the Eigen mode expansion theory. Then, in Section 3, the numerical simulations of the complete modal analysis via a 3D full-vectorial model based on the EME method is used to illustrate the modal characteristics of the super modes inside the MCFs. In Section 4 the simulation results obtained by FIMMWAVE and FIMMPROP will be discussed. Finally, the conclusions will be drawn.

2 Fundamentals of seven-core fibres

MCFs can be classified into three categories: multicore, single-mode fibres with coupled cores; multicore, single-mode fibres with uncoupled cores; and multicore few-mode fibres. For all the MCF structures we consider the homogenous, identical, 7-core MCFs consisting of one central core labelled (1) concentrically surrounded by hexagonally distributed six cores labelled (2–7) as shown in Fig. 2. For simplicity of design and fabrication, we assume that each core has an identical radius and refractive index r_{co} and n_{co}, respectively, while the cladding has a refractive index of n_{cl} as in Table 1. The values of refractive indexes correspond to fluorine-doped fi-

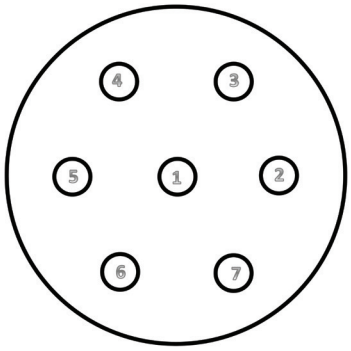

Figure 2: Seven-core coupled structure consisting of 6 cores symmetrically disposed around a central core.

bre [20] at the wavelength 415 nm. It is also assumed that the MCF cross-section is uniform along the *z*-axis.

Table 1: MCF parameters and their values.

Parameter	Value
r_{co}	2 [μm]
Λ	7 [μm]
n_{co}	1.45125
n_{cl}	1.449

3 The 3D full-vectorial Eigen Mode Expansion (EME) method

In this section the EME method is used to model the field propagation in the MCFs. The EME method has been well known in photonics for some time through the film-mode matching (FMM) method [21], [22]. It is based on the idea that any solution of Maxwell's equations in the region of the waveguide can be written in terms of a superposition of the forward (propagating along +z) and backward (propagating along -z) propagating modes [23]. The field in any section can be written as a linear combination of the 2D eigenmodes with the corresponding propagation constants β_k. Such modes can be calculated using Fimmwave's mode solvers:

$$\boldsymbol{\psi}(x,y,z)=\sum_{i=1}^{N}(C_i^f e^{j\beta_i z}+C_i^b e^{-i\beta_i z})\boldsymbol{\psi}_i(x,y) \qquad (1)$$

where $\boldsymbol{\psi}_i=[E_i, H_i]$ is the mode profile, β_k is the corresponding propagation constant and C_i^f, C_i^b are the forward and backward complex amplitude coefficients of the i^{th} mode, respectively.

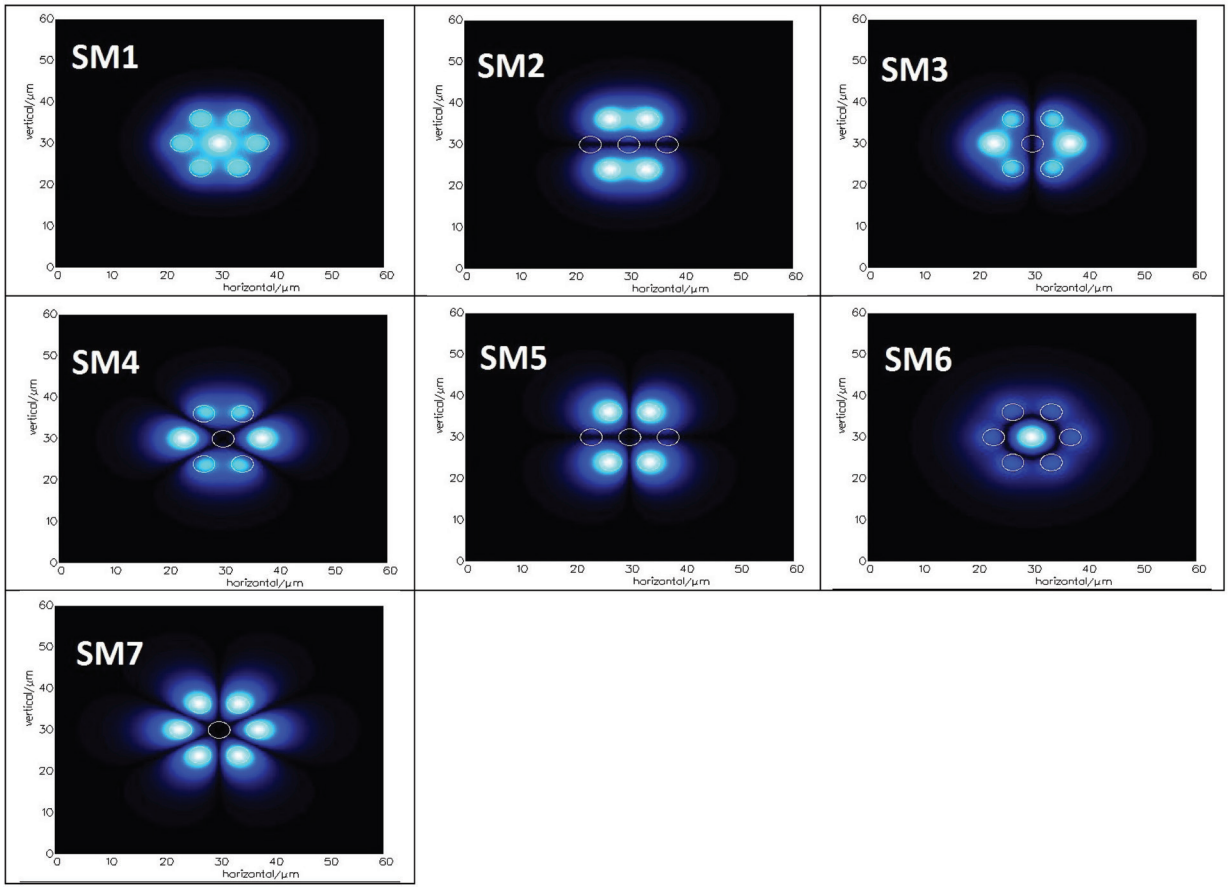

Figure 3: Electric field of the seven super-modes using a finite-element mode solver.

For MCFs with coupled cores, the pitch distance between the cores is reduced in order to increase the core-to-core coupling. As a result, evanescent core coupling occurs and light propagates through all the cores as a super-mode. Each super-mode is a linear superposition of the individual core modes. The total number of non-degenerate super-modes equals the number of cores. The super-mode patterns are calculated using a finite-element mode solver (Fimmwave by Photon Design). The intensity patterns for the seven super-modes of the seven-core fibre design based on table 1 are shown in Fig. 3.

In theory, if the excitation radiation is only launched into the central core, only the super-modes with none zero intensity in the centre core, performing the mode-overlap conditions, can be excited. These modes are SM_1 and SM_6 in Fig. 3.

Currently, analytical expressions have been proposed for the propagation constants and the super-modes inside the MCFs with circularly distributed cores [24-27]. In addition, a semi-analytical model [28] was calculated for the transmission of light in the MCF using the equation

$$T(\lambda) = 1 - P_1 P_6 sin^2\left(2\sqrt{7}\, C(\lambda) L\right) \quad (2)$$

where P_1 and P_6 are the fraction of light carried by the super-modes SM_1 and SM_6, respectively, C is the core-coupling coefficient and L is the MCF segment length.

4 Simulation results and discussion

The methodology was applied to simulate different designs of seven-core fibre by changing the lattice parameters, core diameters and scanning the transmittance in the external cores and the central core of the MCF in a certain range of wavelengths until we reach the optimum design, which matches the excitation/emission wavelength fingerprint of any selected fluorophore.

In order to simulate the propagation dynamics of the seven-core fibre design based on table 1 as a function of the fibre length for a wavelength of 415 nm the light launched into the central core of the MCF, i.e., $A_1(0)=1$. Then the transmitted power in every core is detected by an "offset" single-mode waveguide having a radius similar to that of the cores in the MCF. The result is presented in Fig. 4. This figure shows how the power transfer to the outer cores after the coupling length and then swings back again along the length of the MCF.

To further numerically simulate the transmission characteristics of the proposed seven-core fibre, we define

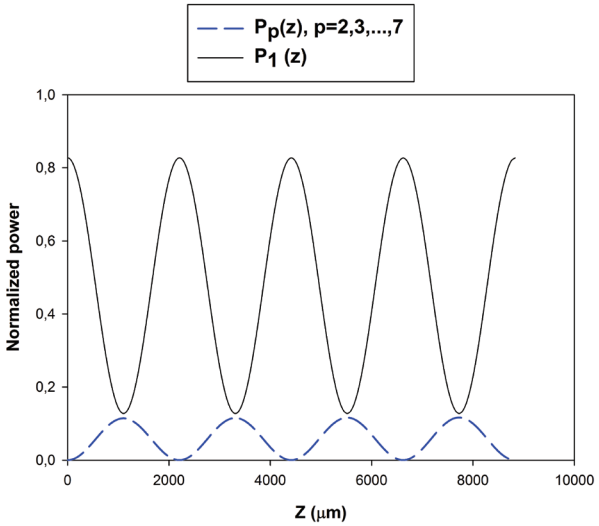

Figure 4: Propagation dynamics of a homogeneous seven-core MCF for the case of light injected into the central core.

the transmission function $T_p(\lambda)$ for the p^{th} core as the ratio of the power output from this core to the power input into the central core at z = 0.

Next, we set the MCF length to an integer multiple of the coupling length and run the simulation to scan the transmittance in all the cores as a function of the wavelength. The results are shown in Fig. 5. The important features in Fig. 5 are the two cases corresponding to the peak transmission at wavelengths of 365 and 410 nm. Therefore, the central core can be used to transmit and couple the excitation radiation of 365 nm to the outer six cores. Using all the cores for delivering the excitation from the light source to the sample in comparison to excitation by a single-core fibre reduces the risk

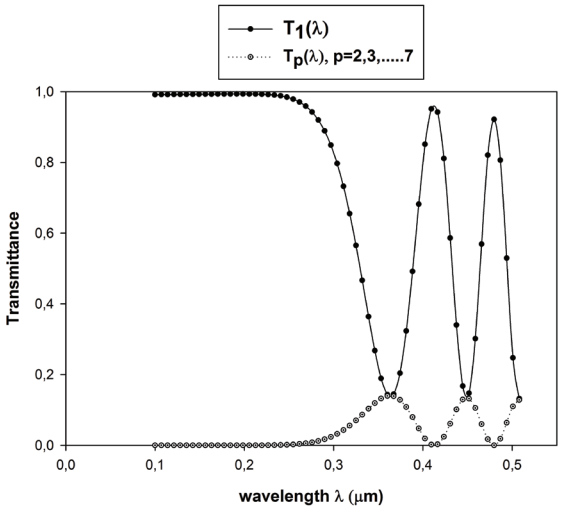

Figure 5: Transmittance of the central core and the outer cores as a function of the wavelength.

of the sample causing photochemical damage due to high light power density. Then the fluorescence emission feedback radiation (415 nm) can be collected in the outer six cores, and the fluorescence signal can be coupled from these cores to the central core.

5 Conclusions

A novel type of fibre probe has been proposed. It can be used for many applications such as efficient fluorescence signal collection and spectral filters. With an appropriate choice of parameters, the probe can be designed to offer a narrowband spectral filter.

Changing the optical or geometrical parameters influences the effective refractive index of the coupled modes and therefore leads to variations in the coupling coefficient and the overall response of the coupled system.

One obvious challenge is to optimize the filtering characteristics of the MCF filter in order to match the excitation/emission wavelength fingerprint of any selected fluorophore. This can be done by changing the geometrical parameters of the MCF probe.

Our future work will be to splice a conventional single-core, step-index, single-mode fibre to the central core of the fabricated MCF and to measure the transmission characteristics of the proposed fibre probe with a broadband light source and an optical spectrum analyser.

6 Acknowledgments

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