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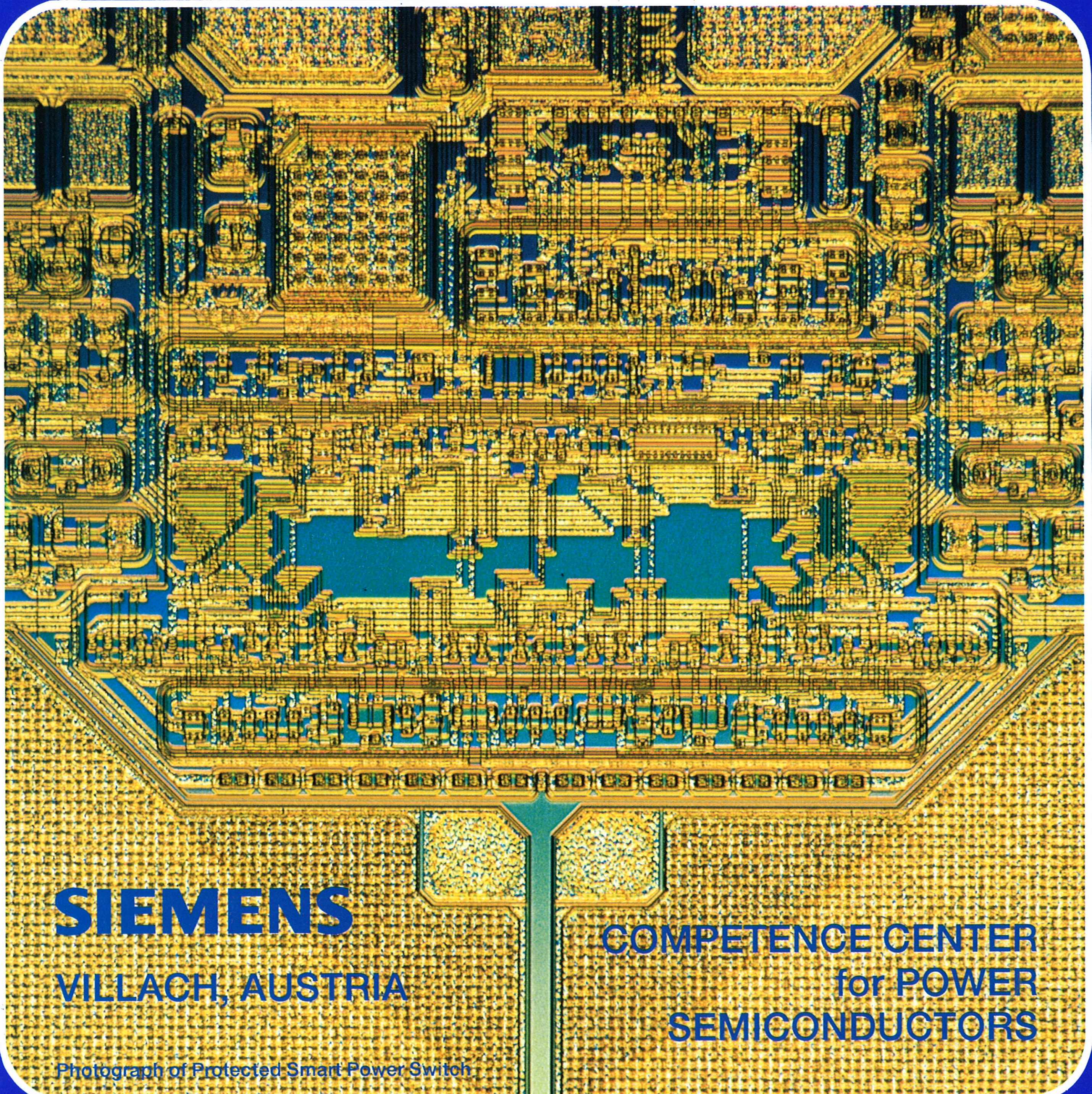

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Slika na naslovnici: Izrez čipa iz PROFET družine vezij

Front page: Cutout of a PROFET power semiconductor with two switching channels

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MIDEM'97 Conference

In September 1996 the MIDEM Society successfully organized MIEL-SD'96, the joint 24th International Conference on Microelectronics, MIEL'96, and 32nd Symposium on Devices and Materials, SD'96, in Nova Gorica. Both conferences attracted a large number of Slovene and foreign experts working in these fields.

There were certain comments given to the organizers that the topics covered by the joint conference are quite diverse. Furthermore, to present about 60 papers in seven sessions in three days also seems to be rather demanding. However, once a year our scientists have the opportunity to present their work at home to the international public and to meet and discuss trends, news and problems related to their fields of work. We believe that this balances the effort required by the attendees and the organizer.

The joint conference was organized for the fifth time. However, after discussions with several foreign and Slovene society members, the MIDEM Executive Board finally decided to accept the proposal of Dr. Rudolf Ročak, former MIDEM Society President, and in future to organize only **one conference** under the name "International Conference on Microelectronics, Devices and Materials" - MIDEM Conference. We would like to show that this is a conference with a long tradition, and therefore we shall use the highest sequence number from the SD symposium series.

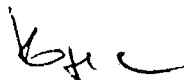
We will strive to preserve the high level of scientific content at the Conference and its friendly atmosphere.

Therefore, you are kindly invited to take part in the forthcoming

33rd International Conference on Microelectronics, Devices and Materials - MIDEM'97

to be held in Gozd Martuljek, Slovenia, September 24 - September 26,1997

MIDEM Society President



Dr. Marija Kosec

Editor-in-Chief "Informacije MIDEM"

M. Sc. Iztok Šorli, dipl.ing.

INNOVATIVE SMART POWER SEMICONDUCTORS FOR AUTOMOTIVE APPLICATIONS

A. Lechner, Siemens Semiconductor Division, Munich

INVITED PAPER
24th International Conference on Microelectronics, MIEL'96
32nd Symposium on Devices and Materials, SD'96
September 25.-September 27., 1996, Nova Gorica, Slovenia

Key words: SPT, Smart Power Technology, Smart Power Semiconductors, automotive electronics, fuel reduction, energy saving, increased safety, increased comfort, automotive industry, smart power devices, smart power switches, smart power IC, drive actuators, power supplies, bus interfaces, TEMPFET transistors, HITFET transistors, MINI-PROFET transistors, PROFET transistors,sensPROFET transistors, senseFET transistors, MULTIFET transistors, motor control, DC motors, motor bridges, high currents.

Abstract: The paper gives an overview of the manifold benefits of smart power semiconductors and over silicon and assembly technologies. Today, these devices are the key for further fuel reductions of cars, for energy saving and for increased safety and comfort. The presentation links technology features, circuit implementations and device characteristics in order to show the interdependence of all required aspects for practible electronics system solutions.

Inovativna pametna močnostna integrirana vezja za uporabo v avtoelektroniki

Ključne besede: SPT tehnologija močnostna inteligentna, polprevodniki močnostni inteligentni, elektronika avtomobilska, zmanjšanje potrošnje goriva, prihranek energije, varnost povečana, udobje povečano, industrija avtomobilska, naprave močnostne inteligentne, stikala močnostna inteligentna, IC vezja integrirana močnostna inteligentna, aktivatorji gonilni, napajalniki močnostni, vmesniki vodil, TEMPFET transistorji, HITFET transistorji, MINI-PROFET transistorji, PROFET transistorji, sens-PROFET transistorji, senseFET transistorji, MULTIFET transistorji, krmiljenje motorjev, motorji enosmerni, mostički motorni, tokovi veliki.

Povzetek: V delu je podan pregled prednosti pametnih močnostnih polprevodniških vezij, kakor tudi ustreznih tehnologij za montažo in njihovo izdelavo na siliciju. Danes so to ključne komponente pri nadaljnem zniževanju porabe goriva pri avtomobilih, pri varčevanju z energijo ter za povečanje varnosti in udobja. Glavne značilnosti tehnologije, izvedbe posameznih vezij in karakteristike komponent so prikazane na tak način, da bralec spozna medsebojno odvisnost vseh teh dejavnikov pri praktični rešitvi in izvedbi elektronskega sistema.

1. INTRODUCTION

The evolution of the car towards an environmental-friendly, easy to use, save and comfortable transport vehicle is continuously bound to progress in automotive electronics. Smart power semiconductors play an ever increasing role to achieve reliable and high performant electronics systems. Today, a wide range of smart power devices, made possible by dedicated smart power technologies, are offered by the semiconductor industry and used by the electronic system producers. Is has become evident, that the symbiosis between electronics and car technology is the key for future success of both industries, in order to achieve such ambitious goals like to build cars that consume less fuel than 3 l / 100 km. Intensive cooperation between semiconductor producers, electronics systems and car manufacturers lead to further optimization of systems, smart power devices, silicon and assembly technologies with regard to system performance and system cost. The implications on smart power electronics coming from the 3 l car challenge conclude the paper.

2. APPLICATION AREAS AND REQUIREMENTS ON SMART POWER DEVICES

Smart Power ICs are highly appreciated in electronics systems for the following purposes:

- drive actuators (lamps, motors, magnetic valves,...)
- power supply
- signal conditioning (accomodation of high voltage signals)
- bus interfacing
- or combinations of these functions.

The key element of smart power devices is its switching element, the power transistor. While the first generation of power transistors in the 60'ies have been built as bipolar transistors, in the 70'ies the development of the DMOS-(Double Diffused MOS)-transistor allowed to break the limits of 2nd breakdown and high drive current imposed on bipolar devices. In the late 80'ies, the advent of smart power technologies made possible to combine the DMOS power transistor with analog and

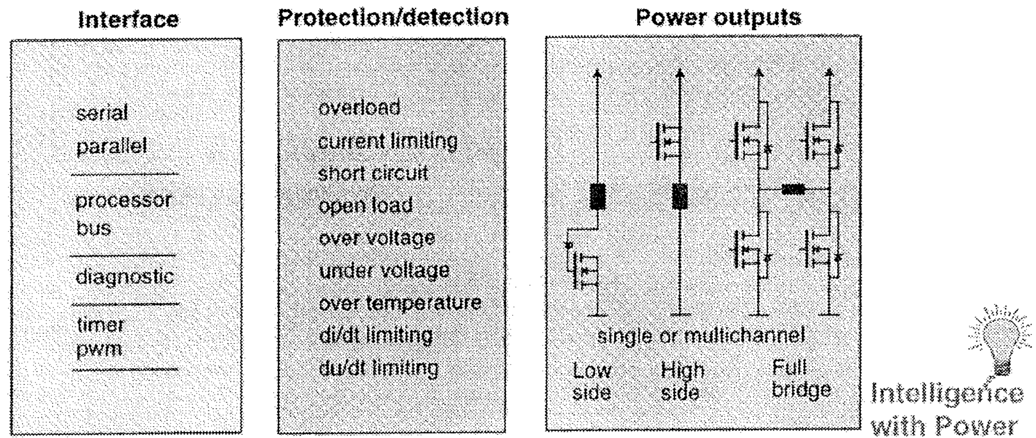


Fig. 1: Smart Power Devices

digital circuitry, thereby realize devices with enhanced functionality so-called "Smart Power Devices (fig.1). In the current decade, the industrialization of smart power applications with the automobile as a technology driver takes place as well as the evolution of smart power towards system-oriented value-adding smart power IC's.

The main technological challenge of smart power is to provide the required voltage capability, reliability and ruggedness of the semiconductor devices to withstand the harsh environmental conditions in cars. Although the nominal battery voltage of cars is 12 V, smart power devices need technologies with about 60 V standoff capability, as can be seen from fig. 2. This is due to instable board nets, some irregular conditions like load-dump, EMI interference and switching of inductive loads.

Also, the temperature requirements of smart power are higher than for most other devices. Generally, an operating range of -40°C.....125°C is specified for smart power devices. However, the devices have to protect themselves and have considerable power dissipation. As a consequence the junction can reach temperatures up to 170°C. Especially for safety-critical applications like ABS, also this is not sufficient. Here the device will give a warning signal at overtemperature, however it has to be guaranteed by design that it maintains its functionality also beyond 200°C.

To maintain functionality under normal and exceeded operating conditions and to operate in a well-defined way under irregular conditions is of utmost importance for smart power devices. This is one of the most challenging design issues of smart power devices. It can be accomplished only by a close cooperation between IC and system designers.

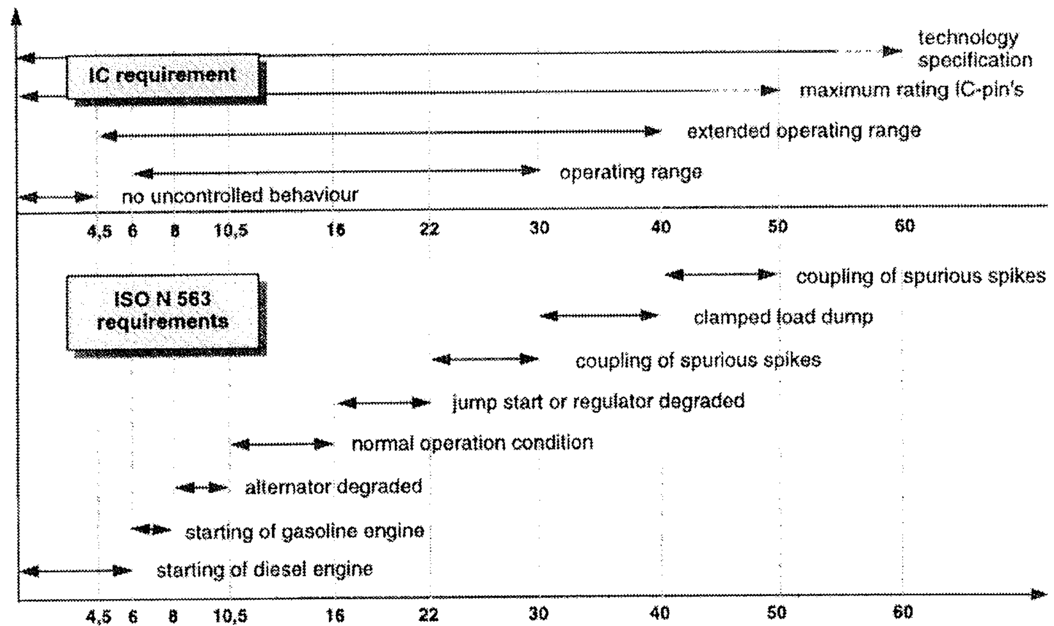


Fig. 2: Voltage standoff requirements

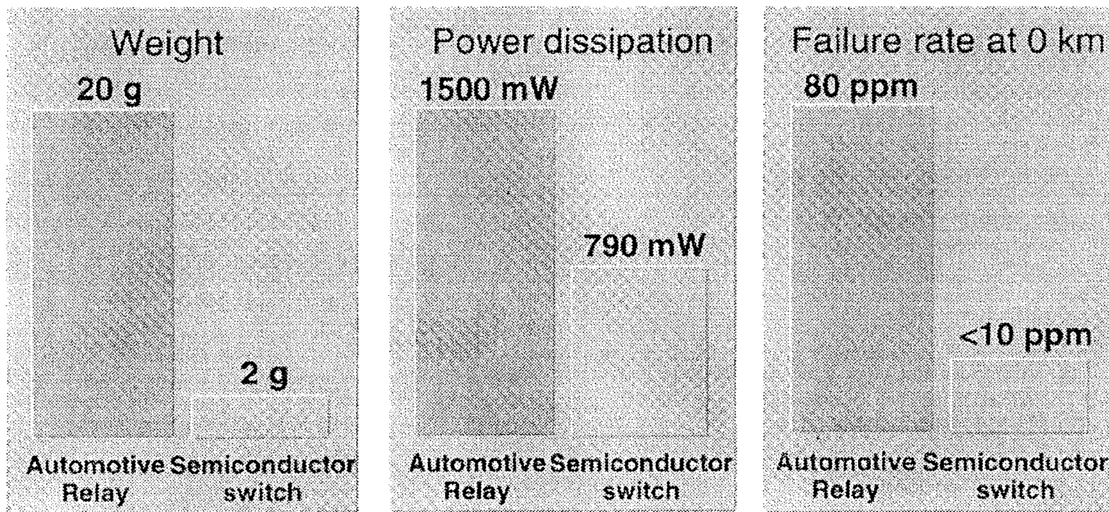


Fig. 3: Benefits of semiconductor switches versus relais

2.1 Smart Power Switches

The most important element in smart power electronics is the "Smart Power Switch". It is needed either in highside or lowside configuration, see fig.I. Since several years, smart power switches continuously are replacing relais and mechanical switches in cars due to their 4 main benefits: reliability, size, weight and power consumption, with the reliability advantage as the most important from an economical point of view. This is illustrated in fig. 3. Of course, the protection and interface functions of smart power devices cause additional costs due to higher die area, needed around the power transistor for this circuitry, and more expensive wafer or assembly technologies. However, higher costs pay off at the system and maintenance level. In addition, smart power semiconductor devices make possible applications that cannot be realized by relais like PWM operation or inductive switching.

Today, several product families of smart power switches are offered by the leading companies that have focused on this innovative field of semiconductor application like Siemens, SGS-Thomson Philips or IR. The smart power switch product families available today comprise solutions for highside and lowside switches and bridges, implementations of different protection levels and digital interfaces as well as adaptions to specific loads and applications. Within each product family, usually several switches with different on-state resistors of the DMOS power transistor (R_{ON}) are offered.

The TEMPFET, HITFET and PROFET smart power switch product families have been well introduced into the market. Fig. 4 gives an overview over these families and their protection and interface concepts.

All these smart power devices are produced with the Smart SIPMOS, S-Smart and the SPT technologies, which are described in chapter 3. As the PROFET concept is already well-known from the literature /3/, the following paragraphs will concentrate on recent developments, which address the following directions:

- Increase system value / decrease overall costs
- Expand the application horizon

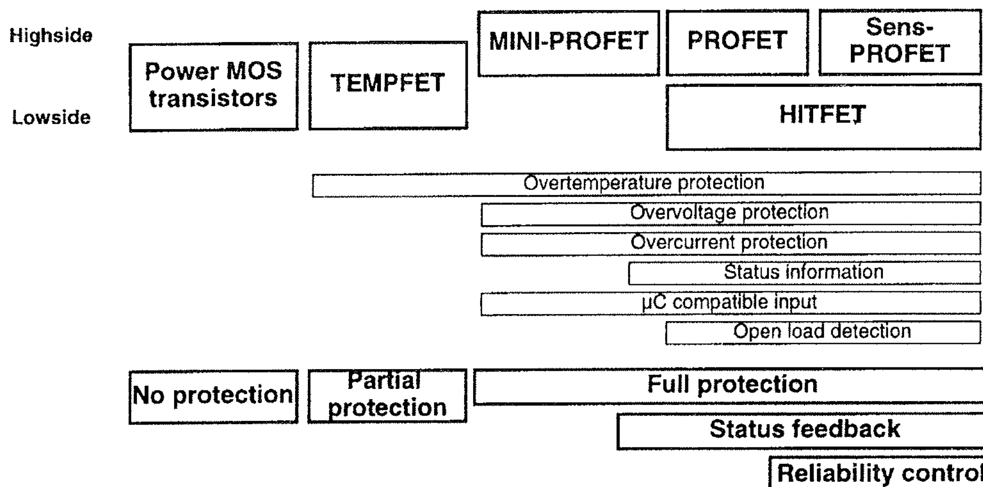


Fig. 4: Smart Power Switch product families

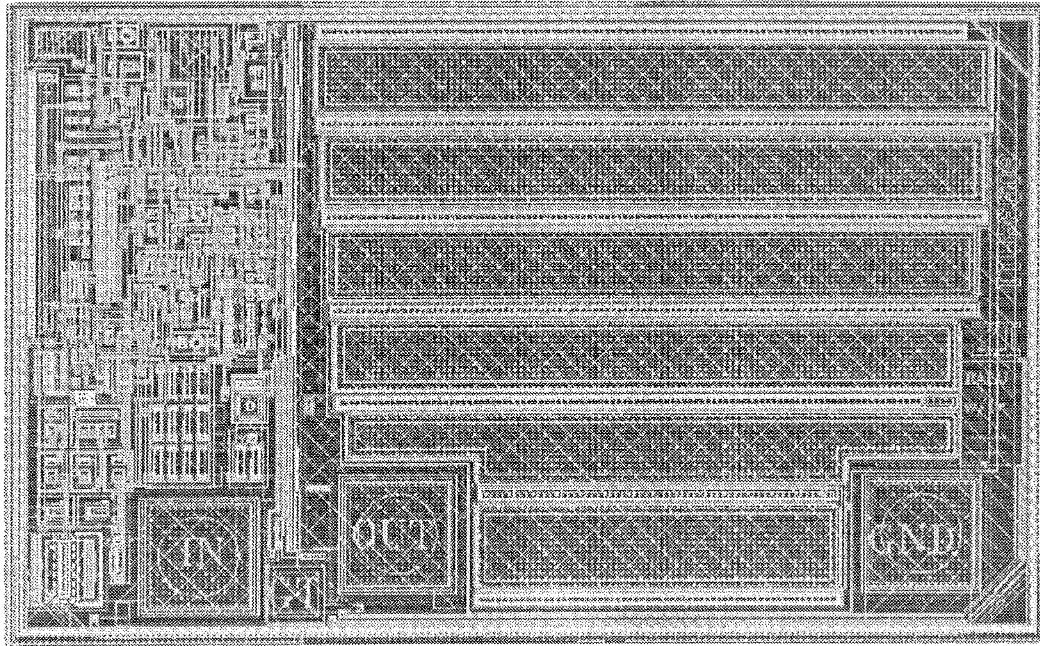


Fig. 5: BSP75 Mini-HITFET chip layout

2.2 MINI-Smart product family:

A large number of applications doesn't require low R_{ON}'s for switching of high currents. What is urgently needed, however, is the ruggedness and voltage capability of the device, i.e. the protection functions, and an attractive price. As a solution to these requirements, the MINI-Smart product family has been developed. These devices combine the high performance of the PROFET or HITFET switches with small die sizes due to small power transistors and the low-cost SMD package SOT223. The product family comprises highside and lowside switches. As an example of recent developments the BSP75 Mini-HITFET is shown in fig. 5. The MINI-Smart devices are ideally suited for driving of relais and small lamps, for climate control or data line driver. There are also manifold applications in industrial control.

2.3 SenseFET product innovation:

As the most recent enhancement of the PROFET family, a so-called "Sense Highside Switch" (SensPROFET) has been developed. This power switch delivers a sense signal proportional to the load current in addition to the normal status line. With this signal processed by a μC with ad-converter, the system has precise control over the load status and all irregular conditions. Fig. 6 shows the system configuration of the current sense feature. Of course, the SensPROFET contains all the protection features already known from the PROFET. With the SensPROFET, also the fuse can be replaced electronically, thus this device saves the relais plus the fuse! As the μC exactly knows the current consumption of the system improved diagnosis as well as more sophisticated concepts for energy saving may be realized.

The first member of the SensFET family is the BTS640S2 /1/, a highside switch with 30mΩ on-resistance, which has been realized with the new S-Smart technology (see chapter 3.2). Fig. 7 shows a layout diagram of the device.

2.4 High current MULTIFET motor bridges:

The bidirectional control of dc-motors requires the combination of high- and lowside switches in a motor bridge configuration. Today, several motor bridge ic's are offered in bipolar and SPT technologies. The MULTIFET is a new and costeffective approach utilizing existing PROFET and Lowside switches. A dual-channel

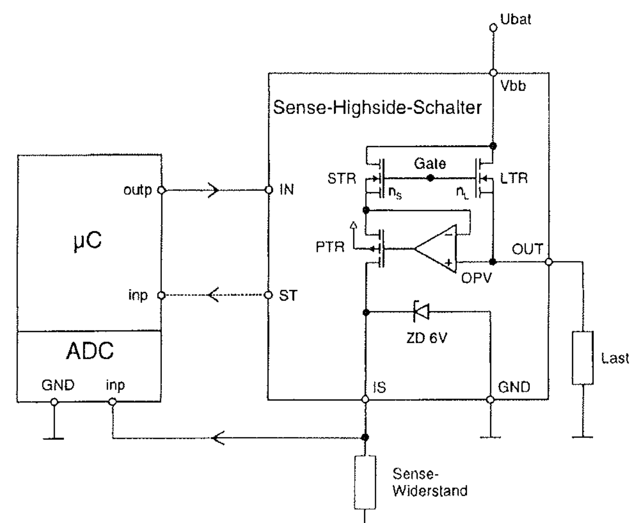


Fig. 6: Circuit Diagram of the Sense Highside Switch

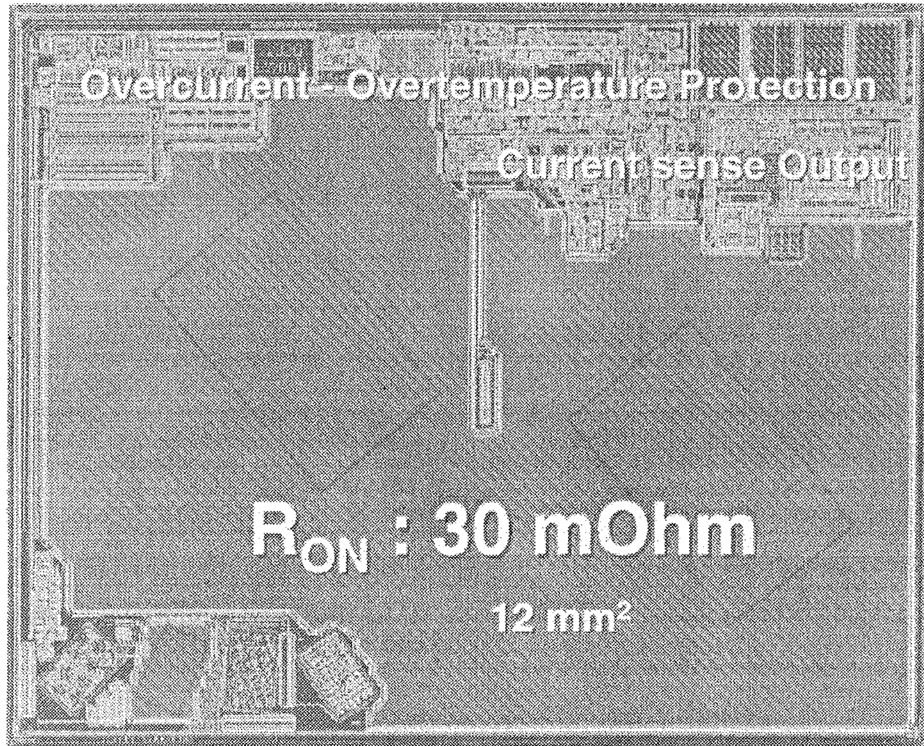


Fig. 7: BTS640S2 Sense PROFET chip layout

Features:

- **Short circuit protection**
- **Charge pump**
- **Current limitation**
- **Thermal shutdown**
- **Diagnostic feedback**
- **Open load detection in on-state**
- **CMOS compatible input**
- **Under- and overvoltage shutdown with auto-restart and hysteresis**

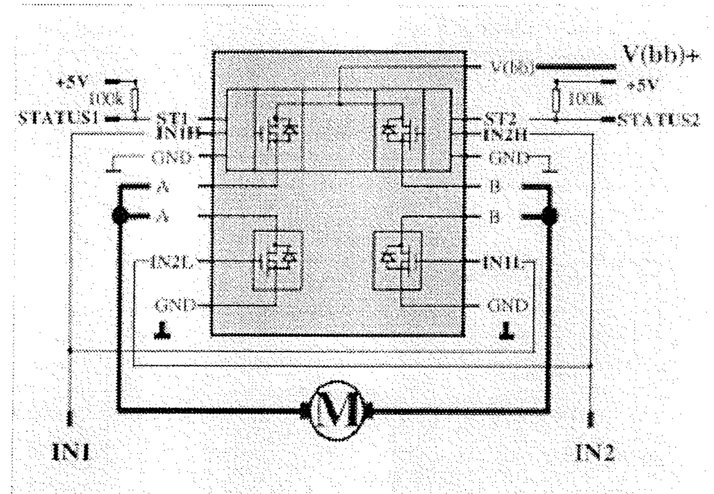


Fig. 8: High Current MULTIFET Motor Bridge

PROFET is combined with two standard power transistors in a DSO-20 plastic package with splitted lead carrier (see fig.8 block diagram). The MULTIFET concept thus allows to use the most cost-effective solutions for the high- and lowside switches seperately and combine them with standard assembly techniques. The leadframe arrangement is shown in fig. 9.

The MULTIFET devices are designed to handle currents as high as 2...4 A. The product familiy can be easily and quickly expanded according to market needs.

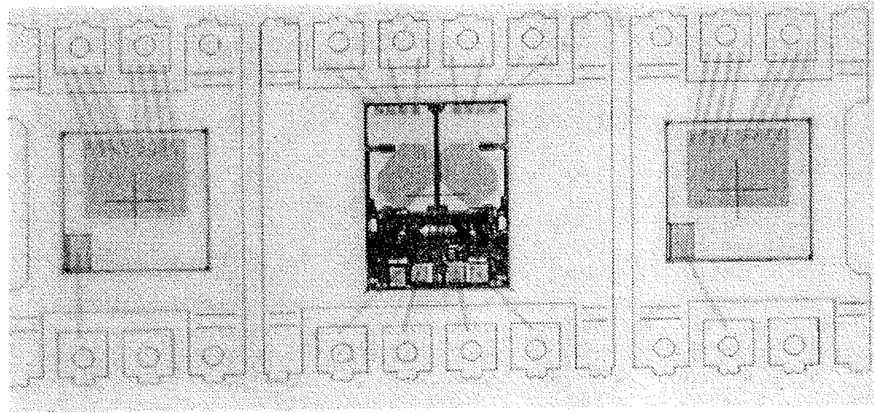


Fig. 9: MULTIFET split leadframe carrier

2.5 Smart Power System Integration

Compact electronics systems like door modules, engine control, airbag or ABS require the integration of all functions on quite a few highly integrated devices. The evolution of most systems can be generally described by fig.10. It turns out that a 2-chip approach is a very cost-effective partitioning, comprising of a standard μC and a system-specific smart power IC containing the power driving, analog processing, system supply and interfacing functions (see fig.11).

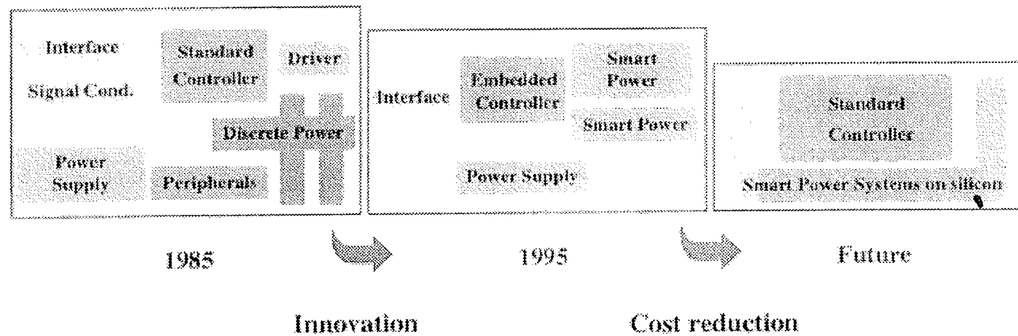


Fig.10: Automotive System Evolution

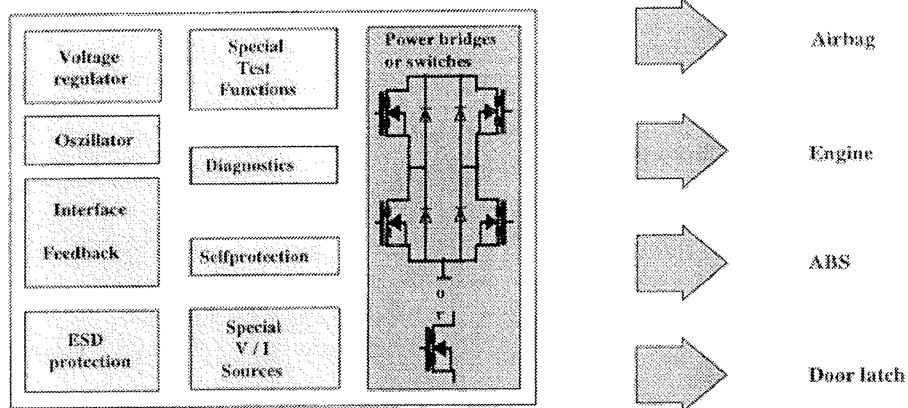


Fig.11: Smart Power Systems on Silicon

3. SMART POWER TECHNOLOGIES

As already mentioned, the application area of "Smart Power" comprise the realization of a big variety of different functions within electronics systems. The common and final measure is the overall system cost. As a consequence, smart power technologies have to be dedicated to the specific system architectures, partitionings and implementations, and have to make possible system solutions providing an overall benefit. Of course, progress in silicon technologies is a pacemaker. However, also assembly techniques, mounting and cooling concepts play a very important role especially in the field of smart power. These issues will be viewed now.

The workhorse of today's smart power technologies are silicon technologies with the DMOS transistor for power switching and CMOS and bipolar for logic and analog functions. Technologies with self-isolation and junction-isolation are in massproduction, technologies with dielectric-isolation in the experimental phase.

3.1 SPT, a versatile junction-isolated smart power technology

The SPT is a bicmos power technology with an optimized dmos transistor. The technology is optimally suited for complex smart power ics with multichannel power switches, analog processing and logic interfaces. Fig. 12 shows the crossection of some major devices and the junction isolation concept. The junction isolation is performed by a seperate bottom and top p+-implant. Thickness and doping level of the epitaxial layer is optimized to provide the required drift region for the dmos. The dmos current flow is lateral, i.e. it is fed to the surface via the buried layer and an n^+-sinker, which allows multiple transistors at arbitrary voltage levels. A large variety of devices can be constructed with the SPT by utilizing the available implants skillfully. The cmos and bipolar devices are provided in different versions, in order to optimize packing density, standoff voltage or analog behaviour, as needed for the specific circuit function. For high voltage circuits, beside the dmos, a high voltage pmos can also be realized by inclusion of a tapered lateral drift region.

The SPT uses an advanced fully self-aligned dmos cell (fig. 13). Not only body and source implants are defined by the same mask, also the source contact is applied to the same structure, after a deep etch controlled by spacers. This selfaligned dmos cell yields a very high cell density, resulting in low on-resistance (R_{ON}) of the dmos power transistor.

The SPT technology is improved continuously in order to increase the packing density of cmos, bipolar circuits and dmos cells.

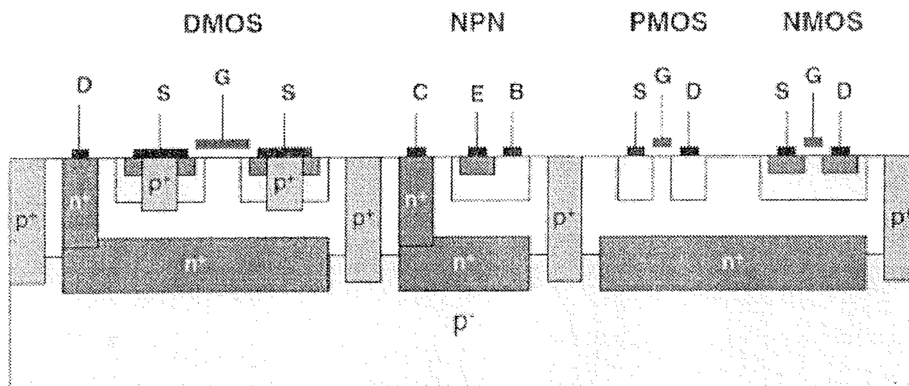


Fig.12: Cross-section of SPT Technology

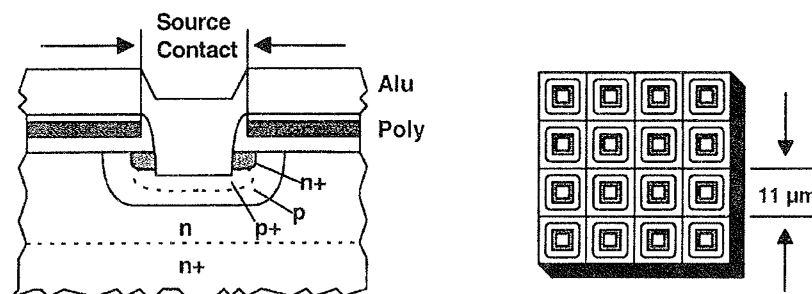


Fig.13: DMOS Transistor of SPT

3.2 Smart SIPMOS, the highside switch technology

As mentioned earlier, the protected switch is the most important device of smart power. For ist realization, only processing steps absolutely necessary for protection circuitry should be added to a power transistor process. This is the idea of the Smart SIPMOS process, a self-isolated technological approach to smart power. A simplified crosssection is shown in fig. 14. Chargepump, overtemperature and overvoltage protection as well as status feedback can be realized with low- and high-voltage cmos transistors. Smart SIPMOS, with several technological improvements, has made possible 5 generations of PROFET devices up to now. Furthermore, designers have learned to realize cost-effective HITFET lowside devices with this technology too.

In recent development, the conventional Smart SIPMOS has been improved and combined with the self-aligned SPT dmos cell. The new technology is called S-Smart and it provides an increase in packing density of up to 40%. It is first applied to the current sense PROFET.

3.3 Packaging and assembly technologies

Today, the TO-220 is the package with highest production quantities used for smart power electronics. With its 5-pin and 7-pin configurations, 1- and 2-channel smart power switches and motor bridges can be assembled in a cheap standard plastic package with excellent thermal properties. The TO-220 can also be delivered in a SMD compatible lead configuration. However, the trend towards higher integration, reduced volume and fully automated pcb handling gives a strong driving force for advanced SMD-type packages with small outlays (like SOT, DSO and MQFP) and pincounts ranging from at least 3 for mini power devices over 20...28 for medium integrated power devices to 64 and more for complex smart power system ics (see fig.15).

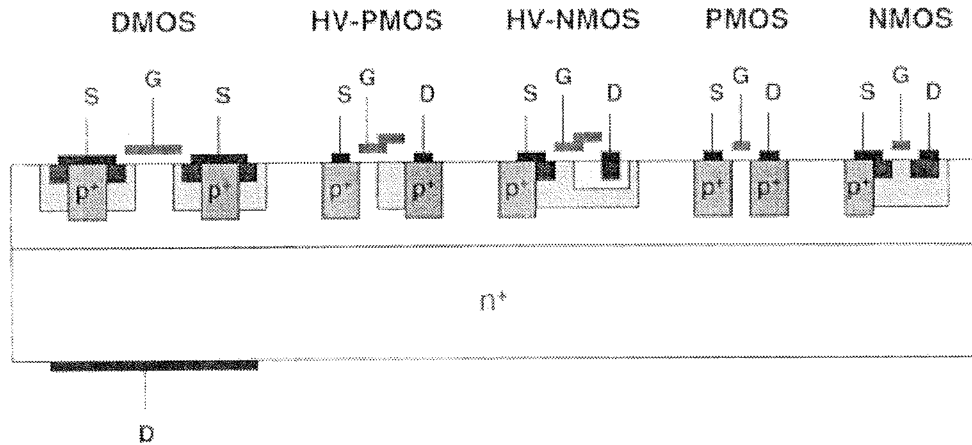


Fig.14: Smart SIPMOS Technology

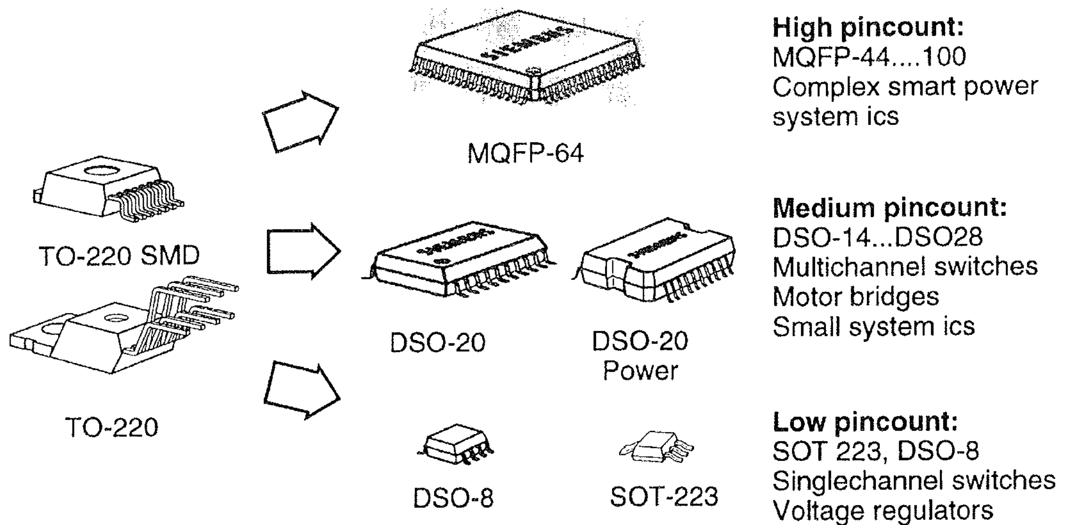


Fig.15: Smart power package trends

In order to provide low-cost solutions, it is very important to use high-volume production lines with no or only small modifications for smart power devices. Modifications are required e.g. for enhancing thermal properties (special leadframes, additional Cu-blocks), for electrical isolation purposes (leadframes with multiple carriers). Additionally, the system aspects also for packaging has to be taken into account. As an example the "silicon vs. heatsink" concept shows, that heatsinks can be avoided by switches with low R_{ON}. Although these semiconductor devices are more expensive, the overall system cost is lower, and weight and volume benefits are provided.

The product examples mentioned earlier show the importance of these innovative assembly concepts. With further minituarization its importance will even increase. Hybrid assembly, multichip modules and the integration of micromachined sensor elements are current trends, that make mechatronics concepts a big challenge of the next years.

4. THE 3 l CAR CHALLENGE

The automotive industry today faces the challenge to drastically reduce the toxic exhaust and the fuel consumption of cars within the next 10 years. As a common wording, the 3l-car is the goal of this effort. With this target in mind, engineers worked out the dependencies of fuel consumption and found that 50 kg additional weight as well as 100 W additional electric power yield an additional fuel consumption of about 0,15 l /4/. The consumption of electric power of an average car is about 500 W, with a rising tendency for the next years. This means that today about 0,75 l / 100 km fuel is needed for the electrical power generation. For high-end cars this value has to be doubled, and for the future the situation would get worse.

As a consequence, energy and weight saving is essential to achieve a 3 l-car. Future cars therefore will require an efficient power management system with all loads controlled by semiconductor switches. Mechanical solutions like the fuel pump as an example, will be replaced by an electronically controlled pump, adapting the power to the actually required amount. Advanced control systems like PWM operation and switched-mode DC-DC conversion, which reduce electric losses, will dominate over conventional systems.

Furthermore, it is becoming clear that the current 12 V board net also is a severe limit. Leading european car manufacturers have founded the initiative "Bordnetz 2005", to define a next generation architecture for the car board net. Results are not yet available, however it is obvious, that the supply voltage will increase, may be towards 40 V. A higher supply voltage, together with new electric and electronic components, especially designed for high yield and less weight, are required to face the challenge. What consequences will this have on power semiconductor devices?

As can be seen from fig. 2, the breakdown voltage requirements of power semiconductors today are defined by supply voltage irregularites rather than by the battery voltage. A higher battery voltage therefore doesn't necessarily imply a higher standoff voltage for the technology. The standoff voltage of the semiconductor devices will depend on the stability of the new boardnet that can be achieved. A higher battery voltage will help to increase the stability of the net, as the current levels will decrease accordingly. Lower current levels will as a further benefit reduce ohmic losses in the wiring cables.

5. CONCLUSION

The application of smart power devices in cars is increasing, as a high level of maturity of the electronic systems could be achieved with respect to system functionality, reliability and cost. The available smart power device palette, ranging from switches for high- and lowside configurations up to smart power system ics is refined and enlarged continuously by close cooperations between semiconductor and system manufacturers. The improvement of dedicated smart power silicon technologies and assembly technologies both is of equal importance to achieve the growing perfomance and price requirements.

However, this development by far has not come to an end now. As has been shown, the challenge to achieve more environmental-friendly cars will bring about a new push to rework the car board net architecture with respect to weight and power savings.

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LOW PRESSURE PLASMA PROCESSING IN MICROELECTRONICS

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Key words: electronics, microelectronics, plasma processing, low pressure plasma, low pressures, surface treating, surface etching, surface coatings, IC, integrated circuits, plasma drilling, PCB, printed circuits boards, wafer fabrication, decoating.

Abstract: Low pressure plasmas are widely used for treating, etching and coating surfaces of different materials. This technique is indispensable for manufacturing of very large scale integrated circuits used by the microelectronics and electronics industry. In this paper new applications of low pressure plasma processing are presented:

Dry cleaning of wafer boats coated by LPCVD - Si and Si_3N_4 through plasma etching leads to a dramatic reduction of boat replacement. Ashing of photoresist in IC fabrication using modern microwave batch systems is much more economical than the classic single-wafer process. Cleaning of substrates on which ICs are mounted increases strongly the pull strength of wire bonds and improves the adhesion of mouldings used for IC encapsulation. Plasma drilling of microvias into thin flexible PCBs pushes the dimensions of PCB structures beyond the limits set by the conventional, mechanical drill process.

Uporaba nizkotlačnih plazemskih procesov v mikroelektroniki

Ključne besede: elektronika, mikroelektronika, procesiranje plazemsko, plazma nizkotlačna, pritiski nizki, obdelava površinska, jedkanje površinsko, prevleke površinske, IC vezja integrirana, vrtanje plazemsko, PCB plošče vezja tiskanega, proizvodnja rezin, odstranjevanje prevlek.

Povzetek: Procese, ki potekajo v nizkotlačni plazmi množično uporabljamo za obdelavo, jedkanje in prekrivanje površin različnih materialov. Ta tehnika je nepogrešljiva pri proizvodnji integriranih vezij zelo visoke stopnje integracije, ki jih danes uporabljata mikroelektronska in elektronska industrija. V tem prispevku pa predstavljamo nekatere nove možnosti uporabe procesov v nizkotlačni plazmi.

Suho plazemsko čiščenje ladjic za rezine, ki so prekrite z debelim nanosom LPCVD silicijevega nitrida, omogoča dramatično znižanje števila zamenjav ladjic zaradi poškodb. Odstranjevanje fotorezista v mikrovalovnem šaržnem reaktorju pri proizvodnji integriranih vezij je bolj ekonomično kot klasično čiščenje rezine po rezino. Čiščenje substratov, na katere so pritrjena integrirana vezja v čip obliki v veliki meri poveča trdnost in zanesljivost žičnih povezav med čipom in substratom - ohišjem ter poveča adhezijo materialov, ki jih uporabljamo za zalivanje, oz. zapiranje integriranih vezij. Plazemsko vrtanje mikrolukenj v tanke upogljive PCB substrate omogoča zmanjševanje njihovih dimenzij daleč izpod meja, ki jih narekuje konvencionalno mehansko vrtanje lukenj.

1. Introduction

Low pressure plasmas are known and investigated since the mid of 20s. Many promising features have been found since that time and the new technology entered industrial manufacturing nearly 30 years ago. The large variety of surface modifications which can be obtained by low pressure plasmas as well as environmental and economical aspects are reasons for the further growing interest in this technique.

Excellent results obtained and low running cost due to low consumption of energy and process materials are the most attractive features of plasma processing. The plasma process utilizes inexpensive and easy-to-handle gases only. Workpieces are absolutely dry after treatment and high cost for an additional energy-intensive drying process can be saved. Cost for the disposal of waste and the recycling of wet chemicals can be saved as well. The plasma process requires no special safety measures and provides a cleaner and safer workplace. An important characteristic of low pressure plasma is its penetrating power. The gas penetrates into small pores and structures that are difficult or impossible for liquids to access. Thus, micro-structures can be formed and parts with complex shapes can be processed easily. Due to the manifold of technological, environmental and economical advantages low pressure plasma can be said a powerful tool for future applications in microelectronics and electronics industry.

In this paper newly developed plasma processes are presented that are applied in wafer fabrication, assembling technology and PCB manufacturing.

2. Plasma in Microelectronics

Low pressure plasma processing is well-established in the microelectronics industry, the production of integrated circuits of today´s standard wouldn´t be possible without using plasma. In addition, lab scale plasma equipment is used for IC decapsulation in the case of failure. Recently, dry plasma removal of CVD-layers from long quartz boats has been invented and ashing of photoresists using modern microwave batch systems has been developed to a highly economical process in IC fabrication.

2.1 Decoating of Wafer Boats

Quartz boats used as substrate carrier in IC fabrication are coated several times with CVD - Si and Si_3N_4 during wafer processing and have to be cleaned periodically. Dry plasma decoating recently developed is a new alternative to cleaning of the quartz boats using wet chemicals. The dry plasma process has an improved etch selectivity between quartz and CVD layers reducing the attack on quartz. Therefore, plasma decoating results in an extreme increase in boat life time and leads to a dramatic cost reduction on quartz ware. Cost for the consumption and disposal of wet chemicals are saved as well. These facts are the key arguments for dry plasma decoating. High throughput - two boats can be cleaned in approx. 1 hour cycle time - and cleanroom compatibility of plasma equipment are additional properties which make plasma processing continued attractive for the use in IC fabrication.

Fig. 1 shows the plasma equipment with the process chamber opened. The system is capable to hold two 80 cm long quartz boats. A plasma power of 2.4 kW totally is supplied by four microwave generators working at a frequency of 2.45 GHz.

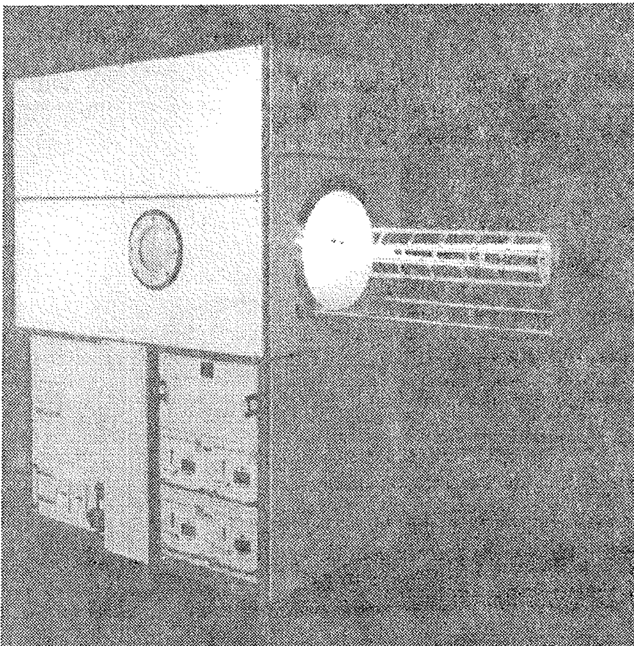

Fig. 1: Plasma equipment for dry removal of CVD layers on long quartz boats.

2.2 Smart Ashing of Photoresist

Photo resist stripping is a regular process during wafer fabrication. The strip process is carried out up to 20 times for the production of a CMOS wafer. Current etch technique is the single-wafer process using RF plasma in competition to wet chemical processes. Through recent developments the single-wafer process is replaced by a batch process in a low pressure plasma applying modern microwave technology. The main difference between the two processes is the time of plasma treatment resulting in a lot of advantages on the side of the newly developed batch process. The most important is the improved yield for batch processing (Tab. 1). Whereas low throughput of 15 - 50 wafers/h is obtained in the case of single-wafer ashing, high throughput of 60 - 120 wafers/h is achieved for microwave batch ashing. Up to 50 wafers can be processed simultaneously in the latter case. Moreover, the plasma batch system developed has 200 mm wafer capability with unmatched productivity and provides low particle and metal contamination owing to special loading mechanism and quartz materials used. Minimum footprint required in cleanroom area and high process yield results in very low cost-of-ownership for the plasma batch system. Fig. 2 shows the plasma processor 300 Autoload whoose specifications are listed in Tab. 2.

Table 1: Capacity of single-wafer process and batch process

	Single-wafer asher	Batch asher
Process time	1 - 3 min.	20 -50 min.
Loading / unloading	0.5 - 2 min. (per wafer)	5 min. (per batch)
Throughput	15 - 50 wafer/h	60-120 wafer/h

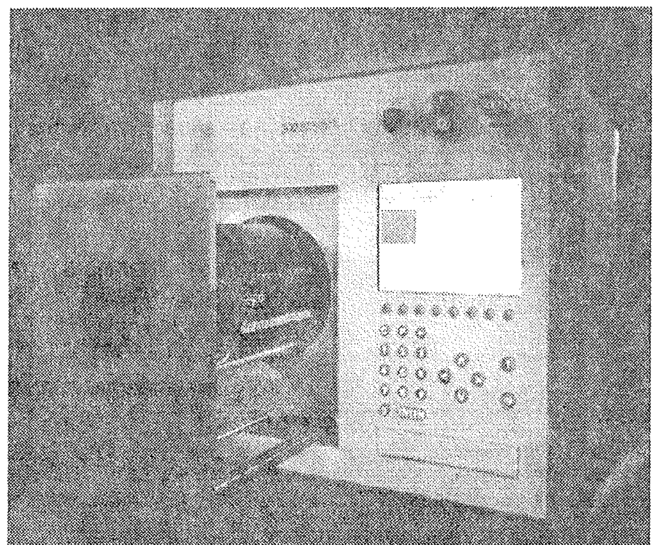

Fig. 2: Plasma system 300 Autoload PC - superior microwave plasma batch system for ashing of photoresist.

Table 2: Plasma system 300 Autoload PC - Specifications

Performance Data	
Maximum batch size	50 wafers per load
Wafer size	all sizes up to 200 mm
Typical cycle time	20-25 min. per batch
Productivity	approx.100 wafers per hour
Uptime	>95%
MTBF	> 500 h
MTTR	<2h
Particle count	< 10 particles (0.12 μ^2 on 6" wafer)
Technical Data	
Quartz process chamber (easy to clean)	ϕ = 245 mm (9.6"), depth 380 mm (15")
Wafer loading	Automated loading mechanism
Microwave plasma generation	Frequency : 2.45 GHz, Power : 0 -1000 Watts
Vacuum gauge	Capacitance manometer, MKS Baratron
Process gas control (up to 4 channels)	Mass Flow Controller, 2 channels standard (2 optional)
Minimum footprint	W/H/D : 705 / 605 / 700 mm 273/4" / 23.8"/ 27 1/2"
Weight	140 kg
System Operation	
System control	Dialog PC 386/33 (optional 486/66), Floppy disk drive, 10" TFT color monitor, RS 232 interface, Optical End Point Detector, IR thermometer
Software package	Manual and automatic operation, graphical display, multiple recipe storage, system check
Option	Automatic cassette loading handler for 150 and 200 mm wafers

In the case of the new batch process there are additional technical benefits in comparison to the single-wafer process. The extended time of plasma treatment effects higher desorption of chemical residues (corrosion inhibition), enables curing of Spin-on-Glass still during the plasma process and provides safe overash as well as backside or double side ash.

The most important benefit of the new system, however, is the use of microwaves of 2.45 GHz for large volume plasma generation. In comparison to RF frequency higher electron density is produced coupled with higher concentration of radicals that are the reactive species in the plasma. Microwave frequency creates not only high plasma density, but also very low self-bias potential on the substrate surface. In Fig. 3 the self-bias voltage is depicted versus the frequency used for plasma exitation. For microwaves of 2.45 GHz the self-bias potential

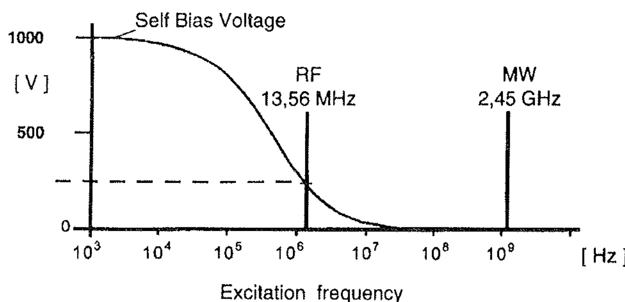

Fig. 3: Self bias potential as a function of the excitation frequency used. Low self bias voltage for microwave frequency.

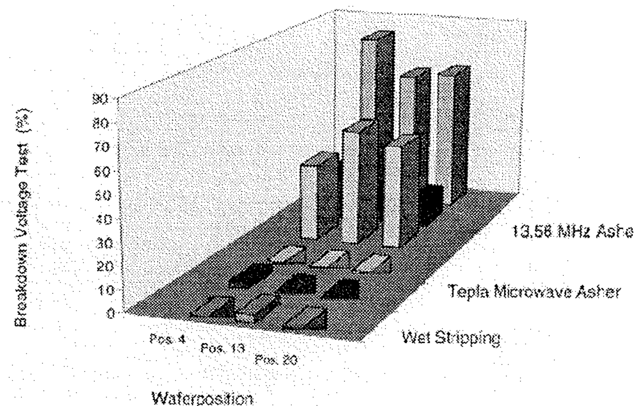

Fig. 4: Gateoxid integrity after resist stripping. Comparison of different etch processes.

is between 5 and 15 Volts typically. Thus, microwave plasmas are damage-free and electronic devices are not destroyed during exposure to plasma. This behaviour has an enormous effect on the gateoxid degradation during photoresist stripping. Up to now extremely low damage level is reported by wafer fabs having long term experience with the new plasma equipment. Gateoxid degradation is investigated by means of break down tests with high voltages applied. Fig. 4 shows the breakdown failure in arbitrary units as a function of different wafer positions in the carrier. Wet chemical etching, plasma ashing in a 13.56 MHz barrel asher and microwave batch ashing are compared. The microwave plasma batch process is superior by far over the competitive plasma process using RF frequency, and it reveals results equal to the wet process. With respect to economical and ecological aspects microwave batch ashing is superior to the wet process as well.

3. Plasma in PCB Technology

For about 15 years low pressure plasmas are successfully used in PCB manufacturing for drill hole desmear and etch back of multilayer printed circuit boards. Plasma desmearing replaces here the wet etching process using highly aggressive chemicals such as $KMnO_4$. During the last years PCB technology developed rapidly. The dimensions of PCB structures became smaller and smaller, the wire density and the number of layers grew up. Mechanical drilling for formation of interconnections between electric circuit layers is a limiting factor which can be overcome by plasma drilled holes. The new and revolutionary DYCOstrate® technology which has been invented by DYCONEX AG is using a plasma process developed by Technics Plasma GmbH. The continuous miniaturization of PCB structures also results in new assembling techniques for the electronic devices, e.g. the Chip-on-Board technique. Therefore, cleaning of substrates on which ICs are mounted is also presented in this chapter.

3.1 DYCOstrate® - Plasma Drilling

DYCOstrate® technology. The concept of the DYCOstrate® technology which is illustrated in Fig. 5 is simply said the substitution of the mechanical drilling process in glass-reinforced base materials by plasma drilling in thin plasma-etchable dielectrics. The scope of products which can be manufactured using the new DYCOstrate® technology ranges from flexible PWBs to flex-rigid PWBs, rigid PWBs as well as MCM substrates. DYCOstrate® products can be ideally used as substrates for the new direct-assembling techniques such as COB, TAB, (μ)BGA and others.

DYCOstrate® - C technology. The majority of today´s applications are simple rigid boards. Therefore, the so-called DYCOstrate® - C (commercial) technology is developed, in which an FR-4 buttered Cu-foil is laminated onto one or both sides of a standard FR-4 core. Besides plasma-drilled blind vias ordinary mechanically drilled through holes are also applied. DYCOstrate® - C enables the low-cost manufacture of PWBs which are densely wired.

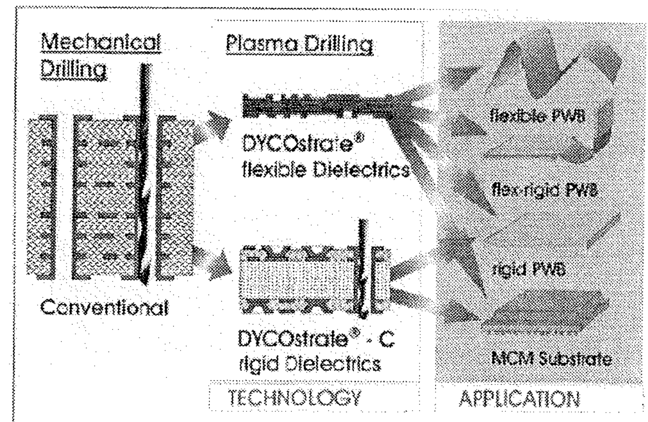

Fig. 5: Basic concept of DYCOstrate® technology.

Plasma formation of through holes. Plasma drilling enables the production of PCB´s without rejecting conventional PCB processing. Usual photo resist technique is applied to produce the Cu mask prior to plasma etching of the organic base material of the DYCOstrate® foil. Base materials typically used are polyimide and FR-X materials. The isotropic etch effect leads to an inherent undercut which is nearly levelled after Cu plating and Ni/Au deposition. „Drill hole" diameters of 75μm and less are recently produced (Fig. 6).

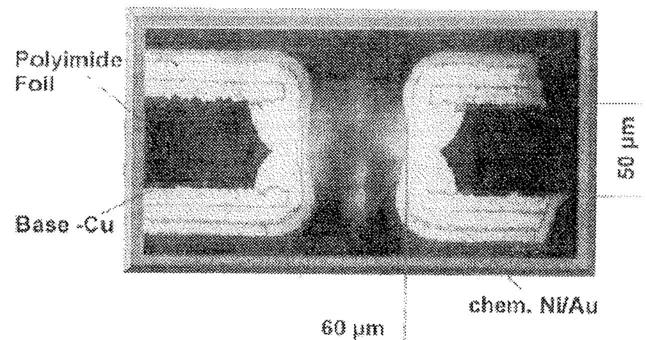

Fig. 6: Cross section through a plasma etched through via after Cu plating and Ni/Au deposition.

Plasma formation of blind holes. The former Dip-In-Hole assembling technique has been widely replaced by the current Surface Mount Technology. Coupled with this development the production of blind vias has become more and more important for the connection of two related layers. An outstanding feature of DYCOstrate®- plasma drilling is: The production of blind vias is technically easy (Fig. 7). Multilayer build-ups (Fig. 8), for instance, can be completely new designed by applying the DYCOstrate® process.

Both, minimum-sized hole diameter and the technically easy production of blind vias makes plasma etching a promising tool for future PCB manufacturing.

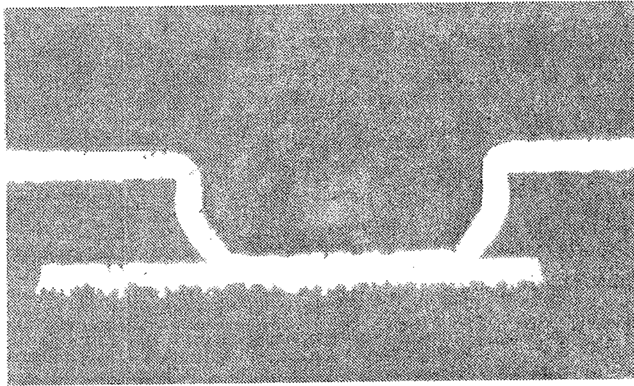

Fig. 7: Cross section through a plasma etched blind via after hole forming and Cu plating.

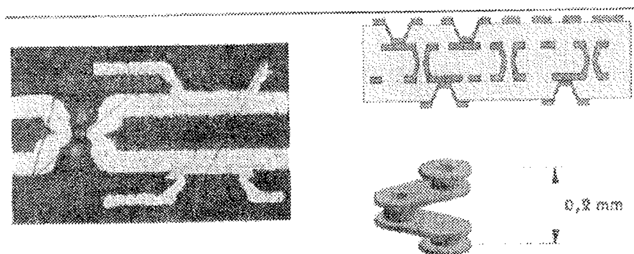

Fig. 8: Micro cross section of DYCOstrate® 4D interconnect.

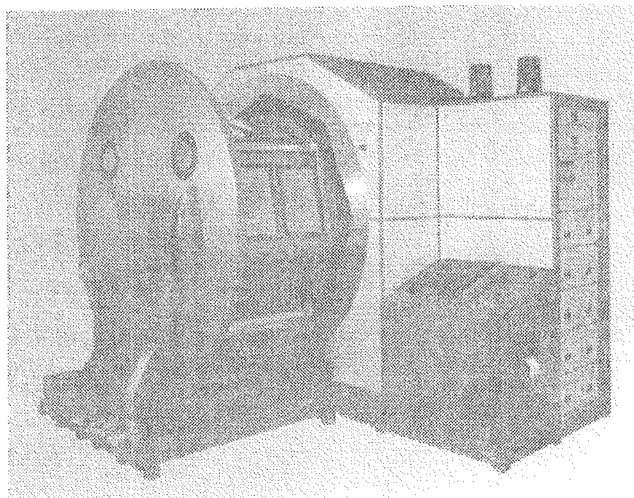

Fig. 9: Plasma plant MK IV with a capacity of six 18"x 24" panels - the world biggest plasma drill equipment.

Technics Plasma GmbH has built plasma drill equipment with different capacity. The currently world biggest plasma drill equipment MK IV has a capacity of six 18"x 24" panels per run (Fig. 9). The drill process lasts for approx. 25 minutes. As for the microwave batch ashing the plasma drill process is highly economical, based on 1-shift operation the operating cost per panel are 0.70 US $ only.

3.2 Substrate Cleaning prior to Wire Bonding and Encapsulation

Plasma cleaning of lead frames and Ball Grid Arrays (BGAs), especially Plastic-BGAs, has become a major focus for improving the reliability of high density interconnections.

Plasma treatment after die bonding has a dramatic influence on both the bonding yield and the bonding strength. Bonding yields with and without plasma cleaning are shown in Fig. 10 as a function of the ultrasonic energy used. Fig. 11 shows the strong improvement of bond strength after plasma cleaning with oxygen. Plasma removes here organic deposits that migrate to the bond pads during the curing process following die attach. The metal surface becomes highly activated and a solid metallurgical bond is much more easily formed. The entire process flow in IC packaging following the final wafer test is depicted in Fig. 12. The plasma treatment prior to wire bonding also activates the substrate for the encapsulation step. Adhesion of epoxy moulds used for encapsulation is strongly improved and their delamination in operation, called pop-corn effect, can be prevented.

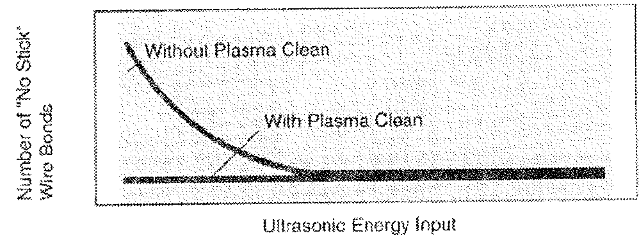

Fig.10: Effect of plasma cleaning for low ultrasonic energy input.

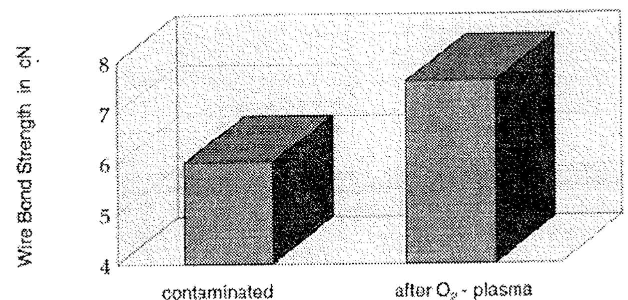

Fig.11: Optimum wire bonding through plasma cleaning.

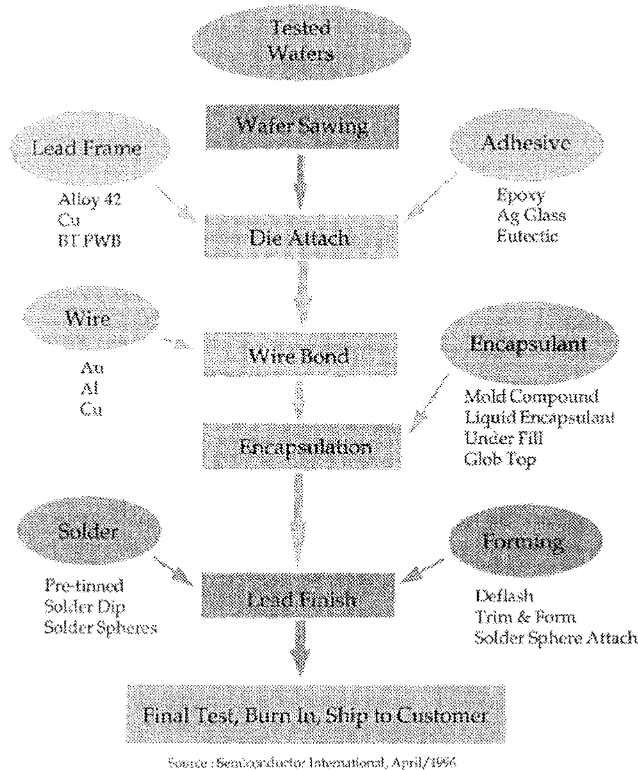

Fig.12: Process flow in IC assembling

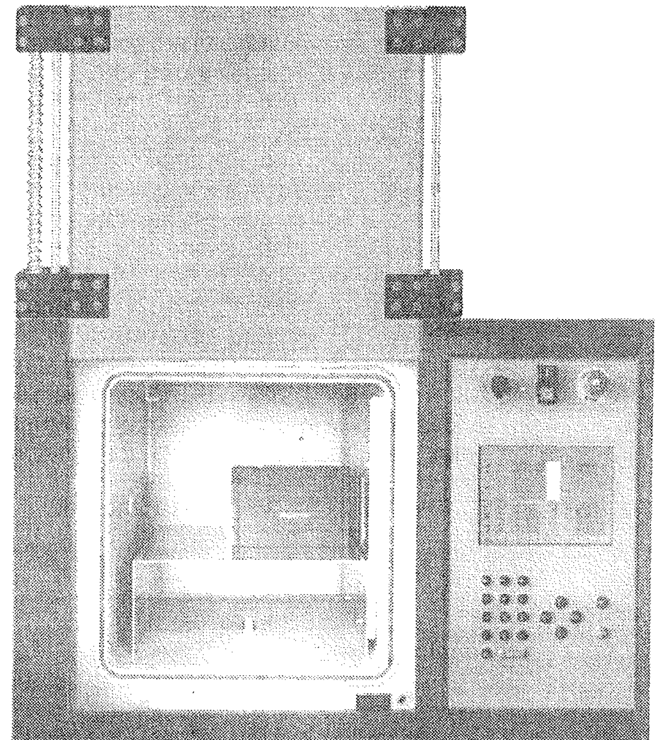

Fig.13: Plasma cabinet 400 Inline for cleaning of lead frames and PBGAs

Plasma processing in IC packaging increases in importance with the appearance of new lead frame materials, such as BT resin substrates or lower cost material. These substrates cannot handle the conventional wire bonding temperatures of 175-190 °C for long. High lead count devices will be packaged in these materials. Plasma cleaning will enhance the ability to lower the bonding temperatues maintaining high yields and high quality of components in the low cost BGA scenario.

Technics Plasma GmbH has built a lead frame and BGA cleaner shown in Fig. 13. The process chamber has a volume of 64 liters, the front-door opens vertically. This plasma system operates computer controlled and can be fully integrated in automated assembling lines.

4. Conclusions

The applications described in this paper demonstrate clearly the power of this technology for wafer fabrication as well as for PCB manufacturing. The low pressure plasma process works extremely reliable and cost-effective. Technics Plasma equipment features superior microwave technology showing a lot of advantages: electrodeless microwave power supply, very high yield and damage-free process.

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SEMICONDUCTOR GAS SENSORS AS AN EXAMPLE OF THICK-FILM TRANSDUCERS

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Key words: electronics, microelectronics, thick-film transducers, solid state transducers, thick-film hybrids, semiconductor gas sensors, manufacturing of sensors

Abstract: The research on solid state transducers started in the University of Oulu in the middle of the 1970s, soon after the beginning of the research on thick-film hybrids in the Microeletronics Laboratory. Screen printing is the common technology for the fabrication of both hybrid circuits and thick-film transducers, and has served also as a good possibility for the integration of our thick-film sensors with the necessary signal processing electronics in the form of hybrid modules. A novel double-paste screen-printing method was also developed in our Laboratory for the fabrication of multilayer transducer structures. Pad printing is another thick-film printing technique which offers the possibility for printing fine lines down to a width of about 50 μm. Therefore, it offers a possibility for more dense structures, especially in thick-film sensor arrays. A useful feature of the technique is that it offers a possibility to 3-dimensional printing, which allows a printing for complicated structures.

Semiconductor gas sensors are taken here as an example of our study on thick-film transducers. Our research on semiconductor gas sensors has continued since 1983 and during 1987-1991 we were a research partner in a EUREKA project that aimed to develop semiconductor gas sensors for some practical applications. We have also studied the possibility of using semiconductor gas sensors for monitoring of pollutant gases in combustion emissions and in city air. In a semiconductor gas sensor, the chemical receptor signal on the semiconductor surface is usually transduced through the microstructure of a sintered ceramic into a resistance change of the ceramic. Therefore, different thick-film tehcniques serve as a useful and economic way to produce these devices.

Plinski senzorji - primer razvoja debeloplastnih pretvornikov

Ključne besede: elektronika, mikroelektronika, pretvorniki debeloplastni, pretvorniki polprevodniški, hibridi debeloplastni, senzorji plinov polprevodniški, proizvodnja senzorjev

Povzetek: Z raziskavami na področju pretvornikov smo na Univerzi v Oulu začeli sredi sedemdesetih let, kmalu po začetku raziskav na področju debeloplastnih hibridnih vezij v Laboratoriju za mikroelektroniko. Sitotisk je primerna tehnologija tako za izdelavo hibridnih vezij kakor za izdelavo debeloplastnih pretvornikov in je tako ponujal možnost integracije debeloplastnih senzorjev s potrebno elektroniko za obdelavo signala v obliki hibridnih modulov. Za večplastne strukture pretvornikov smo v našem laboratoriju razvili nov način sitotiska. Za tiskanje ozkih linij s širino do 50 μm pa je primeren gravurni ofset tisk. To omogoča izdelavo še gostejših struktur, kar pride v poštev pri debeloplastnih senzorskih poljih. Uporabna značilnost tega načina tiskanja je, da omogoča tridimenzionalen tisk, kar posebej pride v poštev pri izdelavi zapletenih struktur.

Polprevodniške plinske senzorje smo tukaj vzeli le kot primer preučevanja debeloplastnih pretvornikov. Naše raziskave polprevodniških senzorjev tečejo že od leta 1983 in v letih 1987-1991 smo kot raziskovalni partner sodelovali v EUREKA projektu, katerega cilj je bil razviti polprevodniške plinske senzorje za praktično uporabo. Ravno tako smo preučevali možnost uporabe polprevodniških plinskih senzorjev za nadzor onesnaževanja mestnega zraka. V polprevodniškem plinskem senzorju kemijska sprememba na površini polprevodne keramike povzroči spremembo upornosti. Na ta način lahko različne debeloplastne tehnike uporabimo za učinkovito in ekonomično izdelavo omenjenih elementov.

1. INTRODUCTION

In the literature on sensors, gas sensing devices which consist of a semiconductor between two metal electrodes and which respond to changes in the composition of the surrounding atmosphere with a change in conductance are commonly termed as semiconductor gas sensors. Sometimes they are called as homogeneous gas sensors to distinguish these devices from structured sensors such as gas sensing diodes and field effect transistors. In the case where metal oxides are the gas sensitive semiconductors, the devices are also called oxide, metal-oxide or ceramic gas sensors.

Semiconductor gas sensors utilize the chemical sensitivity of semiconductor surfaces for gas sensing applications. A metal-oxide n-type semiconductor is the usual sensing material in these devices. The sensor detects a gas component due to a change in electrical conductance of a polycrystalline ceramic semiconductor. For the basic understanding of a chemical sensor one needs to separate the receptor function which

recognizes a chemical substance, and the transducer function which transduces the chemical signal into an electric output signal. In a thick-film semiconductor gas sensor, the chemical signal on the semiconductor surface is transduced through the microstructure of the sintered semiconductor into a resistance change. Hence, various grain contacts together with the grain size of the ceramic microstructure are the key concepts for the transducer function /1/. In addition, the mobility of donors, like oxygen vacancies in oxidic semiconductors, may have strong effects on the transducing properties of the sensors /2-4/.

Although the metal oxides used as sensing materials in semiconductor gas sensors have wide band gaps typical of insulators, they possess conductivity in the range of semiconductors due to point defects in the crystal structure. Semiconducting oxides are employed as gas-sensitive resistors for monitoring changes in oxygen partial pressure and small concentrations of impurity gases in air. In the case of response to changes in oxygen partial pressure at temperatures around 700 °C and above, the materials are reflecting the equilibria between the atmosphere and their bulk stoichiometry. The conductance change may then reflect the bulk conductivity effect, i.e. the change in the amount of bulk charge carriers due to native defects related to non-stoichiometry. An n-type binary oxide, TiO_2, is the material which is used commercially for these applications (lambda sensors).

In the case of the second major category which is to monitor the concentration of minor constituents of an atmosphere (normally air), the oxygen partial pressure remains effectively constant. For this type of application, the sensing material is normally held at a relatively lower temperature (below 500 °C), when some surface reactions cause the conductance changes. In sensor applications, the semiconductor material is usually in the form of a thick or thin film over a substrate containing metal film electrodes and a heating resistor. In this structure a high surface area to bulk ratio is achieved.

For the basic understanding of the operation of semicnductor gas sensors, one needs to know both the surface interaction with the active gases (receptor function) and the way to transduce it into conductance signals (transducer function).The dissociation of the oxide lattice (starting at the surface) occurs usually with low oxygen pressure and/or high temperature. In the case of sensing the oxygen partial pressure with the bulk conductivity change (lambda sensor), such a dissociation reaction is the prerequisite for the sensor operation. There is also the possibility that such a reaction will occur on the semiconductor surface at lower temperatures when "surface conductivity" changes are used for sensing. For this case, however, the mechanism most often quoted as the dominant one for detection of reducing or combustible gases in an oxygen containing atmosphere is the adsorption/desorption mechanism in which oxygen is preadsorbed on the surface of the material, trapping electrons from the conduction band, the amount of oxygen chemisorbed being controlled by the oxygen concentration and the amount of reducing gases in the atmosphere.

The surface defect mechanism, provided with the creation and diffusion of oxygen vacancies in the surface layer, is the other suggestion for the receptor function which may also provide a better explanation for some slow response and recovery properties of semiconductor gas sensors. The dissociation problem, which is very important in selection of semiconducting oxides for sensor applications, is closely related to slow and irreversible changes in the conductance of the sensor and limits even some of the most desirable oxides, such as ZnO, in their temperature range of application /5/. Removal of lattice oxygen by a chemical reaction on the oxide surface (CO or hydrocarbons, for example) is another source for the surface defect mechanism. Tin dioxide, SnO_2, has resistant surfaces against irreversible decomposition up to 500 °C and, therefore, it is the usual material in commercial sensors.

2. THICK FILM PRINTING TECHNIQUES

2.1 Screen printing and sensor integration

Thick-film technology based on screen printing serves as an economic way to produce sintered SnO_2 sensors with a high surface area to bulk ratio. The simple structure of a thick-film sensor is shown in Fig. 1(a). A planar ceramic alumina acts as the substrate for the thick-film sensor. Laser machining is used for scoring and drilling the alumina. Both the metal electrode (normally Au) and the SnO_2 layer over the electrode, are made by screen printing on the substrate which has a thick-film Pt heating resistor (around 10 Ω) printed on the reverse side of the substrate.

The gas-sensitive layer is prepared by making the semiconductor powder in the form of a paste suitable for screen printing. Commercial SnO_2 powders of high purity and decomposable salts of tin, such as $SnCl_4.5H_2O$ and $SnSO_2$, have been used in paste making for SnO_2 sensors. In the case when the chloride was used, different conductivity levels were obtained by adding Al or Sb in chloride form to the solution from which tin hydroxide was precipitated and the oxide formed in a calcination step. A surface binder, such as silica, is usually added to the mixture which is formed into the paste. The binder may have a strong effect on the characteristics of the sensor.

There are many procedures to introduce catalysts into the SnO_2 powders used to make thick-film layers. One way is to modify the SnO_2 powder with the catalyst, screen print the layer, and then sinter. Agglomeration of the metal particles into small isles results from this technique.

Screen printing is the common technology for the fabrication of hybrid circuits in addition to thick-film transducers, which has served as a good possibility for the integration of thick-film sensors with the necessary signal processing electronics in the form of a hybrid module. An integration of SnO_2 gas sensor into a screen-printed hybrid module is shown in Fig.1(b). Because of the heating of the sensor up to elevated tem-

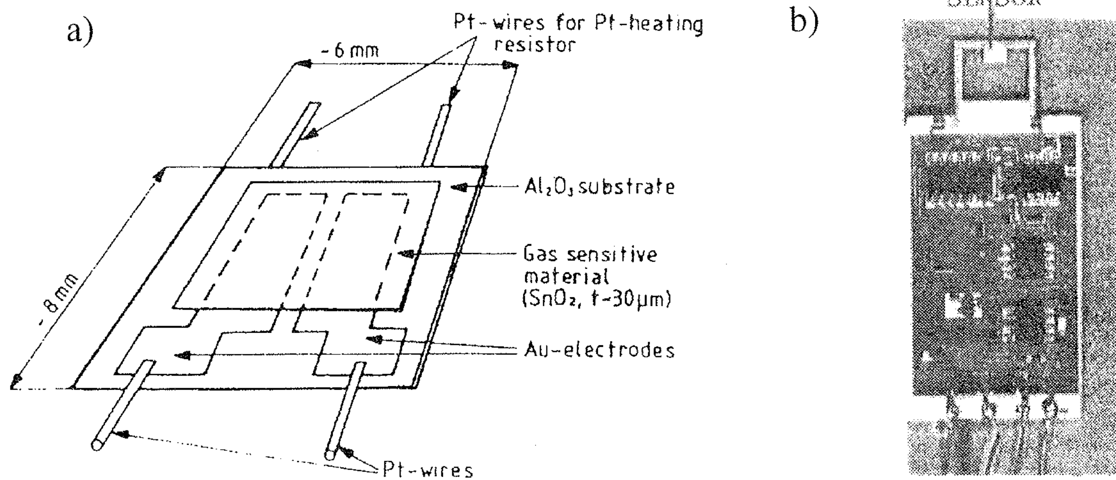

Figure 1: (a) Cross section of an SnO_2 thick-film sensor together with a Pt-heating resistor on the reverse side of an alumina substrate (6x8 mm^2). (b) An integration of a thick-film SnO_2 gas sensor (3x3 mm^2) with a signal-processing hybrid circuit into a screen-printed hybrid module.

peratures, it is connected to the hybrid circuit only with narrow (about 1 mm) alumina-substrate bridges containing electrodes both for sensing and for the Pt heating resitor on the reverse side. Conductance response is changed to a voltage output by the module.

2.2 Pad printing of one-electrode gas sensors

Standard thick-film technology based on screen printing is practicable for many sensor applications, but has also some limitations compared with thin-film techniques. The narrowest line widths obtained by standard screen printing are about 100 μm and this has some limitations for sensor applications. Pad printing or gravure-offset printing is a novel thick-film printing technique which offers the possibility of printing conductor lines down to a width of 50 μm /6/. The principle of gravure-offset printing is described in Fig. 2. The desired pattern which is etched in a gravure plate is first flooded

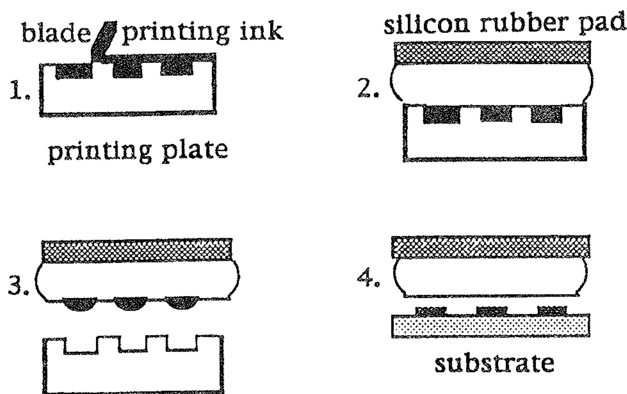

Fig. 2: Description of the principle of pad printing or gravure-offset printing.

with ink and then scraped clean so that ink remains only in the engraved pattern. Subsequently, the pattern is picked up and transferred from the plate by a flexible silicone rubber pad when it is pressed against the substrate. In order to get a good print, it is necessary to optimise all the parameters of the printing process. Typically the depth of the engraved pattern in the plate after etching is 15-25 μm. The smoothness of the substrate surface has a considerable effect on the quality of printing trace, but generally all thick-film substrates can be used. A useful feature of gravure-offset printing is that the technique offers a possibility of 3-D printing, which allows the printing of very complicated structures.

One-electrode semiconductor gas sensors are taken here as an example of the use of pad printing in sensor fabrication. In a typical sensor construction, the sensing semiconductor is between two metal (Au or Pt) electrodes and a third metal electrode, usually platinum, is used for the heating of the sensor device (Fig.1). In the one-eletrode construction /6/, a thin platinum-wire (ϕ = 20 μm) spiral is embedded inside a sintered oxide-semiconductor buttom. Figure 3(a) shows a construction of the one-electrode sensor /6/. The one-electrode spiral acts both as the heating resistor and measuring electrode, and the sensor works under a stabilized constant current feed. The function of the one-electrode sensor is based on shunting of the heating resistor as a result of a gas interaction with the oxide semiconductor. The equivalent circuit in Fig. 3(b) describes the operation of the sensor. At the gas exposure, the sensor response is obtained as a voltage change ΔV_M. In the case of a reducing gas like CO with an n-type semiconductor, a decrease of the overall resistance R (parallel resistance of the Pt resistor R_H and oxide-semiconductor shunt resistor R_S), decreases the heating power RI^2 (with a constant current I) and the operation temperature of the sensor.

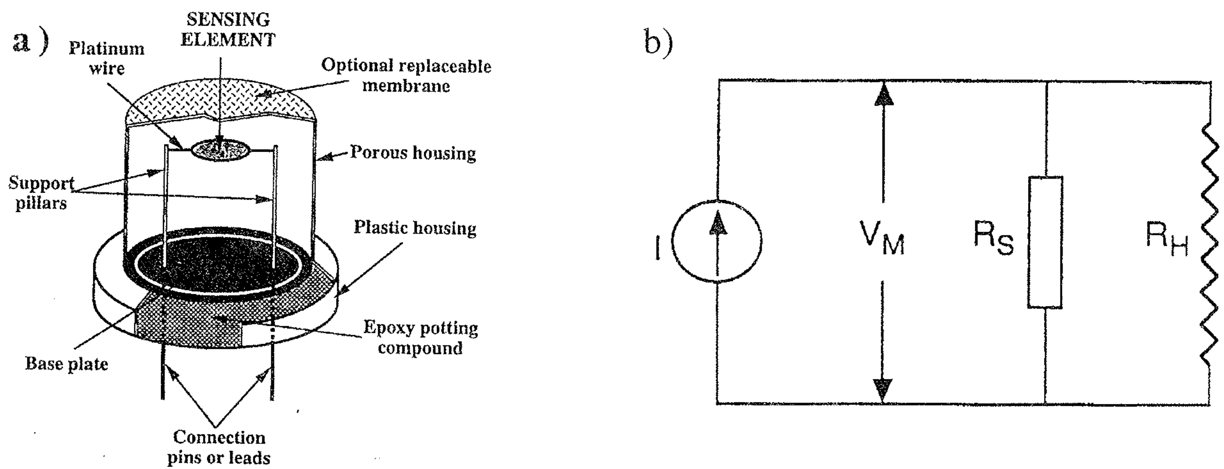

Fig. 3: (a) Structure of a bulk-type one-electrode semiconductor gas sensor where a thin Pt-wire spiral is embedded inside a sintered oxide-semiconductor buttom. (b) Equivalent circuit for the operation of the one-electrode semiconductor gas sensor. R_H and R_S are the Pt-heating resistor and shunting-semiconductor resistor, respectively.

Both screen printing and pad printing were used in the fabrication of our one-electrode thick-film sensors to print Pt thick-film resistors over alumina substrates. The structure of these two sensor types with screen-printed (I-type) and pad-printed (II-type) Pt resistors are shown in Figs. 4(a) and 4(b), respectively. Screen printing is used for the printing of the sensing SnO_2 thick film over the Pt resistor in both sensor types.

The practical limit for the minimum line width in screen printing is currently about 100 μm. This makes possible to print Pt resistors with resistance only up to few tens of ohms over a small substrate area (about 5x5 mm^2 or less) of the sensor. The shunting semiconductor thick-film resistor should have a resistance value of the same order with that of the Pt resistor at the operation temperature. That means, in the case of screen-printed Pt resistors, a heavy doping of the sensing oxide, e.g., SnO_2 with a group V element such as Sb. However, the heavy doping may change the sensing properties of the oxide film and impair the performance of the sensor. Therefore, an increase of the resistance of the Pt thick-film resistor is of great practical importance for the fabrication of our sensor prototype.

Pad printing offers possibilities for fine-line printing which makes possible to increase substantially the resistance of the Pt resistors. Sinterable Pt pastes for the resistor printing were modified by adding an appropriate mixture of organic binder and solvents to make the viscosity suitable for pad printing. Typically, the thickness of the fired conductors printed by gravure-offset technique ranges from 1 to 3 μm depending on the properties of the paste and the depth of engraving on the printing plate. The line width of the Pt resistor in Fig. 4(b) was possible to press down to about 50 μm. Then, pad printing made possible to produce Pt thick-film resistors with resistance up to kΩ and avoid the heavy doping of the sensing SnO_2 films with donors.

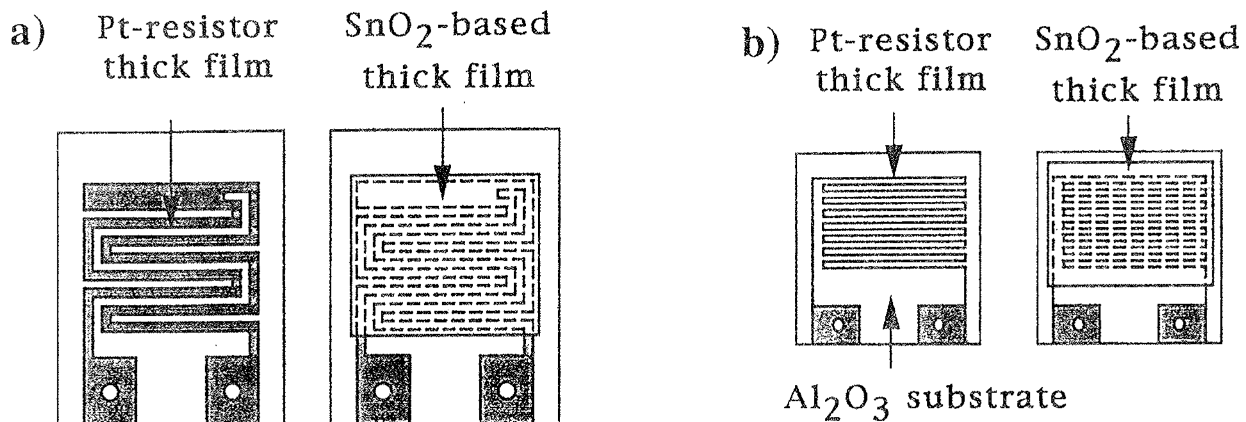

Fig. 4: Structure of thick-film one-electrode semiconductor gas sensors with a) screen-printed (I-type) and b) pad-printed (II-type) Pt thick-film resistors on alumina substrate. The SnO_2 sensing layer over the Pt resistor is screen printed in both sensor types. The substrate areas were 6x8 mm^2 and 5x5 mm^2 with the line width of Pt resistors of about 100 and 60 μm, respectively, for I-type and II-type sensors /6/.

The response of two one-electrode thick-film sensors with the same Ag-doped SnO_2 sensing layer to different amounts of H_2S (1,2,3, and 4 ppm) in dry synthetic air is shown as a function of time in Figs. 5(a) and 5(b), respectively, for sensors with screeen-printed (I-type) and pad-printed (II-type) Pt-heating resistors. Heating powers were adjusted in pure synthetic air to correspond the operation temperature of 450°C for both sensors. The sensor with the pad-printed Pt resistor (II-type) is sensitive to H_2S from 1 ppm level up, but the sensor with screen-printed Pt resistor (I-type) is not at all suitable for H_2S sensing in the low ppm range. The low resistance of the screen-printed Pt resistor as compared with that of the shunting SnO_2 layer is the reason for that behaviour. In the case of the II-type sensor in Fig. 5(b), the Pt-resistor resistance is comparable with the shunting resistance.

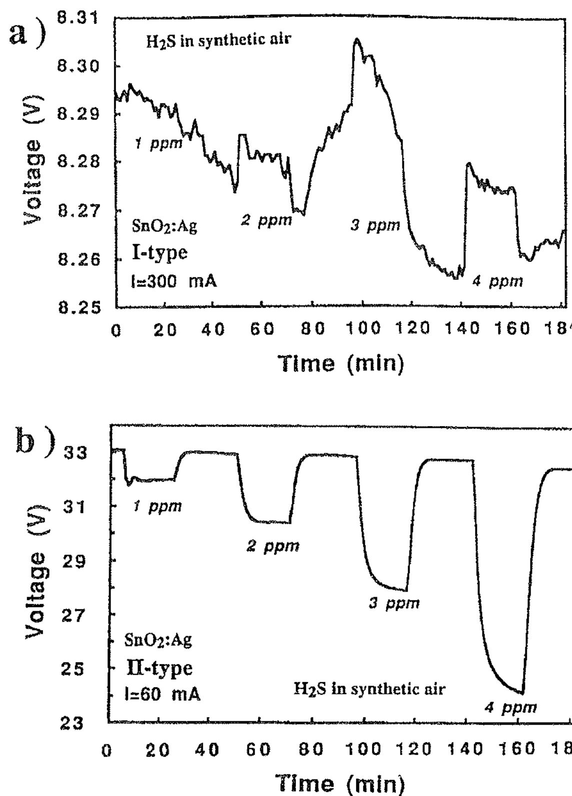

Fig. 5: Voltage response of (a) a I-type and (b) II-type sensor with Ag-doped SnO_2 sensing layer to 1, 2, 3 and 4 ppm of H_2S in dry synthetic air.

3. CONDUCTANCE OF SINTERED SnO_2 THICK FILMS

It is well known that negative charges accumulate on the surface of n-type semiconductor materials like SnO_2 in oxygen-containing atmospheres. According to the general electronic theory of chemisorption this is due to discrete energy levels introduced by oxygen within the band gap. This negative charge generates a depletion layer and a Schottky potential energy barrier on the semiconductor surface which has a very pronounced effect on the electrical conductivity if the material is in the form of porous ceramics, as in the case of SnO_2 thick films. The vibrating capacitor (Kelvin probe) seems to be a useful tool for measuring work-function changes also over the surface of thick-film samples /7/. Result of simultaneous response of work function and resistivity of some SnO_2 based thick-film samples to H_2 at three different temperatures of 420, 500 and 620 K /7/ support the Schottky barrier model for the conductance response. The depletion mode seems to prevail on SnO_2 surfaces in the presence of small H_2 concentrations in air, although in the UHV (ultra high vacuum) case, ionized surface donors, e.g., adsorbed hydrogen atoms or oxygen vacancies may turn the surface to the accumulation mode /8/. In the case of surface depletion, the work function eV_K of an n-type semiconductor increases by the amount of the Schottky barrier eV_S, as is sketched in Fig. 6(a). A decrease of the negative surface charge

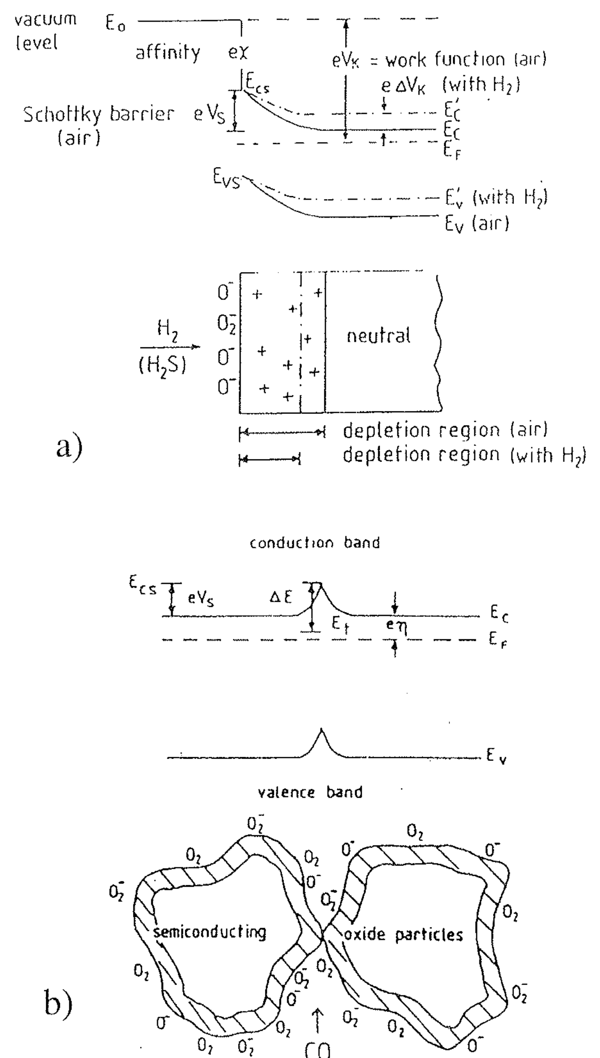

Fig. 6: (a) Illustration of the effect of negative surface charge (oxygen ions) and the Schottky barrier eV_S on the work function eV_K on the surface of an n-type semiconductor. (b) Schematic picture of the contact between two semiconducting oxide particles where the negative surface charge due to ionosorbed oxygen species generates a depletion layer and a Schottky barrier, as is sketched in the upper band diagram.

(adsorption/desorption mechanism) as a consequence of catalytic reactions, e.g., H_2 in the figure, also decreases the work function (by $e\Delta V_K$ in Fig. 6(a)). A change of the work function may origin also from the surface defect mechanism, since a release of lattice oxygen by a reducing agent such as CO at the surface may create a dipole layer at the ionic surface.

A schematic picture of the contact between two semiconducting oxide particles in sintered thick films is shown in Fig. 6(b) where the negative surface charge due to ionosorbed oxygen species generates a depletion layer and a Schottky potential energy barrier eV_S as is sketched in the upper band diagram in the figure. An energy level E_t introduced by oxygen within the band gap, near the Fermi level E_F in the surface region, is also shown in Fig. 6(b), although there are, of course, different levels related to different oxygen species (O_2^-, O^-). Reducing agents such as H_2 (or CO) in the ambient remove the negative charge from the surface by catalytic oxidation reactions (adsorption/desorption model) which have the effect to decrease the Schottky barrier eV_S and increase the conductance of the sample.

The Schottky barriers at intergranular contacts in sintered samples (Fig. 6(b)) dominate the resistance, since the electrons must overcome a substantial energy barrier eV_S in order to cross from one grain to another. In a compressed powder pellet, at least, the same constant surface barrier eV_S (Fig. 6(a)) may be assumed to exist on both sides of the intergranular contact in Fig. 6(b) and, as a first approximation, the conductance G at a temperature T may be described by the equation

$$G = G_o \exp(-eV_S/kT) \qquad (1)$$

where G_o may be considered as a factor which includes the bulk intragranular conductivity and geometrical effects. In order that the form of eqn. (1) is valid, the voltage drop at each intergranular contact must be less than kT/e so that the voltage dependence of the current is ohmic.

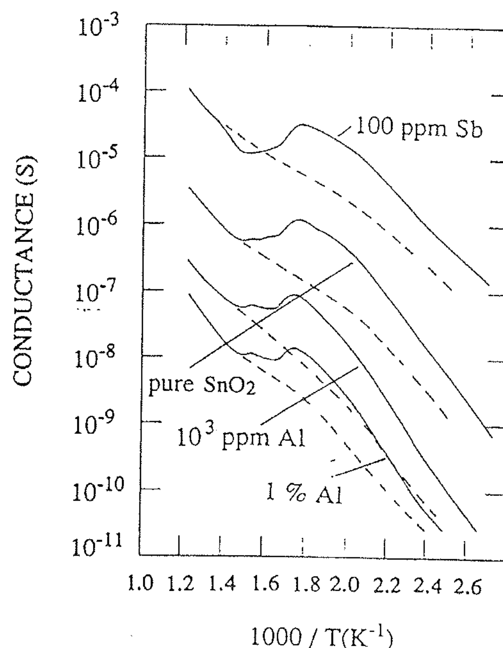

Fig. 7: Conductance of pure, Sb- and Al-doped SnO_2 thick-film samples with Au electrodes in dry synthetic air as a function of inverse temperature, measured at a cooling (- - -) and heating (——) rate of 2.4 $Kmin^{-1}$ /9/.

Figure 7 shows measured conductance values of pure, Sd-doped and Al-doped SnO_2 thick-film samples in dry synthetic air (humidity few ppm) between 100 and 550°C during heating and cooling with a rate of 2.4 $Kmin^{-1}$/9/. The Arrhenius plots with the irreversible conductance behaviour in Fig. 7 are very characteristic for sintered SnO_2 samples in dry ambient atmosphere. During heating, the conductance of all the four samples with very different surface concentration of electrons turn to decrease at exactly the same temperature of 280°C.

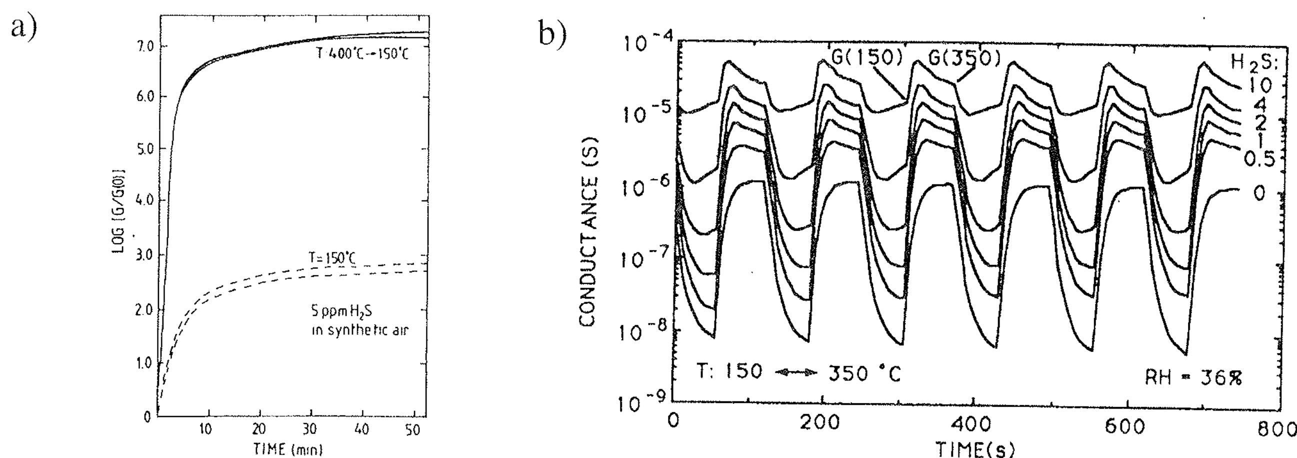

Fig. 8: (a) Conductance with time of two SnO_2 thick-film sensors in synthetic air after introduction of 5 ppm of H_2S at time zero on equilibrium surfaces at 150°C (- - -) and on non-equilibrium surfaces rapidly cooled from 400 to 150°C (——)/10/. (b) Conductance response of an SnO_2 thick-film sensor in the temperature-pulsed mode between 150 and 350°C to 0, 0.5, 1, 2, 4 and 10 ppm of H_2S in air with r.h. of 36 %.

Therefore, the behaviour origins from structural surface changes which naturally relate to the lattice-oxygen balance at ionic oxide surfaces. A clear understanding of the unusual sigmoid variation of conductance with inverse temperature were very desirable, since some "sensitization" of sensors seems to relate to this phenomenon. After a rapid cooling from temperatures above the downward deflection temperature (280°C), sensors are usually much more sensitive at low temperatures. Fig. 8(a) shows conductance response of two SnO_2 thick-film sensors in dry air after introduction of 5 ppm of H_2S at time zero on equilibrium surfaces at 150°C and on non-equilibrium surfaces rapidly cooled from 400 to 150°C /10/. In the case of equilibrium surfaces, the sensors were allowed to remain at 150°C for two days before the measurements, while in the case of non-equilibrium surfaces, temperature of the sensors was raised to 400°C and they were allowed to remain at this temperature for about 20 h. This makes possible a temperature-pulsed mode of sensor operation (Fig. 8(b)) /11/.

4. COMPUTATIONAL APPROACH FOR CHEMICAL SURFACE ACTIVITY

A model approach for the chemical response of a semiconductor surface is based (1) on a possible ionic response of the semiconductor bulk on changing internal electric fields, (2) on rate equations to describe electron transfer processes between the semiconductor- bulk Bloch states and surface adsorbates, and (3) on localized electron interactions at the surface. High-speed computers of today make possible to attack to all these three prerequisities for a proper dynamical treatment of the chemical surface activity /12/. At elevated temperatures, the grains in a ceramic semiconductor may behave as a solid electrolyte where dopant distributions inside the grains change with changing electrical potentials. Now, the electrical potential inside a grain is a solution of the Poisson-Boltzmann equation for which a computational approach is necessary, e.g., in the spherical grain geometry. It was found /13/ very large differences in the potential distribution inside a grain between the two cases with frozen and mobile donors, respectively. Expressions which are similar to those for the generation-recombination processes in semiconductors (Shockley-Hall-Read theory) can be used to describe the variation of electron transfer rates versus surface potential for MOS diodes. In our simulation procedure for electron transfer rates between the bulk Bloch states and surface adsorbates, we have adopted similar expressions to describe electron capture rates from the bulk conduction band, e.g., to oxygen surface species /14/.

A computational approach for localized electron interactions at the semiconductor surface is described here. A surface structure and adsorbates on the surface can be modeled either with a cluster, a chunk of surface, or a slab model, an infinite periodic system with a unit cell describing the surface structure of interest. Cluster models, which are often most convenient to describe localized structures and phenomena ignore the periodicity, and thus, yield a molecular electronic structure with discrete one-electron levels. If the band structure of the continuum levels at the surface is essential, one has to invoke the slab models and intrinsically periodic methods.

The case chosen to present here is stannic oxide SnO_2 and its (110) surface to illustrate some basic aspects of the gas-sensor surface phenomena. SnO_2 is one of the most applied material and the stable (110) face is its nonpolar surface that can be studied even in its bulk derived geometry without relaxation. Nitrogen oxide (NO molecule) is taken as an example of the adsorbate and chromium (Cr atoms) as an example of an impurity used to dope the SnO_2 semiconductor. The adsorption and doping effects can be examined as local phenomena to the extent where a cluster model in Fig. 9 is adequate /15/.

For such a large cluster the density functional method with the local density approximation (LDA) is the method of choice, if an ab initio level approach is desired. There are a collection of good commercial software, of which we have mostly been using DMol and DSolid from Biosym, but also academic codes have

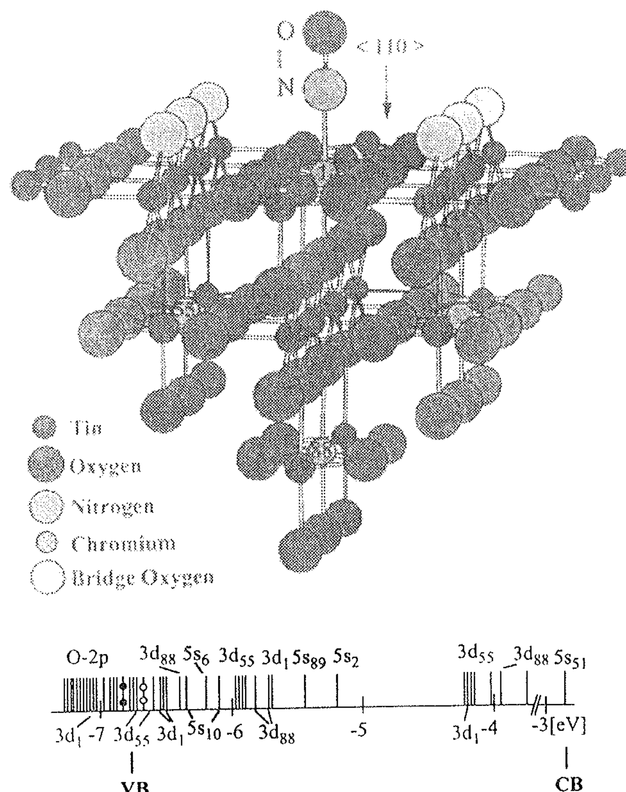

Fig. 9: Geometry of an $Sn_{28}O_{71}Cr_4$ cluster (in C_{2v} symmetry) modeling the (110)-1x1 surface of SnO_2. Cr atoms as dopants substitute some of the Sn at 1,55 (and its C_{2v} symmetry site) and 88 sites, and a NO molecule is placed as an adsorbate on a probable surface site. The bridge oxygen sites on the surface are assumed to be occupied in usual conditions. The calculated "molecular" one-electron level structure (without the adsorbate) at the "band-gap" region is shown below. Part of the population analysis (the strongest atomic orbital component of each level) is also shown /15/.

been employed for more specific purposes. Very briefly, these SCF ab initio methods are based on the linear-combination-of-atomic-orbitals (LCAO) theory and basis functions in numerical form from atomic and ionic calculations.

The band gap of bulk SnO_2 is about 3.6 eV, and roughly, the valence band maximum is created from 2p levels of oxygen and the conduction band minimum from 5s levels of tin. There are some surface states (levels) in the band gap, of which many are related to the missing bridge oxygen atoms. There are also gap levels arising from the finite size effect of our small cluster, i.e., there is more surface than only the intended (110) surface. All this can be nicely seen in the level map in Fig. 9. Chromium impurities in SnO_2 have a strong effect on the electrical properties both in the bulk and at the surface. It is a consequence of Cr 3d levels, which emerge in the band gap. The bulk impurities cause the deep levels near the valence band and the surface impurities create levels in the middle part of the gap. Both of these level types behave as conduction electron traps in an n-type SnO_2 semiconductor. This explains, for example, why Cr impurities have so strong effect on the conductivity of polycrystalline SnO_2 film.

Chromium impurities in SnO_2 have a strong effect on the catalytic properties, too. It seems that the high reactivity of Cr ions at the surface is responsible for the enhanced adsorption and dissociation of NO. We can start the analysis from the one-electron orbitals of the NO molecule, shown in Fig. 10.

The bond in the NO is formed by the fully occupied bonding 1π and 5σ orbitals and weakened by one electron in the antibonding $2\pi^*$ level. Thus, the bond is something between the triple bond of N_2 and double bond of O_2. Further occupation of antibonding levels would weaken the bond, and in fact, dissociation of free NO implies degeneration of the 1π, 5σ, $2\pi^*$ and $6\sigma^*$

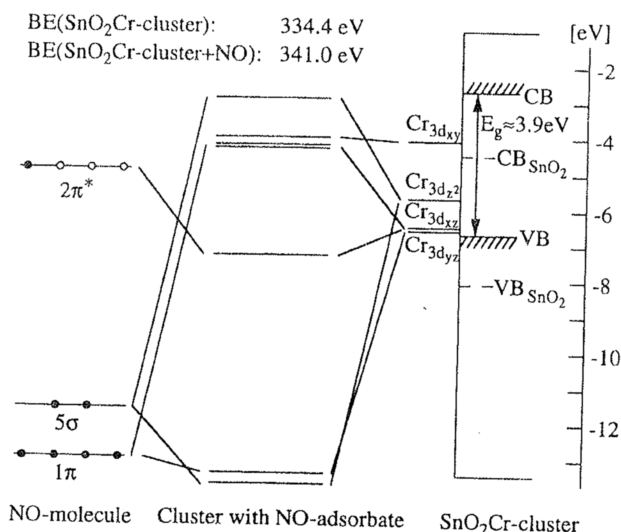

Fig. 10: Calculated one-electron levels of free NO molecule and the SnO_2-Cr cluster with and without the NO adsorbate. Only the levels originating from NO or Cr are shown explicitly /15/.

levels to the atomic 2p levels, thus decreasing (increasing) the occupation of bonding (antibonding) levels. This is also the mechanism of the NO dissociation on the Cr activated SnO_2 surface, though energetically much more favorable than the dissociation of free NO. In Fig. 10 it is seen how NO 1π, 5σ, $2\pi^*$ orbitals hybridize with the Cr 3d levels leading to slightly decreased occupation of bonding and strongly increased occupation of antibonding molecular orbitals. This is actually the conventional picture of transient formation of an NO^- ion with increased occupation of $2\pi^*$ in catalytic reduction of NO.

Surface relaxation and even reconstructions are known to be large for some compound semiconductor surfaces. Usually they are also essential in tuning the catalytic activity through adjusting the polarity and dangling bonds and oher factors in the surface density of states. In the present case removal or adding the bridging oxygen atoms in Fig. 9, change the surface relaxation considerably. For instance, we want to establish the role of the bridging oxygen atoms in the irreversible conductance behaviour of different doped SnO_2 samples in Fig. 7. In the case of CO exposure, for instance, conductance changes of the samples in Fig. 7 follow the exposure only at temperatures above 280 °C, and now the structural surface changes have also a close relation to the catalytic properties of the surfaces.

Though static geometries give certain understanding of surface processes in the long run with increasing computational resources it will be possible to study more dynamical aspects at the ab initio level. This could be done by ab initio molecular dynamics or through evaluation of potential energy hypersurfaces, for example /16/.

5. AN EXAMPLE OF H_2S MONITORING AS AN AIR POLLUTANT

An important application of gas sensors is for the measurement of air pollutants, concentrations of which are usually in the low ppb range. To obtain good sensitivity and selectivity to a certain polluting gas with semiconductor gas sensors is not very straightforward at the moment. We have used some Ag-doped SnO_2 sensors to monitor the H_2S concentration as a polluting agent in the atmosphere of the city Oulu /11, 17, 18/. A sensor array construction consisting of few SnO_2 sensors has been installed at the city air-pollution monitoring station where H_2S and SO_2 concentrations are being simultaneously recorded by commercial analysing equipment based on coulometric titration together with the conductance signals from the semiconductor gas-sensor array.

The southern part of the city Oulu was an ideal place for such a test. The schematic location of the city monitoring station (centre of the circle) is shown in Fig. 11 together with the city map and the distribution of wind directions in the city area. The most probable sources for polluting gases have also been marked on the city map. There are three concentrated sources of air pollution between the West North West (WNW) and the North North East (NNE) while the other directions are clean. The wind has about 40 % probability of blowing from the directions between WNW and NNE.

The recorder trace of a mV recorder was used to describe the conductance response of the SnO_2 sensors together with the H_2S and SO_2 outputs from the commercial analysers. The SnO_2 sensors, differently doped with Ag and mixed with Al_2O_3, were running at a constant temperature of 250°C during the monitoring. A recorder trace covering a day interval from the city station is shown in Figs. 2(a) and (b). The time period in Fig. 12(a) covers 24 h starting at 4.00 am (16 th December, 1990). During that time the wind turned from W to SSE, passing through the directions of the three main air-polluting sources in the city (a cellulose factory in WNW, the city heat power plant in NNW and a chemical factory in NNE). Half-hour average values of H_2S pollution in $\mu g/m^3$, available in a printed form from the station, are also shown around each hour in Fig.12(a). The relation 1 ppb $\approx 1.35\,\mu g/m^3$ holds for H_2S in atmospheric air around 20°C. The highest H_2S pollution peak (106 $\mu g/m^3$) appeared around 5.00 am from the cellulose factory. Between 2.00 pm and 11.00 pm, the origin of the H_2S pollution was the chemical factory and the half-hour average values of the H_2S pollution increased up to 8 $\mu g/m^3$. As is shown in Fig. 12(a), all the three SnO_2-based sensors are very sensitive to H_2S pollution. They also show conductance peaks between 8.00 am and 12.00 am when the wind blew from the direction (NNW) of the city heat power plant and the commercial analyser showed zero H_2S pollution. The same situation appears also in Fig. 12(b), where the wind stayed in clear directions all day and the readings from the commercial H_2S analyser were zero. In spite of that, the semiconductor sensors show some conductance peaks, especially around midday. It seems that the sensors are sensitive to H_2S pollution even in the sub-ppb range.

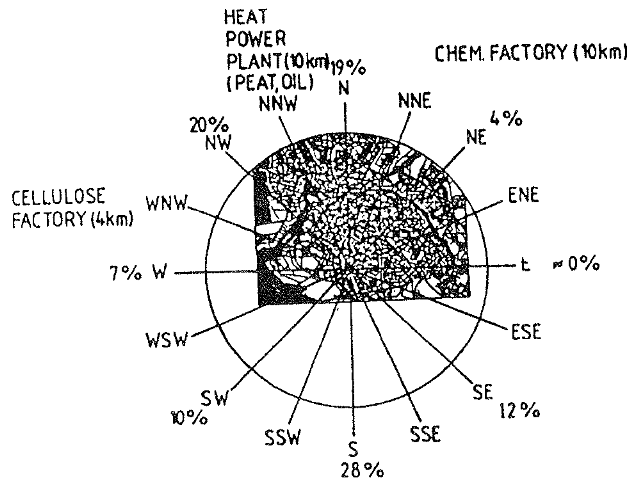

Fig. 11: Location of a pollution monitoring station (centre of the circle) shown on the city map of Oulu, Finland. The distribution of wind directions and three main polluting sources are also shown /17/.

6. SUMMARY

Semiconductor gas sensors are discussed as an example of research with different thick-film transducers in the Microelectronics and Material Physics Laboratories of the University of Oulu, Finland. The use of different thick-film printing techniques in the fabrication of semiconductor gas sensors is also described. An example is given of the use of the common screen-printing technology for the integration of a semiconductor thick-

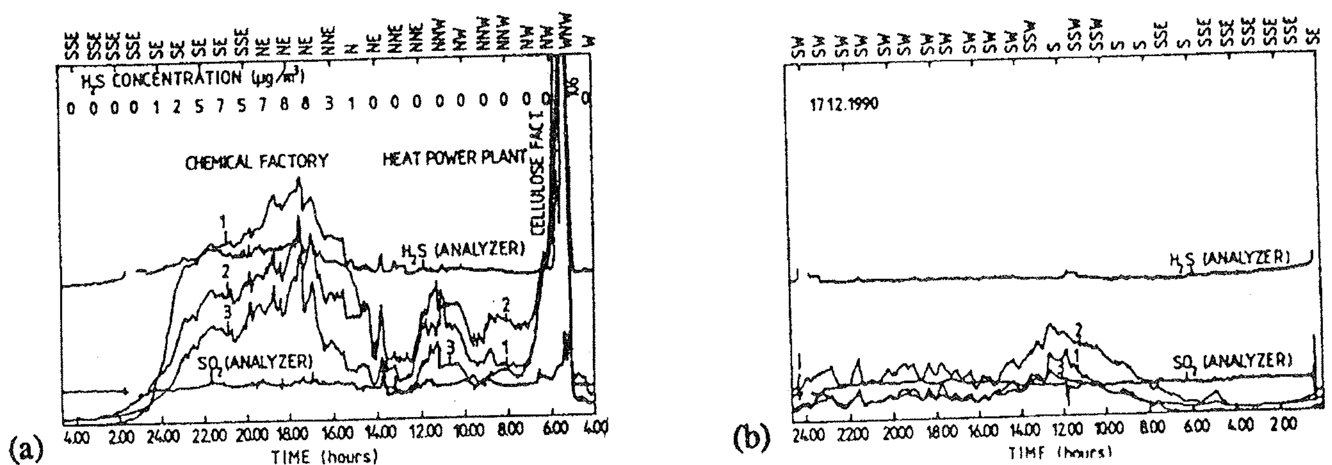

Fig. 12: (a) Recorder trace of 16th December, 1990 (starting 4.00 am) from the city air-monitoring station. Curves numbered 1 to 3 show the conductance response of the three differently doped SnO_2 + (Ag + Al_2O_3) sensors together with the outputs of the commercial H_2S and SO_2 analyser. The time scale increases from right to left and the wind directions, together with the half-hour average concentrations of H_2S, are shown at the top /11/. (b) Recorder trace of 17th December, 1990 from the city station with the same symbols as in (a). The wind was in clean directions between SE and SW all the time /11/.

film gas sensor with a hybrid circuit for signal processing. Semiconductor gas sensors in the form of the one-electrode construction are used to describe the possibilities of pad printing in the fabrication of thick-film transducers. Conductance response of semiconductor thick-film gas sensors to different ambient atmospheres is also discussed and a computational approach for the chemical activity of semiconductor surfaces is described. H_2S monitoring as an air pollutant in city air is taken as an example of the application of semiconductor gas sensors.

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CHEMICAL SENSORS BASED ON ISFET TRANSDUCERS

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Key words: microelectronics, chemical sensors, biochemical sensors, ISFET sensors, ISFET transistors, MOSFET transistors, theoretical fundamentals, semiconductor modelling, computer modelling, EIS capacitors, Electrolyte-Insulator-Semiconductor capacitors, fabrication technologies, electrochemical parameters, ion-sensitive, ion selectivity, ISFET-CMOS processes

Abstract: In this paper, we address the increasingly important and rapidly developing field of ISFET-based silicon integrated biochemical sensors. ISFET transduction mechanism, modelling and electrochemical characterization techniques are reviewed. ISFET fabrication technology, mainly with reference to the ISFET-CMOS process developed at IRST, is described. Two examples of ISFET-based systems for application in the environmental monitoring field are presented.

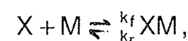
Kemični senzorji na osnovi ISFET pretvornikov

Ključne besede: mikroelektronika, senzorji kemijski, senzorji biokemijski, ISFET senzorji, ISFET transistorji, MOSFET transistorji, osnove teoretične, modeliranje polprevodnikov, modeliranje računalniško, EIS kondenzatorji elektrolit-izolator-polprevodnik, tehnologije proizvodnje, parametri elektrokemijski, občutljivost na ione, selektivnost za ione, ISFET-CMOS procesi

Povzetek: V prispevku opisujemo vse bolj pomembno in hitro se razvijajoče področje biokemičnih senzorjev na osnovi integriranih ISFET tranzistorjev na siliciju. Podamo mehanizme pretvorbe ISFET tranzistorjev, modeliranje in tehnike elektrokemične karakterizacije komponent. Ravno tako opišemo tehnologijo izdelave teh pretvornikov, kjer kot osnovo vzamemo ISFET-CMOS proces, ki smo ga razvili na IRST. Na koncu predstavimo dva primera uporabe senzorjev na osnovi ISFET pretvornikov pri nadzoru okolja.

1. INTRODUCTION

A chemical sensor is a device which is capable of converting a chemical quantity into an electrical signal. Chemical species to be detected are usually present in mixtures where the sample matrix might be gas, liquid or solid. For instance, a chemical sensor may be required to detect the presence of hydrogen in air (gas sensor), the presence of water vapour in air (humidity sensor) or the presence of ions in water (ion-sensitive sensor). A chemical sensor may also be requested to detect the presence of more complex molecules such as sugar or proteins in a liquid. A chemical sensor designed to detect a biological quantity is usually referred to as a biochemical sensor or biosensor. The different types of chemical sensors can be classified according to the sensing principle by which they detect the chemical measurand. For example, the interaction of a chemical species X with the sensing material M can usually be described by the following reaction:



$$X + M \underset{k_r}{\overset{k_f}{\rightleftharpoons}} XM,$$

where k_f and k_r are the forward and reverse reaction-rate constants. When the reaction liberates (or abstracts) heat due to a change in enthalpy, this can be detected calorimetrically. Alternatively, when the reaction is accomplished by liberation (or abstraction) of electrical charges, this can be detected conductimetrically, amperometrically, or potentiometrically. Selectivity, i.e. the capability to detect only the chemical species X among the many different ones usually present in the sample matrix, depends upon the nature of the reaction mechanism. Selectivity can be enhanced by selecting an active material M which reacts preferentially with the measurand X. Thin or thick layers of these active materials, eventually associated with some filtering action, can be coupled with suitable transducers to develop selective biochemical sensors.

This paper will focus on and discuss only potentiometric biochemical sensors based on the Ion-Sensitive Field-Effect Transistor (ISFET) /1, 2/. This choice is motivated by the following considerations. (i) An ISFET can be considered as a transconductance amplifier that transform an input voltage (high input impedance) to an output current (low input impedence). Therefore, ISFET-type potentiometric sensors do not draw any significant input current and the output signal is much less susceptible to noise. (ii) ISFET's lend themselves to low-cost mass production by using the well established silicon planar technology. (iii) ISFET's can be made compatible, with some limitations, with conventional CMOS processing, which allows smart sensors to be designed and fabricated.

The paper is organized as follows. ISFET theory and modelling are reviewed in Section 2, while fabrication technology is described in Section 3 with emphasis on the ISFET-CMOS fabrication process developed and currently in use at IRST (Trento, Italy). Section 4 is devoted reliability issues, mainly related to selective membrane deposition and device encapsulation and packaging. Finally, among the large variety of possible application of ISFET-based (bio)chemical sensors, only the increasingly important environmental monitoring field will be briefly addressed in Section 5, where two examples of applications recently developed at IRST are presented.

2. ISFET THEORY AND MODELLING

In this section, the operation of the ISFET is first outlined by comparing it to that of a MOSFET. Then, the theory of Electrolyte-Insulator-Semiconductor (EIS) systems is reviewed, and the chemico-physical phenomena underlying the ISFET transduction mechanism are described in more detail. Finally, a simulation technique is briefly described, aiming at a detailed, device-level analysis of pH-ISFET's.

2.1 ISFET vs. MOSFET

The operation of the ion-sensitive field-effect transistor can be best explained by comparing it to that of a conventional Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET).

As shown in Fig. 1, the ISFET can be viewed as a MOSFET in which the gate metal is replaced by an electrolytic solution with a reference electrode immersed into it. The sequence of contacting phases in the two devices is as follows:

- MOSFET: metal / silicon dioxide / silicon / metal
- ISFET: metal / Ag / AgCl / saturated KCl / test solution / pH-sensitive insulator / silicon dioxide / silicon / metal

where an Ag/AgCl electrode has been assumed as reference electrode for the ISFET. Moreover, the simplest case of ISFET has been considered (and will also be assumed in the following, unless otherwise stated), namely an H^+-sensitive ISFET. To make the device sensitive to other ionic species, specific polymeric membranes can be deposited on top of the gate insulator /3/. As can be seen, when transforming a MOSFET into an ISFET, the interface between metal gate and insulator is to be replaced by a number of additional phases representing the reference electrode, the solution under test, and the pH-sensitive insulating layer. Correspondingly, the ISFET threshold voltage, V_T^*, defined as the externally applied V_{GS} voltage required to bring the silicon surface to the onset of strong inversion, can be deduced from that of the MOSFET, V_T, by simply adding the potential drops at the additional interfaces /4/:

$$V_T^* = V_T + E_{ref} + \varphi_{lj} + \chi_e - \Psi_0(pH) - \varphi_m / q. \quad (1)$$

In the above equation, E_{ref} is the reference electrode absolute potential, φ_{lj} is the liquid junction potential difference between the reference solution and the electrolyte under test, χ_e is the electrolyte-insulator surface dipole potential, φ_m /q is the work function of the gate metal relative to vacuum. Ψ_0(pH) represents the potential difference between the insulator surface exposed to the electrolyte and the bulk of the electrolyte itself, and is actually the sole pH-dependent term in the ISFET threshold voltage.

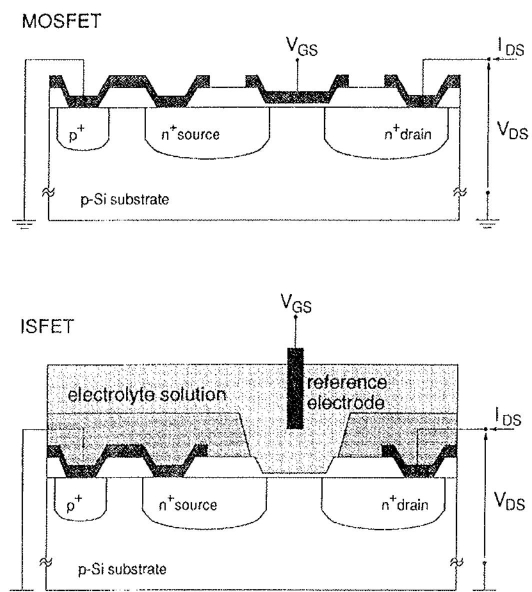


Fig. 1: Schematic cross-sectional view of a MOSFET compared with that of an ISFET.

Once the threshold voltage is known, the current flowing from source to drain in an ISFET can formally be expressed, as a function of the applied voltages, exactly in the same way as in a MOSFET, i.e.:

$$I_{DS} = \begin{cases} K\left[\left(V_{GS} - V_T^*\right) - \left(V_{DS}/2\right)\right]V_{DS} & for\ V_{DS} < V_{GS} - V_T^* \\ K/2\left(V_{GS} - V_T^*\right)^2, & for\ V_{DS} > V_{GS} - V_T^* \end{cases} \quad (2)$$

where the conduction factor K is given by K = μ_n Ci W/L, μ_n being the electron (for an n-channel device) mobility, Ci the insulator capacitance per unit area, W and L the channel width and length, respectively.

In the next section, the term Y0(pH) of the ISFET threshold voltage will be shown to be correlated to the surface chemical reactions occurring at the electrolyte-insulator interface. Already at this point of the discussion, however, it is possible to understand the operating principle of the ISFET as a pH sensor: any chemically-induced change in one of the terms at the right-hand side of eqn. 1 shifts, in fact, the threshold voltage of the device, inducing a corresponding change in the device current which can be detected and monitored. To this purpose, ISFET's are normally operated at constant I_{DS} and V_{DS}, i.e. using a feedback circuit, as that depicted in Fig. 2, which compensates for induced changes in I_{DS} by adjusting V_{GS}. The device is commonly biased in the linear part of the triode region (i.e. with $V_{DS} << V_{GS} - V_T^*$), where the drain current, written by neglecting the non-linear term, is simply given by

$$I_{DS} \cong K\left(V_{GS} - V_T^*\right)V_{DS} \quad . \tag{3}$$

Combining eqns. 3 and 1 yields:

$$V_{GS} \cong I_{DS} / (KV_{DS}) + V_T + E_{ref} + \varphi_{lj} + \chi_e - \Psi_0(pH) - \varphi_m / q , \tag{4}$$

which, for I_{DS} and V_{DS} held constant, can be written as:

$$V_{GS} \cong const. - \Psi_0(pH) . \tag{5}$$

The term denoted as "const." in the above equation summarizes all the quantities at the right-hand side of eqn. 4 which are unaffected by a change in the solution pH. It is evident from eqn. 5 that any change in the electrolyte pH will induce a corresponding change in the gate voltage V_{GS}. This latter can therefore be assumed as the pH-dependent output voltage of the circuit shown in Fig. 2.

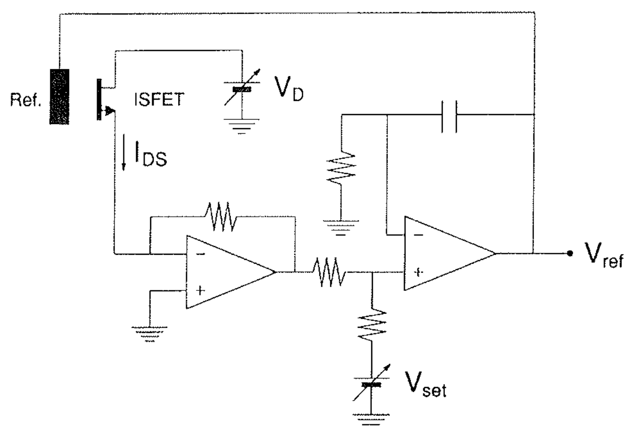


Fig. 2: Sketch of a feedback circuit for measuring pH sensitivity in ISFET devices.

2.2 THE ELECTROLYTE-INSULATOR-SEMICONDUCTOR SYSTEM

ISFET transduction mechanism relies on the properties of the Electrolyte-Insulator-Semiconductor (EIS) capacitor forming the gate structure of the device.

The response of EIS systems to changes in the electrolyte proton concentration is commonly explained by invoking the so-called *site-binding* theory /5/, to describe the physico-chemical processes occurring at the electrolyte-insulator (EI) interface /4, 6 - 10/. According to this theory, the presence of ion-specific binding sites at the surface of the insulator exposed to the electrolyte is responsible for the development of an ion-charge layer on the insulator surface, as a result of chemical reactions between binding sites and H^+ ions. In addition, other ions present in the solution (for instance, Na^+ and Cl^- in a typical univalent electrolyte) can form ion pairs with the charged surface sites. The electrical double layer developing at the electrolyte-solid interface is then completed by a diffuse charge layer formed by the hydrated electrolyte ions. A schematic picture of the charge density distribution throughout the EIS system is given in Fig. 3(a), where σ_0, σ_β, and σ_d represent the charge densities associated with surface sites, counter-ions, and diffuse layer, respectively. Figure 3(b) shows the corresponding electrostatic-potential distribution. The Outer Helmholtz Plane (OHP) is the locus of the centers of the hydrated ions forming the diffuse layer with the closest approach to the solid, while the Inner Helmholtz Plane (IHP) is the plane of the adsorbed ions which form pairs with the charged surface sites.

In an EIS structure having Si_3N_4 as dielectric material exposed to the electrolyte, silanol sites, as well as primary, secondary, and tertiary amine sites, are present on the Si_3N_4 after oxidation. Neglecting the contribution of secondary and tertiary amine sites, the charge density σ_0 due to surface sites can be expressed as /4/ (similar expressions hold also for different insulating materials):

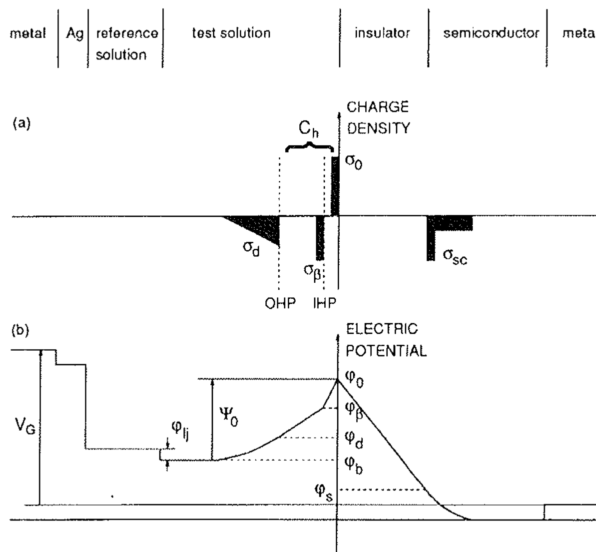


Fig. 3: Sketch of the charge-density (a) and electric-potential (b) distributions in an EIS structure.

$$\sigma_0 = q\left(\frac{[H^+]_s^2 - K_+K_-}{[H^+]_s^2 + K_+[H^+]_s + K_+K_-}\right)N_{sil} + \tag{6}$$

$$+q\left(\frac{[H^+]_s}{[H^+]_s + K_{N+}}\right)N_{nit}.$$

In the above equation, N_{sil} and N_{nit} are the silanol and primary amine binding-site density, respectively, whereas K_+ , K_- and K_{N+} represent the dissociation constants of the surface chemical reactions involving binding sites and H^+ ions. $[H^+]_s$ represents the proton concentration at the EI interface, which is related to that assumed in the electrolyte bulk $[H^+]_b = 10^{-pH}$ through the Boltzmann equation:

$$[H^+]_s = [H^+]_b\, exp[-q(\varphi_0 - \varphi_b)/(kT)], \tag{7}$$

where φ_0 and φ_b are the electrostatic potential at the EI interface and in the electrolyte bulk, respectively. The diffuse layer is governed by the Gouy-Chapman-Stern theory, which dictates that the charge in a column of unit cross-sectional area extending from the OHP to the electrolyte bulk is given by /6, 8/:

$$\sigma_d = \sqrt{8\varepsilon_w kTc_0}\,\sinh\left[\frac{q(\varphi_b - \varphi_d)}{2kT}\right], \tag{8}$$

where φ_d is the potential at the OHP, c_0 is the ion concentration of the solution, and ε_w is the solution permittivity. Neglecting the counterion charge (σ_β) at the IHP, φ_d is related to φ_0 by the Gauss law applied to the electrolyte region extending from the EI interface to the OHP:

$$\varphi_d = \varphi_0 + \frac{\sigma_d}{C_h}, \tag{9}$$

C_h being the capacitance per unit area of the complete Helmoltz layer.

To complete the EIS model, additional equations are needed, defining the charge distribution in the solid-state part of the structure. From the MOS-capacitor theory, one can express the semiconductor charge density, σ_{sc}, as a function of the sole electrostatic potential at the insulator-semiconductor interface, φ_s:

$$\sigma_{sc} = \pm\sqrt{2\varepsilon kTp_{p0}}\left[\left(\frac{q\varphi_s}{kT} - 1 + exp\left(\frac{q\varphi_s}{kT}\right)\right) + \frac{n_{p0}}{p_{p0}}\left(\frac{q\varphi_s}{kT} - 1 + exp\left(\frac{q\varphi_s}{kT}\right)\right)\right]^{1/2}. \tag{10}$$

In the above equation, ε_s is the semiconductor permittivity, n_{p0} and p_{p0} are the equilibrium concentrations of electrons and holes, respectively, and the sign plus applies to the case of $\varphi_s<0$, the minus to the case of $\varphi_s>0$. Moreover, the Gauss law applied to the insulator region yields:

$$\sigma_{sc} = C_i(\varphi_s - \varphi_0). \tag{11}$$

Finally, the charge neutrality for the whole EIS system requires that:

$$\sigma_0 + \sigma_d + \sigma_{sc} = 0, \tag{12}$$

where charges in the oxide and at the $Si\text{-}SiO_2$ interface have been neglected for simplicity.

Equations 6 to 12 can be assumed as the EIS system model. From a mathematical point of view, they form a system of seven equations, which, for instance, can be solved for the following seven unknowns: σ_0, $[H^+]_s$, σ_d, σ_{sc}, φ_0, φ_d, and φ_s, having assumed $[H^+]_b=10^{-pH}$ and φ_b (which differs from the externally applied gate voltage by a constant) as externally defined parameters. So doing, the charge and potential distribution in the whole EIS structure can be calculated for any given value of the solution pH and of the externally-applied gate voltage. Alternatively, system 6-12 can be solved with φ_b unknown and φ_s set to the value of $2\phi_F$ (ϕ_F being the Fermi potential in the semiconductor region), that is, to the onset of strong inversion condition at the semiconductor-insulator interface. In this case, the quantity $\Psi_0=\varphi_0-\varphi_b$, which enters into the ISFET threshold voltage expression (see eqn. 1), can be computed as a function of the solution pH.

2.3 DEVICE-LEVEL SIMULATION

Efforts aimed at making the ISFET fabrication process compatible with CMOS techologies are in progress, to allow chemical sensors and signal-conditioning electronics to be integrated on the same chip. This fact, while opening the way to the development of chemical

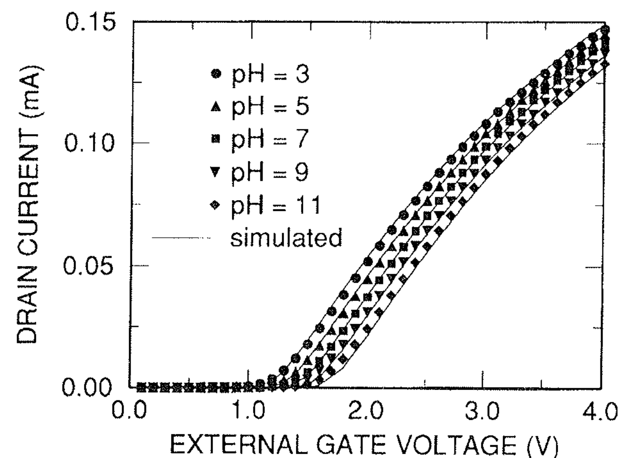


Fig. 4: ISFET transfer characteristics at different pH and V_{DS}=0.1 V.

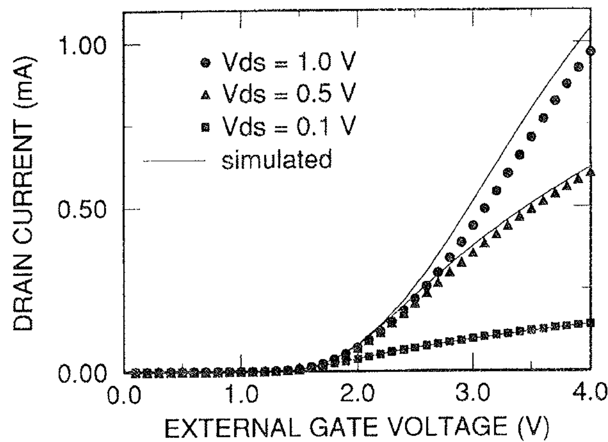


Fig. 5: ISFET transfer characteristics at different drain voltages and pH=7.

smart sensors, imposes that suitable CAD tools be adopted to efficiently and reliably design ion-sensitive IC's. To meet this need, a SPICE model has, for instance, been proposed in /4/. When dealing with the development of ISFET devices and the optimization of fabrication processes, however, a more straightforward relationship between process parameters and device electrical responses is desirable, with respect to that allowed by compact, circuit-simulation-oriented models. This can be achieved by means of device-level simulation. In the following, a technique is briefly described, which allows for the device-level analysis of pH ISFET's. Full account of the simulation technique, as well as of its experimental validation, can be found elsewhere /11, 12/. In this approach, the ion-charge build-up model given by eqns. 6-9 is incorporated into the 2D device-simulator HFIELDS /13/. Such a program solves the fundamental device equations, i.e. Poisson and carrier-continuity equations for electrons and holes, supplemented by the drift-diffusion expressions for the electron and hole current densities. Numerical solution of these equations is carried out by discretizing them on a 2D triangular grid. To the purpose of linking eqns. 6-9 to the semiconductor-device model, a gradual approximation is assumed to hold within the electrolyte, i.e., the potential at the electrolyte-insulator interface is assumed to vary slowly along the direction parallel to the insulator surface. This allows for the adoption of a 1D, lumped model of the charge distribution in the electrolyte along the direction normal to the same surface. Equations 6-9 are then coupled with Poisson's equation and solved at each element of the discretized electrolyte-insulator interface, thus providing a self-consistent description of the charge and potential distribution within the whole EIS system. By this approach, technological details such as the actual doping profile, specific geometries, surface defects, oxide-trapped charge, etc., can easily be taken into account and the TCAD optimization of the ISFET device and fabrication process is made feasible.

To validate the implemented models, the HFIELDS program equipped with the new capability has been employed to simulate ISFET's fabricated at IRST with a CMOS-compatible technology, whose main features are described in the next section. Computed characteristics have, then, been compared to actual device responses. Experimental characteristics shown in the following were measured in the dark at 25°C, with the gate voltage applied through an Ag/AgCl reference electrode, soaked in a 0.1 M, NaCl solution electrolyte. Titration was performed by adding NaOH and HCl to the solution, while monitoring the pH value with a Crison 2002 pH-meter. Simulations take into account a realistic description of the actual doping profile, as well as fixed oxide charges and Si-SiO_2 interface traps. Figures 4 and 5 show the transfer characteristics at different pH values (at a given V_{DS}) and at different V_{DS} values (at a given pH), respectively. As can be seen, the agreement between simulated and measured curves is quite satisfactory and, in particular, the pH-dependent threshold shift is predicted accurately. A sensitivity of about 53 mV/pH can be extracted from the simulated V_{GS}(pH) data, in good agreement with both experimental results and literature data /14/.

3. FABRICATION PROCESS AND ELECTROCHEMICAL CHARACTERIZATION

As an example of ISFET fabrication technology, the ISFET-CMOS process developed at IRST is described in the first part of this section. Then, the main electrochemical parameters used to characterize ISFET's as pH sensors are defined and the main issues related to their measurement are discussed. Finally, results are presented from the electrochemical characterization of a chip, which has been especially-designed and fabricated to test the suitability of the IRST ISFET-CMOS technology for the production of ISFET-based pH sensors with on-chip read-out electronics /15/.

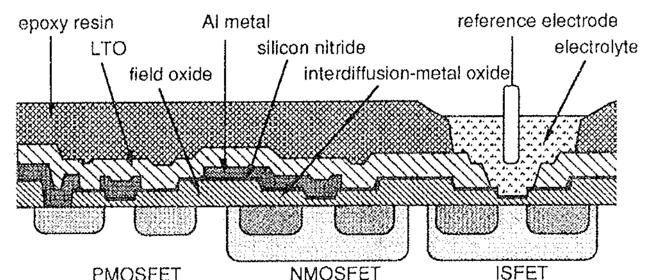


Fig. 6: Cross-sectional sketch of the n-channel ISFET and n- and p-channel MOSFET's produced by the ISFET-CMOS technology.

3.1 FABRICATION TECHNOLOGY

A summary of the process sequence is reported in Table 1, while a schematic cross-sectional view of the active devices produced is shown in Fig. 6. The basic sequence of the fabrication process consists of 13 photosteps and 7 implants, and closely resembles that of a conventional p-well, metal-gate, CMOS process. Some process steps have, however, been added or improved in order to get a higher flexibility and to make active

devices more resistant to the hostile conditions of the typical application environment. The threshold voltages of p- and n-channel devices, ISFET's included, are adjusted by separate implants. Channel-stop implants have been implemented for better device isolation, while, for improved ESD immunity, the natural inter-diffusion-metal oxide has been thickened by adding an undoped oxide, deposited at 712°C in an LPCVD system using TEOS. In addition, the breakdown voltage of source and drain junctions, as well as the source and drain contact resistances have been optimised in view of the CMOS integration. The gate dielectric is composed of 110 nm of thermally-grown SiO_2 and 100 nm of Si_3N_4, this latter providing the ion-sensitive layer. The Si_3N_4 layer is deposited at 775°C in an LPCVD system (ASM DRF 210), using ammonia and diclorosilane in a 4:1 flow ratio. Appropriate annealing steps are carried out to stabilize the layered oxide/nitride dielectric and to reduce the interface trap density. In order to minimize the fabrication process complexity the Si_3N_4/SiO_2 double layer is present on all transistors.

Table I: IRST ISFET-CMOS fabrication process outline

Substrate: CZ, (100), 8 ohm-cm, n-type Si
1st photostep: p-well 1st implant: Boron, 100 keV, $4.5x10^{12}$ cm^{-2}, through screenoxide p-well drive in: 1150°C, 15 h, dry
2nd photostep: p+ guard-ring 2nd implant: Boron, 120 keV, $1x10^{13}$ cm^{-2}, through screenoxide 3rd photostep: n-substrate active area 3rd implant: Phosphorus, 70 keV, $3x10^{12}$ cm^{-2}, through screenoxide field-oxide growth: 975°C, 9 h, steam, 1150 nm
4th photostep: define diodes
5th photostep: p^{+}-select 4th implant: BF_2, 80 keV, $5x10^{15}$ cm^{-2}, through screenoxide diode drive in: 975°C, 80 min, inert ambient
6th photostep: n^{+}-select 5th implant: Phosphorus, 80 keV, $5x10^{15}$ cm^{-2}, through screenoxide diode drive in: 1150°C, 1 h, inert ambient
7th photostep: define gate area 8th photostep: p-select 6th implant: BF_2, 50 keV, $1x10^{12}$ cm^{-2}, through sacrificial oxide
9th photostep: n-select 7th implant: Boron, 30 keV, $1x10^{12}$ cm^{-2}, through sacrificial oxide 10th photostep: p & n-select gate-oxide growth: 975°C, 30 min, dry, 30 nm LPCVD nitride deposition: 795°C, 30min, dry, 100 nm
11th photostep: contact opening Al sputtering deposition: 1200 nm
12th photostep: define metal LTO deposition: 430°C, 30 min, 500 nm
13th photostep: define overglass contact sintering: 400°C, 5 min

3.2 ELECTROCHEMICAL PARAMETERS

pH-sensitive insulators are characterized by three main parameters: sensitivity, drift rate, and hysteresis. These parameters appear to depend on the same fundamental phenomena occurring at the insulator-electrolyte interface and are therefore correlated to each other. Their values are influenced by the measurements procedure as well, and therefore suffer from lack of standardization, which often makes it difficult to quantitatively compare results published in the scientific literature.

Sensitivity is defined as the sensor output-voltage variation, induced by a unit change in the pH of the electrolytic solution. With the ISFET operated as in Fig. 2, for instance, pH-sensitivity can be measured by evaluating the slope of the $V_{GS}(pH)$ linear regression. This parameter greatly depends on the chemical/morphological characteristics of the insulating layer exposed to the electrolyte.

ISFET operation has so far been assumed to be exempt from nonidealities, such as long-term drift and hysteresis. On the contrary, such phenomena have been found to affect all the main insulators used as pH-sensing surfaces, ultimately limiting the accuracy with which an ISFET can be used to measure pH.

Long-term drift is evidentiated by an irreversible output-voltage variation with time at constant pH. Despite no conclusive arguments about its origin has been presented yet, drift appears to be a consequence of the interaction of certain ions present in the electrolyte with either the surface or the bulk of the insulator /16/. An important characteristic of drift, which is common to all the main insulators used in ISFET's, is that the drift rate tends to rapidly decrease with time. This means that by waiting for a sufficiently long time, drift can be reduced to very low values. State-of-the-art Si_3N_4-ISFET's, for instance, show, after appropriate stabilization, drift of $0.1 \div 0.3$ mV/h.

A much more serious problem for the accuracy of the sensor is hysteresis, observed when an ISFET is exposed to consecutive upward and downward pH sweeps. Hysteresis is usually measured by evaluating the difference in the residues of the V_{ref} vs. pH linear regression after a pH closed loop. This phenomenon has been suggested to be a direct consequence of the presence in the ISFET time response to pH changes of a slow, delayed term following the immediate response /17/. While this latter lasts less than $1 \div 2$ min and accounts for more than 90% of the overall output variation, the time constant characterizing the slow response after a pH step is tipically in the order of $3 \div 4$ h. As a result, when the device is exposed to a periodic pH input, the output will be somewhat delayed relative to the input and thereby show a hysteresis. Due to the slow response, long-term drift has to be measured after appro-

priate stabilization time, in order to minimize the memory for previous pH change, avoiding any significant overlap between the long transient response and the actual device drift. As far as the origin of the slow response to pH changes (and therefore of hysteresis) is concerned, the most probable explanation, in the context of the site-binding model, is that a fraction of the sites responds more slowly to pH changes than those accounting for the immediate response This could in turn be due to imperfections in the insulator layer, such as roughness or microporosity, giving rise to sites located beneath the insulator surface. In the specific case of Si_3N_4, such interior sites might be secondary amines located close enough to the surface to be able to partecipate in a slow equilibrium with protons /17/. It is, in any case, widely recognized that more fundamental work, using surface physico-chemical characterization techniques, as well as improved phenomenological modelling, is needed for a complete understanding of the response of pH-sensing insulators employed in ISFET's.

3.3 AN ISFET-CMOS TEST CHIP

The test chip, a microphotograph of which is shown in Fig. 7, consists of three separate sections to cover the three main aspects involved in the ISFET-CMOS technology development, i.e. sensor optimization, techology evaluation, and testing of basic integrated-circuit blocks. With reference to Fig. 7, the top portion of the chip contains an ISFET and two matched, Al-gate, n-channel MOSFET's that can be used either coupled with the ISFET in a differential-stage configuration or as thermal sensor. The channel length and width of both ISFET and MOSFET's are 20 and 800 μm, respectively. The source and drain regions are extended to one end of the chip to the purpose of outdistancing the contacts from the gate region, thus easing lead attachment and packaging. The intermediate region of the chip is devoted to basic signal-processing circuit blocks and contains a differential stage and output stages of different types (CMOS, NMOS, and double-stage NMOS) and amplification factors. The bottom portion of the chip contains several test structures (such as differently sized capacitors, diodes, resistors, and transistors) devoted to technology evaluation.

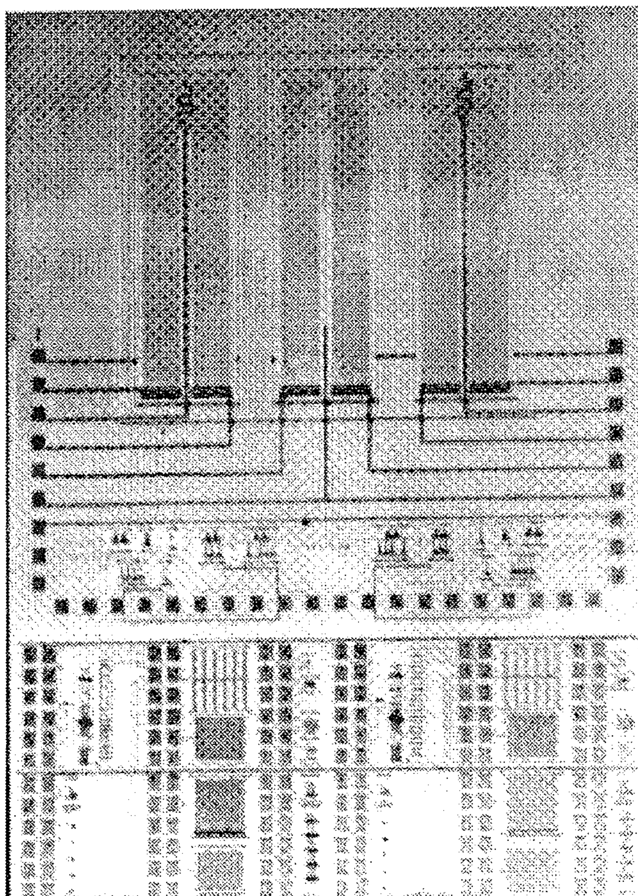


Fig. 7: Microphotograph of an ISFET-CMOS chip fabricated at IRST.

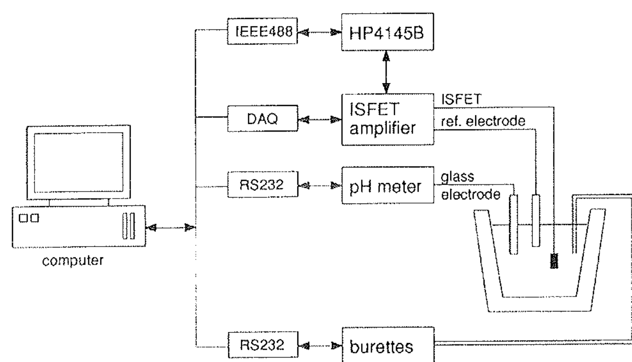


Fig. 8: Computer-controlled sytem for ISFET electrochemical characterization.

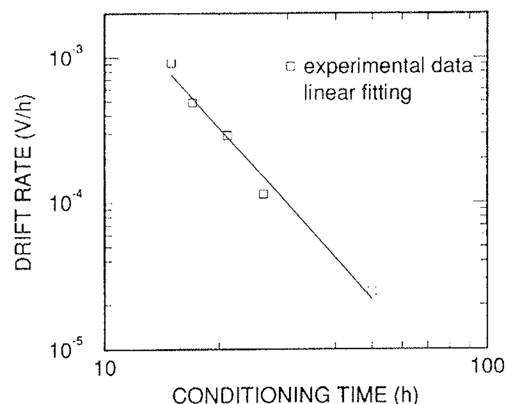


Fig. 9: Drift rate as a function of conditioning time (pH=7).

Complete electro-chemical characterization of the ISFET sensors has been performed by employing a computer-controlled test system (similar to that reported in /16/), allowing several devices to be tested in parallel in a calibrated solution whose pH and temperature are automatically controlled. A block diagram of the measurement set-up is shown in Fig. 8. The test solution is contained in a water-jacketed titration vessel, in which the temperature is maintained at 25°C. The pH is moni-

tored with a pH meter (CRISON 2002), while an Ag/AgCl electrode is used to provide the reference voltage for ISFET operation. Addition of acids and bases is carried out by means of two micro-burettes (CRISON 2031). The ISFET is connected to a feedback amplifier, shown in Fig. 2, allowing V_{DS} and I_{DS} to be set simultaneously by adjusting the gate voltage. This latter is measured by means of a data acquisition board (NI AT-MIO16L). A HP4145B semiconductor parameter analyzer is used to bias the ISFET and to measure currents. The burettes, the pH-meter, the data acquisition board, as well as the HP4145B are interfaced with a personal computer, controlling all the different phases of the characterization procedure. To this purpose, a package of C-language programs has been developed by exploiting the LabWindow 2.0 environment. A typical test sequence includes: (i) encapsulation verification, (ii) measurement of the I_{DS} vs. V_{GS} characteristics; (iii) long-term drift evaluation; (iv) determination of pH sensitivity and hysteresis.

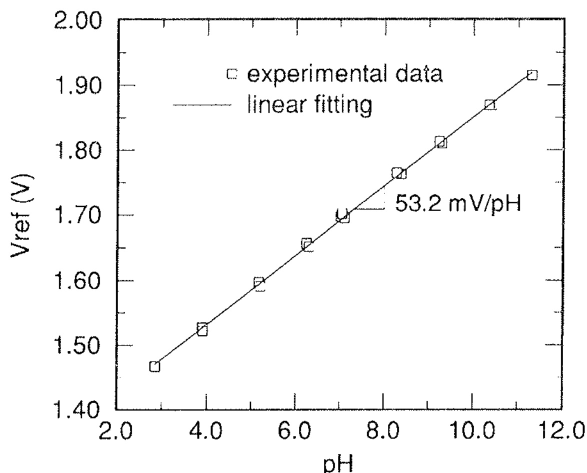


Fig. 10: Gate voltage (V_{ref}) as a function of pH. From the slope of the fitting line a sensitivity of 53.2 mV/pH is extracted

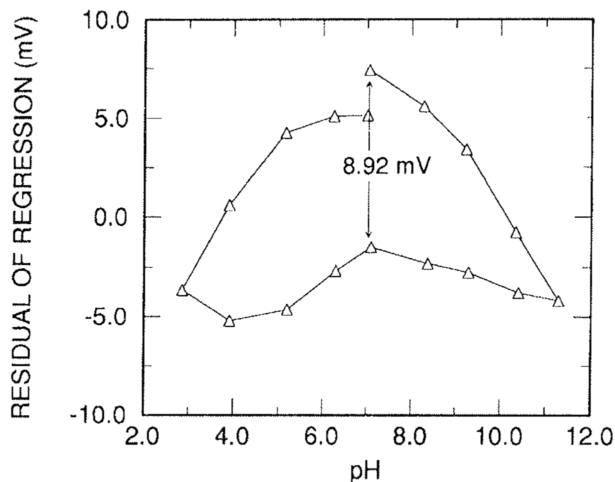


Fig. 11: Residues of the V_{ref} (pH) linear regression as a function of pH.

(i) To check the integrity of ISFET isolation, the leakage current flowing through the encapsulated device is measured, before and after the standard sensor conditioning (15 h at pH=7), by sweeping the reference electrode voltage from -3 to 3 V, while keeping source, drain and bulk terminals to ground /18/. ISFET with good-quality isolation shown leakage currents in the pA range throughout the wide reference-voltage interval adopted, whereas failures in the encapsulation are usually evidenced by exponetially growing leakage currents at voltages above certain threshold voltages. (ii) ISFET transfer characteristics are measured at constant pH (usually pH=7) and different V_{DS} voltages. Typical results are shown in Fig. 5. From the I_{DS} vs. V_{GS} characteristics electrical parameters, such as threshold voltage and transconductance, can easily be extracted. (iii) Drift rate is evaluated by monitoring the feedback-amplifier output, at constant temperature and pH (usually pH=7) for 1 h. ISFET's are immersed in the solution 12 to 50 h before drift measurement is started. In Fig. 9 results are reported, showing that the drift rate decreases markedly with time, reaching values comparable with the experimental error after conditioning times of 30÷40 h. (iv) Sensitivity and hysteresis are measured by changing the solution pH and monitoring the sensor output voltage. The electrolyte solution used is tipically a 0.1 M NaCl with low-concentraton buffers included to stabilize the pH reading. pH excursion begins at pH=7, where the ISFET is allowed to stabilize before the measurement starts. The pH is changed in steps of one unit down to 3, then stepped upwards to 7. After that, the sequence is repeated towards the basic extreme, which is usually pH=11. The time spent for each step is 6 min, the measurement of the output voltage being taken 4 min after each acid or base addition. Figure 10 and 11 show typical results of this experiment. V_{ref} is plotted against pH in Fig. 10, where the slope of the linear-regression line provide a pH sensitivity of 53.2 mV/pH. In Fig. 11, the residue of the linear regression is reported as a function of pH. The maximum amplitude of the hysteresis curve is measured at pH=7, yielding a value of 8.93 mV. Typical values of the different electrochemical parameters characterizing ISFET's fabricated at irst are summarized in Table 2.

Table II: Typical values of the main electrochemical parameters characterizing ISFET's fabricated at IRST.

PARAMETER	VALUE
sensitivity	51.0±1.3 mV/pH
hysteresis (3<ph<11)	11 ± 3 mV
linearity	0.9995
drift (after 50 h)	<500 μV/h

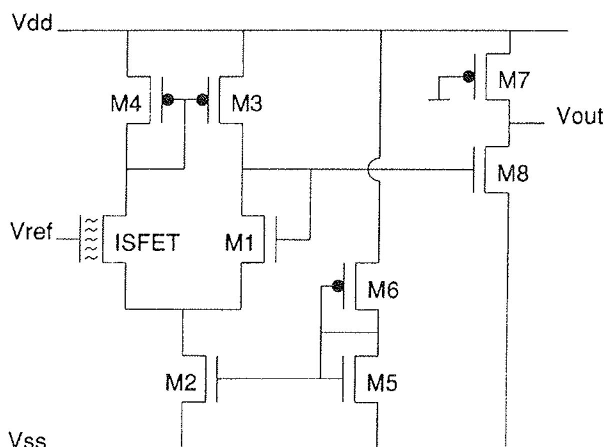


Fig. 12: Schematic of a differential stage with an ISFET as one of the input transistor and a CMOS output stage.

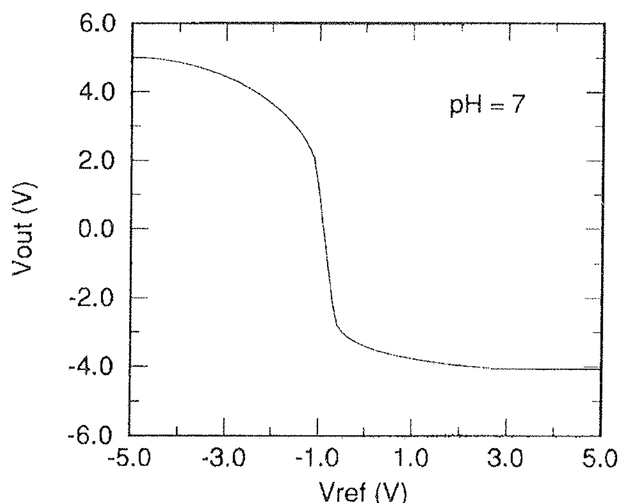


Fig. 13: Experimental transfer characteristic of the circuit in Fig. 12.

The functionality of all the circuit blocks present on the test chip has been verified both at wafer level and in packaged devices. As an example of testing in operating conditions, the transfer characteristic of a differential stage having an ISFET as one of the input transistors and a CMOS output stage is shown in Fig. 13. The schematic of the circuit is given in Fig. 12.

4. ION SELECTIVITY AND PACKAGING

In this section, the use of ISFET's to develop complete (bio)chemical sensors is discussed and the main technological drawbacks to overcome in order to fully exploit commercially the potentialities of ISFET's are reviewed. The everlasting problem of an efficient, reliable, low cost packaging procedure is then outlined.

4.1 DIRECTLY AND INDIRECTLY SENSING DEVICES

As stated previously, ISFET in its simplest form operates as a pH sensor, where its threshold-voltage shift depends upon the concentration of hydrogen ions in the electrolyte. The use of Si_3N_4 or Al_2O_3 or Ta_2O_5 as pH-sensitive insulator allows an almost linear response to be achieved. Selectivity can be provided by a semipermeable membrane covering the device. The use of different types of ion-selective polimeric membranes deposited on top of the gate insulator has led to the application of ISFET to detect other cations, such as Na^+ and K^+. The first report on ISFET covered with such membrane was published in 1975 /19/, when a potassium-sensitive ISFET was fabricated by covering the ISFET with a 300-μm thick plasticized PVC membrane. Following this first achievement, a variety of membrane covered ISFET's sensitive to calcium, sodium, ammonium, and other cations have been published. Moreover, the use of biological membranes such as enzimes has resulted in biosensors. Main problem with such approach to a specific chemical sensitivity is the membrane limited lifetime, mainly due to leaching of components and bad adhesion. To prevent leaching, membranes that are intrinsically rubbery, e.g. polysiloxanes, or photopolymerizable ion-selective membranes, e.g. methacrylate-type polimers, have been suggested and used. This latter approach might be suitable to mass production. However, to our knowledge, no successful on-wafer fabrication to produce low cost, highly reliable membrane covered ISFET's has so far been reported. To improve adhesion, a number of technological solutions have been proposed and tested. Since all the ion-sensitive membranes so far used are applied to the gate after encapsulation, membrane adhesion problems are closely related to ISFET packaging technology.

pH-sensitive ISFET's, as well as membrane-covered ISFET's, can be considered "directly sensing devices", since they directly provide a voltage output shift related to the specific ion concentration in the electrolytic solution. However, the practical application of ISFET's is not limited to the detection of ionic species only. It is also possible, in fact, to add an intermediate layer to the system to transduce, by a suitable auxiliary chemical reaction, a variation in a (bio)chemical variable into a corresponding variation of ionic species resulting from the auxiliary reaction, which can be directly sensed and measured. This is the way ISFET-based "indirectly sensing devices" operate. PCO_2-sensitive ISFET's /20, 21/ and ISFET-based enzime sensors /22/ are particularly relevant examples of such indirectly sensing approach. Also in these cases the use of an ISFET as the detecting element in a more complex chemical sensor is particularly attractive because of its small size and of the possibility to couple its ion-sensitive gate region to miniaturized flow-through chambers. Biomedical devices for extra-corporeal use often require flow-through chambers with a minimum internal volume, which allows for a small sample size and a fast response. Such structures can be recalibrated easily and regularly, thus solving the ISFET drift problem. The potential low cost of mass produced ISFET's is also of interest in the

development of biosensors, because the limited lifetime of biologically active intermediate sensing layers requires the use of cheap disposable sensors.

4.2 ENCAPSULATION AND PACKAGING

No sensor can be used in measurements without proper packaging. In fact, packaging should be considered as an integral part of the sensor design process. There is no unique and generally applicable packaging method for all the ISFET-based biochemical sensors. Each device works in a special environment and will have unique operational specifications. The packaging therefore will have to be designed to satisfy these conditions. Additional problems are encountered when ion-selective membranes are deposited on top of the ISFET transducer, i.e. the fixation of these membranes to the sensor and their compatibility with the packaging materials. Packaging should asssure: (i) electrical isolation of leads, sensor chip and electronics to prevent leakage; (ii) mechanical, optical and thermal protection to ensure structural integrity, dimensional stability and photo- or thermally-generated spurious signals; (iii) chemical isolation from the harsh external environment and, especially in case of biosensors, biocompatibility. Encapsulation materials interfacing with the environment should be inert and should not release toxic products during the sensing operation. It is evident that the final application of the sensor determines the packaging technology to be used. In this respect, the different approach in packaging methodology between disposable-type sensors (i.e. one-time use during relatively short time periods, with low price) and reusable sensors (i.e. repeatedly used, long time periods, higher price) has to be underlined.

With respect to the design and the development of ISFET-based biochemical sensors, the encapsulation and packaging remain an often underestimated aspect. Especially with the recently developed micromachining methods, totally new device realizations are conceivable, which offer improved long-term performance of the sensor. Also, a miniaturized reference electrode, which remains a necessary part of every electrochemical system, can possibly be integrated on chip with these techniques. Micromachining methods may also set the trend for future developments in miniaturized ion-sensor systems as, by using these techniques, complete biochemical analyzer systems based on arrays of specialized ISFET sensors integrated on a single chip can be envisaged.

5. APPLICATION EXAMPLES

The marketing opportunities of ISFET-based (bio)chemical sensors are first outlined. Then, two examples of systems recently developed at IRST for environmental applications are described.

5.1 MARKET PERSPECTIVES

Although the ISFET concept has existed for over 20 years, i.e. since the pioneering work of Bergveld in 1970 /1/, practical applications are still emerging only very slowly, in spite of the large research and development effort in the field. Two classes of practical problems have been and, at least partially still are, limiting factors in the commercial breakthrough and exploitation of biochemical sensors based on ISFET transducers: those which are inherent to the transducer itself, arising from limitations in materials and technologies used, and those which are common to the applications of any solid-state (micro)sensor, i.e. the need for an efficient encapsulation and packaging procedure, as stated previously, and the need for a stable, on chip micro-fabricated reference electrode.

Two application areas particularly suited for ISFET-based biochemical sensors that are becoming increasily important are the environmental monitoring and medical diagnosys. Both of these applications require quite sofisticated sensor systems and data processing methods. World-wide market for the various type of (bio)chemical sensors in these two fields was estimated to be 100 million US$ in 1990, with a predicted value of 700 to 800 million US$ for the year 2000. This market value forecast justifies the continuing research and development effort in the field. In the following, two different systems are described, aimed at the detection of microorganisms in water and of formaldehyde in air, respectively. Both systems exploit ISFET's as sensing elements. Full account of design, implementation, and testing of the two systems can be found /23/ and /24/, respectively.

5.2 ON-LINE DETECTION OF MICRO-ORGANISMS IN WATER

The system described in the following allows for the detection of living microorganisms by measuring the cell-induced acidification rate in micro-samples of water periodically drawn from the main stream under observation and conveyed to an especially-designed flow-through microchamber. This latter is encapsulated on top of the transducer chip. A sketch of the system block diagram is shown in Fig. 14. The fabrication technology and the layout of the sensor chip have already been described in Sec. 3.1 and 3.3, respectively. A Si_3N_4-ISFET and an Al-gate MOSFET form the input pair of a differential stage, followed by a CMOS output stage (see Fig. 12).

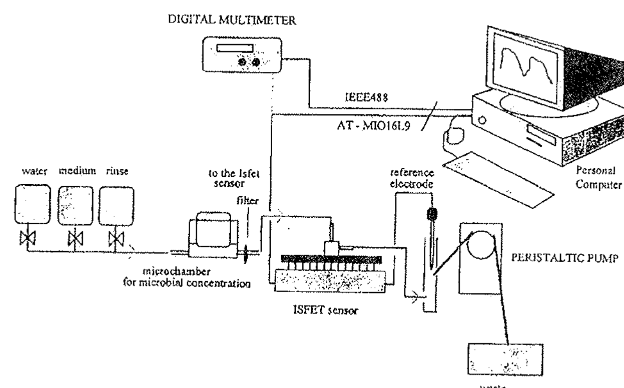


Fig. 14: Block diagram of the system for on-line detection of microorganisms in water.

The effectiveness of the system has been tested by means of two different experiments. In the first one, the system is fed with an F12 solution with known concentrations of bacteria (10^5 ml^{-1}, 10^6 ml^{-1}, 10^7 ml^{-1}). In the second, the system is fed with a sterile F12 solution, whereas the bacteria have previously been inserted into the syringe filter at the same different concentrations. The first experiment represents the simulation of an on-field measurement, the bacteria being contained in the flowing medium and accumulating in the filter during the measurement. In these conditions, the concentration of bacteria is fixed in the medium, while increasing in the filter. In the second experiment, which can be used to evaluate the system sensitivity, the microbial concentration inside the filter is constant. In both cases, the duration of the test is 60 min, the flow rate is 0.2 ml/min with an ON/OFF duty cycle of 10min/5min. Results from the first experiment are shown in Fig. 15 for different microbial concentrations. An increase in the total acidification detected by the system can clearly be observed. This is due to the fact that the total amount of bacteria inside the filter grows proportionally to the flow time. Figure 16 illustrates the results of the second experiment. As can be seen, the Δ pH is constant with time for microbial concentration of 10^5 ml^{-1} and 10^6 ml^{-1}, due to the fixed bacteria concentration inside the filter. At the microbial concentration of 10^7 ml^{-1}, the unexpected acidification change is probably related to variations in the metabolic state of the microorganism population.

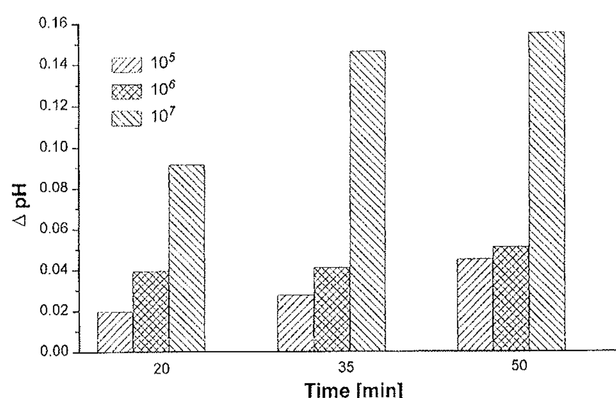


Fig. 15: pH variations for different microbial concentrations obtained in the first experiment.

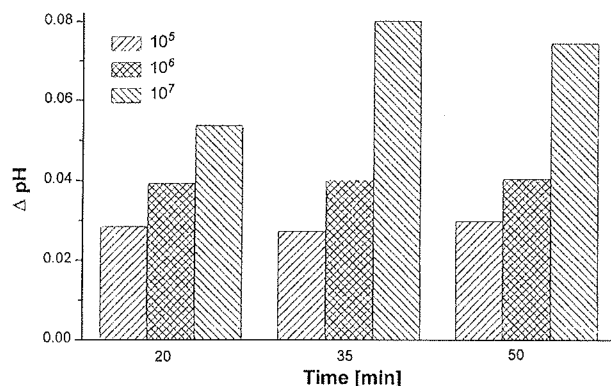


Fig. 16: pH variations for different microbial concentrations obtained in the second experiment.

5.3 POTENTIOMETRIC SAMPLING OF FORMALDEHYDE IN AIR

Formaldehyde, a suspected carcinom, is an automotive exhaust gas and an important chemical in the manufacturing of a variety of consumer products and in performance of medical services. Since conventional methods for the determination of formaldehyde (i.e., spectrophotometry, chromatography, or polarography) require expensive and bulky instrumentation with high power demand and well trained operators, a widespread observation of formaldehyde is prevented. In this context, the development of a portable, low-cost sensor for real-time monitoring of this gas-phase pollutant appears of large interest. In the following, a system for monitoring atmospheric formaldehyde is described, which exploits an ISFET in conjunction with an enzyme specific for this pollutant, namely formaldehyde dehydrogenase from *Pseudomonas putida* (FDDP). This enzyme, using oxidised nicotinamide adenine dinucleotide (NAD^+) as cofactor, catalyzes the oxidation of a molecule of formaldehyde with the parallel production of two protons which can be sensed by the ISFET.

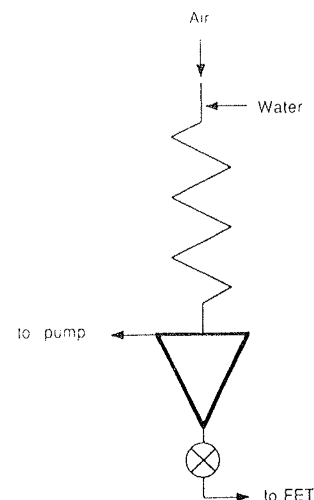


Fig. 17: Block diagram of the system for detection of formaldehyde in air.

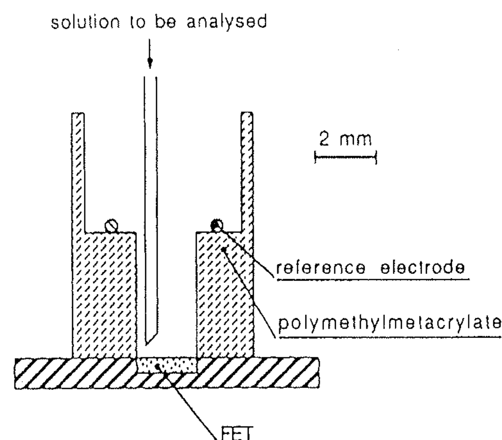


Fig. 18: Measurement cell containing the ISFET transducer.

The scheme of the sampling system is shown in Fig. 17. Formaldehyde is stripped from the atmosphere by pulling it concurrently with the scrubbing solution into a vertical coil. The scrubbing solution flows through the coil at the rate of 100÷200 μl/min, while the air is tipically sampled at 0.5÷1 l/min by a μP controller. The cell, a sketch of which is shown in Fig. 18, permits working volumes as low as 50 μl to be used and the analysing sample to be automatically replaced. The ISFET, whose fabrication technology and main electrochemical characteristics have already been described in Sec. 3.1 and 3.3, respectively, is operated with I_{DS}=100 μA, V_{DS}=300 mV, by means of a low-noise feedback amplifier, while the gate voltage is recored on an X-t chart recorder. ISFET active surface is covered by a membrane prepared by addition of glutaraldehyde (10 mg/l) to a solution of bovine serum albumin (40 mg/l), or by deposition of a solution of γ-aminoethyltriethoxysilane (22% in ethanol) followed by spin-off. FDDP is then covalently immobilized on the surface of the formed membrane by addition of N-(3-dimethylaminopropyl)-N'-ethylcarbodiimide hydrochloride, or alternatively added directly to the sampled solution. To improve detection limit and signal stability, a sodium pyrophosphate buffer in the concentration range 0.5÷2 mM is adopted.

As an example of system response, Fig. 19 shows the output of the ISFET transducer versus formaldehyde concentration. As can be seen, a linear response is measured up to 200 μM of formaldehyde. This behavior, which can appear in contrast with the Nernst law (according to which the response of the ISFET is proportional to the logarithm of the proton concentration), is a consequence of using a buffer at starting pH values close to the pK_a of the buffer itself /24/. A detection limit of 10 μM of formaldehyde in acqueous solution was estimated, corresponding, thanks to the enrichment factor introduced by the sampling system, to an athmospehric concentration in the ppb range.

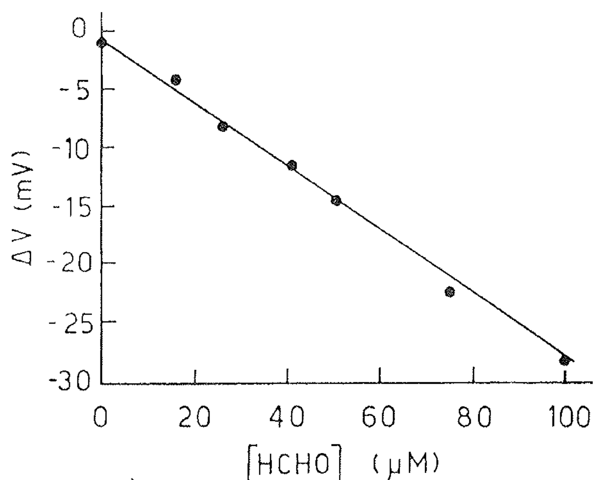


Fig. 19: Potentiometric response to increasing concentration of formaldehyde in the presence of FDDP.

6. CONCLUSIONS

The increasingly important and rapidly developing field of ISFET-based silicon integrated biochemical sensors has been addressed in this paper. ISFET basic operating principles, modelling and electrochemical characterization techniques have been reviewed. ISFET fabrication technology, mainly with reference to the ISFET-CMOS process developed at IRST, has been described. Finally, two examples of ISFET-based biochemical sensors for environmental monitoring applications have been presented.

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TECHNOLOGICAL CHALLENGES FOR SILICON TECHNOLOGIES

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Key words: microelectronics, semiconductors, silicon technologies, technological challenges, CMOS technologies, optimization of technologies, future trends, BICMOS technologies, fabrication processes, FA, Furnace Annealing, RTA, Rapid Thermal Annealing, 0.5 micrometer technologies, 0.07 micrometer technologies, Si-Ge technologies, HBT, Heterojunction Bipolar Transistors, low power technologies, CCD-CMOS technologies, NVM, Non volatile memories, Flash EEPROM memories, LV, low voltages, SOI technologies, Silicon-On-Insulator technologies, DUV lithography, Deep UltraViolet lithography, EUV lithography, Extreme UltraViolet lithography, SOG, Spin-On-Glass, TLM technology, Three Layers of Metal, 5LM, 5 layers of Metal, CMP technology, Chemical-Mechanical Polishing technology

Abstract: An overview is given of the present status and future requirements in association with the increasing functionality added to the core CMOS-based technologies, such as e.g. mixed signal, bipolar, low voltage, non volatile memories, low power and smart technologies. The stringent impact on the optimisation of different technological modules is illustrated. Future trends related to process modules such as optical lithography, isolation schemes, interconnects and metallization schemes are outlined. To some extent restrictions imposed by device physics and reliability aspects have to be taken into account.

Tehnološki izzivi za tehnologije na siliciju

Ključne besede: mikroelektronika, polprevodniki, Si tehnologije silicijeve, problemi tehnološki, CMOS tehnologije, optimiranje tehnologij, trendi prihodnji, BICMOS tehnologije, procesi proizvodni, FA žganje v peči, RTA žganje hitro termično, tehnologije 0,5 mikrometer, tehnologije 0,07 mikrometer, Si-Ge tehnologije, HBT transistorji bipolarni heterospojni, tehnologije moči majhnih, CCD-CMOS tehnologije, NVM pomnilniki neizbrisljivi, Flash EEPROM, LV napetosti nizke, SOI tehnologije silicij-na-izolantu, DUV itografija ultravijolična globoka, EUV litografija ultravijolična ekstremna, SOG steklo tekoče naneseno centrifugalno, TLM tehnologija treh plasti kovinskih, 5LM tehnologija 5 plasti kovinskih, CMP tehnologija poliranja kemijsko-mehanskega

Povzetek: V prispevku je podano trenutno stanje in nove zahteve za tehnologije na siliciju, predvsem s stališča povečane funkcionalnosti, oz. zahtev v smislu obdelave mešanih signalov, nizke delovne napetosti, nizke moči in realizacije pametnih funkcij. Prikazano je tudi, kako te zahteve nujno prizadenejo in vplivajo na optimizacijo različnih tehnoloških modulov. Predstavljene so bodoče zahteve glede posameznih procesnih modulov, kot so optična litografija, načini izolacije ter povezovalne in metalizacijske tehnike. Do neke mere moramo upoštevat tudii notranje omejitve, ki nam jih postavljata zanesljivost in fizika polprevodnikov.

1. INTRODUCTION

The "VLSI revolution" has made the microelectronics industry to become one of the largest industries with respect to turn-over and employment opportunities, and has surely a strong impact on many aspects of our social life. The microelectronics revolution is clearly visible in areas such as defence, telecommunication, computers, software services, robotics, medical electronics, consumer applications, instrumentation, industrial electronics, automotive applications... The high expectations in multimedia linked to the electronic highway surely rely on the availability of integrated circuits with high packing density levels and improved speed performances. Handheld, ultralow power electronics will have a strong impact on the the future way people work, play and life together.

Device scaling continues, with a 0.12 μm technology expected in 2004. Every 3 years a new device generation brings 25% more processing steps, 38% larger chips size, a 35% increase in cost of ultra clean materials and a 20% increase in test cost /1/. The technology driver towards higher transistor densities and improved performances is nowadays surely CMOS for memory applications such as SRAMs and DRAMs, while microprocessor requirements push the interconnect technology and routing schemes to high packing density and complex multi level metal processing. The overall trends of the core digital technology for memory applications and mpu's is well known and is schematically illustrated in Fig. 1. In general, the scaling trends are following Moore's law, i.e. the average lifetime for a technology generation is about three years and for every new generation the memory density increases by four. By the end of the century, 0.25 and 0.18 μm technologies will be the standard for volume production of 1 G memories, notwithstanding the extremely high costs to introduce a new technology generation. These deep submicron technologies are requiring advanced processing modules such as e.g. deep UV optical lithography, improved isolation schemes, appropriate metallisation and interconnect schemes for allowing 4 to 5 metal layers, and optimised device engineering concepts to improve the device reliability /2/. The roadmap for some DRAM parameters in shown in Table I.

Table I: Roadmap for some DRAM parameters.

	1 Mb	4 Mb	16 Mb	64 Mb	256 Mb	1 Gb	4 Gb
Year	1987	1990	1993	1996	1998	2001	2004
L (μm)	1.0	0.7	0.5	0.35	0.25	0.18	0.13
Levels	11	14	18	21	21	23	23
Gate (nm)	20	15	12	10	7	5-4	5-4
Steps	200	300	400	500	550	600	600
Junct. (μm)	0.25	0.2	0.15	0.1	0.07	0.05	0.03
access (ns)	50-80	70	50-80	50	40	?	?
wafer (mm)	125	150	150	200	200/300	300	300

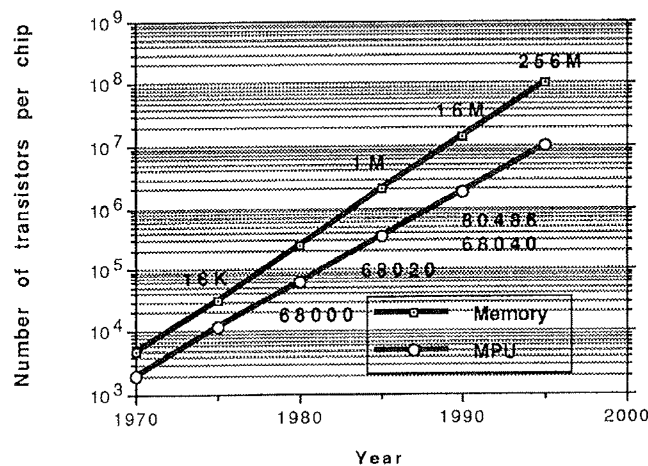


Fig. 1: The change in number of transistors per chip for DRAM and MPU's.

The microelectronics market is not only a digital one, so that beside the trends towards 0.25 and 0.18 μm minimum feature sizes, much attention is also given to an increase of the functionality of a technology. This implies that while a digital technology is taken into production, efforts are devoted towards the development of additional functions such as e.g. analogue building blocs, CCD-CMOS, low voltage, low power, higher frequencies and low noise performance. The added functionality to the core digital process necessitates the availability of dedicated processing modules. This paper reviews first some general trends related to an increased functionality, before discussing future technological challenges in order to keep up with the overall scaling trend. The latter will be illustrated by briefly reviewing the optical lithography, the device isolation, and the interconenct and metallization processing modules.

2. FUNCTIONALITY OF Si TECHNOLOGIES

This section reviews some key aspects related to increasing the functionality of core digital technologies. Attention will be given to BICMOS technologies, the potential of a Si-Ge technology, low power applications, CCD-CMOS, non volatile memories and SOI-CMOS.

2.1 BICMOS

The increased demand for functionality has given a push for the development of analog-digital (mixed mode) and BICMOS technologies. In the past analog-digital technologies came around one year later in production than the pure digital process, while at the moment often a company which has an important market share in mixed mode products tries to have the analog-digital process as fast as possible, meaning at the same time as the digital technology. A modular technology concept facilitates the implementation of additional processing modules.

However, the last few years more and more emphasis has been put on developing technologies with more and different functionality compared to the standard digital and analog-digital technologies. The extension of a CMOS technology with bipolar transistors in order to get an increased speed at an acceptable increase of cost,

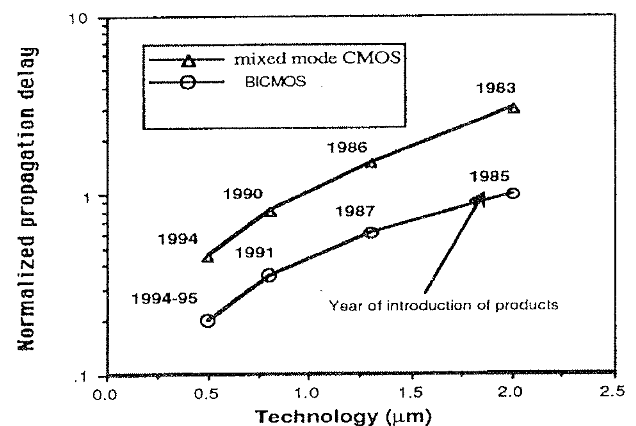


Fig. 2: The normalised propagation delay versus the minimum feature size for mixed mode CMOS and BICMOS technologies respectively /3/.

becomes more and more popular. As shown in Fig. 2 the introduction of a BICMOS technology was 1 to 2 years behind the availability of analog-digital processes with the same minimum feature size. At the moment the difference in time for introducing these technologies is almost negligible. However, when introducing additional functionality there is always an increase in cost. Furthermore the implementation of bipolar transistors in CMOS results in less performant bipolar devices than when they are fabricated in a pure bipolar technology. Different trade off' s for CMOS and BICMOS technologies are summarised in Table II.

Table II: Trade off's between key features in different technologies. The + means the best score and the - means the lowest score.

	Bipolar	CMOS	BICMOS
Speed	+	-	+
Power consumption	-	+	+/-
Packing density	-	+	+/-
Analog features	+	-	+
Driving capability	+	-	+
Complexity	+	+	-
Cost	+	+	-

For high frequency analogue applications the transistor 1/f noise is an important parameter. It has been demonstrated (see e.g. /4/) that for a polysilicon emitter technology, the interfacial oxide thickness and the amount of oxide break-up not only has an impact on the DC parameters, but also strongly influence the low frequency noise performance. To obtain a general picture on the noise behaviour, i.e. to develop fundamental noise models, one has to take into account both technological (pre-cleaning, polysilicon deposition technique, furnace or RTA anneal) and operating (low or high current regime) conditions. The device fabrication process has to be optimised in such a way that the improved noise performance has no degrading impact on the current gain. Recently, a clear relationship between both parameters has been observed as illustrated in Fig. 3. Process splits with both furnace anneal (FA) and rapid thermal anneal (RTA), and with different interfacial oxide layers, have been used to evaluate devices processed in a 0.5 μm technology /5/.

2.2 SiGe Technologies

Another technological approach to achieve high speed performance circuits is to use a SiGe technology. Although the first reports on these Hetero-junction Bipolar Transistors (HBT) became available in 1986, SiGe devices are not found in production yet. The material aspects of growing the required compound layers with a minimum of lattice strain (too high strain will lead to the generation of interface dislocations) is nowadays well under control. The lattice mismatch, which depends on the Ge concentration and the layer thickness, can be engineered by adding small amounts of carbon. According to Vengard's law a Ge to C ratio of 9:1 would allow a perfect match with the silicon lattice. The pioneering SiGe material and device work has surely been done at IBM and very promising results have been achieved by Daimler-Benz, Analog Devices and NEC. A cross-sectional illustration of an advanced self-aligned SiGe technology is given in Fig. 4. Each hetero-junction transistor is isolated by 1 μm wide trenches etched 4 to 5 μm deep in the silicon and refilled with polysilicon and oxide. Heavily n^+ and p^+ polysilicon layers form the contacts to the emitter and base regions. The contacts are filled with tungsten and a standard Al/Cu metallisation scheme is used.

The driving application for SiGe devices is RF wireless communication, although there is a strong competition in the field from both Si and GaAs devices. At the 1995 IEDM meeting several devices with a f_T around 30 GHz have been reported. The real breakthrough of the Si-Ge

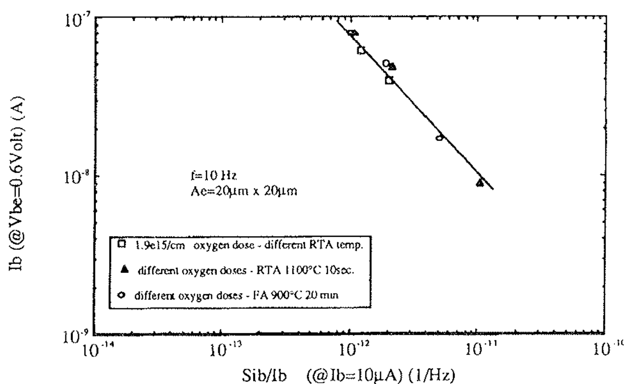


Fig. 3: Experimental relationship between the normalised base current noise spectral density (at I_B = 10 μA and f = 10 Hz) and the base current I_B (at V_{BE} = 0.6 V) /4/.

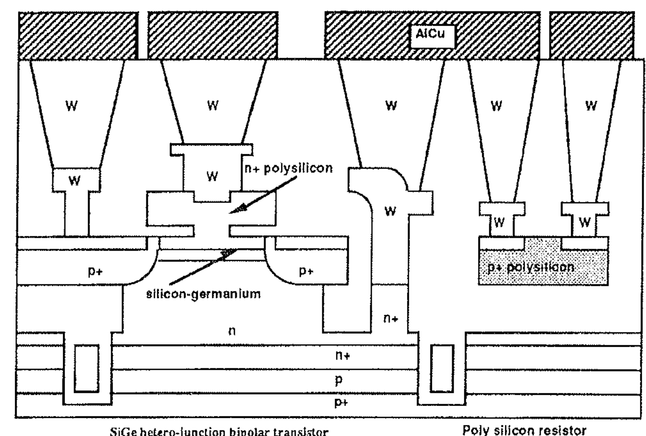


Fig. 4: Schematic illustration of an advanced SiGe circuit, after Cressler /6/.

technology will strongly depend on cost and manufacturing related issues instead of on performance, as the overall goal is to meet the performance specifications at minimum cost in a reproducible way. The closer the fabrication technology can be matched with standard silicon technology, the cheaper the final product will be. Also for some optoelectronic applications SiGe based technologies have a strong potential. A recent review on Si-Ge based materials and devices can be found in /7/. It should finally be mentioned that SiGe HBTs are very promising for cryogenic applications /8/ and have recently been demonstrated to be radiation hard up to 1 Mrad total dose levels /9/.

2.3 Low Power

The increased use of battery-operated products such as portable computers, cordless telephones, pocket calculators, pagers ... has strongly triggered the interest in low power technologies /10/. The power consumption can be restricted by lowering the supply voltage and limiting the load capacitance. However, a figure of merit of the circuit performance is given by the power-delay product. In order for CMOS circuits to compensate for the reduction of the speed performance by lowering the supply voltage, one has to lower the threshold voltage. A typical trade-off between delay time and supply voltage is illustrated in Fig. 5 for different technologies. However, a lower threshold voltage is also making the circuit more vulnerable to threshold voltage fluctuations caused by variations in the fabrication process and short-channel effects. It is therefore necessary either to change some technology steps resulting in higher speeds for the same dimensions, as is the strategy for low power/low voltage CMOS technologies, or to introduce new types of design gates as is more used in low power/ low voltage BICMOS processes. In CMOS the effective channel length, the series resistances, the gate oxide thickness and all the parasitics are reduced as much as possible when reducing the supply voltage from 3.3 V to 1 V. However, it is much more difficult to obtain the same speed for a 1 V CMOS technology then it is for a standard 3.3 V CMOS technology. The threshold voltage is set by the specification on subthreshold current and the required noise margins. Lower supply voltage means reduced drive current, but the loss can be limited by using small threshold voltages and thin

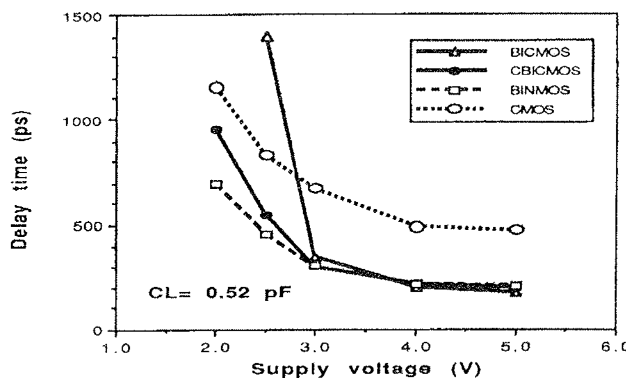


Fig. 5: Delay time versus supply voltage for different CMOS and BICMOS technologies /11/.

gate oxide dielectrics. The loss in speed as a result of reduction in current can be pushed to a minimum by reducing the parasitics like source/drain capacitance, overlap capacitance and routing capacitance and the related resistances. Furthermore a change in design concept is necessary to optimize a low voltage circuit next to technology changes.

The larger increase with decreasing voltage of the delay of standard BICMOS gates has lead to the development of new BICMOS cells like the CBICMOS cell and the BiNMOS cell. These new cells can be used for lower supply voltages. Especially the BINMOS gate is at 1.5 V supply voltage still faster than a loaded standard CMOS inverter gate, while its current drivability is significantly better than that of a CMOS gate. The influence of the supply voltage on the delay time is also illustrated in Fig. 5 for the CMOS and different BICMOS configurations for inverters with an additional capacitive load of 0.52 pF.

2.4 CCD-CMOS

The functionality of digital CMOS processes can be extended by including dedicated processing modules for achieving a CCD-CMOS technology. The CCD technology is superior for imaging applications, while the CMOS part allows the on-chip integration of pre- and/or post-processing functions. In cases where the image quality is less important, e.g. for automated inspection and control applications, the CMOS building blocs also can be used for imaging. In this case either a diode or a transistor cell is used as a pixel. Nowadays there is great interest in CMOS imagers as they can be fabricated at a lower cost compared to the standard CCD devices. Active vision for robotics applications requiring features such as selectable frame rate and integration time, random access of the region of interest, and real-time programmability of the sensor resolution can be achieved by a CMOS technology /12/.

2.5 Non Volatile Memories

An important market segment is taken by circuits based on non-volatile memory (NVM) cells. Although there exists a large variety of cell concepts for realising a floating gate memory structure /13/, the fasted growing market share is taken by the Flash Electrical Erasable PROM (Flash-EEPROM) type devices. Compared to a standard digital CMOS process, this requires the implementation of a second polysilicon layer and the use of very thin oxides. To overcome the major drawback of NVMs which are relying on conventional channel hot electron injection for programming and therefore requiring an external high voltage, a new cell concept called HIMOS, consisting of a split-gate structure and a coupling capacitor has been proposed /14/. In a 1.2 μm and 0.7 μm technologies, 5 V only programming can be achieved in a few microseconds and also the 3.3 V operation has been demonstrated. For further down scaled technologies like 0.5 μm and 0.35 μm the HIMOS cell gives even faster writing speeds. Only minor process modifications are needed for the implementation of the HIMOS cell in a standard digital CMOS technology.

The additional processing steps are the growth of a tunnel oxide, an additional EEPROM drain junction implant and a second polysilicon layer. Based on the diffusion enhanced oxidation rate, the interpoly oxide is grown simultaneously with the gate oxide. For reliability reasons the tunnel oxide has to be of very good quality, limiting the thickness scaling of the tunnel oxide to keep retention within specification. Nitride oxides for tunnel oxide give improved results related to degradion. Much attention is also given to the use of oxynitride (ONO) type of interpoly dielectrics.

Another class of NVM is based on the use of a ferroelectric technology. As ferroelectric layer PZT ($PbZr_xTi_{1-x}O_3$), deposited by either laser ablation or a sol-gel technique, is often used. Although these layers can easily be implemented in a CMOS process flow, there still remain some questions concerning the compatibility and possible contamination risk when processed in a Si fabrication line.

2.6 SOI Technologies

Increased functionality can also be obtained by using a Silicon-on-Insulator technology. Compared to bulk CMOS, a higher speed performance is obtained for the same gate length. Dependent on the application fields, SOI technologies are beneficial for deep submicron /15/, low temperature /16/, low power /17/, radiation-hard, and high temperature operation respectively. The material aspects have originally hampered the breakthrough of SOI technologies for commercial applications, but these have been strongly improved since the availability of SIMOX and wafers bonding (BESOI). In the recent years, a revival of the interest in SOI technologies has been observed. During the last decade several processing modules have been optimised for processing on SOI wafers /18/. Especially for analogue applications, the low frequency noise performance has to be minimised. Recently, an in-depth study of the origin of the different noise sources and their relation to the technological parameters has been published /19/. Furthermore, the lower subthreshold swing for fully depleted SOI devices compared to standard CMOS makes SOI a good candidate for low voltage applications.

2.7 Future Trends

There are also other means to increase the functionality of the circuits by using e.g. smart power, neural network based concepts or the combination of standard CMOS or bipolar processing with micro machining and/or sensor technology. The latter results into integrated microsystems on chip /20-21/. In the coming years these technologies will surely take an important share of the microelectronics market. However, within the restrictions of the present paper they are not addressed.

3. TECHNOLOGICAL CHALLENGES

By the end of the century the core CMOS technology in volume production will have 0.25 μm feature sizes, with 6 nm gate oxides and 0.07 μm junction depths. However some of the more advanced companies will already run 0.18 μm CMOS in production. The process will need more than 20 masking levels and it is expected that more than 5 metal levels will be needed. Therefore it is of crucial importance to develop on time the required advanced processing modules. In order to illustrate the difficulties that this may impose, a few process modules, such as optical lithography, device isolation, and interconnects and metallization schemes will be briefly discussed.

3.1 Optical Lithography

The optical lithography roadmap for submicron technologies is schematically illustrated in Fig. 6. While g-line lithography (436 nm wavelength) was commonly used for a 1 μm technology, i-line lithography (365 nm) was first introduced for 0.7 μm technologies. Nowadays, i-line lithography is the standard for all 0.5 μm processes. Most likely i-line will allow to go down to 0.35 μm and even to 0.30 μm feature sizes in production. Deep UV (DUV) lithography at 248 nm (KrF laser) was first introduced to perform research at the 0.35 μm level and will become the mainstream technology for 0.25 μm technologies /22-23/. It is even expected that 248 nm will be capable to handle 0.18 μm geometries. By further reducing the wavelength to 193 nm (ArF laser), there is a good perspective that optical lithography can be used for volume production of 1 Gb devices. This has also been confirmed by simulations based on Depict 3.0, pointing out that by using a 0.6 numerical aperture (NA) 193 nm DUV exposure tool combined with annular illumination and the use of attenuated phase shifting masks, an acceptable process window can be obtained for 0.12 μm geometries /23/. The main difficulty for optical lithography is to obtain the required resolution with a sufficient depth of focus. Also the presence of underlying topography leads for standard lithography to large problems when scaling down the geometries to values smaller than 0.5 μm. Beyond 193 nm the roadmap is less clear and several possible alternatives are being mentioned, i.e. proximity x-ray, extreme UV at 13 nm (EUV), the exploration of new wavelengths like 126 nm and 157 nm, and ion projection /24/.

On the stepper side it is possible to optimise the numerical aperture of the lens and to reduce the wavelength of the excimer laser. On the processing side, one can work with improved resist schemes or one can use more advanced processing sequences, like the use of top

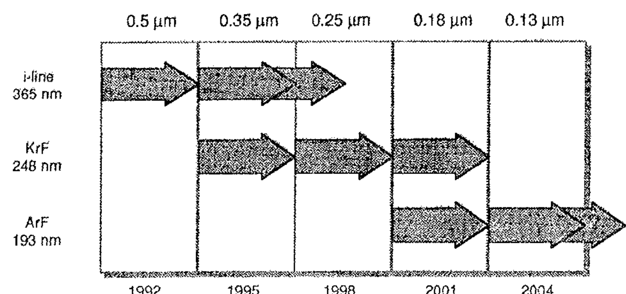
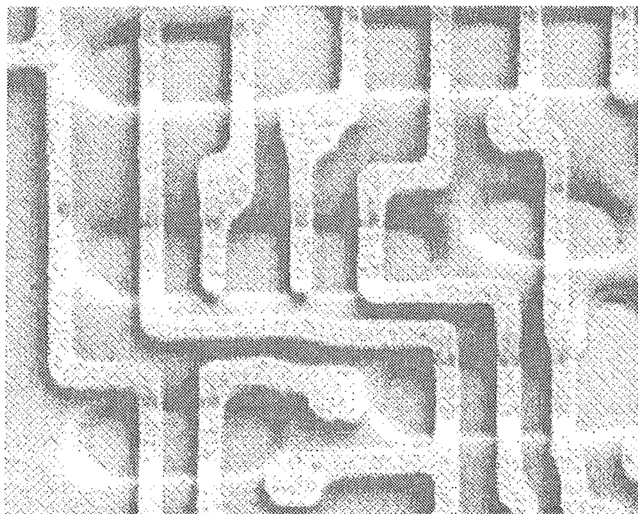


Fig. 6: Roadmap for optical lithography.

and bottom anti-reflective coatings. For the moment, extensive research is on-going related to various resolution enhancement techniques such as respectively multilayer resist schemes, surface imaging techniques (e.g. DESIRE process), off-axis illumination, and the use of phase shifting masks. A recent review on these topics has been published by Van den hove and Ronse /23/. The strong potential for optical lithography is illustrated by the SEM pictures shown in Fig. 7.

Beside the technically feasible solutions, a key factor remains the capital investment and the processing costs. With predicted price tags above $5 million for a DUV stepper and taking into account the associated processing cost, raw calculations point out that about 50% of the wafer fabrication cost is due to patterning. Therefore, in industry preference will be given to an evolutionary approach instead of switching over to a more revolutionary strategy. Mix and match approaches with DUV steppers for the critical layers and i-line for non critical ones will allow 0.18 μm technologies in production. Much attention is also given to the step-and-repeat DUV scanners. Although x-ray lithography /25/ has already been used for 0.5 Mb test memories in a 0.35 μm technology /26/, its breakthrough will only occur when the limits of optical lithography are reached (sub -0.15 μm feature sizes?) due to the high capital investment.



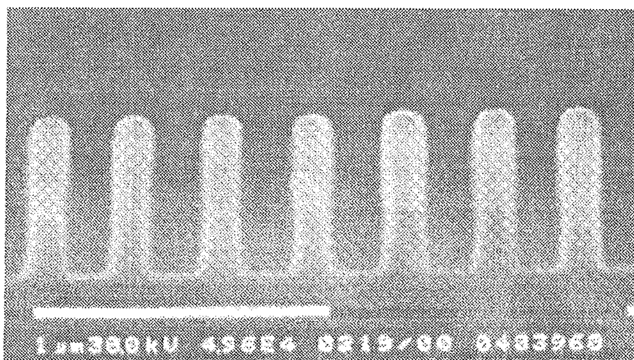


Fig. 7: SEM pictures illustrating the strong potential of optical lithography for deep submicron technologies. (a) 0.25 μm shift register and (b) 0.15 μm line and spacings

Initial results on mixed x-ray and optical lithography have recently been reported for 0.15 μm effective gate length devices /27/.

3.2 Device Isolation

From a technological viewpoint, the down scaling of device geometries is strongly associated with the capability of using an appropriate isolation scheme. For MOS technologies, local oxidation of silicon (LOCOS) has been used as the workhorse isolation technology over the past 25 years /28/. Different alternative approaches have in 1992 been reviewed by Wolf /29/. In general, the optimisation of a LOCOS technique is done by optimising the pad oxide and nitride thickness, the overall thermal budget and/or implementing additional layers in order to reduce the associated stress levels. To optimise an isolation scheme, important features such as the bird's beak length, the overall topography, the generation of bulk defects, gate oxide thinning phenomena, field oxide thinning or thickening, and the electrical device performance (leakage current, gate oxide integrity, overlap capacitance ....) have to be taken into account. In the early 90's it was expected that trench isolation would be needed for submicron technologies. However, the processing difficulties associated with this technique and the progress made in optimising the standard LOCOS technique have strongly hampered its breakthrough. For 0.5 μm technologies, advanced LOCOS techniques are commonly used. Good results are obtained with the polysilicon buffered LOCOS (PBL), while a further improvement by replacing the polysilicon layer in a PBL approach by an amorphous silicon layer as a strong potential to become production worthy for a 0.35 μm technology /30/.

For 0.25 μm technologies a promising approach is the Polysilicon Encapsulated LOCOS (PELOX), first introduced in 1993 by Roth et al. /31/ but further fine-tuned more recently /32/. The scaled-down PELOX is using, similar to LOCOS, a SiO_2-Si_3N_4 stack. However, after patterning the stack and the resist strip, a HF solution is used to undercut the nitride layer and to create a 50 nm deep cavity into the pad oxide. Subsequently the wafers are reoxidised and a 20 nm thick amorphous silicon layer is deposited. During field oxidation the diffusion process is retarded in the filled cavity region, thereby limiting the lateral encroachment and the associated bird's beak formation.

The potential of this PELOX technique is illustrated in Fig. 8, showing a cross section SEM image for 0.2, 0.25 and 0.3 μm wide isolated active area regions respectively. Even for the 0.2 μm wide active regions, the oxide growth under the nitride layer is limited and no pronounced bird's beak is formed /33/. A good control of the recess depth into the silicon, resulting from the dry etching of the active regions, is required for reducing the bird's beak length /34/.

The electrical device performance also depends on the defect formation in the silicon substrate, which is closely related with the associated stress levels in the substrate near the bird's beak. Therefore, stress modelling is becoming essential for the development and optimisa-

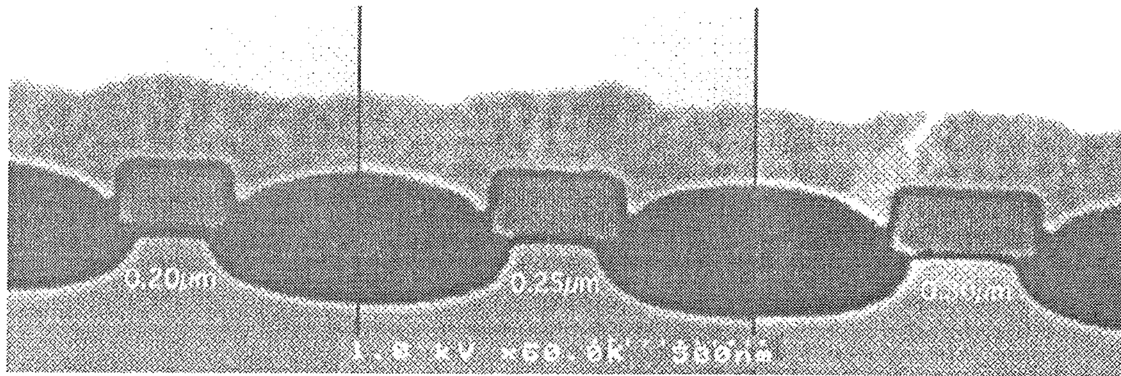


Fig. 8: Cross sectional SEM picture showing 0.2, 0.25 and 0.3 μm wide active regions fabricated with polysilicon encapsulated LOCOS /32/.

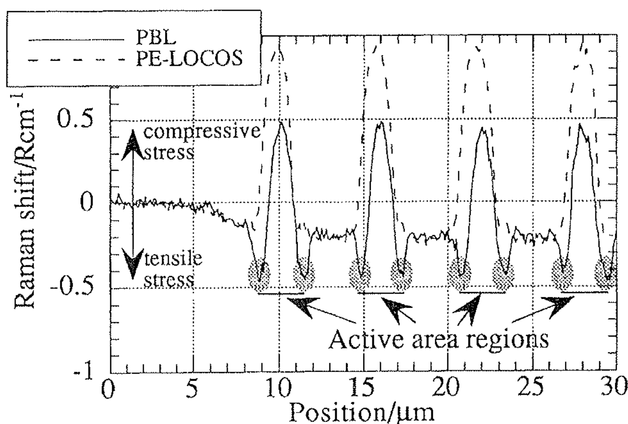


Fig. 9: Illustration of Micro-Raman Spectroscopy to study the difference in stress distribution between PBL and PELOX isolation /32/. A positive Raman shift corresponds with a compressive stress, while a negative shift indicates a tensile stress

tion of an isolation technique. Good theoretical models /35/ are available and experimentally validated by using Micro-Raman Spectroscopy (μ-Raman) in combination with Transmission Electron Microscopy /36/. Detailed information on the local stress distribution can be obtained by combining Convergent Beam electron Diffraction with Electron Diffraction Contrast Imaging /37/. Effective stress measurements combined with 2-D simulations have shown to be a powerful tool for determining in the limits of LOCOS-based isolation techniques /37/. Figure 9 illustrates the use of μ-Raman to study the differences in stress distribution for the PBL and PELOX /32/. In the latter case the tensile stress (negative shift) is reduced, while the compressive stress in the active regions is increased. Too high tensile stress levels will result in the generation of dislocations in the silicon substrate, thereby strongly affecting the leakage current. For an in-depth study, one also has to take into account the quality of the silicon substrate. The impact of the interstitial oxygen content of the substrate on the electrical performance of the LOCOS isolation has recently been demonstrated /38/. Most likely, the increased leakage current for a higher oxygen content of the starting material may be associated with the role of the silicon interstitials on the silicon yield stress /39/. Three dimensional stress analysis can also efficiently be used for studying the defect formation of trench isolation structures /40-41/.

For 0.18 μm CMOS shallow trench combined with Chemical Mechanical Polishing for planarization will become the standard isolation scheme also for ASIC applications.

CMOS-SOI processes are frequently making use of a mesa isolation technique. Also in this case, down scaling the devices may cause some problems. Therefore, attention is given to a refill process combined with planarization. Recently, good results have been reported on using a Chemical Mechanical Polishing (CMP) step for the planarization of 0.35/0.25 μm technology /42/.

3.3 Interconnects and Metallization Schemes

To lower the resistivity of the interconnects in order to increase the speed performance of the circuits, the resistivity of the interconnection should be kept as low as possible. Therefore it has become common practice for VLSI and ULSI technologies to use a salicide technology. For deep submicron feature sizes, the most studied silicides are either $TiSi_2$ or $CoSi_2$. $TiSi_2$ is widely used in manufacturing processes because of its low resistivity and its good thermal stability. The process challenges for yield improvement are related to the silicidation of narrow runners, the elimination of bridging phenomena, and the integration of silicides in combination with shallow junctions respectively /43/. Important parameters to control the yield of silicided narrow polysilicon lines are the doping type and concentration, and the thermal budget of the back-end processing. Retarded silicidation reactions have been observed for As doped layers, and are more pronounced for thinner silicide layers. In the case of narrow active regions, the silicidation reaction can be enhanced by using an As amorphization implant, however with the increased risk for increased junction leakage.

For feature sizes below 0.35 μm, there is a strong interest in the use of $CoSi_2$ in view of the larger process window. For $TiSi_2$ the silicidation is related to the trans-

formation of the high resistivity C49 phase (60-90 $\mu\Omega$cm) into the low resistivity C54 phase (12-15 $\mu\Omega$cm). The transition temperature increases with decreasing film thickness, while at the same time the film disintegration temperature decreases. In addition, the doping type and concentration dependent silicide growth is strongly affecting the use of shallow junctions in a salicide process. In the case of $CoSi_2$, the transformation temperature from the CoSi into the $CoSi_2$ phase is proportional to the film thickness, and is therefore less influenced by down scaling effects. The thermal stability of $CoSi_2$ is also better than that of $TiSi_2$. The larger process window for $CoSi_2$ makes $CoSi_2$ a serious candidate to replace $TiSi_2$ in future scaled down technologies.

For Co silicidation the pre-cleaning step is, however, more critical than for Ti due to the gettering action of the Ti. To overcome this difficulty, investigations have been done to study bilayer systems where either an interfacial Ti layer (Ti/Co scheme) or a Ti capping layer (Co/Ti scheme) is used. Although both bilayers are resulting in a low and uniform sheet resistance for small linewidth, aspects such as the impact on the thermal stability, stress generation at the edges possibly resulting into void formation, the required cleaning steps, and the possible epitaxial regrowth phenomenon have an influence on the reproducibility and overall performance of the system and should therefore be taken into consideration.

The different metallisation schemes that are used have also to be optimised from a reliability viewpoint in order to avoid stress-induced voids and to reduce electromigration problems. The most commonly used metallisation schemes are based on a Al-Si-Cu or Al-Cu alloy. However, interest in other alloys is strongly growing. The research in novel Al-alloys is driven by electro- and stress migration requirements, which become dominant for smaller dimensions. For future technologies much attention is given to Cu-based interconnect layers, while also some more exotic alternatives are investigated. An important problem associated with metallisation is the step coverage, especially when a high aspect ratio is used. Therefore, advanced multilayer metal systems are based on contact and via filling. This can be achieved by using either W-CVD or hot Al-CVD. The selection of either W or Al for contact fill depends strongly on the quality of the barrier layer, both as chemical barrier and adhesion layer and as electrical barrier. Therefor the bottom and sidewall coverage of the barrier layer is of extreme importance, making scaling more and more difficult because of the increased aspect ratio's. Al planarisation is very attractive since its bulk resistivity is only 25 % of that of W-CVD. Present research is aiming at lowering the depostion temperature. Recently, a contact plug technology based on selective nickel silicidation has been proposed /44/. Each of the different plug filling technologies has its own advantages and drawbacks. Another important aspect, which is not addressed here, is the requirement for using barrier layers underneath the metal lines.

Spin-on glass (SOG) and etch-back techniques are commonly used for local topographical smoothing or partial wafer planarisation. However, the introduction of more than 3 metal layers with scaled down dimensions and stacked vias require the implementation of global planarization process steps as illustrated in Fig. 10. The figure shows the difference in approach for a 0.5 μm technology with three metal layers (TLM) and for a 0.35-0.25 μm technology with five metal layers (5LM) respectively. The former is using a SOG planarization, while the latter is based on chemical-mechanical polishing (CMP). One possible process is based on the etch back of Accuflo material, while a better alternative, which is also valid for further scaled down processes, is to use chemical-mechanical polishing (CMP). Although for a long time hampered by equipment, processing and defect control issues, CMP is nowadays a standard for global planarization. The main advantage is related to the global planarity, which compensates for shallow depth of focus. In additional the metal step coverage problems and the associated reliability hazards are also avoided. Some general information of the different aspects of CMP technology are given in /45,46/.

To increase the speed of the circuits, much attention is given to the study of low dielectric materials in order to replace SiO_2 as the interlayer dielectric.The capaci-

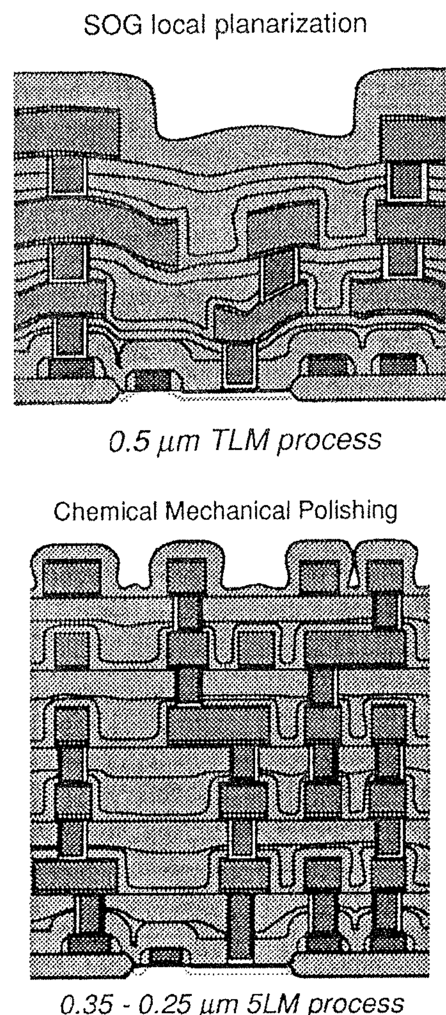


Fig. 10: Illustration of the difference in approach for a 0.5 µm three metal layer (TLM) technology and a 0.35-0.25 µm technology with five metal layers (5LM).

tance is directly proportional to the dielectric constant of the material so that a high K value strongly increases the RC delays. For small geometries, the total capacitance will be dominated by the line-to-line capacitance. This implies that the desired speed (related to the dielectric constant) will depend on the minimum feature size. The target roadmap for low dielectric material is shown in Table III /47/. For different future technologies, to be used for the manufacturing of microprocesses, the table indicated the maximum number of interconnect layers, the possible dielectric material, the desired dielectric constant, and the possible year of introduction.

Table III: Target dielectric constant (K) for future technologies /47/.

Technology µm	Interconnect Layers	Dielectric Material	K	Year
0.35	4-5	SiO_2	3.9	1995
		$SiO_2(F)$	3-3.7	
0.25	5	polymer	<3	1998
0.18	5-6	polymer	<2.5	2001
0.13	6	polymer	<2	2004
0.10	6-7	polymer	1-2	2007
		aerogels/air		
0.07	7-8	polymer	1-2	2010
		aerogels/air		

The status of the different dielectric materials given in Table III has recently been reviewed by Murarka /48/. The most important conclusions are briefly summarised. The doped oxide films contain 2 to 14 atomic percent fluorine in order to lower the dielectric constant. As for too high fluorine concentrations the films become unstable, the optimum concentration lays around 10%, resulting in a K value of about 3-3.2. However, not only the concentration itself but also the way the fluorine atoms are incorporated in the film has an impact on the dielectric constant. A large variety of polymers have been studied and are still under investigation. The polymerisation process results in anisotropic properties. Cross linking between polymer chains improves the rigidity and may also reduce the anisotropy. Both spin coating and vapour phase deposition techniques are used, with from an environmental viewpoint a preference for the latter due to the fact that they are solvent free. Polyimide siloxane and polysiloxane are intensively studied. Air has the lowest dielectric constant of 1, but imposes some practical problems due the interaction with metal schemes. Therefore aerogels, xerogels or foams in which air is trapped as bubbles in a solidified gel seem to be very promising. To develop a low dielectric material, a variety of materials properties have to be taken into account, such as rigidity, chemical stability, etching behaviour, interaction with metal layers, moisture take up, thickness uniformity, intrinsic stress levels, gap filling and planarization properties .... /49/. The characterisation of these low dielectric materials is a hot topic for the moment and not withstanding the strong industrial need in the near future, the development of new materials has just begun.

4. CONCLUSION

The future trend in silicon technology is on one hand a strong drive towards higher packing densities and increased electrical performances, pushing towards smaller device geometries, and on the other hand an increase of the functionality of core digital technologies by adding different functional options. Both approaches are associated with particular technological challenges. However, to achieve performance specifications at a minimum cost, the overall process complexity and the industrial manufacturability have to be kept under control.

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ZINC OXIDE BASED VARISTORS and PARALLEL CIRCUIT PROTECTION: THE STATE OF THE ART

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Key words: ZnO varistors, parallel circuit protection, historical survey, state-of-the-art, applications, main world manufacturers, R&D, Research & Development, technology trends

Abstract: In this conference the Author gives the historical of the research and the technology of Zinc Oxide based varistors since 1960 to this day with the following points:

- Discovery of the varistor effect in 1960 by Russians,
- Industrial development by Japanese,
- Current manufacture technique,
- Curreni performances: threshold voltage, residual voltage, Capacity of energy absorption, Aging.
- Main applications,
- Main manufacturers in the world.

The author described the main orientations of research and development:

- Increase of the threshold voltage (of 200 V/mm to 400 V/mm),
- Increase of the absortion capacity of energy (of 200 J/cm^3 to 600 J/cm^3),

The future technology will be:

- Chemical mixed powder method,
- Direct Oxydation of an alloy.

Varistorji na osnovi cinkovega oksida in zaščita vezij: trenutno stanje

Ključne besede: ZnO varistorji, zaščita vezja paralelna, pregled zgodovinski, stanje razvoja, aplikacije, proizvajalci glavni svetovni, R&D raziskave in razvoji, trendi tehnologije

Povzetek: V prispevku avtor podaja zgodovinski pregled razvoja in tehnologije izdelave cink oksidnih varistorjev od leta 1960 pa vse do danes in sicer:

- odkritje varistorskega efekta leta 1960 s strani Rusov
- industrijski razvoj, ki so ga opravili Japonci
- trenutne tehnike proizvodnje
- trenutne lastnosti: pragovna napetost, rezidualna napetost, kapaciteta absorpcije energije, staranje
- glavne veje uporabe
- glavni svetovni proizvajalci

Avtor opiše glavne smeri razvoja in raziskav:

- povečanje pragovne napetosti (od 200 V/mm na 400 V/mm)
- povečanje kapacitete absorpcije energije (od 200 J/cm^3 na 600 J/cm^3)

Tehnologija bodočnosti bo:

- izdelava iz kemično mešanega prahu
- direktna oksidacija zlitine

1. INTRODUCTION

Electrical circuit protection against overvoltage of atmospheric origin or coming from internal defects of the grid, needs non-linear resistive elements (i.e. elements whose current becomes very important when the voltage applied on its ends exceeds certain threshold value), such as park gaps, Silicon junction devices or varistors. The word "varistor" comes from the association two words: "Variable resistors". Before the coming of Zinc Oxide based varistors on the market of circuit protection, elements above-mentioned are used, for lack of something better, with their own disadvantages. Spark gaps represent two major disadvantages that are the variation of the protection voltage with the rise time of the overvoltage and the existence of the follow current. Silicon junction devices such as Diodes, Thyristors are used only for low voltage circuits and for small energies (in the range of 1 Joule). Varistors are represented by two types of materials, Silicon Carbide based

varistors and Zinc Oxide based varistors. The first type of varistor (SiC) presents a very high leakage current (more than 10 mA) and a low nonlinearity (10 times lower than Zinc Oxide based varistors) Figure 1. One was therefore constraint to use Silicon Carbide based varistors in series with a spark gap. The threshold voltage of this association becomes very sensitive to the over-voltage rise time.

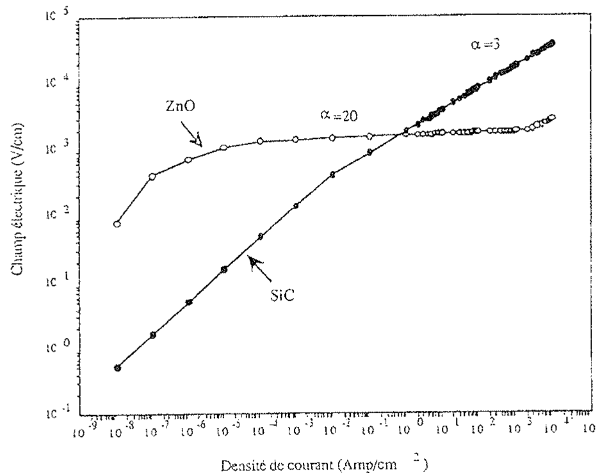

Figure 1

Zinc Oxide based varistors, recently arrived in the market, are not exempted of defects, but they represent an acceptable compromise in the field of energy, leakage current, response time and cost to be used in most of applications. In this communication, we give an overview on the history of varistors, its actual development and research undertaken in Laboratories with the aim to improve its electrical properties.

2. ZINC OXIDE VARISTOR STORY

In 1958, MS. Kosman and IA. Gesse in the former USSR, put forward, for the first time, nonlinear properties of Zinc Oxide based materials without a great echo in the industrial world /1/. It was only in 1968 that Matsuoka of the Matsushita Electronic Components company announces the discovery of the varistor effect after researches made on rectifier contacts between a semiconducting ceramic (Zinc Oxide) and a metal (Silver) /2, 3/. Since this date this company throws, in 15 years, in very diversified applications going from the low voltage to the high voltage protection.

Some years after publication of Matsushita in 1970, the main companies producing equipments for electricity, embarked in the same adventure. It concerns General Electric Company, Meidensha and ABB. The Meidensha Company benefits from the cooperation with Matsushita /4/.

The case of General Electric Company is very typical and merits to be related /5/. After the announcement by Matsushita in 1970 of the realization of Zinc Oxide based varistors, GE Co started in 1971 in the research and the development of the material by solving successively the problems concerning the sintering of the large pieces of varistors, the improvement of the nonlinear coefficient, the stability of the varistor under AC and DC voltage, the choice of electrodes and the coating of the varistor to avoid the flashover. These works have lasted 5 years. At the end of 1976 this Company began the production of the arrests for AC grids going from 10 KV to 600 KV. Firsts DC arresters of 588 KV, without spark gaps, are installed for the first time on the Brazilian system of ITAIPU.

Similarly to this effort of development, the researches developed strongly with as results the understanding of the conduction mechanism in this type of material, the correlation between some doping elements and electrical properties of the material. During years of 1980 one can count approximately 80 publications per year appeared in scientific reviews. Then this rate decreased to stabilize currently around 40 publications/year.

It is difficult to estimate exactly the economic weight of Zinc Oxide based varistors in the world. But one can have a precise idea of the Japanese production /6/. This country produces 1.2 Billion units per year with about $250 Millions.

In Europe producers of varistors are the following: Harris, ABB, LCC-Thomson, Soulé, Siemens, Iskra, Power development....

3. ZINC OXIDE VARISTORS: THE SATE OF THE ART

3.1 Manufacturing method

The composition

Most ZnO varistor materials contain more than 90 mol % ZnO and the composition is balanced by the addition of other oxides. A number of different additive oxides can be used to form varistor properties of a material, examples are oxides of Bi, Pr, Ba, Sr, La, Co, Mn, Ni, Co, Cr, Sb, Si, B, Ti. A typical ZnO varistor contains additions of Sb_2O_3, Bi_2O_3, CoO, MnO and Cr_2O_3. Powders of the oxides are mixed, spray dried, and they are subsequently pressed into green bodies which are sintered at temperatures around 1200°C.

Manufacturing process

Zinc Oxide based varistors are made, in general, by conventional process used for the manufacturing of ceramics. The main steps are described schematically in the figure 2. Doping additives in the form oxides powder with dimension about few microns, are weighed and mixed with ZnO by means of balls grinding. The duration of this operation takes some hours in wet medium with addition of organic products such that binders and lubricants that will facilitate following operations. The drying of the composition is accompanied by a granulation. This last operation gives a powder of spheroides of 100 μm in diameter.This powder is then pressed in mold with an appropriate form. These samples are then sintered at 1100 -1300°C. This operation is very important because it insures the crystalline growth of Zinc Oxide grains and the formation of the microstructure from which depend electrical properties of the varistor.

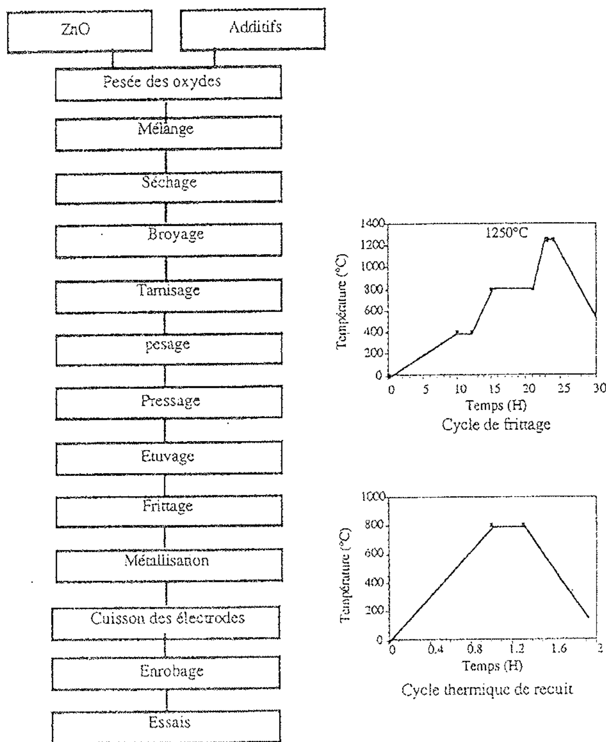

Figure 2

On sintered samples one deposits electrodes on the two parallel faces of the varistor bloc and an insulating layer of glass or of synthetic resin to avoid the flash over during shocks of great amplitude current.

3.2 The microstructure of ZnO varistor materials

The resulting microstructures consist of ZnO grains and intergranular phases. Intergranular phases are spinels of the type $Zn_7Sb_2O_{12}$, and a number of Bi-rich phases. There are other minor phases which are not readily detectable by conventional technique.

Spinel grains are usually present between the ZnO grains. The grains of spinel are considered to be electrically insulating and do not directly contribute to the non-linear current/voltage characteristics. Bi-rich phases may be present between the ZnO grains and spinel grains and these can form a three dimensional network along triple grain junctions of ZnO. The majority of the ZnO grain boundaries in the varistor material are devoid of intergranular film but they instead contain segregated Bi atoms.

The chemical formulations of the sintered products are complex and their complexity is further compounded by the nature of the doping elements that are invariably present in each phase. The major dopant in the ZnO phase is cobalt but manganese, chromium, nickel and antimony are also present in very small concentrations. The main compounds of the intergranular material are all doped by chromium, manganese, cobalt and nickel.

The breakdown voltage of a varistor is determined by the ZnO grain sizes in the varistor material. The ZnO grain size varies from few microns in the material for high voltage applications, to hundred microns in the material for very low voltages in electronics. The grain sizes are controlled by the amount and the nature of added oxides.

The basic building block of the ZnO varistor is the ZnO grain formed as a result of sintering. During this process, various chemical elements are distributed in such a way in the microstructure that the near-grain boundary region becomes highly resistive, and the grain interior becomes highly conductive.

The functional microstructure of ZnO varistor materials can be described as consisting of

- doped semiconducting ZnO grains ;
- ZnO interfaces which provide the barriers to electrical conduction and which give rise to the non-linear current - voltage characteristics ;
- a continuous network provides an alternative conduction path, that avoids the barriers that are associated with the ZnO interfaces, and can give a significant contribution to the conductivity in the pre-breakdown region of the current-voltage characteristics.

3.3 Electrical characteristics

I(V) curve and energy absorption capability /7/

Generally some electrical tests (on-line or off-line) are performed on varistors. First of all, one measures the electrical characteristic current-voltage I (V). From zero to 10 mA, this measure is made by means a DC voltage and automatically. Above 10 mA, one operates with short impulse current to avoid an excessive overheating of the varistor. For varistors to be used in medium and high voltage arrests, other tests are performed to insure their good behavior to thermal and electrical stresses.

Presented in the order where these tests are made, the first test is the aging test. To do this test, one applies a polarization voltage, a fraction of threshold voltage, for example Up= 0.6 Us, and one records the leakage current. This current has to be constant or maintained at a certain value that avoids the thermal run away. To accelerate the ageing and to limit the duration of the test to 1500 h, the sample is placed in a oven at 115°C.

Then one simulates lightning strokes by applying shocks of 65 kA impulse current of 4/10μs form. The variation of the threshold voltage after these tests, must be between 8 and 10%. Finally, one submits samples to long duration impulses (2 ms) to simulate switching overvoltage. Characteristics of these impulses are such that energy applied to the sample must be in the order of 100 J/cm^3. The variation of threshold voltage must be close to 0%.

Equivalent circuit

The equivalent circuit of the varistor can be represented by the following diagram (Fig. 3), where Ri and Ci are the resistance and the capacity of the joint of grain with

Ri dependent strongly the applied voltage Rej is the resistance of the Zinc Oxide grain. One adds an inductive element L because during of tests in shocks one observes a delay between the current and the voltage. One can use the following equation to represent a varistor:

$$U = kI^{1/\alpha} + RgI + LdI/dt$$

Where:

k = a constant depending on the value of the threshold voltage,

α = the nonlinear coefficient,

Rg= the resistance of the Zinc Oxide grain,

L= the inductive part of the varistor.

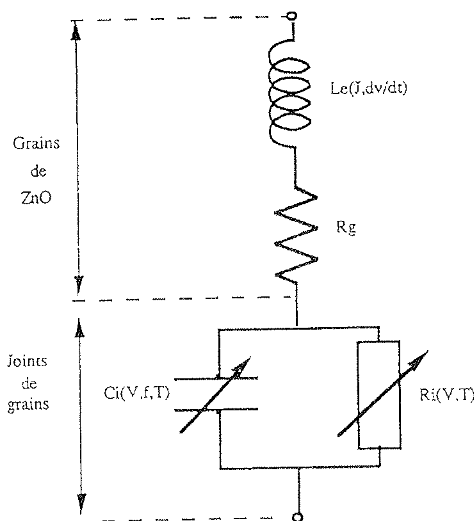

Figure 3

3.4 Conduction mechanism of Zinc Oxide Varistor /6/

Because of the granular structure of the varistor, there are in the ceramic potential barriers between Zinc Oxide grains due to a trapped electrons. These barriers of potential oppose to the passage of the current for low level voltage giving a high resistivity of the material. When the applied voltage to two adjacent grains is near 3 volts approximately, a recombinaison phenomenon is produced neutralizing the space charge and provoking a collapse of the potential barrier. The resistivity of the material decreases then strongly and it is limited only by the resistivity of Zinc Oxide grains.

3.5 Application of Zinc oxide Varistor in low voltage network

The overvoltages are always present in electrical networks (at low or high voltage). For low voltage system, the overvoltages come from the external side of the grid (lightning overvoltage, overvoltage coming from defect of the distribution system), as well as from the internal side (fusion of fuses in inductive circuit,..etc...). One estimates that the overvoltages can occur on the average 5 times per year with amplitude that can reach 4 KV. Taking into account on the other hand that the dielectric breakdown of most of domestic electrical machines do not exceed 1500 Volts (the rule 2U + 1000), one can see easily that it arrives often to observe the breakdown of these machines or in the most favorable case to observe a shortening of their duration of life. It is therefore imperative to protect them by protective devices that one puts in parallel to the entry of the power line. In a system with 3 phases, one inserts them between phases, between phases and earth and between neutral and earth.

Components used in protective system (a module) are generally Zinc oxide varistors and the gas spark gap. Useful characteristics of Zinc oxide varistors are:

- A very good non-linearity coefficient (more than 50)
- The variable threshold voltage following the thickness,
- A very good coefficient of quality: V (1mA)/V (5kA) =1.6-1.8
- A high capacity of energy absorption (200J/ cm^3)
- A weak drift of the electrical characteristic with the aging.

The spark gap is a protective device used in the past in the area of telecommunications. It is composed metallic electrodes and a ceramic envelope filled with a rare gas. On the wall of the envelope one deposits lines of graphite that serve as starter of the discharge. The energy absorption capacity of the spark gap is not great. Its interest resides in the low value of the capacity. For this reason, one uses them to protect signal lines.

Low voltage protection modules or low voltage arrests are made to be connected to the public distribution system or to electrical installations with voltage below I000V, for their protection against atmospheric or industrial overvoltages. Modules are realized with Zinc oxide varistors or in association of Zinc oxide varistors and spark gaps. Spark gaps are rarely used alone for the power line 250/ 400 V because of the extinction problem.

The multi-step protection is often used in very low voltage installation (< 50 V) to obtain a strong power dissipation and a weak residual level voltage.

4. CONCLUSIONS

Concerning research works, it is important to point out the following points:

- Research on the influence of the some doping elements on electrical properties of the ceramics,
- Research on chemically mixed oxides. These oxides are obtained by pyrolyse of nitrates or oxalates of metals dissolved in water. This method allows to obtain a homogeneous mixture,
- Research on others types of materials: SnO to replace ZnO, Praseodymium Oxide to replace the Bismuth Oxide,

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– Research on the manufacturing process and the composition to increase the threshold voltage (from 200 volts to 400 volts per mm) and the energy absorption capability of the varistors (from 100 J/mm to 300 J/mm).

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PZT THIN FILMS FOR MICRO SENSORS AND ACTUATORS

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Key word: micromechanical systems, PZT thin films, integration onto silicon substrates, ultrasonic micromotors, IR detectors, PZT ferroelectric materials, MOCVD, Metal-Organic-Chemical Vapor Deposition, MOD, Metal-Organic Decomposition, piezoelectric microactuators

Abstract: The paper reviews different aspects of deposition, integration, and device fabrication of $PbZr_xTi_{1-x}O_3$ (PZT) films for application in micromechanical systems. The deposition of such films and the principal processes for their integration onto silicon substrates are now fairly well mastered. Current efforts concentrate on tailoring the film properties for the various applications, and on optimization of the device designs and patterning processes. Current work on an ultrasonic micromotor and a pyroelectric IR detector is presented and discussed.

PZT tanke plasti za mikro senzorje in aktivatorje

Ključne besede: sistemi elektromehanski, PZT plasti tanke, integracija na substrate silicijeve, mikromotorji ultrazvočni, IR detektorji sevanja infrardečega, PZT materiali feroelektrični, MOCVD nanosi kemični s paro kovina-snov organska, MOD dekompozicija kovinsko-organska, mikroaktivatorji piezoelektrični

Povzetek: Prispevek v pregledni obliki podaja različne aspekte nanosa, integracije in izdelave komponent s $PbZr_xTi_{1-x}O_3$ (PZT) filmi za uporabo v mikromehanskih sistemih. Nanos teh filmov, kakor tudi načini njihove integracije na silicijeve substrate so danes že precej poznani in dozoreli. Trenutno so napori usmerjeni v prilagajanje lastnosti plasti različnim uporabam, optimizaciji načrtovanja komponent, ki jih uporabljajo, kakor tudi procesom fotolitografije. V prispevku prikazujemo trenutno stanje in delo na področju uporabe teh plasti pri izvedbi ultrazvočnega motorja in piroelektrićnega IR detektorja.

1. INTRODUCTION

In general, thin films allow an increase in functionality of devices by miniaturization, and reduction of fabrication costs by batch processing. Integration onto silicon offers the possibility to apply silicon micromachining techniques, and to integrate sensor and electronics on the same substrate. In recent years, a number of research groups have concentrated their efforts on the preparation of the ferroelectric material $PbZr_xTi_{1-x}O_3$ (PZT) as a thin film, and its integration onto silicon substrates for the development of ferroelectric memories, piezoelectric actuators and sensors, and pyroelectric infra-red detectors. Various obstacles were and are encountered on the way to achieving a perfect film for a given device. High quality films require deposition or annealing temperatures of around 600 °C in oxygen or air. For this reason the deposition process often is not compatible with other materials in the device: Interdiffusion and/or delamination may occur. Film growth conditions and integration technology influence each other and both affect the device performance. In this paper different aspects of deposition, integration, device fabrication and applications of PZT films are reviewed.

2. THIN FILM DEPOSITION

A historical review of ferroelectric thin film deposition is given in ref. /1/. Whereas before 1990 mostly physical deposition techniques (evaporation, RF sputtering) were applied, chemical methods dominate at present. Metal-organic-chemical vapor deposition (MOCVD) is the preferred technique for IC applications, because of its superior step coverage. Metal-organic decomposition (MOD), with or without sol-gel reactions, is likely to emerge as the leading method for actuator and sensor applications because of the low investment needed. Sputtering will keep its place in cases where a lowering of the deposition temperature is of importance.

High quality PZT thin films can be grown with in-situ deposition techniques like sputtering at 500 to 550 °C /2,3/, or with MOCVD at 700 °C /4,5/. The post-anneal for sol-gel deposition has to be carried out at temperatures between 600 and 650°C /6/. All processes usually work with an excess of lead. Lead or PbO desorb quickly from the surface at these temperatures, as long as they are not incorporated in the perovskite lattice. With in-situ deposition techniques one observes a self stabilization

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of the lead content at stoichiometry above a critical temperature, even for large quantities of excess lead flux. The critical temperature depends on the deposition method and is 700 °C for $PbTiO_3$ grown by MOCVD /7/, and was found to be lower for sputter deposition (550°C) due to plasma effects /8/.

3. INTEGRATION

The choice of substrate is usually dictated by the application or by the need to lower production costs. Hence, the substrate is often not the most ideal one for growing the ferroelectric thin film. The integration technology has to solve adhesion and interdiffusion problems and should provide a mean to arrive at the required film microstructure. Finally, the patterning, i.e. the selective etching of the involved films, has to be mastered.

The most important substrate for micro systems is silicon. High quality PZT films cannot be grown directly on it. Buffer layers are needed to prevent interdiffusion and oxidation reactions. For most applications, the PZT film has to be grown on an electrode, which obviously should neither oxidize nor become insulating. The most often reported materials include platinum, and the metal oxides RuO_2 (rutile structure) /9/ and (La,Sr)CoO_3 (LSC, perovskite structure) /10/. Usually, the chemical barrier function is provided by two or more layers, including the electrode. PZT/Pt/Ti/SiO_2/Si is the most widely applied sequence, where the Ti is needed as an adhesion layer. Platinum does not inhibit the diffusion of Ti to the PZT side, where it reacts with oxygen and serves as nucleation centers for PZT. There is also evidence that oxygen migrates along the grain boundaries through the platinum film and reacts with the Ti layer /11/. For stable electrodes the latter has to be preoxidized /11/. Barrier schemes with insulating films, such as SiO_2 and Si_3N_4, cannot be applied when a direct electrical contact to a silicon or metal substrate is required. In this case, RuO_2 electrodes are superior to platinum electrodes. In combination with a second metal (e.g. Cr), which stops the residual oxygen diffusion, RuO_2 allows the growth of PZT on very reactive refractory metals, such as zirconium (see fig. 1) /12/.

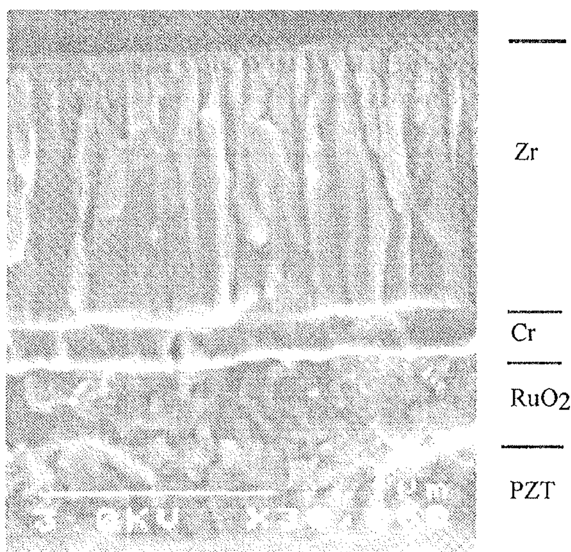

Fig. 1: Scanning electron microscopy image of a cross section of the layer stack PZT/RuO_2/Cr/Zr (the photo is up-side-down) deposited for piezoelectric activation of thin zirconium membranes (from ref. /12/, 0.6μm sputtered PZT).

The requirements with respect to film microstructure depend on the application. For piezoelectric applications polycrystalline films may be sufficient. However, for pyroelectric applications it is advantageous to have a textured film with the ferroelectric polarization perpendicular to the substrate plane. This is not easy to obtain for $PbTiO_3$, in which an additional complication arises due to the cubic-to-tetragonal ferroelectric phase transition below the deposition temperature. With a perfectly textured (100) film in the cubic high temperature phase, only 1/3 of perpendicular polarization is obtained a priori below the phase transition. The degree of perpendicular polarization (c-axis orientation) finally obtained at room temperature is strongly influenced by the thermal expansion mismatch between substrate and film /13,14/. Well c-axis oriented films are obtained on $SrTiO_3$ /15/ and MgO /16/ substrates, because their high thermal expansion compresses the film upon cooling from the growth temperature and the larger c-axis is switched out of the plane.

Due to its much smaller thermal expansion, this does not happen on silicon substrates. Even worse, if the deposition process yields a tensile stress, as caused by the shrinkage of the sol-gel preparation technique, its stress is compensated by switching the c-axis into the plane and thus useful polarization is lost. Sputter processes allow incorporation of a compressive stress during in-situ deposition, and hence stronger c-axis orientation /3/. With stress measurements as a function of temperature it is in principle possible to determine the degree of c-axis orientation (see fig. 2). Note that stress compensation by 90° domain flipping works only above about 300 °C.

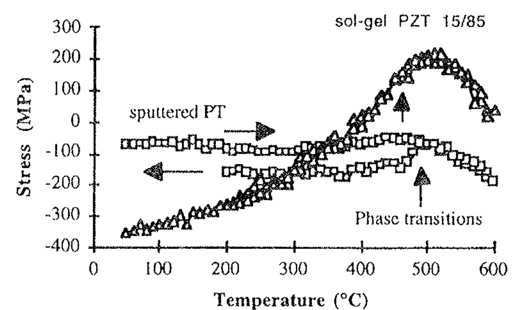

Fig. 2: Film stress vs. temperature curves for a heating/cooling cycle. The curves result from the difference between the substrate curvatures with and without (etched off) P(Z)T film. Positive values indicate tensile stress, while negative indicate compressive stress. The phase transitions are marked as known from bulk ceramics. The intensity ratio I(002)/I(200) of the <100> sputtered film dropped form 1 to 0.8 due to thermal cycling. The sol-gel film exhibited mainly (100) orientation. (The measurements have been performed with a commercial FLX 2900 system).

With sol-gel deposition, (111) oriented PT films turned out to be the better choice. Their pyroelectric coefficient is close to the theoretical value expected for this orientation (60 % of (001) single crystal coefficient), because poling involves only switching of 180° domains.

Textured growth can be controlled by a number of process parameters and by the electrode. The phenomena observed in in-situ sputter deposition do not seem to be so much different from those observed in sol-gel deposition techniques. For the growth of textured PZT films on platinum electrodes /17/ two nucleation regimes are observed:

1. Self orientation of PZT (100). These faces have a lower surface energy and thus the (100) orientation is obtained under certain favorable circumstances. These are: lead excess, which leads to a high mobility; slow nucleation, i.e. no faster nucleation of another orientation takes place; Ti rich at the nucleation interface (The Ti may also come from below the platinum.). With in-situ sputter deposition, (100) nucleation of $PbTiO_3$ works very well, whereas for PZT(100) a $PbTiO_3$(100) template has to be applied (see fig. 3) /8/.
2. Epitaxial orientation of PZT(111) on well textured Pt(111). The close lattice match between these two lattices is not sufficient to assure a good (111) orientation. An additional "glue" is often required. A very effective method consists of applying a 1 to 2 nm thin TiO_2 seed layer. It could be shown /18/ that this film is textured, i.e. it grows epitaxially on Pt(111). This seed layer promotes a quick nucleation of PZT(111), during which it is dissolved in the PZT. The method works as well with in-situ sputter deposition as with sol-gel techniques /18/.

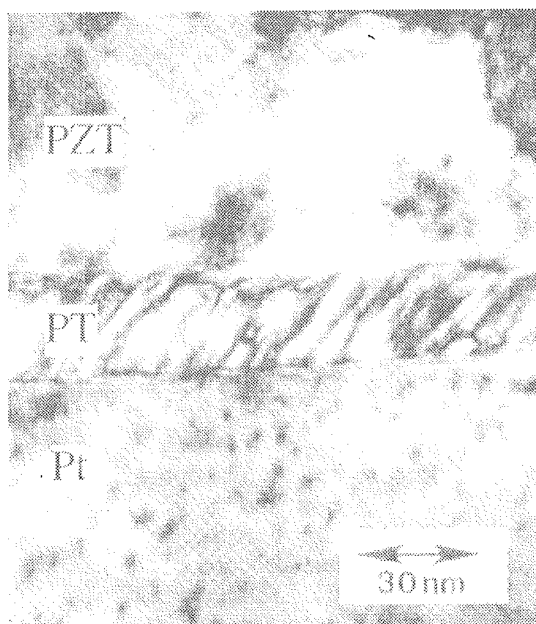

Fig. 3: Transmission electron microscope image of a 30 nm thick $PbTiO_3$ template film between the platinum electrode (bottom) and the PZT film. The oblique stripes are caused by the domain structure of alternating (100) and (001) orientations (from ref. 8).

4. ACTUATORS

Piezoelectricity is a competitive actuation principle for micro-actuators and sensors. Compared to thermal methods (bi-metal and shape memory alloys), piezoelectricity dissipates less heat and can be applied at much higher frequencies. With regard to electrostatic actuation, piezoelectricity demands less complex structures, exhibits a better linearity between applied voltage and force, and yields a larger force output.

4.1 Operation principle

For actuation, the reverse piezoelectric effect is exploited between the E-field (E_3) parallel to the polarization, being perpendicular to the film plane, and the stress perpendicular to the polarization (σ_1 and σ_2) in the film plane. These stresses create a bending moment with respect to the neutral plane of a membrane or cantilever structure. It is clear that the passive part below the piezoelectric film must be at least as thick as the piezoelectric film. Compared to the usual e_{31} coefficient for full clamping, the effective piezoelectric coefficient is enhanced by the fact that the film is free to expand perpendicular to the surface (direction of index 3). For a uniform planar geometry one obtains /19/:

$$\sigma_{1,2} = -e_{31,eff} \cdot E_3 = -\frac{d_{31}}{s_{11}^E + s_{12}^E} \cdot E_3$$

The stress σ_1 can be determined from the resonance frequency shift vs. applied dc field of a membrane containing the piezoelectric film /19/. More often, the strain x_3 perpendicular to the film plane is determined, as it can be accurately measured by means of double side interferometry /20/ without need for structuring the substrate. The so derived coefficient d_{33} is also an effective value, which is lowered by the substrate clamping /21/. In fig. 4 strain and frequency shift (stress) are compared as a function of the applied dc voltage. The two "butterfly" curves look pretty much the same and illustrate how the thickness increase of the film (positive strain) is accompanied by an increasing tensile stress (positive frequency shift) in the film plane. The d_{31}/d_{33} ratio was derived, taking into account the elastic compliance constants of bulk ceramics. The obtained values between -0.4 and -0.5 are in agreement with bulk ceramic data.

PZT thin films exhibit higher coercive fields (typically 50 kV/cm) and higher break-down voltages (300 kV/cm) than bulk ceramic PZT. It is therefore possible to drive thin film devices with higher fields in order to compensate partially for the smaller thickness (t_p). (The relevant force per unit width of the film is $e_{31,eff} \cdot E_3 \cdot t_p$).

Ultrasonic actuators, such as stators for micromotors or fork structures for resonant sensors, utilize diaphragms or other structures in resonance. Here it is important to consider the influence of the geometry on the coupling constant, and to minimize the stress of the involved films. If the thickness h of the passive part (low stress nitride, silicon) is increased beyond about three times the thickness of the PZT film, the square of the coupling

constant k, k^2, is decreased as h^{-1}, i.e., a smaller fraction of electrical energy can be converted into mechanical work. When k^2 becomes less than tanδ, more energy is dissipated than transformed into mechanical work. The figure of merit of efficiency can be given as: $(e_{31,eff})^2 \cdot t_p/(\varepsilon \cdot \tan\delta)$. Ideally the PZT film thickness is about half as thick as the supporting silicon structure. In this case, an effective coupling constant k_{eff} of 0.40 has been calculated for a cantilever /22/. Tensile film stresses have to be avoided, because they drastically reduce the coupling factor in the range of small silicon thicknesses, where the coupling constant would be highest.

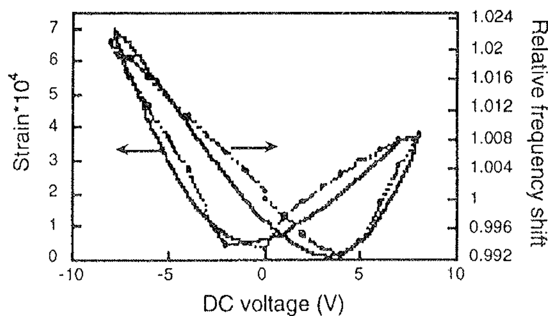

Fig. 4: Normalized strain measured perpendicular to the film plane by optical interferometry, and the normalized frequency shift of a resonating membrane, as a function of the applied dc voltage. The latter is proportional to the in plane stress (from ref. /19/, 0.6µm sputtered PZT 45/55, two different substrates). The piezoelectric coefficients evaluated from the slopes are: $d_{33,eff}$ = 50 pm/V, $e_{31,eff}$ = 4 C/m^2.

4.2 Ultrasonic micromotor

The first characterization of a functional PZT thin film micro motor has recently been performed /23,24/. A hybrid type motor was applied, which utilizes static deflection waves of an ultrasonic thin film stator. These are transformed into a rotational movement by an elastic fin rotor /25/. The motor could be operated with voltages of less than 1.0 V_{rms}. A maximal torque of 0.3 µNm was achieved with 2.4 mN normal force applied between stator and rotor. The highest speed observed was 20 rps. Fig. 5 shows a schematic cross section of the motor set-up, and in fig. 6 a picture of the electrode structure is displayed. Moving rotor and gear are shown in the video picture of fig. 7.

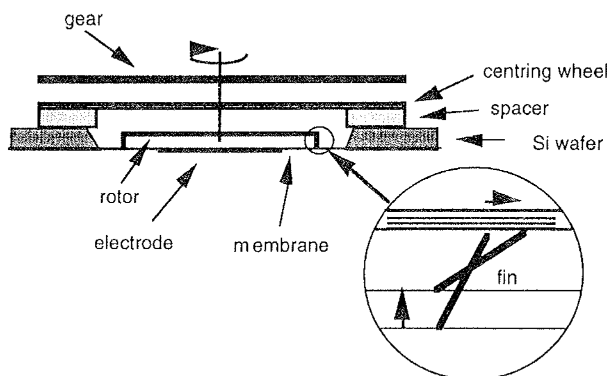

Fig. 5: Schematic cross section through the set-up of the elastic fin motor.

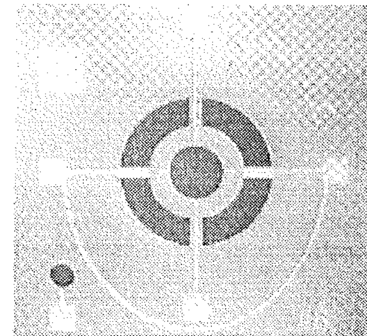

Fig. 6: Image of the ultrasonic stator as seen from the electrode side. The outer diameter of the ring shaped electrode is 3.6 mm (from ref. /24/.

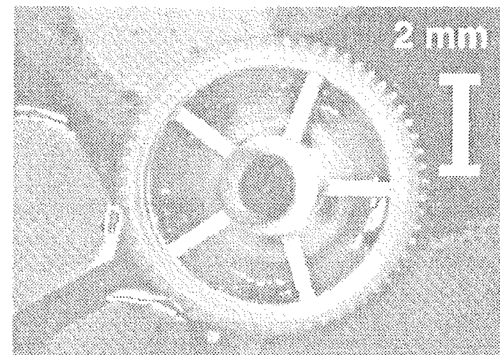

Fig. 7: Video picture of working micromotor. Rotating rotor (bottom) and load wheel (top) are seen. The static wheel fixes the axle (from ref. /23/).

Stators with 1 µm thick sol-gel deposited PZT 45/55 of (111) orientation have been investigated for various thicknesses (15 to 100 µm) of the passive silicon part. In fig. 8 the speed vs. applied ac voltage is displayed. The application of an additional dc bias increases polarization and piezoelectric constant, and thus the rotation speed of the motor. There is a threshold voltage of 0.5 to 1.0 V_{rms} below which there is not enough amplitude for initiating the rotation. Above the threshold, the speed increases linearly with the applied ac voltage, and thus the deflection amplitude. The torque at zero speed saturates at low voltages of 1 to 2 V_{rms} at 0.25 to 0.3 µNm, which must be the value of the frictional torque /25/ for the applied normal force. Speed and torque per voltage, as well as the threshold voltage, did not change with varying silicon thickness. It must be concluded that the motor receives a constant fraction of the mechanical power delivered by the stator, as this power does neither change in the given thickness range.

The output power of the motor was measured as 1 to 2 $\mu W/V_{rms}$ typically (independent of silicon thickness). This is for the thinnest membrane (i.e. 15 μm thick silicon) 4×10^{-4} times the reactive power delivered to the capacitance, and hence also smaller than the dielectric loss power ($\tan\delta = 0.03$). The square of the effective coupling constant k^2_{eff}, measured as 0.03 from impedance measurements, is a rough measure for the amount of electrical energy that is converted into mechanical work of the membrane. The transmission efficiency between stator and rotor therefore seems to be rather small. For an improvement, the normal force needs to be increased, in order to increase the frictional torque.

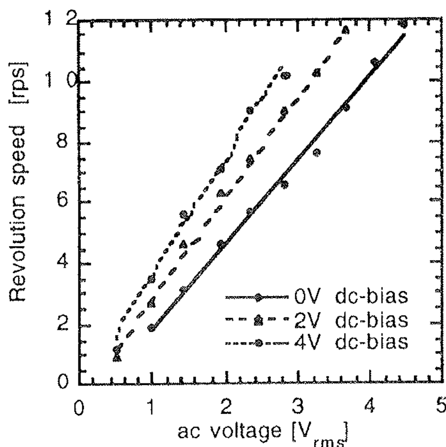

Fig.8: Revolution speed as a function of applied ac voltage for a stator with 50 μm thick silicon and a 1 μm thick PZT film (B_{10} mode at 108.1 kHz, /24/).

5. INFRA-RED DETECTORS

Pyroelectric infra-red detection is a potentially important application for ferroelectric thin films. Compared to bulk devices, thin film devices exhibit a small thermal time constant (t_{th}) and thus work better at higher frequencies, which is interesting for thermal imaging. Several industrial laboratories therefore have programs for the development of 2-dimensional arrays /26/. Due to the small heat capacity of thin film elements, heat conduction to the substrate (acting as heat sink) must be reduced. Silicon micromachining is a very convenient technique to tailor the thermal properties. Very thin ceramic membranes of 0.9 μm can be fabricated in this way as a supporting structure /27/. The thermal insulation by such membranes is so effective that the cooling by air convection becomes dominant /28/.

The output of a pyroelectric can either be measured as a voltage response R_V or a current response R_I. The frequency behavior of a simplified situation is shown in fig. 9. In contrast to bulk sensors, thin film sensors have electrical time constants (t_e typically 10 to 100 s) that are larger than the thermal ones (t_{th} typically 30 ms or smaller). This has an important advantage: The noise voltage drops already in the intermediate frequency range between inverse electrical ($1/t_e$) and inverse thermal time constant ($1/t_{th}$), which is the ideal range for voltage detection (see fig. 10).

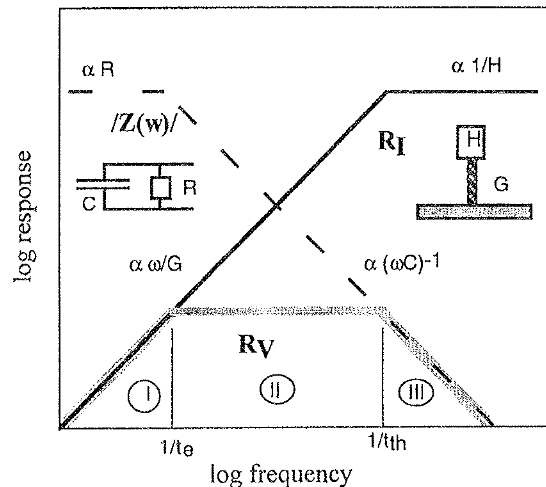

Fig. 9: Log-log scheme of current and voltage response, together with the impedance for the typical thin film situation where the thermal time constant is much shorter than the electrical one. Thermal wave length effects are neglected. (G is the thermal conductivity, H the heat capacity.)

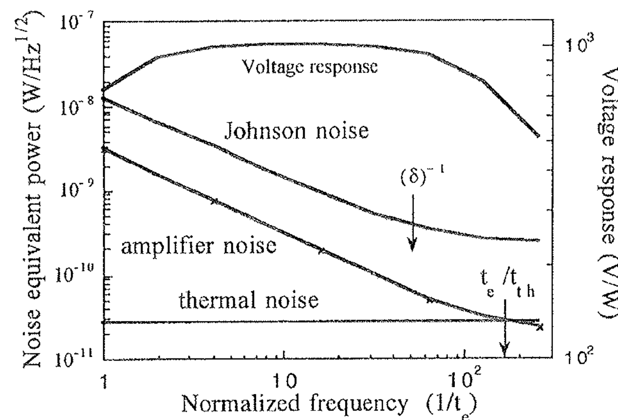

Fig. 10: Noise equivalent powers (NEP) of different sources for a model element with 1 mm^2 surface and cooling by air convection only, calculated from experimentally verified parameters. (Formulas from ref. /31/.) The displayed frequency is normalized to $1/t_e$

An array of 900 x 400 x 1.5 μm elements on Si_3N_4/SiO_2 membranes has been realized /28,29,30/. In order to avoid the above mentioned orientation problem of tetragonal PZT, the 1.6 μm thick PZT 15/85 film was grown in (111) orientation by sol-gel techniques, applying the TiO_2 seed layer. Black platinum was taken as absorbing layer on top of PZT (see fig. 11). A voltage response of 800 V/W was obtained at 1 Hz, and a current

response of 15 μA/W was measured at more than 20 Hz /29,30/ (see fig. 12). Thermal wave length effects account for the increase of the current response above the calculated behavior in fig. 12. The elements exhibited typically a noise voltage of 1 μV at 1 Hz /28/, corresponding to a noise equivalent power of 1.2 nW. This low noise level is in agreement with the calculations of fig. 10. Although the thin film elements do not have yet the sensitivity of $LiTaO_3$ single crystals at the low frequency of 1 Hz, their signal to noise ratio is as good.

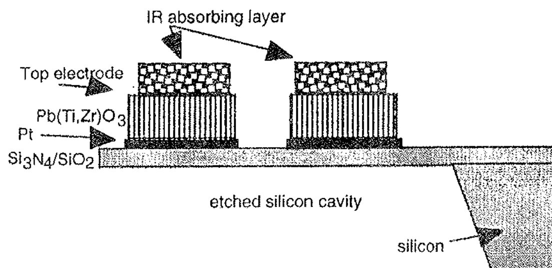

Fig. 11: Typical structure of pyroelectric elements on a thin membrane fabricated by means of micromachining (only a fraction is shown).

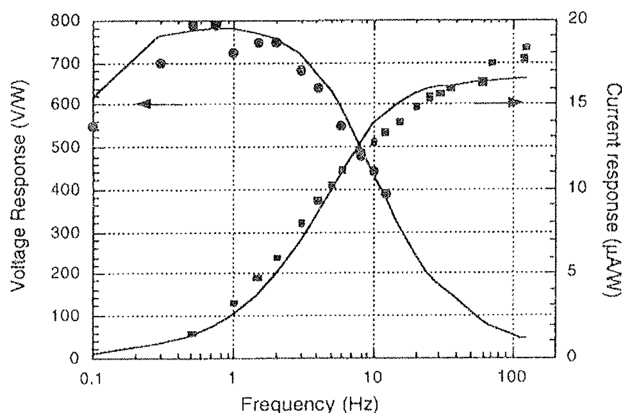

Fig. 12: Measured voltage and current responsivities (dots) as a function of modulation frequency for a PZT pyroelectric array element (from ref. /29/). The full lines are calculated responses.

6. OUTLOOK

Ferroelectric thin films offer alternative solutions for microsystems in the field of microactuators and sensors. Ideal designs still have to be done, especially in the case of piezoelectric devices. Improvement of film properties can certainly be expected, since there is still room for optimizing film composition and microstructure. Thicker films are of great interest, since they allow to increase the force output of actuators, and to decrease the dielectric noise of sensors. Finally, the degradation of PZT films in ac (vibrating structures) and dc applications (switches) has to be studied.

7. ACKNOWLEDGEMENTS

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ANALYTICAL ELECTRON MICROSCOPY OF ADVANCED CERAMIC MATERIALS

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Keywords: advanced ceramic materials, AEM, Analytical Electron Microscopy, PZT-PNN piezoelectric materials, PLZT ferroelectric thin films, TEM, Transmission Electron Microscopy

Abstract: Application of analytical electron microscopy (AEM) in the development of advanced ceramic materials is presented and discussed. The capabilities of different techniques which are used in analytical electron microscope are described with examples of the investigation of various materials such as PZT-PNN, Si_3N_4, NiO-ZnO solid solution, RuO_2 based thick film resistors and PLZT thin ferroelectric films. The importance of proper TEM sample preparation and selection of appropriate operating conditions for transmission electron microscope experiments is emphasized.

Analitska elektronska mikroskopija sodobnih keramičnih materialov

Ključne besede: materiali keramični zahtevnejši, AEM mikroskopija elektronska analitična, PZT-PNN materiali piezoelektrični, PLZT plasti tanke feroelektrične, TEM mikroskopija elektronska transmisijska

Povzetek: Hiter razvoj sodobnih keramičnih materialov s posebnimi mehanskimi, električnimi, optičnimi ali magnetnimi lastnostmi je pogojen z uporabo specialnih metod karakterizacije mikrostrukture. V delu so opisani primeri uporabe analitske elektronske mikroskopije (AEM) pri raziskavah in razvoju novih materialov. Metode preiskav, ki jih omogoča AEM so visokoločljivostna elektronska transmisijska mikroskopija (HRTEM), s katero direktno opazujemo kristalno mrežo, energijska spektroskopija rentgenskih žarkov (EDXS), ki nam omogoča določitev elementne kemijske sestave izredno majhnih volumnov in različne vrste elektronske difrakcije (elektronska difrakcija izbranega področja (SAED), mikrodifrakcija ter elektronska difrakcija s konvergiranim snopom (CBED)), ki nam omogočajo določitev strukture in kristalografskih odnosov med posameznimi fazami v vzorcu. Materiali, ki jih delo obravnava so feroelektrični prahovi in tanke plasti na osnovi PZT, Si_3N_4 keramika, azbesti, fulereni, ZnO-NiO trdne raztopine in debeloplastni upori na osnovi RuO_2.

1. INTRODUCTION

The development of advanced ceramic materials with special mechanical, electrical, optical or magnetic properties is related to the parallel development and use of different methods for their microstructural characterization. In many cases, a knowledge of the chemical composition and structure of various phases (precipitates, intergranular layers, corrosion products, interface layers) is important for a better understanding of the chemical and physical processes taking place during the fabrication of ceramic materials.

Methods which may be used for the characterization of the microstructure of advanced ceramic materials are limited due to the relatively small particle size of some phases. Various techniques of optical microscopy can be used for the study of particles with sizes much larger than a few µm. X-ray diffraction, normally used in routine investigations of phase composition, cannot detect the presence of amorphous or extremely fine-grained phases. For determination of the chemical composition, electron probe microanalysis (EPMA) may be used in cases where particles of interest are not smaller than a few µm. With relatively low accelerating voltages (below 10 keV) it is possible to avoid the influence of the matrix or substrate material, and to analyze particles with sizes just below 1 µm, but under such conditions large errors in the results are to be expected.

Frequently the only method allowing the examination of very small volumes is analytical electron microscopy (AEM), which combines scanning transmission electron microscopy and some microanalytical method, such as energy dispersive X-ray spectroscopy (EDXS) and/or electron energy loss spectroscopy (EELS). AEM enables simultaneous examination of the structure, structural relationships between phases, and chemical composition of the samples. /1/

The basic techniques for material investigations using the analytical electron microscopy are:

- Conventional Transmission Electron Microscopy (CTEM) which is used for the observation of the

morphology of samples, determination of different parameters related to crystal structure and identification of various defects and features in crystal lattices using bright and dark field experiments. /2/

- High Resolution Transmission Electron Microscopy (HRTEM), where direct imaging of the crystal lattice is possible. The application of this method is limited by the resolution of TEM. The technique is used for determination of very thin intergranular phases, examination of interfaces in multilayer structures, and investigation of different defects and the crystal lattice structure. /3/
- Various techniques of electron diffraction, such as Selected Area Electron Diffraction (SAED), Microdiffraction and Convergent Beam Electron Diffraction (CBED). From the diffraction patterns the structure, orientation, symmetry, crystallographic relations and thickness of the sample may be determined. /2/
- Energy Dispersive X-ray Spectroscopy (EDXS). This method allows chemical analysis of very small particles. While qualitative and semiquantitative analysis is rather routinely used, the quantitative analysis of small particles and phases containing light elements (C,N,O) is quite complicated and time consuming. /4/
- Electron Energy Loss Spectroscopy (EELS) is used for chemical analysis of light elements, determination of the valency state of elements, energy filtering, etc. /5/

In the present paper examples of the application of techniques of analytical electron microscopy in research on and development of different advanced ceramic materials are presented and discussed.

2. EXPERIMENTAL

Experimental details of the preparation of the materials used in this study were published elsewhere /14-16, 20, 21, 27, 29/. Powder samples were ground in an agate mortar in ethanol and ultrasonically dispersed on a hollow carbon coated Cu grid for TEM investigations. Plan-view specimens of bulk samples and thin films supported on substrates were prepared by mechanical thinning, dimpling and ion milling using argon ions. In the case of bulk material, samples were eroded from both sides, while in the case of thin films only from the substrate side. Cross-sections of the thin film samples were prepared using a Gatan cross-sectional TEM specimen preparation kit. Normally, samples were cooled with liquid nitrogen during the final stages of ion erosion.

Samples were examined by Jeol 2000 FX transmission electron microscope (TEM), operated at 200 kV. The chemical composition of phases was determined using a Link AN-10000 EDXS system (Energy Dispersive X-ray Spectroscopy) with an Ultra Thin Window Si(Li) detector, connected to the TEM. The Cliff-Lorimer /6/ method and absorption correction /7, 8/ were used for quantitative analysis. In most cases the concentration of oxygen was calculated from stoichiometry. Quantitative EDXS analysis with a precision (defined as the relative standard deviation) equal or below 5% was achieved, notwithstanding problems during the sample preparation, peak overlapping and absorption corrections.

3. RESULTS AND DISCUSSION

3. 1. TEM-EDXS analysis of powder and porous bulk samples

AEM techniques used in investigations of powder samples enable chemical reactions taking place during the ceramic material fabrication to be followed on a micro or even nano scale. The size (thickness) of the powder particles should not be much higher than 100 nm to enable the penetration of electrons. Thicker particles should be milled, but in such a case the interfaces and the relationships between different powder particles are usually destroyed. Various methods /9-12/ of embedment of larger powder particles were proposed using epoxy, electroless nickel and copper or amalgam. Subsequently TEM samples are prepared employing ion erosion or microtome cutting. These methods may be problematic due to excessive heating and selective ion milling, or introduce defects due to large stresses (in the case of microtomy).

A solid solution of $Pb(Zr,Ti)O_3$ - $Pb(Ni_{1/3}Nb_{2/3})O_3$ (PZT-PNN) is a promising material for piezoelectric applications. Chemical reaction mechanisms during synthesis of the material are not yet well understood because of the quite complicated composition (5 different starting oxides)/13/. Many binary and ternary compounds in this system have similar crystal structure with similar unit cell parameters, and some starting oxides have extremely small particle size, and therefore just the XRD technique alone could not be used for positive identification of all the phases present during thermal treatment of the samples. Using analytical electron microscopy we were able to answer some unsolved questions /14/. We systematically examined TEM samples of the starting mixture of oxides and powders prepared at different firing conditions. On each sample we inspected numerous particles and determined their structure by electron microdiffraction (the size of the particles was between 20 and 200 nm) and chemical composition by quantitative EDXS. In Figure 1 TEM micrographs (a), EDXS spectra (b) and microdiffraction patterns (c) of powder fragments of PZT-PNN loose powder, thermally treated at 650 °C for 60 min are shown. Most of powder the particles were small enough, not to require any particular sample preparation. Using EDXS and electron microdiffraction techniques, it was found that the three binary phases PN, PZ and PT could coexist at this temperature. NiO and partly ZrO_2 were still unreacted at this point of the sample synthesis. The ternary compound $Pb(Ti,Zr)O_3$ was also detected (not present in Fig. 1). Obviously NiO enters the solid solution at much higher temperatures.

Examination of the chemical composition of primary particles (grains) in the first stages of sintering (neck formation stage) may provide interesting and valuable results. Preparation of such samples for TEM observation represents severe problem. Usually samples are

mechanically extremely sensitive and should be handled with great care during the grinding, polishing and dimpling procedures. In the ion erosion step the structure and chemical composition of the grains could be altered due to overheating.

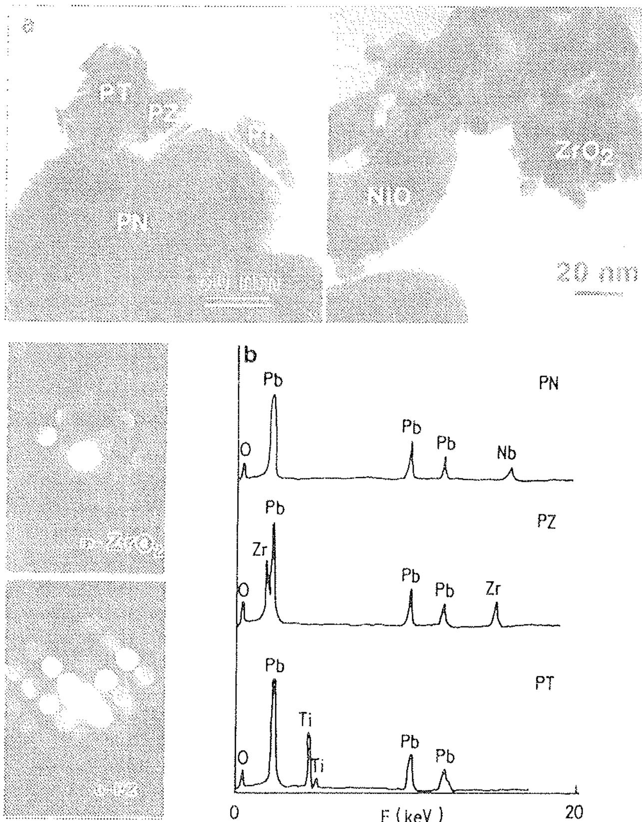

Fig. 1: (a) - TEM micrographs of fragments in a PZT-PNN loose powder sample fired at 650 °C for 60 min, (b) - EDXS spectra of $Pb_2Nb_2O_7$ (PN), $PbZrO_3$ (PZ) and $PbTiO_3$ (PT) phases, (c) - microdiffraction patterns of monoclinic ZrO_2 and orthorhombic PZ.

Particles (grains) are bound together only in the necks, so that thermal conductivity is poor. Cooling of the sample with liquid nitrogen in the final stages of ion milling could partly, but not completely overcome heating problems.

Figure 2 displays a dark field TEM micrograph of sol-gel derived PZT (50/50) grains in a sample fired at 650 °C for 5 hours and reheated at 850 °C for 1 hour. The TEM sample was prepared by ion milling (Ar ion energy of 4.0 keV) and was cooled with liquid nitrogen (LN_2) in the final stages of the erosion (last half hour). The micrograph was taken using diffuse scattered electrons, so that the bright contrast around grains and at neck areas represents an amorphous phase containing extremely small (few nm) precipitates (bright spots). Deficient cooling of the sample during ion milling could be deduced from the results. After using a lower energy of ion milling (3.8 keV) and a longer cooling period (during the whole milling time) it was found that some PbO - rich phase was still present at the neck areas. Based on other experimental results of methods such as XRD, DTA and sintering curves, it was concluded that this t PbO rich phase was not an artifact but a consequence of dehomogenization during the early stages of sintering /15/.

3. 2. Deterioration of the structure and chemical composition during TEM experiments

Beside the danger of altering the structure and chemical composition of the samples during ion milling, some samples could also deteriorate during observation in the transmission electron microscope (in-situ) due to electron beam induced heating or high energy electrons damage. The latter case is characteristic of high-energy microscopes (400 keV and higher). Most organic materials, glasses and inorganic solids with high volatility (for example lead and bismuth oxides), or with chemically bound crystalline water or (OH)- groups (talc, chrysotile asbestos, etc.) are especially sensitive to this phenomenon. Fullerene, a globular form of carbon (with chemical formula C_{60} and C_{70}) is among the materials that are very susceptible to an electron beam.

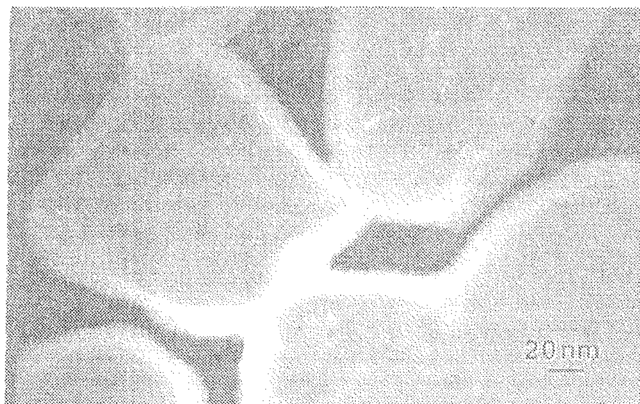

Fig. 2: Dark field TEM micrograph (using diffused scattered electrons) of neck areas in a sample of PZT (50/50) fired at 650 °C for 5 h and 850 °C for 1 hour.

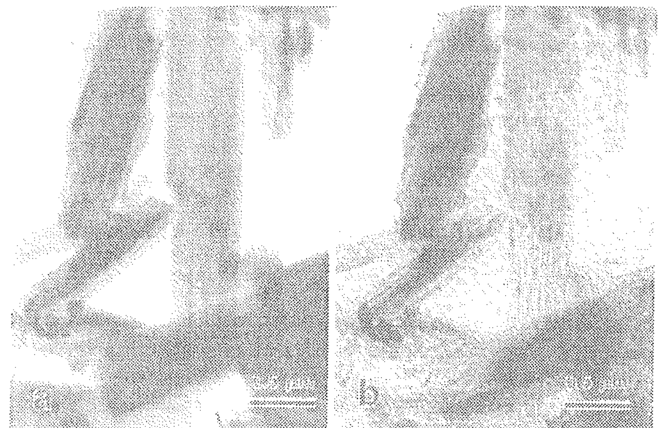

Fig. 3: (a) - TEM micrograph of fullerite crystals before and (b) - after the in-situ heating experiment

In Figure 3a a TEM micrograph of crystals of fullerite (crystals of a solid solution of C_{60} and C_{70} in f.c.c. or h.p.c. form) before degradation is shown. During the in-situ heating experiment using an intense electron beam (larger condenser aperture and smaller spot size), part of the material evaporates. The residues of the crystals (skeletons) became amorphous but still preserve their original size and shape. The evaporated material condensed in the vicinity of the amorphous residue of the crystals. In Figure 3b a TEM micrograph of the crystals after the heating experiment is displayed. Small (up to 50 nm) droplets between the skeletons of the crystals were found to consist of fullerite nanocrystals. We were able to explain the anomalous vapour pressure of fullerite at higher temperatures in terms of its tendency to become amorphous on heating /16/.

3. 3. Structural ceramics, wear and erosion

Ceramics used for applications where mechanical properties are of main importance and limit their use (strength, hardness, toughness, shock resistance, etc.) are called structural ceramics. Among other materials, light Si_3N_4 is quite promising, mainly for high temperature applications (turbine rotors etc.). During the fabrication of Si_3N_4 ceramics, a thin amorphous oxy-nitride layer is normally formed at the grain boundaries (GB) between adjacent grains, with the exception of the low angle and special grain boundaries /17/. The presence of this amorphous phase is usually determined by different techniques of transmission electron microscopy /18/. Serious problems in using these methods include the thickness of the intergranular phase (around 1 nm), the amorphous contamination layer and the grain boundary grooving produced during ion milling of the samples. The chemical composition of the secondary phase at the GB, which is believed to have a strong influence on the mechanical properties at high temperature, could not be accurately determined even using extremely narrow electron beams in dedicated TEMs with field emission guns /19, 20/. The most reliable method for determination of the presence of the amorphous intergranular phase is high resolution electron microscopy.

Figure 4 represents a high resolution transmission electron microscope (HRTEM) micrograph of a 1 nm thick

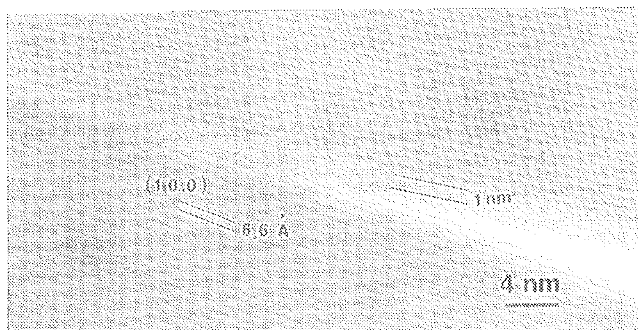

Fig. 4: HRTEM micrograph of a 1 nm thick intergranular layer of oxy-nitride glassy phase between two Si_3N_3 grains in Si_3N_4:Yb_2O_3 ceramics.

intergranular layer of oxy-nitride glassy phase between two Si_3N_3 grains in Si_3N_4:Yb_2O_3 ceramic material.

The wear mechanism of structural ceramics is affected by the temperature, by their reactivity with the counter material, as well as by the presence of active species in the environment (humidity, lubricants etc.). In the case of Si_3N_4 in contact with itself under dry conditions, brittle fracture of Si_3N_4 grains prevails, resulting in severe wear and a high coefficient of friction. In the case of the presence of humidity, a protective oxide layer is formed resulting in a significantly lower wear rate. Identification of the reaction products formed in dry or lubricated contact between the two parts is of major importance for understanding (and reduction of) the wear of ceramics in different environments. Such products were examined using methods of analytical electron microscopy in isostatically hot pressed silicon nitride plates on top of which a Si_3N_4 ball was oscillating. It was found that the fretting wear of silicon nitride depends on the amplitude of oscillation and on the environmental conditions, at least in the range examined /21/.

Figure 5 shows a TEM micrograph (bright field) of an area in the wear scar on a Si_3N_4 plate exposed to fretting at an amplitude of 15 μm for 30 minutes. The microcracks which were found around the silicon nitride grains severely deteriorate the mechanical properties of this part of the ceramic material.

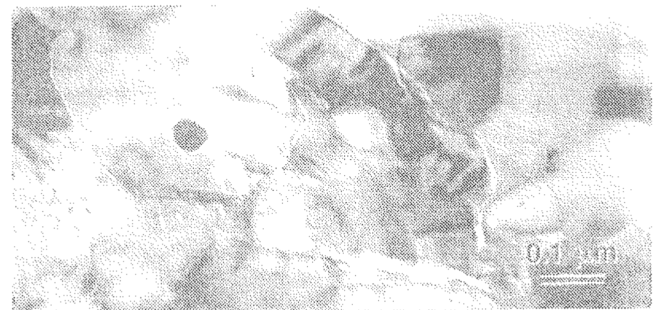

Fig. 5: TEM micrograph of an area in the wear scar on a Si_3N_4 plate exposed to fretting at an amplitude of 15 μm for 30 minutes.

Superficially completely different, but actually a very similar case of the use of AEM in the identification of erosion products is the determination of asbestos fibres in drinking water. Asbestos fibres are a health hazardous material that increase the risk of lung cancer when they are inhaled. In waterworks and piping systems, built several decades ago, asbestos-cement pipes were used. This material incorporates asbestos fibres as a hardening agent. When water flows through this type of pipes, the walls are eroded and the asbestos fibres are carried away. In the last decade the potential health effects of asbestos fibres in drinking water have received much attention. There has been some concern that populations exposed to high concentrations of asbestos in their drinking water over long periods of time could show an increased incidence of gastrointestinal tract cancers. Asbestos often occurs naturally in

drinking water, and concentrations of several million fibres per litre are not uncommon. The normal use of asbestos-cement pipe contributes relatively low levels of fibres to the water which is conveyed through them. Today it is believed that asbestos fibres are carcinogenic only when inhaled, and not when ingested /22/.

The only method that could positively identify asbestos fibres is analytical electron microscopy /23-26/. As a positive identification high matching of the morphology (aspect ratio), chemical composition (ratio of elements Na, Mg, Ca, Fe to Si) and the structure (using electron diffraction) to standard values should be achieved.

In Figure 6a TEM micrograph, an electron diffraction pattern and an EDXS spectrum of chrysotile asbestos fibre from drinking water (waterworks in a city in Slovenia) is shown.

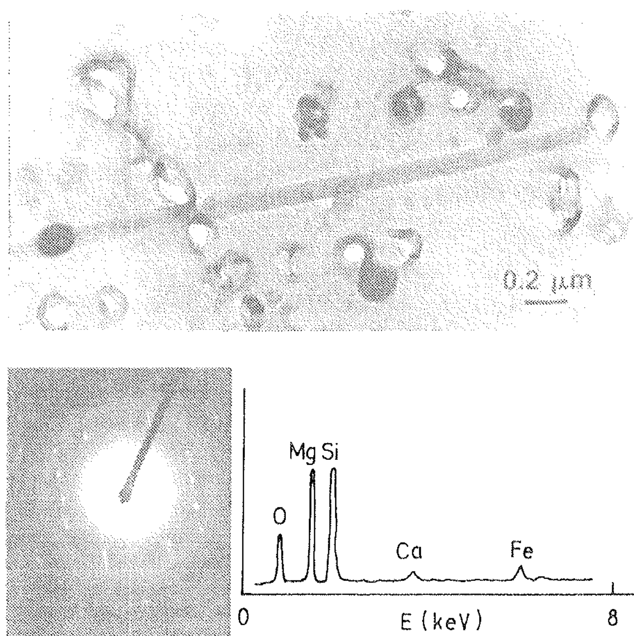

Fig. 6: TEM micrograph, electron diffraction pattern and EDXS spectrum of a chrysotile asbestos fibre from drinking water.

3. 4. Electronic ceramics; properties vs. microstructure

In the ZnO - NiO system two solid solution phases (ZnOss: solid solution of NiO in ZnO phase and NiOss: solid solution of ZnO in NiO phase) coexist. It was found that this material posseses a positive temperature coefficient of electrical resistivity (PTCR) if it contains a suitable ratio of the two phases. The origin of the PTCR anomaly was explained on the basis of the percolation model. The conductivity of ZnOss is much higher than that of NiOss grains in the ceramic material. On the other hand, the linear thermal conductivities of the two phases are very different, and thus on heating the interconnections between the particles of the highly conductive phase are loosened and the bulk conductivity is substantially decreased.

A TEM micrograph is given in Fig. 7, showing the stress field (S) at the top of a microcrack (M) at the ZnOss-NiOss boundary in a thermally treated sample with 40 wt.% of ZnOss /27, 28/. The thermal expansion differences cause mechanical stresses at the grain boundary during cooling of the sample. These stresses are relaxed by the formation of microcracks which could not be annealed at lower temperatures, and therefore provoke ageing and finally, after repeated thermal cycles, the collapse of the material. This effect prevents the practical use of the material.

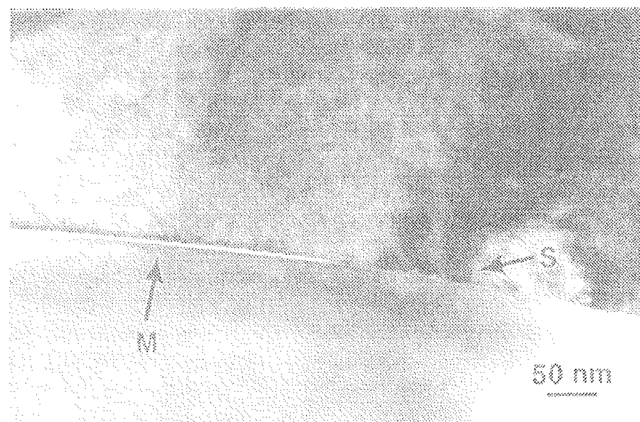

Fig. 7: TEM micrograph showing the stress field (S) at the top of a microcrack (M) at the ZnOss-NiOss boundary in a thermally treated sample with 40 wt.% of ZnOss

A similar example where only AEM techniques could confirm suspected reasons for distinctive electrical properties is the influence of the microstructure on the gauge factors in thick film resistors /29/. The gauge factor of a resistor is defined as the ratio of the relative change in resistance and the strain applied. As well as geometrical reasons alone (change in dimensions due to applied stress), it was found that the size and distribution of the particles of the conductive phase also plays an important role in this phenomenon. In Figure

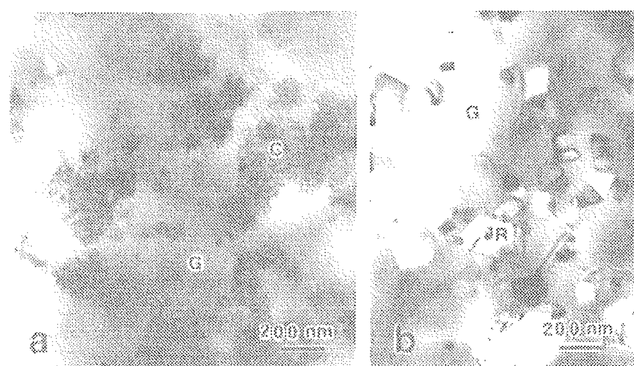

*Fig. 8: (a) - TEM micrograph of a DuPont 8041 sample (C - clusters of RuO_2 particles)
(b) - Heraeus 8241 sample (R - RuO_2 grains). In both micrographs G is the matrix glass phase.*

8a a TEM micrograph of a sample of DuPont 8041 thick film resistor material is displayed. Clusters of very small (< 10 nm) RuO_2 crystalls were found, up to 200 nm in size. This material posesses a relatively small gauge factor (3.5). On the other hand, material with larger RuO_2 particles (up to 200 nm) which are more or less uniformly distributed in a glassy matrix exhibit a much larger gauge factor (16). The microstructure of such material is shown in Figure 8b (Heraeus 8241 sample). From these findings it was concluded that materials with larger average distances between the conductive grains exhibit larger gauge factors than materials with a shorter average distance between the grains /29/.

3. 5. Ferroelectric thin films

Materials based on lead zirconate-titanate ($Pb(Zr,Ti)O_3$) or lead-lanthanum zirconate-titanate ($(Pb,La)(Zr,Ti)O_3$) are currently being extensively investigated due to their potential use in electronic and electro-optic devices. The use of these materials in non-volatile memories, piezoelectric SAW devices, microactuators, pyroelectric sensors and electrooptic modulators requires miniaturization, which is achieved by using thin films on substrate materials. For ferroelectric thin film fabrication, various methods are used, amongst which the sol-gel method appears to be the one with the highest possibility of controling the stoichiometry of composition /30/.

In Figure 9 a dark-field TEM micrograph of a cross-section of a sol-gel derived PLZT (9.5/65/35) thin ferroelectric film is shown. The sample was thermally treated at 600°C for 20 hours. Due to its very small thickness (0.5 μm), transmission electron microscopy is again the only method which enables the observation of the microstructure across the film. Seven different layers could be observed in Figure 9. First from the bottom is an amorphous (800 nm) SiO_2 layer which is on the top of a Si monocrystal wafer. Then follows a 40 nm thick amorphous Pb-Si-O reaction layer, a 20 nm thick crystalline TiO_2, 100 nm Pt (electrode) layer, 20 nm thick $PbTiO_3$ (seeding) layer, a 300 - 400 nm thick perovskite layer and finally a 50 - 100 nm thick fine-grained pyrochlore

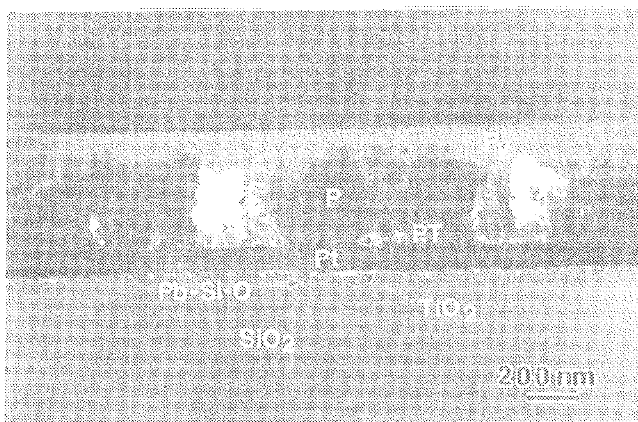

Fig. 9: TEM micrograph of the cross-section of a sol-gel derived PLZT thin ferroelectric film on <Si>/SiO_2/TiO_2/Pt substrate fired at 600 °C for 20 hours.

layer. Due to a defective Pt layer, the PbO from the PLZT film reacted with SiO_2 during the firing procedure, forming a reaction layer. Lead-oxide deficient PLZT film did not completely crystallize in perovskite form but a thin pyrochlore layer was formed on the top of the sample.

Applications of AEM techniques in the study of various ferroelectric materials, such as quantitative EDXS analysis of bulk PZT materials, chemical line profiles across thin PLZT films, determination of the degree of homogenization, etc. are to be found in /31/.

4. CONCLUSIONS

In this work some examples of the investigation of various inorganic materials in the form of powder, bulk ceramic and thin films using techniques of analytical electron microscopy are described. Detection of submicron phases, intergranular layers, microcracks and the distribution of phases throughout thin ferroelectric were presented and discussed. In many cases it was found that TEM sample preparation is the critical step that can introduce artifacts or deteriorate the structure or chemical composition. Analytical electron microscopy is an indispensable tool in the research and development of modern ceramic materials.

Acknowledgment

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DETERMINATION OF CRITICAL CONDITIONS FOR CONTACT RELIABILITY OF Ag-BASE CONTACT MATERIAL

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Keywords: electrical contacts, material for electrical contacts, contact resistance, potential difference of closed contacts, voltage levelling, contamination of electrical contact, heating of contact, supertemperature of contact spot, measuring systems, vacuum degassing, cleaning of contact surfaces, RF plasma cleaning, CFC solvents, ChloroFluoroCarbon solvents

Abstract: Due to cost-effective manufacturing of electromechanical relays and similar switching devices for low power switching applications the feasibility of Ag-base contact materials in order to replace Au-base contact materials has been studied. Commercialy available materials were used for test samples: AgNi 0.15, Ag/Ni 10 and Ag/CdO 10. Samples were pretreated by various cleaning methods prior to testing. A low power limit for reliable application of sample material was estimated by measuring contact resistance versus contact force relationship and close-contact voltage fall versus electric current relationship under various ambient conditions and state of contact surface

Določitev spodnje meje stikalne moči za kontaktno zanesljivost pri gradivih za električne kontakte na osnovi srebra

Ključne besede: kontakti električni, materiali kontaktov električnih, upornost kontaktna, razlika potencialov kontakta sklenjenega, stabilizacija razlike potencialov, onesnaženje kontakta električnega, segrevanje kontakta, supertemperatura mesta kontaktnega, sistemi merilni, razplinjevanje vakuumsko, čiščenje površin kontaktov, FR čiščenje plazemsko radiofrekvenčno, CFC topila klorofluoroogljikova

Povzetek: Raziskana je možnost, da se v relejih za preklapljanje električnega toka malih moči namesto dražjega gradiva za kontakte na osnovi Au uporablja gradivo na osnovi Ag. Za raziskavo so bili uporabljeni komercialno dobavljivi vzorci sledečih gradiv: AgNi 0.15, Ag/Ni 10 in Ag/CdO 10. Površina vzorcev je bila predhodno obdelana z različnimi čistilnimi postopki. Spodnja meja za zanesljivo preklapljanje kontaktov iz vzorčnega gradiva je bila ocenjena z meritvijo odvisnosti med kontaktno silo in kontaktno upornostjo, ter odvisnosti med tokom skozi sklenjen kontakt in razliko potenciala na njem pri različnih pogojih okolja in stanja kontaktne površine.

1. Introduction

High contact reliability even at extremely low switching current and voltage can be achieved by Au-base contact materials, which are on the other hand not price-friendly. For low-to-medium switching power less expensive Ag-base material are more suitable. In order to enlarge the application range a multilayer contacts are used, having thin outer layer of Au-base material and bulk of Ag-base material.

In order to make proper decision not to choose expensive material if not necessary, a study of applicability of Ag-base contact material for low power switching is performed.

The reliability of contacs depends not only on material, but also on contact force, microscopic conditions of contact surface and ambient conditions in which contacts operate. In low power switching devices contact parts are ordinary incapsulated thus providing a certain degree of protection against influence from ambient. From our own experience it is known, that the initial contact surface state before assembly are essential for contact reliability.

2. Preparation of samples prior to measurements

The research was oriented on application of contact materials at manufacturing conditions, therefore commercially available materials were used as sample materials:

- AgNi 0.15 alloy
- Ag/Ni 10 composite
- Ag/CdO 10 composite

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Pretreatment of contact surface prior to measurements was made by following methods:

- cleaning in chloro-fluoro-carbon (CFC-Freon) at ultrasound agitation
- vacuum degassing at elevated temperature
- etching in RF low pressure hydrogen plasma
- sulphurizing in H_2S
- exposing to laboratory dust ambient

3. Principles of measurements

In order to evaluate contact reliability following quantities were measured:

- contact resistance R_C (four-connection measurement)
- potential difference on closed contacts U_C (contact voltage fall)

A cross-rod principle of contact system was applied. Contact pair consists of two crossed miniprofile strips with cross-section, shown on Fig. 1. Sample strips are pressed by contact force F_C, which is set by actuator of force control and weighing system. Measuring and control system were interconnected via computer due to synchronization of force setup and measurement of contact characteristics, as shown on Fig. 2. Special computer software has been made for control and measurement operations.

In order to enable measurement on various contact sites of individual contact sample, contact strip was mounted on holder with computer controlled XYZ-axis drive. Obtained measured results can therefore be averaged along contact strip.

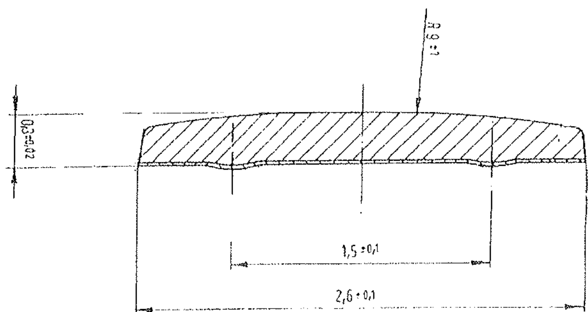

Fig. 1: Cross-section of sample contact strip. Mating contact surface has a semicilindric form with curvature radii of 9mm.

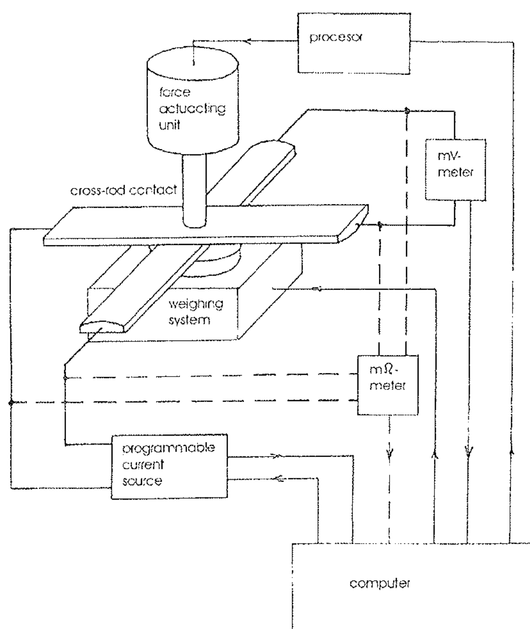

Fig. 2: Arrangement of control and measuring system for measurement R_C - F_C and U_C - I relationship

4. Measurement of R_C versus F_C

Contact force F_C was set in the range from 3 cN to 50 cN, starting with minimal value and gradualy increasing in steps. At each step contant force was maintained constant during measurement of contact resistance R_C. Special care was taken to minimize the effect of ambient vibrations. An average of 10 measurements obtained on 10 contact spots 1mm apart of each other at each specified F_C value and standard deviation was calculated. Results were arranged on R_C (F_C) plot of average values.

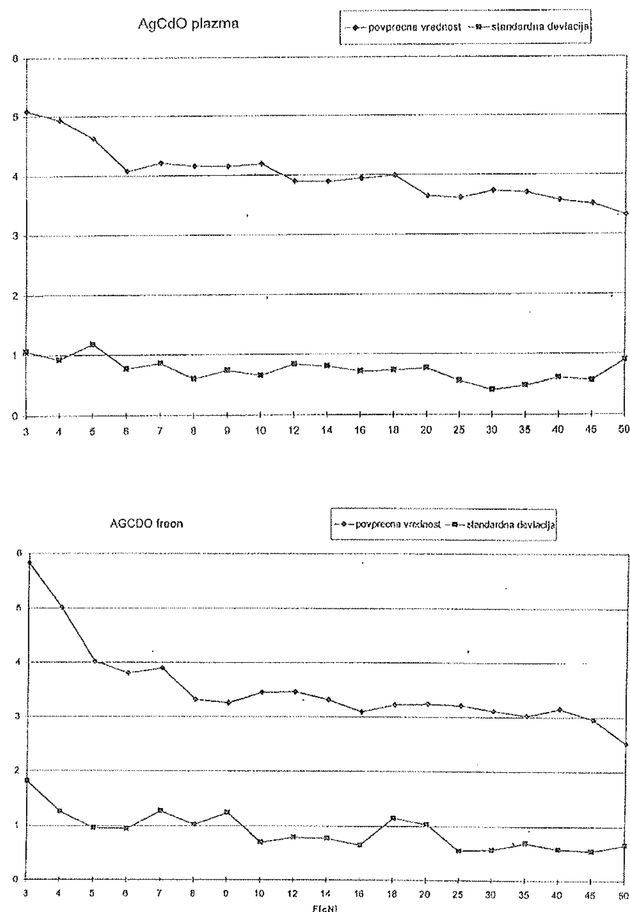

Fig. 3: Graphs of R_C (F_C) and standard deviation for Ag/CdO 10 sample material after treatment in RF hydrogen plasma (upper plot) and after cleaning in CFC (lower plot); R_C scale in [mΩ]

R_C follows significant decreasing function at increasing of F_C, as shown on graph of Fig. 3, according to general theory of contact resistance /1/. Standard deviation is over the entire range approx. 1 mΩ. At 3 cN contact resistance is between 5 and 6 mΩ, approaching to 3 mΩ at 50 cN, irrespective of sample material. Characteristics are more sensitive on state of contact surface, then on the composition of sample material. Plasma etched samples exibit for about 1 mΩ higher contact resistance at 50 cN than samples prepared by other cleaning methods.

Very high and unpredictable values of R_C were also obtained on various contact samples at low F_C untill some critical value has been reached. Beyond this limit R_C again decreases to low and stable value. The effect is attributed to insufficient cleaning and thin films remaining from previous handling of sample material (grease, finger prints, dust particles embedded on contact surface, etc.). By increasing contact force con-taminating film was destroyed and low contact resistance is obtained.

5. Measurements of U_C versus I

For this type of measurements contact force was set on predetermined value and kept constant during measurement procedure. Measurements were performed at 3 cN and 15 cN. The potential difference U_C was measured on closed contacts at current I through contact spot. U_C was measured during the increase of I starting from 0 value to 3 A.

By comparing results of individual contact sites of the same sample, significant differencies between characteristics can be indicated. Some of them are linear functions U_C (I) reaching few mV at 3 A. In such cases contact spot behaves as pure ohmic resistor due to constriction resistance. A weak influence of various pretreatment of contact surface is presummably also indicated on graphs of Fig. 4, although any existence of contaminant films on contact spot is indicated. Other characteristics reveal deviations from linearity and at 3 A measured voltage reaches a value of few 10 mV. A tendency of contact voltage to approach toward certain limiting value can also be observed, as shown on Fig. 5. In this case not only constriction resistance, but also resistance of foreign film over contact spot contributes to measured contact voltage /1, 2/. Foreign films often reveals semiconducting characteristics /3/, therefore in consequence a nonlinear behavior of voltage-current characteristic. In the extreme case nonlinearity results on so called "voltage levelling", where U_C value at increasing current approaches constant value /4/. Levelling phenomenon on Ag-base contact sample is displayed on graph of Fig. 6. According on theory of contact spot potential difference U_C relates to supertemperature on contact spot /3/, therefore at levelling thermal decomposition of foreign films by fritting and broadenning of current conducting area take place. The highest U_C value is obtained at melting of contact spot /5/ or even evaporation of contact bridge. For pure Ag and composite Ag-base materials (Ag/Ni, Ag/MeO, etc.) following data /6/ at melting of contact spot ($U_{C\ melt}$) and disruption of contact bridge ($U_{C\ disr}$) due to evapo-

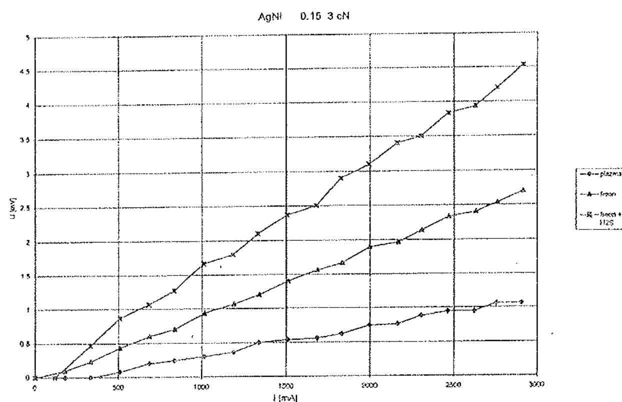

*Fig. 4: Graphs of $U_C(I)$ at F_C 3 cN for AgNi 0.15 sample material after various pretreatment procedure: ♦ - in RF hydrogen plasma, Δ - in CFC, * - exposed to H_2S. Linearity indicates constant constriction resistance of stable contact spot*

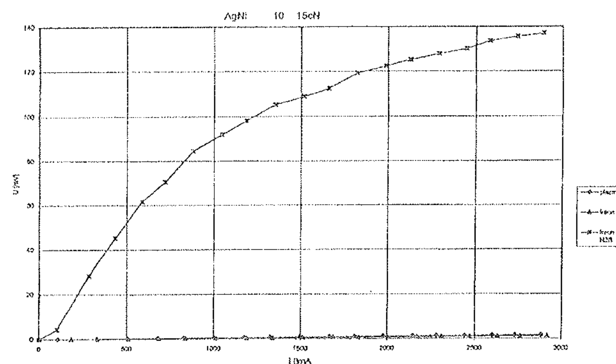

Fig. 5: Strong nonlinearity of U_C (I) graph, obtained on Ag/Ni 10 at 15 cN after H_2S treatment (--), presummably due to heating of contact spot*

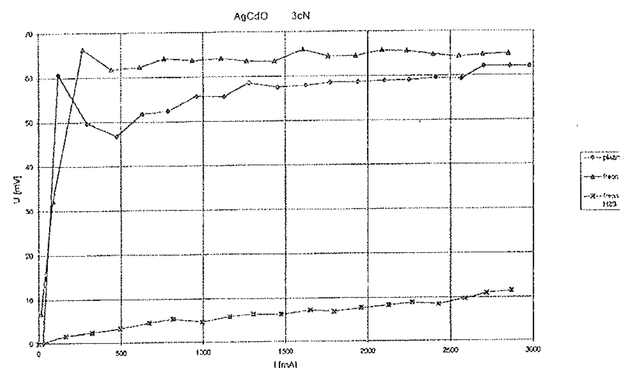

Fig. 6: Voltage levelling at approx. 60 mV observed on different Ag/CdO 10 samples at 3 cN after various (insufficient) cleaning process (♦ - plasma, Δ - CFC). Sample contact exposed to H_2S indicates slight nonlinearity of U_C - I characteristics. Results are reather controversal due to local variations of surface contamination

ration are valid:

$U_{C\,melt}$ = 0.39 V (at 961°C) $U_{C\,disr.}$ = 0.70 V

Approximative relation between supertemperature T_m [K] and level voltage U_C derived from exact theoretical expression can be applied for estimation of temperature on contact spot. For Au and Ag the following expression give us values with accuracy of ±10% in temperature range from 100 to 500°C /3/:

$$T_m \cong 3100\sqrt{U^2 + 0.009}$$

Following values for voltage level values were obtained and estimated temperatures of contact spots were calculated:

U_C [mV]	T [°C]
200 ± 20	≅ 385
150 ± 10	≅ 250
80 ± 10	≅ 85
30 ± 5	-

Among these results only value of 200 mV can be referred to melting of Ag_2S layer. Values above 100 mV can be attributed to softening of silver, other values seems to be too low for indentification of melting of foreign substances on contact spot.

No correlation of U_C level values to the particular contact material is found. At lower contact forces sometimes higher level voltages were detected (Fig. 7). Consequently not only one layer is presummably present on contact spot.

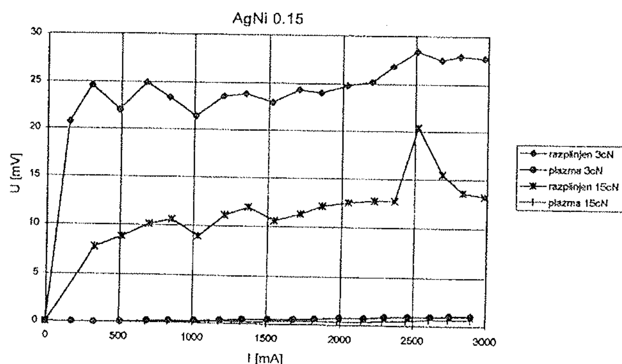

Fig. 7a: Voltage levelling at low values on various contact materials after vacuum degassing. Higher level is obtained at low contact forces (- ♦- 3 cN) and lower level at greater (-- 15 cN). Contamination on contact spot presummably consists of semihard insulating film*

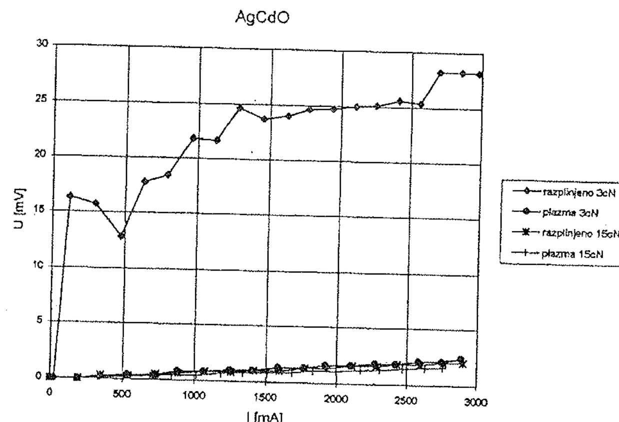

Fig. 7b: Voltage levelling at low values on various contact materials after vacuum degassing. Higher level is obtained at low contact forces (- ♦- 3 cN) and lower level at greater (-- 15 cN). Contamination on contact spot presummably consists of semihard insulating film*

6. Conclusions

Critical conditions, which restrict the application of Ag-base contact materials in low-power switching, are determined primary by the nature and degree of contamination on contact surface. Chemical composition of bulk contact has no significant influence on contact reliability at low-power switching.

Contact resistance of properly cleaned contacts is low and stable even at extremely low contact forces down to few cN.

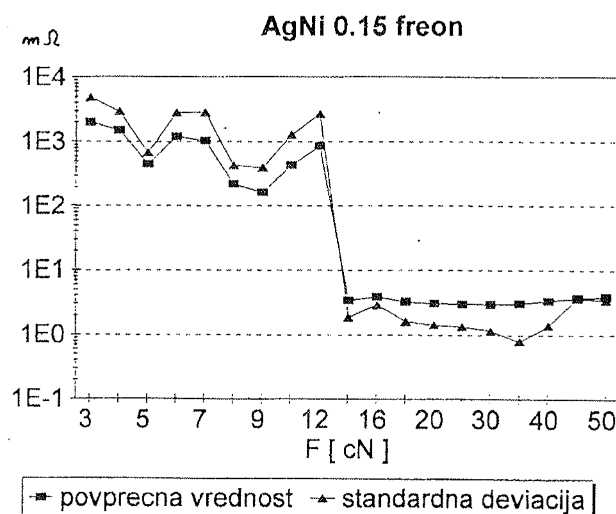

Fig. 8a: Critical contact force providing reliable switching can be estimated from graphs as shown on these plots. Insufficiently cleaned contacts reveal high and unstable contact resistance up to approx. 15 cN.

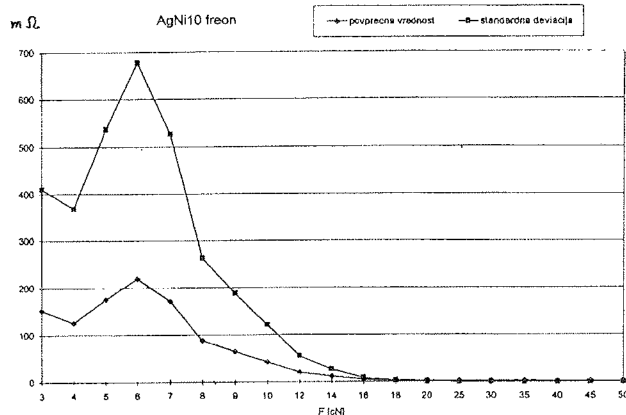

Fig. 8b: *Critical contact force providing reliable switching can be estimated from graphs as shown on these plots. Insufficiently cleaned contacts reveal high and unstable contact resistance up to approx. 15 cN.*

By comparing various cleaning methods cleanning in RF hydrogen plasma gives us best result, when parameters of the process ensure us apropriate cleaning effect. Standard application of chloro-fluoro-carbons is less successive even at very carefully performed cleaning. CFC agents are also ecologicaly unacceptable. Vacuum degassing is also not succesfull method of cleaning, because contamination films do not consists only of easily evaporating substances. This process presummably solidifies contamination films, therefore higher contact forces is required to achieve low and stable contact resistance, which can be estimated from graphs of Fig. 8.

Results of our present research indicate no detrimental influence on significant increase of contact resistance, when properly cleaned contacts have been exposed to moderate dusty or slightly sulphurizing ambient atmosphere for few days or even a week.

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THIN FILM HUMIDITY SENSOR BASED ON POROUS TITANIA

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Key words: humidity sensor, thin-film sensors, RH, Relative Humidity, TiO_2 porous titanium dioxide, electrical properties, sol-gel method, morphology

Abstract: The effect of introducing pores in undoped and potassium doped TiO_2 thin films on their humidity sensing characteristics was studied. Films were prepared by the sol-gel technique. Different potassium compounds were used to introduce potassium ions into the sols that were used for preparation of samples. The influence of these compounds and of the film firing temperature on sample morphology, and on the electrical properties of TiO_2 thin films were also studied. Introduction of the porosity in thin films had a positive effect on the humidity sensing characteristics of the samples. Sol-gel processed, porous, and 10 at% potassium doped TiO_2 thin films heated to 450°C exhibited an outstanding humidity sensitivity over the entire RH range.

Tenkoplastni senzor vlage na osnovi poroznega titanovega dioksida

Ključne besede: senzorji vlage, senzorji tankoplastni, RH vlaga relativna, TiO_2 titanov dioksid porozni, lastnosti električne, postopki sol-gel, morfologija

Povzetek: V članku so predstavljeni senzorski elementi za zaznavanje relativne vlažnosti zraka na osnovi s kalijem dopiranih in nedopiranih TiO_2 tankih filmov. Predstavljen je tudi način, kako v tanek film lahko vpeljemo poroznost in kako le ta vpliva na njegove senzorske lastnosti. Filmi so bili pripravljeni s pomočjo sol-gel procesa. Različne kalijeve spojine so bile uporabljene kot dodatek k solom za pripravo tankih filmov. Študirali smo vpliv teh spojin in temperature žganja na morfologijo in električne lastnosti TiO_2 tankih filmov. S kalijem dopirani TiO_2 tanki filmi, ki so bili žgani pri 450°C in ki so bili pripravljeni s pomočjo sol-gel postopka, so imeli odlično občutljivost na spremembo relativne zračne vlage. Rezultati so pokazali, da poroznost pozitivno vpliva na občutljivost teh vzorcev.

Introduction

The trend towards automated control systems for environmental monitoring and miniaturisation requirements for on chip integration of sensors is the driving force for development of integrated humidity sensors /1, 2/. The final target is the development of intelligent system that will be easy to operate and have microprocessor-compatible read-outs. However, not only the electronics but also the materials technology is fundamentally important in improving research and development on humidity sensors. A complete understanding of the material's characteristics and of its sensing mechanism, using prototypes, is needed for the further development of advanced devices. In the field of humidity sensors, several attempts have been made to integrate a humidity sensor on silicon microchips, along with all electronics needed for a practical device. Both polymeric /3/ and ceramic films /4/ have been investigated as humidity sensitive elements.

Today, most commercially available humidity sensors are based on polymeric films /5/, in spite of the fact that ceramic humidity sensors exhibit better chemical resistance and mechanical strength than polymeric sensors / 6/. This situation is a consequence of the high costs that are incurred during the production of ceramic humidity sensors based on porous sintered oxides /1, 7/, because of the use of conventional ceramic technology. For that reason less costly manufacturing technology for miniature ceramic sensing elements is needed. Recently, films prepared by sol-gel methods were studied /8, 9/ as humidity sensing devices. This chemical technique offers a very promising feature, namely, the possibility of powder-free processing of ceramics in their final shape (films or fibres), which can be used as active elements in sensing devices /10/.

That is probably one of the reasons that several authors studied the suitability of sol-gel processed TiO_2-based thin films for humidity sensors / 8, 9, 11, 12/. Titania was used as a sensing material because very interesting results have been reported for sintered porous compacts and thick films of titania and doped titania-based humidity sensors /13, 14, 15, 16, 17/. In the literature it was considered that a large pore volume and control of the pore size distribution are necessary for high humidity sensitivity of ceramic materials /7, 18/. For this reason it is interesting that an outstanding humidity sensitivity over the entire RH (relative humidity) range has been

reported in dense, pore-free thin films /12/. Such a high response of sol-gel processed K-doped TiO_2 films has also rarely been observed for porous sintered ceramics. It is known that addition of alkali ions is effective in increasing the RH sensitivity of several ceramic oxides by affecting the sinterability of the material in pellet form /15/, decreasing the intrinsic resistance of the material /19/, or increasing the number of adsorption sites /20/. However, measurements performed by the authors /8, 12/ indicated a humidity sensing mechanism that is different from that generally accepted for porous ceramics This mechanism involves the direct participation of alkali ions in conduction during the exposure of the sensing material to a humid environment / 8/.

In this study the influence of the introduction of pores in undoped and potassium doped TiO_2 thin film on their sensing characteristics is studied. Different potassium compounds were used for introduction of potassium ions to the sols that were used for preparation of samples. The influence of these compounds on the morphology and on the electrical properties of TiO_2 thin films were also studied.

Experimental

Doped and undoped TiO_2 thin films were prepared by the sol-gel technique. Precursor solutions for production of porous TiO_2 coatings were prepared by a slightly modified method reported by Kato et al. /21, 22/. Titanium tetraisopropoxide $Ti(OPr^i)_4$, diethanolamine, and ethanol were mixed and stirred in a nitrogen glove box to prepare a homogenous solution. For preparation of doped TiO_2 films 10 at % of K was added to the solution. Three different compounds were used for doping of the sols: potassium nitrate (KNO_3), potassium acetate ($KOOCCH_3$), or potassium ethoxide (KOC_2H_5). Afterwards water diluted with ethanol was mixed into the solution. The water/alkoxide molar ratio was 1.

Polyethylene glycol (PEG), molecular weight 1800-2200, was used as a pore former /21/ in several samples. In order to evaluate the influence of the concentration of the pore former on the porosity, the amount of PEG was varied between 2 and 4 wt. %. A summary of the samples prepared is presented in Table 1.

Silicon wafers and alumina plates were used as support substrates. For electrical measurements, prototype sensors were prepared by depositing TiO_2-based films on alumina substrates with comb-type Au electrodes. The films were deposited from the solutions by the spin coating technique, using a rotation speed of 3000 RPM. Gel coatings were dried at 100°C and fired at 650°C for 1 hour /21/. Samples were also fired at 450°C for 2 hours in order to evaluate the influence of firing temperature on the sensing characteristics of TiO_2 thin films. The thickness of the TiO_2 coating was increased by repeating the cycle from spinning to firing.

The morphology of the coatings was examined by scanning electron microscopy (SEM, JEOL JXA-840A). The humidity sensitive electrical properties of the thin films were evaluated using an impedance analyser (HP 4192A LF). An environment varying relative humidity (RH), ranging from 15 to 95 % at 25°C was obtained using an environmental chamber (Weiss SB1 160).

Table 1: Summary of prepared samples

	Pore former	
potassium dopant	PEG added	No PEG added
KNO_3	KN/Px.x*	KN
$KOOCCH_3$	KA/Px.x*	KA
KOC_2H_5	KE/Px.x*	KE
No K^+ added	NK/Px.x*	NK

x.x represents the wt. % of PEG added. Example: KN/P2.4, sample with KNO_3, and 2.4 wt. % of PEG added to the sol.

Results and discussion

Figs 1 and 2 show scanning electron micrographs of the undoped, and potassium doped TiO_2 coatings prepared from the precursor solutions.

The TiO_2 coating prepared from the solution without addition of polyethylene glycol (NK/P0.0, Fig.1A) had almost no visible texture. Addition of 2.4 wt. % of PEG to undoped titanium tetraisopropoxide (TTIP) sols yielded thin films (NK/P2.4) with a porous microstructure (Fig. 1B). Pores were from 100 to approximately 270 nm in diameter. The sample morphology was slightly different from the morphology of thin films reported in the literature /21/ but this difference can probably be ascribed to the different coating technique used.

The influence of the addition of potassium compounds to the TTIP sol on the microstructure of the TiO_2 thin film is presented in Fig. 2. The amount of potassium compound ($KOOCCH_3$, KNO_3) added was calculated to yield 10 at. % of potassium ions with respect to titanium ions.

Fig 2A show the morphology of a KA/P2.4 sample (potassium acetate and 2.4% of PEG added to the TTIP sol) fired at 650°C for 1 hour. There was no difference in morphology between samples without addition of PEG (KA/P0.0) and samples with 2.4 wt. % of PEG added (KA/P2.4). Both samples had microstructures almost identical to the fine granular microstructure of the sample KN/P0.0 (KNO_3 added, no PEG added) that were fired at 650°C for 1 hour. The samples had a grain size in the range from ~20 nm to ~100 nm (Fig 2A).

An increased concentration of pore former in the KNO_3 doped precursors (sample KN/P2.4) yielded a microstructure that is presented in Fig 2B. The sample had a grain size around 100 nm and pores in the range from ~20 nm to ~200 nm. Large cracks from 0.5 to 2 μm were also present in these samples. During the preparation of the KN/Px.x samples separation of small crystallites was observed. This was probably a consequence of the low solubility of KNO_3 in TTIP sols.

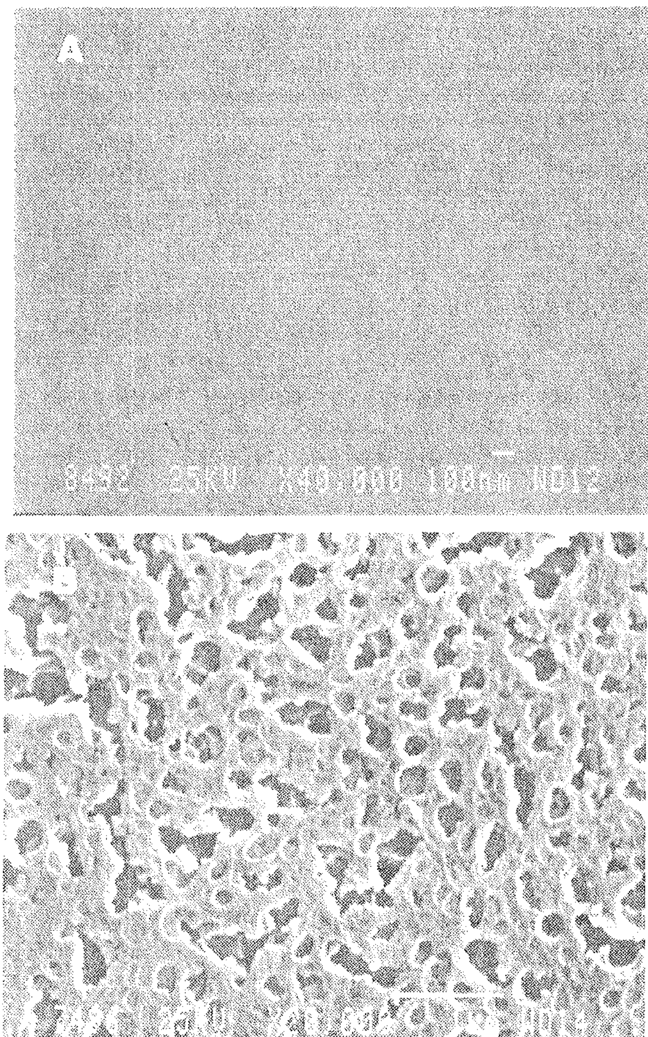

*Fig. 1: Morphology of undoped TiO_2 thin films fired at 650°C for 1 h.
A: NK/P0.0, B. NK/P2.4*

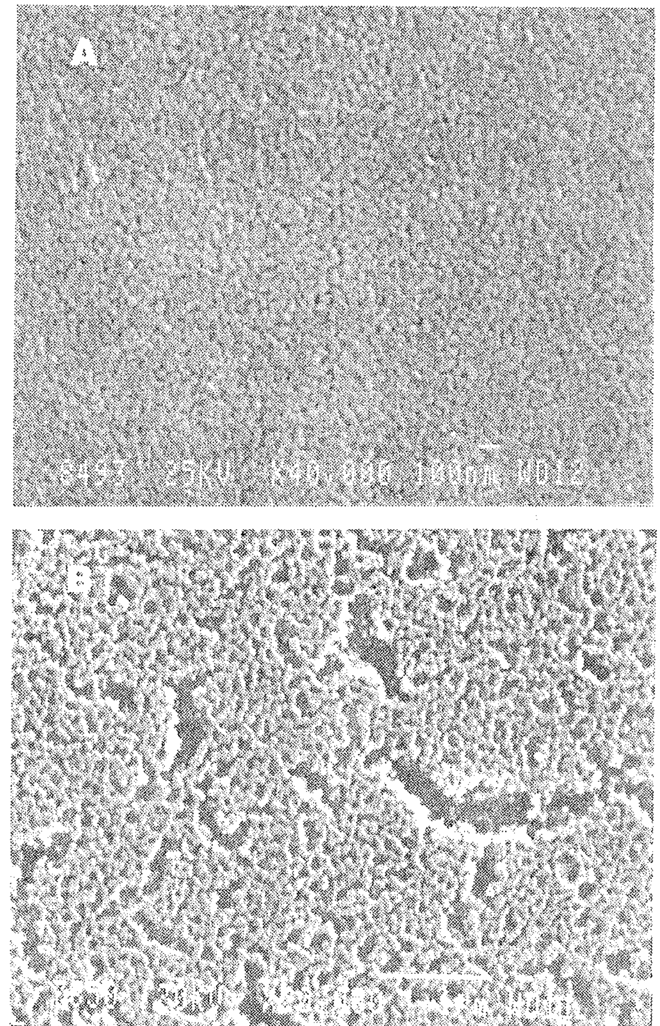

*Fig. 2: Morphology of potassium doped TiO_2 thin films fired at 650°C for 1 h. Samples were prepared from $KOOCCH_3$ and KNO_3 doped sols.
A: KA/P2.4, B. KN/P2.4*

Fig 3 show the morphology of K doped TiO_2 thin films fired at 650°C for 1 hour. Potassium ethoxide was used as precursor. The sample without PEG added (KE/P0.0) had a granular microstructure with ~100 nm grains and 10-50 nm pores (Fig 3A). There was no visible difference between the morphology of KE/P0.0 and the morphology of the KE/P2.4 sample. Both samples had some areas with larger grains and different contrast (Fig 3A). EDX analysis revealed that concentration of K ions is higher in areas of different contrast (DC) than in the rest of the coating.

Areas with different contrast could also be observed in samples where the PEG concentration was increased to 4.0 wt. % (sample KE/P4.0 at Fig 3B), but their visibility was worse. It is interesting that in spite of the fact that the PEG concentration in KE/P4.0 samples was higher than in potassium undoped (NK/P2.4) samples (Fig 1B), no pores with higher diameter developed. The microstructure was still similar to the microstructure of the KE/P0.0 sample in Fig 3A.

It can be seen from these results that introduction of potassium compounds into the TTIP sols had a profound effect on the sample morphology. First, the formation of the pores in the samples with added potassium precursors was hindered with respect to the samples without K added. Second, the potassium doped samples fired at 650°C always exhibited the granular morphology whereas the undoped samples fired at same temperature (Fig. 1) had almost no granular texture.

Samples prepared from TTIP sols based on potassium ethoxide precursor, were selected to evaluate the influence of firing on the morphology and electrical properties of the thin films. Samples KE/P0.0 and KE/P4.0 were fired at 450°C for 2 hours (Fig 4). TiO_2 thin films without added pore former (KE/P0.0) had no visible texture (Fig 4A). TiO_2 coatings prepared from the precursor solution with PEG added (sample KE/P4.0) developed a different microstructure. As can be seen from the micrograph in Fig 4B, there were fine pores in the coating. The pores

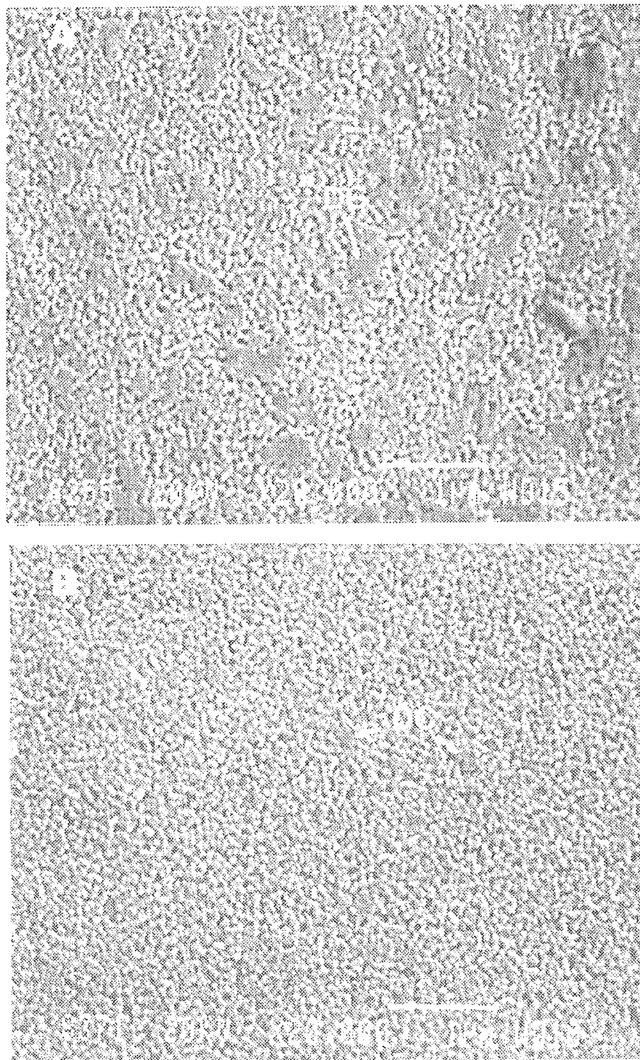

Fig. 3: *Morphology of potassium doped TiO_2 thin films fired at 650 °C for 1 h. Samples were prepared from KOC_2H_5 doped sols. A. KE/P0.0, B. KE/P4.0*

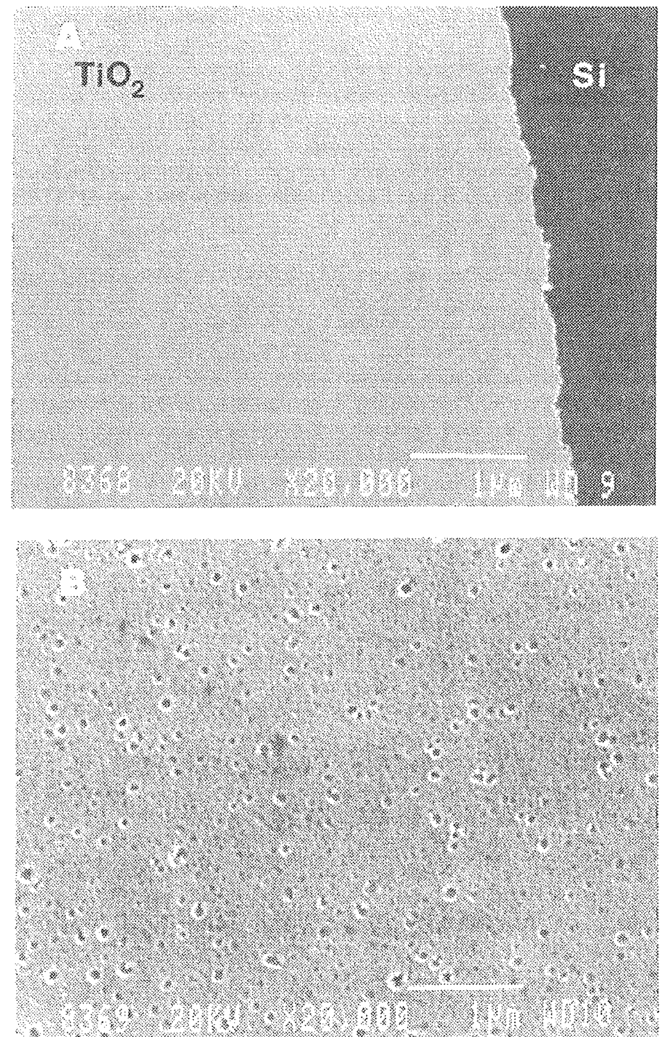

Fig. 4: *Morphology of KE/P0.0 and KE/P4.0 samples fired at 450°C for 2 h. A. KE/P0.0, B. KE/P4.0*

were ~30 to ~100 nanometres in diameter. No areas of different contrast could be observed in these samples.

Electrical measurements proved that potassium nitrate was unsuitable for sample doping due to the low solubility of KNO_3 in the TTIP sols. For this reason the potassium concentration in the TiO_2 thin films doped with this compound was under 10 at. % (with respect to Ti), and as a consequence /12, 15, 19, 20/ KN/P0.0 and KN/P2.4 samples were poorly sensitive to changes of relative humidity (RH).

Fig 5 show the dependence of the capacitance of potassium doped TiO_2 thin films at 200 Hz and 25°C. Samples KE/P0.0 and KE/P4.0, fired at 650°C for 1 hour, exhibit a change of capacitance only at high RH. The sensitivity of the samples to change of RH increased with addition of pore former (sample KE/P4.0) only for a relative humidity over 70 %.

The capacitance change for samples KE/P0.0 and KE/P4.0 fired at 450°C was 4 orders of magnitude between 15 and 90 % RH. Sample prepared from precursors with an increased concentration of PEG (KE/P4.0) had higher sensitivity in the range from 15 to 45 % RH than the KE/P0.0 sample. From 45 % RH, sensitivity of the KE/P4.0 sample decreased, and in the range from 50 to 95 % RH followed the sensitivity of the KE/P0.0 sample at higher capacitance level.

On the one hand, the dramatic increase of sensitivity with decreased firing temperature could be explained by a coarsening of the microstructure at 650°C. At that temperature grains of TiO_2 are already well formed. Grains are also connected with necks (Fig 3), in contrast to the sample films fired at 450°C (Fig 4) which show no grain morphology in SEM observations. It has been shown that formation of grain boundaries and ordering of the crystalline structure is able to block ionic conduction within the material / 8, 9/. The authors /8/ showed that the free movement of alkali ions is necessary for exceptional conductivity of K doped TiO_2 thin films. The decrease of sensitivity could probably be also connected with the potassium segregation that can be

observed in the samples fired at 650°C (Fig 3). Such segregation is not yet well understood, and further investigations are needed to explain it.

On the other hand, samples fired at 450°C show an exceptional change of capacitance in the entire RH range. This change could also be related to the increased number of water adsorption sites, due to the formation of a higher number of surface defect sites /1, 20/.

The presence of small pores in the KE/P4.0 sample fired at 450°C is probably responsible for the higher sensitivity of the thin film at lower relative humidity (below 45% RH) compared to the KE/P0.0 sample which was fired at the same temperature, and that has no visible porosity. Formation of grains and further coarsening of the sample microstructure (KE/P4.0) at 650°C probably resulted in the disappearance of the porosity that can be observed in Fig 4B. In any case, the porosity of the KE/P4.0 sample sintered at 650°C was still higher than the porosity of the KE/0.0 sample sintered at same temperature, and that probably resulted in higher sample sensitivity at a relative humidity over 70% RH.

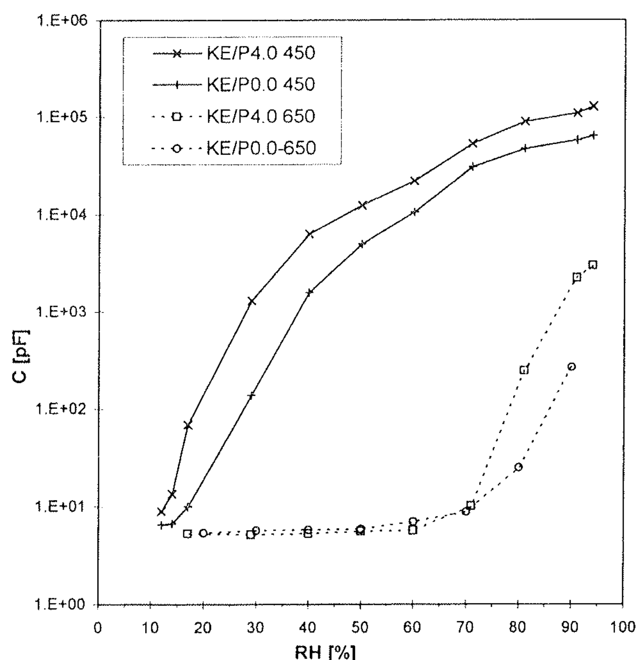

Fig. 5: The RH dependence of the capacitance of K doped thin films at 25°C. Sensors fired at 650°C for 1 h and at 450°C for 2 h. The frequency of the applied filed was 200 Hz.

Conclusions

Porous potassium doped and undoped TiO_2 thin films were prepared from alkoxide solutions by the spinning technique. The results showed that the formation of pores in the samples prepared from TTIP sols with potassium precursors added was hindered with respect to the samples prepared from TTIP sols without added potassium precursors.

Introduction of porosity in thin films had a positive effect on the humidity sensing characteristics of the potassium doped samples. Sol-gel processed, porous, and 10 at % potassium doped TiO_2 thin films heated to 450°C show an outstanding humidity sensitivity over the entire RH range. The change of capacitance was 4 orders of magnitude in the range from 15 to 95% RH.

Acknowledgements

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MIEL-SD'96 CONFERENCE PRESENTATION OF LABORATORIES, ENTERPRISES AND SPONSORS

KONFERENCA MIEL-SD'96 PREDSTAVITVE LABORATORIJEV, PODJETIJ IN SPONZORJEV

Iskra Avtoelektrika The Leading Manufacturer of D.C. Motors and Electronic Controllers

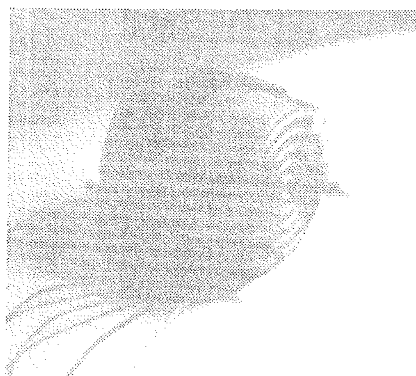
D.C. motors and controllers for battery supplied transport vehicles are becoming more and more important range of Iskra products.

Last year we added to this programme by transferring the production from the Bosch company. So Iskra has become the leading manufacturer of D.C. motors and electronic controllers in Europe.

The entire range of products is designed for exports. The buyers of these products are the reputable manufacturers of fork-lifts and electrohydraulic components, namely STILL, LINDE, JUNGHEINRICH, STEINBOCK, ATLET, FIAT OM, WAGNER, FENNER, SMITHS, SHIMADZU...

This range of products includes:

- Electronic controllers in thyristor technology
- Electronic controllers in MOSFET technology
- Broad selection of D.C. motors for electrohydraulic generator sets of the power from 100 W to 12 kW and the voltage from 12 V to 80 V
- Traction motors and drive systems within the range of voltage from 12 V to 80 V and the power up to 12 kW
- New generation of D.C. contactless motors

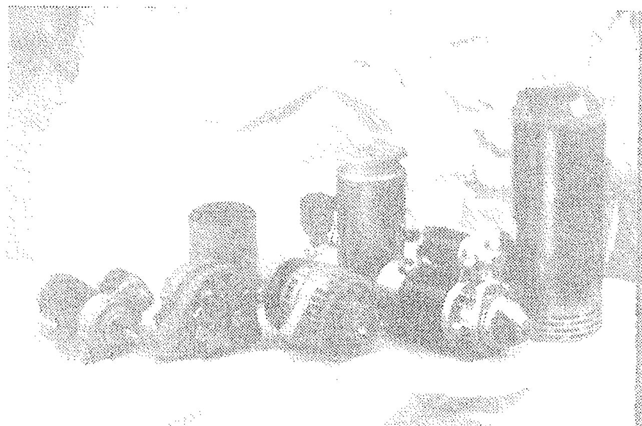


A CONTACTLESS MOTOR

In the field of automotive electricity we have updated the technology of our range of products by introducing a new generation of reduction gear starters.

They are designed for starting diesel motors from 2000 ccm to 8000 ccm. The advantages of these starters are:

- Higher quality and reliability,
- Longer life,
- Ecologically friendly products,
- Smaller dimensions and weight,
- Higher specific power and lower current consumption.



Other products:

- STARTERS FOR PASSENGER CARS
  12 V 0.9 kW to 1.7 kW
- STARTERS FOR COMMERCIAL VEHICLES
  12 V 1.8 kW to 4 kW
  24 V 3.2 kW to 6.5 kW
- ALTERNATORS
  As regards their nominal voltage and output current, the alternators are manufactured in the following versions:
  14 V 30 A to 95 A, 28 V 27 A to 180 A
- Electronic, electromechanical relays

Iskra Avtoelektrika
Vodilni proizvajalec enosmernih motorjev in elektronskih krmilnikov

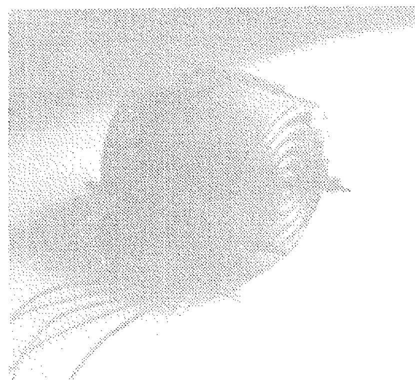
Enosmerni motorji in krmilja za baterijsko napajana transportna sredstva so vse pomembnejši proizvodni program Iskre.

V lanskem letu smo ta program dopolnili še s prenosom proizvodnje iz firme Bosch. Tako je postala Iskra vodilni proizvajalec enosmernih motorjev in elektronskih krmilnikov v evropskem prostoru.

Proizvodni program je v celoti usmerjen v izvoz. Med kupci tega programa nastopajo renomirani proizvajalci viličarjev in elektrohidravličnih komponent, kot so STILL, LINDE, JUNGHEINRICH, STEINBOCK, ATLET, FIAT OM, WAGNER, FENNER, SMITHS, SHIMADZU...

V okviru tega proizvodnega programa nudimo:

- Elektronska krmilja v tiristorski tehnologiji
- Elektronska krmilja v MOSFET tehnologiji
- Širok izbor enosmernih motorjev za elektrohidravlične agregate moči od 100 W do 12 kW in napetosti 12 V do 80 V
- Vozne motorje in pogonske sisteme v napetostnem območju 12 V do 80 V in moči do 12 kW
- Novo družino enosmernih brezkontaktnih motorjev

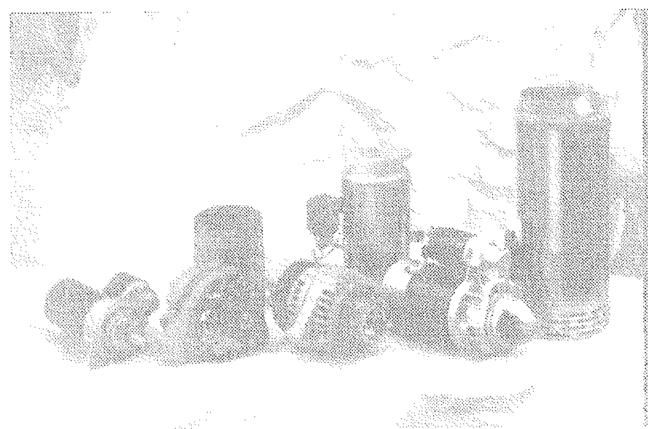


BREZKONTAKTNI MOTOR

Na področju avtoelektrike pa smo tehnološko posodobili program z novo družino zaganjalnikov z reduktorjem.

Namenjeni so za zagon diesel motorjev od 2000 ccm do 8000 ccm. Prednosti teh zaganjalnikov so:

- višja kakovost in zanesljivosti,
- daljša življenska doba,
- ekološka neoporečnost,
- manjše dimenzije in masa,
- višja specifična moč in nižja poraba toka.



Ostali programi:

- ZAGANJALNIKI ZA OSEBNA VOZILA
  12 V 0,9 kW - 1,7 kW
- ZAGANJALNIKI ZA GOSPODARSKA VOZILA
  12 V 1,8 kW - 3,6 kW
  24 V 3,2 kW - 6,5 kW
- ALTERNATORJI
  Glede na nazivno napetost in izhodni tok se alternatorji proizvajajo v izvedbah:
  14 V 30A -95A, 28 V 27A -180A
- elektronski, elektromehanski releji

IMEC, Leuven, Belgium
(from 1995 Annual Report)

Foreword to 1995 IMEC ANNUAL REPORT

The importance of electronics is reflected in the fact that this industrial sector is growing twice as fast as any other. For microelectronics wich is the heart of this evolution, the turnover for the period 1996-2000 looks set to increase by approximately 20% per annum. That figure should come as no surprise, considering the increasing use of electronics and micro-electronics in almost every aspect of modern life.

This growth will be based on a wide range of new fabs for integrated circuits and on a rapid expansion of the design capacity. Technological evolution will also require a sustained R & D drive. This development will of course depend on the availability of specialists with the right skills. As a research centre in the field of microelectronics, IMEC makes an appreciable contribution to the training of these specialists.

The following points bear this out:

- 100 students carry out their course-requirement scientific research for their PhD degree papers at IMEC;
- every year, some 50 students visit IMEC to write their theses for their master's degree;
- IMEC's personnel throughflow is approximately 16% p.a.;
- over 100 seminars are organized each year, many of which can now be followed in our teleclassing programme;
- IMEC's advanced CAD tools aid the education of designers of integrated circuits at 13 Higher Polytechnic Schools and three universities in Flanders. Each year more new designers swell the ranks;
- as IMEC co-operates with the three Flemish universities, much of the research run by their departments of electronics, physics and chemistry is relevant to microelectronics. Also, specialists are trained in their laboratories;
- taking into account the foreign graduate students, the industrial residents and staff in the context of affiliation programmes, IMEC has 30 different nationalicies.

The availability of these specialists, and the existence of well- equipped science parks and industrial plants, make Flanders an attractive prospect for the creation of R&D laboratories, design houses and industrial product lines. This initiative in microelectronics is part of the Flemish government's strategy for information technology, which also means there is a solid framework of support measures.

1995 will go down as an outstanding year for IMEC, marked by the foundation of our 8th spinoff company, increasing international co-operation, intensification of our inter-university work, interactive research with 37 companies throughout Flanders, the publication of approximately 200 scientific articles in periodicals, and the presentation of more than 300 contributions at international conferences.

Together with our staff of some 600, we look to the future with confidence.

R. Van Overstraeten, President

Figures

Research valorization

Evolution of revenue from contract research

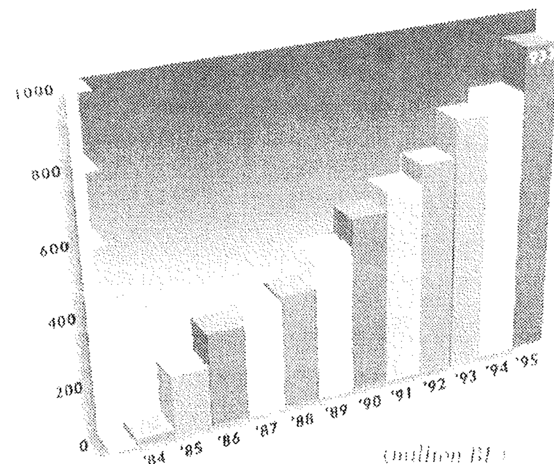
The year under review was characterized by continued growth of total revenue from contract research from BEF 801 million/US $ 22 million (excluding sundries) in 1994 to BEF 933.4 million/US $ 26 million (excluding sundries) in 1995, which represents an increase of 16% on 1994.

Revenue from Flemish industry took a sharp upturn, both in absolute figures (a BEF 120 million/US $ 3.3 million increase on 1994 to BEF 385 million/US $ 10.6 million) and in terms of relative share (41% of total research revenue as against 33% for 1994 and 32% for 1993). In 1995, revenue from Flemish industry increased by 45% in relation to the figures for 1994. IMEC cooperated with 37 Flemish companies. The role of the IWT (Institute for the promotion of Scientific and Technological Research in the Industry) was to act as an important catalyst.

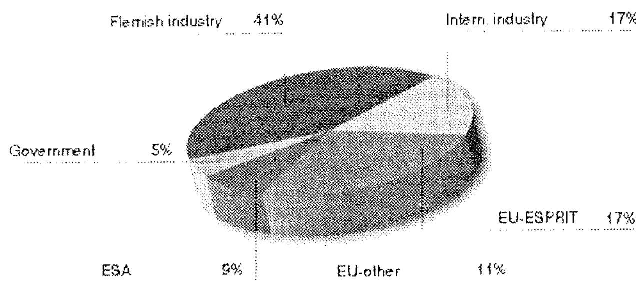
The share of contract revenue coming from bilateral industrial interaction outside Flanders likewise showed vigorous growth, from BEF 94 million/US $ 2.6 million (1994) to BEF 158 million/US $ 4.4 million (1995).

In all, bilateral industrial operations have therefore evolved from BEF 359 million/US $ 10 million (1994) to BEF 543 million/US $ 15 million (1995).

Receipts from ESA increased nearly 11% (from BEF 74 million/ US $ 2 million to BEF 82 million/US $ 2.3 million) which, allowing for the difficult reorganization phase in ESTEC, is a good result.



Sources of revenues from contract research



Personnel

In the course of 1995, the payroll grew from 450 to 476 staff members (+5.8%). In addition, IMEC also continues to attract a considerable number of guest researchers; their number rose 22% to 115, bringing the total number of IMEC employees to 591. 86% of these are directly employed in R&D. In this way IMEC strives to direct its efforts as far as possible towards research.

Further evidence is provided by the large number of PhD students (17% of the total workforce). With 17% of its workforce made up by foreign employees from 30 different countries, IMEC has a decidedly international character. The combination of advanced education, young age, easy; informal working relationships and businesslike approach makes IMEC a particularly stimulating environment in which to work.

Levels of Education

IMEC staff members are highly educated. 75% will usually have pursued their studies to university level (university graduates and industrial engineers).

- university: 64 %
- higher polytechnic school: 11 % non-university
- higher education: 10 %
- secondary school: 15 %

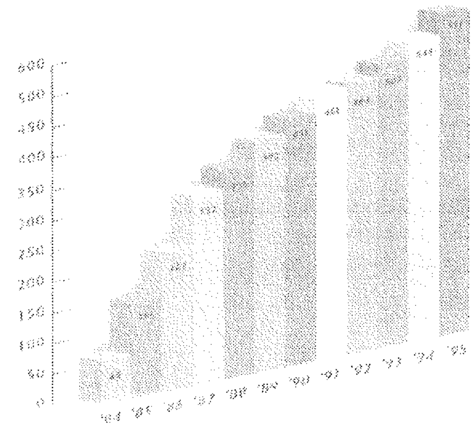
PhDs in the scientific departments

Basic research continues to be of crucial importance to IMEC. This is reflected in the large number of employees preparing for their doctorate

- R & D staff: 69%
- PhDs: 18%
- Technical and logistics staff: 13%

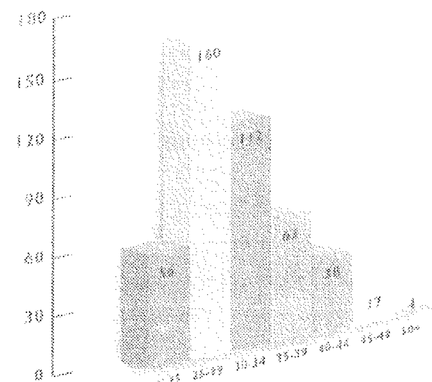
Growth of employment level

The tocal number of employees increased by 8.6% during 1995. A further 19% can be added to that figure to account for the guest researchers. They come from the academic world as well as from industry:



Age

IMEC is a young company, and wishes to stay that way. It seeks to strike a balance between purposeful renewal on the one hand and holding on to the necessary expertise on the other. The average age in the company is 31 years.



MIEL-SD'96 KONFERENCA - POROČILO
MIEL-SD'96 CONFERENCE - REPORT

24. Mednarodna konferenca o mikroelektroniki, MIEL'96
32. Simpozij o elektronskih sestavnih delih in materialih, SD'96

25.9.96 - 27.9.96, Nova Gorica, Slovenija

Štiriindvajseta mednarodna konferenca o mikroelektroniki, MIEL'96 nadaljuje tradicijo mednarodnih konferenc, ki jih vsako leto prireja MIDEM - Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale. Že petič zapored je ta konferenca potekala skupaj s tokrat dvaintridesetim Simpozijem o elektronskih sestavnih delih in materialih, SD'96.

Oba dogodka nudita priložnost mnogim strokovnjakom širom Evrope, da predstavijo svoje delo in najnovejše rezultate, kakor tudi da izmenjajo izkušnje s svojimi kolegi. Rdeča nit konference je ostala možnost druženja, povezovanja in graditve prijateljstva med strokovnjaki s tega področja.

Obe konferenci sta znani tudi zaradi udeležbe priznanih povabljenih referentov.

Letos smo imeli priliko poslušati A. Lechnerja, Siemens, München, Nemčija, čigar referat "Inovativna pametna močnostna integrirana vezja za uporabo v avtoelektroniki" je podal pregled nad prednostmi pametnih močnostnih integriranih vezij na siliciju s posebnim poudarkom na uporabi v avtoelektroniki. Naslednji povabljeni referent, W. Petasch iz firme Technics Plasma, München, Nemčija, je v referatu "Uporaba nizkotlačnih plazemskih procesov v mikroelektroniki" opisal uporabo plazemskih procesov v mikroelektroniki, proizvodnji hibridnih vezij in v novi Dycostrate tehnologiji za izdelavo fleksibilnih tiskanih plošč. V. Lantto, Univerza Oulu iz Finske, je v prispevku "Plinski senzorji - primer razvoja debeloplastnih pretvornikov" pregledno opisal različne tehnologije tiskanja debeloplastnih plasti pri izdelavi večplastnih pretvorniških struktur. G. Soncini, IRST, Trento, Italija, je v prispevku z naslovom "Kemični senzorji na osnovi ISFET pretvornikov" podal trenutno stanje in trende razvoja kemičnih senzorjev na osnovi FET tranzistorjev integriranih na siliciju. C. Claeys, IMEC, Leuven, Belgija, je v prispevku "Tehnološki izzivi za tehnologije na siliciju" orisal trenutno stanje in nove zahteve za tehnologije na siliciju, predvsem s stališča povečane funkcionalnosti, oz. zahtev za novo tehnologijo v smislu obdelave mešanih signalov, nizke napajalne napetosti, nizke delovne napetosti in pametnih funkcij. Bui Ai, LGET/CNRS, Toulouse, Francija, je v referatu "Varistorji na osnovi cinkovega oksida in zaščita vezij - trenutno stanje" podal zgodovinski pregled nad raziskavami in tehnologijo cink oksidnih varistorjev od leta 1960 dalje. V prispevku "PZT tanke plasti za mikro senzorje in aktivatorje" je P. Muralt, EPFL, Lausanne, Švica, opisal nanos, integracijo, izdelavo in uporabo PZT tankih plasti. V zadnjem vabljenem referatu, ki ga je podal G. Dražič, IJS, Ljubljana, Slovenija, "Analitična elektronska mikroskopija sodobnih keramičnih materialov" smo spoznali analitično elektronsko mikroskopijo kot izredno uporabno tehniko za raziskave sodobnih keramičnih materialov predvsem zaradi majhne analizne prostornine in hkratnega opazovanja strukture, strukturnih odnosov med fazami in kemične sestave.

Zbornik referatov, ki smo ga izdali, obsega 446 strani in je razdeljen v več delov, podobno kot je bila razdeljena konferenca in sicer MIEL sekcije: Integrirana vezja, Tehnologija in komponente, Modeliranje in fizika polprevodnikov, Optoelektronika in SD sekcije: Tankoplastna tehnologija, Debeloplastna tehnologija, Keramika, kovine in kompozitni materiali.

Ponovno letos je bila posebna sekcija posvečena predstavitvi podjetij, raziskovalnih laboratorijev za mikroelektroniko in elektronske materiale ter konferenčnih sponzorjev. Namen predstavitve je bil seznaniti širši krog poslušalcev z delom in možnostmi, ki jih nudijo različne raziskovalne skupine in firme. Same predstavitve niso tiskane v zborniku, vendar jih objavljamo v tej številki revije "Informacije MIDEM".

Konferenca je potekala od 25. do 27. septembra 1996 v hotelu HIT HOTEL CASINO PERLA v Novi Gorici. Poleg izvrstnih konferenčnih zmogljivosti hotela, ki jih nudijo organizatorjem konferenc, sta vodstvo in osebje hotelskega kompleksa s svojo prizadevnostjo pripomogla k uspehu konference.

Še nekaj suhoparnih podatkov:

- na konferenci je bilo predstavljenih 57 referatov
- celotno število udeležencev konference je bilo 77 in sicer po državah:

  Slovenija: 57
  Italija: 5
  Nemčija: 3
  Švica: 2
  Avstrija: 4
  Belgija: 1
  Madžarska: 3
  Francija: 1
  Finska: 1

Konferenčni pogoji so bili odlični, sam potek konference in njen strokovni nivo visok, število udeležencev in referatov zadovoljivo, pa tudi 14% udeležba strokovnjakov iz industrije ni bila zanemarljivo majhna.

Iztok Šorli

24th International Conference on Microelectronics MIEL'96 32nd Symposium on Devices and Materials SD'96

25.9.96 - 27.9.96, Nova Gorica, Slovenia

The 24th Conference on Microelectronics MIEL'96 continued the tradition of the annual international conferences organized by MIDEM, Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia. For the fifth time, the Conference was organized jointly with the 32nd Symposium on Devices and Materials, SD'96, another annual meeting of the same Society. Traditionally, these conferences have provided an opportunity for experts from all over the Europe to meet and discuss new developments in the fields covered by the Conference. The goal of connection and building of the friendship among the scientists and their companies remained the keystone of the organizer.

As well, the Conference has always attracted distinguished guest speakers.

This time we had the opportunity to meet A. Lechner, from Siemens Semiconductor Division in Munich, Germany, whose paper "Innovative Smart Power Semiconductors for Automotive Applications" gave an overview of the manifold benefits of smart power semiconductors and over silicon and assembly technologies. Next guest speaker, W. Petasch from Technics Plasma in Kirchheim bei Munich, Germany, in the paper "Low Pressure Plasma Processing in Microelectronics" dealt with the application of low pressure plasma technology in microelectronics, in production of hybrid circuits and in new Dycostrate technology which replaces old PCB technology. V. Lantto, University of Oulu, Finland, in the paper "Gas Sensors as an Example of Research with Thick Film Transducers" overviewed different thick film printing techniques in the coarse of making multilayer transducer structures. G. Soncini from IRST, Trento, Italy, in the paper "Chemical Sensors Based on ISFET Transducers" gave an up to date overview of the status and trends of chemical sensors based on silicon integrated ion sensitive FETs. C. Claeys, IMEC, Leuven, Belgium, in "Technological Challenges for Silicon Technologies" overviewed the present status and future requirements in association with the increasing functionality added to the core CMOS based technologies, such as e.g. mixed signal, bipolar, low voltage, non volatile memories, low power and smart technologies. Bui Ai, LGET/CNRS, Toulouse, France, in his paper "Zinc Oxide Based Varistors and Parallel Circuit Protection: The State of the Art" gave historical overview of the research and the technology of zinc oxide based varistors since 1960 to this day. In the paper "PZT Thin Films for Micro Sensors and Actuators", P. Muralt, EPFL, Lausanne, Switzerland, overviewed deposition, integration, device fabrication and application of PZT thin films. Last invited paper by G. Dražič, Jožef Stefan Institute, Ljubljana, Slovenia, "Analytical Electron Microscopy of Advanced Ceramic Materials", described analytical electron microscopy as a very useful technique for the investigation of advanced ceramic materials due to a relatively small analyzed volume and simultaneous examination of structure, structural relationship among phases and chemical composition.

The Conference Proceedings which was published along with the Conference has a volume of 446 pages and is divided into several parts according to the Conference sessions such as MIEL sessions: Integrated Circuits, Technology and Devices, Device Physics and Modeling, Optoelectronics, and SD sessions: Thin Films, Ceramics, Metals and Composites, Thick Films.

Also this year, a special session devoted to presentation of microelectronics and material research laboratories, enterprises and Conference sponsors was held. The aim of the presentation was getting acquainted with the work and possibilities of different research groups, companies and their projects. These presentations are not published in the Proceedings but appear in this Journal.

The Conference was held at HIT HOTEL CASINO PERLA, Nova Gorica, Slovenia, September 25th - 27th 1996. Its excellent conference capabilities and technical as well as menagerial support brought this Conference to a successfull end.

Let me add some statistical data:

- on the Conference 57 papers were presented
- there were totally 77 participants from the following countries:

  Slovenia: 57
  Italy: 5
  Germany: 3
  Switzerland: 2
  Austria: 4
  Belgium: 1
  Hungary: 3
  France: 1
  Finland: 1

Conference conditions were excellent, scientific level of the presented articles was high, we were satisfied with total number of papers presented and participants out of which 14% came from industry.

Iztok Šorli

UDELEŽENCI KONFERENCE MIEL-SD'96
MIEL-SD'96 CONFERENCE PARTICIPANTS

	NAME	COMPANY	ADDRESS	CITY	CODE
1	ŽEMVA ANDREJ	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
2	ALJANČIČ UROŠ	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
3	AMON SLAVKO	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
4	BELAVIČ DARKO	HIPOT HYBRID	TRUBARJEVA 7	ŠENTJERNEJ	SLO-8310
5	BERNIK SLAVKO	"JOŽEF STEFAN" INSTITUTE	JAMOVA 39	LJUBLJANA	SLO-1000
6	BIZJAK MARTIN	ISKRA STIKALA	SAVSKA C. 14	KRANJ	SLO-4000
7	BLAŽIČ VOJKO	FACULTY OF ELECTRICAL ENGINEERING	VRTOJBENSKA 62	ŠEMPETER PRI GORICI	SLO-5290
8	BUI AI	LGET	118 ROUTE DE NARGONNE	CEDEX	F-31062
9	BUŠEN DUŠAN	ISKRA AVTOELEKTRIKA	VRTOJBENSKA 62	ŠEMPETER PRI GORICI	SLO-5290
10	CLAEYS COR	IMEC	KAPELDREEF 75	LEUVEN	B-3001
11	CVELBAR ANDREJ	MZT (IJS)	SLOVENSKA 50 (JAMOVA 39)	LJUBLJANA	SLO-1000
12	DRAŽIČ GORAN	"JOŽEF STEFAN" INSTITUTE	JAMOVA 39	LJUBLJANA	SLO-1000
13	FORTUNAT JULIJAN	FACILTY OF ELECTRICAL ENGINEERING	VRTOJBENSKA C.62	ŠEMPETER PRI GORICI	SLO-5290
14	FURLAN JOŽE	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
15	FURLAN JOŽE	ISKRA AVTOELEKTIKA	VRTOJBENSKA 62	ŠENPETER PRI GORICI	SLO-5290
16	GROZNIK ALEŠ	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
17	HORVATH ZSOLT J.	RESEARCH INSTITUTE FOR TECHNICAL PHYSICS	UJPEST 1, P.O.BOX 76	BUDAPEST	H-1325
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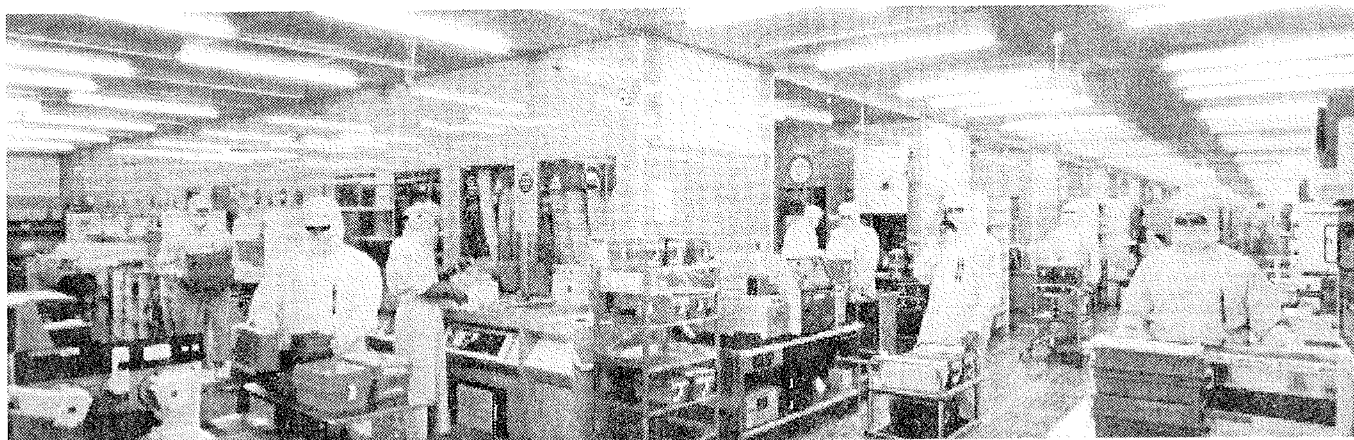
19	JENKO BOJAN	MINISTRY OF SCIENCE AND TECHNOLOGY	SLOVENSKA 50	LJUBLJANA	SLO-1000
20	KAMIN MATEJ	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
21	KLJUN IGOR	ISKRA AVTOELEKTRIKA	VRTOJBENSKA 62	ŠEMPETER PRI GORICI	SLO-5290
22	KOBE A.	FACULTY OF MECHANICAL ENGINEERING	AŠKERČEVA 6	LJUBLJANA	SLO-1000
23	KOROŠAK DEAN	FACULTY OF CIVIL ENGINEERING	SMETANOVA 17	MARIBOR	SLO-2001
24	KOSEC MARIJA	MIDEM	DUNAJSKA 40	LJUBLJANA	SLO-1000
25	KREMSER WOLFGANG	INSTITUT FUR WERKSTOFFE DER ELEKTROTECHNIK	GUSSHAUSSTRASSE 27-29	VIENNA	A-1040
26	KREN BRANE	MIKROIKS	DUNAJSKA C. 5	LJUBLJANA	SLO-1000
27	KRIŽAJ DEJAN	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
28	KUNC VINKO	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
29	KUTTNER FRANZ	SIEMENS-EZM	SIEMENSSTR. 2	VILLACH	A-9500
30	KUŠČER DANJELA	"JOŽEF STEFAN" INSTITUTE	JAMOVA 39	LJUBLJANA	SLO-1000
31	LANTTO VILHO	DEPARTMENT OF ELECTRICAL ENGINEERING	LANNANMAA	OULU, FIN.	90570
32	LECHNER ALEXANDER	SIEMENS MUNICH, HL LH PE 1	BALANSTR. 73	MUNICH	D-81617
33	LIMPEL META	MIDEM	DUNAJSKA 10	LJUBLJANA	SLO-1000
34	LUSITANI ANTONIO	DUPONT	VIA VOLTA 16	COLOGNO MORZESE	I-20093
35	MALIČ BARBARA	"JOŽEF STEFAN" INSTITUTE	JAMOVA 39	LJUBLJANA	SLO-1000
36	MALOVRH JANEZ	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
37	MANDELJC MIRA	"JOŽEF STEFAN" INSTITUTE	JAMOVA 39	LJUBLJANA	SLO-1000
38	MAČEK SREČKO	"JOŽEF STEFAN" INSTITUTE	JAMOVA 39	LJUBLJANA	SLO-1000
39	MEŽNAR ŽUPANC LEA	INSTITUTE OF SURFACE ENGINEERING AND OPTOELECTRONICS	TESLOVA30	LJUBLJANA	SLO-1000
40	MOŽINA JANEZ	FACULTY OF MECHANICAL ENGINNERING	AŠKERČEVA 6	LJUBLJANA	SLO-1000
41	MRDJEN TOMO	"JUŽEF STEFAN" INSTITUTE	JAMOVA 39	LJUBLJANA	SLO-1000
42	MURALT PAUL	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	MX-D ECUBLENS	LAUSANNE	CH-1015
43	NAPOLI ETTORE	DEPARTMENT OF ELECTRONICS, UNIVERSITY OF NAPLES	VIA CLAUDIO 21	NAPLES	I-80125
44	OSTENDORF HANS-CHRISTOPH	SIEMENS CORPORATE RESEARCH AND DEVELOPMEN, DEPT. ZFE T	EP 2	MUNICH	D-81730
45	PAVLIN MARKO	HIPOT HYBRID	TRUBARJEVA 7	ŠENTJERNEJ	8310
46	PETASCH WOLFGANG	TECHNICS PLASMA GMBH	DIESELSTRASSE 22 A	KIRCHHEIM	D-85551
47	PIGNATEL GIORGIO	UNIVERSITY OF TRENTO	VIA MESIANO 77	MESIANO	I-38050
48	PISTAUER M.	SIEMENS DESIGNCENTER FOR MICROELECTRONICS	SIEMENSSTRASSE 2	VILLACH	A-9500
49	PLETERŠEK ANTON	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
50	POPOVIČ PAVLE	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
51	RAIČ DUŠAN	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
52	REICHMANN KLAUS	INSTITUTE FOR CHEMICAL TECHNOLOGY OF INORGANIC MATERIAL	STREMAYRGASSE 16	GRAZ	A-8010
53	RESNIK DRAGO	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
54	RIESZ FERENC	RESEARCH INSTITUTE FOR PHYSICS	P.O. BOX 76	BUDAPEST	H-1325
55	ROZMAN MARKO	"JOŽEF STEFAN" INSTITUTE	JAMOVA 39	LJUBLJANA	SLO-1000
56	ROČAK DUBRAVKA	"JOŽEF STEFAN" INSTITUTE	JAMOVA 39	LJUBLJANA	SLO-1000
57	ROČAK RUDOLF	MIKROIKS	DUNAJSKA 10	LJUBLJANA	SLO-1000
58	SLOKAN MILAN	MIDEM	DUNAJSKA 10	LJUBLJANA	SLO-1000
59	SLUNEČKO JAROSLAV	"JOŽEF STEFAN" INSTITUTE	JAMOVA 39	LJUBLJANA	SLO-1000
60	SMOLE FRANC	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
61	SOLAR MITJA	FACULTY OF ELECTRICAL ENGINEERING	SMETANOVA 17	MARIBOR	SLO-2000
62	SONCINI GIOVANNI	IRST	VIA MESIANO 77	MESIANO TN	I-38050
63	STARAŠINIČ SLAVKO	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
64	STRLE DRAGO	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
65	SUHADOLNIK ALOJZ	FACULTY OF MECHANICAL ENGINEERING	AŠKERČEVA 6	LJUBLJANA	SLO-1000
66	TOPIČ MARKO	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
67	TRONTELJ JANEZ	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
68	TUYEN VO VAN	RESEARCH INSTITUTE FOR TECHNICAL PHYSICS	UJPEST 1, P.O.BOX 76	BUDAPEST	H-1325
69	VALANT MATJAŽ	"JOŽEF STEFAN" INSTITUTE	JAMOVA 39	LJUBLJANA	SLO-1000
70	VANRIETVELDE G.	DUPONT ELECTRONIC MATERIALS	CHEMIN DU PAVILLON 2	GENEVA	CH
71	VECCHI MARIA CRISTINA	DIPARTIMENTO DI ELETTRONICA, UNIVERSITA DI BOLOGNA	VIALE RISORGIMENTO 2	BOLOGNA	I-40136
72	VOJTEH MOČNIK	ISKRAEMECO	SAVSKA LOKA 4	KRANJ	SLO-4000
73	VRTAČNIK DANILO	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
74	ZARNIK MARINA SANTO	HIPOT HYBRID	TRUBARJEVA 7	ŠENTJERNEJ	SLO-8310
75	ZELINKA IGOR	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	LJUBLJANA	SLO-1000
76	ŠOBA STOJAN	HIPOT HYB	TRUBARJEVA 7	ŠENTJERNEJ	SLO-1000
77	ŠORLI IZTOK	MIDEM	DUNAJSKA 10	LJUBLJANA	SLO-1000

PREDSTAVLJAMO PODJETJE Z NASLOVNICE
REPRESENT OF COMPANY FROM FRONT PAGE

The Siemens Semiconductor Plant and Microelectronic Design Center Villach, Austria



In the early 1960s Siemens first ventured into fabrication of integrated circuits, concentrating these activities in Munich, Germany. The infrastructure was already in place and, although the quantities were still small, the advantages of closeness of ressources was apparent. Balanstraße in Munich was the first production plant.

The Villach plant - a first step abroad

In 1970 Villach was the first Siemens plant to start IC production outside Germany. A wide variety of technologies have been adapted and put into volume production over the last 26 years, as the following, brief history line shows:

1969:

- Decision to start up the Villach plant
- Production of discrete semiconductors and IC packaging and assembly

1979:

- Creation of first wafer fabrication
- Establishment of the Microelectronic Design Center (EZM)

1981:

- Startup of MOS fabrication, dynamic memories, production start for micro-computer chips

1984:

- Creation of second wafer fabrication
- Startup of volume production of 256-Kbit memories

1990:

- Production of 16-bit controllers
- Startup of 1-μm CMOS process line

1991:

- Startup of bipolar production

1994:

- Transfer of bipolar production completed
- Production start for SPT devices (Smart Power Technology)

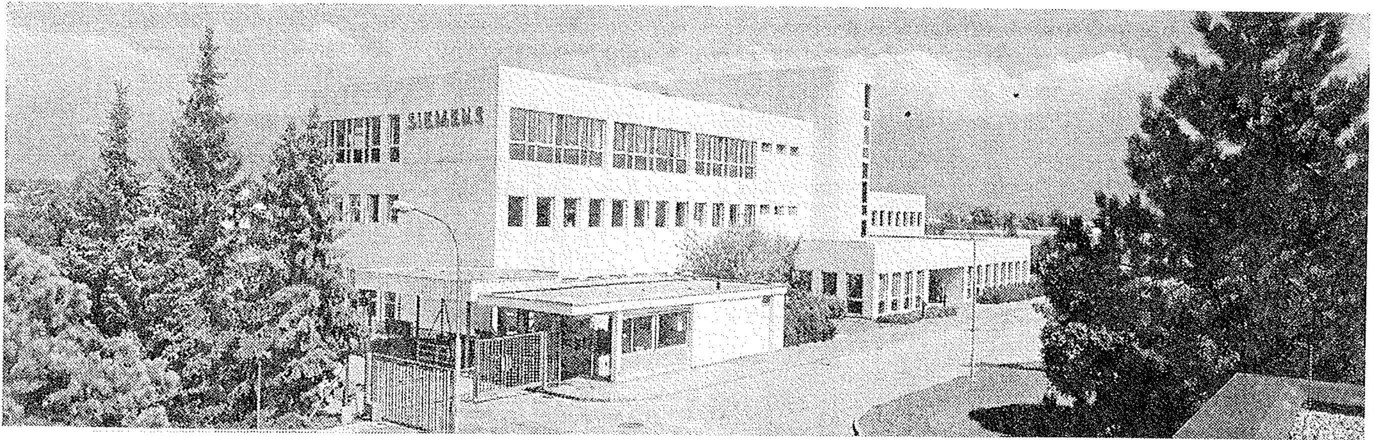
1996:

- Decision to expand R&D and production of power semiconductors involving major R&D efforts and investment of 5 billion Austrian Schillings

The long and extensive experience lead to a reliable know-how-basis for the IC- production, which is today applied mainly in the fields of automotive, consumer and industrial electronics and information technology. A close cooperation with the Siemens Microelectronic Design Center is of key importance for fast product development cycles and effective introduction to the global market.

Facts and Figures (as of 9/96)

Total area	125.000 sqm
Built-up area	25.000 sqm
Floor space	45.000 sqm
incl. cleanroom	8.000 sqm
Employees	approx. 1.650
Wafer starts/year	750.000



The Microelectronic Design Center

The Microelectronic Design Center (EZM) in Villach was founded in 1979 and nowadays represents the largest R&D potential for ICs in Austria. More than 150 highly qualified engineers work here on creating integrated circuits for the latest and emerging applications in information technology, entertainment and automotive electronics.

The following history line shows some important milestones:

1979:

- Establishment of the Microelectronic Design Center (EZM)
- First projects: mixed A/D circuits for telecom applications (Codecs, SICOFI-family).

1985:

- CMOS ADCs and analog modules for micro-controllers

1988:

- Successful volume production of mixed A/D circuits: 1 Mio. SICOFIs shipped

1989:

- First mixed A/D projects for consumer applications (TV)

1990:

- First smart power system IC projects

1992:

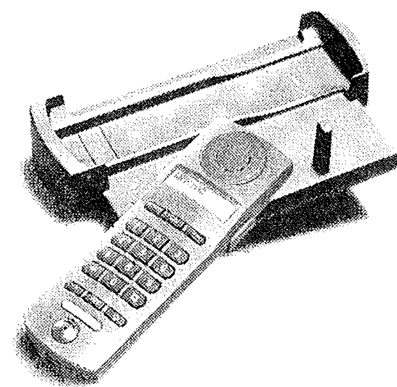
- Establishement of a technology developement group
- Start of sensor system ICs

1995:

- Mixed Signal designs for multimedia applications
- 70 Mio. telephone lines, 30 Mio. ABS- and airbag-systems, 15 Mio. TV sets in the worldmarket are already equipped with chips from Villach.

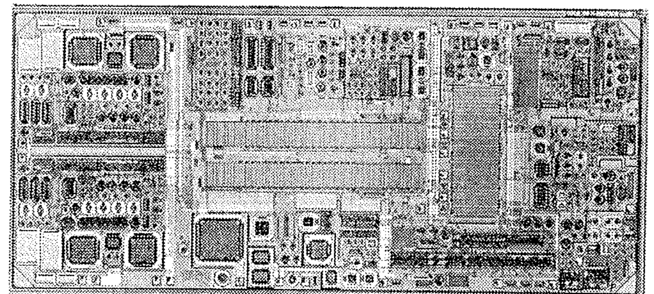
Cooperation with customers who are leading names in these segments has won the EZM a worldwide reputation. Its know-how, which now amounts to more than 1.200 man years, also goes into a number of European research projects, like JESSI, MEDEA and ESPRIT, the EZM is partner in the Network for European Analog Research (NEAR).

World standard in information technology



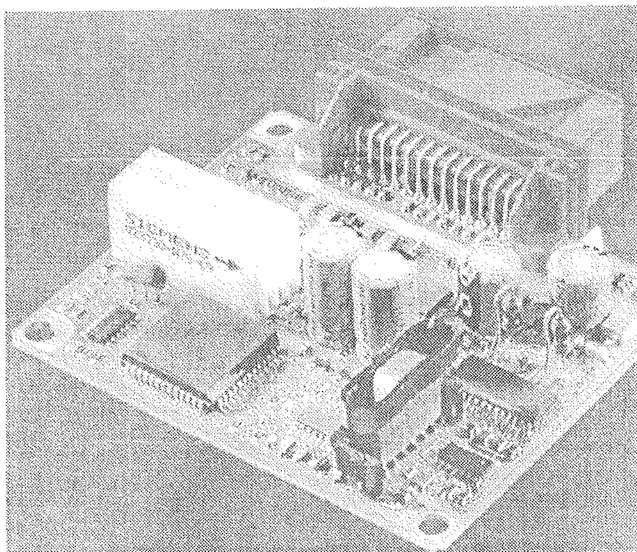
EZM know-how also went into the Gigaset 910 cordless telephone

Since it was first set up, the EZM has worked on ICs for telecommunications. The focus is on circuits that convert analog speech signals into digital information (line card ICs) and condition them for further pro-cessing in central offices. In addition analog modules for the GSM- and DECT-chipsets are developed. Today the EZM is virtually unrivaled by any other design center in its technical contributions to this growth sector.



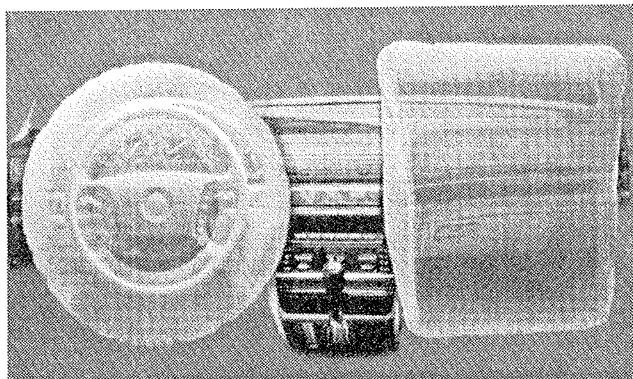
PEB 4065 - a high voltage subcriber line interface circuit (HV-SLIC), which fits to all telephone standards in the world.

Innovations for automotive electronics



Printed circuit-board showing the components of an airbag system

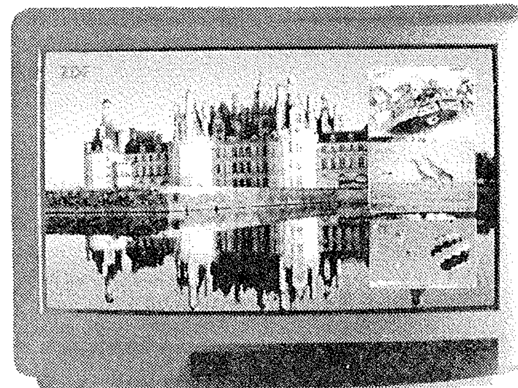
Microelectronics makes a considerable contribution to innovation in automobile engineering. It extends to all areas, like safety with airbags and anti-skid systems. The EZM has successfully developed smart power ICs that combine control, safety, diagnostic and switching functions on a single chip. By using these chips, electronic systems can be made compact but with even better performance. Reliability takes a leap forwards, the decisive quality feature in safety electronics. A further benefit is the huge cost advantages for the automobile industry. And ultimately safety systems can be mass produced so that even more purchasers are able to afford them. The trend goes to very compact systems with as few components as possible (smart power system integration).



View of airbags after activation

Right up front in TV technology

Advanced television is moving over to the digital 100 Hz technology. Picture-in-picture insertion is also standard in today's TV sets. The EZM has developed circuits that include video A/D and D/A converters, digital deflection controllers, display controllers and A/D converter modules for the Siemens line of 8-bit and 16-bit micro-controllers. These chips lead to more flexibility in chassis design and to increased performance of the TV-sets.

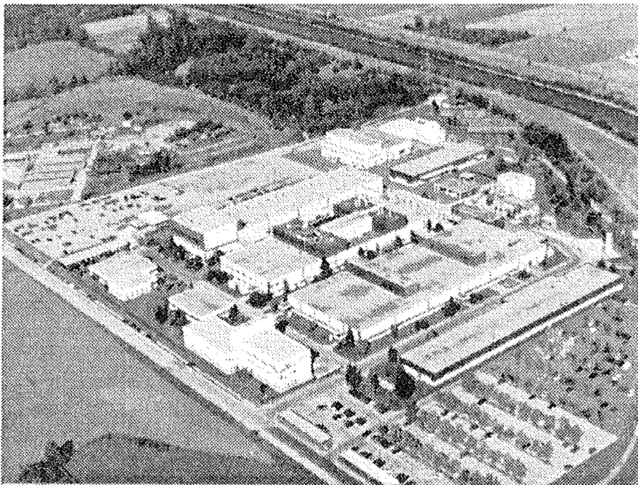


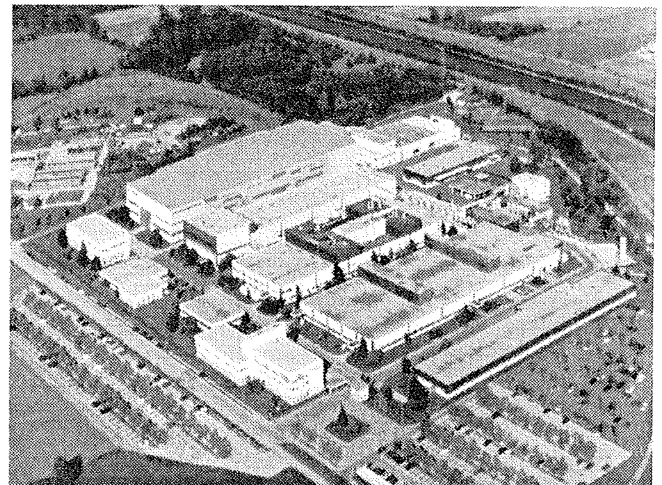
Picture-in-picture (PIP) technology can be found in many modern TV-sets

Compentence from development to volume production

The ramping up of production is optimized in close cooperation with the Villach semiconductor plant

Every project begins with a definition phase for the system solution, and a proper partitioning into sub-systems (chips) of different kind, thus generating specifications. Naturally, this process is carried out in close cooperation with the customer (concurrent engineering), because every design is an integral part of an overall system solution and must fit into the application fast and precisely without any follow-up optimization. After the design phase the EZM handles sampling and develops characterizing and test pro-grams. It also trials the samples and supports ramp-up of production as well as volume application of the ICs.





Aerial view of the Villach location before (left) the investment and in the future, including the new fab (right)

World Standard of Quality

HARMONIZED SYSTEM OF QUALITY ASSESSMENT FOR ELECTRONIC COMPONENTS
CECC CENELEC Electronic Components Committee — Electronic Components Quality Assurance Committee ECQAC

CERTIFICATE OF APPROVAL OF MANUFACTURER
CECC 00 114 Part 1

REGISTRATION NUMBER: F 103/07
FOR: Siemens Entwicklungszentrum für Mikroelektronik Ges.mbH und Siemens Bauelemente OHG
AT THEIR PLACE(S) OF WORK: Siemensstraße 2, A-9500 Villach
IN RESPECT OF GENERIC/SECTIONAL SPECIFICATION: CECC 50 000/CECC 90 000/CECC 90 100

THE ORGANIZATION, FACILITIES AND INSPECTION PROCEDURES AT THE ABOVE PLACE OF WORK HAVE BEEN FOUND TO COMPLY WITH THE REQUIREMENTS OF THE CENELEC ELECTRONIC COMPONENTS COMMITTEE AND IN PARTICULAR OF DOCUMENT CECC 00 114 PART 1, AND EN ISO 9001 FOR QUALITY ASSESSMENT IN RESPECT OF THE FAMILIES OF COMPONENTS LISTED IN THE APPROVAL DOCUMENT(S)

THIS CERTIFICATE DOES NOT AUTOMATICALLY ENTITLE THE MANUFACTURER TO USE THE MARK OR CERTIFICATE OF CONFORMITY. THE APPROVAL OF ANY PARTICULAR TYPE OF ELECTRONIC COMPONENT IS SUBJECT OF A SEPARATE CERTIFICATE

IT IS HEREBY CERTIFIED THAT THE QUALITY SYSTEM OPERATED BY THE COMPANY IS IN COMPLIANCE WITH EN ISO 9001

P&Z — ÖVE

The Villach plant and the Microelectronic Design Center is qualified to CECC and ISO standards of quality. Permanent customer audits - an average of one a month - with excellent assessments and top positions in the Best in Class Survey confirm the exceptionally high standard of quality. And independent institutes also put Villach in the world class when it comes to major categories like yield, cost and complexity of production. All our business is oriented toward the principles of the EFQM.

The Future

Just recently it has been decided, that the Villach location of Siemens Semiconductors will be restructured to the "Competence Center for Power Semiconductors". This decision includes a major investment in a new fabrication line of 3.500 sqm clean room including the transition from 5" to 6" wafersize. Several new technologies for volume products of the future will be developed and introduced into volume production as e.g.:

- Advanced IGBT
- MOS Power Transistor Technology
- Technologies for smart power system ICs (max. breakdown voltage 40 - 170 V)

Start of production in the new fab line is scheduled for October 1997, the overall R&D effort including new investment for this competence center will amount to ATS 5 Billion and will need an additional workforce of ca. 300 people. The Microelectronic Design Center will also need additional highly qualified personnel for the increased demand on new products for the world market.

Dr. Wolfgang Pribyl

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Fax +43 4242 305-745

Microelectronic Design Center:

Siemens
Entwicklungszentrum für Mikroelektronik Ges.m.b.H.
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A-9500 Villach
Tel. +43 4242 305-341
Fax +43 4242 305-223

MIDEM IN NJEGOVI ČLANI
MIDEM SOCIETY AND ITS MEMBERS

In memoriam

Odšel je dr. Borut B. Lavrenčič. Pogrešajo ga njegovi domači, prijatelji in sodelavci "Instituta "Jožef Stefan". Pogrešamo ga tudi člani društva MIDEM, kjer je zavzeto delal vrsto let. S spoštovanjem se še enkrat spominjamo njegovega dela in njegove osebnosti.

Predsednica društva MIDEM
dr. Marija Kosec

Dr. Borut B. Lavrenčič

Poslovili smo se od dr. Boruta B. Lavrenčiča. Mnogo prezgodaj je odšel, saj smo ga poznali polnega načrtov. Tudi bolezen ni uspela uničiti njegove življenjske volje, vzela pa nam je Boruta.

Rojen je bil 7. avgusta 1942 v Ljubljani. Diplomiral je leta 1965 na Oddelku za fiziko Fakultete za naravoslovje in tehnologijo Univerze v Ljubljani. Kot nadarjen študent je takoj po diplomi odšel na študij k profesorju Uehlingu na "University of Washington" v Seattlu v Združenih državah Amerike. Tu je magistriral kot najboljši študent univerze. Žal se je že tedaj oglasila bolezen in moral je predčasno prekiniti izpopolnjevanje. Vrnil se je v Ljubljano na Institut "Jožef Stefan". Tu so tedaj v Odseku za fiziko trdne snovi potekale raziskave feroelektričnih tekočih kristalov z metodami jedrske magnetne resonance. Borut Lavrenčič je prvi začel optične raziskave feroelektričnih kristalov - postavil je optični laboratorij v okviru odseka. Njegove pionirske članke o ramanskem sipanju v feroelektričnih kristalih še danes citirajo kot pomembna dela. S tega področja obsega njegova bibliografija 21 znanstvenih člankov v mednarodnih revijah in 22 objavljenih prispevkov z mednarodnih strokovnih srečanj. Pozneje se je posvetil tudi aplikativnim raziskavam in vodil skupino za aplikacijo feroelektrikov. Rezultat teh raziskav je bil uspešen razvoj javljalnikov požarov in detektorjev za protivlomno zaščito ter prenos te tehnologije v proizvodnjo. V zadnjih letih se je ukvarjal z raziskavami feroelektičnih tankih plasti, ki jih je še pred kratkim objavil tudi v Vakuumistu. Rezultat aplikativnih raziskav je pet patentov in tehničnih izboljšav.

Za svoje delo je bil dr. Lavrenčič večkrat nagrajen. Leta 1982 je dobil nagrado sklada Borisa Kidriča za raziskave dinamike faznih prehodov s sipanjem laserske svetlobe in istega leta še nagrado sklada za izum "Pasivna infrardeča alarmna naprava". Leta 1984 je prejel nagrado za izum "Naprava in sistem naprav za protipožarno zaščito industrijskih in odpraševalnih kanalov", leta 1987 pa za izum "Optoelektronski javljalnik plamena". Te nagrade je dobil skupaj s sodelavci.

Že med podiplomskim študijem v Ameriki si je nabral računalniškega znanja in potem ves čas spremljal razvoj na tem področju. V zadnjih petih letih se je intenzivno vključil v razvoj sodobnih komunikacijskih sistemov. Bil je eden prvih v Sloveniji, ki je spoznal pomembnost komuniciranja z elektronsko pošto in prenašanja podatkov po računalniških omrežjih. Še v Jugoslaviji je pomagal pri ustanovitvi podjetja YUNAC, ki je uvedlo elektronsko pošto za univerze in inštitute po vsej državi. Širil je znanje o novih možnostih komuniciranja in sodeloval pri tovrstnih seminarjih. Predvsem na Institutu "Jožef Stefan" je pomagal mnogim sodelavcem pri obvladovanju spretnosti pri delu s temi novimi elektronskimi mediji. Med vojno leta 1991 je po elektronski pošti vsakodnevno seznanjal strokovno javnost po vsem svetu o stanju v Sloveniji. Leta 1992 je pomagal pri ustanavljanju akademske in raziskovalne mreže Slovenije ARNES. Ukvarjal se je tudi z varovanjem elektronskih podatkov in s kriptografijo. Prirejal je seminarje in izdajal zbornike s to tematiko. Po osamosvojitvi se je vključil v sindikalno gibanje na Institutu "Jožef Stefan" in na ta način postal znan vsem sodelavcem instituta. Zaradi aktivnosti in zaupanja, ki si ga je pridobil pri sodelavcih, so ga le-ti izvolili za svojega predstavnika v upravnem odboru instituta.

Delo, ki ga je začel dr. Lavrenčič, nadaljujejo mladi raziskovalci. Na temeljih, ki jih je postavil on.

Dr. Janez Slak
Delo, 18.12.1996

KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA
CONFERENCES, COLLOQUYUMS, SEMINARS, REPORTS

4. Konferenca o materialih in tehnologijah

1.-4. oktober 1996, Kongresni center GH Emona, Portorož

4. Konferenca o materialih in tehnologijah je združevala: 48. Posvetovanje o metalurgiji in kovinskih gradivih, 4. Posvetovanje o materialih in 16. Slovensko vakuumsko posvetovanje. Potekala je v novem Kongresnem centru GH Emona v Portorožu, od 1. do 4. oktobra 1996. Po zgledu bolj razvitih okolij je bil prvi dan namenjen prof. dr. Francu Vodopivcu, za njegovo 65. letnico. Prof. F. Vodopivec, priznani strokovnjak za kovinske materiale, je bil tudi dolgoletni pobudnik in organizator vsakoletnega, sprva *Jesenskega srečanja metalurgov*, nato *Posvetovanja o metalurgiji in kovinskih gradivih* in zadnja štiri leta *Konference o materialih in tehnologijah*. Tradicionalnemu posvetovanju o metalurgiji in kovinskih gradivih so se na njegovo pobudo pridružili strokovnjaki, ki delujejo na področju keramike, polimerov in zanj pomembnih tehnologij ter na področju vakuumske tehnike, tankih plasti in površinah materialov in se združili v konferenco o materialih in tehnologijah. Obenem je bilo na pobudo prof. Vodopivca leta 1991 ustanovljeno Slovensko društvo za materiale. Svečanega dne so se aktivno udeležili njegovi svetovno priznani kolegi, prijatelji in bivši doktorandi. Otvoritveno predavanje je imel prof. Hans Jürgen Grabke z Max-Planck Instituta für Eisenforschung iz Düsseldorfa. V uvodu je predstavil delo prof. Vodopivca in mu ob jubileju posvetil svoje predavanje kot je navada v zahodni raziskovalni sferi. Nato so se zvrstila še predavanja s področja kovinskih materialov.

V poslovno tehničnem delu posvetovanja so predstavili vodilni iz industrijskih podjetij njihovo raziskovalno razvojno politiko in problematiko. V uvodnem predavanju je o industrijski in tehnološki politiki v Sloveniji spregovoril prof. F. Vodopivec. Prof. M. Mihelčič je seznanil udeležence z ekonomskimi pojmi in zakonitostmi s predavanjem "O ugodnosti ekonomskih kategorij odločajo tudi inženirji". Predstavljena je bila razvojna strategija Koncerna slovenskih železarn do leta 2005, prenova valjarne plošč in trakov v podjetju Acroni, razvojne možnosti in doseženi rezultati na novi ponovčni peči v Acroni in dosežki - milijon ton neorientirane elektro pločevine v podjetju Acroni, ter razvojni trendi v mehki poliuretanski blok peni. O univerzitetnem študiju "Materiali in tehnologije" je spregovoril dekan Naravoslovno tehniške fakultete prof. J. Lamut.

V znanstvenem programu posvetovanja je 12 predavateljev iz Nemčije, Avstrije, Švice, Italije, Češke in Slovaške predstavilo pregledna dela s posameznih področij. Pri kovinskih materialih so bile predstavljene raziskave segregacij elementov v sledeh in njih vpliv na mehanske lastnosti jekel, raziskave produktov visoko temperaturne oksidacije z modernimi metodami za karakterizacijo površin, na področju polimerov so bili predstavljeni novi organski materiali za uporabo v optoelektroniki, v vakuumski tehniki lastnosti getrov in tanke plasti nanesene z naprševanjem, preiskave materialov s tunelsko mikroskopijo itd. Najnovejše dosežke s posameznih področij je v govornem delu predstavilo 12 domačih strokovnjakov s področja proizvodnje in uporabe kovinskih materialov, varilstva, tribologije, trdih dekorativnih prevlek, uporabe polimernih materialov v konstrukcijah, močnostnih feritov na MnZn osnovi ter alnico magnetov, raziskav keramičnih materialov z elektronsko mikroskopijo, raziskav s področja katalize ter kot posebnost uporaba postopka vakuumske impregnacije za konzervacijo kosti mamuta.

Mladi raziskovaci so letos predstavili rezultate svojih raziskav v 10 minutnih govornih prispevkih večinoma v angleškem jeziku. Vsi so bili dobro pripravljeni in nekateri kar za vzgled starejšim kolegom. Nastopilo je 32 mladih, ki so se potegovali za nagrado za najboljše predstavljeno delo. Komisija v sestavi prof. dr. D. Kolar, prof. dr. L. Vehovar in prof. dr. I. Emri je sklenila, da dobijo nagrado naslednji mladi raziskovalci: Matjaž Godec za področje kovinskih materialov, Mojca Hafner za področje keramike in Bobi Cvelbar za področje polimerov; mladih raziskovalcev s področja vakuumske tehnike letos ni bilo.

Vsa ostala dela, ki jih je bilo 106, pa so bila predstavljena v dveh večernih postrskih sekcijah. Letos so bili postrski prispevki predstavljeni tudi v govornem delu. Navkljub nekaterim pomislekom, se je novost pokazala za izredno zanimivo, avtorji so uspeli v 2 minutnem prispevku z 1 do 2 folijami prikazati svoje delo in povabiti zainteresirane k diskusiji ob postrih. Ob kozarcu rujnega in dobrem prigrizku je diskusija trajala pozno v noč.

Letošnja razstava, čeprav številčno skromna, je bila zanimiva, razstavljalci pa zadovoljni, saj so bili ves čas v središču dogajanja.

Dela, predstavljena na posvetovanju, bodo recenzirana in objavljena v treh delih v znanstveni reviji Kovine zlitine tehnologije v letu 1997, ki si je v letošnjem letu pridobila citiranost v pomembnih bazah podatkov: Chemical abstracts, Metal Abstracts, Engineered Materials Abstracts, Bussines Allert Abstracts (Steels, Nonferrous, Polymers, Ceramics, Composites), Aluminium Industry Abstracts, Referativyj Žurnal: Metalurgija. Na internetu je revija Kovine zlitine tehnologije dosegljiva na naslovu: http://www.ctk.si/kovine/.

V splošnem bi lahko zaključili, da je bilo posvetovanje uspešno, da si v bodoče želimo več predavateljev iz industrije in že zdaj vabimo vse strokovnjake, ki delajo na področju materialov k aktivnemu sodelovanju konference, ki bo tako kot vsa leta do sedaj v Portorožu od 3. do 5. oktobra 1997.

M. Jenko

VESTI - NEWS

News from AMS

Austria Mikro Systeme produces new DELTA t field bus controller

Austria Mikro Systeme and DELTA t GmbH, Hamburg, have signed a contract for the production of the programmable field bus controller IX1.

The benefit from using this programmable field bus controller IX1 is that sensor/actuator systems can be connected to all common field bus systems with one and the same hardware.

The concept of the IX1 has proven to be very successful through practical experience. The advantages are significant cost savings in development, shorter time-to-market with the availability of products for a wide range of field bus systems. Through easy programming the IX1 is an economical and technically simple solution where existing systems are enhanced.

The IX1 is the first programmable field bus controller which has been optimized for the processing of serial protocols. It allows easy adaptation of sensor/actuator systems to a large number of common field buses. Software for ASI, CAN, InterBus-S,. P-NET and PROFIBUS is available; BATIBUS, BITBUS, DIN-Meabus, EIB, FIP, Home Systems, ISDN-SO, J1850, MODBUS and VAN can be easily implemented for the IX1. Software for FieldBus Foundation and Hart-Protocol are in preparation.

Austria Mikro Systeme will produce the IX1 in 0.6 micron technology. This product is characterized by a high baudrate and very low power operation.

ASIC Sales Office in Barcelona opened by AMS Group

To extend the customer base and to expand the market position of the AMS Group in Europe in the field of mixed analogue / digital ASICs, the AMS Group has opened a new ASIC sales office in Barcelona (Spain). Hence, the urgent wish by customers to make the technical competence and engineering expertise of the AMS Group available on site in this economic region in Europe has been met.

In recent years Spain's electronic and supplier industry has been characterized by strong and healthy growth in the areas of communications, automotive and industrial electronics (the prime emphasis of the AMS Group).

The sales office team consists of highly qualified Spanish sales and applications engineers, all specialists in the field of mixed analogue/digital high performance circuits.

The address of the new sales office:

Austria Mikro Systeme International S. L.
Parc Technologic del Valles
08290 Cerdanyola
ESPANA

Mr. Horst Gebert, President and CEO: *"The continuous increasing acceptance of the AMS Group by the market has been confirmed by the establishment of this sales offce in Barcelona."*

Last year Austria Mikro Systeme opened a sales office in Hong Kong.

New 50 Volt Mixed Signal CMOS Process Family at Austria Mikro Systeme

Austria Mikro Systeme announces the availability of a new family of mixed signal CMOS processes - designated as "CBT, CBY, CBZ" suited for high voltage ASIC solutions for up to 50V.

General Description

The 2 micron, double metal, single poly, basic process "CBT" was primarily developed for ASICs incorporating complex digital parts with high speed and high density elements operating in a high voltage environment. The "CBY" process is a double metal, double poly version for the integration of linear capacitances and "CBZ" is a double metal, double poly, high resistive poly process for linear resistance applications requiring a minimum of area.

A variety of high voltage devices is available in addition to the standard low voltage MOS transistors: HV-NMOS, -PMOS, -DMOS transistors, N-junction FETs, isolated NPN bipolar transistors, isolated HV-NMOS transistors, Etc. High voltage and standard devices can be easily combined on the same ASIC through the new technology.

Low power consumption, fast switching capabilities and applicability to a wide range of automotive and industrial performance requirements are further key benefits of this advanced process family, being especially suited to withstand high voltage spikes which typically occur in such environments. Further applications include its use in fast high precision analogue circuits and in analogue frontends for sensors and transducers.

Together with the proven 2 micron digital library the new 2 micron process family represents the ideal solution for high voltage ASICs.

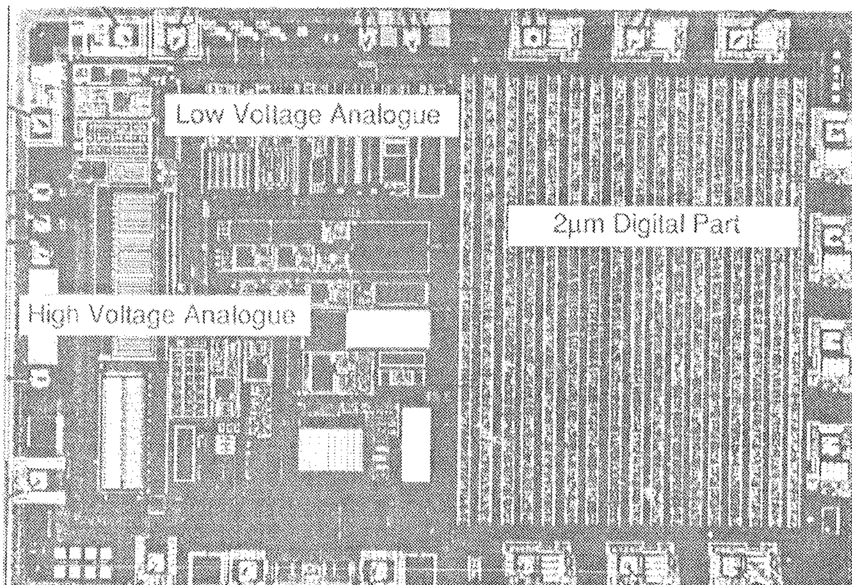
Key Features

- Cells for up to 50V in Mixed Signal CMOS
- CMOS Si-Gate Process Technology with Analogue Capacitor Module
- Lowest Power Consumption, Fast Switching Capabilties
- Two Unrestricted Layers of Metal and One Layer of Poly
- Optional: Two Layers of Poly (CBY)
- Optional: High resistive Poly Layer (CBZ)
- TTL and CMOS Interfacing Capability
- Peripheral Cells with High Driving Capability (Voltage and Current)

Applications

- For ASICs Incorporating Complex Digital Functions with High Speed, High Density Elements
- Fast High Precision Digital Circuits
- Applications to Withstand High Voltage Spikes
- Analogue Frontends for Sensors and Transducers
- Automotive and Industrial Markets

This file is available on the internet address: http:llwww.ams.co.at



Technology Benchmarks

Feature Size:	2.0 µm
Supply Voltage:	Max. 50 V (CMOS Logic 5 V)
Gate Delay:	2 ns
D-Flip Flop Delay:	10 ns
Max. Toggle Rate:	100 MHz

Solid State Technology, October 1996

Russian firms Angstrem, ELMA shopping for capital equipment

Among the groups making the rounds on the SEMICON/West show floor in July was a Russian contingent, made up of government officials and representatives from Angstrem, a semiconductor company (see table), and ELMA, a producer of silicon wafers. Their mission: researching equipment acquisitions for new fab lines at Angstrem, and an expansion of ELMA's capacity from 100-mm to 150-mm wafers.

Angstrem, based near Moscow in Zelenograd ("Silicon City"), has a nearly complete 150-mm fab facility built in 1990 but never equipped, and a newer 4800-m^2 cleanroom built by Meissner + Wurst. The module is ready for equipment installation, and is capable of processing 20,000 to 30,000 wafers/month at design rules down to 0.6 µm. Proposed products include 16Mbit DRAMs, microcontrollers, and custom devices.

Company president Valery Dshkhunyan said his business plan calls for the production of ASICs and other devices in the facility for the Russian market, as well as foundry work for other Asian firms. Currently the company has 1.0 µm facilities; the new line would be capable of 0.5-µm production, said Dshkhunyan.

The main obstacle, of course, is obtaining hard currency for tool purchases. The Russian government, through its Federal Fund for Electronics Development, will provide some support, and there is also the possibility of striking a deal with a technology partner. The US ExportImport Bank, which can provide support for offshore projects that will benefit US companies, is also in funding discussions with the company

Angstrem vital statistics

Employees:	3500
Cleanroom size:	21.500 ft^2 (Class 10)
Capacity (wafers/week):	11,500
Processes:	CMOS, Bipolar, BiCMOS
Products:	Consumer electronics ICs,logic

Feature sizes: 1.0 μm-2.0 μm,
0.8 μm being installed

Source: Integrated Circuit Engineering, Angstrem

ELMA is also talking to the ExIm Bank, and is seeking funding guarantees from the Russian government.

Dshkhunyan can be reached by fax at (+7) 095 53145 23; Sergey Petrov president of ELMA, can be reached by e-mail at Sergey@ elma.zgrad.ru.

Small signs of recovery among Eastern Europe's chipmaking firms

For the first time since the collapse of the Soviet Union, Eastern Europe's semiconductor industry is showing some small signs of recovery though the region appears "relegated to the slow lane for the foreseeable future," according to a new report from Integrated Circuit Engineering and Future Horizons Inc.

Semiconductor production in Eastern Europe grew by almost 9 percent in 1995, and Future Horizons (whose article appears in ICE's recently released MidTerm 1996 report) predicts a similar hike in the current year. There has been a shift in export product mix, away from watch and calculator chips to more sophisticated voltage regulators, power MOSFETs, standard logic and analog ICs. "With Russia's Angstrem now moving into the 150-mm, submicron processing arena, a further shift to more value-added MPU-based products can be expected during 1996," notes the report. Producers in Belarus, the Czech Republic, Poland, and even Serbia are likely to come on line this year with their own niche-based offerings.

Total Eastern European production remains very low however at less than half a billion dollars, and the regions own needs could be met by one mediumsized wafer fab. Most of all, the lack of available cash poses a difficult obstacle to the growth of a local industry.

IMEC newsletter, August 1996

Sirius Communications enters wireless business

Sirius Communications, IMECs most recent spin-off initiative, was established to design and market spread spectrum chips. Spread spectrum is a wireless communication technique intended for use in environments with a high interference background. Application domains include satellite communications, industrial monitoring and control networks, cellular communications and wireless LANs. These markets are currently entering a worldwide explosive growth phase.

The current product range of Sirius Communications consists of a number of highly integrated digital spread spectrum ASICs, evaluation boards and development kits. Their high degree of flexibility makes them well suited for various applications. The strength of Sirius Communications is its combination of spread spectrum know how and expertise in complex ASIC designs. Complete spread spectrum transceivers are integrated on a single chip, together with on-chip processor cores to allow for application dependent flexibility. New, customised spread spectrum chips will be developed in the context of partnerships with OEM builders.

The spin-off initiative originated from a number of successful ESA projects done by IMEC in cooperation with SAIT Systems. The shareholders of Sirius Communications are IMEC, SAIT Systems, Software Holding and Finance, the microprocessor company ARM Ltd, and the management.

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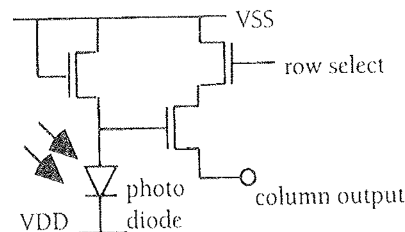
Fuga 15d image sensor

The Fuga 15d is a new variant of the 512x512 pixels, random acccess CMOS image Fuga 15b. Here again AD convertor and automatic illumination control circuitry are integrated on chip. Compared to the earlier Fuga 15b imaging chips, the non-integrating pixel structure (see figure) has been modified to yield sharper



images (high Modulation Transfer Function (MTF)). The sharper images are realised by the use of the shallow P in N-WELL photodiode detectors. This new pixel structure also results in a lower sensititivy in the near infrared (NIR). A single chip Fuga 15d camera is now commercially available through the IMEC spin-off company C-Cam.

ADEQUAT+

IMEC has been selected to coordinate advanced development work on 0.25 μm/0.18 μm CMOS in ADEQUAT+, a new 15-month project funded under the ESPRIT Framework IV programme of the European Commission. The project aims to develop interconnect processing steps and modules for 0.25 μm CMOS by the end of 1996. These backend modules will be combined with 0.25 μm transistor (front-end) modules developed in the previous ADEQUAT-2 project.

The implications of low-voltage 0.25 μm applications will be assessed through a low voltage test circuit selected from several options. Concept testing and patterning feasibility for 0.18 ltm frontend modules should also be completed by the end of 1996. The full 0.18 μm lithography process is expected to be established in a follow-on in 1997, with 0.18 μm front-end and back-end modules in place by early 1998 and 1999, respectively.

Other partners in the ADEQUAT+ project include research centres such as DIMES (Netherlands), Fraunhofer Gesellschaft (Germany), and GRESSI (France), together with the companies GEC Plessey Semiconductors, Philips, Siemens, and SGS-Thomson.

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Development of a low noise amplifier in InP-based HEMT technology with Alcatel Espace

The development of Monolithic Microwave Integrated Circuit (MMIC) technology based on InP-HEMTs at IMEC has led recently to the realisation of many mm-wave demonstrator circuits (low noise amplifiers (LNAs), distributed amplifiers, oscillators...).

Last April this work led to the start of a joint feasibility study with Alcatel Espace for an evaluation circuit to be realised in the InP-based HEMT technology developed at IMEC. Purpose of the study is to investigate the suitability of this technology for demanding future telecommunications applications. This study includes design, fabrication and characterisation of a 30 GHz LNA circuit with challenging specifications. Throughout this development, the potential of this technology in a real industrial environment will be evaluated and its impact on future telecommunication systems can be estimated.

These applications are based upon the underlying R&D, sponsored in the framework of the European Space Agency (ESA) project PLEIADES.

CAST & Prototyping

IMEC's CAST (Custom Application Specific Technologies) and Prototyping services are a respons to industry's growing needs for more flexible design and processing services in order to shorten the product design cycle and to address experimental design and production or small volume series. Such processing or prototyping services are, most of the time, difficult or impossible to get from commercial foundries (volume too low, non-standard processing).

CAST & Prototyping, an ISO 9001 certified service at IMEC, allows you to realise your inhouse designed prototype circuits at the highly advanced silicon processing facilities of IMEC. The technologies offered can be split up according to their distinct features:

- next generation digital or mixed mode CMOS technologies (0.5 μm TLM, 0.35 μm PLM)
- extended state-of-the-art CMOS technologies (embedded CCD or NVM, BiCMOS, low voltage, ...);
- the CAST service.

For more info:
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e.mail: leman@imec.be
or consult
http://www.imec.be/aspinfo/cast/CASTall.html.

System level abstraction of telecom network ASICs

Behavioural synthesis has been an active field of research during the laste decade, leading to a number of research demonstrators, e.g. IMEC's Cathedral and commercial products (e.g. DSP Station™ of EDC/Mentor Graphics). In parallel with the Digital Signal Processing (DSP) application area, behavioural synthesis can also play a key role in reducing design complexities for future telecom network ASIC designs of which the desired behaviour is often characterised by complex algorithms that must operate on large dynamically allocated data structures (e.g. linked record list) where the algorithms and the data structures are tightly coupled.

To address this application domain, researchers at IMEC have been exploring new behavioural synthesis techniques above current commercial behavioural synthesis tool. The research is being conducted in collaboration with engineers from Alcatel-Bell (Antwerp), as part of a larger system design technology effort for supporting system design of telecom network applications (e.g. ATM based broadband networking).

To drive the research effort, IMEC and Alcatel-Bell are jointly studying an actual industrial application. The driver ASIC is a Segment Protocol Processor (SPP) that implements the AAL4 protocol of a connectionless transport server architecture. The connectionless server supports data communication between geographically distributed computers or local area networks (LANs). The functionality is particularly interesting because it is and will be used also in several related systems, The SPP protocol server itself is responsible for storing and forwarding user data, for finding a route to the destination, and for performing various checks.

To aid in the design of this type of applications, IMEC and Alcatel-Bell are exploring into object-oriented programming principles for modeling telecom network systems. New system level synthesis functionalities are being studied.

GOOD-DIE

GOOD-DIE is a project funded by the 4th Framework Initiative of the European Commission DG III. The results will be of interest to all those, not only in Europe, who are concerned with the manufacture, supply, test and use of ICs in die or chip sealed package (CSP) form as

well as to those providing software and hardware to support die usage and multi-chip module (MCM) design. The project aims to assess the Known Good Die (KGD) standards and user interfaces and will set up a database to enable the selection of KGD and a database to provide detailed design information. The GOOD-DIE Network, which coordinates with EUROPRACTICE-MCM and maintains contacts with MCC, Sematech and HDP-UG, has been installed.

The project team consists of Lucas, CODUS, IMEC, Philips, Rood and Eltek. Associate members are Alcatel Mietec, GPS, Matra MHS, TEMIC and Siemens.

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fax +32.16.281.501
or consult
http://www.imec.be/kgd.

KOLEDAR PRIREDITEV 1997

FEBRUAR

03.02.-05.02.1997
SEMICON KOREA '97
Seoul, South Korea
Info.: +1 415 940 6918

06.02.-08.02.1997
1997 IEEE International Solid-State Circuits Conference
San Francisco, CA, USA
Info.: +11 852 2358 7062

12.02.1997
Laser Marketplace Seminar 1997
San Jose, CA, USA
Info.: +1 603 891 9224

20.02.-21.02.1997
2nd International Conference on Chip-scale Packaging
Sunnyvale, CA, USA
Info.: +1 610 799 0419

24.02.-28.02.1997
Semiconductor Technology Seminar
Tampa, Florida, USA
Info.: +1 415 941 8272

MAREC

03.03.-05.03.1997
CleanRooms '97 East
Boston, MA, USA
Info.: +1 603 891 9140

09.03. -14.03.1997
22nd International Symposium on Microlithography
Santa Clara, CA, USA
Info.: +1 360 676 3290

10.03.-12.03.1997
3rd International Symposium on Advanced Packaging Materials
Info.: +1 800 435 4746

17.03.-20.03.1997
ED&TC97 European Design and Test Conference and Exibition
Paris, France
Info.: +44 131 300 3300

APRIL

31.03.-04.04.1997
Spring meeting of the MRS
San Francisco, CA, USA
Info.: +1 610 696 8300

MAJ

12.05.-16.05.1997
Semiconductor Technology Seminar
Glasgow, Scotland
Info.: +1 415 941 8272

12.05.-14.05.1997
2nd International Symposium on Plasma Process-Induced Damage
Monterey, CA, USA
Info.: +1 408 737 0767

14.05.-16.05.1997
11th European Microelectronics Conference
Venice, Italy
Info.: +1 800 435 4746

19.05.-21.05.1997
2nd International Conference on Low Dimensional structures and Devices
Lisbon, Portugal
Info.: +44 1865 843721

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