SWITCHING NOISE IN DISTRIBUTED CLOCK SYSTEMS

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Key words: electronics, integrated systems, A-D integrated systems, analogue-digital integrated systems, mixed design, substrate noise, switching circuits, switching noise, distributed clock signal, noise optimization, design results

Abstract: Substrate noise is a serious limiting factor in the design of analogue-digital systems. Distributed clock systems can be used as an efficient method to solve the crosstalk and simultaneous switching noise associated with the data processing and clock distribution. In this paper we concentrate on the switching noise model for clock pipelines in order to find some interesting parameters for the circuit design. Expressions for clock transition time, switching current ripple and optimal clock symmetry are given. The comparison of an optimized clock pipeline, consisting of N stages with the central clock buffer shows that substrate noise due to the power bus voltage drops can be reduced approximately by $1.2 \cdot N$. Similarly, the reduction factor for substrate noise due to carrier injection from clock nodes can be as high as » $0.75 \cdot N$.

Preklopni šum v sistemih s porazdeljenim signalom ure

Ključne besede: elektronika, sistemi integrirani, A-D sistemi analogno digitalni integrirani, snovanje mešano, šum substrata, vezja preklopna, šum preklopni, signal ure porazdeljeni, optimizacija šuma, rezultati snovanja

Izvleček: Šum substrata je eden od pomembnih faktorjev ki omejujejo integracijo analogno-digitalnih sistemov. S porazdelitvijo signala ure lahko pomembno zmanjšamo presluhe in preklopni šum, ki je povezan z signalom ure in z obdelavo podatkov. V delu raziskujemo model preklopnega šuma v razvodu ure in poiščemo nekatere najbolj pomembne parametre za načrtovanje. Izvedeni so izrazi za čas prehoda signala ure, za stresanje toka napajanja in za optimalno simetriranje signala ure. Primerjava optimalno porazdeljenega signala s klasičnim pokaže, da v sistemu z N stopnjami lahko dosežemo zmanjšanje šuma v substratu za faktor »1.2·N zaradi zmanjšanih konic v napajalnem toku in za faktor » 0.75·N zaradi manjšega vpliva signala ure na substrat.

1. Introduction

In distributed clock systems the central clock is replaced by a large number of time-distributed signals, generated by a clock pipeline. In the simplest form the pipeline can be built as the chain of invertors integrated with the flip flops and logic gates /1/. If the system layout is done in such a way that pipeline stages are put close together with their loads, noise performance of the circuit as a whole can be improved significantly.

2. Switching properties of the distributed clock driver

The CMOS load is a combination of parasitic capacitances to V_{dd}, represented as C_p and parasitic capacitances to V_{ss}, represented by C_n. To analyze the circuit speed, all capacitances can be treated as one single load $C_l = C_p + C_n$ connected to V_{ss}. However, for the switching noise analyze the mode how the capacitances are connected with regard to power supply and the driving stage becomes important and the two capacitances must be treated separately. As presented on Fig.1, the power bus currents are different from the currents in the driving stage; they are smaller and different at the rising or falling edge of the signal.

Dynamic characteristic of the CMOS inverter becomes very complex if the slope of the input signal is comparable to the output signal slope. However, the influence of input signal waveform on the output is limited because of nonlinearities in the vicinity of the threshold voltage. If we apply a ramp function to the input of the chain of equally loaded inverters, such as presented on Fig.2, the responses converge rapidly to a 'characteristic' waveform /2/ that is independent from the initial signal slope. The most important measure for clock driver noise analyze are the slew rates of the rising and falling edges in the characteristic waveform, measured at their maximum value. These values are very close to slew rates measured at $V_{dd}/2$:

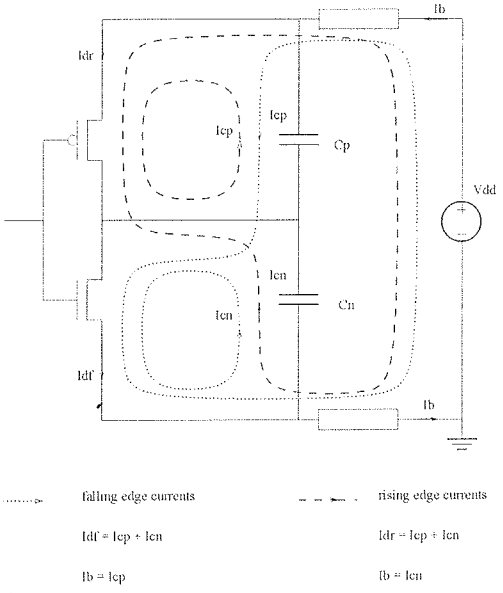

Figure 1: Load currents in the CMOS buffer with local loads; power bus currents are different from the driving transistor currents

$$s_r = \max\left(\frac{dv(t)}{dt}\right) \approx \left.\frac{dv(t)}{dt}\right|_{v(t)=vdd/2} \quad (1)$$

$$s_f = \max\left(\frac{-dv(t)}{dt}\right) \approx \left.\frac{dv(t)}{dt}\right|_{v(t)=vdd/2} \quad (2)$$

In general, s_r and s_f are not equal so that it is appropriate to define the *slew rate symmetry ss*

$$ss = \frac{s_r}{s_f} \quad (3)$$

Clock drivers are usually based on *equal slope* design (*ss* ≈*1*) to achieve best noise immunity and waveform symmetry. For this type of characteristic, the threshold voltages and gain factors (K_p, K_n) for PMOS and NMOS transistors must be equal /3/.

Table 1: *Peak currents in the power bus and in the driving transistors*

I(peak)	Power bus	Driving transistor
Rising edge	$sr \cdot C_n$	$sr \cdot (C_n+C_p)$
Falling edge	$sf \cdot C_p$	$sf \cdot (C_n+C_p)$

Table 1 shows the difference between peak currents in the power bus and driving transistors in a single CMOS clock buffer. To achieve the symmetric characteristic, the P-transistor must be larger than the N transistor so that $C_p \approx 3C_n$. Under these conditions the difference between rising and falling edge bus current spikes becomes considerable. For purposes of noise analyze we will use

$$C_p = p \cdot C_n \quad (4)$$

The simplified presentation of switching currents in stage *i* and the neighboring stages is shown on Figure 3. The interaction of delay times and signal slopes determines how individual switching currents are summed in time to form the power supply current.

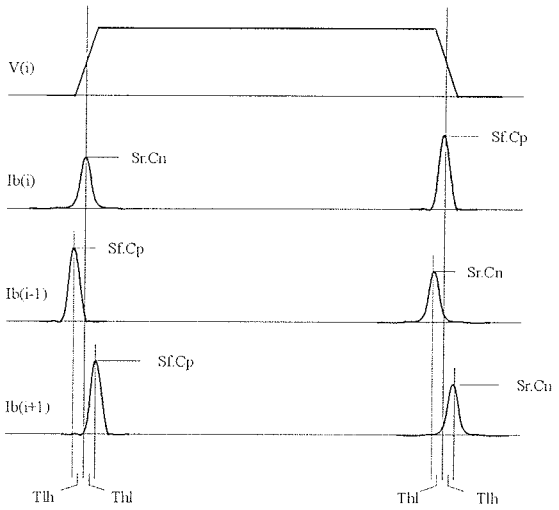

Figure 3: *Bus currents in the chain of inverting buffers with local loads*

Due to the serial signal passing across the buffer chain only a few stages are active at a given time. The sum of power supply currents in the chain depends on the interaction of delay times and the shape of the switching waveforms, but is independent of the chain length (Fig. 4).

If stage *i* is considered as reference stage in the clock pipeline, *neighbor activity* α_n can be defined as the ratio of slew rates in neighboring stages and the reference stage, measured when the reference output reaches $V_{dd}/2$:

$$\alpha_n = \left.\frac{s_{i-1} + s_{1+1}}{2s_i}\right|_{V_i=V_{dd}/2} \quad (5)$$

In the case when slew rate of the reference signal is larger than slew rates of it's neighbors, the switching point in stages with lower slew rates comes closer to $V_{dd}/2$ so that α_n increments. Neighbor activity in pipelines with non-symmetric switching characteristics is therefore different if measured at the rising edge or at the falling edge of the reference signal. However, as long as we are not too far from the symmetric case, values for both edges are close to each other so that an average value can be substituted.

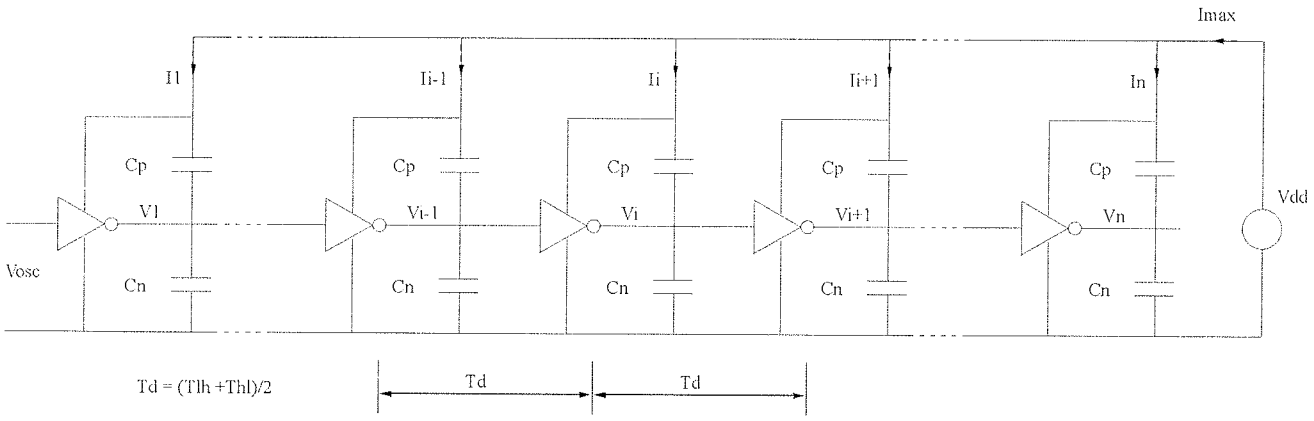

Figure 2: *The distributed clock driver as the chain of inverting buffers*

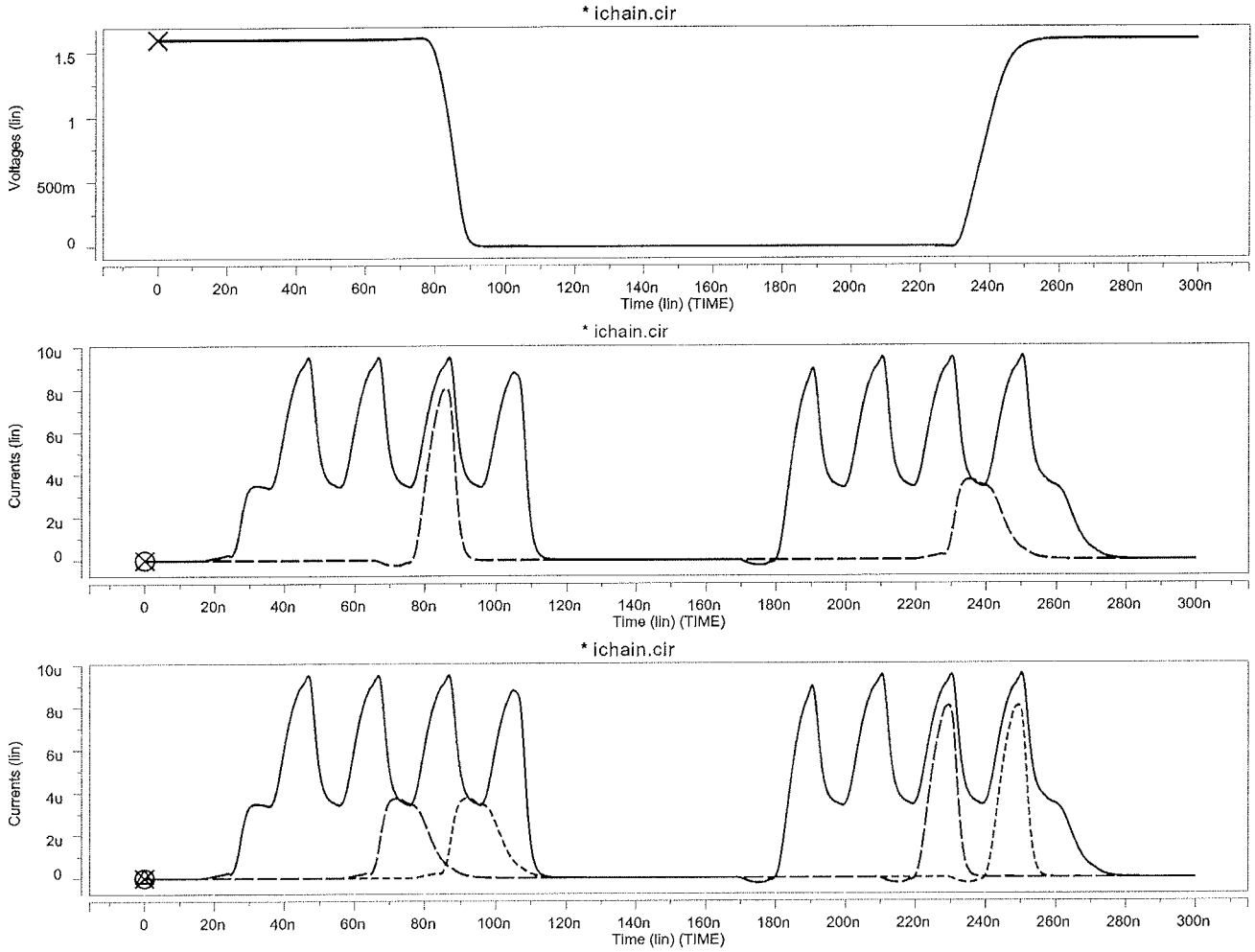

Figure 4: *Accumulation of local currents into the supply current for the case when $s_f C_p > s_r C_n$. Upper pane represents output signal in stage j; current contribution of stage j is shown by dashed line in the middle pane against the total supply current (solid line). Dashed lines in the lower pane represent current contribution of stages i, k against total supply current (solid line). On the rising edge, the supply current is dictated by currents in stages i, j that exhibit falling edges; on the falling edge, it is dictated by the current spike in stage i. The difference between solid line and the dashed lines (≈ 20%) is due to the activity of the neighboring stages. The circuit, based on Figures 1 and 2 with N = 8, was simulated at $V_{dd} = 2V_T$, $C_l = 10C_g$ and $s_f C_p = 2.5 s_r C_n$.*

The average value in the range $K_p/K_n \approx 0.5...2$ is practically independent from K_p/K_n and load capacitances (Fig.5). With a series of simulations for circuits with equal absolute threshold voltages for P and N-type transistors we have found a satisfactory approximation for α_n as

$$\alpha_n = 0.555 \frac{V_{dd} - V_T}{V_T} \qquad (6)$$

If we take into consideration supply currents in the driving stage and in the closest two neighbors, the total supply current for rising edge signal is equal to

$$I_{dd,rise} = s_r C_n + 2 s_f' C_p$$

where s_f' stands for slew rate in the neighboring stages when s_r is maximal:

$$s_f' = \alpha_n s_r$$

so that

$$I_{dd,rise} = s_r \left(C_n + 2\alpha_n C_p \right) \qquad (7)$$

Current peak for the falling edge signal can be expressed in a similar way. Once both current peaks are known, we can define the *relative supply current ripple* as

$$r_r = \frac{I_{dd,rise}}{I_{dd,fall}} = ss \frac{C_n + 2\alpha_n C_p}{C_p + 2\alpha_n C_n} \qquad (8)$$

For each signal transition on the input, active driver stages draw supply current $I_{dd}(t)$. As the signal travels along the pipeline, $I_{dd}(t)$ alternates between leading edge ($I_{dd,rise}$) and trailing edge ($I_{dd,fall}$) peaks. Signal transition time for the whole chain is given by

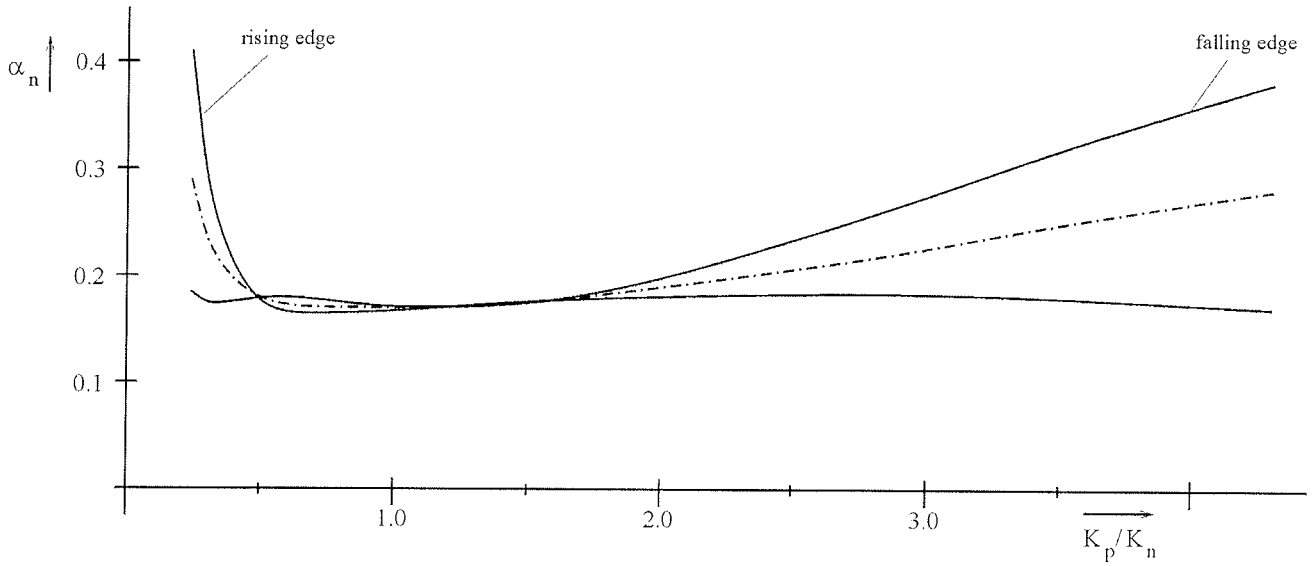

Figure 5: *Activity of the first neighbors (stages i-1, i+1), measured when V_i in the reference stage reaches $V_{dd}/2$. Activity of stages next to the closest neighbors is practically equal to 0. The dashed line shows rising/falling edge average.*

$$T_t = N\frac{T_{lh}+T_{hl}}{2} \tag{9}$$

Maximum supply current takes place in stages with rising edges if $r_r > 1$, or in stages with falling edges if the relation is opposite. Regardless of the case, maximum current occurs in every second stage so that the ripple period is equal to

$$T_{pair} = T_{lh} + T_{hl} \tag{10}$$

3. Noise optimisation

The supply current ripple can be minimized if the rising and the falling edge peaks are made equal. By setting r_r = 1, equation 8 gives optimal clock symmetry

$$ss_{opt} = \frac{p+2\alpha_n}{1+2\alpha_n p} \tag{11}$$

If we now apply equation 6, we get optimal K_p/K_n ratio as

$$\left(\frac{K_p}{K_n}\right)_{opt} = 2ss-1 = \frac{3+(1-\alpha_n)(p-2)}{2(1+2\alpha_n p)} \tag{12}$$

For purposes of noise analyze it is convenient to define the *pipeline activity* α_p as the ratio of switching currents of the entire driver chain and one single stage:

$$\alpha_p = \frac{I_{dd,rpipeline}}{I_{dd,stage}} \tag{13}$$

In general, the entire switching event must be covered. Rising and falling edge currents are equal as long as we treat the optimized pipeline as a whole, but they can be different inside individual stages. For that reason the single stage current must be expressed by the average of rising/falling edge values, so that α_p of a noise-optimized pipeline can be given by

$$\alpha_p = 2\frac{I_{dd,rise,pipeline}}{I_{dd,rise,stage}+I_{dd,fall,stage}} =$$

$$2\frac{I_{dd,fall,pipeline}}{I_{dd,rise,stage}+I_{dd,fall,stage}}$$

From the second expression we get

$$\alpha_p = 2\frac{s_f(C_p+2\alpha_n C_n)}{s_r C_n + s_f C_p} = 2\frac{p+2\alpha_n}{ss+p} \tag{14}$$

Application of optimal symmetry from equation 11 gives

$$\alpha_p = 1+\frac{\alpha_n p^2+4\alpha_n^2 p+\alpha_n}{\alpha_n p^2+p+\alpha_n} \tag{15}$$

In spite of quadratic form the pipeline activity α_p shows almost linear dependence from a_n and p in the range of common design conditions. Influence of p is very low because the pipeline is optimized. In most cases α_p evaluates to values around 1.4 ≈ 1.5.

4. Results

The power bus relaxation of a distributed clock system compared to the central clock system can be estimated by the ratio of peak supply currents. If C_L is the total load of a central clock buffer then the load of an equivalent N-staged clock pipeline would be given by

$$C_L = N(C_n + C_p)$$

We can assume that the central clock buffer has got symmetric switching characteristic, defined by $s = (s_r + s_f)/2$. In favor of fair comparisons we will consider only the last stage of the central clock driver. According to table 1, the switching current in that stage would reach $I_{dd,central} = s \cdot C_L$. The switching current of the distributed driver can be expressed by the average single stage current and α_p, so that we can define the *power bus relaxation factor* R as

$$R = \frac{I_{dd,central}}{I_{dd,pipeline}} = \frac{(s_r + s_f)N(C_n + C_p)}{\alpha_p(s_r C_n + s_f C_p)} \quad (16)$$

Application of equations 14 and 11 gives

$$R = N\frac{(p+1)^2(2\alpha_n + 1)}{2p + 4\alpha_n(p+1)^2} \quad (17)$$

For a typical design case with $p = 2$ and $a_n = 0.15$ we get $R = 1.24\ N$. Bus relaxation factor larger than N can be explained by optimal weighting of rising/falling edge currents and local load discharging in the pipeline, leading to a situation where discharge currents disappear from the power supply lines.

Substrate noise reduction has somehow different background. Since only one pipeline node is active at a given time, we can assume that the coupling capacitance of clock nodes is virtually reduced by N. If the pipeline activity is considered as well then a rough estimation for substrate noise reduction can be given by

$$S = \frac{N}{\alpha_p} \quad (18)$$

We see that substrate noise reduction is smaller than R, particularly because equation 18 is probably too optimistic. Typical values for S can be expected somewhere from $0.5\ N$ to $0.75\ N$.

It has to be pointed out that above noise reduction assessments are valid for clock pipeline alone. Although being known as an important source of switching noise, the clock driver is not the only noise generator. Regular structure of the pipelined driver allows relative high values for R and S that cannot be achieved in other parts of the system.

5. Conclusion

One way to distribute activities of a synchronous digital system in time is to replace the central clock by a large number of equally delayed signals generated by a clock pipeline. The sum of switching currents in this case produces pulses with low amplitude and long duration, leading to substantial reduction of supply current spikes in comparison to systems with central clock. The resulting power bus relaxation and substrate noise reduction are beneficial for both pure digital and mixed projects.

Pipeline clocking has the potential to reduce three important noise sources: power bus bouncing, signal cross-talk and substrate noise. In order to find optimal design measures for noise reduction, switching properties of clock pipelines have been studied. Neighbor activity has been defined as the basis for calculation of a number of important parameters, among which supply current ripple, ripple frequency and length, optimal symmetry and the K_p/K_n ratio have been found. Assessment of power bus relaxation and substrate noise reduction have been given as well.

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