UDK621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 25(1995)2, Ljubljana

MICROELECTRONIC R&D FACILITY AND ITS IMPACT ON ELECTRONIC INDUSTRY IN NEWLY INDUSTRIALIZING COUNTRIES

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Key words: microelectronics, R&D, Research and Development, Newly industrializing Countries, electronic industry, ASIC, Application Specific Integrated Circuits, IC, integrated circuits, state of the art, electronic equipment, know how, licences, equipment manufacturing, IC design, top down design, monolithic circuits, microelectronics centres

Abstract: Microelectronics has impacted and continues to impact on modern society. Newly industrializing countries can not stay aside from these developments. The concept of R&D microelectronic center running in academic society in particular NIC can serve as a moderate and state of the art microelectronic activity. Such center could represent the seed for further industrial growth if the market excuses high investments needed.

Mikroelektronska razvojno - raziskovalna enota in njen vpliv na elektronsko industrijo v industrijsko se razvijajočih deželah

Ključne besede: mikroelektronika, R&D raziskave in razvoji, NIC dežele industrijsko razvijajoče se, industrija elektronska, ASIC vezja, IC vezja integrirana, stanje razvoja, oprema elektronska, know how znanje in izkušnje, licence, proizvodnja opreme, IC snovanje vezij integriranih, top down snovanje od zgoraj navzdol, vezja monolitna, centri mikroelektronike

Povzetek: Mikroelektronika je in bo vedno vplivala na razvoj moderne družbe. Industrijsko se razvijajoče dežele ne morejo stati tem dogajanjem ob strani. Razvojno - raziskovalni mikroelektronski center delujoč v akademski sredini v določeni industrijsko se razvijajoči deželi lahko obenem služi tudi kot njena moderna in ne predraga mikroelektronska aktivnost. Tovrstni center bi lahko predstavljal seme za nadaljnjo industrijsko rast, če bi trg le lahko opravičil potrebna visoka vlaganja.

1. INTRODUCTION

Many authors clearly justify the need of domestic microelectronic activity in NICs. They point out the predominant need of their own ASIC capabilities. /1/

In establishing the efficient domestic production of the electronic equipment under licensing agreements the need of good starting capabilities of domestic producers is quite evident. The success of domestic production in environment qualified to independently develop and manufacture the industrial products is much higher compared to others without this expertise. The insufficient know how also influences the purchases of licenses for production of state of the art goods, thus locking the country into obsolete and with little domestic value added fabrication. Therefore extensive modern system expertise and ASIC experience and possibly production capability is mandatory in pursuing an efficient and rewarding domestic electronic equipment manufacturing.

2. ACTIVITIES NEEDED TO GET ASICs

a) IC design

ASIC expertise is comprised of the design effort, fabrication of prototypes and their functional verification and volume production and testing. /2/

Basis for the efficient ASIC expertise is in the profound system knowledge. The procurement of ICs follows one of the two self explanatory flowcharts (Figs.1 and 2) and is thoroughly monitored by IC designers residing in system house and or in the silicon foundry which could be vertically integrated or not. A set of well proven control procedures follows every design consisting of feasibility

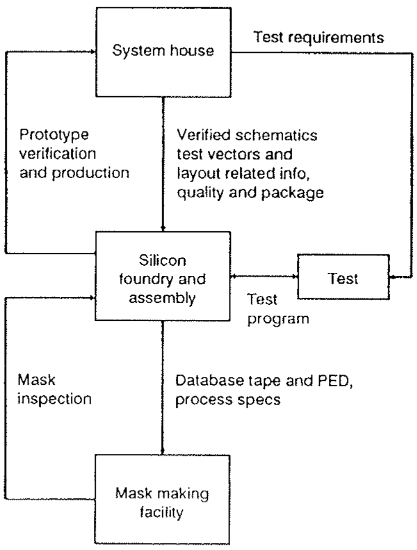

Fig. 1: Simulated schematic interface to silicon foundry

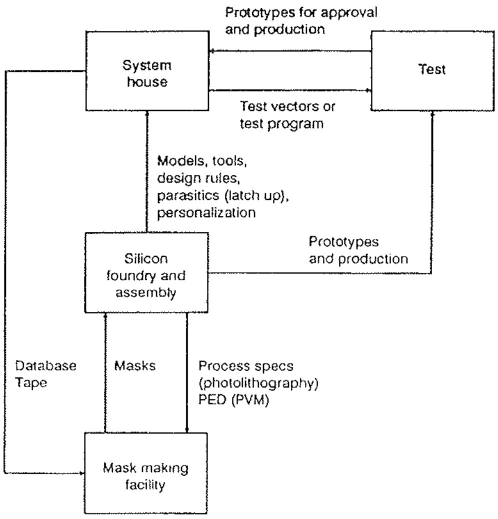

Fig. 2: Layout database interface to silicon foundry

study, circuit specifications development, schematic capture, simulations, test program definitions, layout verifications and cost considerations.

The design procedure follows one of the options, shown on Fig. 3. The design of digital ASICs is strongly supported by comprehensive CAD tools and silicon compilers. This is still not the case for analog and mixed signal ASICs designs. At the beginning the progress in analog design /3/ was impeded by the lack of motivation since everybody believed that everything would go digital. Very strong conservatism was present among so called analog experts. The advent of monolithic technology widely opened new horizons in the design philosophy which changed dramatically from old discrete designs in which integratable parts were put on chip into the abundant use of active devices giving the accent to functional optimization as the primary objective.

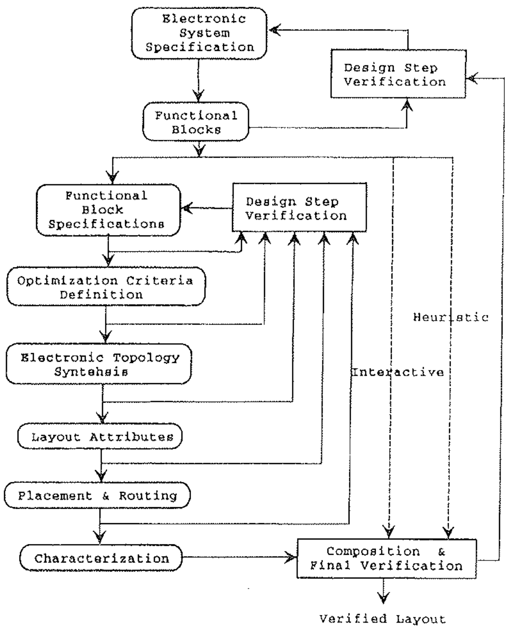

Fig. 3: Hierarchically Oriented Top down IC design

Using hierarchical top down design, the problem is reduced to appropriately combining standardized basic circuits composed of conventional devices. The method is widely supported by various CAD tools.

The other option is translation of the function to be implemented on silicon into the dedicated and optimized circuit. This is built from conventional blocks or structures based on physical phenomena and combined with appropriate layout of integratable structures.

b) Monolithic IC technology

The investments needed to cope with the developed countries in the field of IC technology are too high to be justified in the majority of NICs. Competitive silicon foundry namely needs the free access to know how in down stream technology, to modern process equipment and materials, to services etc. Due to political reasons this is still not viable in NICs. The very little chances to sell their production on the developed markets is another drawback. Domestic markets are usually too small to guarantee economically justified volume production. In recent years many silicon foundries in NICs were forced to shut down their operations in spite purchasing state of the art IC technologies from the developed countries. This fact of course doesn`t mean that the semiconductor technology is with few exceptions reserved only for the developed economies.

3. PROPOSED MODEL DESCRIPTION

Academic research teams working in small but state of the art equipped centers in NICs could serve as a potential seed to industrial microelectronic operations. They are open and non-profit organizations and therefore able to establish tight relations with similar institutions in the developed countries exchanging their expertise and talented highly trained individuals.

Accumulated know how can than be easily transferred to industrial environment if such need exists.

The model for the microelectronic center of excellence is therefore ,comprised by the team of well trained system specialists who work hand in hand with the IC design engineers. They need to have good access to the modern CAD tools and open window to the microelectronically developed community. This is even more valid for their colleagues - process engineers. Small test and packaging activity could be part of the proposed scheme. Very well established fields of interests for academic groups of the kind are usually the device physics, design methodology, CAD tools, process technology and special niche applications like intelligent sensors, medical electronics etc. To these activities real ICs for industrial applications should be added which are mature enough to be suitable for volume production elsewhere.

The proposed scheme could be altered in the communities who pay little or no interest to semiconductor technology. The electronic system and IC design and test and evaluation teams can get the silicon foundry services from the selected silicon vendors or from institutions like Euro-

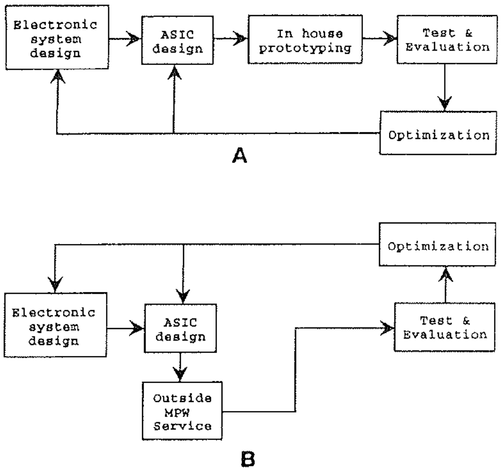

Fig. 4: Model of the Microelectronics Centre
Option A:
Complet design / optimization cycle in NIC
Option B:
Outside Multi Project Wafer processing service

chip where low cost multi project wafer services can be purchased. This model is usually less efficient due to the fact that MPW services take longer turnaround time and only standard process steps are available. Fig 4 shows both options of the proposed model.

Microelectronic know how is a key element in maintaining and improving the competitive position of domestic electronic industry elsewhere.

Associated research should be focused and directed at issues and problems on and beyond current industrial horizons. Wherever practical it should be carried out cooperatively with industry and academic institutions on an international basis.

4. CASE STUDY

Laboratory for microelectronics of the University of Ljubljana fits very well into the proposed model.

The laboratory was founded 25 years ago. It is active in the development of CMOS & BiCMOS submicron process modules, in industrial ASIC design, in the design and analysis of complex electronic systems and in the development of new design methodologies and CAD tools for mixed analog-digital signals.

Research staff totals 14 PhDs with average 15 years of experience, 11 MS senior designers and technologists and 12 experienced engineers and technicians.

Faculty for Electrical and Computer Engineering supports all other services which are vital for the successful operation of the laboratory.

Research facility includes 400m^2 of clean room area for experimental CMOS and BiCMOS processes, 1800m^2 floor space for technology support, assembly and design, maskshop and test laboratory.

Laboratory started with the development and the design of complex thin film integrated circuits and monolithic discrete devices. In 1976 the 2" wafer prototyping line was operational. At present 4" wafer line serves the laboratory needs. Some process steps were developed jointly with International Microelectronic Products Int.

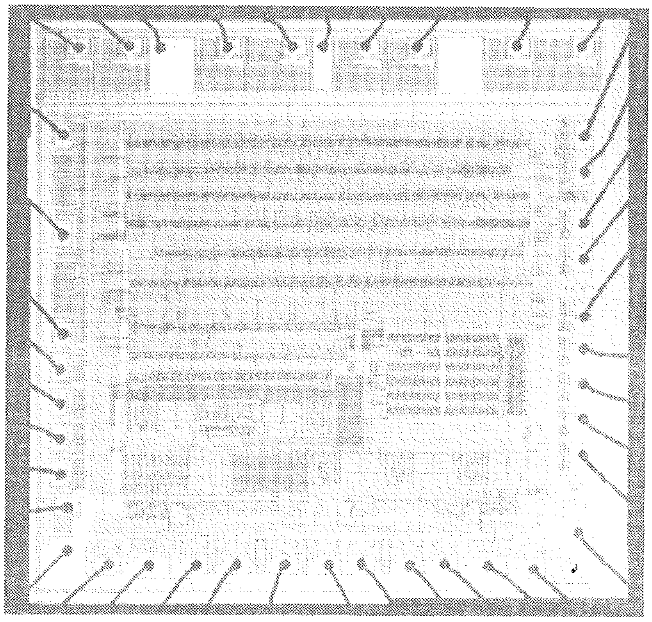

Fig.5: Universal Dual Channel SLIC Interface
Chip size: 4701 µm x 4642 µm
Process: 3µm Dual Poly Single Metal p-Well

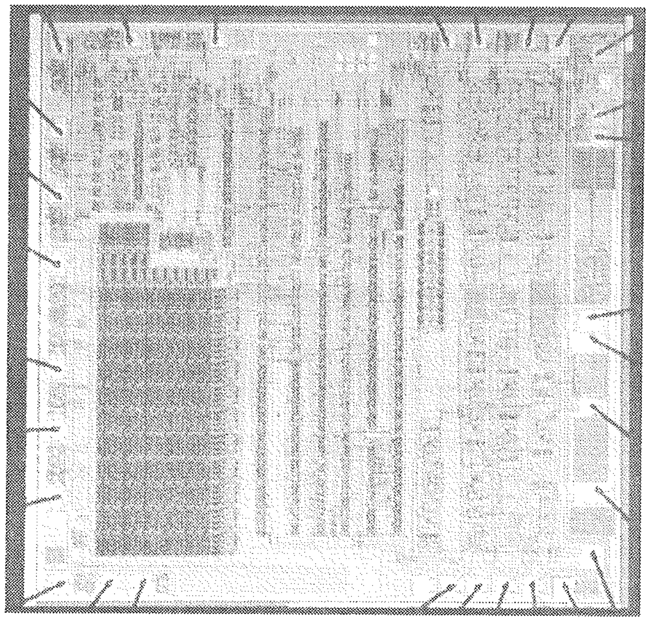

Fig.6: Single Chip Telephone with Loudspeaker
Chip size: 5000 µm x 5120 µm
Process: 3 µm Dual Poly Single Metal p-Well

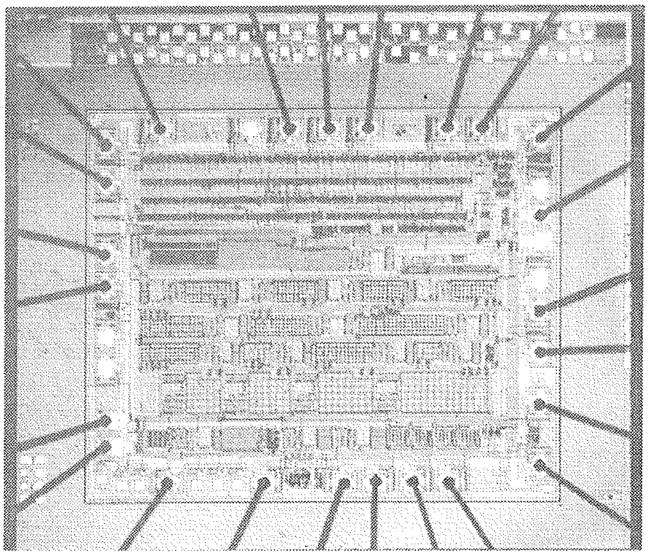

Fig.7: *Data Communication Interface on Power Lines for Remote Energy Management*
Chip size: 3614 μm x 2993 μm
Process: 2 μm Dual Poly Dual Metal n-Well

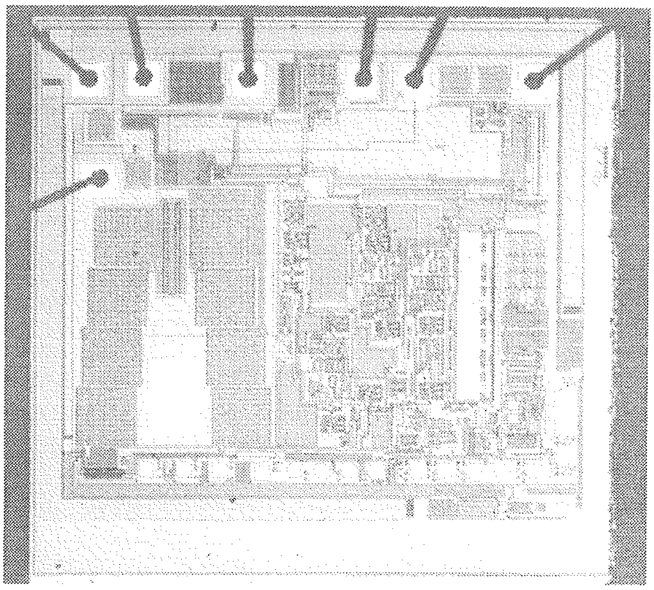

Fig.9: *Voltage Regulator for Alternator with Multiple Fault Detection & Indication*
Chip size: 2800 μm x 2600 μm
Process: 5 μm Dual Poly Single Metal p-Well

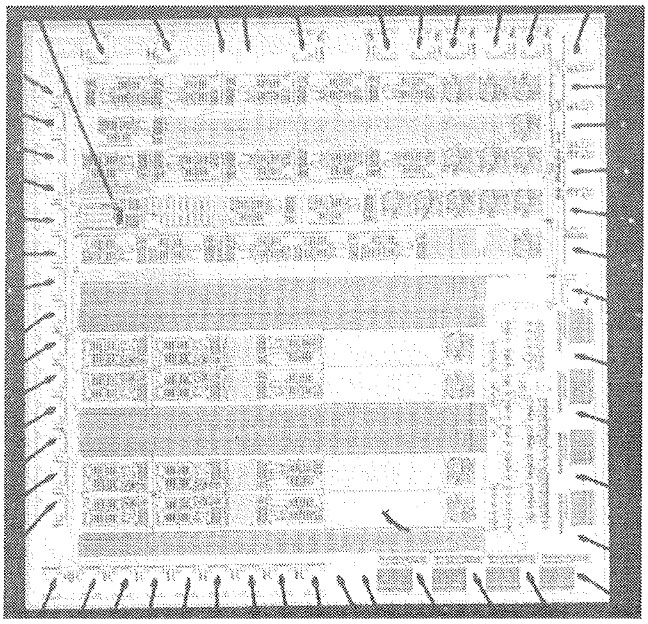

Fig.8: *Radiation Hardened 16 bit Absolute Angular Encoder for High Reliability Space Applications*
Chip size: 4684μm x 4676 μm
Process: 2 μm Dual Poly Dual Metal n-Well

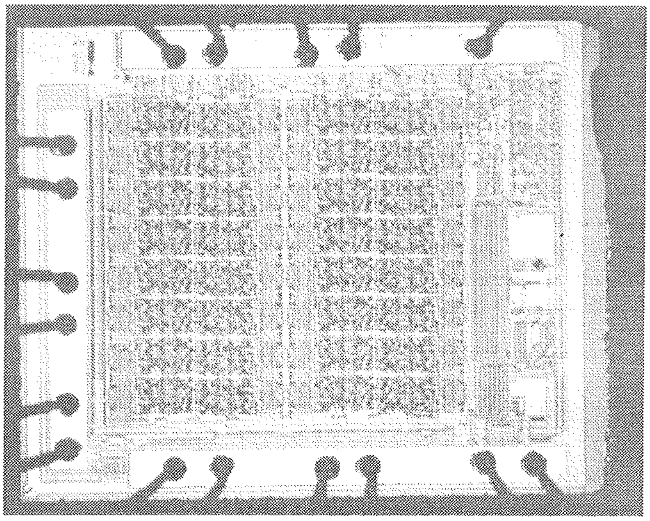

Fig.10: *Wireless Proximity Electronic Key IC*
Chip size: 2296 μm x 2114 μm
Process: 5 μm Dual Poly Single Metal p-Well

The members of the laboratory participated in joint development teams with American Micro Systems Inc., International Microelectronic Products Inc., and with Austria Mikro Systeme Inc. In some areas the achievements of the Laboratory were at the leading edge of IC design and the design methodology.

Some of the designed ASICs in the area of telecommunications, precision measurements, automotive, security systems and medical electronics were produced in the quantities over million pieces.

Fig. 5 to 11 show some of the successful designs of Laboratory in the above fields.

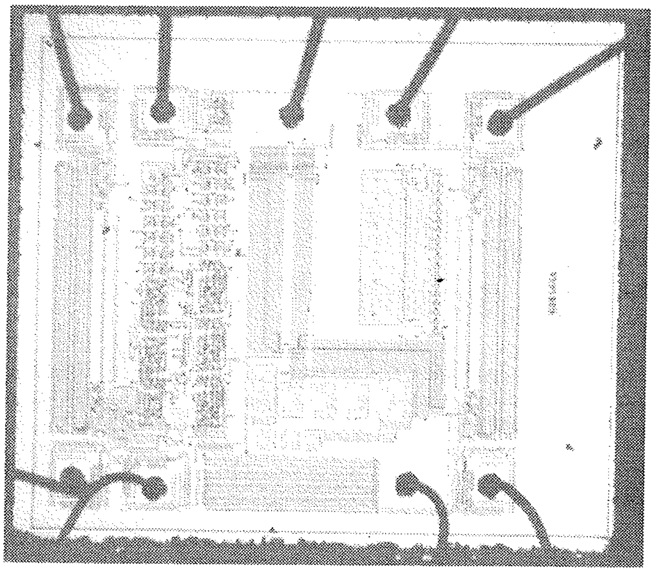

Fig.11: Implanted Dual Channel Electronic Stimulator for Rehabilitation in Humans
Chip size: 1876 μm x 1711 μm
Process: 5 μm Dual Poly Single Metal p-Well

5. SUMMARY

Investments into microelectronic submicron volume production lines nowadays exceed one billion dollars. Underdeveloped markets in NICs normally do not allow such huge investments. The lack of well trained marketing personnel able to sell microelectronic products worldwide and small domestic consumption is another obstacle against these investments. Proposed model is one possible solution for NICs to educate engineering community and to maintain the ties with the mainstream microelectronic developments. Furthermore such possibility offers NICs to retain their activities and to remain competitive in selected niche electronic applications worldwide such as in the area of micromachining.

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7. BIOGRAPHICAL NOTE

Dr. Lojze Trontelj is a full professor of Microwave theory and Microelectronic technology at the University of Ljubljana, Faculty of Electrical and Computer Engineering where he founded Microelectronic Laboratory in 1969. He is authoring over 100 technical papers and holds several patents. He was a member of the presidency of the National Research Council. He has received several national awards for his research work.

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Prispelo (Arrived): 3.7.1995 **Sprejeto (Accepted): 11.7.1995**