AN ON-CHIP RFID RECEIVER STAGE

Anton Štern, Janez Trontelj

Faculty of Electrical Engineering, University of Ljubljana, Slovenia

Key words: RFID, reader, receiver, CMOS, amplitude demodulation, noise, smart card

Abstract: The article describes the development of an on-chip receiver stage intended to be used for receiving the transponder's modulation in a single chip low power RFID reader system for the ISM 13.56MHz frequency range. The operating is based on a low noise double envelope follower for AM detection. The receiver gain and bandwidth can be optimized to be compatible with all ISO RFID communication protocols and with customer defined protocols from a low frequency direct modulation systems up to 848kHz subcarrier modulation. The receiver stage design is described and the measurement results of the implemented prototype are presented.

Sprejemnik za RFID integrirani bralnik

Ključne besede: RFID, bralnik, sprejemnik, CMOS, amplitudna demodulacija, šum, pametna kartica

Izvleček: V prispevku opisani sprejemnik je namenjen sprejemu modulacije kartice v celoti integriranem bralniku brezkontaktnih pametnih kartic v ISM frekvenčnem področju 13.56MHz. Amplitudni demodulator je nizko šumni vhodni sledilnik obeh ovojnic. Nastavljivo ojačenje in nastavljiva frekvenčna širina sprejemnika omogočata prilagoditev sistema vsem ISO standardiziranim in drugim uporabniško definiranim načinom komunikacije s pametnimi karticami od direktne modulacije do modulacije podnosilnega vala na 848kHz. Opisano je načrtovanje sprejemnega dela veza, podani pa so tudi rezultati, izmerjeni na izdelanih vezjih.

1. Introduction

In the recent years the RFID procedures have become commonly used in many areas of human activity. At some special applications, like car immobilizing, the number of the transponders is almost the same as the number of the readers (e. g. for two keys there is one reader on each side of the car and one at the ignition lock). Consequently, on the market there is a strong need for a small and cheap reader - the integrated reader. The receiver stage, which is described in this article, is an important part of such RFID system.

2. The receiver

The receiver described is intended to be used in a single chip 13.56MHz RFID integrated reader. In an RFID system with defined geometry and defined output power the operating range is limited by the sensitivity of the receiver on one hand and the dynamic range of the receiver on the other hand.

The reader chip which has been designed is highly versatile and can operate with all ISO standardized coding and modulation schemes /1,3/. It can also operate with known customer defined and partly standardized coding and modulation techniques. The following requirements must be covered by the receiver part: the receiver must be capable of operating with the 212kHz, 424kHz and 848kHz subcarriers. The operating with the transponders without the use of the subcarrier is also needed. Different coding protocols (OOK, BPSK, NRZ) request different receiver response at the beginning of the data stream.

Consequently, the gain and frequency response of the receiver must be optimized for each subcarrier frequency and coding used due to different noise bandwidth to achieve reasonable sensitivity. Since the receiver is intended to be used together with an on-chip low power transmitter the expected operating range for a card size transponder is between 10cm and 20cm depending on the reader antenna size and transponder type. The receiver sensitivity needed is in a range of milli-volts carried on a $5V_{PP}$ RF carrier. On the other hand the receiver output signal should not be corrupted when the transponder is close to the reader antenna where modulation signal can reach up to one half of a volt on the RF carrier.

Figure 1 presents the block diagram of the receiver. It is composed of an envelope detector, DC level cancellation and gain stage, second order low-pass with gain, high-pass with gain and a digitizing circuit. The low-pass and high-pass corner frequencies and receiver gain can be set by option pins to optimize receiver performance to system demands.

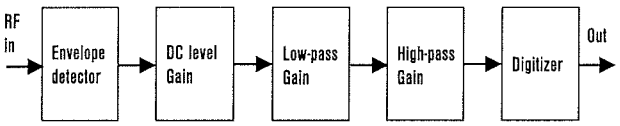

Figure 1: Block diagram of the receiver

The envelope detector is the most critical part of the receiver due to the direct impact of the detector input noise to the system noise and sensitivity performance. The schematic is presented in figure 2. It is composed of NMOS and PMOS source follower which detect upper and lower

envelope. Both signals with partly suppressed carrier are impedance decoupled with two voltage followers and then subtracted. The detector's loss is approximately 1.2dB due to the body effect of the MOS transistors. This loss is compensated in the subtraction stage. Since there is no gain in the detector the input followers, amplifiers and gain setting resistors used must ensure low noise contributions. The expected input noise is between 25nV/√Hz and 40nV-√Hz with process variations and in temperature range from -40°C to 120°C.

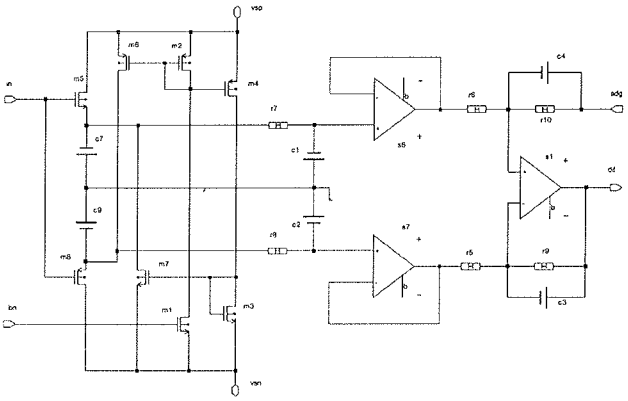

Figure 2: Envelope detector

Figures 3 and 4 present simulation results of the receiver chain. Figure 3 presents a time domain simulation where the input signal is composed of three AM bursts on an RF carrier each of a different amplitude (upper panel). In the middle one there is the signal after filtering and gain stages and in the bottom there is the digitized output signal.

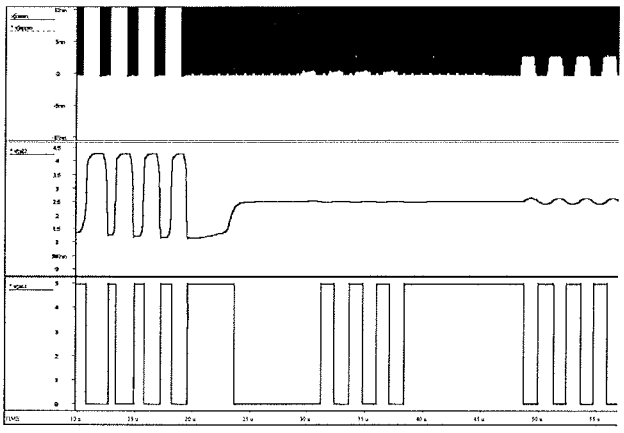

Figure 3: Time domain simulation results

The frequency domain simulation in figure 4 is used to examine the gain and filtering properties of the circuit (upper panel) and the noise levels (middle and bottom panel).

The layout of the receiver is shown in figure 5. In the bottom left hand corner there is the input envelope detector with source followers and current sources, followed by shielded filtering capacitors. In the right and on the top there are amplifiers and in the middle there are capacitors used in high pass filter.

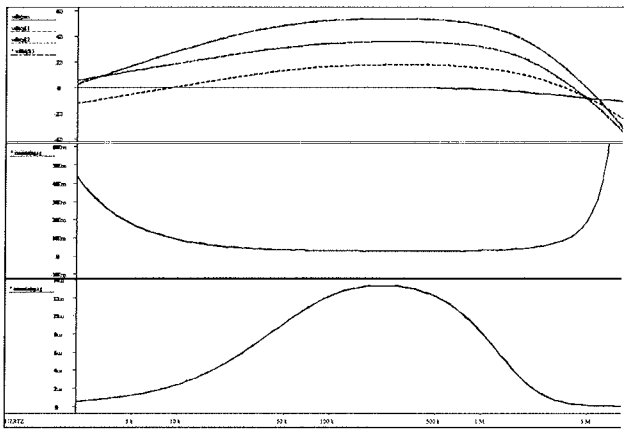

Figure 4: Frequency domain simulation results

The circuit was integrated in a double metal, double poly 1μm C-MOS process together with the other blocks needed to complete RFID reader system. A significant care has been taken when the different blocks were put together to minimize the influence of one block to the other. Especially the capacitive cross-talks and substrate currents from the transmitter driver to the input stages of the receiver can corrupt noise and stability properties.

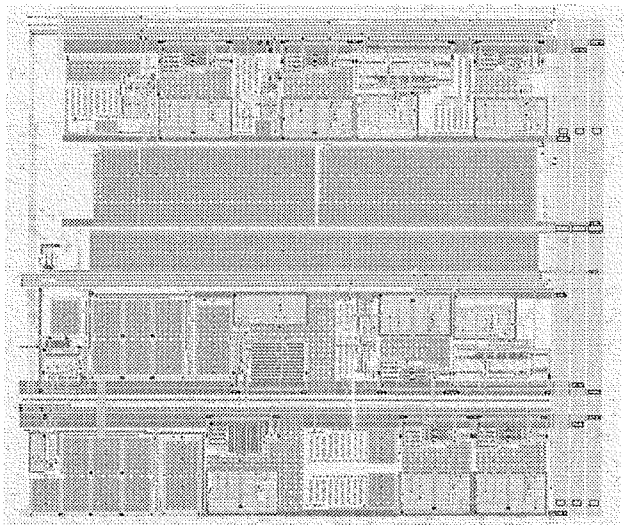

Figure 5: Layout of the receiver

The fabricated samples were tested for noise, bandwidth and sensitivity properties. In table 1 there are the results of the output spot noise level measured at different frequencies and for different bandwidth settings. In the last column there is the output noise integrated over the entire receiving bandwidth. We can calculate that typical input spot noise is approximately 27nV/√Hz which is expected. The integrated input noise is 35μVRMS with a high bandwidth setting. The noise spectrum is shown on figure 6.

The receiver noise is not the only noise source in the system. The transmitter's oscillator has its own phase noise which goes through the transmitter and matching network to the receiver's input. The oscillator's noise sidebands are demodulated, thus increasing the receiver's input noise. The transmitter's oscillator is designed as a quartz crystal type which exhibits lowest possible noise sidebands for a reasonable price. The oscillator's noise increases the receiver's input spot noise for approximately 30% at 100kHz. At frequencies below 100kHz the spot noise rise is higher than 30% and above 100kHz it is lower than 30%, but the RMS noise is also increased for approximately 30% in 400kHz bandwidth. This means that there is no dominant noise source in the system which could be easily decreased to efficiently improve noise and sensitivity performance of the system.

BW set to	Spot noise at 25kHz	Spot noise at 100kHz	Spot noise at 210kHz	Spot noise at 840kHz	RMS noise
kHz	$\mu V/\sqrt{Hz}$	$\mu V/\sqrt{Hz}$	$\mu V/\sqrt{Hz}$	$\mu V/\sqrt{Hz}$	mV_{RMS}
1000	7,2	7	6,5	5,4	8,8
400	7,2	7	6	1,6	5,4
200	7,2	6	3,4	0,35	3,7

Table 1: Noise measurement results at gain setting 48dB

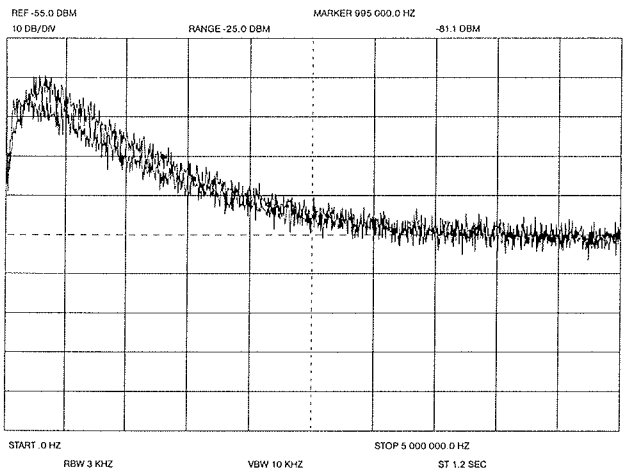

Figure 6: Noise spectrum

Low pass filter high cut-off frequency can be set to approximately 1000kHz, 400kHz and 200kHz. The belonging measured values are 1070kHz, 420kHz and 240kHz respectively at room temperature. On figure 7 the frequency response plot is presented. The gain can be set to 48dB and 42dB. The sensitivity can be set to 0.6mV$_{PP}$ for lower frequency range (200kHz) and to 1.5mV$_{PP}$ for higher frequency ranges (400kHz and 1000kHz) on a 5V$_{PP}$ RF carrier.

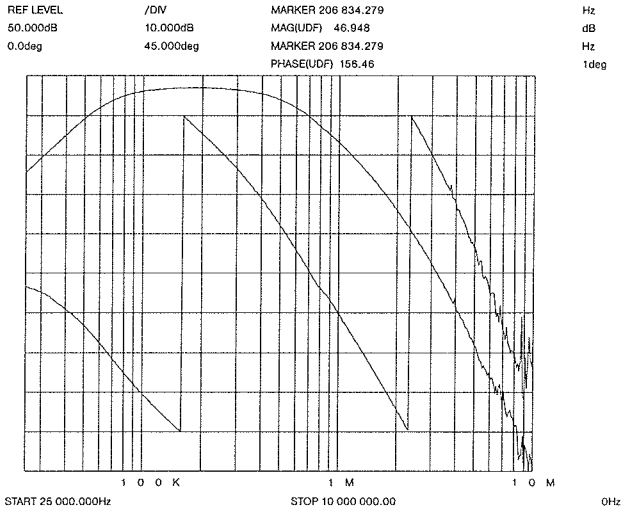

Figure 7: Frequency response of the receiver (BW set to 400kHz)

Receiver was tested in a complete RFID system together with the associated low power transmitter. The transmitter's output power was 20dBm and the reader antenna diameter was 12cm, while the Q factor was 23. The transponder was a card size transponder with a coil inductance of 1.42μH. The resonance at 13.56MHz is achieved by a capacitance of 97pF. The small signal quality factor Q=45 was decreased to Q=12 when the transponder was put in a minimum operating field strength. Both the transponder and the reader coil were tuned to 13.56MHz±150kHz.

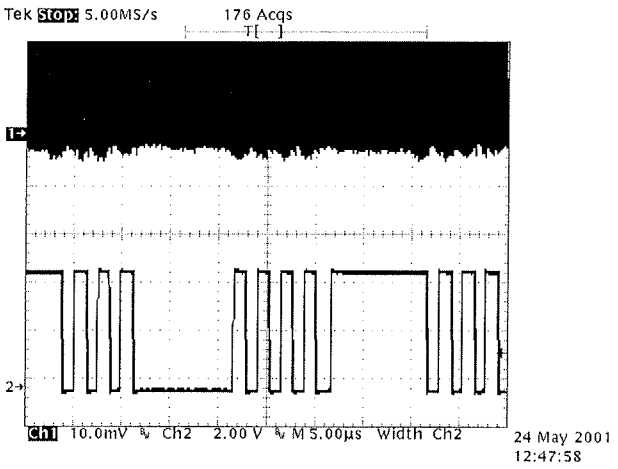

Figure 8: 424kHz subcarrier, on/off keying, distance 16cm Upper trace- RF in, lower trace - digitized output

Receiving the transponder's modulation was checked for different transponder's subcarrier frequencies at distances from the maximum operating range to the minimum operating range, which means that the transponder is at the surface of the reader antenna. On/off keying and BPSK coding was also checked. Figure 8 presents receiver's input signal (upper trace) and correct digitized receiver's

output at 16cm distance, which is close to the maximum operating range of a system when 424kHz, 53kbit/s OOK coding is used. Figure 9 presents the same signals at 848kHz, 53kbit/s OOK, but the transponder is set very close to the reader antenna. The envelope magnitude is 0.5V_{PP} and DC level shift at modulation start and stop is approximately 0.25V. The DC level cancellation circuit is fast enough not to lose pulses at the beginning of the burst. Operating range is 16-17cm when lower frequency system is used and 15-16cm when higher frequency subcarrier system is used.

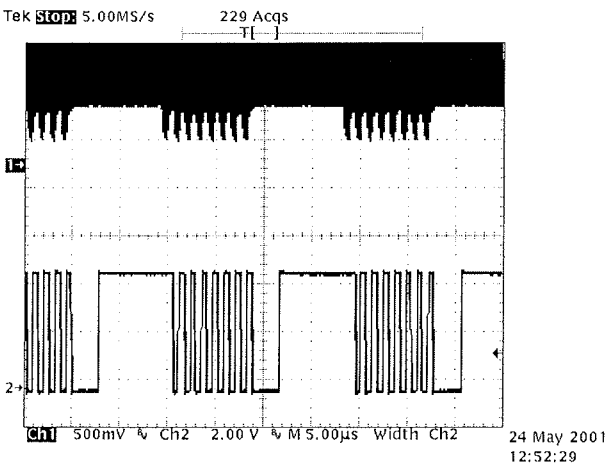

Figure 9: 848kHz subcarrier, on/off keying, distance 0.5cm Upper trace- RF in, lower trace - digitized output

3. Conclusion

The receiver stage for a single chip RFID integrated circuit was designed in a 1µm CMOS process. A special attention was paid in the layout phase to minimize capacitive and substrate cross-talks between the receiving and transmitting part not to corrupt receiver input noise or stability of the system. The chip was evaluated both as a standalone AM receiver and as a part of an RFID transmitter-reader system. The input noise level of 7µV/√Hz at 100kHz enables a system sensitivity of 1.5mV_{PP} at 1000kHz bandwidth. When operating with an associated on-chip low power transmitter (20dBm) the single chip reader system can communicate with a card size transponder in a 15cm-17cm operating range depending on a system used.

4. Acknowledgement

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5. References

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Anton Štern, Janez Trontelj
Faculty of Electrical Engineering
Tržaška 25, 1000 Ljubljana, Slovenia
E-mail: tone@kalvarija.fe.uni-lj.

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