MIXED SIGNAL ASICs - A MANUFACTURER´S VIEW

Volker Kempe
Austria Mikro Systeme International AG, Unterpremstätten, Austria

INVITED PAPER
33rd International Conference on Microelectronics,
Devices and Materials, MIDEM´97
September 24. - September 26., 1997, Hotel Špik, Gozd Martuljek, Slovenia

Keywords: semiconductors, IC, Intergrated Circuits, ASIC circuits, Application Specific Integrated Circuits, MS ASIC, Mixed Signal ASIC, MS, Mixed Signals, wirebound communications, wireless communications, microelectronic technologies, high perfomance, submicron technologies, technology trends, market share, design tools, automotive electronics, industrial electronics

Abstract: Mixed Signal ASICs play an important role in the ASIC market. In most applications, they fill the gap between internal information processing and the external world. This causes a need for a broad variety of microelectronic technologies aimed at fulfilling the often completely different requirements for supply and operating voltages, for input and output currents, for signal frequency ranges, for accuracy and signal resolution capabilities, for ESD, EMC and robustness in harsh environments etc.

Complex signal processing combined with analog front end in wireless and wirebound communication, high gate count embedded in high voltage interfaces for harsh environments in automotive and industrial electronic and the combination of signal conditioning in microsystems are the challenges for MS ASICs.

System integration on chip in submicron technologies including high performance analog blocks requires powerful and robust MS processes, a combination of high level design automation for digital blocks with interactively driven design tools for analog blocks and a changing cooperation between customer and ASIC supplier.

Mešana ASIC vezja - proizvajalčeva perspektiva

Ključne besede: polprevodniki, IC vezja integrirana, ASIC vezja, MS ASIC vezja za signale mešane, MS signali mešani, komunikacije žične, komunikacije brezžične, tehnologije mikroelektronske, zmogljivost visoka, tehnologije submikronske, trendi tehnologije, delitev tržišča, orodja snovalna, elektronika avtomobilska, elektronika industrijska

Povzetek: Mešana vezja igrajo pomembno vlogo na tržišču ASIC integriranih vezij. V številnih uporabah ta vezja premostijo prepad med notranjo obdelavo podatkov in zunanjim svetom. To ustvarja potrebo po širokem spektru mikroelektronskih tehnologij, ki naj bi zadostile velikokrat različnim zahtevam za napajalne in delovne napetosti, za vhodne in izhodne tokove, za različna frekvenčna območja signalov, za točnostjo in ločljivostjo signalov, za ESD in EMC odpornostjo v težkih pogojih delovanja itn.

Zapletena obdelava signalov, združena z analognimi izhodi v žičnih in brezžičnih komunikacijah, velika gostota elementov v visokonapetostnih vmesnikih v zahtevnem okolju industrijske elektronike in avtoelektronike ter prilagajanja obdelavi različnih signalov v mikrosistemih, so le nekateri izzivi za mešana integrirana vezja.

Integracija sistema na čip v podmikronskih tehnologijah vključno z zahtevnimi analognimi bloki zahteva zmogljive in robustne mešane procese, kombinacijo avtomatiziranega načrtovanja digitalnih blokov in interaktivna načrtovalska orodja za načrtovanje analognih blokov, kakor tudi stalno sodelavo med stranko in dobaviteljem ASIC vezijih

Introduction

Mixed Signal (MS) ASICs represent two coinciding worlds:

- the world of ASICs and
- the world of Mixed Signal IC-Design.

The ASIC world is part of the IC universe, which is expanding like the real cosmos after the big bang with unlimited speed but with some fluctuations (Fig.1).

The IC-market expansion is based on

- the, historically unprecedented, development of microelectronic technologies which is now rapidly approaching 0.1 μm (Fig. 2) and
- an ever growing demand of applications for processing, storage, generation and transfer of information starting from signal acquisition and binary handshaking in simple control systems and ending with personal and mobil computing, communication, multimedia and integrated microsystems.

From the first transistor in Si-planar technology in 1959 (Fairchild) over the first ICs with transistors, resistors and capacitances by Texas Instruments in 1960 and the first microprocessor with 2300 transistors in 1971 (Intel) until Intel´s Pentium II with 7.5 Mio transistors and 266 MHz clockfrequency in 1997, produced in 0.35 μm technologies (some versions now in 0.25 μm), the chip complexity has grown 10 times in six years (approx. 50 times in 10 years) and the chip performance (related to microprocessor power) has increased 10 times in eight years. The DRAM complexity is even growing with a factor four in three years almost exactly following

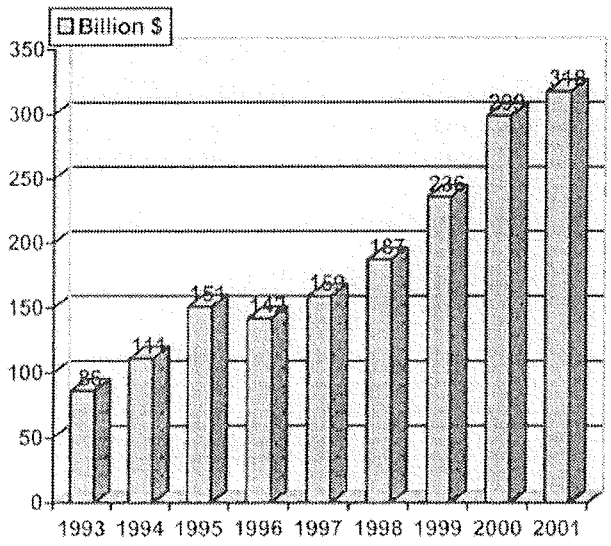

Fig. 1 Worldwide Semiconductor Market

Moore´s law (100 times in 10 years). Every 10 years the price/performance ratio (in stable currency) improved by a factor of 100.

Applying these breathtaking figures to the development of cars in the period 1960 - 1995, today one should be able to buy a Rolls Roys running 8 Mill. km with one litre petrol for less than 1.50 $.

Today highly improved production equipment in a perfect cleanroom environment allows the realisation of wafer defect densities in the order of 0.25 defects per sq.cm. Large chips with die sizes well over 1 sq.cm can be produced in volume production with yields exceeding 75-80 %. This trend is enforced by the econo-my of scale of growing wafer sizes leading to a more intense utilisation of the expensive production equipment. Nearly unlimited complexities can be integrated on chip with reasonable cost. The integration of separate functional components or subsystems on chip is substituted more and more by system integration on chip (or integration in dedicated chipsets). Memories are the only exception. Here the functional requirements for the main application areas (computers) with respect to memory size and speed („the hunger for information storage") have not yet reached a level of saturation, which would allow handling large memories like on-chip macros for system level integration. For instance, todays 64 Mbit RAMs are sufficient to store the information needed to code a genom of a bacteria; for the human genom 64 Gbit are required.

However, system integration has become a major target for many IC suppliers, because more and more customers discover the economy and relative simplicity of turnkey solutions in the form of systems or well defined subsystems on chip.

Especially ASIC suppliers are heavily confronted with this changing nature of the functional content of ICs. Indeed, system integration means the inclusion of product definition and functional system development in the ASIC development cycle, extending the classical implementation oriented IC design towards a complete product development. System design requires further specialisation and competence focusing. The broad range of applications served in the past by many ASIC suppliers has to be limited. New fabless design houses are filling the gap between specialised, system level supported IC and ASIC design and the need for serving an ever growing number of applications. Very often spin offs from universities or research institutes bring in special system level or architectural expertise, which is figured as starting capital of the new design house.

Also standardisation helps to bundle the technical requirements for similar applications or at least for similar subsystems and therefore limits this gap redu-cing the number of different components necessary for similar applications. Standards for cellular communi-cation systems like GSM and DCS 1800, DECT, CDMA or for broadband ISDN like ATM or for image coding like MPEG2 etc. have paved the way for open markets, higher volumes and represent an indispensable precondition to invest in very high integrated system solutions and components for them.

Parameter	1995	1998	2001	2004	2007	2010
Structure(μm)	0.35	0.25	0.18	0.13	0.1	0.07
DRAM (bits)	64M	256M	1G	4G	16 G	64 G
Gate/Chip	800k	2M	5M	10M	20 M	40 M
Supply (V)	3,3	2,5	1,5...2,5	1,5	1,2	0,9
Clock (MHz)	200	500	1000	1500	2000	2400
Metal-Layer	4...5	5	5...6	6	6...7	7...8
CPU-performance	15	30	40	120	200	240
I/O per Chip	750	1500	2000	3000	4000	5000

Fig. 2: CMOS Technology-Trends up to 2010

The technologies for most of the segments of the ASIC market - Gate Arrays including FPGAs, PLDs, Digital Standard Cell ASICs - follow the main stream microelectronic production processes with some delay (Fig. 3). However, driven by the price war in the DRAM sector and the quick alterations in microprocessor generations on the one side and the giant investment for new technologies and fabs on the other side, some large IC suppliers are pushing their way into the ASIC market using fabs and technologies, which were initially developed and used for DRAMs or microprocessors and which are no longer best suited for the newest technologies and products. Therefore, IC suppliers which concentrate on digital ASICs or on a mixture between dedicated logic ICs and digital ASICs are forced to speed up their development of minimum feature size technologies. All in all, the gap between the feature size of leading DRAM technologies and ASIC technologies becomes closer. In the area of MS ASICs (like in the Analog IC seg-ment) there are additional process requirements like analog performance, special RF or High Voltage features etc., which not only weaken this trend but lend a characteristic profile to the family of MS ASIC processes. For many applications specific performance parameters of active or passive devices are required which may outweigh digital performance parameters like gate density, gate delay, etc.

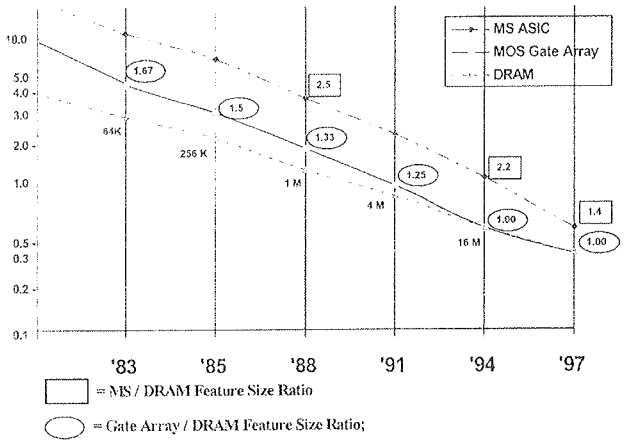

Fig. 3 ASIC Technology Trend

Very often the minimum size is not the most important requirement for MS ASICs (and even more for analog ICs), although with the growing content of digital blocks this basic characteristic of a process becomes increasingly important in the world of MS ASICs as well.

The specific requirements for some MS ASIC processes will be considered later.

The MS ASIC Market

Progress in process and technology development as well as the volume of investments in new fab lines and design tools are driven by the market situation. An ASIC manufacturer and even a MS ASIC manufacturer like Austria Mikro Systeme targets only a small, but important, segment of the IC market. However, this segment covers all application areas like Computing, Communication, Consumer electronics (the 3 large Cs), industrial and automotive electronics etc. and is closely linked to the whole IC market due to the simple fact that in most of the applications an appropriate mixture of the products of the different segments of the IC market has to be used.

The whole IC market, which drops in the critical year 1996 to an overall volume of $117 Bill., is growing with a compound annual growth rate (CAGR) of 19% . Memories and microprocessors/controllers represent nearly a two third share of the IC market. The dominant IC application areas are Computers with 55% of the worldwide IC usage (1996), Consumer Electronics with 16%, Communication with 15%, Industrial Electronics with 8% and Automotive Electronic with 5%.

Computer and Communication shares are expected to grow slightly in the next five years, however more important is the merge between computing and communication in networking and multimedia, the unbroken growth of mobile communication, the growing content of microelectronic components in cars, households and consumer goods and the entry of microsystems in the era of commercialisation.

According to Dataquest the content of microelectronic components in electronic products will double from 16% today to 32% in 2010, whereas the production of electronic products will triple in the same interval (750 Bill.$ in 1995). Microelectronics will penetrate in nearly every product. No reasons can be seen for slowing or even stopping the microelectronisation of todays technique.

ASICs will remain an important part of the IC production, offering the possibility of a customised solution for a special application and a given customer.

However, the nature of ASICs is changing. The boundary between ASICs and Application Specific Standard Products (ASSPs) developed for one application but for more than one customer become more and more fuzzy. Based on their own system definitions, ASIC vendors develop core products for selected application areas which can be used as ASSPs or modified for customer specific solutions (ASICs). This approach is especially important for complex systems and/or for a significant content of high performance analog blocks on chip which require a large design effort.

For Standard Cell or even Full Custom ASICs the time to market can be shortened considerably starting the ASIC design based on an appropriated core product or ASSP. Generally, in correspondence with the changing relation among design effort, production cost and the related customer benefits , the various segments of the ASIC market (Fig. 4) grow differently. Today (1996) the whole ASIC market with approx. $ 17 Bill. represents a 15 % share of the complete IC market. Due to the higher average sales prices per unit nearly four times, the market share in units is considerably smaller.

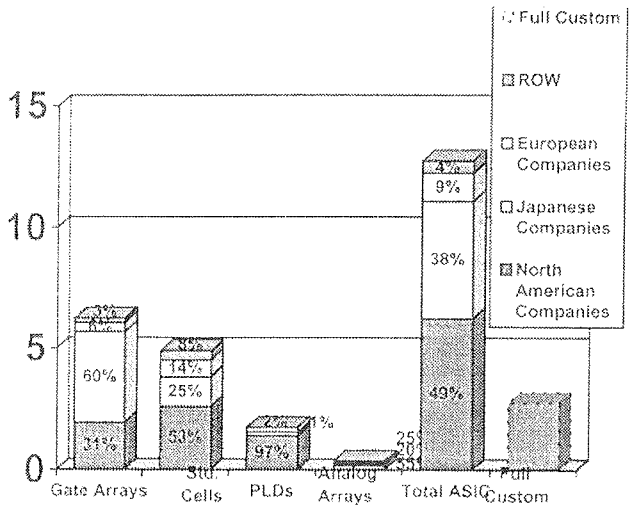

Fig. 4 ASIC Segment Market Share 1995

The ASIC market increases at an estimated rate of 18 % per year.

The fastest growing segment is (beside the FPGA subsegment) even the MS Standard Cell ASIC area with an expected annual growth rate of 26-30% (according to ICEs „ASIC 1997"/ „ASIC 1996"), which is well over the average growth of most of the other IC market segments. Some uncertainties in the whole MS ASIC area are caused by the lack of information on the Mixed Signal part of the Full Custom ASIC segment. The 26% to 30% are therefore related to the MS Standard Cell ASICs, which represent the largest part of the MS ASICs.

Gate Arrays are losing, complex PLDs are gaining some additional shares.

The driver applications for MS are

- the global wireless communication including cellular voice and data communication as well as multimedia and
- the local wireless or wire bound communication based on RF to Infrared local communication for voice and data transfer and for local multimedia access.

(Laurie Stanley from Cadence called this convergence of multimedia, communication and computing the consumerization of electronics /1/.)

In 1996, the market for cellular communication has seen more than 50 Mill users. For 1999 optimistic forecasts expect more than 500 Mill new subscribers.

Spin-offs are GPS, environmental, traffic and industrial control, medical care and households.

Austria Mikro Systeme is well established in the $ 6,2 Bill Standard Cell ASIC market and ranks sixth in the approx. $ 2 Bill MS ASIC market (1996). The Austria Mikro Systeme Group has to be placed as Number 5. MS Std. Cell ASICs represent more than 75% of the business of the company. The main application areas are Communication, Industrial and Automotive Electronics.

In front of the weak position of European companies in the IC market which serve only a 9% share of the worldwide IC market, the 14% share in the Standard Cell ASIC segment and the even higher share of more than 25% in MS-Standard Cell ASIC is a remarkable exception demonstrating the often stated European competence in Mixed Signal design and production. Austria Mikro Systeme is one of the representatives of this leading European position. The leading US publication „Semiconductor International" in its March issue rates Austria Mikro Systeme as one of the very few companies which will have a fundamental influence on the strategically important segment of ASICs in the future.

Driving Forces for Mixed Signal Design

MS design is not the simple sum of digital design of well defined parts of the chip plus transistor level oriented design of predefined analog blocks. The latter is typical for analog ICs. MS design is a tightly coupled design of digital and analog functions including their definition, architectural mapping, block specification, circuit design including MS simulation, and physical implementation.

Not seldom the analog part in modern ICs represent only a small part of the area. However the design time occupies an inversely large part of the whole design cycle, the design has a much higher risk and often causes redesigns.

There are three tendencies in the world of MS design:

1. the growing role of analog and MS effects and of MS parts in deep submicron digital ICs
2. the increasing importance of digital signal processing (DSP) forcing the substitution of analog functions by their digital functional equivalents
3. the rapid growth of MS ICs, especially ASICs and ASSPs

1. Analog effects at gate, block and system level in deep submicron digital ICs like interconnect delay, power dissipation, complicated timing behaviour of digital standard cells for a large range of operating conditions, substrate crosstalk, ground bounce and power bus noise, electromigration, dependencies from neighbourhood etc. confront the digital designer with typical MS design problems. Additionally, analog blocks like VCOs and PLLs for high performance clock distribution become an indispensable part of the design.

Most of the new problems in digital submicron design are attacked by the whole EDA industry and the large IC players by developing new tools, methods and design flows. Quick and safe solutions are necessary in order not to delay the comprehensive usage of the newest manufacturing technologies. New products like SNAKE TECHNOLOGIES´ Layin-software for substrate modelling and crosstalk analysis based on 3D extraction of coupling models, CADENCE´s 2 1/2 D extraction software or IBM´s power bus noise analysis methodology /3/ (not yet commercialised) demonstrate that not only the key problems of digital design can be effectively

solved but MS design can benefit from the „analogisation" of digital submicron design.

2. The tendency towards digitalisation of signal processing seems rather to increase the MS- IC world than to weaken it. Indeed, in the past, digital signal processing was mainly realised as PCB- integrated systems based on dedicated Digital Signal Processors and analog ICs for signal conditioning, pre- and postfiltering and AD and DA conversion. These solutions migrate more and more in one chip MS systems often including additional functions. DSP cores like GOULD´s PINE or OAK or Austria Mikro Systeme´s GEPARD as well as improved design environments for hardware-software codesign support this migration and open the way for new applications. Powerful analog blocks like high performance AD and DA converters are crucial elements in expanding the digital signal processing to higher signal frequencies, increased accuracy, low supply voltages and low power consumption.

3. The area of MS ICs covers a broad spectrum from simple extensions of digital circuitry towards the integration of analog I/0 functions up to the realisation of high performance analog and complex digital blocks on chip.

The functional and structural partitioning of an ASIC in analog and digital subfunctions and blocks requires a careful evaluation by experienced designers. The advantages of digital parts like robustness and easy design as well as the disadvantages of analog circuitry like sensitivity against noise disturbances and interference, susceptibility to process variations, to mismatching, to inaccurate device models, high design effort and risk etc. must be weighted against the cost of an appropriate manufacturing process, the die size, the power consumption, the reliability, the overall design costs, the possibilities of sharing design work, the test effort etc. In conjunction with the growing submicron possibilities, digital realisations will substitute analog functions where possible.

However, very often the driving force for an analog realisation of functional blocks is the impossibility of a digital realisation. The limitations for digital realisations are determined by

- the necessity of analog interfaces to the external world
- high signal frequencies not allowing precise AD-conversion and/or real time digital signal processing

For many interface functions, digitalisation is taking place, too, e.g. for driving an external load with low pass characteristic like a loudspeaker membrane. Here the analog output amplifier can often be substituted by a simple digital output stage driven by a pulse modulated signal. Pulse based techniques (pulse width, pulse frequency, pulse density, stochastic logic) are the favourites for digitalisation at the border area between analog and digital. However, for high voltage environments or smart power applications an analog signal conditioning, power matching and/or distur-bance handling is necessary. Special high voltage processes with usually purer digital performance are required here to handle the necessary voltage range.

Mixed Signal Process Technologies:

MS processes have to keep the digital performance of the basic process but are enhanced by different features necessary for the realisation of analog blocks. It has to be emphasised that one of the basic requirements for a MS process is not only the addition of new analog properties respectively process modules like linear poly capacitances and resistances or special active devices but a perfect control and an excellent characterisation of the basic process itself. Low threshold voltage spread, good matching properties of active and passive devices, stable and well controlled AC-parameters of MOS transistors in the saturation region, low resistive and capacitive device and interconnect parasitics etc. can be obtained using a well controlled and characterised digital process may be with slight modifications as for instance for improved active area surfaces necessary for better noise behaviour.

Of course, dedicated processes for MS RF or for High Voltage applications have to start from appropriate device concepts rather than to take a high density process and to extend this process for RF or HV requirements.

Let´s consider the most important requirements for MS ASIC technologies and some consequences for the MS design:

1: Noise

The accuracy of voltage (or current) levels in digital systems must be sufficient for an error-free recognition of the status information. In binary systems only two levels have to be differentiated. In analog systems the signal is characterised by a continuous set of states which must be recognised with an accuracy sufficient for the reconstruction in a given failure interval. The accuracy limits are determined by static and dynamic distortions and by the Signal to Noise Ratio.

The theoretical limit for the required power to achieve a given SNR over a given bandwidth f is

$$P = 8xkTxSNRxf$$

In practice, the additional power consumption due to auxiliary circuitry as well as the additional noise coming from the whole environment will increase the necessary power by up to more than one order of magnitude. However, the basic dependencies such as the usualy linear impact of SNR and bandwidth are sufficiently correct reflected: good SNRs over large bandwidths require large currents and consequently large transistors.

This situation is nearly independent on the process technology because the SNR for MOS transistors does not change significantly with the transfer to a new submicron technology.

Indeed, for the same device area the thermal noise of a transistor can be slightly reduced due to the increase of Gm. However, this will be roughly compensated by the reduction of the power supply in the deep submicron area shown in p.2.

Consequently, the area of low noise analog cells will remain nearly constant for different CMOS technologies whereby the digital cells approximately follow the area reduction of the minimum devices.

In Fig. 5, a Mixed Signal ASIC with relatively high analog content in the form of some low noise amplifiers is shown, ported from 1.2 μm to 0.6 μm. The analog part couldn't be reduced. The digital part was reduced in area by nearly a factor of four.

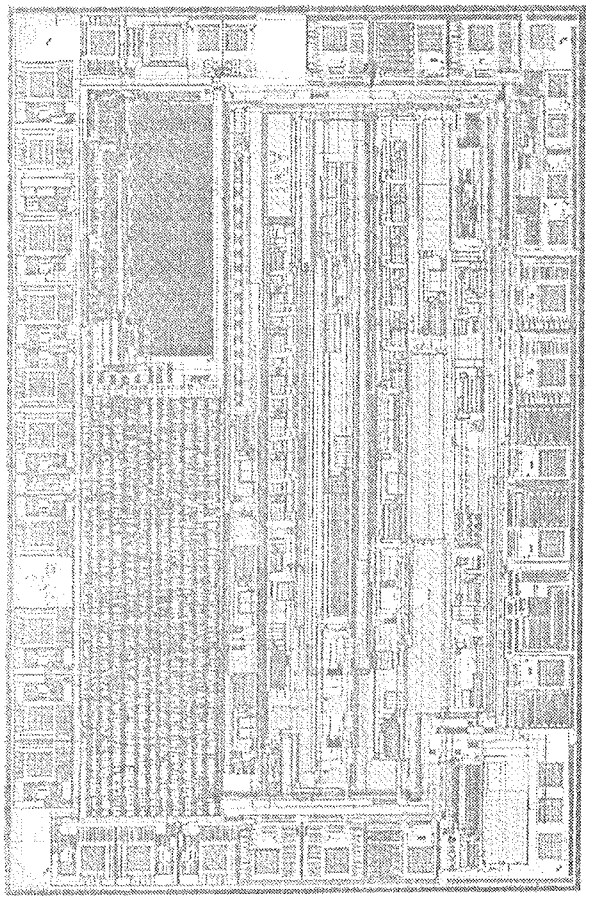

Fig. 5 Mixed Signal ASIC

As can be seen, the improvement of analog noise performance is barely related to the minimum feature size as is the case for digital systems. However, in case the noise is not the dominant factor, analog design benefits from improved dynamic behaviour of active and passive elements in the submicron area.

2: Power consumption

The on chip system integration requirement drives MS technologies in the submicron area. ICs with large digital part as for instance baseband chip sets for mobile communication represent an increasing share of MS ASICs. Therefore, gate density and speed remains an important criteria and the trend to submicron processes is nearly as important as for digital processes (at least for CMOS based technologies). The typical power problems of submicron LSI are imported in the MS area. Roughly speaking, they can be divided into the followings:

- power necessary for fast internal circuit switching must be dissipated
- large currents are needed for fast output drivers and limits their numbers
- the large currents need lower wiring and bonding resistances

For instance, the switching power P = fxCx V^2 for a f=250 MHz clock speed and an overall active load of C=10 000 pF results for a p-p swing of V=5 V in more than 60 W which have to be dissipated requiring a careful thermal management. To avoid unacceptable derating the junction temperatures should be not higher than approx. 120 °C. Low thermal resistances between junction and package as well as special, expensive packages with enlarged surfaces and good airflow are required. However reducing the peak to peak swing to 1 V drops the power down to 2.5 W - a value which can be much more easily handled. Sophisticated design techniques to reduce switching activities (asynchronous logic) and/or load capacitance (Full Custom design) can further help to decrease power consumption. However, the quadratic impact of V is the most important limitation forcing the decrease of the supply voltages at least at the entry to the sub-half micron area (Fig.6). The consequence is a reduction in the dynamic range of analog signals. This, in conjunction with the nearly constant threshold voltages of MOS devices (lightly decreasing with smaller feature sizes), requires new and more powerful circuit techniques to be developed, with the emphasis on low current and low power even at high frequencies.

The low power design of analog blocks at low voltage supply is one of the biggest challenges in deep submicron MS design.

The current necessary to switch a single output at a given speed is I = CxdV/dt.

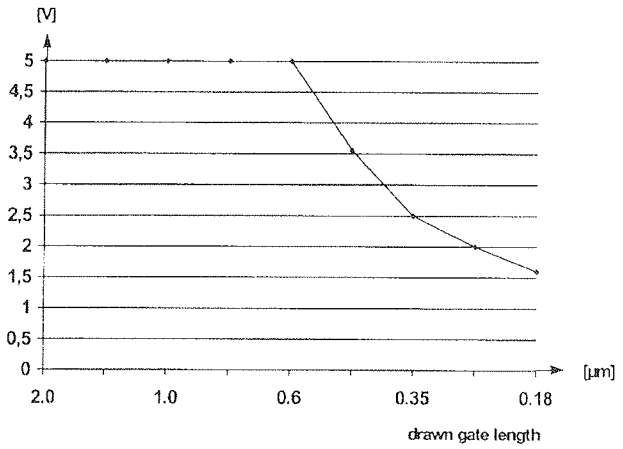

Fig. 6 Supply Voltage Reduction

Assuming a load capacitance of 10 pF, rise time of 100 psec and a swing of 1 V, a peak current of 100 mA is necessary. Only a large transistor in the order of some hundreds of the minimum device will guarantee a small enough output drop of say 100 mV. Intermediate buffers between the minimum internal gate and the final output device are needed. Therefore, a large area is required for handling the output. For a 32 bit bus interface, the peak current will reach 3.2 A. The examples can be easily extrapolated for higher speeds and gate counts.

Adding together current hungry outputs, switching power and current consumption for even current intense analog blocks, a power consumption in the order of Watts become a typical value rather than an exception. According to SIA´s roadmap the maximum power consumption for ASICs will be in the order of 5 W/ sq.cm for 0.5-0.35μm technologies and increase up to 10W/sq.cm for 0.18μm technologies.

The required currents of some Amps must be brought on chip and distributed. This means that power distribution in bond and interconnect wires becomes a significant factor. The cross-sectional area must be high enough and the specific conductance must be decreased. Copper-doped aluminium instead of aluminium seems to be the next choice for the submicron metallisation followed possibly by pure copper wires.

The consequences for analog blocks on chip are positive because analog parts do not shrink in the same order as digital logic with the migration to submicron technologies. The internal interconnect wires may remain in the same dimension as active analog elements. Therefore the weight of resistive parasitics should decrease.

3: Matching

Good matching of active and passive devices is one of the most important criteria for analog design. The process dependent parameter spread of all devices is in the order of some percent. Typical 3 sigma values are well over 10%. The only way for the construction of precision analog blocks is to exploit the much better relative accuracies of devices which inversely improves with the distance between them.

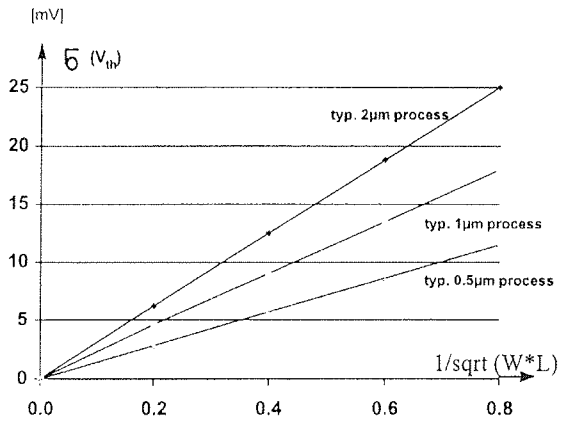

Fig. 7 Area Dependence of Vth Matching

The matching parameters improve for submicron technologies. According to /4/ the threshold voltage matching for a 0.5μm process is more than two times better than for a 2.0 μm process. Fig. 7 shows this behaviour for different transistor areas.

Passive linear elements like poly resistors and capacitors in Austria Mikro Systeme technologies can be matched with accuracies in the order of 0,1% or even less, high resistive poly resistors with 0.15-0.3% precision, however according to Austria Mikro Systeme´s internal measurements, there is no signifi-cant improvement with scaling down technologies.

4: High frequency analog processing

Wireless communication is the driving force for the on chip integration of high frequency analog processing (as for low noise input amplification, up and down mixing, synthesis of local oscillator frequencies etc.) together with analog IF and/or baseband modules and digital baseband processing / system control.

For input frequencies in the GHz range fast bipolar transistors must be combined with dense CMOS devices leading to modern BiCMOS processes. Modern BiCMOS processes like Austria Mikro Systeme´s 0.8 μm BYE (Fig. 8) combine

- vertical npn-transistors with high ft and low parasitic capacitances to substrate
- capacitors and linear resistors with low parasitics
- CMOS devices and
- the possibility for the integration of inductances.

	0.8 µm	0.6 µm
Status	production	in developt.
Technology	2 poly/2 metal	2 poly/2 metal
	15 masks	16 masks
poly/poly caps	+ 1 mask	+ 1 mask
High Res resistor	+ 1 mask	+ 1 mask
trench isolation	optional	+ 1 mask
CMOS		
Vth/Vtp (V)	0.70/-0.75	0.70/-0.80
L_{eff}	0.65 µm	0.55 µm
Bipolar		
Ft	12 GHz	20 GHz
Beta	110	110
Cjs (fF)	57(trench:30)	45(trench:20)

Fig. 8 AMS BiCMOS Technology

The low impedance substrate requires special attention to avoid noise coupling between CMOS logic and analog blocks (e.g. differential logic in ECL or CMOS with separate substrate connections). SOI processes which offer excellent substrate isolation properties, are under discussion. SiGe Heterojunction Bipolar Transistors integrated in CMOS may be another alternative to improve RF integration on chip.

5:High Voltage inputs and outputs

At present some automotive and industrial peripheral ASICs must withstand static levels up to 50 V and even higher impulse levels. Special high voltage NMOS and PMOS transistors must be integrated. To easily adapt low voltage parts, floating NMOS, PMOS and DMOS devices are advantageous. More expensive processes have additional vertical bipolar devices (BCD processes). Austria Mikro Systeme´s 2.0μm and 0.8μm CMOS technologies are used for ASICs with high voltage in- and outputs, voltage regulators and level shifters as well as with analog and digital blocks working at 5V supply voltage, which is generated on chip. The transfer of this concept in even deeper submicron areas is a big challenge as well as the extension of the voltage range up to 100V and higher, which opens the way in complete new application areas.

6: Adding Microsystem Technologies

Microsystems are leaving the halls of academic research and entering into a growing number of indu-strial and commercial ventures. With the industrialisation of microsystems the link between microelectronic and microsystem technologies have become closer and closer. For cost reasons, microelectronic compatible technology steps, which can be piggybacked to a MS-base technology, have proven to be crucial for the success in microsystems.

However, microsystems are not based on a generic element as is the case in micro-electronics. Here the transistor is used as a switch for voltages (or currents) in digital systems or as element operating voltages and currents at the same time in analog systems. Microsystems bring in additional physical domains like mechanical deflections, electric, magnetic and electro-magnetic fields - later up to optical wavelengths etc. Handling these domains usually requires exploiting effects and structures, which are foreign to microelectronic systems. Some well known exceptions are the usage of „parasitic" dependencies in microelectronic structures like the temperature dependency of transistors or resistors which can be the basis for temperature measurements, or the dependency of current distribu-tion in a resistive plate (n-well) which can be the base for magnetic field measurements by constructing Hall elements on chip. However, even in these cases, special package technologies for adapting the chip to the new application must be added.

Generally, a nearly unlimited number of already existing and new technologies has to be integrated in microelectronics to cover all possible effects. A carefully evaluated selection of piggyback technologies is necessary to cover effects and applications as much as possible.

Austria Mikro Systeme has developed a special etching technology for bulk micro-machining and a special joining technology for sealing together conducting Si-structures. So, mechanical beams and membranes can be integrated in an MS ASIC. These technologies open the way to a broad range of acceleration and pressure sensors.

Similar combinations - some of them integrated under one roof, others handled in cooperation between different technology suppliers - will enhance MS proces-ses and enforce the merge between microelectronics and microsystems.

7: Robustness and statistical models

Typical volumes for ASICs cover a broad range from some thousands up to millions of units. Prototype runs for products under development represent very low volume production. MS ASICs are implemented in the best suited, but different processes. Therefore, an ASIC fab has to run a broad spectrum of different products in different processes and relatively low volumes.

Due to the increasing wafer size (8" and even 12" wafers) the number of wafers needed for a given product will decrease down to single (and sub-single) wafer production. Statistical monitoring of fab in-line and electrical test parameters will become insufficient for process fine tuning. Robust, insensitive against small modifications of primary process input parameters (equipment, material etc.) processes have to be established based on sensitivity simulations.

However, robustness does not only mean insensitivity against primary process parameter variations but includes insensitivity against environmental parameters like humidity, pressure, radiation as well as ESD, EMV and latchup. A basic requirement is a negligible impact of a given layout on the electrical test and device parameters.

The process sensitive design of high performance analog blocks as well as the analysis of sensitive MS effects require a hierarchy of statistical models of electrical test parameters, device model parameters, parameters of the elementary building blocks and of subsystems. This hierarchy can be used for statistical simulations at various levels and for optimisation of a given design (design related yield improvement). Statistical matching models must be integrated. The methodology for automatic generation of the parameter distributions for the various models at different design levels as well as the automatic generation of compact parameter sets for Monte Carlo simulations at this design levels has to be improved and integrated in the standard MS design flow. Hierarchical optimisation techniques are needed for a sophisticated truncation of the parameter space at a given design level.

European semiconductor companies have concentrated their efforts to develop sophisticated mixed analog/digital sub half micron processes in the framework of the European SHAPE project. The goal is to further improve the good position of European companies in the MS area. Participating in SHAPE Austria Mikro Systeme focuses now on the implemen-tation of a powerful 0.35 μm MS process fulfilling the above mentioned criteria.

MS Design Tools and Environments

Design efficiency is the main target for creating MS design tools and environments. Efficiency includes safety because any faulty design may cause an additional fabrun and a redesign.

The growing gap between chip complexity and design productivity must be closed

- by fully integrated design environments even for MS design
- by standardisation of tools and languages
- by rapidly extended reuse of blocks, subsystems and complete designs.

Today, the leading edge MS design systems are top down oriented and based on a combination of second generation analog Hardware Description Languages like HDL-A, VHDL-A,VERILOG-A and well introduced digital HDLs like VHDL or Verilog.

Austria Mikro Systeme offers front-to-back design kits for CADENCE and MENTOR tools. Special userware and scripts guarantee a smooth integration and fast simulation.

The principal design flow is shown in Fig. 9. a and b.

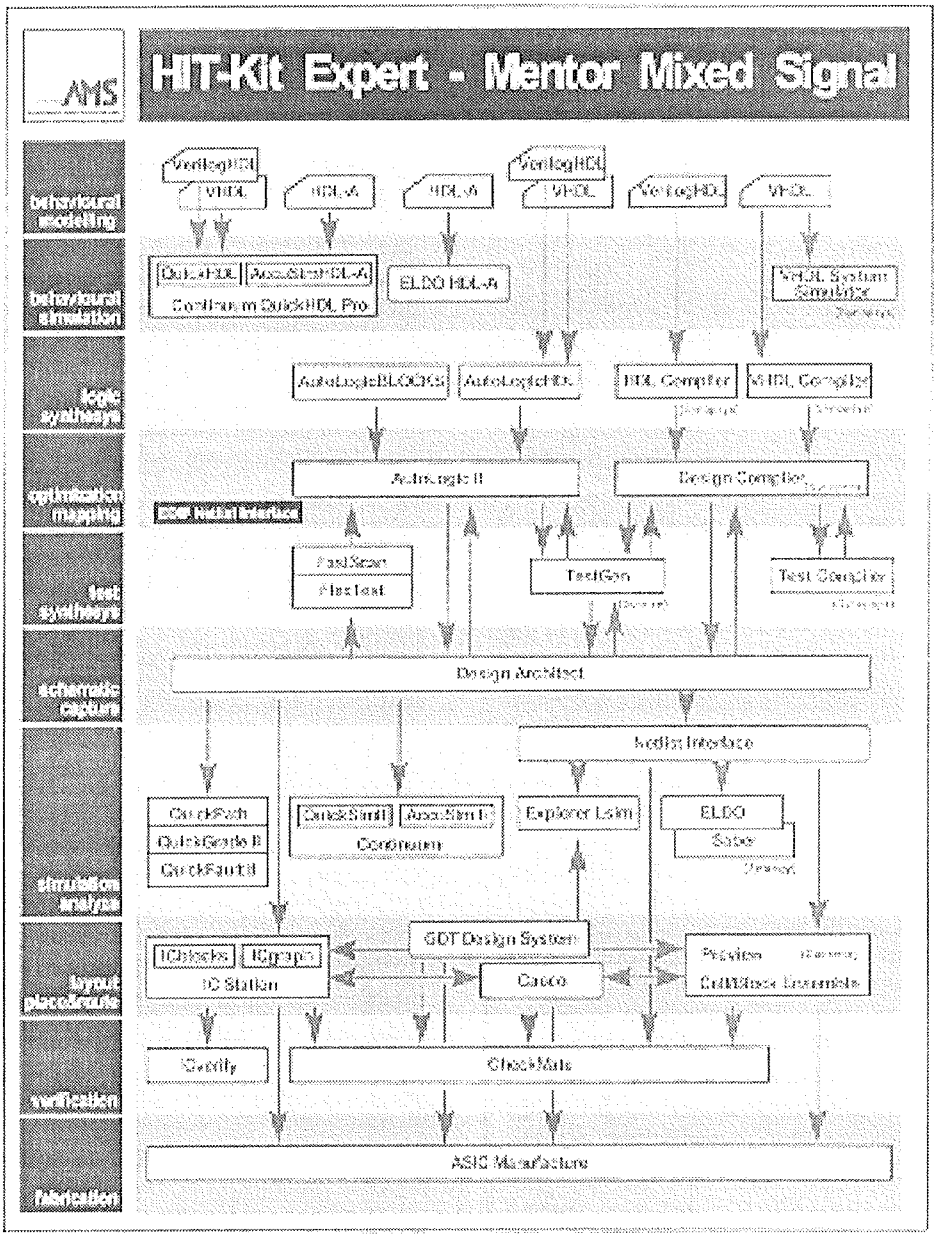

Fig. 9 a

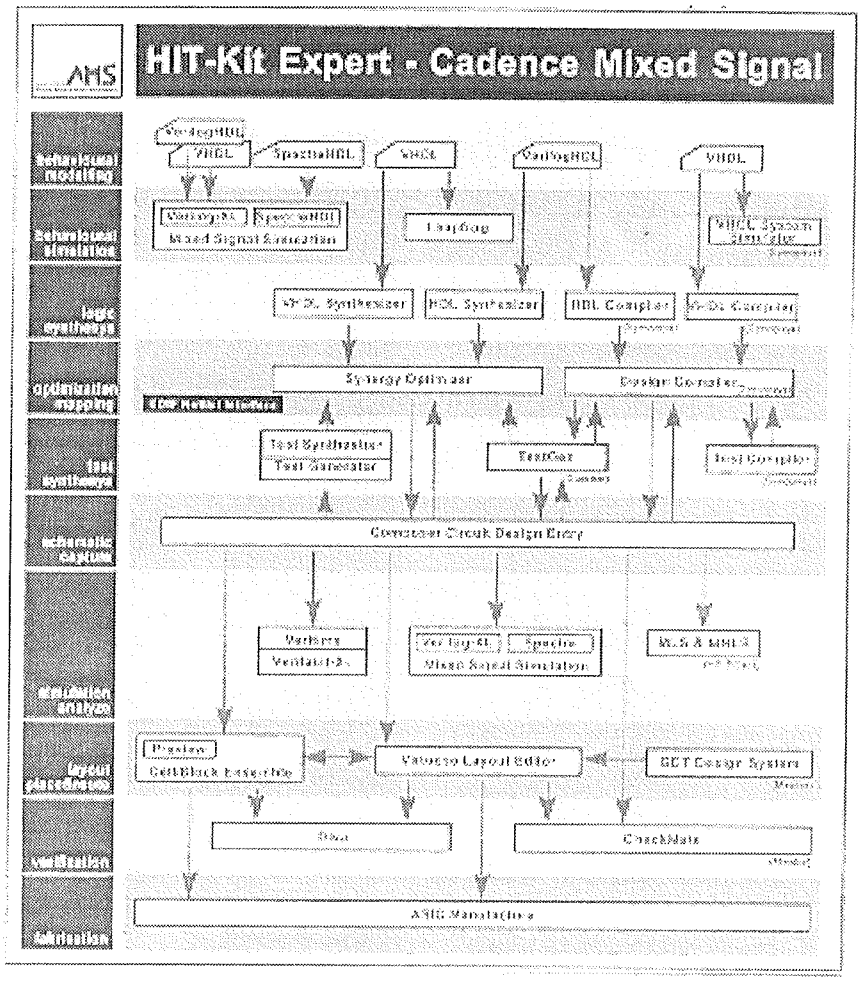

Fig. 9 b

Block type	Flexibility vs.predictability	Representation	Process technology	Portability
Soft	Very flexible, unpredictable	Behavioural: synthesizable RTL-description or netlist of generic library elements	Independent	Unlimited
Firm	Flexible, unpredictable	RTL, blocks: synthesizable RTL code or netlist of generic library elements, structurally and topologically optimised by floorplanning, placement for specific process families (not routing)	Generic	Library mapping
Hard	Inflexible, predictable	Polygon data -Layout	Fixed	Process mapping

Fig.10. Reusable blocks

HDL-A in combination with VHDL, Verilog A in combination with Verilog and other combinations can be used for high level simulation of MS systems. Different simulation techniques can be applied. Either cosimulation back-planes for synchronisation of analog and digital simulators such as ELDO, SpectreHDL (later with fully integrated Verilog A simulator) on the one hand and LEAPFROG, Quick-HDL on the other hand or digital extensions of analog simulators as announced for ELDO are state of the art. The EDA vendors permanently try to improve the tools and methodologies. The situation is changing very quickly confronting the design houses and ASIC suppliers often with new releases despite not having reached satisfactory performance level using the last release. Despite the success in language standardisation and simulation environments, there is still a long way to go until simulation engines become available based on standardised languages describing digital and analog functions with the same tool.

Verilog A/MS being the analog/mixed signal extension of Verilog by Open Verilog International (OVI) may be one of the candidates. Verilog A/MS standard was taken by the IEEE to create a more general version, compatible to the IEEE 1364 Standard from 1995. A new standard - IEEE 1364 - 1998 is planned and will be certified next year. An analog/mixed signal standard for VHDL-A is still missing.

Standardised MS HDLs shift the design from a schematic based methodology to a language based one. They are not only the precondition for the top down design but are absolutely necessary for Intellectual Property (IP) reuse, because proprietary descriptions are a serious barrier for mixing and matching foreign and own macros.

IP reuse has become a catchword. The invoked vision of a 90% share of reuse in designs in 2001 against a maximum of 10% reuse in 1991 seems to be unrealistic at least for MS designs.

However, the methodology and standardisation efforts for IP reuse are growing fast and are supported by a group of more than 80 leading electronic companies. The future reuse of System Level Macros (SLM), Cores and Megacells shall be based on the Virtual Socket Interface (VSI) concept, defining the form and content of information which has to be passed from the IP creators to the users. Interface standards shall transform the blocks into virtual components that fit into virtual sockets at functional and physical levels.

Soft, firm and hard blocks (Fig. 10) are the basic elements for a block based design.

A steadily growing number of companies are entering the IP supplier community. Nearly 2/3 of the worldwide IP business is created in California. However, only very few IP creators offer MS or analog blocks.

The reasons are principal: Process and design sensitive analog blocks have to be represented as hard blocks. Process mapping is then necessary which limits the applicability of IP reuse in MS design.

Analog synthesis would help to shift these borders. However, synthesising multi-parametrical, multistructural and multicriterial analog blocks is not comparable with digital synthesis. Digital synthesis is an intelligent decomposition of Boolean functions. The existing approaches for analog synthesis like simulation or equation based selection of structures and parameters or design plan based iterative searches are in fact analytic methods, applied to different representations of more or less predefined segments of the search space. Even the choice of the necessary minimal dimension of the structural search space is an unsolved problem.

Analog synthesis is not a problem of computational power but of adequate modelling of analog functions and their decomposition into elements, which can be mapped onto simple topological structures. Progress in analog synthesis will be made only in small steps. IP reuse of analog macros will remain rather the exception than the rule. However, the creation of analog macros by specialists or specialised small teams , which offer appropriate support for the adaptation of these blocks to a target process, seems to be a promising way for the reuse of analog core competencies.

Conclusion

Mixed Signal ASICs are quickly entering the sub half micron technologies. The integration of complex systems on chip changes the nature of design. System design aspects become as important as the implementation. Specialisation at system level changes the whole IC industry, creating fabless design houses supplementary to the well established in-house development of IC companies. Foundry business is growing correspondingly. The MS ASIC industry supports this trend offering steadily improving design support at the implementation level. Dedicated MS processes and powerful design tools are being developed and made available to customers and design houses. Analog effects such as noise, parasitic couplings, distributed system behaviour at RF, on chip statistical variations of device parameters etc. must be simulated and integrated into the top-down and bottom-up design flows. The standardisation of MS hardware description languages for the behavioural description of blocks and ICs supports shared design and IP reuse. High performance MS ASICs will be used in well known application areas such as communication, industrial and automotive electronis and will open the door for new applications, many of which will be in conjunction with the entry of microsystems in all spheres of our daily life.

References

/ 1 / Cheryl Aljuni, Analog/Mixed-Signal Standards Needed For Next Generation Design Tools, Electronic Design Automation, April 14, 1997; pp. 65 - 75

/ 2 / C. Forzan, B. Franzini, C. Guardiani, Accurate and Efficient Macromodel of Submicron Digital Standard Cells, Proceedings 1997, DAC, pp. 371 - 376

/ 3 / H.H. Chen, D.D. Ling, Power Supply Noise Analysis Methodology for Deep Submicron VLSI Chip Design, Proceedings 1997, DAC, pp. 638 - 643

/ 4 / P. Kinget, M. Steyart, Impact of transistor mismatch on the speed-accuracy-power trade-off of analog circuits, Proceedings of IEEE CICC 1996, pp. 333 - 336

/ 5 / M. Pelgrom et al., Matching properties of MOS transistors IEEE, Journal of solid-state Circuits, Vol. 24, n° 5, pp. 1433 - 1439, 1989

/ 6 / Status 1996, A Report On The INTEGRATED CIRCUIT INDUSTRY, Integrated Circuit Engineering Corporation

/ 7 / Status 1997, A Report On The INTEGRATED CIRCUIT INDUSTRY, Integrated Circuit Engineering Corporation

/ 8 / Stanley T. Myers, The Realities of Conversion to 300 mm Silicon Wafers, Semiconductor International /83 April 1996

/ 9 / D. Alles, G. Vergottini, Taking A Look At Internet-Based Design In The Year 2001, Electronic Design / January 6, 1997

Dr. Volker Kempe
Austria Mikro Systeme International AG,
A-8141 Unterpremstätten, Austria
tel. +43 3136 500
fax + 43 3136 500 347

Prispelo (Arrived): 15.09.1997 *Sprejeto (Accepted): 09.12.1997*