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VSEBINA **CONTENT**

A first timer's experience of a MIDEM conference

Marija Kosec has many times told me about the very big and active MIDEM organization and its conferences so it was with great interest I went for my first personal experience of such a conference.

And reality turned out to be better than the prospect!

A large number of very high-level papers were presented, with a clear dominance of local or neighbor country speakers. When it comes to R&D in ceramics Central and East Europe is very strong and MIDEM (and other IMAPS Chapters) is really a catalyst making these laboratories communicate and share experiences and know-how!

It is a pity that the local microelectronics industry is growing pretty slowly in these countries. Especially in Slovenia the infrastructure is now very rich and the level of education high so a good future is easy to predict, but when?

One of the outstanding factors was also the language; all speakers were very clear and correct in their English, an important factor when only a minimal minority (if any!) of participants had English as their first language. The topic area of MIDEM is much wider than in most IMAPS Chapters, but most papers still generated a discussion, time allowing, showing the broad education of the participants and their habit to think interdisciplinarily.

To utilize the trip fully I spent the weekend in Slovenia sight seeing wonderful castles, enormous caves (20 km long !) and mountain areas. How can such a small country accommodate so many natural and historical wonders?

I want publicly to thank all the conference organizers with Marija Kosec and Darko Belavic in the top for all hospitality and an excellent IMAPS event!

Paul Collander

Nokia Networks

IMAPS Nordic President

SOLUTION SYNTHESIS OF $Pb(Zr,Ti)O_3$ CERAMIC NANO-POWDERS

Barbara Malič, Marija Kosec

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INVITED PAPER
MIDEM 2002 CONFERENCE
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Key words: $Pb(Zr,Ti)O_3$ (PZT), nano-powder, solution synthesis, ceramics

Abstract: Solution synthesis of multicomponent ceramic materials, such as $Pb(Zr,Ti)O_3$ (PZT), should yield better homogeneity, chemical purity and lower processing temperatures as a consequence of nano-meter range particle size in comparison to solid state synthesis.

Synthesis of stoichiometric PZT ceramic powders with the Zr/Ti ratio 50/50 based on hydrolysis of n-butoxide-derived heterometallic complex was found to yield loosely agglomerated powders consisting of about 100 nm-sized aggregates that could be sintered to almost theoretical density at 1000°C, a temperature a few 100 °C lower than those typically used for solid-state synthesized ceramics.

Priprava nano-prahov $Pb(Zr,Ti)O_3$ (PZT) iz raztopin

Ključne besede: $Pb(Zr,Ti)O_3$ (PZT), nano-prah, sinteza iz raztopine, keramika

Izvleček: Sinteza iz raztopin večkomponentnih keramičnih materialov, kot na primer $Pb(Zr,Ti)O_3$ (PZT), omogoča doseganje večje homogenosti, čistoče in nižje procesne temperature v primerjavi s klasično sintezo v trdnem stanju.

Sinteza prahu $Pb(Zr,Ti)O_3$ z razmerjem Zr/Ti 50/50, ki ga sestavljajo približno 100 nm agregati, temelji na hidrolizi heterometalnega butoksidnega kompleksa. Keramiko s skoraj teoretično gostoto pripravimo po toplotni obdelavi pri 1000 °C, kar je nekaj 100 °C niže od značilnih temperatur sintranja keramike, pripravljene s sintezo v trdnem stanju.

Introduction

In the last years the research of the solution synthesis of ceramic powders has increased due to the potential advantages of better homogeneity, chemical purity and nanometer-range particle size in comparison to the solid state synthesis. Alkoxide based sol-gel processing is one of the various solution syntheses; it is based on the reactions of hydrolysis and polycondensation of metal alkoxides $M(OR)_n$ shown schematically by Eq. 1 - 3 /1,2/. In the first reaction the reactive alkoxide groups are exchanged by hydroxyl groups in the extent depending on the amount of water and in the following ones the metal-oxygen-metal bonds are formed.

Hydrolysis: $\text{M-OR} + \text{HOH} \rightarrow \text{M-OH} + \text{ROH}$ (1)

Polycondensation:

$\text{M-OR} + \text{M-OH} \rightarrow \textbf{M-O-M} + \text{ROH}$ (2)

$\text{M-OH} + \text{M-OH} \rightarrow \textbf{M-O-M} + \text{HOH}$ (3)

Schematic representation of the reactions of one alkoxide group.

M: metal atom, -OR: alkoxide group, -R: alkyl group

Transition metal (TM) alkoxides, i.e. Ti- or Zr- alkoxides, are extremely sensitive to the nucleophyllic attack of water due to their low electronegativity and a possibility to increase their coordination number. The products are typically oligomeric units where the type and amount of functional groups - hydroxyl, alkoxide, oxo - depend on the reaction conditions, type of the alkoxide group and amount of water used for hydrolysis /1/.

In the case of multicomponent systems, typically those for functional ceramics, the first step of the process is the synthesis of a heterometallic alkoxide or a complex based on simple alkoxides and metal salts. In the next step, this intermediate product is hydrolysed to yield a precursor powder, usually amorphous, whose morphology depends on the choice of the reactants and the reaction conditions. In the further heat-treatment steps, i.e. drying, pyrolysis and crystallisation, a crystalline powder with the stoichiometry of the target material is obtained, typically at lower temperatures than those required in the solid state synthesis /3/.

The properties of the units of a ceramic powder - crystallites, aggregates and agglomerates essentially determine the cold compaction behaviour of the powder, therefore

the pore size distribution in the green compact, sintering and the microstructure of the ceramics /4/. The use of non agglomerated, chemically pure, nano-powders with a narrow particle size distribution can lead to dense ceramics with a fine-grained microstructure and a narrow distribution of pores /5/. The fine particle size allows reaching high density at lower sintering temperatures that are typical for classically prepared ceramics. The lowering of the sintering temperature is important for the ceramics, containing components with a high vapour pressure such as PbO, as for example $Pb(Zr,Ti)O_3$ solid solution /6/.

The comparison of the processing steps of PZT ceramics by solid-state and solution synthesis is shown in Figure 1.

PZT Solid State Synthesis
Starting compounds:
PbO, ZrO_2,TiO_2
↓
mixing
↓
calcination (800-900°C) ≈ 500°C:
$PbO + TiO_2 \rightarrow PbTiO_3$> 700°C: $PbTiO_3 + PbO + ZrO_2 \rightarrow Pb(Zr,Ti)O_3$
↓
Sintering
(≈1200°C)
↓
PZT ceramics

PZT Solution Synthesis
Starting compounds:
Pb-salts, Zr-, Ti- alkoxides
↓
precursor solution
↓
hydrolysis
↓
drying
pyrolysis
heat treatment
↓
Sintering
(≈1000°C)
↓
PZT ceramics

Figure 1: Comparison of the solid-state and solution processing of $Pb(Zr,Ti)O_3$ ceramics.

The present contribution summarises an overview of the authors' work in the field of novel ceramic processing of PZT based ceramics /7-11/ with the emphasis on the correlation between the solution chemistry - the choice of the starting compounds and reaction conditions that determine the structure and reactivity of the heterometallic precursor and the physical properties of the ceramic powder - the particle size, agglomeration state and its sinterability.

EXPERIMENTAL

The manipulation of chemicals was carried out in dry nitrogen atmosphere due to great reactivity of alkoxides towards humidity. The reactions were performed by standard Schlenk technique. The flow sheet is shown in Fig. 2.

Dehydrated lead (II) acetate ($Pb(OAc)_2$, JM Alfa, ultra pur) and TM n-propoxides and n-butoxides (TM = Zr, Ti, $TM(On\text{-}Pr)_4$, $TM(On\text{-}Bu)_4$, JM Alfa, metal content determined gravimetrically) were used for the synthesis of heterometallic Pb(Zr,Ti)-precursors with Zr/Ti = 50/50. Pb-Ti and Pb-Zr precursors were also prepared. The solvent was the parent alcohol, n-propanol or n-butanol, respectively. Typically, the batch was between 25 and 75 milimoles. The reactants were dissolved upon heating, refluxed, distilled to remove the by-products. The 0.25 M solution was hydrolysed with 10 moles of deionised water/mole of Pb-acetate to yield a suspension. After drying at 60 °C and 150 °C the amorphous precursor powder was heated at 650 °C for 5h in flowing oxygen. The ceramic powders were milled for 120 min. in parent alcohol and dried at 100 °C. The green compacts were prepared by uniaxially pressing at 50 MPa and isostatically at 500 MPa. The pellets were sintered at a heating rate of 10 °C/min. with $PbZrO_3$ as packing powder.

$Pb(OAc)_2$+0.5 **$Zr(OR)_4$** +0.5 **$Ti(OR)_4$**
R: n-Pr (C_3H_7), n-Bu(C_4H_9)
Solvent: R-OH
↓
Clear yellow solution @ 60°C
Reflux
Distillation
↓
PZT-complex solution
↓
Hydrolysis: R_W = 10
Drying @ 60°C, 150°C
↓
Amorphous PZT precursor
Calcination 650°C, 5h
Milling in parent ROH, 2h, planetary mill
↓
Ceramic powder
Cold isostatic pressing @500 MPa
Annealing (750-1000°C, 1h)
↓
PZT ceramics

Figure 2: PZT precursor synthesis and processing.

The volatile reaction by-products were analysed by gas chromatography (GLC, FFAP 5% on Chromosorb W, TC, He) with methylphenylether as an internal standard.

The morphology of the powders was analysed by SEM (Leitz AMR 1600T, JEOL JXA 840A). Particle size distribution was determined by laser granulometry (Cilas Alcatel) and the specific surface by BET (Perkin Elmer 212D). Thermogravimetry was performed in air at a heating rate of 10 °C/min (Netzsch, STA 429). The density of ceramic samples was determined picnometrically. The samples for microstructural analysis were prepared by thermal etching (60 sec at the sintering temperature). The average equivalent grain diameter was calculated from the grain areas by measuring approximately 200 grains.

RESULTS AND DISCUSSION

Synthesis of the heterometallic precursors

The synthesis of the heterometallic complex occurs by a reaction between Pb- acetate and TM-alkoxides upon dissolution in the parent alcohol. This reaction can proceed either by ester elimination (Eq. 4) and/or addition (Eq. 5) /3,12-14/. (The reactions below are schematical, for one functional group per reactant.) The former reaction leads to the formation of oxo (-O-) bridges and the latter to the formation of acetate bridges between Pb and TM atoms.

$$\text{Pb-OAc} + \text{M-OR} \Rightarrow \text{Pb-O-M} + \text{ROAc} \qquad (4)$$

$$\text{Pb-OAc} + \text{M-OR} \Rightarrow \text{Pb-OAc}\rightarrow\text{M-OR} \qquad (5)$$

In reality both reactions occur, leading to a product containing oxo, alkoxo and acetate groups (Eq. 6).

$$Pb(OAc)_2 + M(OR)_4 \Rightarrow PbMO_x(OAc)_y(OR)_z \qquad (6)$$

The presence of alkylacetates in the distillates, that is in the by-products of the reaction between Pb-acetate and TM-alkoxides, was determined by GLC analysis. Distillation residue could not be analysed due to extreme sensitivity to humidity. The alkylacetate/alcohol (ROAc/ROH) ratios for propoxide and butoxide derived Pb-Zr and Pb-Ti complexes are shown in Fig. 3. For both Pb-Zr and Pb-Ti the (ROAc/ROH) ratio is noticeably higher for the butoxide-derived complexes. We therefore conclude that the ester-elimination reaction (Eq. 4) contributes more in the butoxide system than in the propoxide one, hence the butoxide-based reaction product contains fewer alkoxide and acetate groups than the propoxide based one.

The hydrolysed Pb-TM complex is schematically described as $[PbMO_{x1}(OAc)_y(OR)_{z1}(OH)_w]_n$. The alkoxide groups are partially removed by hydrolysis while the acetate ligands remain bonded to metal atoms. The presence of hydroxyl and acetate groups in both propoxide- and butoxide- derived as-dried precursors has been qualitatively confirmed by FTIR /11/. Thermal decomposition of as-dried Pb-Zr-Ti precursors was followed by thermogravimetry in order to determine the relative amounts of hydroxyl and organic groups (Figure 4).

The propoxide based precursor decomposes upon heating to 550 °C in three steps, with the total weight loss of

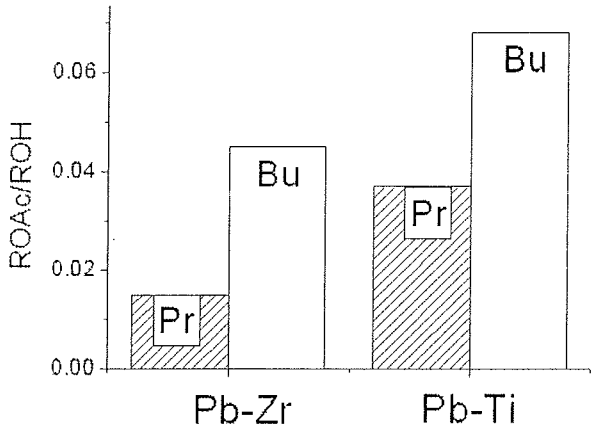

Figure 3: Alkylacetate (ROAc)-alcohol (ROH) ratio in distillates formed in the reaction between Pb-acetate and Zr- or Ti-alkoxide (R= Pr,Bu), respectively determined by GLC. Note that the azeotropic mixtures for PrOH/PrOAc and BuOH/BuOAc are similar /15/ therefore a comparison of the two systems is reasonable. (From /11/).

about 13 %, while the decomposition of butoxide- based precursor occurs in two steps upon heating to 400 °C, the total weight loss is 9 %. Additional characterization of the decomposing species by EGA (spectra not shown here, /7/) revealed that in both cases the first weight loss from room temperature up to 200 - 250 °C is due to water evolution, while at higher temperatures organic groups , i.e. acetate and alkoxide, are pyrolyzed. The relative amount of organic groups is higher in the propoxide-derived precursor than in the butoxide-derived one. This result is in agreement with the GLC results shown in Figure 3 namely that the amount of acetate groups in the propoxide-based complex is higher than the amount in the butoxide-based one.

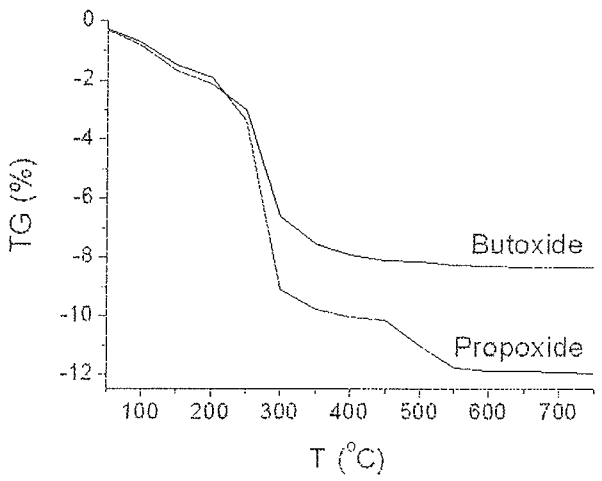

Figure 4: Thermal decompositions of propoxide and butoxide derived as-dried PZT precursors.

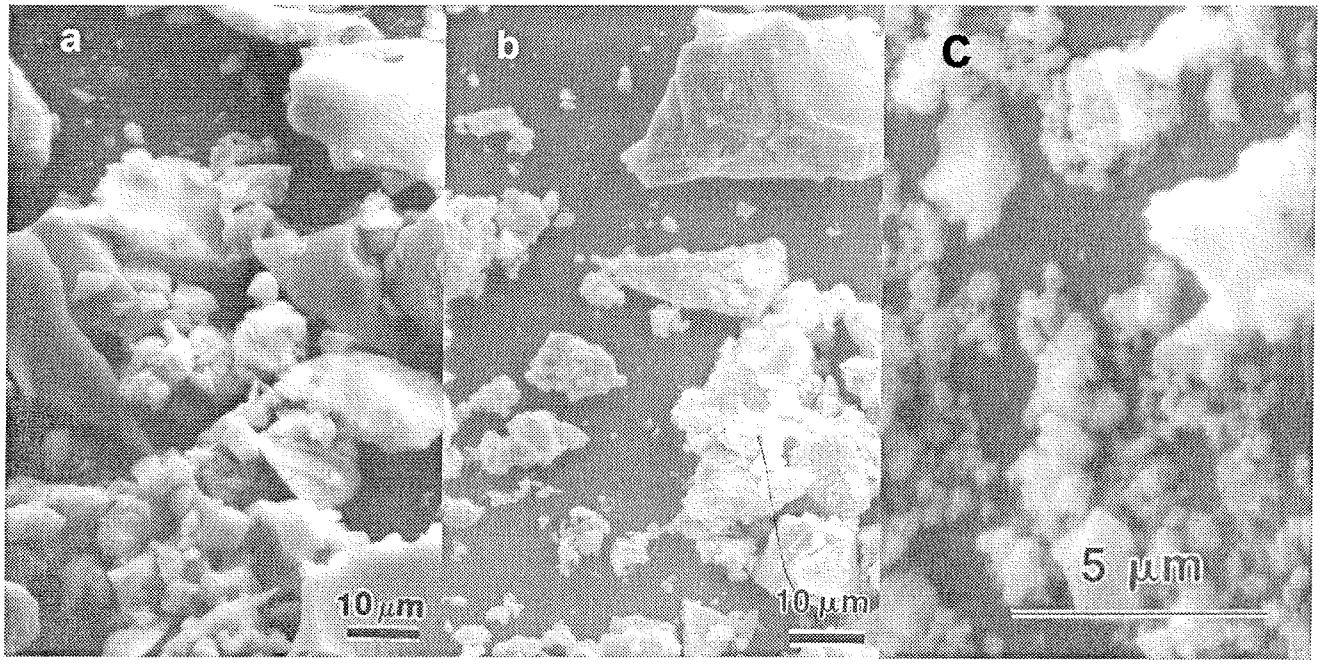

Figure 5: SEM micrographs of propoxide derived powder after drying at 150 °C (a), after heat -treatment at 650 °C, 5h (b) and additional milling (c).

Morphology of the dried and calcined PZT powders

Upon hydrolysis with an excess of water the propoxide complex forms a viscous opaque suspension, while the butoxide complex precipitates. There is a significant difference in morphology of the two powders (Figures 5, 6). The as-dried propoxide powder consists of irregularly shaped gel fragments with sizes up to 60 μm without a noticeable texture. The morphology of irregularly shaped fragments ranging from a few to 60 μm is retained also after heating at 650 °C - the temperature required to remove organic residues and obtain pure perovskite phase /7/. By additional milling we achieve a partial desintegration of the gel fragments. The median particle size is reduced to 1 μm, nevertheless the irregular morphology of the powder is retained as it is clearly shown in the micrograph.

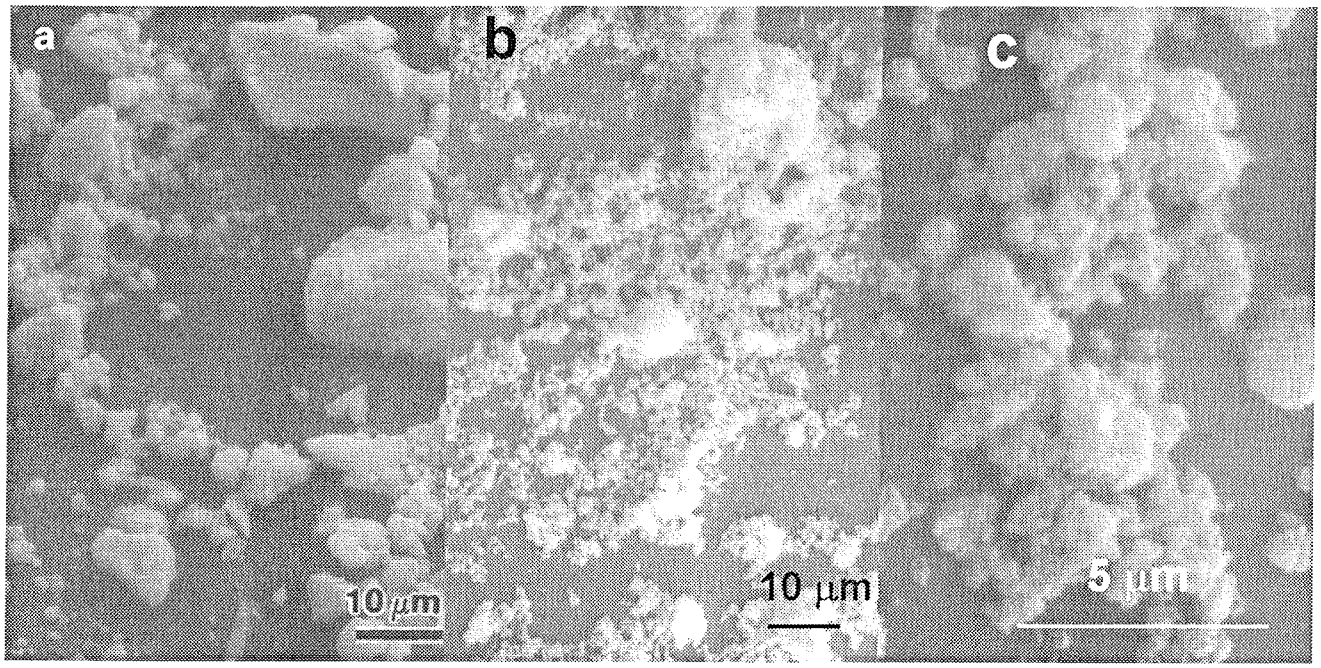

Figure 6: SEM micrographs of butoxide derived powder after drying at 150 °C (a), after heat -treatment at 650 °C, 5h (b) and additional milling (c).

In contrast the butoxide derived powder is much finer after drying than the propoxide-derived one. It is composed of agglomerated submicrometer particles ranging up to 60 μm with the median value at 10 μm, with a clearly discernible texture. The BET surface area of 192 m^2/g equals the particle size of 8 nm. (Note that the BET measurement of the propoxide powder could not be performed - the powder decomposed during the measurement.)

After heating at 650 °C for 5 h the crystallite size determined from the broadening of XRD-peaks of the perovskite phase is 30 nm and the aggregate size calculated from the BET surface area is 110 nm. The median agglomerate size determined by laser granulometry is 2 μm with agglomerates ranging up to 20 μm. Presumably the agglomerates in the as-dried powder decompose upon calcining with coincident decomposition of the functional groups resulting in a similar effect as produced by milling. After additional milling of the butoxide powder the median agglomerate size is 0.7 μm with the largest agglomerates below 2 μm as determined by granulometry.

The comparison of the particle sizes of the propoxide and butoxide derived powders after calcinations and milling reveals only slightly higher values for the propoxide derived powder. Nevertheless the morphology of the two powders is significantly different: while the former consists of irregular fragments, the latter is composed of almost spherical units. In order to obtain further information about the strength of the agglomerates the compaction behaviour of propoxide and butoxide powders was compared (results reported elsewhere /9/). The gel fragments present in the as-calcined and milled propoxide derived PZT powder behave as hard agglomerates such as present in ceramic powders washed with water /16,17/. The powder compacts exhibit a broad pore size distribution. Quite the opposite the as-calcined and milled butoxide derived PZT powder results in a compact with a narrow pore size distribution such as it is typical for compacts of soft agglomerates composed of loosely bonded particles, that can be disintegrated by a low compaction pressure /4,17-19/.

Sinterabiliy of ceramic powders

The sintering curves of the two powder compacts were recorded by a heating-stage microscope (Figure 7), the results are expressed as density calculated from the mass and dimensions of the pellets vs. temperature. The onset of the shrinkage is at approximately 900 °C for both compacts. The propoxide-derived powder compact densifies over a broad temperature range, reaching the final value of 92 % at about 1200 °C. Quite the opposite the butoxide-derived compact shrinks in a narrow temperature interval, reaching the final value of about 96 % of theoretical density below 1000 °C. Such results have been indeed expected. The butoxide-derived compact is characterized by a fine particle size and a uniform and a narrow particle and pore size distribution therefore sintering to a high relative density occurs at a lower temperature as in the case of a larger particle size /20,21/. The presence of hard agglomerates in the propoxide-derived powder hinders reaching high green density and high final density even if the particle size is small /5/.

The propoxide-derived powder compact was then sintered at 1000 °C for 2 h. The ceramic sample has got 96 % relative density and it is characterized by large lens-shaped defects in the microstructure (Figure 8). The result is in agreement with the observation that voids in the microstructure, typically a consequence of a nonuniform porosity distribution in the green compact, are the reason for reaching lower final densities /22/.

The butoxide-derived powder compacts were sintered between 850 °C and 1000 °C for 1 hour. The density and grain size data are gathered in Table 1. Density above 98 %TD is obtained at/above 900 °C. The grain size of PZT ceramics is in the micrometer range as evident from the microstructure of PZT sintered at 1000 °C for 1 h (Figure 9).

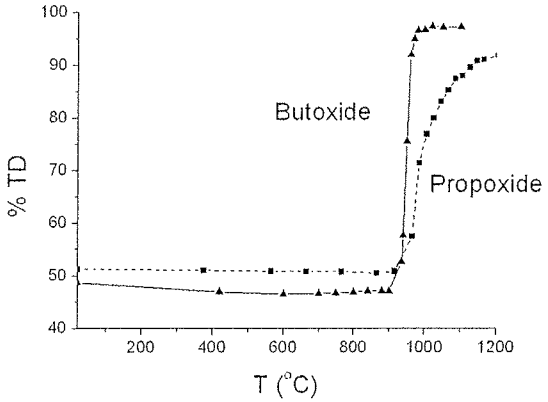

Figure 7: Dynamic sintering curves expressed as % of theoretical density TD vs. temperature of propoxide- and butoxide-derived PZT powder compacts recorded in air. Heating rate: 5 °C/min. TD_{PZT} = 8.00 g/cm^3. (From /8/.)

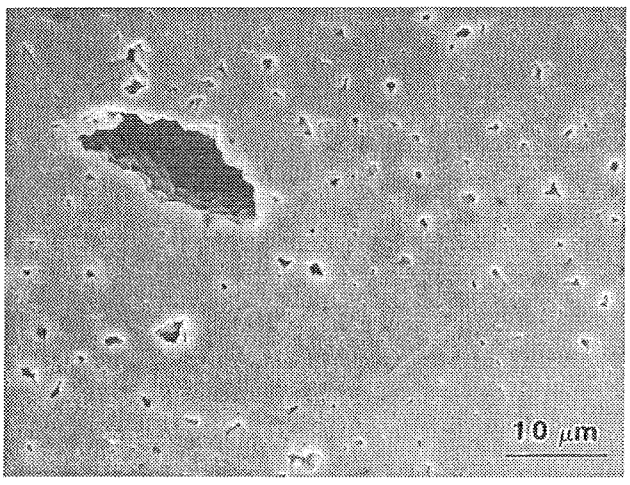

Figure 8: Microstructure of propoxide derived PZT ceramics, sintered at 1000 °C for 2 h. Relative density is 96 %. (From /9/.)

Table 1: Density (%TD) and grain size (d) of butoxide-derived PZT ceramics after heating at 850 °C and 1000 °C for 1 hour. (From /9/.)

T (°C)	% TD	d (μm)
850	89.0	0.9
900	98.6	1.0
950	99.8	1.2
1000	99.1	1.3

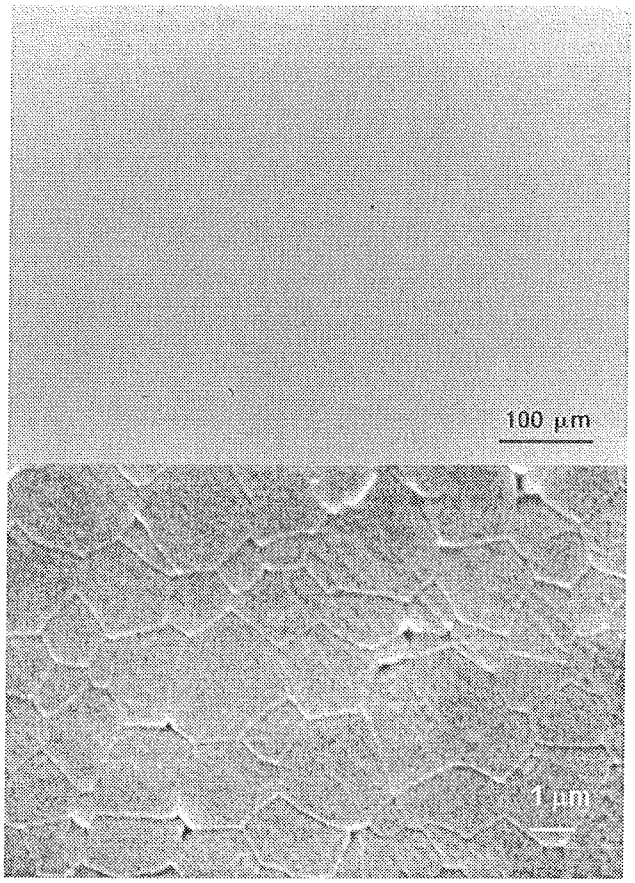

Figure 9: Microstructure of butoxide-derived PZT ceramics after heating at 1000 °C for 1 hour.

Summary

Stoichiometric PZT 50/50 ceramics were prepared by alkoxide based solution processing. The choice of the starting alkoxides influences the reactions in solution and further particle formation upon hydrolysis of the heterometallic complex.

The hydrolysis of the propoxide-derived heterometallic complex yields a viscous opaque suspension, and upon drying irregularly shaped gel fragments. This initial morphology is preserved upon further thermal treatment. As expected such powder results in ceramics characterized by large defects in the microstructure.

Butoxide-derived precursor yields a fine ceramic powder with a narrow particle size distribution. Sintering results in almost completely dense ceramics between 900 °C and 1000 °C with micrometer-sized grains.

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BUSINESS AND TECHNOLOGY CHALLENGES IN ELECTRONICS INDUSTRY IN THE EARLY 21st CENTURY

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Abstract: The end of the 20th century has been characterized by a rapid technological evolution and very promising consumption behaviour and a continuous growth seemed to be granted. In 2001 almost all electronics sectors have been severely affected by the implosion of communications market and consequently the biggest downturn in the history of electronics industry.

Despite this recent recession, the progress will certainly continue in the future and the coming years will be the years of extraordinary development of personal, data and wireless communications requiring hand-held, nomadic products and asking for more complex and intelligent integrated circuits. It will require a very strong miniaturisation, an increase of working frequency and a significant cost reduction. High performance, high volume, low cost and a very short time-to-market are the main drivers.

Poslovni in tehnološki izzivi v elektronski industriji v zgodnjem 21. stoletju

Ključne besede: tehnološka revolucija, poslovni trendi v elektronski industriji, tehnološki izzivi v elektronski industriji, tok podatkov, komunikacije

Izvleček: Konec 20.stoletja sta zaznamovala hiter tehnološki razvoj in povečanje potrošnje, kar naj bi zagotavljalo stalno rast ekonomije. Toda v letu 2001 je vsa področja elektronike prizadel razpad trga telekomunikacij, kar je imelo za posledico največji poslovni padec v zgodovini elektronske industrije.

Navkljub tej zadnji recesiji, se bo napredek v prihodnjosti nadaljeval. Sledila bodo leta izjemnega razvoja na področju osebnih, podatkovnih in brezžičnih komunikacij, ki bodo zahtevale prenosne in gibljive naprave ter posledično povzročile povpraševanje po bolj zapletenih in pametnih integriranih vezjih. Razvoj bo zahteval agresivno miniaturizacijo, povečanje delovnih frekvenc in zmanjšanje stroškov. Glavne gonilne sile tega razvoja bodo tako zmogljivi izdelki, kratki časi razvoja, nizki stroški in velike količine.

1. INTRODUCTION

The progress and changes in electronics and microelectronics industry are extraordinary. Just over 120 years ago Thomas Edison realised the first lamp and today's portable computer is making thousands of millions of operations per second and there isn't almost any human activity where electronic would not be present. The complexity of integrated circuits and their performance is doubled every 18 months following thus the famous Moore's Law. This enables to integrate a several millions of transistors in one chip, making circuits more and more complex and intelligent. There is no doubt that technical progress will continue but after the disastrous downturn in 2001 the economy changed and in the future only the most dynamic, the most flexible or the most diversified companies able to continue to develop new technologies on the economical basis and to serve different markets will survive. How it will influence the future trends?

2. BUSINESS AND TECHNOLOGY TRENDS IN ELECTRONICS

2.1. General trends

The coming years we will see the development of personal, data and wireless communications requiring hand-held, nomadic products for consumer electronics but traditional market sectors such as military, instrumentation, avionics, medical which were in the past driving forces for performances, will be still valuable and granting the business stability. High performance, high volume, low cost and a very short time-to-market will be the main drivers.

As we are just at the beginning of the 21st century we will try to find out what are the business, technology and economic challenges in face of electronics companies in the coming years.

Technology - The most visible and obvious change in the electronics industry has been in technology. The driving force will be the application of the mix of analog, digital and embedded software technology to ever-increasing applications. To reduce operating complexity and cost, we are seeing new products i.e. System-on-Chip (SOC) dedicated to specific functions. Many of these dedicated products will be built from reusable and/or programmable cores. System designers will select the functions they need and "turn off" those they don't. A model for success into the next millennium, the Silicon System Platform (SSP) goes beyond today's SOC and is based on software and hardware re-use. It defines a flexible way to build sophisticated systems from a small number of blocks, all of which may be different but which can be put together following common rules. Today's technology is limited by the number of functions we can put on a chip and the speed we can make electrons move. Researchers are looking at optical, chemical and biological structures, but none of these are far enough along to be a practical replacement for electronics.

Processing & packaging - Integration and miniaturisation of electronics became a challenge. Changes in packaging have been both: internal (building and interconnecting transistors on the chip) and external (interconnecting of chips inside a multichips module and interfacing to the board). New processing and packaging technology also offer a lower cost.

Design & production processes - The design process of advanced mixed-signal IC is very complex. As a direct consequence of this, the design of digital products and equipment now requires several design groups working in parallel and much of the analysis-intensive process has been automated on computers. Before the digital revolution and Electronics Design Automation (EDA), electronic systems were designed by trial-and-error and test instrumentation was a key component in the design process. Today exist powerful EDA's tools for high level synthesis and simulation enabling the design of multimillion gates digital ICs.

On the other hand, the complexity of analog or mixed-signal parts design is still a barrier to a real synthesis technology. When considering the future of synthesis in the analog/mixed-signal world, one must consider the limitations that intellectual property libraries and the designers' behaviour impose. Other factors driving design process change were integration and miniaturisation. When prototype test was key to the design project, we planned for three or more prototypes to get it right. Now, most testing is done on computerised model in a design automation system. The ideal is a prototypeless design that works the first time and the collaborative development or concurrent engineering is taking more and more importance in design cycle.

With ever increasing IC complexity and feature size reduction the cost of design and production of highly-customized made-to-order products become incompatible to the manufactured volume per specification. A cooperative R&D is a part of a global solution for cost sharing.

Technical knowledge & intellectual property - The key questions today are no longer "What new technologies can we develop?" and "What can we use this technology for?" but "What technologies do we need to serve this market?". Customer knowledge, rather than leading-edge technical knowledge, has become the key source of new product innovation.

Semiconductor makers are starting to question the value of their production divisions. They cannot overwhelm the competition with their own in-house technology alone. Companies can get an edge by having the world's best technology in one area, and using the industry standard or acquired technology elsewhere.

Industry structure - Also the industry structure is changing from a vertical integration around industry segments to a new horizontal structure based on four major levels of integration (packaging): chip-level integration (ICs), board-level miniaturisation (SMT), productisation (PCs, peripherals, communication sets & instruments) and system integration. These four levels require distinctly different design, manufacturing and management skills and techniques.

One big change is in supply chain management. Rather than a simple, sequential structure of a chain, modern demand and supply networks require real-time, continuous interaction with parallel co-ordination among multiple business partners. While technology forecasters do not make long term projections, they estimate by 2004 as much as 40% of all electronics manufacturing outsourced.

E-commerce is a direct result of the need for companies to reduce the cost and cycle time associated with procurement programs. Electronic transmission of purchase orders, requests for quotations, order confirmations, demand forecasts and electronic payments, save companies time and money.

2.2. Industry strategy after 2001

The computer, communications and consumer electronics industries are merging and it is no longer possible to tell the difference between them until after they have been configured for specific applications. Also many of these products are being adapted for industrial or military uses. Making predictions in a rapidly evolving industry is a tricky business, but some CEOs agree that across high tech, survival over the next five years rests on management's ability to be more flexible than ever in how they seize opportunities, more creative in finding the competitive strategy hidden in their supply chain, and willing to invest more heavily in learning about their customers and what they want /1/.

The downturn in 2001 has affected everybody, but there were companies that managed quite well and not only sur-

vived the slowdown but even enlarged their market share. Looking to the strategy of these "winners" one can observe that they all maintained a diverse group of products in different market sectors and different geographical areas and they continued investing in research and development.

The long-term winners should have a flexible cost structures, a flexible portfolio approach being able to accelerate, hold, or kill the development projects as appropriate for the current market conditions, a portfolio that will be well targeted, cohesive and competitive. They will develop a true gain-sharing partnership with their suppliers and a honest relationship with staff and sell products through the optimum mix of direct and indirect sales channels.

2.3. Market segments and evolution

Communications - Communication and computing have now converged in an exceptional development. New ideas for the future communications appear. *Alcatel* on *ISS European 2002* conference in Lisbon, presented its strategy set to match the needs of what the company identified as the "Ambient Intelligence" of "Sentient Spaces". The idea is that communication devices could deploy a digital environment that is sensitive, adaptive and responsive to presence of people. By processing the context of gathered information, services could be triggered by the computing devices present within the user's environment /9/.

Until 2000 the GSM was the biggest driver of the wireless market in the world. After the unforeseen downturn in 2001, market specialists are cautious. However they predict about 1 billion units in 2004 and 1.2 B in 2006 (about 33% in Europe). The arrival of new technologies for mobile Internet such as 3G, I-mode, UMTS or GPRS should have a limited growth at that time and shouldn't affect too much the above figures.

The 2.4 GHz wireless communication protocol "Bluetooth" arrives much slower than foreseen. The "Bluetooth" standard defines a short-range radio link capable of voice or data transmission in the unlicensed ISM band at 2.4 to 2.48 GHz using a spread-spectrum, frequency-hopping, full-duplex signal. Modules are assembled today as MCM on LTCC substrates, waiting for single-chip solutions. The "Bluetooth" market is expected to grow from 70 M units in 2002 to 700 M in 2005 according to the figures announced on *Bluetooth Congress 2001* in Monaco. Also the offers are diversified and other standards for wireless communications appeared (HomeRF, 802.11x, HyperLAN).

The well-known SMS (Small Messaging Services) sending today only a text massage will be replaced in the future by MMS (Multimedia Messaging Services) able to provide text, image, audio and video.

The third-generation UMTS (Universal Mobile Telecommunications System) mobile handsets will carry voice, data and video for mobile multimedia and will be 10 times more complex than today, however its introduction been delayed by many telecom operators from 1 to 3 years! First terminals for the "3G" were presented in February 2002 on the GSM Congress in Cannes, France. Presented there, *Motorola*'s A820 mobile includes all multimedia MMS functions (voice, video, images), MP3, GPS and even video camera. Despite the development of new technologies some specialists predict that the global revenue from worldwide telecommunications including base stations, mobile phone, fix phone and networks, and local area networks will not recover the downturn in sales revenue before 2004.

Networks, Internet - *Dataquest* projects the market for data-networking equipment will grow from $ 160 billion in 99 to $ 216 billion by 2003. The GSM's infrastructure is still the biggest market (49% of cellular phones) however new systems progress rapidly. The investments in 2001/2002 for the networks of "3G" represented 35% /2/. According to *IFX Market Model* the wireless modems should grow from 200 M in 2001 to about 1 B units in 2005. These figures include WLAN, Bluetooth, analog and digital telephony.

The physical transport of the data streams has typically been done over microwave links, coaxial cables and optical fibers. But as data rates increase, copper and microwave based schemes rapidly run out of bandwidth and give way to optical fibers. Holding a lot of promise for the future, Wavelength Division Multiplexing (WDM) and its recent generations promise ten- to thousand-fold increase in data throughput.

Asymetric Digital Subscriber Line (ADSL) transmission technique, revealed in 1994, multiplies by hundred telephony lines capacity contributing to the development of Internet video transmission.

Information appliances, Multimedia, Entertainment - Networking, multimedia and portability are giving people the ability to move around with the constraints of time and location by letting them communicate anytime, anywhere and with anyone. These "nomadic" products include cellular phones, personal digital assistants (PDA), hand-held PCs and intelligent cards. Collectively called "digital consumer products" (DCP) they will become major segments of the semiconductor market in the new century. Powerful information appliances will include telephones that provide voice mail, e-mail and faxes on one screen, voice-controlled set-top boxes that capture and play videos and DVDs, enable e-commerce and bring together the power of voice and video communications, freestanding, PC-independent smart printers and Web-connected kitchen appliances.

Automotive, Telematics - The part of electronics in car is continuously growing. Engine management, security, navigation, telematics are the most important applications.

The future car will be able to give directions (navigation, parking assistance), to perform diagnostics, to tune equip-

ments automatically (seat, radio, engine, road-handling management), to keep its owner safe (airbags, emergency call system, ABS, collision and blind-spot detection, remote keyless entry) and to communicate via wireless, Internet, FM/digital radio broadcast and vehicle-to-roadside. The electronics entered to the engine and control it precisely by means of piezo-ceramic injection system. The lighting benefits from High Density Discharge xenon lamps and a rapid progress in DEL luminosity.

The number of sensors in car explodes: a high end cars can have as many as 60 sensors. In order to facilitate the management of all these systems *SAE* (*Society of Automotive Engineers*) defined three classes of communication networks. Class A for communication at low speed (<10kbit/s) for comfort applications (audio, air conditioning, doors locking), class B for medium speed (10 to 125 kbit/s) for general information transport (instrumentation, speed control) and class C for high speed communication (125 kbit/s to 1 Mbit/s) for all real-time applications (engine control, breaking, airbag triggering). Every class has its own protocol of data transfer.

The introduction of 42V power supply network will require many new power electronic components and actuators as well as new batteries system.

Telematics is an emerging market of automotive communications technology that combines GPS, cellular phone, modem and software to provide location-specific security, information, productivity (news, multimedia, Email) and in-vehicle entertainment services for drivers and passengers (movies, DVD). And, from the automobile, navigation systems will communicate with local traffic-monitoring networks to provide the best route home for avoiding rush-hour traffic.

Domotics and Personal Applications - The first products compatible with HomeRF standard arrive. They use the band of 2.4-2.5 GHz and enable a transfer speed of 2 Mbits/s and plans are afoot to raise to over 10 Mbits/s. The specification is designed to simplify communications between PCs, peripherals, cordless phones and consumer electronic products in the same house. The domotics applications will grow considerably in coming years and will become one of the largest market sectors.

Today's electronics is generally integrated into a package. The future electronics will be also embedded into personal care objects such as clothes, glasses, belts, bracelets. That's a new emerging domain called "wearable computing" or "communicative wear".

Medical - Beside the traditional applications such as pacemakers, blood pressure measurement, insulin injection or hearing aids the electronics is more and more used in other domains. To visit intestines, there are now available special highly miniaturized pills equipped with CCD camera and DEL day- or infra-red lighting, able to transmit 30 images per second video, takes samples or inject a medicament.

The brand new application is brain stimulator to help in case of Parkinson disease.

Today's chemistry allows to elaborate polymers macromolecules which change their shape under the action of an external stimulus (electrical field, light) and can act as actuators. Thus new application domains appear: bio-medical and micro-surgery (prosthesis), space (robots), micro-mechanics (clock industry, micro-robots) and nano-technologies (sensors-actuators).

Looking more ahead we can imagine that in 10 or 20 years paralysed will walk grace of electronic robotized prosthesis, blind will see thanks to video camera connected directly to the view nerve and even a memorisation process could be aided by an extended memory.

Smart-Cards - For the first 20 years of its existence, the smart-card market has been dominated by single-application cards such as phone-cards, bank cards, pay-TV cards, GSM SIM cards, health cards and many others. The key challenge faced by smart-card chip manufacturers was to provide the highest level of security appropriate to the application at the lowest possible cost.

The smart-card of the future will support multiple applications, many of which will be downloaded after the card is issued. In this way, a single card will be able to act as a public transport payment card, a phone card and so on with the ability to link these functions securely. Interoperability, complying with international standards, will be a key requirement, in addition to the perennial cost and security issue.

Contactless operation will also play a rapidly growing role in the smart-card market. RFID etiquette is an emerging market but with a huge potential. Personal, vehicles, products on shelf contactless identification is estimated to progress of 35% a year to reach $ 7.5 billion in 2006. As per today RFID can communicate via GSM mobile phone. The major obstacle today is a lack of common standards.

The brand new application, related to the security, is a card using bio-metrics principles for persons identification. They use silicon, capacitive passive, active or reflective sensors for face and fingerprint recognition basing on ultrasonics or optical principle.

2.4. Electronics technology evolution

Semiconductors - 2000 and 2001 have been two record-setting years for the electronics industry. In 2000 production and sales of electronic equipment both reached their highest historical level and set a 20-year record in growth. 2001 will have known the first recorded downturn in the 50-year history of electronics industry. According to preliminary statistics by *Gartner Dataquest* the global semiconductor market revenue declined by 33% to $ 152 billion /3/.

According to the last issue of "*International Technology Roadmap for Semiconductors*" released by *SIA* in 2001,

the minimum dimensions should be about 90 nm in 2004, 65 nm in 2007 and 45 nm in 2010. In 2014 microprocessors should use 0.02 µm lines which is considered by *SIA* as CMOS technology limit. Regarding the gate's width of MOS transistors it will achieve 25 nm in 2007 and 9 nm in 2016 which will the physical limit (not enough of molecules to form a layer). Afterwards, something else should be invented.

By the end of 2001, *Intel Corp.* announced the TeraHertz® technology based on depleted SOI substrate, high dielectric constant gate and gate width of 15 nm. This technology enables to build transistor with 2 630 GHz switching frequency ! It should be used for next generation of microprocessors from 2005 onwards. Other big companies also presented transistors with similar performances. They used new materials such as hafnium or zirconium oxide (HfO_2, ZrO_2) to replace traditional SiO_2 /5/.

Recently *IBM* announced the world's fastest semiconductor circuit, built using IBM's latest silicon germanium (SiGe) technology and operating at speeds of over 110 GHz /4/.

Forecasted by *SIA* in 1999 the density of integration should double every 2 years from 2 M transistors per cm2 in 2000 to 44 M in 2005 and 684 M in 2014 for low cost consumer ICs and for high performance ICs from 24 M transistors this year to over 2 G in 2014. In comparison with the above forecast, the last version of *Intel's Pentium 4* microprocessor built with 130 nm lines on 300 mm wafer contains 55 million of transistors and working frequency of 2.4 GHz. In August 13th, 2002, *Intel Corp.* has unveiled several technology developments that it has integrated into its new 90nm process /10/. This new 90 nm process combines higher-performance, lower-power transistors, strained silicon, high-speed copper interconnects and a new low-*k* dielectric material. All of these technologies will be integrated into a single manufacturing process next year using 300 mm wafers.

Advanced transistors: *Intel's* new 90 nm process will feature transistors measuring only 50 nm in length (gate length), which will be the smallest, highest performing CMOS transistors in production. These transistors feature gate oxides that are only five atomic layers thick (1.2 nm). A thin gate oxide increases transistor speed.

Strained silicon: Intel has integrated its own implementation of high-performance strained silicon into this process. By using strained silicon, current flows more smoothly, increasing the speed of the transistors.

Copper interconnects with new Low-k dielectric: The process also integrates a new carbon-doped oxide dielectric material that increases signal speed inside the chip and reduces chip power consumption. This dielectric is implemented in a simple, two-layer stack design, which is easy to manufacture.

The technology evolution prediction, even for near future, is difficult and not always true, as it has been already observed in the past. So it should be taken with reserve. In 2000 the *SIA* forecasted DRAMs 1 Gbit in 2005 and 16 Gbit by 2011. Today these figures seem to be too pessimistic. During the *ISSCC* conference in San Francisco, in February 2002, *Samsung* and *Toshiba* presented 1 Gbits NAND flash memory and recently *AMD* announced a memory based on MirrorBit technology enabling to stock 2 bits per gate. In February, *Intel* used its 90 nm process to make the world's highest capacity SRAM chips at 52 megabits. These fully functional chips pack 330 million transistors in an area measuring only 109 square millimeters.

As existing storage principle are not completely satisfactory, new principles of an "ideal" memory are being developed. Although the way of FRAM (Ferroelectric RAM), MRAM (Magnetic RAM) and OUM (Ovonic Unified Memory using the change from amorphe to crystal structure) is still long, they are indicated as the future replacement for existing technologies.

Another solution is to build 3D structures. The good example could be a 512 Mbits memory from *Matrix Semiconductor*, designed with 130 nm rules and 8 levels of stacked cells, takes 8 times less silicon and costs 10 times less than standard memory /6/.

To be able to design and to manufacturers these devices new materials, new lithography methods and new design tools are necessary.

What kind of materials will be used in coming years? For sure in the next 10 years the silicon will be still the basic material with Silicon-On-Insulator (SOI) however SiGe will grow also rapidly as a competitor to GaAs. Also the carbon doped SiGe (SiGe:C) has been qualified en BiCmos process at *Motorola*. According to the "10 top" semiconductor manufacturers by 2005 between 35 to 50% of wafers will be in SOI technology.

The recent progress in silicon reactivated the development of GaAs technology which should allow to reach 400 GHz transition frequency. According to *Strategy Analytics* GaAs will be the first technology used for MMICs by 2003. Especially when GaAs can be deposited on silicon. This technology, developed by *Motorola*, is not only cheaper than standard GaAs, but also enables to integrate on the same silicon chip RF and electro-optics components (laser, LED) as well as silicon IC. Other emerging material such as GaAlAs, GaInAs, GaN, SiC as well as copper in place of aluminium will unavoidably contribute to higher speed and better power dissipation.

The biggest semiconductor manufacturers are working very hard to develop new technologies which will boost electronics industry. *IBM* announced a "strained silicon" technology which improve electrons mobility by 70% and increase transistors speed by 35% without changing its geometry. Next improvement can come from research work in the domain of molecular electronic, especially in field of carbon nano-tubes. Recently *CEA* in France has demonstrated the first quantum transistors called *Quantronium*

using aluminium supraconductor and Josephson junction effect.

These always ever higher density components need much improved photolithography technique. The decrease of light length improved continuously was not enough for the future generation of semiconductors. The new Extreme UV Lithography (EUVL) with 13.4 nm wave length and also Electron Projection Lithography (EPL) technology open the doors for 32-45 nm generations.

Another problem is related to EDA tools especially when very fine line rules or mixed-signal design are necessary. It seems that semiconductor industry is going ahead faster than electronic design tools.

As gates density and working frequency increase, also power dissipation became a challenge. A power density in the next generations of microprocessor can rise up to 3 W/mm^2 in hot points. This will require not only packages with a very low thermal resistance but also a power dissipation to the environment (air or board). Very promising solution could be "heat pipelines" integrated to the metallic base of packaging or mother board. Based on the principle of evaporation and condensation, the liquid inside the pipeline (only 125 µm thick) is distributed by the capillarity effect. Thus, *Novel Concept*, an American company, achieved the thermal resistance in the range of 0.09 to 0.28 °C/W for 71 mm square, 1 mm thick, molybdenum heat-sink. *Dynex Semiconductor* has presented a new solution with a "metallic foam" heatsink.

In next 5 years the majority of designs will be done on programmable logic making thus development faster and enabling the reuse of IC-s. By the end of 2001, *QuickLogic* introduced a programmable circuit which contains a full RISC 32bits processor, FPGA, SRAM and ALU blocs, everything fully programmable by the user.

MEMS-s represent a new very fast growing market. They cover many different applications in automotive (air-bag accelerometer, tyre pressure system, ride stabilization), medical (blood pressure monitoring, Lab-on-Chip, insulin pump), environmental (gas sensor) and RF communications sector, where they can be used in tuneable lasers and filters, attenuators, variable optical equalisers, switches, relays, capacitors and inductors. Their attraction reside in their compactness, robustness and their relatively low cost. *In-Stat* projects an optical networking market for MEMS growing from $ 67 million in 2001 to $ 2.3 billion in 2005 /7/.

Because of the basic similarities between MEMS and IC fabrication, several semiconductor companies and equipment providers have moved into the MEMS arena. While the industry is optimistic about the enormous market potential of MEMS devices and applications, there are several hurdles to be overcome before the dream of large-scale commercialization is realized. Some of the teething problems in MEMS fabrication can be categorized as follows:

- Product-specific process: an important requirement for large-scale manufacturing of MEMS devices is the standardization of fabrication process technologies.
- Special raw material: MEMS devices require exotic materials such as gold, piezoelectrics, and shape memory alloys making the fabrication more expensive.
- Low volume, high cost due to the specialized nature of the devices
- Packaging: the diversity of MEMS devices makes packaging an expensive and time-consuming task in the overall MEMS product development cycle

RF&Hyper exhibition in Paris in March 2002, confirmed the fact that the miniaturisation of RF and microwave components is the major factor in this sector. The smallest full "Bluetooth" module in LTCC technology with buried passive components including pass-band filter which needs only an external antenna has been presented. Regarding multiplexing, although the first sets of multiplexer-demultiplexer OC768 at 40 Gbits/s in technology CMOS 130 nm or InP arrived, it seems that for the next 2-3 years circuits OC192 (10 Gbits/s) in technology CMOS will take the major part of this market.

And what about the power management? In 1999, more than 50% of the world's electricity was consumed by electric motors. The majority of them still use an electro-mechanical contactor to turn the motor on or off. Replacing contactors with electronic variable speed motor drives will result in annual savings of up to $ 72 billion in electricity consumption.

Power MOS transistors and IGBT are in fierce competition. They continue to decrease the R_{ON} resistance and increase switching frequency. There is an increasing demand for low profile, high density, board-mounted DC/DC converters.

Also new materials such as SiC and having much better thermal conductivity than silicon have been announced.

Also the bio-chips market interests a lot semiconductor industry. It can offer a low cost solutions for medical diagnostics, for food and for environmental applications. Two types of chips are in development. Simple ones, with biochemical (generally DNA) molecules on glass or plastic substrate and Laboratory-on-Chip (LOC) containing microsensors, micro recipients for tested products, actuators and controlling microprocessor.

Optoelectronic components & displays – The integration of different optical functions on unique platform or better on one chip is the "leitmotiv" of all manufacturers in order to reduce the size and cost of optical components. Technologies of semiconductors III-V, GaAs, InP are currently used. However, 2D MEMS and new principles in switching such as LCD are being developed.

For the last ten years a big development effort has been accomplished in LED field. White and blue LED are the

reality and performances of LED surpass now those of halogen lamps. They achieve 40 lm/W level. However, the cost per lumen is still relatively high and especially for white LED. The technology is changing as well. Instead of saphire or SiC as a base substrate, silicon with a thin GaN layer can be used.

Very promising is the use of laser beam for mass storage of data. There are a few major solutions. One of them consists to use a blue laser 405 nm and the density of a standard DVD can be as high as 27 Gbytes. The use of the principle of fluorescence - Fluorescent Multilayer Disc (FMD) allows to stack about 100 layers and to reach to volume of 100 Gbytes per 12 cm disk. Going further in this direction, *Storex Technologies* uses a bloc of FPV (Fluorescent Photosensitive Vitroceramic) with a possibility to distinguish about 1000 levels and to stock 10 Tbytes of data !

The another way is a holographic storage. Many companies (*IBM, NEC, MIT, Bell Labs*) are working hard on this subject. A potential capacity is very high - many Tbytes and transfer speed is about 1000 times higher than presently existing due to the lack of inertia of laser beam. The first, commercially available in 2003 holographic 12-cm disk should have a capacity of 100 Gbytes and a transfer rate of 20 Mbytes/s.

A very rapid evolution is observed also in displays domain. The 3rd generation mobile phones will be equipped with colour displays. Many new technologies are emerging such as plastic LCDs or organic electroluminescent displays (OLED). The major problem is the lifetime, shorter than for other types of displays but the advantage of OLED is that the architecture is simple, there is no need neither for backlighting, nor for diffuser, nor for polarizer nor for filters. It means OLED should be cheaper.

Conversion of solar energy is an other item. The recent development confirms that solar cells can be built using a polymer optimised with nano-composites (CdS nano-tubes) in very efficient and low cost way as plastics are. That has been demonstrated by a Californian start-up *Nanosys*.

MCM, hybrids, "3D" modules - *BPA* makes distinction between performance and simple MCMs. The "simple" MCMs are meant more for the consumer sector and "friendly" environment, whereas the "performance" MCMs belong to the automotive and industrial sector.

The evolution of the first group is stimulated by an explosion of cellular market. The enlargement of the use of LTCC technology with burried components (resistors, capacitors, inductors, filters) contributes significantly to the speed-up of simple MCMs. LTTC technology is used largely for "Bluetooth" and other RF modules.

Also the use of silicon as MCM's substrate jointly with flip-chips, CDAs or CSPs enters in its maturity phase achieving high volume and low cost.

But the major breakthrough comes from integration of IC chips into so called "3D" modules, using either packaged devices (eg. memories in TSOP package) or naked dies. This System-in-Package (SIP) concept is known to combine highest functional density with minimal outline size, minimal Cost-of-Ownership and minimal Time-to-Market even in moderate volumes when compared to Chip-on-Silicon ASICs on one hand or photovia board level miniaturisation on the other.

The ever existing tendency is to pack more and more in smaller and thinner package. Therefore a "thinning" of naked dies down to 100 µm or less is now under development. The specialists project that in the next ten years the thickness of chips in 3D modules will drop to 20-25 µm enabling to integrate in a smart-card a multilevel chip. Its is obvious that traditional wire-bonding technology will be replaced some kind of micro-balls or flip-chip technique.

Passive components - Ceramic and tantalum capacitors stayed for a long time with limited CV values. Today, there is a big move in this sector. Some companies announced already ceramic capacitors X5R (-55 to +85°C) up to 1 µF in 0402 and up to 100 µF in 1210 package. Increasing capacitance and competitive prices are helping multilayer ceramic capacitors (MLCC) displace tantalum capacitors from areas they have long dominated. Both technologies now compete between 0.1 and 100 µF.

For tantalum capacitors, pulled by automotive under hood application, the change occur in CV increase and operation temperature rise. Capacitors up to 100 µF in 2220 and 10 µF 6.3V in 0603 and 0402 are now and also a 150°C and 175°C operating temperature tantalum will be shortly available. On the other hand the aluminium-polymer capacitors with high capacitance and low resistance (2 mW) attack also tantalum ones.

Chip resistors are achieving their size limit of 0201. Further miniaturisation will not improve board space saving due to the necessary solder pads area and placement accuracy. The integrated resistors network will be preferable.

Other components such as VCOs, TCXOs and even OCXOs follow this tendency and their dimensions have been reduced dramatically during the last 2 to 3 years. The physical volume of VCOs has been divided almost by 10 during last three years from 0.2 cm^3 down to 0.025 cm^3. Some of TCXOs come today in 0805 equivalent size and a crystal oscillator of 0.5 mm thick for contactless smart-cards was presented.

Although passive components changed dramatically their size during last ten years, their miniaturization tends to reach its limits. This not even related to size's limitation itself but due to problems with placement's precision, attachment's difficulties and due to the economical reasons. Further miniaturization (except very specific applications) cannot justify the cost of procurement, storage and placement of single chips.

This ever smaller components with ever smaller pitch size require denser mother boards and especially much more

precise pick-and-place equipment. Today's equipments guarantee 3 sigma precision of 15 to 25 µm. The specialists say that by 2008 this precision should be improved to 6 to 10 µm in order to be able to mount any kind of components. However, to be able to assembly flip-chip with 30 µm pitch also solder should be replaced by anisotropic adhesive, which present another challenge !.

But as the ratio of passive to active components is more than 20:1 for cell phones, the major breakthrough will come from integration of passive components in a network. The high integration of passive components in one ASPIC results not only in size, volume and height reduction but also in placement cost decrease and yield improvement.

LTCC technology allows the use of dielectric with different dielectric constants, printed coil with reasonable Q factor and antennas.

In RF range, the integration of passive components in a network on silicon above the IC covered with a passive layer of low dielectric constant, could be an interesting solution.

Interconnections - The high density, high speed semiconductors require also much better interconnection and more miniaturised passive components.

Between 1997 and 2002 worldwide market for board-to-board connectors with a pitch of 1.27 mm and smaller (1, 0.8 and 0.5 mm) increased significantly. But the miniaturisation is not the sole parameter. The "high speed" aspect is important as well. The importance of connectors able to guarantee signals integrity at 200 and 500 MHz became more significant. As a traditional connector male-female is achieving its limit with 0.8 mm pitch, connectors based on BGA approach with 0.4 mm pitch arrived.

For fiber-optics a new generation of parallel connectors with a bandwidth of 2.5 to 3.3 Gbit/s per channel have been introduced.

PCB substrates - According to the specialists in this domain the substrates for mobile phone by 2004 will have up to three levels of micro-vias per side with conductor/space 50 µm, micro-vias of 23-30 µm and halogen-free materials. Already some PCB manufacturers announce today technologies with 20 µm tracks width realised in only 5 production steps. This will require heavy investment, investment compatible only with a large volume of production.

We observe a strong development of new materials. Suppliers offer today PCB substrates for almost any application (high temperature, RF, laser drilling) using also other resins than epoxy (polyimide, BT, PTFE). Also bromine-free laminated substrates are improved and qualified. For RF applications above 20 GHz PTFE resin is unavoidable, but its price varies from 6 (low cost version) to 40 times (high performances version) of FR4 substrate.

A brand new idea was to integrate in PCB also optical fibers. This idea came from *IZM Fraunhofer Institut* in Berlin. The optical path realised with a polymer are organised in layers barried in-between electrical signal layers. This OECB (Opto-Electrical Circuit Board) with VCSEL diodes used as transmitters showed during the feasibility phase a transfer rate of 2.5 GHz with insertion losses of 0.2-0.3 dB/cm.

Packaging - Traditional packages, such as SO, TSOP, QFP and PGA show limitations regarding number of pins, packaging density and cost. Emerging packaging technologies like BGA, CSP, SIP (System-in-Package) will be expanded rapidly in coming years. They are in competition with unpackaged solutions (DCA, flip-chip). Wafer-level packaging (WLP), signals special editorial merit with its technological challenges, significant commercial advantage and further integration with "front-end" wafer process.

The role of a packaging is four-folded: to connect the chip to the outside, to distribute signals, to evacuate power dissipation and to protect the chip from the environment.

The increased speed requires lower dielectric constant and lower losses in substrate. Therefore there is a tendency to move from ceramic to new organic substrates. Higher frequency contributes to higher power dissipation which not only demands better thermal conductivity of packaging but also the innovation in package building and the improvement of integrated power control. More functions and larger chips have also more I/O. This requirement jointly with chip's size reduction push to much higher density of output leads.

The package trends for memory and ASIC for a few years behind and ahead show a strong pitch size evolution: Ball Grid Array (BGA) with 1.27 mm and 1 mm, Fine Pitch Ball Grid Array (FPBGA) with 0.8 mm, Chip Scale Package (CSP) with 0.5 mm and the Flip Chip (FC) with 0.25 mm and lower. Each of the above mentioned packages is under constant miniaturisation and cost reduction.

Under development are electroless bump deposition of Ni-Au, which is a low cost approach, and the Polymer Flip-Chip process (PFC) using silver-filled conductive bumps, which are stencil-printed. PFC bump patterns have successfully produced bumps as small as 50 µm on 100 µm pitch.

When power dissipation and low thermal resistance are concerned, BGA are replaced by Land Grid Array (LGA). That's the case of power and RF devices. These types of packages are used not only for large I/Os integrated circuits but also by manufacturers of transistors, diodes, voltage regulators.

What is the best package? Unfortunately there is no winner. Every company has its own favourite package. Today's applications require different permutations of materials and processes. This is leading to a multiplicity of packages and

form factors. Any BGA, CSP, LGA packages and stacked 3D modules will be predominant in the near future.

The pitch size is constantly decreasing making assembly more and more critical. A soldering method with very fine pitch of BGA or CSP should be replaced by more tolerant anisotropic conductive adhesives. The mechanical requirements are rising too and to compensate TCE mismatch between different materials an underfill became unavoidable.

Therefore research laboratories work on the next generation of interconnects for chips. *Intel*'s Bumpless Buil-Up Layer (BBUL) technology will be used in the near future (2006-2007) for microprocessors with 20 GHz clock rate and more. This technology consists in establishing interconnects directly on the chip and eliminating the intermediate level which reduce electromagnetic parasitics, increase frequency bandwidth and improve power dissipation.

Batteries, fuel cells – Nomadic applications require lighter, thinner and lower cost batteries. Specialists estimated that the 3rd generation of cell-phones will require the energy density of 350-400 Wh/l versus 200-300 Wh/l today.

Fortunately, batteries progress in all directions. Although NiMH still presents about 50% of mobile phone, the lithium-ion (Li-ion) entered already to its maturity stage and it would be difficult to expect more than 400-500 Wh/l (160-180 Wh/kg). The lithium-ion polymer is the "star" today and its thickness is going down to 2.5-3 mm for mobile applications. The advantage of this technology is the possibility to realise almost any shape and relatively high energy density which achieved today between 170 and 300 Wh/l. Lithium-sulphure and LiMnO2 should allow to achieve the capacity of 380 Wh/l in 2001. Aluminium-air is another competitive technology which achieves 8 times higher energy density than lithium-ion.

Although batteries progress, it seems that Fuel Cells will be the future solution for nomadic equipment. The most popular are hydrogen (H_2) and methanol (MeOH) based solution. Many companies are working hard on this subject. This year a German company *Smart Fuel Cell* demonstrated the first methanol fuel cell able to generate 175 Wh from 175 ml methanol cartridge with 50 W of maximum power /8/. There are still many problems to be solved such as difficulty to control a chemical reaction, to eliminate products of reaction (CO_2, water) and to reduce volume and weight.

3. CONCLUSIONS

The coming years of the 21st century will bring a market and technology evolution which is difficult to predict on longer term. This paper indicated only some trends on relatively short term of 3 to 5 years. A few specialists say that after 2012 when the microelectronics will achieve a technology limit situated at 0.01 µm a major changes must occur to ensure the future evolution on actual level.

In the meantime, electronics industry will face a number of challenges and the industry landscape will change significantly. System-on-a-chip (SOC) are favoured for reasons of manufacturing cost, performance and Intellectual Property (IP) protection. Hardware/software co-design is in need of real-time simulation.

Challenges faced by all industry sectors such as technical performances, quality, cost and time-to-market generate many other, more subtle challenges that are faced by companies engineers and managers. They are being pressed from all directions: improve their product's performance, reduce costs, get it done faster, keep a high profitability, satisfy customers and shareholders. The today's engineers and managers need to have a technical expertise, a very good knowledge of the market, a high innovation potential, a quality approach, managerial skills and a high resistance to stresses.

This is a formidable challenge for today's electronics industry faced with systems and technologies in perpetual evolution. Information, training and support will be the key elements for companies to complete projects and keep their competitive lead. Electronics products will in the future need a global approach to track them from the design stage through to their end of life and recycling.

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FLIP CHIP, CSP AND WLP TECHNOLOGIES: A RELIABILITY PERSPECTIVE

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Abstract: Several factors have caused wire bonding to remain the predominant first level interconnect solution across a wide range of systems, from low-end consumer applications to high-end computing systems. Early on, system performance demands were such that the electrical and thermal limitations of wire bonding interconnect did not prove restrictive. Spurred on by US OEM investments in large-scale assembly houses in low cost Far Eastern countries, the wafer and assembly processing equipment industry developed rapidly for wire bonding and soon established a global presence. On the other hand, IBM had invested significant resources in capturing an early lead and maintaining an exclusive hold on the intellectual property rights to several key steps in the design and fabrication processes for flip chip (FC) silicon die and associated packaging. The process required critical control in sputter deposition of the multiple terminal metals to create the C4 bump for FC. Equally important were the design methodologies for FC and the technology of FC packaging materials. The mismatch in thermal expansion between silicon and polymer based substrate materials led to ceramic as the preferred choice of substrate material. Starting in the late sixties. The widespread use of FC technology in IBM systems naturally assured a performance edge over competitive offerings using wire-bonding right through the seventies and early eighties. However, the premier large Japanese OEM's, namely Hitachi, Fujitsu and NEC began narrowing USA C4 lead during the eighties, thanks to their own versions of comparable flip chip interconnect and multichip packaging. Nonetheless, application of FC or flip chip solder interconnect remained solely within the domain of leading mid-range and main-frame systems where I/O density, stringent reliability, electrical switching noise and thermal dissipation needs of bipolar based systems were the critical drivers. Other areas of flip chip application included automotive, and, in commodity products like high volume watches, using for example, thermocompression bonding on a polyimide carrier, driven primarily by size constraints, cost and the absence of reliability constraints. Reliability challenges for the FC technology, i.e., harsher environments, smaller geometries, higher performance, are rising constantly. Numerous developments have been implemented since the early days of FC. Underfilling or encapsulation of the FC has been perhaps the single most significant improvement. The implementation of this technology made Flip Chip on Board (FCOB), a reality. Organic packages with FC are very common in the market today. This talk paper surveys the history of FC from its early days and includes emerging technologies derived from the FC, including CSP, WLP. We will also address jet technology as way of underfilling FC and CSP packages.

Pogled na tehnologije FLIP CHIP, CSP in WLP s stališča zanesljivosti

Ključne besede: montaža, bondiranje, povezovanje, zapiranje, tehnologije zapiranja flip chip in chip scale

Izvleček: Bondiranje je še vedno prevladujoča tehnologija povezovanja na prvem nivoju v mnogih elektronskih sistemih, od cenenih širokopotrošnih do zapletenih računalniških. V preteklosti se je namreč izkazalo, da električne in termične omejitve bondiranja niso omejevale funkcionalnosti na nivoju sistema. Velike investicije ameriških firm v montažne kapacitete na Daljnem Vzhodu so povzročile hiter rast in razvoj industrije naprav za povezovanje, ki je kmalu tudi sama prerasla v globalno industrijo. Na drugi strani pa je firma IBM vložila ogromna sredstva v razvoj ključnih korakov tehnologije, ki omogoča FC (Flip Chip) tehniko montaže silicijeve tabletke na substrat. Med drugim je bilo potrebno razviti nekatere kritične korake nanosa različnih kovinskih plasti, ki so omogočale izdelavo kroglic za FC. Enako pomembne so bile metodologije načrtovanja za FC in tehnologije materialov za FC način zapiranja. Neujemanja temperaturnih koeficientov med silicijem in polimernimi materiali je privedla k uporabi keramičnih materialov za FC substrat v poznih šestdesetih. V sedemdesetih in osemdesetih letih je široka uporaba FC tehnologije znotraj firme IBM seveda omogočila ustrezno tehnološko in konkurenčno prednost pred ponudbami njenih konkurentov, ki so temeljile na tehnologijah klasičnega bondiranja. Šele koncem osemdesetih let je nekaterim vodilnim japonskim velikanom, kot so NEC, Fujitsu in Hitachi, uspelo zmanjšati ta tehnološki zaostanek, ko so razvili lastne tehnologije FC povezav in multichip ohišij. Kakorkoli, tudi nadalje je uporaba FC tehnologije bila omejena le na srednje velike in velike računalniške sisteme, kjer so gostota vhodov/izhodov (I/O), zahteve po zanesljivosti, majhen električni preklopni šum in visoke zahteve po termični stabilnosti teh v glavnem bipolarnih sistemov zahtevale tak pristop. Uporaba FC tehnologije se je prijela tudi na drugih področjih elektronike, kot so avtomobilska industrija ter proizvodnja ur, kjer so majhnost sistema in nizka cena, manj zanesljivost, bile glavne gonilne sile. Zanesljivostni izzivi za FC tehnologijo so vse večji, kot so denimo delovanje v težkih razmerah okolja, vse manjše geometrije in vse boljše karakteristike. Prvim razvojnim korakom FC tehnologije so sledile številne izboljšave. Ena od najpomembnejših izboljšav je sigurno bila upeljava tehnike zalivanja tabletke s spodnje strani. Ta korak je pravzaprav omogočil montažo FC ohišja na substrat - FCOB (Flip Chip On Board). FC tehnike zapiranja na organski osnovi so dandanes zelo prisotne na trgu. V tem prispevku podajamo zgodovinski oris razvoja FC tehnologije od njenega nastanka do opisa nekaterih novih tehnologij, ki so se razvile iz nje, kot so CSP in WLP. Opisali bomo tudi tehnologijo brizga kot možnost zalivanja FC in CSP ohišij.

Introduction

Upon the introduction of transistors into the electronic packaging, and circuit integration on portable products, minituarization of integrated circuits became a necessity. Along with this microelectronic packages came an even more important demand perhaps, namely the performance and reliability of such products. The inconsistent, and often defect from manual wire-by-wire bonding no longer could support mass production. A faster bonding process was necessary, a method where simultaneously interconnects could be manufactured. A natural solution such as the FC process was implemented on Solid Logic Technology (SLT). The idea of having the active devices facing the interconnection, i.e., the flipping of the die was very novel idea. Protection of these devices became a major subject, and the discipline of ball limiting metallurgy (BLM), commonly referred these days as the under-bump-metallurgy (UBM) emerged. Problems of electrical shortage solder running on the surface metal line conducting media. Implementation of stiff interconnections was utilized to overcome this problem, but as technology evolved, geometries became larger wearout mechanisms became an issue in the form of low cycle fatigue. FC technology needed a solution, and once more, the soft solder interconnection was used, only this time it was attached to what we refer to day as "thin film" on a thick ceramic substrate (die carrier). Co-fired metallurgy and the thick ceramic carrier made up a package FC land that prevented solder running. In the last few years the concept of die circuit redistribution has been popular in the industry. This redistribution is done either to convert wire-bonded designs that consist die and large, peripheral arrays to fully populated array, or simply to allow usage of most area of the die for high-density interconnection (HDI). Although this package type has been used extensively for several years without been considered other than a subset of FC, nowadays is denominated as Wafer Level Package (WLP). WLP may be sometimes being referred as a Chip Scale Package (CSP). All these variations are indeed, based on the FC technology concept. In fact, very often the geometry aspect ratio is kept unaltered.

Wirebonded Packages

History

Wirebonding is the most common die connection technology today in the microelectronic industry and the most common wirebonded assembly in organic packages. The die is mounted backside down with epoxies and metals onto the substrate. Wires are bonded on one at a time, in one of mainly three processes: Ultrasonic bonding (UB), thermocompression bonding (TCB) and thermosonic bonding (TSB). Wirebonding was the first technique to be applied for assembly of devices. As early as 1957, Bell Labs in New Jersey (USA) use the technique and it was referred as Thermocompression Bonding, the other types of Wirebonding were introduced soon after when lower temperatures were required by some thermally sensitive devices. These bonders were manually operated and very labor intensive. Gold silicon eutectic between the die and the die carrier was used to attach the die prior to wire bonding. Gold and aluminum wires were the only choice. Wire bonds yields have improved and so also has their reliability. Most reliability detractors for the wirebonding technology are manufacturing defect related. Refined manufacturing practices have increased the reliability performance of this technology. Die bond, whether is metal solder, epoxy, or glass can fail during thermal cycling.

Reliability Issues in Wirebonding

Perhaps, the most widely known reliability problem for wirebond involves the *Au-Al* interface. The formation of the intermetalic $Au\text{-}Al_2$ (purple plague) during the Au material bonded to Al metallization. Although, this compound may be inconsequential to the wirebond reliability, its presence may indicate the bond integrity has been otherwise degraded already. The embrittlement of these wires make them more vulnerable to induced fracture when TC and mechanical loading. Another concern is the diffusion that occurs at higher temperatures. The Al diffuses into the *Al*-rich $AuAl_2$ phase, leaving behind Kirkendahl voids that arise from the different interdiffusion kinetics. When this voided coalesce, an electrical open may occur. Minimizing the time spent at high temperatures, improves the reliability of these packages significantly. Gold plating impurities, in particular thallium form low temperature melting eutectics that will weaken grain boundaries in the thermocompression ball bonding. For cases where injection molding is used to encapsulate the package, wire sweeping is a mayor defect producer. Significant improvements have been made with wirebond rates by the implementation of automated bonders. Improvement on the purity of materials used in the wirebonding technology to accommodate changes in the die passivation and termination, bump metallurgy is extending and widening the use of it. The use of aluminum ball bonding to improve bonding rates and the use of copper wires to bond to copper thin and thick films is gaining acceptance in today's packages. Wirebonding sweeping occurring from fluid and gas flow as in the case of injection molding or convection cooling has been identified as a major problem. Thin wires are especially susceptible to such manufacturing processes and to regular machine operation.

Flip Chip Interconnection

History

Early in the 1960's the solder bump interconnection technology was sighted as a replacement to the traditional wirebonding /1/. A solution for the expensive, unreliable and low productivity WB process was needed. The VLSI era demanded more functionality and reliability of the ever-increasing I/O count. Rent's rule forecasting of an order of

magnitude increase in number of integrated circuits per decade, stressed the need of alternatives to the rather low density capabilities of one and two row wirebonding technology. The introduction of FC technology, which requires a bump formation prior to attachment, seems as a deterrent to the acceptance of the FC interconnection at first. However, this technology will make the die become a standalone package. Protection of this new package would become a challenge, and under bump metallurgy (UBM) discipline became "a science." The common peripheral design of wirebonded die of the early sixties was, in a sense, an "under design" for the FC. Area arrays of different footprints could now be accommodated with the new bump technology. The active devices in the die will now face the connections, i.e., the die needed to be flipped. Surface tension of the soft solder dictates the amount of gap collapse between the die and the die carrier along with the geometries of the lands, i.e., UBM and the die carrier wet able area. The nomination of C4, Controlled Collapse Chip Connection seems a natural description of these bumps. The technology first used in the Solid Logic Technology (SLT) to replace the slow, unreliable and low manual productivity wirebonding technique. The glass passivation that came along with the C4 introduction made a sealed package. Package hermeticity required for wirebonding could perhaps be avoided for many applications by the new sealed technology. The electrical shorting between unpassivated die edges and solder problem was alleviated by the use of a non-collapsible stiff copper ball instead of soft solder that went though reflow. Reliability problems from low cycling fatigue forced the use of soft solder as the die geometry got larger and harsher environments needed to be survived. A thick glass dam that limited the flow of the solder during reflow to the edges of the die physically retained the solder was added. Densities of about eighteen thousand 25 μm bumps on 50μm pitch have been reported. PbSn has been the most popular choice for the C4 metallurgy. Indium alloys have also been used, although with limited applications. Copper, palladium and Nickel are common choices for the UBM. Cr and Ti usually surround terminal metals in the die and Au is used for protection on most of these metals. We must be aware that the C4 bumps serve not only electrical connections, but also as mechanical support for the die. Hence, there have to be enough bums to support the bulky die. Dummy bumps are often used for this purpose. A great advantage of the reflowable bump technology is its self-alignment capabilities from the high surface tension of the materials involved. A 50% misalignment between the pads can easily be accommodated by the FC bumps.

Reliability Issues in FC

The reliability issues on FC are quite different from the previous technology namely wire bonding where yields and manufacturing defect were predominant. FC technology must survive strains imparted by mismatch in expansion of the die and the die carrier. These displacement mismatches arise from different coefficient of expansion (CTE), temperature excursions and temperature gradients the package experience during regular operation.

$$\delta_{cb} = r^* |\alpha_b \Delta T_b - \alpha_c \Delta T_c|$$

Such displacement mismatch increases with the size of the package. In general, bumps further away from the centroid of the package, point where there is no relative displacement between the joined components, also called neutral point, will however, for some cases during actual power on/off cycling, where high temperature gradients may be present, buckling can cause interior bumps to experience highest strains and consequently shorter cycle fatigue life have higher strain and hence shorter life. /2/

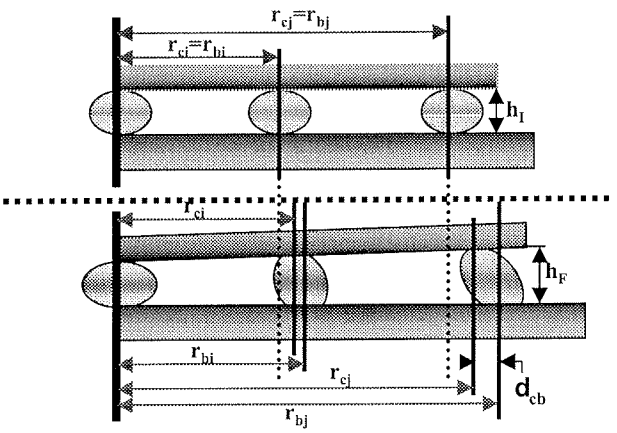

Figure 1. Displacement mismatch between die and die carrier.

The bump geometry for non-encapsulated packages plays a very important role in distributing the applied strains throughout the material. The height of the bump plays a key role in fatigue life, a quadratic relation exist between bump height and fatigue endurance.

$$\text{Life} \prec \gamma^{-2} (f \cdot e^{\Delta H/kT})^{\frac{1}{3}}$$

Recall the average strain of a bump is inversely proportional to its height, and the work done by the interconnection can be derived to be a quadratic function of the strain.

$$U = \int du = \tfrac{1}{2} \int_{\Omega} d\phi \cdot \{\varepsilon\}[K]\{\varepsilon\}^T$$

The material physical properties along with the geometry put some restrains on the current carrying capability of the FC bump. Problems from fusing at very high current levels, and failures due to electromigration mechanisms during machine operation at lower DC currents are potential reliability detractors. Some alloys are more susceptible to the environment, including corrosion, moisture abortion, and dendrite growth. Hermiticity or some environmental protection may be needed. Lead free alloys, for instance, are particularly prom to dendrite growth in the presence of electrical potentials and moisture; some Indium alloys tend

to corrode easily under some environmental conditions. Although, the fatigue life of indium alloys is generally somewhat better than PbSn alloys, the hermeticity requirements for the former has made it less attractive. The radioactivity of Pb based alloys has received special attention due to the generation of soft errors from the alpha-particle emission. The traces of uranium and thorium and daughter element, i.e., polonium may found in this material are the root cause of this intermittent problems. Energy of up to about 8.9 MeV can be imparted by these emitted alpha particles. The intermitant nature of this mechanism can have serious consequences in data storage and active devices.

MATERIAL	Activity(α/cm^2-hr)
C4 Solder (PbSn, 97/3)	0.05 - 10.0
Alumina (Al_2O_3)	0.1
Die Underfill Material	0.002 - 0.02
Plastics	0.04
Silicon Wafer	< 0.004

Table 1. Alpha particle emission rates for some materials used in electronic packaging.

The major wearout mechanisms that affect the FC interconnections are: cyclic creep, corrosion, electromigration and metal migration. The effects of these mechanisms on the package integrity and reliability depend upon several factors: solder type, defect densities, stresses and environment. The introduction of die underfill to improve the reliability of the C4 bump, as well as of a that of a large family of interconnections derived from the C4 concept including, CSP, BGA, CBGA, open a complete new application field to the packaging industry /3/. Various processes have been used to accomplished FC encapsulation including jetting of abrasive underfill materials as well as the less popular forced-flow underfill for some small die and low I/O count.

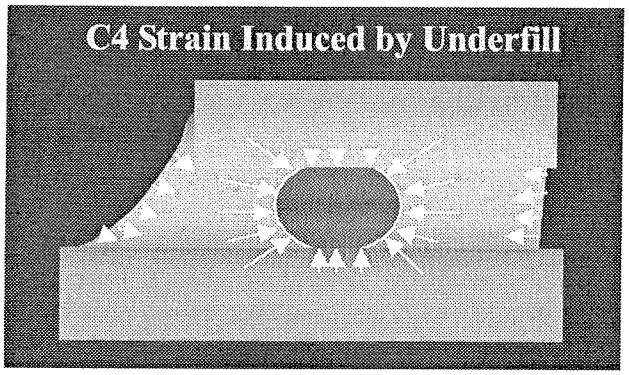

Figure 2. Hydrostatic state of stress resulting from underfilling shrinkage during curing.

Encapsulation makes possible direct chip attach (DCA) to organic carriers with high CTE mismatch to the die, larger geometries, harsher environments and more reliable packages. Nearly one order of magnitude improvement in fatigue resistance can be accomplished with underfilling

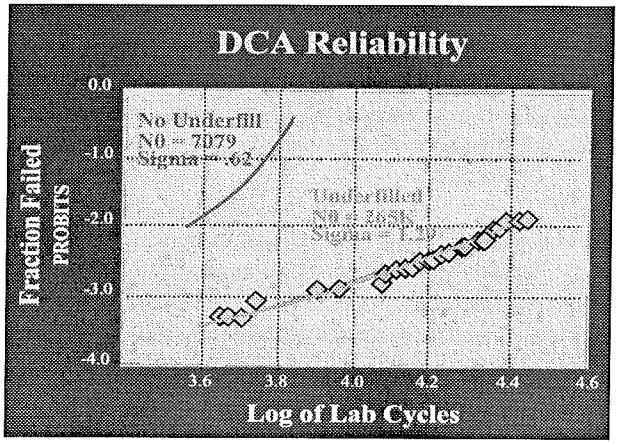

Figure 3. Low cycle fatigue data for no underfilled and underfilled die. (Data from IBM Microelectronics).

Mechanical robustness provided by encapsulants on SMD makes package reliable on many consumer products i.e., cellular phones, laptops, etc. Automotive and avionic applications where high mechanical loads are applied, i.e., vibration and mechanical impact may require underfilling to protect the interconnections from premature fracture/5/.

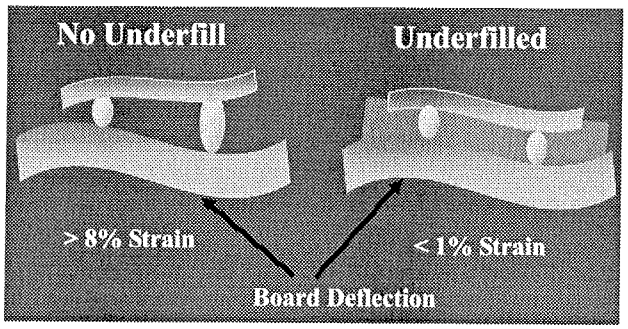

Figure 4. Package deflection from mechanical loading, impact shock resulting from a drop test.

Redistribution layers for the silicon die are becoming a very popular way to utilize peripheral designs and convert them into area arrays footprints, although, this concept have been used for several years as a die design for array packages, today this redistribution techniques is better known as wafer level package (WLP). Cross talk and other electrical detractors need to be addressed when an old peripheral design is converted into fully arrays. Interconnections used in WLP can be larger than those used in C4's. Board densities and low I/O count do not required small bumps. This choice of bump may become closer to the C4 dimensions as high-density boards (HDB) become more popular and package minituralization is required.

Jetting Abrasive Underfill Materials

It was for some time a challenge to be able to jet abrasive materials consistently for extended periods of time due to

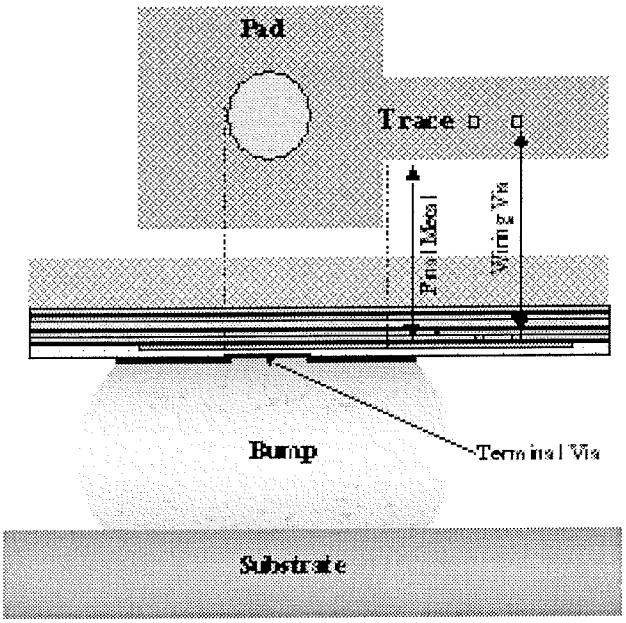

Figure 5. Wafer Level Package showing a two-layer redistribution.

the fact that the materials in contact with the abrasive fluid develop wearout that eventually affect the outcome of the jetted material. Although, this is indeed a fact with the present materials used, the relevant issue is that of the time -to-affect the jetted material characteristics including geometry, volume and mass. Hence, one needs to understand the evolution of such wearout mechanism as function of actual operation and then determine its field mean life. Figure 11 depicts needle wearout evolution resulting from jetting abrasive underfill material, Dexter 4549.

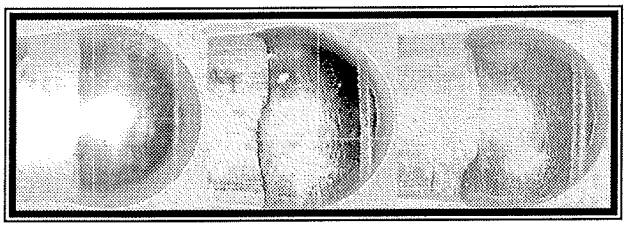

Figure 6. Needle head wearout by the jetting of abrasive underfill material

One can observe the increase on the area of that contour where the needle meets the seat of the jet by displacing the abrasive fluid present prior to impact. Similar wearout can be observed on the nozzle; there the inner diameter has increase and some changes on the geometry (radius of curvature increased) that eventually will affect the volume of material jetted. This nozzle diameter increase is perhaps the parameter that would affect the size volume and shape of the material jetted the most for a given configuration. Some increase in dot size was observed early in the life time test but after a couple of million activations this increase plateau and little to no mass increased was observed subsequently up to about nine million cycles. It was observed that if a new nozzle the size of the dots is similar to that of the dots obtained at the beginning of the test.

Conclusions

- Wire bond technology is a robust and proven to be very reliable. Manufacturing defects, yields may be the main detractor. The reliability is highly dependent on the infant mortality rate.
- FC, CSP and WLP have a common reliability detractor: bump fracture during operation.
- FC main reliability detractor is and has always been, low cycle fatigue.
- Encapsulation of the FC package improves fatigue resistance to the point that today's environments and geometries make the fatigue endurance almost a non-existing mechanism.
- CSP and some large bump WLP have longer fatigue life as expected from their larger bump geometries.
- CSP, WLP and DCA often need to be encapsulated to survive mechanical loading during manufacturing and regular field operation.
- As the package size increase, many of these packages using bump interconnections may need underfilling. Strain levels will increase and hence, fatigue life could be the main reliability detractor for non-encapsulated packages.
- A new jetting technology for underfilling packages including abrasive materials have been demonstrated.
- Small die requiring very low amounts of encapsulation material may be consistently underfilled by using jetting technology instead of the traditionally needle dispensing.

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ELECTRONIC PASSIVE COMPONENTS TRAINING ACTIVITY-DEMAND FOR PERFORMANCE ELECTRONIC PACKAGE DEVELOPMENT

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Abstract: Beside the active electronic components the passive ones are subject of continuing developments. It is difficult to imagine the dynamics of electronic products without the proper "support" of passives. In a way it is possible to say: "Today the passives are very active!". More and more requirements are coming from end users, the equipment developers. In the same time new electronic packaging technology ask for new feature of components. These features must be seen in a large approach that includes electrical, mechanical, thermal, technological and other points of view. This huge amount of knowledge must be appropriate for the packaging engineers. It is expected that in the near future the demand of such specialists will dramatically increase.

Today's exciting new products - including cell phones, laptop computers and personal data assistance - will change the way we live. These products are known for their portability, ease of use, small size and continuing increased performance. Every one of such products uses passive components in one form or another. In fact it is difficult to nominate an electronic product without electronic passive components insides. With many different capabilities and unique performance characteristics available, design engineers can use passive components to address their design challenges like: power handling, ultra high stability, current sensing, low thermal deviation, pulse handling, influence of frequency, etc. By matching the right passive component technology to the design requirements, during the development, the engineer can optimize the overall product.

The paper will be analyzing some aspects of electronic packaging education focused on the most usual electronic passive components. It will be highlighted the influence of parasitic to impedance of passive components at high frequency. One of the main problems for engineer takes into account the proper behavior of the passive components included in the electronic circuits. The impedance of passive components will be analyzed according with technology, material, structure and geometry. The computed results will be comparing with the experimental one.

Potrebne aktivnosti šolanja na področju pasivnih elektronskih komponent, ki zagotavljajo kvaliteten razvoj tehnik zapiranja

Ključne besede: tehnologije zapiranja, aktivne elektronske komponente, pasivne elektronske komponente, ohišje, izobraževanje za tehnologije zapiranja

Izvleček: Ne samo aktivne, tudi pasivne komponente so podvržene hitremu in stalnemu razvoju. Težko si predstavljamo razvoj elektronskih sistemov brez ustrezne podpore pasivnih komponent. Na nek način bi lahko rekli : » Dandanes so pasivne komponente zelo aktivne » ! Vse več zahtev prihaja od končnih uporabnikov, razvijalcev elektronske opreme. Obenem tudi nove tehnologije zapiranja zahtevajo komponente z novimi lastnostmi. Pod lastnostmi razumemo električne, mehanske, termične, tehnološke in druge. Zaradi tega morajo inženirji, ki delujejo na področju montaže komponent obvladovati vsa ta različna znanja. Pričakujemo, da bo v bližnji prihodnosti močno narasla potreba po takih strokovnjakih.

Že danes obstoječi elektronski izdelki, kot so prenosni telefoni, prenosni računalniki in dlančniki, bodo kmalu spremenili način našega življenja. Gre za izdelke, ki so prenosni, majhni in jih odlikuje enostavnost uporabe kljub stalno naraščajočemu številu funkcij. Vsak od teh izdelkov uporablja pasivne komponente, oz. težko najdemo izdelek, ki ne bi imel vgrajenih pasivnih komponent. Načrtovalci lahko danes uporabijo mnoge pasivne komponente v primerih, ko je potrebno zadostiti zahtevam po moči, izredni stabilnosti delovanja, zaznavanju toka, termični stabilnosti, obvladovanju pulznega delovanja, vplivu frekvence ipd.. Z uporabo ustreznih pasivnih komponent lahko načrtovalec že v razvojni fazi optimizira elektronski sistem.

V prispevku obravnavamo določene poglede na izobraževanje za tehnologije zapiranja in za uporabo ustreznih pasivnih elektronskih komponent. Posebej bomo poudarili vpliv parazitnih pojavov na impedanco pasivnih komponent pri visokih frekvencah delovanja. Le-to bomo analizirali glede na tehnologijo, material, strukturo in geometrijo. Izračunane rezultate bomo primerjali z eksperimentalnimi.

1. INTRODUCTION

It is important for engineers to know and understand the technology and the science of passive components and material in order to develop the best overall product designs. With many different capabilities and unique performance characteristics available, engineers can use passive components to address many of their design challengers: power handling, current sensing, ultra high stability, low thermal deviation, thermal sensing, frequency response.

In literature there are many papers about these components, but most of them analyze the technologies, materials, precision and stability, dissipated power, thermal deviation, noise, integrated structures and applications. Only a few papers present the frequency response, respectively characteristics at high frequency .Having in view the increasing of electronic circuits' frequency, this aspect become very important for the users. For this reason in the paper will be presented some aspects of this subject.

2. PARASITIC ELEMENTS AND EQUIVALENT CIRCUITS FOR RESISTORS

Any electronic component has different parasitic elements, which may modify the good function of component. For resistors, considering the parasitic effects, the results of the equivalent circuit are shown in figure1. By neglecting the skin effect and losses in the dielectric at high frequency, the resistor can be represented by the equivalent circuit diagram shown in figure 2:

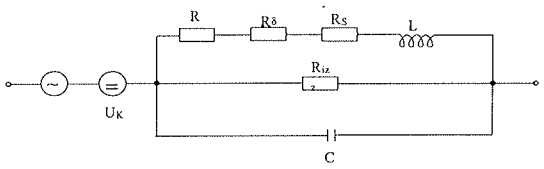

Figure 1. General equivalent circuit for resistors

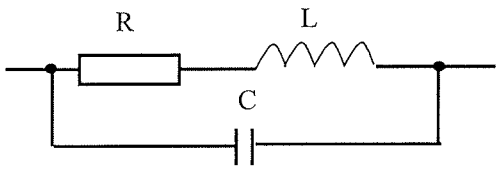

Figure 2. Equivalent circuit of resistor at high frequency

So, for high frequency, the inductance and capacitance of the resistor become important parameters and they must be smaller if the working frequency is high. The inductance is dependent on the structure of the resistor and can be approximated with the inductance of the terminals together with the inductance of the resistive element. The inductance of the terminals is function of the terminals type, dimension and the distance between them. It can be approximated with 10nH/cm for THD (Through Hole Devices) and with 0.2...0.3nH for SMD (Surface Mounted Devices). The inductance of the resistive element depends on its geometry. From this point of view, the resistive elements can be classified in: wire round- with very high inductance, spiraled film-with high inductance and plane film-with small inductance.

The resistor capacitance is dependent on the structure and the dielectric material. Predominant, resistor capacitance is determinate by the "capacitor" formed by the dielectric substrate and the contacts between the resistive element and terminals. So, the capacitance is directly proportional with the substrate dielectric constant and the area of contact between the sensitive element and terminal, and inverse proportional with the distance between contacts. For wire rounded and spiraled film resistors, the capacitance increase due to the parasitic capacitance between the spirals.

3. EXPRESSIONS FOR FREQUENCY RESPONSE OF RESISTORS

The impedance, Z, of the resistor is given by the following equation:

$$Z(\omega) = \frac{R + j\omega L}{1 - \omega^2 LC + j\omega RC} = \mathrm{Re}\{Z\} + j\,\mathrm{Im}\{Z\} \tag{1}$$

The resistive and reactive parts of the impedance will be:

$$\mathrm{Re}\{Z\} = \frac{R}{(1-\omega^2 LC)^2 + (\omega RC)^2},$$

$$\mathrm{Im}\{Z\} = \frac{\omega L(1-\omega^2 LC) - R^2 C}{(1-\omega^2 LC)^2 + (\omega RC)^2} \tag{2}$$

The admittance, Y, of the resistor is:

$$Y = \frac{1}{R + j\omega L} + j\omega C = \mathrm{Re}\{Y\} + j\,\mathrm{Im}\{Y\} \tag{3}$$

It results the conductance and susceptance,

$$\mathrm{Re}[Y] = \frac{1}{R[1+(\frac{\omega L}{R})^2]},\ \mathrm{Im}[Y] = \omega[C - \frac{1}{L\omega^2(1+(\frac{R}{\omega L})^2)}] \tag{4}$$

The resistor has the resonance frequency, f_r, only if

$$\frac{1}{R}\sqrt{\frac{L}{C}} > 1,$$

and is $f_r = \frac{1}{LC}\sqrt{1 - \frac{R^2 C}{L}}$ (7)

By using the expressions (1), (2) or (3), (4) the impedance or the admittance of the resistor can be calculated. In fig-

ure 3 is shown the characteristic Im{RY}-Re{RY}. At high frequency the impedance of resistor may be capacitive or inductive in function of R,L,C values. From figure 3 results:

For $\sqrt{\frac{L}{C}} < R$ the impedance is capacitive at high frequency; the maximum working frequency decrease with the increasing of the resistance value;

For $\sqrt{\frac{L}{C}} = R$ at high frequency the impedance is capacitive, but the resistor has the biggest maximum working frequency;

For $\sqrt{\frac{L}{C}} > R$ (for small value of R), at high frequency the impedance is inductive; the maximum working frequency decreases with the decreasing of the resistance value;

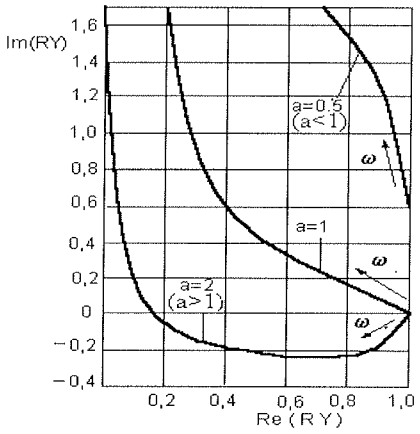

Figure 3 Characteristics Im{RY}-Re{RY} for resistors

The voltage transient response to a current step pulse of magnitude I_0 can be estimated by solving the equation:

$$\frac{d^2u}{dt^2} + \frac{R}{L}\frac{du}{dt} + \frac{1}{LC}u = \frac{RI_0}{LC}$$

The solution of the equation depends on the nature of the roots of characteristic equation. These roots have the form

$$p_{1,2} = -\alpha \pm \beta \text{ where } \alpha = \frac{R}{2L} \qquad (5)$$

So, we distinguish three cases for β real values, imaginary values or β equal to zero.

1) β is real, or equivalent $R > 2\sqrt{\frac{L}{C}}$

In this case the characteristic equation has two different real roots and the solution is:

$$u(t) = R \cdot I_0\left[1 - \frac{e^{-\alpha t}}{\beta \cdot R \cdot C}\sinh(\beta t + k)\right] \qquad (6)$$

with k a constant given by $\tanh k = \frac{\beta}{\alpha - \frac{1}{RC}}$

2) β is equals to zero or $R = 2\sqrt{\frac{L}{C}}$

In this case the characteristic equation has one double root and the solution can be written as :

$$u(t) = R \cdot I_0\left[1 - \left[1 - \left(\alpha - \frac{1}{RC}\right)\cdot t\right]e^{-\alpha t}\right] \qquad (7)$$

3) β is complex, or $R < 2\sqrt{\frac{L}{C}}$. We note $\beta = j \cdot \omega_p$

$$u(t) = R \cdot I_0\left[1 + \frac{e^{-\alpha t}}{\omega_p \cdot R \cdot C}\sin(\omega_p t + k)\right]$$

with $\tan k = \frac{\omega_p}{\alpha - \frac{1}{RC}}$ (8)

So, the pulse behavior of the resistor is somehow similar as in AC current.

Case 1 of above, $R = 2\sqrt{\frac{L}{C}}$ describes the so called damped regime. In this case the response of the resistor increase practically exponential to the final value. The rise time increases with the resistance value.

Case 2 is the critical regime and is obtained if $R = 2\sqrt{\frac{L}{C}}$, In this case the response of the resistor is similar as in case 1. The rise time in this case is lower as in case 1. In a similar way, the rise time increases with the value of C.

In case 3, for $R < 2\sqrt{\frac{L}{C}}$ the response of the resistor has oscillations. The frequency of these oscillations is ω_p which is very close to the resonance frequency of the resistor ω_0. The amplitude of the oscillations increases when R values decreases and the transition time increases with the decreasing values of resistance.

So, the behavior of resistor at current pulses depends on the parasitic elements value in a similar way as in alternative current.

4. THE INFLUENCE OF PARASITIC INTERCONNECTIONS TO THE RESISTOR

The resistor works in an electronic circuit and for this it is necessary to be connected with other components. The parasitic elements of the interconnection line modify the impedance of resistor. In this case the equivalent circuit is shown in figure 4.

In figure 4 L_1, L_2 respectively C_1, C_2 are the inductance, respectively the capacitance of the interconnection lines. The resistance of the line was neglected because it has a small value. This resistance may influence the resistance of resistor only for precision and very low resistance resistors. L_1, L_2, C_1, C_2 depend on the type and length of the interconnection lines.

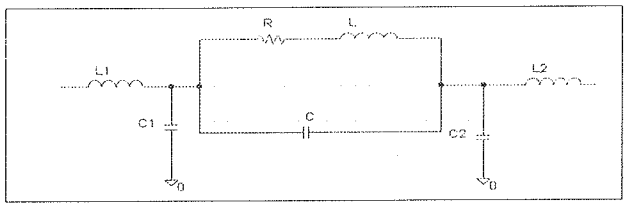

Fig.4. The equivalent circuit of resistor in interconnection environment.

At high frequency, when clock speeds in excess of 5..10MHz, or when rise times faster than 5ns exist, should be used a multilayer board and the lines should be of type microstrip and stripline.

For a microstrip line the inductance and capacitance are:

$$L_0 = 2 \ln \frac{5.98\ H}{0.8W + T} \quad \text{(nH/cm) for 0.4mm<W<1mm} \qquad (9)$$

$$L_0 = 1.64 \ln \frac{5.98\ H}{0.8W + T} \quad \text{(nH/cm) for 0.1mm<W<0.4mm} \qquad (10)$$

$$C_0 = \frac{0.264\ (\varepsilon_r + 1.41)}{\ln \frac{5.98\ H}{0.8W + T}} \ \text{(pF/cm)} \qquad (11)$$

For strip line the inductance and capacitance are:

$$L_0 = 1.998 \frac{(\ln \frac{1.98}{0.8W + T})^2}{\ln \frac{3.81\ H}{0.8W + T}} \ \text{(nH/cm)},$$

$$C_0 = 0.555 \frac{\varepsilon_r}{\ln \frac{3.81\ H}{0.8W + T}} \ (pF\ /\ cm) \qquad (12)$$

All dimensions in the expressions (9)-(12) are in cm. In table 1 are presented some values for inductance and capacitance of microstrip and strip lines with FR-4 material and T=17 μm, in function of W/H.

5. SIMULATION AND COMPUTATIONAL RESULTS FOR RESISTORS

For the impedance computation and for the transient behavior of the resistor were made PSPICE simulations and also the impedance was computed using the given relations. In figures 5 - 12 are presented the computed and simulated results of impedance resistor in different cases. The results sustain the observations presented in the second paragraph. For low values of resistance the influence of inductance is strong, see figure 7; the working frequency decreases with the increasing inductance; for higher resistance values the influence of inductance can be neglected (fig.8). The influence of capacitance is high for high resistance values (fig. 9) and low for low resistance values (fig. 10). The inductance and capacitance of interconnection lines produce series resonant frequency and can reduce considerably the maximum working frequency of resistor.

In figures 13 - 18 are presented the computed and simulated results of the transient voltage across the resistor as response to a current step transition of 1 mA.

W/H		0.1	0.2	0.3	0.4	0.5	0.8	1	1.5	2	2.5	3
Microstrip line	L0 (μH/cm)	7.2	6	5.4	4.9	4.5	3.7	3.36	3.2	2.7	2.22	1.85
Microstrip line	C0 (pF/cm)	0.34	0.4	0.46	0.5	0.55	0.66	0.73	0.92	1.12	1.34	1.62
Strip line	L0 (μH/cm)	7.7	6.3	5.52	4.94	4.5	3.56	3.11	2.3	1.73	1.28	0.42
Strip line	C0 (pF/cm)	0.57	0.7	0.8	0.9	0.98	1.25	1.42	1.93	2.58	3.46	4.48

Table. 1 Inductance and capacitance for strip and microstrip line:

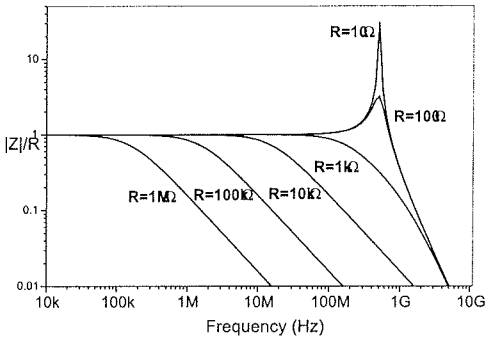

Fig. 5. Normed impedance of resistor for C=1pF, L=100nH, R=(10Ω; 100Ω; 1kΩ; 10kΩ; 100kΩ; 1MΩ)

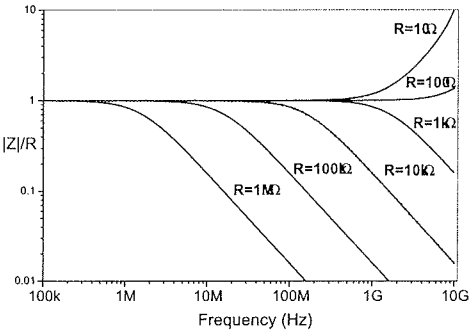

Fig. 6. Impedance of resistor for C=0.1pF, L=1nH, R=(10Ω; 100Ω; 1kΩ; 10kΩ; 100kΩ; 1MΩ)

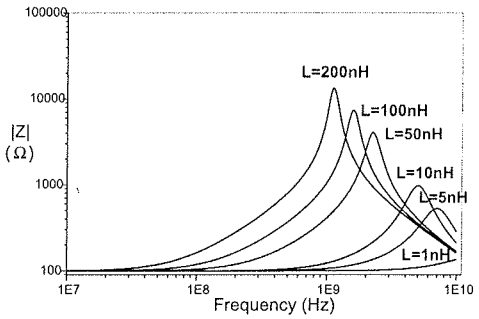

Fig. 7. Impedance of resistor for R=100Ω, C=0.1pF, L=(1; 5; 10; 50;100; 200)nH

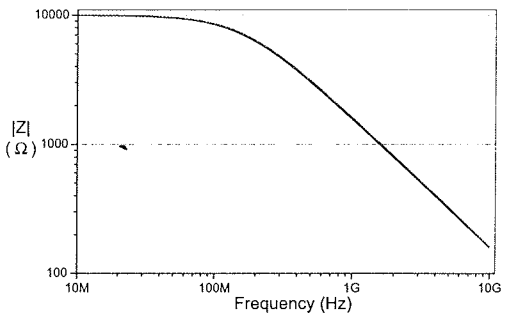

Fig. 8. Impedance of resistor for R=10kΩ, C=0.1pF, L=(1; 5; 10; 50;100; 200)nH

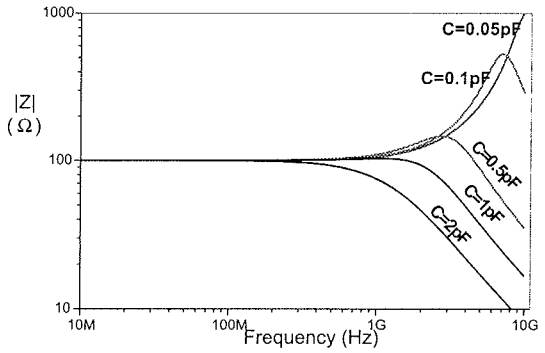

Fig. 9. Impedance of resistor for R=100Ω, L=5nH, C=(0.05; 0.1; 0.5; 1; 2) pF

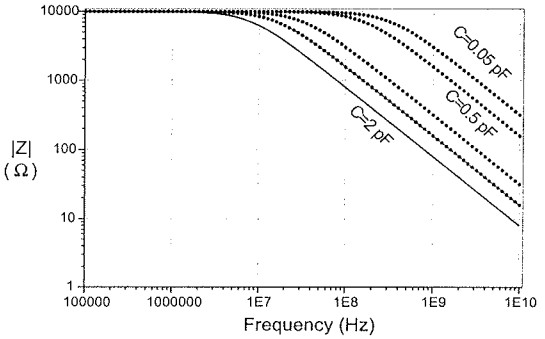

Fig. 10. Impedance of resistor for R=10kΩ, L=5nH, C=(0.05; 0.1; 0.5; 1; 2) pF

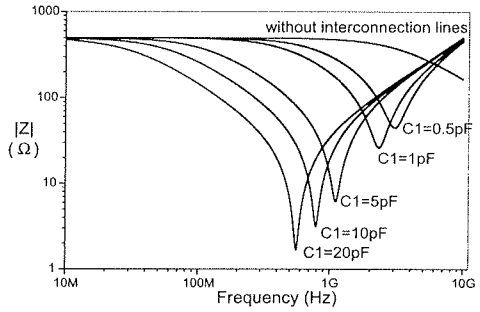

Fig. 11 Influence of the line to resistor impedance for R=500Ω, L=2nH, C=0.1pF, L_1=L_2=4nH, C_1=C_2=(0.5;1;5;10;20)pF

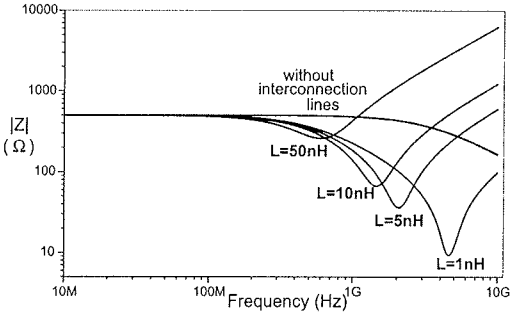

Fig. 12 Influence of the line to resistor impedance for R=500Ω, L=2nH, C=0.1pF, C_1=C_2=1pF, L_1= L_2=(1;5;10;50)nH

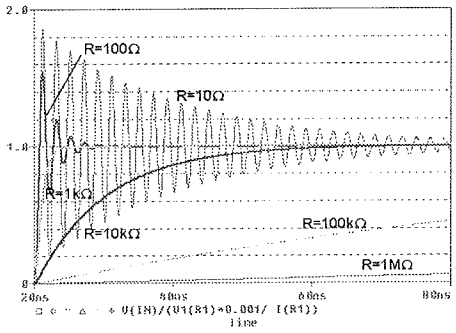

Fig. 13. Normed transient response of resistor for C=1pF, L=100nH, R=(10Ω; 100Ω; 1kΩ; 10kΩ; 100kΩ; 1MΩ)

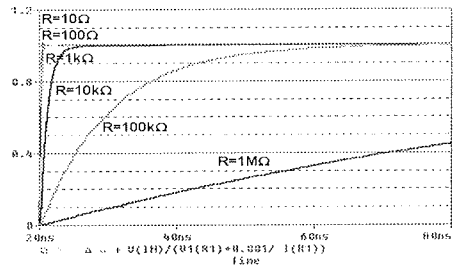

Fig. 14. Normed transient response of resistor for C=0.1pF, L=1nH, R=(10Ω; 100Ω; 1kΩ; 10kΩ; 100kΩ; 1MΩ)

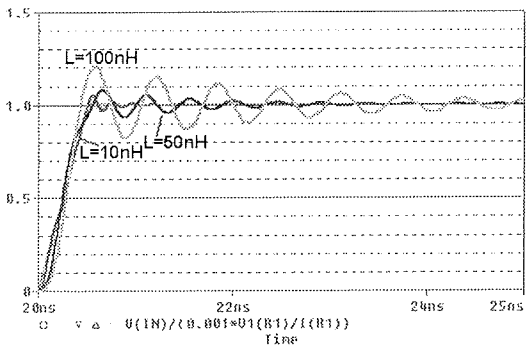

Fig. 15. Normed transient response of resistor for R=100Ω, C=0.1pF, L=(1; 5; 10; 50;100)nH

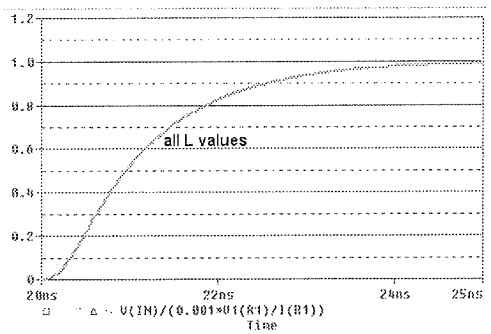

Fig. 16. Normed transient response of resistor for R=10kΩ, C=0.1pF, L=(1; 5; 10; 50;100)nH

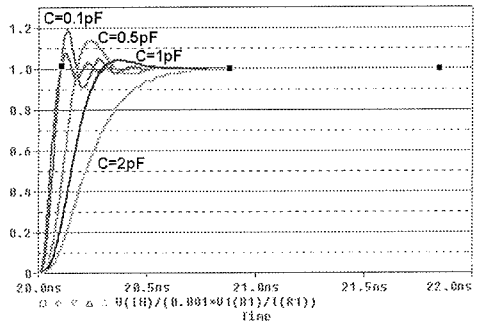

Fig. 17. Normed transient response of resistor for R=100Ω, L=5nH, C=(0.05; 0.1; 0.5; 1; 2) pF

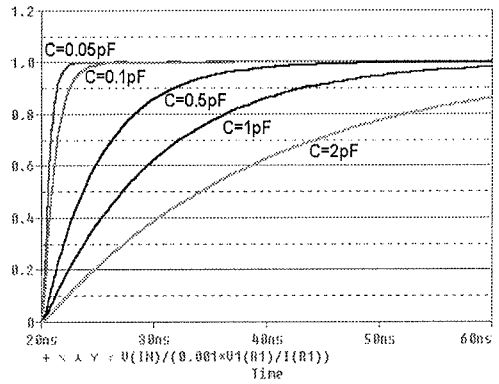

Fig. 18. Normed transient response of resistor for R=100Ω, L=5nH, C=(0.05; 0.1; 0.5; 1; 2) pF

6. PARASITIC COMPONENTS AND EQUIVALENT CIRCUITS FOR CAPACITORS

An ideal capacitor should only have a capacitive component, but in reality also has resistive and inductive components. The resistive components of capacitor are: electrodes and terminals resistance (R_e), AC dielectric loss (R_d), the DC dielectric leakage or insulation resistance (R_i). It also has an inductive component due to electrodes and terminals. Have in view this parasitic components and the structure of capacitors results the equivalent circuit shown in figure 19. At high frequency, the equivalent circuit can be simplified as in figure 20. R is called ESR and L is called ESL.

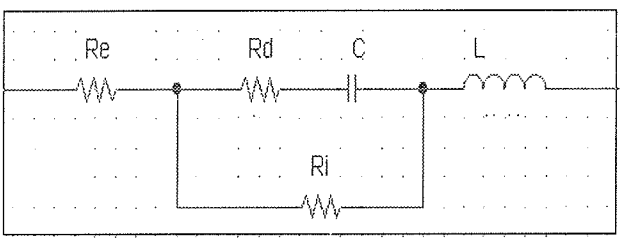

Fig. 19 Equivalent circuit of capacitor

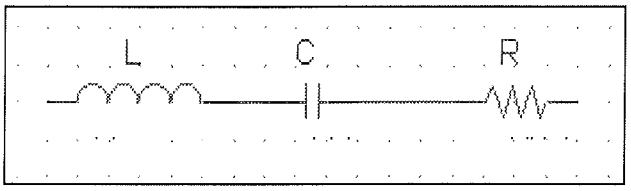

Fig. 20 Simplified equivalent circuit of capacitor at high frequency

In general, the quantities C, ESR and ESL are frequency dependent. For most applications, C and ESL can be regarded as frequency independent below 1 GHz. The inductance L is independent of the dielectric material and is dependent on the size of capacitor. The inductance of chip capacitor increase with the distance between terminations, the high and the electrodes number of capacitor. ESR is determined by energy dissipation mechanisms and is dependent of the dielectric material, electrodes and terminations. At high frequency, for chip capacitor, is very important the electrodes resistance, because this resistance increase with $f^{1/2}$ due to skin effect. The electrodes resistance increases with the distance between terminations and is dependent to the type of material and the thickness of electrodes. ESR is also dependent from frequency and capacitance,

$$R = R_e + R_d = R_e + \tan\delta/\omega C \qquad (13)$$

$\tan\delta$ is the dielectric loss factor.

The resonant frequency is important for high frequency, a decoupling capacitor, as the resonant point will give the most signal attenuation. The resonant frequency is calculated from the simple equation,

$$f_r = \frac{1}{2\pi\sqrt{LC}} \qquad (14)$$

7. CHARACTERITICS OF CERAMIC CHIP CAPACITORS AT HIGH FREQUENCY

For measurement was utilized the impedance analyzer type HP 4396B with a frequency range from 100 kHz to 1.8 GHz and the SMD fixture type HP 16192A.

Ceramic chip capacitors have several dielectric types: NP0, X7R, X5R, Y5V. The NP0 capacitors have the lowest ESR and best temperature and voltage properties, but are only available up to a few nF. X7R capacitors have reasonable voltage and temperature coefficients and are available from several nF to several μF. X5R is similar to X7R, but capacitance may be to 100 μF. Y5V capacitors have high capacitance values, but have very poor voltage and temperature characteristics. In function of dimensions, ceramic chip capacitors may be classified in standard, cube and modified. Standard capacitors have EIA dimension: 0504, 0603, 0805, 1206. 1210, et al. These capacitors have a big ESR and L. Typical ESR at resonant frequency is shown in figure 22. ESR and L have a small variation with dimension. Typical L is shown in table 1. Cube capacitors have the same length, width and height and have a medium ESR and L. Modified capacitors have terminations on the larger sides, see figure 21.

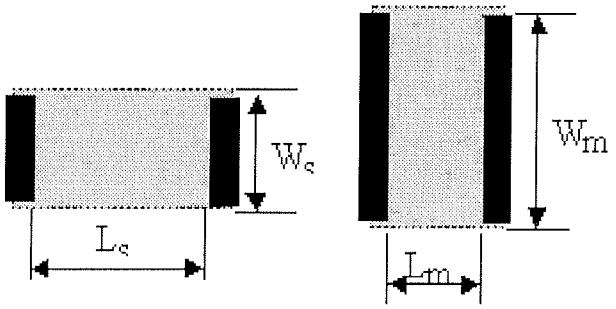

Fig. 21. Standard and modified chip capacitors

Compare standard and modified chip capacitor for the same capacitance and electrode areas, results, /8/,

$$R_m = R_s/k^2, \quad L_m = L_s/k \qquad (15)$$

Where R_m, R_s, L_m, L_s are resistance, respectively inductance of modified and respectively standard capacitor; factor k is

$$K = L_s/L_m = W_m/W_s \qquad (16)$$

So, these capacitors have a low ESR and L.

Using SPICE simulation the impedance versus frequency for different capacitors is shows in figures 22 - 27. For every type on capacitor the impedance at high frequency is depending of ESR, see figure 22 and inductance, see figure 23. A solution for to obtained a capacitor with low ESR and ESL is connection in parallel. The impedance of identical capacitors in parallel is reduced by a factor of two every time the quantity is doubled, see figure 24. The ESR of n identical capacitors in parallel - ESR_p- at the resonance frequency is

$$ESR_p = ESR/n \qquad (17)$$

From figures 25 - 27 results than for to obtain a low impedance in a big bandwidth it is necessary to connect in parallel some capacitors with different capacitance and low ESR and ESL. The capacitor parameters, which are used for SPICE simulation in figures 25 - 27, are presented in table 2. C_{MD} is capacitor with maximum capacitance, C_{mD} is capacitor with minimum capacitance, C_{iD} is capacitor with medium capacitance.

Figure	Capacitor	C (nF)	ESR (mΩ)	L (nH)
6	C_{MD}	470	20	1
	C_{mD}	0.1	100	0.8
7	C_{MD}	470	20	1
	C_{iD}	10	60	0.9
	C_{mD}	0.1	100	0.8
8	C_{MD}	470	7	0,3
	C_{iD}	10	12	0.2
	C_{mD}	0.1	15	0.2

Table. 2 The capacitor parameters, which are used for SPICE simulation in figures 25-27.

Chip type	L (mm)	W (mm)	L/W	ESL (pH)
1210	3.2	2.5	1.28	1020
1206	3.2	1.6	2	1280
0805	2	1.25	1.6	1070
0603	1.6	0.8	2	900
0612	1.6	3.2	0.5	620
0508	1.25	2	0.625	600

Table 3 Equivalent series inductance for some chip capacitors

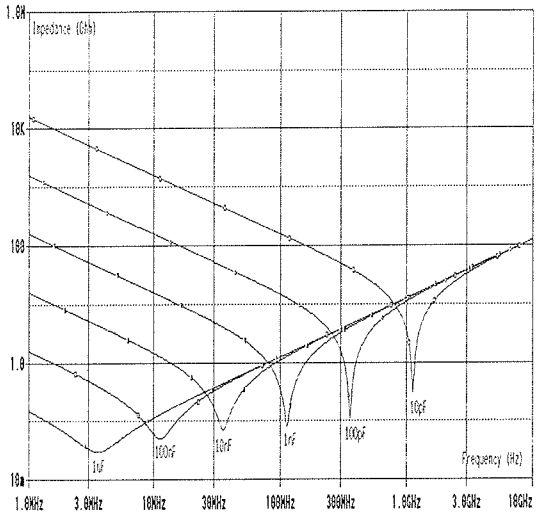

Figure 22. Impedance versus frequency for several standard X7R and NP0 capacitors.

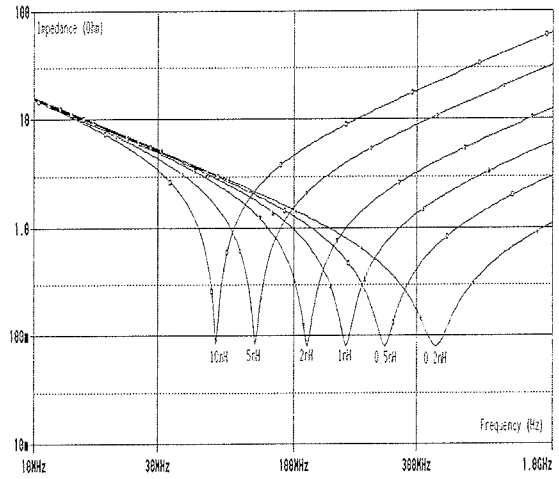

Figure 23. Impedance capacitor for different inductance values.

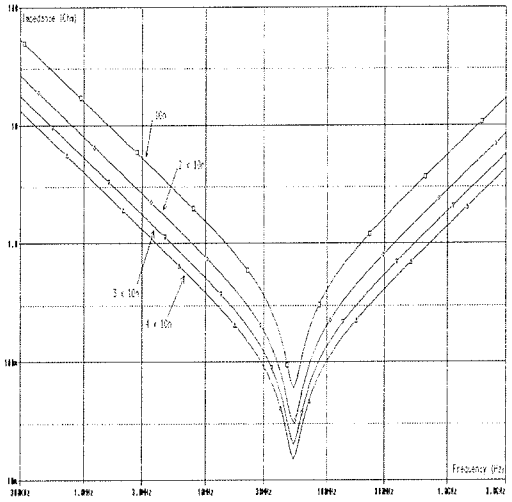

Figure 24. The impedance versus frequency for identical capacitors in parallel.

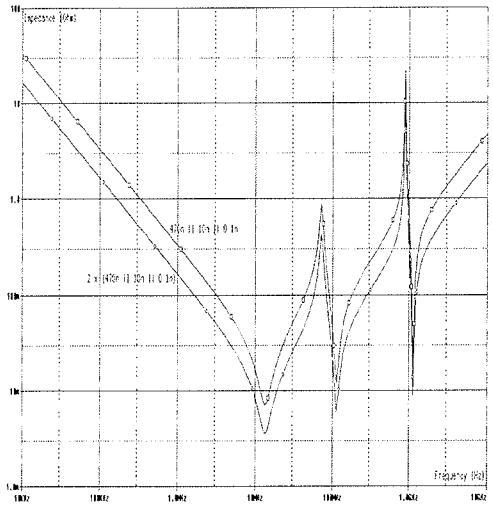

Figure 25. Impedance for three and six chip capacitors with low ESR and L in parallel.

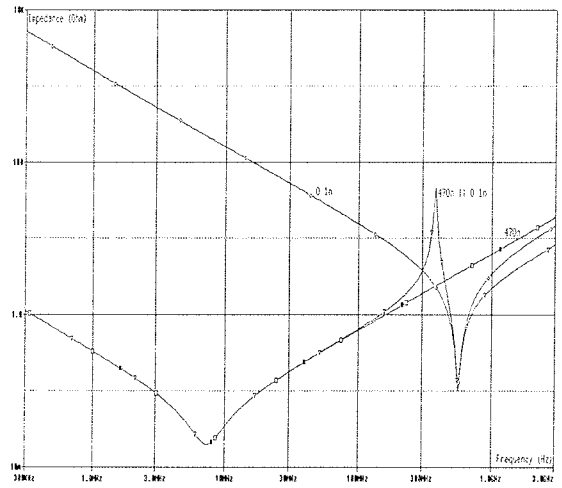

Figure 26. Impedance for two standard ceramic chip capacitors in parallel.

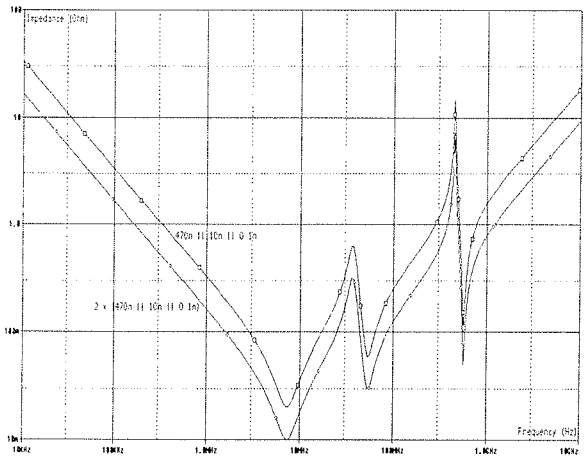

Figure 27 Impedance for three and six standard ceramic chip capacitors in parallel.

8. THE INFLUENCE OF THE RESISTOR PARASITICS ON THE BODE PLOT FOR A RC LOW-PASS FILTER

In figure 32 is shown the influence of the resistor parasitics, with the measured impedance presented in figure 29 - 31, on the Bode plot for a RC low-pass filter with a ceramic capacitor which has the measured impedane presented in figure 28.

9. CONCLUSIONS

At high frequency the impedance of resistor may be capacitive or inductive in function of R, L, C values. For big values of resistance the impedance is capacitive at high frequency and the maximum working frequency decrease with the increasing of the resistance value. For medium values, the impedance is capacitive, but the resistor has

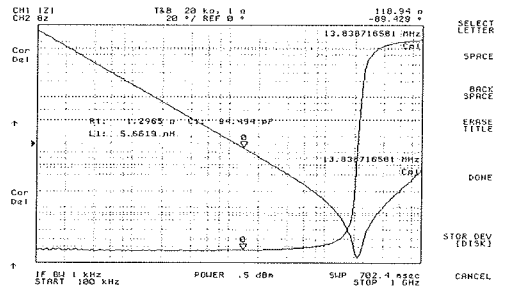

Figure 28. The impedance versus frequency for a ceramic type I capacitor (100pF)

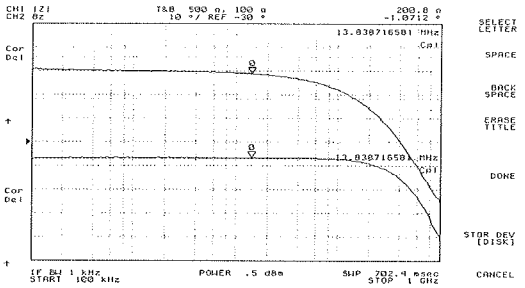

Figure 29. The impedance versus frequency for a thick film resistor- R1 (200Ω

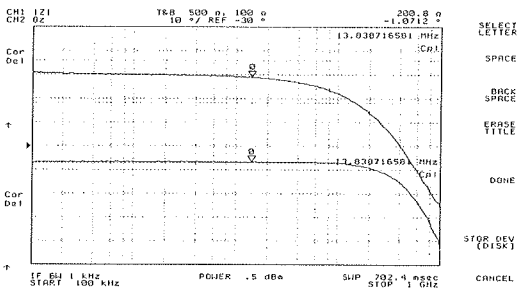

Figure 30. The impedance versus frequency for a carbon film resistor - R2 (200Ω/0.25W))

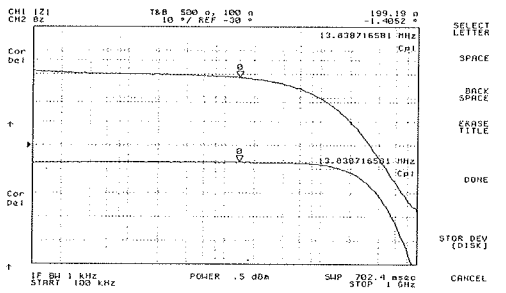

Figure 31. The impedance versus frequency for a carbon film resistor - R3 (200Ω/0.1W)

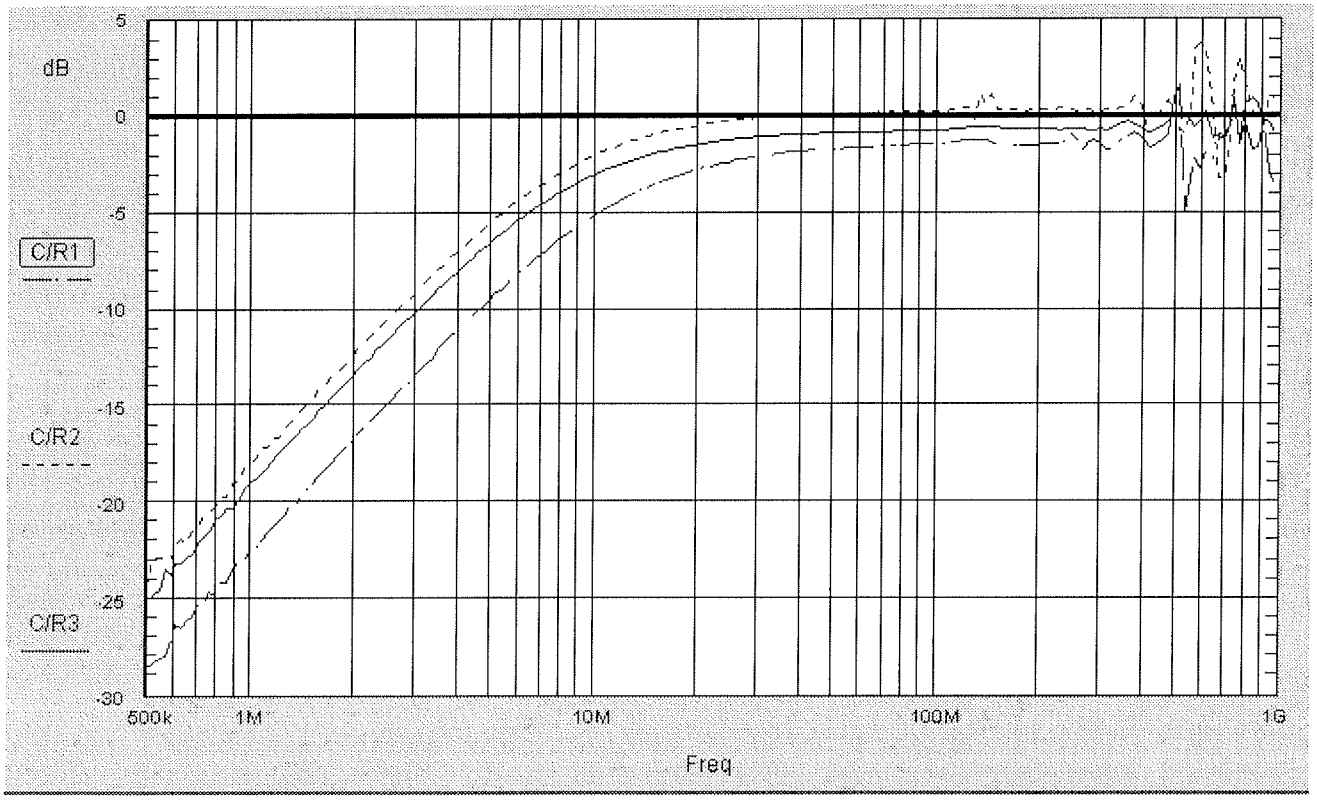

Figure 32. The influence of the resistor parasitics on the Bode plot for a RC low-pass filter

the biggest maximum working frequency. For small values, at high frequency the impedance is inductive and the maximum working frequency decreases with the decreasing of the resistance value.

The frequencies of electronic circuits have increased rapidly in the last time. For the best performance in these applications, low equivalent series resistance and equivalent series inductance, high resonant frequency, low impedance of capacitor is required. These parameters are analised in the paper for multilayer ceramic chip capacitors. A solution to realize a capacitor with low ESR and ESL is connection in parallel of some identical capaacitors. A methodology for realize a capacitor with low impedance in a broad bandwith is connection in parallel of some capacitors with different capacitance.

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LEAD FREE INTERCONNECTION TECHNOLOGY AND THE ENVIRONMENT

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Key words: interconnection technology, lead free soldering, environment protection

Abstract: Trends of growing consumption, decreasing product lifetime and new application fields in nearly all industry segments lead to an enormous increase of electronics products. The production of raw materials and products, their use as well as the end of life treatment of these products cause considerable environmental impacts. To minimise hazards to human health and the environment, an economic growth in a sense of sustainable development has to be realised and new products and process technologies should proof that they contribute to the solution of global environmental issues.

In this paper the interconnection technologies as key technologies for future products are discussed in correlation to their environmental behaviour. At the present a transition to lead free soldering takes place worldwide. In that respect various environmental aspects of the different lead free interconnection systems (solders and surface finishes) should be compared in order to find the best solution from an ecological point of view.

Tehnologije povezav brez svinca za ohranjanje okolja

Ključne besede: tehnologije povezav, spajkanje brez svinca, zaščita okolja

Izvleček: Trendi povečanja porabe, skrajševanja življenjske dobe izdelkov in nove možnosti uporabe v skoraj vseh vejah industrije, peljejo k velikemu povečanju števila elektronski izdelkov. Proizvodnja surovin in izdelkov, njihova uporaba in nazadnje njihova obravnava ob koncu življenjske dobe, imajo močan vpliv na okolje. Z namenom zmanjšati nevarnost za človekovo zdravje in za okolje, moramo zagotoviti tako ekonomsko rast, ki bo omogočala razvoj takih novih tehnologij in izdelkov, ki bodo prispevala k rešitvi nekaterih globalnih okoljevarstvenih problemov.

V tem prispevku opisujemo tehnologije povezovanja kot ključne tehnologije za bodoče izdelke v povezavi z njihovim vplivom na okolje. Dandanes na svetovnem nivoju poteka prehod na spajkanje brez svinca. V tem kontekstu analiziramo različne sisteme povezovanja brez svinca (spajke in površinske obdelave) z namenom najti najboljše rešitve s stališča varstva okolja.

1. INTRODUCTION

The last 10 years were characterised by an explosive growth of electronics and information technology and this trend continues. Microelectronics and microsystems technology make highly miniaturised products possible with high performance, quality and reliability, and they become more and more important for nearly all product applications in leading industry segments.

However, the present trends of growing consumption, decreasing product lifetime and pervasive distribution are leading to serious environmental issues in respect to electronic products, associated with raw material production, product manufacturing, use of these products and their end of life treatment.

By means of miniaturisation the environmental impact of microelectronic products could already be reduced in some respects. Their material and energy consumption is already small (in a first estimation) and their waste volume, too.

But because of the increasing production numbers the quantity of waste of electrical and electronic equipment (WEEE) with the complex mixture of materials is growing. Estimates suggest that the amount will be doubled in 12 years within the EU. The waste of electrical and electronic equipment (WEEE) grows three times faster than municipal waste. And the recycling of products, which are becoming smaller, is more and more difficult, mainly because of the use of inseparable material compounds. Furthermore, there is a tendency towards material compositions that are less suitable to an economical recycling and the small products are more difficult to collect (the users often put them into the waste bins). Moreover, up to now only around 10 % of all products are taken back and recycled. About 90% of it is landfilled, incinerated or recycled without pre-treatment.

The key technologies for future miniaturized products are the assembly and packaging technologies. At present a transition to lead-free soldering takes place. This process was initially driven by new environmental protection legislation (e.g. RoHS) /1/, however it is now more likely driven by marketing reasons. Despite these particular driving forces, new technologies nowadays must be designed in such a manner, that they not only comply with technical/ technological and economic requirements, but incorporate ecological demands for a sustainable industrial development. That means a EcoDesign or Design for Environment (DfE) has to be implemented.

2. DRIVERS FOR APPLICATION OF ECODESIGN

EcoDesign or Design for Environment (DfE) is a term for a systematic approach to environmentally conscious product development and design. The integration of environmental aspects must take place as early as possible during the planning, development and design process and the aspect "environment" must be added to other classical criteria of product development.

Fundamental to EcoDesign is life cycle thinking, the consideration and minimisation of the environmental impacts in all life phases of a product: the extraction of raw materials for the product as well as the production process, the distribution, the use of the product, its recycling and finally the disposal of product parts.

There are several drivers for companies to integrate DfE in their working flow.

- legal requirements
  For reduction of the environmental impact of electronic products the European Commission has announced three legal directives.
  - The first dealing with take back and recycling/ reuse of waste from electric and electronic equipment (WEEE) /1/.
  - The second restricts the use of certain hazardous substances such as cadmium, mercury and lead from 1.7.2006 on (RoHS) /1/.
  - The third is a directive on the design and manufacturing of electronics (EEE).
- the possibility to reduce the liability risk by avoiding pollutants (risk management)
- the demands of the customers for environmental friendly products, for instance buyers in the public sector (customer value)
- the moving towards a good public image (environmental rating)
- the possibility to save money by reducing consumption of energy and materials or wastes and pollutants (cost efficiency)
- an improvement of the market position by innovative, environmental friendly products (market diversification)
- a larger motivation and commitment of the employees since they can take an interest in the responsibility for their actions (human resources).

In several regions the companies have worked out plans and strategies for integration of DfE in their product policy and established environmental roadmaps. Figure 1 shows as an example such a roadmap of the Japanese electronics industry (JEIDA).

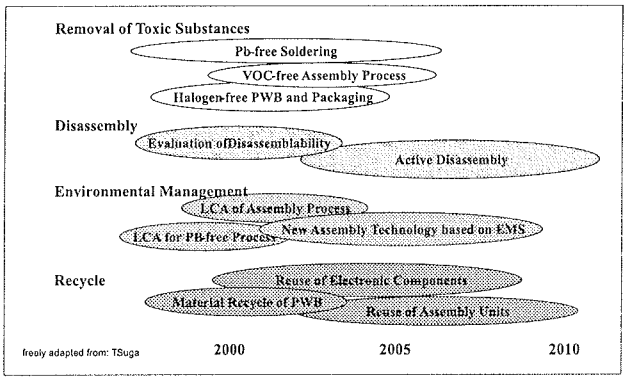

Figure 1: Environmental Roadmap of the Electronics Industry in Japan (JEIDA)

Key points are the removal of toxic substances, the recycling (including disassembly) and the implementation of environmental management systems. For special subjects there are special roadmaps, for instance for the implementation of lead free interconnection systems. The Japanese electronics industry has targeted the full implementation of lead free products not later than 2004/5.

Figure 2 shows a variety of lead free products which are already on the market.

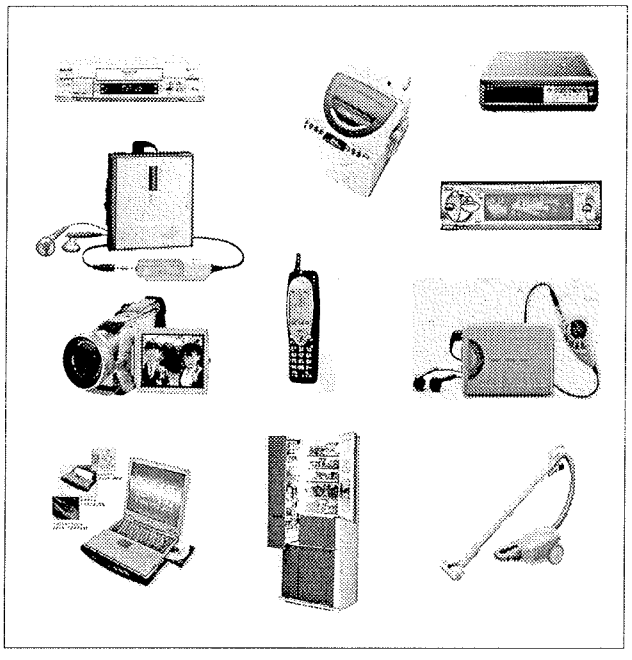

Figure 2: Lead free products

3. ENVIRONMENTAL ASSESSMENT

In order to reduce the environmental impact of their products the industry is looking for tools to assess which products or processes is the best solution from an environmental point of view.

A number of different methods exists for an assessment of the environmental impact of electronic products.

The life cycle oriented approach "from cradle to grave" of products is described in the ISO 14040 and following standards. Balances of material and energy flows as well as emissions are compiled for all processes and aggregated for the product life cycle as production, use and end of life phase including transportation and distribution. The effects are characterized in impact categories like global warming, ozone depletion, acidification, human toxicity and others. Then, the environmental impacts of the emissions and consumption of resources are evaluated and weighted.

These life cycle assessment tools usually require a lot of information about the products components and manufacturing processes. Very often however, are these data not easily accessible. Especially in the case of very complex products, like electrical and electronic products, up to now the life cycle analysis (LCA) is not suitable for a quick assessment and therefore not applicable for optimisation during the design phase.

As for an environmental assessment of lead free products in comparison with conventional products, a whole life cycle analysis is not available at the moment. Two projects were started to carry out a life cycle assessment in the field of lead free soldering, one is the international IMS-project EFSOT with the cooperation of Japanese, Korean and European participants; the another is initiated by the American EPA in the frame of the DfE-project.

However, it is necessary and very important to describe the environmental impact before a new generation of products are mass produced. Simplified assessment methods are suitable to bridge this gap and to get a feeling of how alternative materials for interconnection systems would influence the environmental behaviour of electronic products.

With toolboxes or assessment matrices the environmental properties of a product can be considered from various sites in order to get a broad impression about the environmental impact of the product. In the case of the evaluation of solders and surface finishes, terms such as resource (energy and water) consumption for raw material production and manufacturing, toxicity and leaching behaviour in the end-of-life phase according to the US-American „Toxicity Characteristic Leaching Procedure" TCLP1311 are summarized. By means of the toolbox or the assessment matrices companies can choose which data and which assessment types to concentrate on first and then slowly evolve towards the more comprehensive and time consuming process gathering and evaluating life cycle data for their products.

For an initial screening of products the so called Toxic Potential Indicator (TPI), the essential tool of the Fraunhofer IZM/EE-Toolbox, was used to make a quick environmental assessment in the following cases. This indicator is based on threshold values of the allowable workplace concentration, the water pollution classification and the R-values of the hazardous substances declaration in the EU and is used to evaluate the environmental impact of materials or products by their chemical contents /2/.

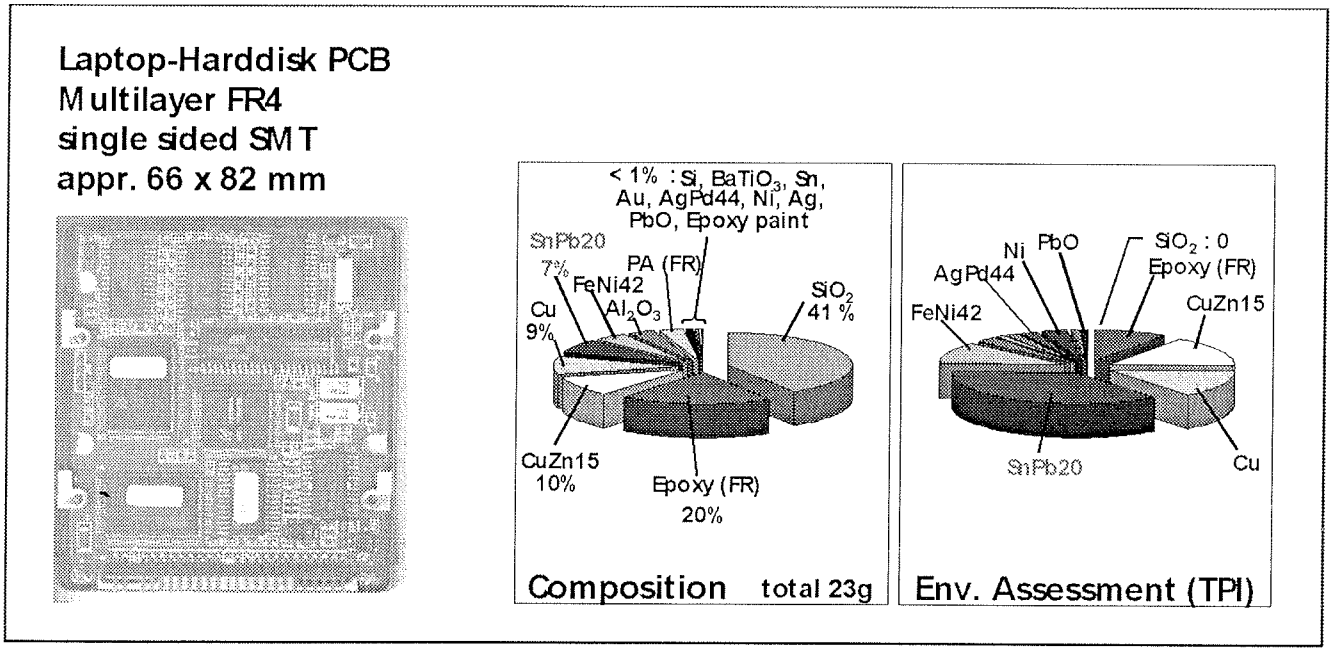

Figure 3: Composition and environmental impact of the materials of a selected PCB

4. LEAD ON PCBs

Even though lead is only used in small amounts on PCBs, due to their toxicity, it is one of the weak points in respect to the boards environmental impact. Figure 3 shows the materials for an PCB example and their parts on the environmental impact regarding the TPI of this PCB. Even though only 7 % of the PCB materials are SnPb it contributes around 25 % to the environmental impact of the this PCB.

With simultaneous consideration of the strongly increased numbers of electronic products, that was one reason for world-wide efforts in research and development to substitute lead in electronic devices.

It has been known for more than a hundred years that lead affects the human nervous system and causes a range of serious problems. Particularly children are concerned.

Most of the lead on PCBs is obtained in the interconnection system consisting of the surface finishes of the board and the component leads or terminations and of course of the solder itself.

Some components such as varistors, thermistors or multilayer capacitors obtain smaller amounts of lead and there are no alternatives at the present. Therefore, a transition to lead free electronic devices has to aim on the most heavily used parts, that will be the solders and surfaces finishes, and replace them.

Not only lead free alternatives (solder and finishes) have to be developed, but highly reliable soldering technologies for interconnects of high quality as well. However, the implementation of a new lead free interconnection technology should not lead to higher environmental burdens. To prevent this, the environmental impact of possible substitutes must be considered during the selection of the new technology.

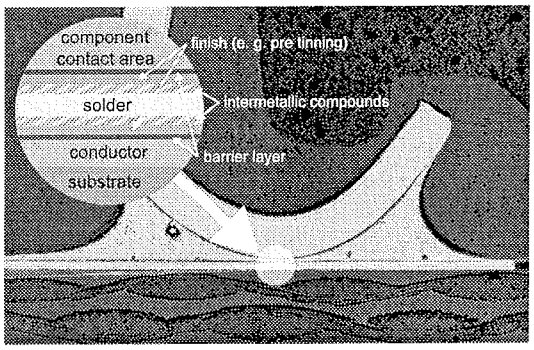

Figure 4: The interconnection system

5. INTERCONNECTION SYSTEM AND THE ENVIRONMENT

Figure 4 shows the interconnection system with the parts which have to be considered: the solder, the finish of the PCB (substrate and conductor) and the component contact area.

State of the art is the application of the eutectic SnPb for solder, Hot Air Solder Leveling (HASL) layers of eutectic SnPb on the PCB in many cases and eutectic SnPb an the components contact area.

5.1 Lead Free Solders

In various projects in Japan, USA and Europe alternative solders to the conventional eutectic SnPb are described from a technical/technological point of view (table 1). Up to now most of the examinations concern the wave soldering processes for the through hole technology and the reflow soldering process for the surface mount technology.

Project /organization	Recommended solder for		
	Reflow soldering	Wave soldering	Repair
ZVEI	SnAg3,9Cu0,6 (217 -219°C)	SnCu0,6 (227°C)	
IDEALS	SnAgCu (eut.:217°C)	SnCu0,7 (227°C); SnAg3,5Cu0,7 (217°C)	SnAg3,5 (221°C)
NEMI	SnAg3,9Cu0,6 (217 -219°C)	SnCu0,7 (227°C); SnAg3 (eut. 221°C)	SnAg3,5 (221°C)
NCMS	SnBi58 (138°C); SnAg3,5 (221°C); SnAg3,5Bi4,8 (205 -210°C)		
Soldertec (ITRI)	SnAg(3,4...4,1)Cu(0,45...0,9) (ca. 217°C)	SnAg(3,4...4,1)Cu(0,45...0,9) (ca. 217°C)	SnAg(3,4...4,1)Cu(0,45...0,9) (ca. 217°C)
JEIDA	SnAg3Cu0,5 (217 -218°C); SnAg(2 -4)Bi(2-6) (205-210°C), SnBi57Ag1 (138°C)	SnAg3Cu0,5 (217 -218°C)	

Table 1: Lead free solders recommended by several organizations/projects for different soldering processes:

ZVEI: Zentralverband Elektrotechnik- und Elektronikindustrie e.V.
IDEALS: Improved Design Life and Environmentally Aware Manufacturing of Electronics Assemblies by Lead-Free Soldering (Brite/EuRam Program)
NEMI: National Electronics Manufacturing Initiative (USA)
NCMS: National Centre for Manufacturing Sciences (USA)
JEIDA: Japan Electronic Industry Development Association (now JEITA)

All of the alternative solders are Sn based alloys. Binary and ternary alloys are mostly examined. The melting temperatures - as the most important factor - differ a lot.

At present most of the activities are directed to tin-silver-copper or tin-silver for reflow soldering and repair and tin-copper for wave soldering.

For the Japanese electronics industry are also very important bismuth and zinc containing solders.

Table 2 shows an overview of the discussed environmental properties of lead free solders that are commonly seen as possible substitutes for SnPb.

Different aspects of the environmental impact of interconnection systems in electronics have been examined covering different phases of the life cycle.

First the Toxic Potential Indication (TPI), is used to give an overall rating. All lead free solders have a better TPI rating than SnPb37, especially tin/copper and tin/zinc solders have good properties. Even the use of the relatively bad rated silver is favourable, because only a small quantity is used in the solder. Information about bismuth is not enough available.

Solder	SnPb (250 °C)	SnCu (280 °C)
Power input until rated value	34 kWh	36 kWh
Time to reach rated value	3,5 h	5,5 h
Power input per h past reached rated value	5 kWh	5 kWh
Power input was determined without PCBs		

Table 3: Power Input for PCB Assembly

Under these conditions the overall power input for soldering with SnCu is 10 to 15 % higher than for the SnPb solder because of its higher melting point of 45 degrees.

Auxiliary materials (flux, cleaning agents) have an important environmental impact on the soldering process with the SnZn alloy which is slightly oxidised. Therefore very aggressive fluxes must be applied and the PCBs have to be cleaned after soldering. That is combined with a certain environmental burden.

To characterize the disposal performance of the solders, the US-American „Toxicity Characteristic Leaching Procedure" TCLP1311 was carried out. Leaching behaviour of SnPb solder is very bad compared to all alternatives. For

Solder	Toxicity (TPI)	Raw Mat. Prod.	Manufact. (Assembly)	Disposal
SnPb37	-	-	+	-
SnAg3,5	+/-	+	+/-	+
SnAg4 Cu0,5	+/-	+	+/-	+
SnCu0,7	+	+	+/-	+
SnBi58	+/-	+/-	+	+/-
SnAg3,5Bi4,8	+/-	+	+	+/-
SnZn9	+	+	-	+

Table 2: Overview about environmental impact of lead free solders in comparison with SnPb Rating the environmental compatibility: Dark grey: very poorly rated, grey: poorly rated, white: well rated

The environmental impact of metal production was measured by the EcoIndicator95 method. The data are available in the literature. The impact of ore mining, transportation and refining (energy consumption and emissions) are summarized to assess the metals. The lead free solders have remarkably good ratings, only bismuth is rated relatively bad because it is assumed that Bismuth is extracted together with lead in these cases. Still the rating of eutectic SnBi58 is better than SnPb37.

The manufacturing processes were coarsely rated according to the assumed energy demand and use of auxiliary materials (flux, cleaning agents, inert gases). Table 3 shows a comparison of energy demand of wave soldering for SnPb and SnCu as measured in a company. For estimation of the power input the heating up value and the energy demand for continuous production from Monday morning until Friday afternoon is assumed.

copper, the leaching from the soldered joints is likely to be negligible compared to the copper PCB-layers. Zinc leaching has not been examined up to now.

At one glance, table 2 shows the potential for environmentally beneficial replacement of lead in the electronic interconnection systems, but also indicates the need for in-depth-studies to choose the appropriate solder.

All of the lead free surfaces are very thin in comparison to the SnPb HASL layers and therefore the layer masses are very small.

Table 5 shows an overview on various aspects of the environmental impact of the different surface finishes along their whole life cycle: the screening assessment by means of the TPI, the assessment of the environmental impact in the raw material production by means of the energy consumption, the assessment of the environmental impact in

Surface finish	Density (layer material) in g cm^{-3}	Layer thickness (µm) and mass (mg cm^{-2}*)	Layer properties
HASL SnPb37	Sn: 7,2 Pb: 11,3	25 / 54,7	Not bondable, multiple solderable, T-stress
Chem Ni/Au	Ni: 8,9 Au: 19,3	5 /0,1 / 11,6	Bondable, multiple solderable, flat layers
Chem Sn	7,2	1 / 1,8	Not bondable, multiple solderable, flat layers
Chem Ag	10,5	0,1 / 0,3	Bondable, multiple solderable, flat layers
OSP	1 (est.)	<0,5 / 0,2	multiple soldering difficult, not bondable, flat layers

*Table 4: Characterization of the lead free finishes in comparison with the SnPb HASL layers (Assumption: *One quarter of the surface is metalized)*

the finish manufacturing by means of energy and water consumption and some short remarks about the environmental impact in the end of life phase.

The screening assessment by means of the TPI shows that the HASL and Ni/Au layers are relatively high (poorly rated) in comparison to the Sn-, Ag- and OSP layers. The reasons are the high toxicity and mass of lead in the HASL and Ni in Ni/Au layers.

5.2 Lead Free Surface Finishes

Up to now the mainly used surface finish is the SnPb Hot Air Solder Leveling (HASL). Alternative lead free surface finishes are

Chem Ni/Au

(Chem Ni/Pd/Au)

Chem Sn

Chem Ag

Organic solder ability protectants (OSP)

The Ni/Pd/Au surface was not included into the following considerations because the market of palladium is very unstable, its costs are difficultly to calculate.

For an average of 50 % of the produced PCBs the surface finishes have to change if the lead ban will become reality. In Asia where consumer electronics is produced the low cost HASL finishes with lead are more applied. The alternatives have not only to comply with technical/technological requirements but should be more environmentally compatible than the conventional HASL SnPb layers.

In Table 4 the different surface finishes are characterized by their layer thickness, the resulting masses of the several materials on a square meter of a PCB and their layer properties.

For the environmental impact of the first life cycle phase - the raw material production - the energy consumption is considered. For the production of the precious metal Au a high energy demand is necessary. That means that the environmental impact for this process is very high.

For the assessment of the environmental impact of the manufacturing the water and energy consumption has to be considered. These results were taken from the PWB Project Surface Finishes of the EPA in USA /4/. There is a distinction between the non-conveyorized and the conveyorized process because of the large differences between them. For further examinations of the environmental process impact all chemicals of the processes have to be included.

As in table 5 is shown, five surface finishing processes consume less water than the reference HASL, non-conveyorized process, including the conveyorized versions of the HASL, chem Ag and Sn technologies, along with both versions of the OSP process. Two surface finishing processes consume more water than the reference process,

Surface Finish	TPI in 10^4 TPI/m^2 PCB	$E_{Raw\,Mat.}$ in 10^3J/m^{2}PCB	Manufacturing				End of Life
			E in 10^6 J/m^2 non-c./ conv		Water consumption in l/m^2 non-c./ conv		
HASL SnPb37	51,7	9615	2,48	1,51	50,5	40,3	Pb leaching
Ni/Au	47,2	73312	5,08	-	83,9	-	Ni-leaching Au-Recycling
Chem Sn	0,2	432	3,28	5,93	73,7	35,6	
Chem Ag	1,1	907	-	3,26	-	21,6	
OSP	0,17	40 (est.)	1,42	0,83	31,3	21,6	No Recycling

Table 5: Environmental impact of lead free surface finishes compared to HASL (conv: conveyorized, non-c: non-conveyorized) Rating the environmental compatibility: Dark grey: very poorly rated, grey: poorly rated, white: well rated

the non-conveyorized version of chem Sn and Ni/Au. The rate of water usage is primarily attributable to the number of rinse stages required by the processes. In general the application of the conveyorized process is generally better than the non-conveyorized process, that means, they consume less water.

Referring to the energy demand table 5 shows, that three of the process alternatives consumed less energy than the reference HASL, non-conveyorized process. Both the non-conveyorized and conveyorized versions of the OSP process, along with the conveyorized HASL process, consume significantly less energy than the reference process. The reductions were primarily attributable to the efficiency of these three processes and their short operating times. On the other hand the long operating time in the case of the Ni/Au process is responsible for the relatively high energy consumption.

For a screening assessment of the environmental impact during the end-of-life phase, especially the disposal behaviour of soldered PCBs, the leaching of the layer materials (only for metals) was examined by means of Toxicity Characteristic Leaching Procedure (TCLP). The results emphasize the well known high solubility of Pb but show that also Ni is very good solved.

Summarizing all facts of the surface finishes from an environmental point of view the OSP finishes should be the best and the NiAu finish should only preferred if technical reasons require it.

6. CONCLUSIONS

Lead free interconnection technologies and cleaner manufacturing will become reality in mass production.

To get a feeling of how alternative materials for interconnection systems would influence the environmental behaviour of electronic products assessment matrices of some solders have been prepared. These matrices show, that in nearly all categories alternative solders are better than tin-lead with a small question mark behind bismuth and Sn-Zn; and that from an environmental point of view the OSP finishes should replace the SnPb HASL layers if technical possible.

But a lot of issues still have to be solved, for instance:

- the environmental impact of solders containing bismuth should be better understood;
- the environmental impact of the manufacturing process with solders containing zinc has to be examined;
- the avoidance of Ni in the surface finish of the PCBs is desirable

However, the environmental impact of a single microelectronic product will be decreased by the various measures, but this positive tendency is still compensated by enormous growth of production numbers and short innovation cycles. Therefore further great efforts are necessary to bring down the burdens for the environment by electronic products.

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PACKAGING AND INTERCONNECT FOR RF AND MICROWAVE

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Key words: packaging, interconnect, single chip package, multichip modules, radio frequency, telecommunication

Abstract: The paper will review different packaging and interconnect issues in the telecom market where RF properties dominate. A short review of single chip packages for different frequency ranges will be followed by a deeper view into multichip modules of different constructions. Last the growing importance of passives and the opportunities to integrate them will be discussed. The view is from a system house that needs to source or subcontract all components and most assemblies.

Tehnologije montaže in povezav za potrebe RF in mikrovalovnih vezij

Ključne besede: montaža, povezave, ohišje z eno tabletko, moduli z večimi tabletkami, radijske frekvence, telekomunikacije

Izvleček: V prispevku obravnavamo različne načine zapiranja in povezav izdelkov za telekomunikacijski trg, kjer prevladujejo RF lastnosti komponent. Kratek pregled ohišij z eno tabletko za različna frekvenčna območja nadaljujemo z globljo analizo modulov z več tabletkami z različnimi konstrukcijami. Nazadnje poudarimo naraščajočo pomembnost pasivnih komponent in obravnavamo možnosti za njihovo integracijo. Opišemo stališče sistemske hiše, ki mora bodisi kupiti ali dati v izdelavo vse komponente in večino sistemov.

1. Introduction

For RF chips, the electrical performance is dominating package construction and assessment work. The aim is to avoid loosing signal strength, avoid electromagnetic interference and still keep the chip cool enough during all use environments. Of course the solutions need to be easy to manufacture, cheap and reliable.

For Micro- and Millimetre- wave chips many semiconductor manufacturers are only now starting to consider delivery in single chip packages and performance is generally specified on bare chip level. Reduced bond-wire length packages are now developed and so are signal compensation elements integrated in package and/or on chip.

Multichip Modules have continuously had a stronghold in RF and High-speed packaging but with the fast growing volumes of RF for Telecom the price pressure is multiplied and very different solutions are needed. Work is ongoing simultaneously on substrate technologies, chip attach and wiring, reliability without hermeticity and last but not least MCM to board second level interconnect reliability and performance.

With the higher integration rate on chips follows a larger number of accompanying passive elements. In RF and analog functions passives dominate. In spite of low cost of passive components their logistics and assembly add to manufacturing cost. As most solder joints in a traditional assembly are for discrete passives their theoretical impact on reliability is big. Both high-speed performance, reliability and substrate space can be greatly improved with integrating the passives instead of using discretes. LTCC has been analysed as a solution for RF MCM-C with integrated passives.

2. MCMs in Telecommunication

In infrastructure telecom equipment performance and cost are biggest development drivers but simultaneously small size comes as a bonus in new packaging and interconnect (P&I) technologies, which also typically has a positive impact on performance and cost. Smaller capacitance and inductance in interconnects and shorter distances to travel all improve signal integrity and minimizes losses.

Main performance limitations have so far come from the chips but as chip design mature and chip size and complexity is approaching a upper limit and as at the same time frequency goes up the need for improvements is coming more focused on the packaging and interconnect technologies.

In Micro- and mm-wave applications, 10 - 60 GHz bare die has been the only format available due to performance losses in single chip packages. The chips have so far been assembled on multiple small special boards layed down in very expensive machined enclosures and have kept this frequency area limited to few and expensive application. Multilayer ceramics has enabled designers to avoid metal enclosures. Limiting assemblies when possible to planar constructions and making these MCMs surface mountable have together limited cost by 2 to 3 orders of magnitude, opening wide avenues of new applications.

3. Passive integration

As complexity is growing so are the number of passive elements. As passives are much bigger than transistors their P&I is becoming more important. Multilayer ceramics and thin film are two preferred methods for this integration. RF and mm-wave functions can be cost efficiently realised in integrated passive elements reducing the need for semiconductor elements. In these high frequency applications multilayer ceramics is the most preferred solution, especially the high conductivity in noble conductors in LTCC in combination with arising offerings of mixed dielectric constants are promising. Thick and thin film resistors complete the technology palette.

By integrating passive elements in a substrate and attaching active chips on top, Multichip modules get an increased significance and competitive edge. Cost efficiency is achieved when known good functional building blocks are the result.

4. RF and Microwave elements and features

Many microwave functions such as filters, hybrids, couplers and baluns can simply be realised with metal strips on one or more dielectric layer, perhaps including resistors but totally without semiconductor components.

There are straightforward design and simulation packages for generating these elements but there are two problems included. On one hand RF and millimetre wave elements always have an area of interaction around them. This give rise to unwanted interference with neighbour elements and also changes in functionality when materials like overcoat or underfill are added. These are much more difficult to forecast and manage in 3D geometries. The other difficulty is the impact of geometrical and material property variances and tolerances and their impact on functionality and functional tolerances. This is a much bigger problem if the supply chain is long and the end-product designer has no direct contact with the substrate manufacturer sourcing the MCM manufacturer.

As applications for millimetre wave arise there is a total lack of substrate suppliers offering fully characterized LTCC substrates and design libraries for these. The only alternative is to make an estimation of performance and run a number of prototype rounds. Can shared test circuit panels be used the same way as multi purpose wafers for semiconductor development? At least we can design test panels with same elements but a variance of dimensions to test out best performance as function of dimensions.

It is thus not very easy to embed these RF elements in the substrate but if so done the top surface can be reserved for other functions demanding active chips.

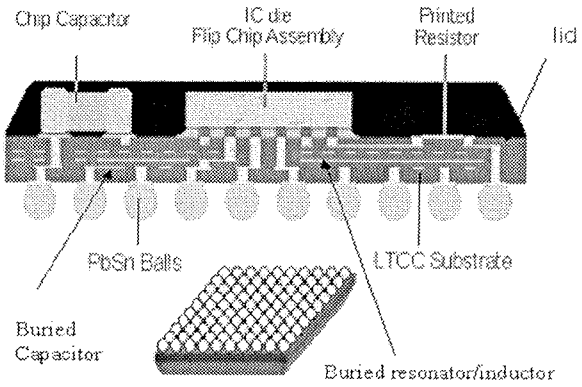

Fig. 1 A schematic picture of a MCM-C for RF applications

5. Subcontracting RF MCM-C

Many modern telecom manufacturer is not at all vertically integrated but has to purchase or subcontract all components and boards. Many semiconductor components are easy to buy off the shelf but most MCMs are custom designed. RF and mm-wave modules are very difficult to design and product management is possible only if a close working collaboration is established between supplier and end product manufacturer. In the relationship also technology responsibility need to be shared down the supply chain, the end product manufacturer can take responsibility only for developing the market and his product for it. What he needs is fully functional SMD MCMs to be applied as supercomponents in his products.

In few last years the LTCC technology has been developed a lot providing cost efficient supply. In the western world these manufacturers use mainly commercial materials that are very well characterized and known. As soon as more special materials are brought into the market place an external designer is on really deep waters as all aspects are not yet documented and second sourcing may be impossible to get.

In Asia the approach is the opposite: LTCC manufacturers have their own proprietary materials that they know them selves but may be difficult to understand totally in a distant country where end product is developed. Second sourcing can be achieved only by internal second sourcing with geographycally separated factories.

In spite of all know how and design help the RF and mm-wave elements and especially the whole module is so hard to design with today's tools and material knowhow that the rule is to have at least three design rounds before satisfactory results are achieved. Running these trial rounds take time if the physical and organisational distance between designer and substrate manufacturer is long. Partnership is here needed for smooth collaboration. Fortunately tooling and running multilayer ceramic rounds is nothing compared with semiconductor rounds, takes weeks instead of months. But in many cases both are needed: Some custom chips are developed with few months turn around and when they finally arrive the manufacturer would like to have ready proved ceramic substrates. If these then are not fully compatible, the hope is that corrective actions can be implemented on ceramics only thus allowing next round to take only weeks.

In fact there is normally a third level of interconnect, the PWB motherboard, where performance still need to be excellent. Not to speak about the 3D integration of boards, external components and perhaps wave guides.

6. Environmental issues

P&I dominate the environmental impact of electronics products . Higher integration level normally diminishes the impact. This is especially true when Pb containing solder joints of discrete passive elements are replaced by the in situe interconnects in the ceramic substrate. In the case of semiconductor components, Pb solder joints may be replaced with wirebonds or Pb free, miniaturised FlipChip joints.

Some high K dielectrics, either in discrete components or integrated in a multilayer ceramic contain Pb. Some manufacturers have a total Pb-free policy and have been able to realise all their products with such Pb free ceramics.

The other emphasized environmental threat comes from the fire retardant halogens. Here all ceramic solutions like MCM-C have an inherent fire retardance due to the nature of the ceramics.

7. Conclusion

Passive integration is the best in multilayer ceramics based MCMs.

Need for passive integration give new speed to MCM utilisation.

Multilayer ceramics material and processes developing fast, knowledge of their microwave properties and tolerances in production are lacking.

Design tools are improving but integrated solutions and tools are only slowly appearing.

Prototyping turnarounds are typically short, few weeks in teory, actual time is depending on partnership relation.

Pb-free solutions are existing.

MCM-Cs are inherently safe without fire retardants.

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LTCC IN MICROSYSTEMS APPLICATION

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Key words: LTCC technology, MCM package, microsystems, sensors, activators

Abstract: Low Temperature Cofired Ceramic (LTCC) technology is used for many years as Multichip Module package. Recently LTCC found very wide area of application in microsystems thanks to very good electrical and mechanical properties, high reliability and stability as well as possibility of making three dimensional (3D) microstructures. The paper describes the new LTCC techniques developed for making microsystems. A short overview of various LTCC sensors, actuators, heating and cooling devices is given. The newest application of LTCC technology (fuel cell, microreactors, photonics and MOEMS packaging) are shortly described.

Uporaba tehnologije LTCC za izdelavo mikrosistemov

Ključne besede: tehnologija LTCC, tehnologija MCM, mikrosistemi, senzorji, aktivatorji

Izvleček: Tehnologijo LTCC (Low Temperature Cofired Ceramics) uporabljamo že mnoga leta za izdelavo MCM (Multi Chip) modulov. Zadnje čase tehnologijo LTCC uporabljamo tudi za izdelavo mikrosistemov, predvsem zaradi dobrih električnih in mehanskih lastnosti, visoke stopnje zanesljivosti in stabilnosti ter možnosti izdelave tridimenzionalnih (3D) mikrostruktur. V prispevku obravnavamo novo LTCC tehnologijo za izdelavo mikrosistemov. Podamo kratek pregled LTCC senzorjev, aktuatorjev ter grelnih in hladilnih komponent. Opišemo tudi nekatere najnovejše uporabe te tehnologije za izdelavo gorilnih celic, mikroreaktorjev, fotonike in MOEMS ohišij.

1. INTRODUCTION

Low Temperature Cofired Ceramic (LTCC) technology is known since eighties /1-3/. LTCC modules with conduction lines were made as first ones. After some years passive integrated elements (MCIC) were added. The technology is well established both for low volume high performance application (military, space) and high volume low cost application (portable wireless, automotive) /4/. LTCC module becomes more and more sofisticated. Recently, the module consists of conduction lines, passive elements and microsystems (sensors, cavities and actuators, cooling and heating systems). Moreover, MEMS and MOEMS package modules made from LTCC ceramics are developed /2,5-7/.

The paper presents general information on typical LTCC technology. New techniques developed for making microsystems (fine line patterning, micromachining of LTCC tapes, lamination, making of cavities, holes and channels) are described. A short overview of most popular LTCC sensors and actuators application is given (gas sensors, gas and liquid flow sensor, temperature sensor pressure sensor, proximity sensor, microvalve, micropump). Moreover, the information on newest application of LTCC technology, such as fuel cell, microreactors, photonics and MOEMS packaging are given.

2. LTCC TECHNOLOGY

Typical LTCC module consists of dielectric tapes, external and internal conductors, surface and buried passive components, thermal and conductive electrical vias. Additional elements are added on the top and bottom of the module using various assembling methods. Flow diagram of a typical LTCC process is presented in Figure 1. LTCC tape is cast on Mylar and stored in this way. Two basic materials are used in the tape fabrication - alumina filled glasses and glass-ceramic materials. After removing from the role, the tape is blanked to a specific size. In the next step the registration holes, vias and cavities are made. The vias and cavities are formed by mechanical punching, drilling, laser formation or photo patterning. The vias are filled with Ag or Au conductor inks. The conductor and passive components are printed by a standard screen printing method. The conductor (Ag, Au or PdAg) and resistors (RuO_2) films are made of almost typical inks. The use of these materials is possible because of the low cofiring temperature equal to 850°C. After printing and drying the sheets are stacked on a lam-

inating plate and laminated in an uniaxial or isostatic laminator. The typical laminating parameters are 200 bar at 70°C for 10 minutes. After laminating process the structures are cofired in two steps (Figure 2). In the first step, at around 500°C, the binder is burn out. In the second step, at 850°C, the final structure is formed. The fired parts typically shrink 12±0.2% in the x- and y- directions and 17±2% in the z- direction. After cofiring the thick film or thin films components can be made on the top and bottom surfaces and additional active or passive elements are added using various assembling methods.

The sheet resistance of Ag and Au conductor lines is equal to 2 ÷ 5 mΩ/sq. The passive elements may be placed on the top of the substrate (surface) or inside the structure (buried). The buried elements are formed as planar (2D) or three dimensional (3D) /8-13/. Schematic cross-section of 2D and 3D LTCC resistor are shown in Figure 3. To increase the final inductance LTCC integrated inductors can be fabricated as planar windings or as a multilayer structure (Figure 4) /11,14/. Capacitors are usually made of two or more plate electrodes with dielectric layer between them. High k dielectric ($BaTiO_3$ or relaxor materials) are widely used for capacitor pastes.

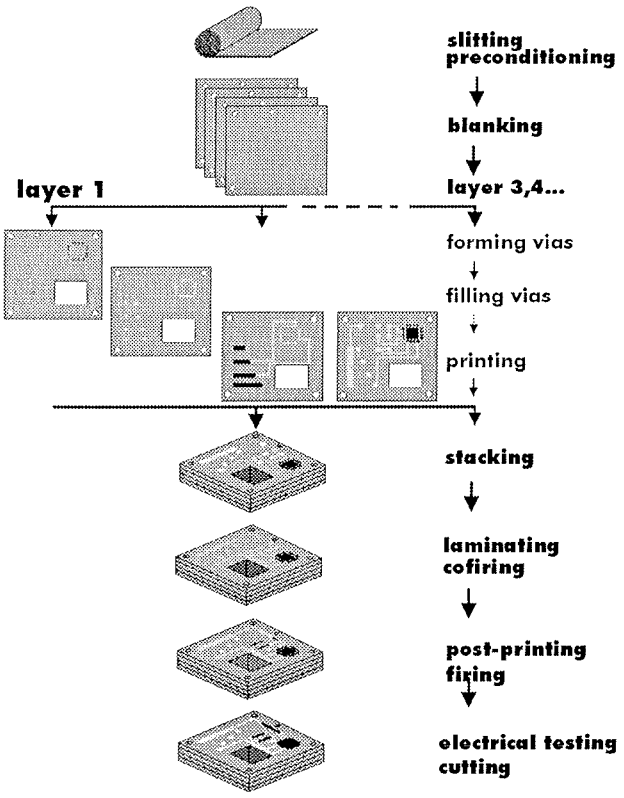

Figure 1: LTCC process flow

New materials are used for tape casting (high k, piezoelectric, piroelectric etc.) and new LTCC techniques are developed for making LTCC microsystems. These techniques are connected with the following processes:

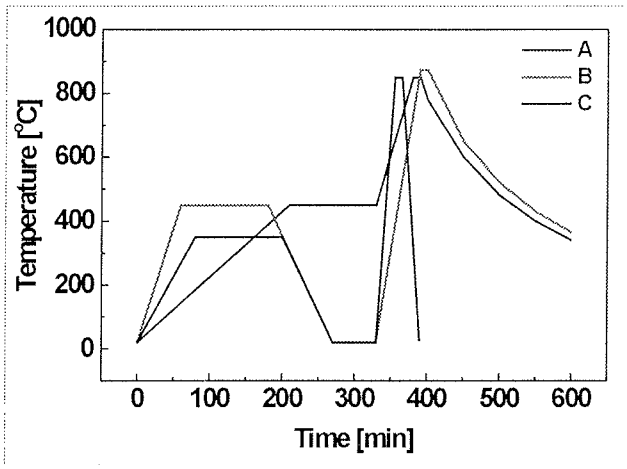

Figure 2: Cofiring profile

- fine line patterning,
- micromachining of LTCC tapes,
- lamination,
- making of cavities, holes and channels,
- bonding of LTCC tapes to other materials.

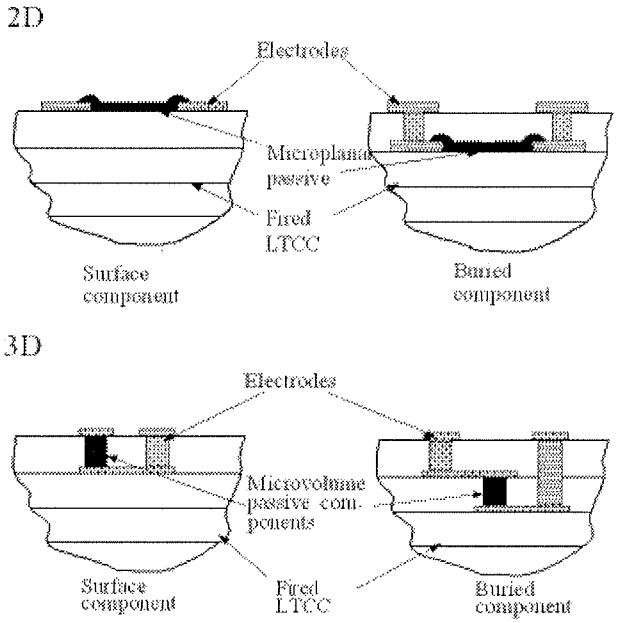

Figure 3: Schematic cross-section of 2D and 3D LTCC resistor

2.1 Fine line patterning

Narrow and precise thick film lines are very important for miniaturisation of electrical equipment and proper work condition for sensors and actuators. Various methods are used for fine line patterning:

- fine line printing,
- FODEL photosensitive pastes (etching of unfired films),

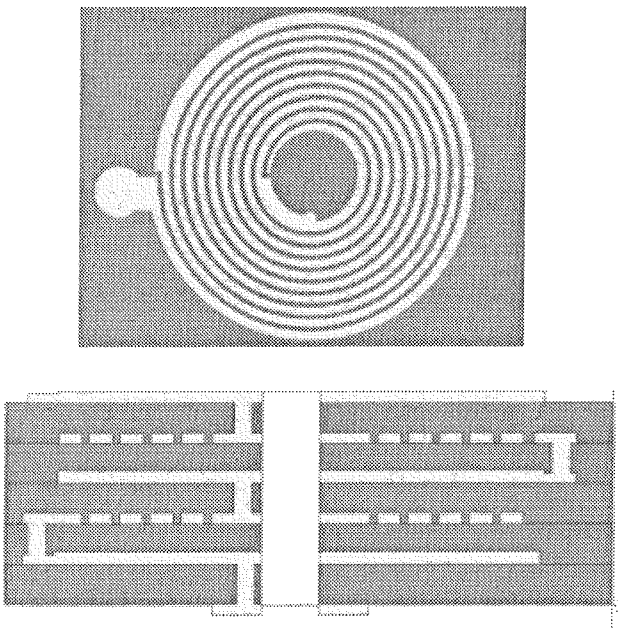

Figure 4: Top view and cross-section of five layers LTCC inductor

- photoimageable paste (etching of fired films),
- gravure printing method /15-17/,
- laser patterning.

Examples of FODEL and laser fine line patterning are shown in Figures 5 and 6.

2.2 Micromachining of LTCC tapes

Making of three dimensional structures, channels and cavities is possible due to special methods of LTCC tape micromachining. The most frequently used methods are:

- laser micromachining /19-21/,
- numerically controlled milling method /7/,
- jet vapor etching /7/,
- photolithographic patterning /7,18,22/,
- using of photoformable LTCC tapes /7,23/,
- casting /6/,
- embossing /6/.

To machine the LTCC tapes with the smallest tolerances Nd-YAG and excimer laser can be used. Computer controlled x-y movement of the workpiece produces complex shapes. Laser cut vias in LTCC tapes from various materials are shown in Figure 7. The channel in LTCC module made by laser is presented in Figure 8.

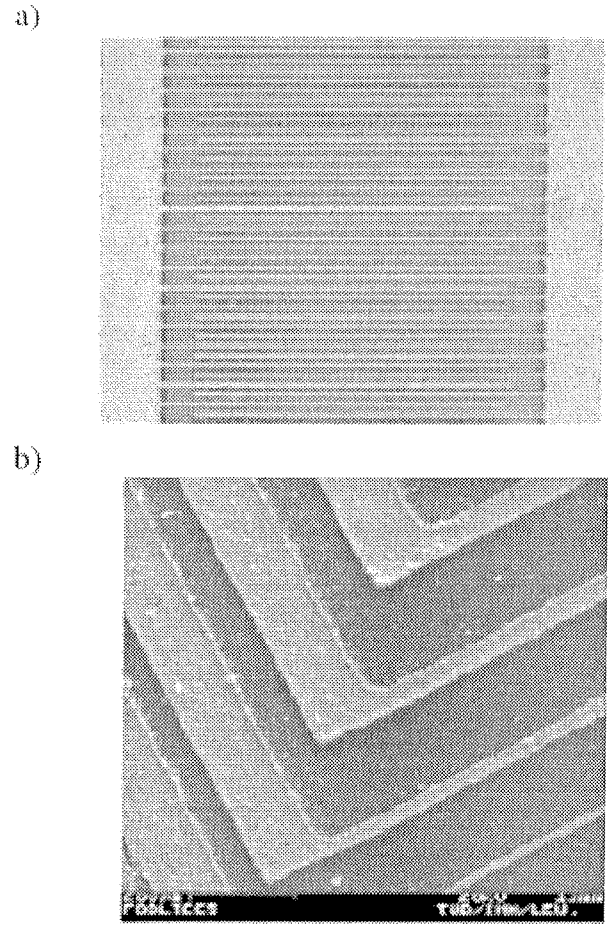

Figure 5: a) Example of an capacitor pattern with 40 μm line width and space realized by the FODEL Q170P on alumina b) test pattern of FODEL Q170P on LTCC /18/

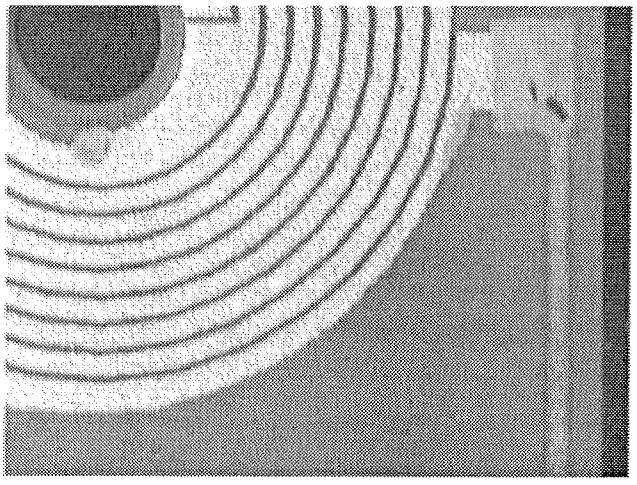

Figure 6: Fine-line laser patterned top layer inductor spirals /11/

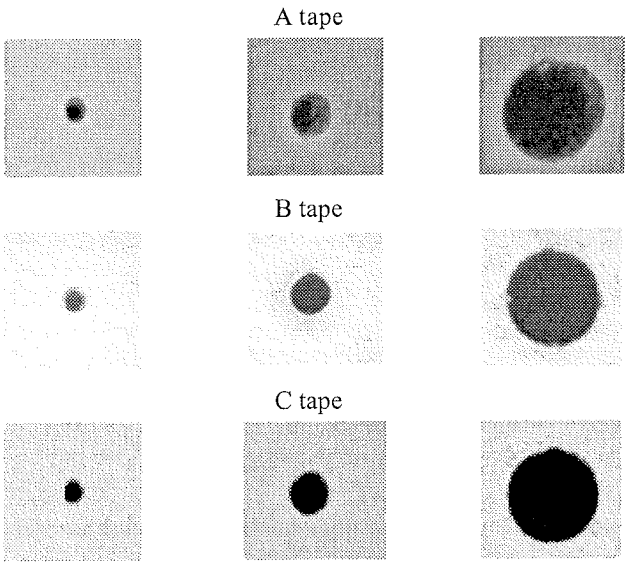

Figure 7: Holes with 75, 150 and 300 μm nominal diameter made in various LTCC tapes by laser /21/

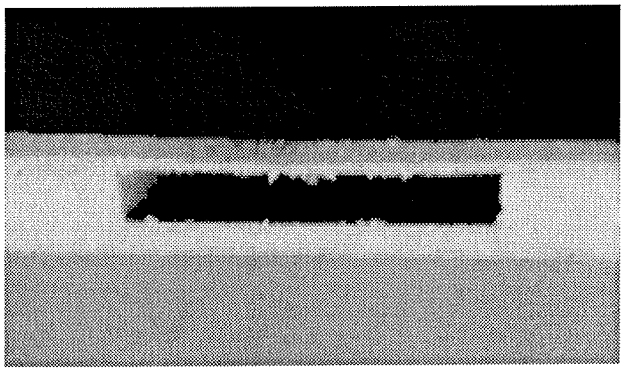

Figure 8: LTCC structure with 2 μm wide channel cut by laser /21/

In the processing of LTCC modules sagging of suspended structure is a problem. The plastic deformation takes place during lamination or cofiring processes /24/. Utilizing Mylar inserts or using lower lamination pressure prevent lamination deformation. Cross section of laser cut channels laminated at various pressures is shown in Figure 9. To avoid sagging during cofiring process the following methods can be used /25/:

- deposition of thick films to compensate auto-supported structures,
- use of sacrificial materials,
- use of fugitive paste,
- bonding of fired LTCC tapes

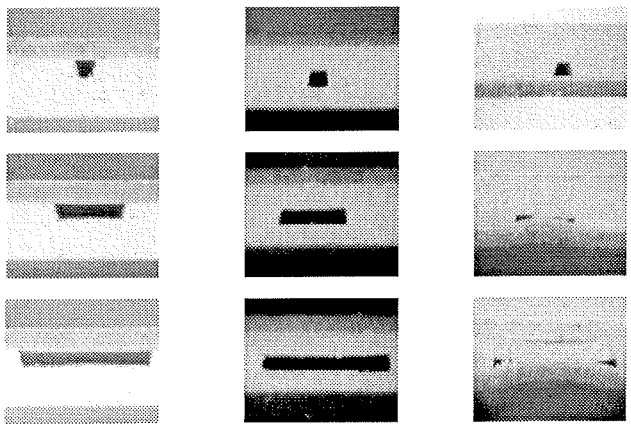

Figure 9: Cross section of laser cut channels laminated at various pressure P (channel width 100, 500 and 1000 μm) /21/

3. SENSOR AND ACTUATORS

Various kind of LTCC sensors and actuators are made in LTCC microsystems. The most popular ones are:

- gas sensors /26-32/,
- gas and liquid flow sensor /25,33/,
- temperature sensor /34/,
- pressure sensor /35,36/,
- proximity sensor /37/,
- microvalve /38/,
- micropump /39/.

There are two kinds of gas sensors. The first is based on tin oxide compositions. The construction of such sensor is shown in Figure 10 /40,41/. The second type of LTCC gas sensors is based on electrochemical processes /30-32/. RTDs, thermistors and thermocouples are typical LTCC temperature sensors. An example of pressure sensor with thick film piezoresistors on the LTCC membrane is shown in Figure 11. There are three main different types of LTCC microvalves: with heater and heated liquid moving the valve /38/ (Figure 12), with moving piezoelectric membrane and hybrid contained silicon membrane with magnet and LTCC coil. Magneto hydro dynamic (MHD) effect is used in LTCC liquid mixer and pump /39,42/. Another interesting application of LTCC are three-dimensional shells for miniature system /43/. Magnetostatically actuated curved LTCC shells are used in three degree of freedom spherical stepper motor.

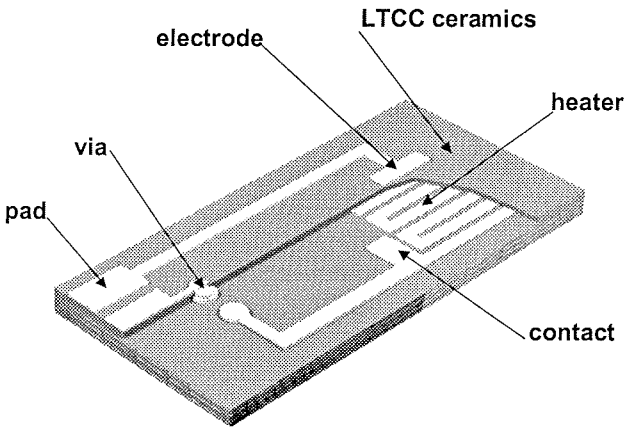

Figure 10: Basic construction of the gas sensor /41/

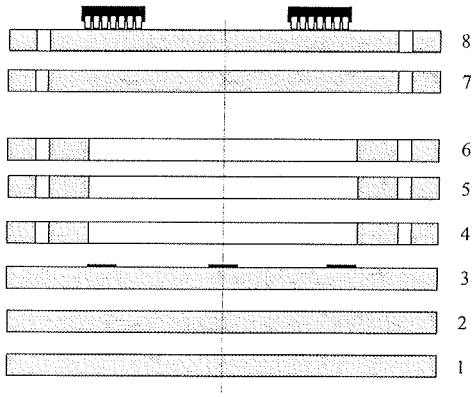

Figure 11: Cross-section of 3D LTCC pressure sensor

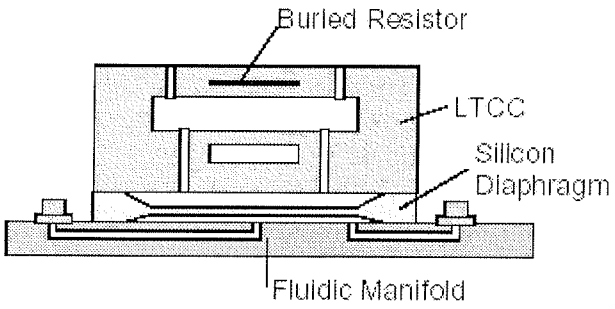

Figure 12: Microvalve principle setup /38/

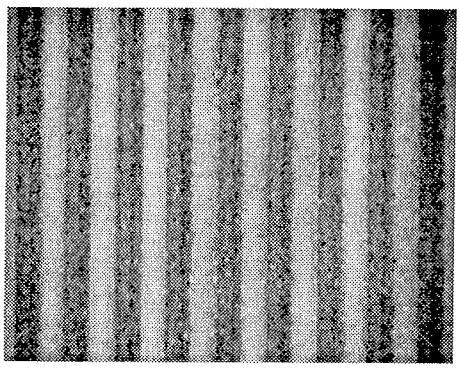

Figure 13: Heater pattern cut by laser (line width 100 μm)

4. HEATING AND COOLING SYSTEMS

Heating and cooling systems are very important parts of LTCC microsystems /39,44-52/. The heaters are made of typical thick film resistors or Pt-based conductors printed in the meander pattern. The second kind of heater can be used additionally for measuring the temperature. The example of LTCC platinum heater cut by laser is presented in Figure 13. Heat pipe /46/ and liquid cooling /21,48,50-52/ systems are most frequently used in LTCC cooling devices. Basic construction of LTCC liquid cooling system is shown in Figure 14. The power needed to be supplied to obtain maximum of the structure temperature equal to 80°C is given in Figure 15. The various types of cooling methods are compared in this Figure.

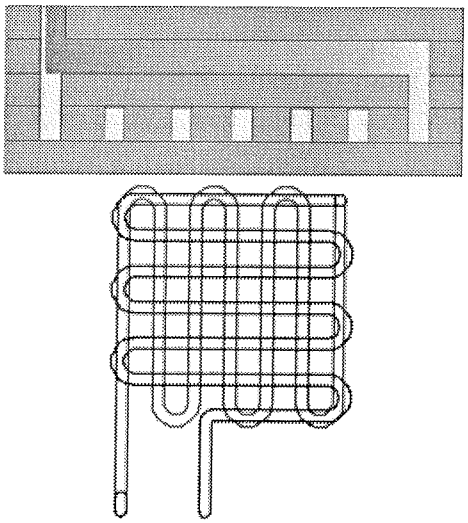

Figure 14: Basic construction of cooling system (top - cross-section, bottom - top view of channel meander) /21/

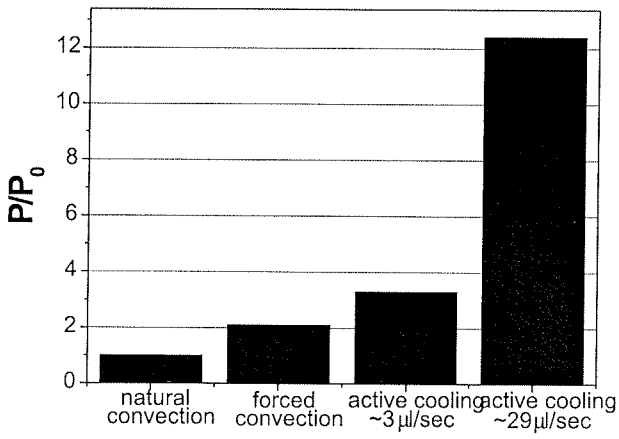

Figure 15: Comparison of power applied to heat source (normalised to P_0) for different types of cooling methods /21/

5. OTHER APPLICATIONS

Other important applications of LTCC are miniature fuel cell energy conversion systems, Micro Total Analysis Systems (μTAS), Fluid Injection Analysis (FIA) structures, photonic devices and MEMS packaging /5-7/.

There are two approaches for producing of the miniature methanol based fuel cell systems: direct methanol conversion (DMFC) and a micro reformer H_2 based system /6/. Development of a chemical microreactor is a key element for fuel cell microsystems.

LTCC technology can be applied to built microsystems for drug delivery, biological parameter monitoring, gas or liquid chromatographs, cooling and heat exchangers, particle separators, polymerase chain reaction (PCR) devices and micro combustion chambers /7,53/. LTCC PCR device was used for DNA amplification using an external peristaltic pump for genotyping experiments /54/.

A three stage LTCC microdischarge device, having an active length of about 0.27 mm and a cylindrical discharge channel 140-150 μm in diameter has been developed and operated in Ne gas /55/. It can be used as UV source in biomolecule assay operations where the targed molecule is fluoresced in the UV light. LTCC grid was used as a focusing electrode in field emitter arrays to obtain high brightness and small electron beam size /56/.

LTCC materials will be applied for the next generation packaging for fiber optic and electro-optic /5/. Opto-electronic systems require direct input/output of optical, RF and other sensitive signals through the package using fiber-optic, coaxial and/or other interconnection approaches. Precise optical alignment is critical to achieve performance capabilities. The opto-electronic MEMS packaging and laser alignment based on a LTCC structure are described in /57,58/.

MEMS packaging is an another very wide field of LTCC application /59-63/. The LTCC package for MEMS Si katharometer cross-section is shown in Figure 16. The package protects the katharometer against mechanical damages and allows on an easy connection of electrical signals. Moreover, the heater and temperature sensors stabilise the temperature of the element.

6. CONCLUSION

The LTCC technology meets the requirements for next generations of microsystems application due to a very good electrical and mechanical properties, high reliability and stability as well as possibility of making three dimensional (3D) microstructures. The new LTCC techniques were developed for making microsystems. A short overview of these techniques and various LTCC sensors, actuators, heating and cooling devices was given in the paper. The newest applications of LTCC technology (fuel cell, microreactors, photonics and MOEMS packaging) are very promissing.

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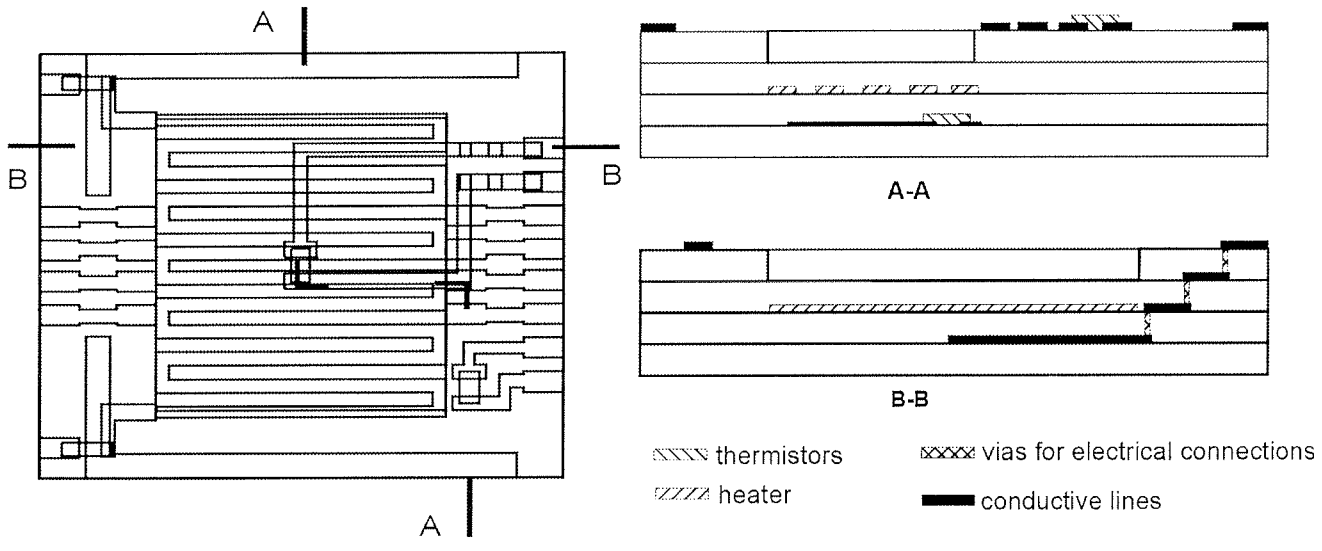

Top view of the structure

Figure 16: The LTCC package crossection

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MATERIALS FOR DIFFUSION-PATTERNING; THICK-FILM INTERCONNECTIONS TECHNOLOGY

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Abstract: Diffusion patterning is a dielectric patterning technology, which is used in the screen-printed thick-film technology for higher density multilayer circuits. This technology is suitable for producing lower cost multichip modules and requires a low additional investment in conventional thick-film technology production lines. Comparisons of via resolution capability of diffusion patterning versus conventional thick-film technology are described and discussed. Preliminary experimental results obtained with a test circuit showed that 200 μm lines and 200 μm vias could be achieved with acceptable yield and with minimal modification to standard production lines. A few results of an investigation of some thick-film materials, which comprise the "set" of pastes for diffusion patterning technology, are presented. The electronic circuit for the pressure sensor was designed with the advantages of semi-custom ASIC and realised with the verified technology as a low-cost ceramic multichip module.

Materiali za difuzijsko oblikovanje; tehnologija za debeloplastne povezave

Ključne besede: debeloplastna tehnologija, materiali, difuzijsko oblikovanje, večplastna vezja, upori

Izvleček: Difuzijsko oblikovanje je debeloplastna tehnologija, ki z običajno tehniko tiskanja in žganja omogoča izdelavo večplastnih vezij z večjo gostoto komponent. Ta tehnologija je primerna za izdelavo cenejših keramičnih modulov z golimi silicijevimi tabletkami (MCM-multi-chip modules), ker zahteva samo minimalne dodatne investicije k obstoječim linijam za proizvodnjo debeloplastnih hibridnih vezij. V članku primerjamo in ocenimo "sposobnost" resolucije odprtin v dielektriku v večplastnih vezjih v primerjavi s "klasično" debeloplastno tehnologijo. Eksperimentalni rezultati so pokazali, da lahko ponovljivo izdelamo 200 um linije in 200 um odprtine z minimalnimi spremembami obstoječe tehnologije. Predstavljeni so izbrani rezultati testiranja materialov za difuzijsko oblikovanje. Elektronsko vezje za senzor pritiska, ki je bilo izdelano s to tehnologijo, je prikazano kot primer uporabe difuzijskega oblikovanja.

1. Introduction

The density of electronic packaging is increasing due to the requirements for higher performance and smaller size in electronic systems. Since smaller size and lighter weight with lower cost are basic requirements, multi-chip module (MCM) technology is an essential technology to meet these demands. Typical MCMs are realised by using bare dies or dies in chip-scale packaging, because the absence of additional leads provides a shorter interconnection length and higher density. Multilayer interconnections contribute significantly to the reduction of overall dimensions. There are several technologies and materials which enable the realisation of interconnections for multichip modules. The general types of MCM are: high-density glass-epoxy laminated printed-circuit board (MCM-L), thick-film on ceramic substrate (MCM-C), and thin film on ceramic or silicon substrate (MCM-D). Each combination of these technologies and materials offers a different level of performance/cost ratio /1-7/. A ceramic MCM-C can be realised using LTCC (low-temperature co-fired ceramic), HTCC (high-temperature co-fired ceramic) and thick-film technology, including also photo-patternable and diffusion-patternable technology. An additional contribution to the smaller size and higher density of MCM-C is the ability to integrate screen-printed resistors or sometimes capacitors and inductors. These screen-printed components can be placed either beneath the discrete components on the surface of the multilayer dielectric or be buried (sandwiched) within the multilayer structure /8-11/.

2. Feasibility study

The market for pressure sensors is one of the largest of all sensor technologies, as a consequence the technology and applications of pressure sensors have developed rapidly. The market niche for small and medium enterprises (SMEs) is to develop and produce application-specific sensors integrated in miniature electronic (sensor) modules.

The technology foresight of the HIPOT-HYB Company (which is an SME) is based on a strategic orientation to research, design, develop and produce pressure sensors and hybrid circuits. The competitive advantage of the HIPOT-HYB Company is the use of thick-film technology in sensor applications. This technology is used in two ways, to produce the sensor elements themselves and/or the electronic circuits for signal processing. However, these days the design of new pressure sensors is faced with strict requirements: device size is reducing, functions and performances are expanding; while at the same time the cost of the sensor is restricted. In this respect the developments in sensor technology for small- and medium-volume production have two directions. The first direction is to integrate all or most of the electronic functions into an application-specific integrated circuit (ASIC), the second is to use one of the lower cost high-density interconnection technologies to integrate the sensing element, ASICs and passive components in a sensor module. A multichip module (MCM) is an essential technology to meet these demands.

The special requirements for the mechanical (pressure) sensor application which must be considered:

- Analog and mixed analog-digital functions;
- A low-frequency range from DC up to 10MHz clock in digital applications;
- Low power consumption;
- A small number of electronic components;
- The maximum number of conductive layers is 3 or in some cases 4;
- Restricted external dimensions;
- Mechanical and thermo-mechanical properties suitable for use in mechanical sensor applications;
- Electomagnetic compatibility (EMC) aspect;
- Ecological aspects.

Due to above-listed requirements, and in particular the mechanical and thermo-mechanical properties, the ceramic multichip module (MCM-C) is an essential or at least a "good" technology to meet these demands /12-14/. A ceramic is probably the most common substrate material for pressure sensors, with a silicon die as the sensor element. The reason lies in its physical properties, which include: high compressive strength and hardness; thermal expansion similar to the silicon die and dimensional stability. In some applications high resistance to chemical attack is also important.

The interconnection performance (number of layers, via size and line pitch) of ceramic multichip module technologies for photo-patternable, screen-printed, diffusion-patternable and LTCC technologies is shown in Fig 1 /15/.

3. Diffusion-patterning technology

Thick-film multilayers are made by printing and firing alternate layers of conductors and dielectrics. The dielectric

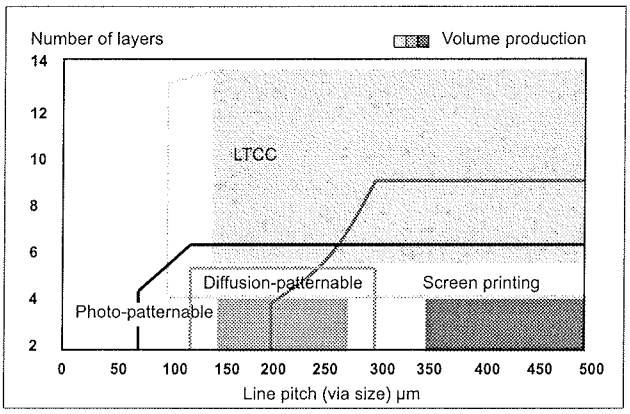

Fig. 1: Interconnection performance of ceramic multichip module technologies /14/.

layer covers the whole area of the substrate. Conductor layers are connected through openings - vias - in the dielectric film. Thick-film pastes are tixotropic; this means that the paste should flow easily when the squeegee pushes it through the screen mesh during screen printing and then "freeze up" in the desired shape on the substrate. However, in the case of multilayer dielectrics, which cover large areas, some compromises are needed. If the multilayer dielectric paste is "stiff", small and well-defined vias can be made. However, small undesirable pinholes could also appear in the layer resulting in short circuits between upper and lower conductor. Therefore the viscosity of the paste should be low enough so that it flows a little after screen printing to "heal", i.e. close up any pinholes. However, this means that vias should be large enough so that they will stay open. This is shown schematically on the left side of Fig. 2. In hybrid circuits production, this limits the dimensions of vias to something like 400x400 um^2.

Diffusion patterning (Diffusion Patterning is a trademark of the Du Pont company) is a technology, which enables the production of smaller vias with standard thick-film technology /16,17/. For diffusion patterning, a layer of dielectric paste Q-42-DP (DP-diffusion patterning) is screen printed over the whole circuit without vias for connecting lower and upper conductor layers. The relatively low viscosity of the dielectric paste, partly due to a lower inorganic content, results in a smooth film with few or no pinholes. After drying of the dielectric layer, the droplets of diffusing (or image) paste are screen printed on to the dielectric layer. Image paste consists of an organic material and an inert alumina filler. At elevated temperatures this organic material diffuses down into the dried and polymerised organic vehicle of the dielectric. Diffused parts are then washed out with warm water (around 80°C) enabling the "creation" of small round vias. This is shown schematically on the right side of Fig. 2. All further production steps are the same as with standard thick-film materials. Unlike standard vias construction with screen-printing, diffusion patterning vias do not need any extra substrate space. The dimensions of vias are similar to the width of the conductor. It is estimated that complex hybrids can therefore be built on 20% to 40% smaller substrates.

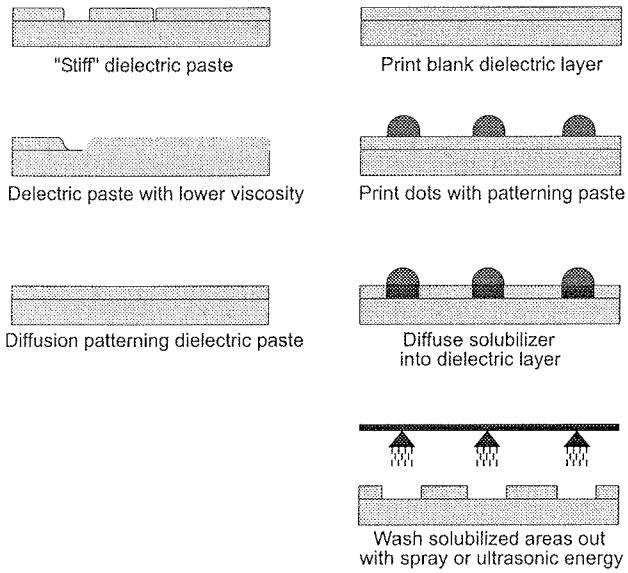

Fig. 2: Vias, realised with standard multilayer dielectric (on the left) and with dielectric for diffusion patterning (on the right) - schematically

The main difference between conventional thick-film multilayer technology and diffusion patterning is an organic part of the multilayer dielectric paste. It is based on a hydrogen bonded acidic acrylic polymer. The active phase in the image paste, which is coloured black for better screen-printed resolution, contains an alkaline organic. During diffusion base and acid materials react and break hydrogen bonds in the acrylic polymer. This results in a reduced green strength of the dielectric layer and enables washing out of the weakened material. The schematics of the diffusion mechanism are shown in Fig. 3 (after Needes et al. /18/).

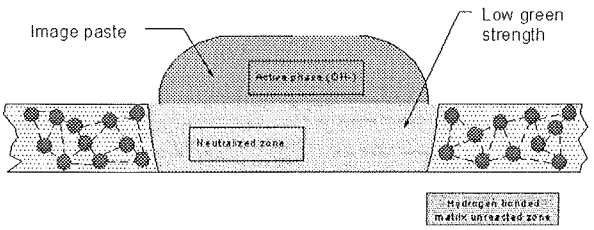

Fig. 3: The schematics of the diffusion mechanism /18/

The diffusion patterning technology is based on high-quality multilayer dielectric material compatible with silver conductors and resistor materials for printing and firing on or under dielectrics. Inorganic material in the Q 42 DP dielectric is the same as in the multilayer dielectric QM42 and is based on the mixture of crystallizable glass and ceramic filler /19/. The silver conductors are used for the inner conductor layers and the Ag/Pd and/or Au are used for the top conductor layer only. Discrete components are added by chip-and-wiring technology and/or with one of the SMT technologies (SMD, Flip-chip,...). Thick-film materials include two resistor series, QM 80 and QM 90, for making resistors on the top of the dielectric layer. Resistors from the QM 80 series are designed for Pd/Ag termination, while those from the QM 90 series are terminated with silver. /20,21/.

Some features of the diffusion patterning process are:

- Substrate: 96% Al_2O_3
- Multilayer dielectric for diffusion pattering Q42DP
- Image paste Q95IP
- Conductors: Ag (Au, Ag/Pd, Ag/Pt)
- Resistors: 1 ÷ 10 Mohm, on dielectric
- Minimum tracks width: 200 μm (150 μm)
- Minimum tracks separation: 200 μm (150 μm)
- Minimum via diameter: 200 μm (150 μm)
- Minimum crossover area/pitch: 400 μm (300 μm)
- Number of conductor layers: 4
- Size reduction factor (compared to the standard multilayer process): 0.6 ÷ 0.8

4. Diffusion-patterning - materials

In this part of the paper the results of an investigation of some thick-film materials which comprise the "set" of pastes for diffusion-patterning technology will be presented. For microstructural investigation the thick-film materials, printed and fired on alumina ceramics, were mounted in epoxy in cross-sectional orientation and then cut and polished using standard metallographic techniques. A JEOL JSM 5800 scanning electron microscope (SEM) equipped with an energy dispersive X-ray analyser (EDS) was used for overall microstructural and compositional analysis. Prior to analysis in the SEM, the samples were coated with carbon to provide electrical conductivity and to avoid charging effects. The conductive phase in the resistors and the "nature" of ceramic filler in the Q42-DP multilayer dielectric were determined by X-ray powder diffraction analysis (XRD) with a Philips PW 1710 X-ray diffractometer using Cu Kα radiation. X-ray spectra were measured from 2 Θ = 20° to 2 Θ = 70° in steps of 0.04°.

4.1. Silver-based conductors

QM 14 is a silver conductor for inner-layer interconnections and QM 34 is a via-fill conductor for buried vias and connections to Ag or Pd/Ag upper conducting layers in a multilayer structure. In Figs. 4.a and 4.b microstructures of QM-14 and QM-34 conductors are shown, respectively. Both materials were fired at 850°C. EDS microanalysis showed that both conductors are based on pure silver. The microstructrure of the QM 14 conductor is densely sintered. The diameter of the grains is from a few micrometers to more than ten micrometers. Exaggerated grain growth is due to the firing temperature, which is close to the melting point of silver at 960°C. On the other hand, the microstructure of QM 34 is porous with small grains of approximately one micron in diameter. On the boundaries of the silver grains small particles of secondary phase with

sub-micrometer dimensions are seen. In Fig. 4.b the particles are denoted with arrows. EDS semiquantitative analysis showed the presence of aluminium, silicon and oxygen. This alumosilicate secondary phase is added to inhibit the grain growth and densification during firing. For the via-fill paste it is important that the volume of dried and fired material is similar. In that way the vias stay filled with the conductor "cylinder" and no cracks, due to shrinkage, appear either between the via-fill conductor and the dielectric or the via-fill conductor and the upper and lower conducting layers.

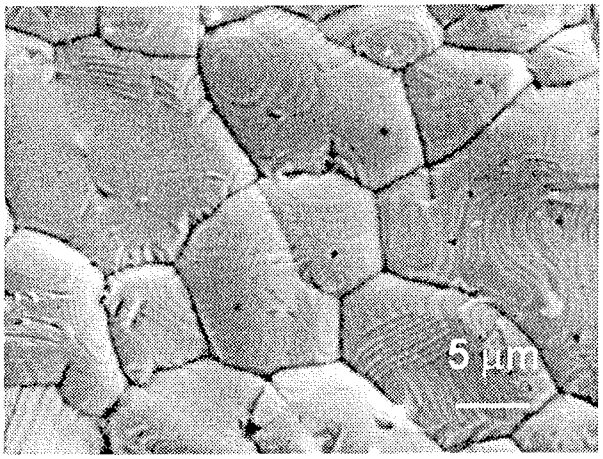

Fig. 4.a: The microstructure of silver-based conductor QM-14, fired 10 min. at 850°C.

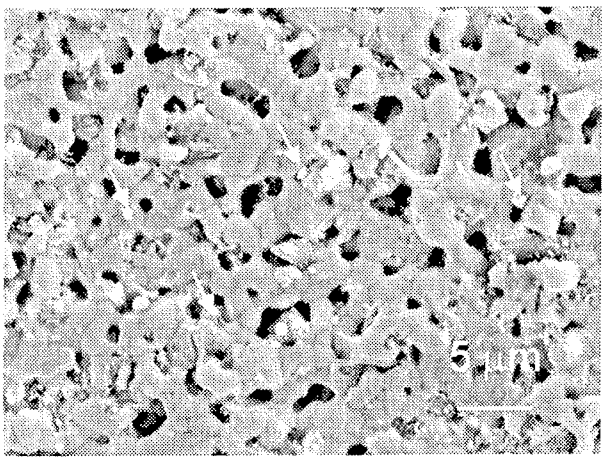

Fig. 4.b: The microstructure of silver-based via-fill conductor QM-34, fired 10 min. at 850°C.

4.2. QM-42 DP dielectric

The inorganic material in the Q 42 DP dielectric is based on a mixture of crystalizable glass and ceramic filler /19/. Fig. 5 shows the cross-section of a thick-film resistor (QM-93), fired on the top of the prefired dielectric layer. The microstructure of the dielectric is dense, with a few small, closed pores. The dielectric is densely sintered. The main elements, detected by EDS microanalysis in the dielectric, are Si, Al, Zn, Ba and Zr. A small amount of cobalt, presumably added for blue colouring, was also detected. The black grains imbedded in the dielectric matrix are alumina particles, added as the ceramic filler.

XRD analysis confirmed that the ceramic filler in the Q42-DP dielectric is alumina. The X-ray spectrum of Q42-DP is shown in Fig. 6. Al_2O_3 peaks are denoted "A". Peaks of another crystalline phase, presumably $SiZrO_4$ (JCPDS file 83-1383), are denoted by an asterisk.

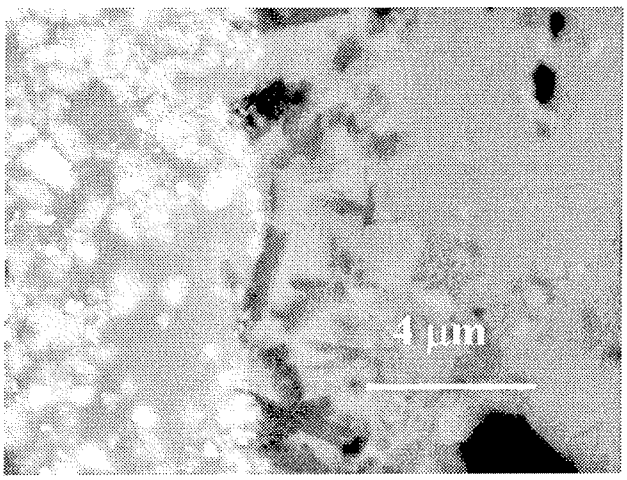

Fig.5: The microstructure of the interface between the resistor QM-93 and the Q42-DP dielectric. The dielectric is on the right.

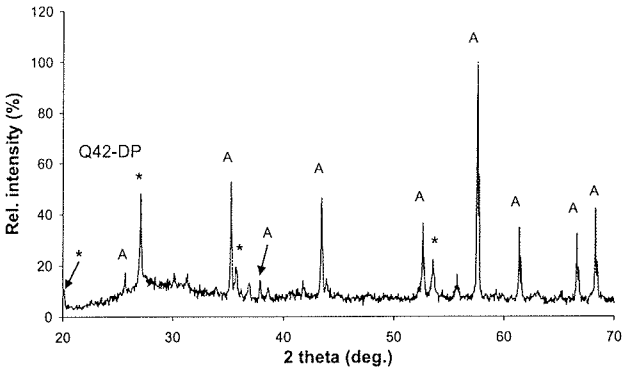

Fig. 6: X-ray spectrum of Q42-DP dielectric. Al_2O_3 and (presumably) $SiZrO_4$ peaks are denoted by "A" and by asterisk, respectively.

4.3. QM-80 and QM-90 resistors

As mentioned before, the Du Pont resistor series QM-80 and QM-90 are designed for firing on a prefired multilayer dielectric layer instead of on the surface of alumina substrates /19,21/. The resistors, made with QM 80 and QM 90 series, are intended for termination with palladium-silver and silver conductors, respectively. X-ray spectra of 1 and 10 kohm/sq. members of both series, fired at 850°C, are shown in Fig. 7.a (QM-83 and QM-93) and Fig. 7.b

(QM-84 and QM-94), respectively. The conductive phase in both 1 kohm/sq. resistors is a mixture of RuO_2 and ruthenate. For resistors with higher sheet resistivities, from 10 kohm/sq. up, only ruthenate was detected by X-ray analysis. Energy-dispersive X-ray quantitative analysis (EDX) indicated the presence of bismuth together with ruthenium. Therefore it is presumed that the ruthenate phase is $Bi_2Ru_2O_7$ or $(Bi_{1-x}Pb_x)RuO_{7-y}$.

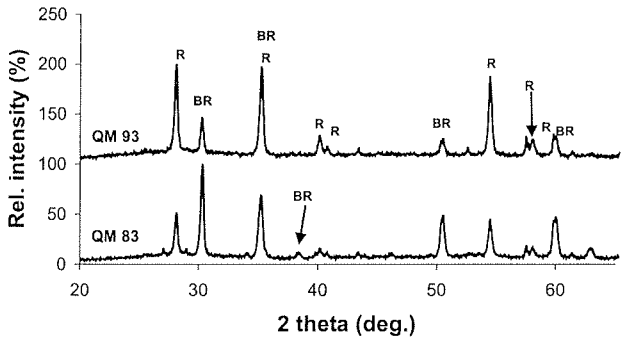

Fig. 7.a: X-ray spectra of 1 kohm/ sq. QM 83 and QM 93 resistors. RuO_2 is denoted R and ruthenate phase is denoted BR.

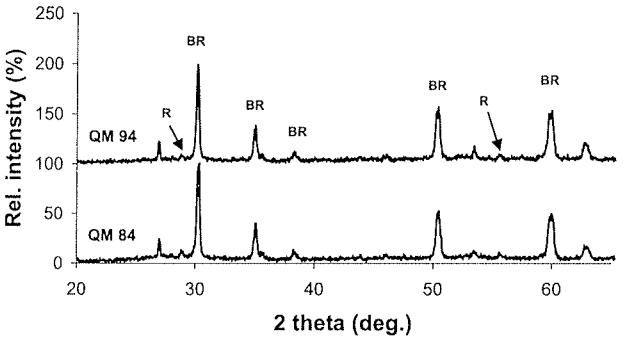

Fig. 7.b: X-ray spectra of 10 kohm/ sq. QM 83 and QM 93 resistors. Ruthenate phase is denoted BR.

Some of the measured electrical characteristics of QM-90 and QM-90 series resistors will be presented. A more complete evaluation of QM-90 resistors, fired also under a dielectric as buried resistive components within a multilayer structure, is reported in /23/.

Resistors were printed and fired on prefired QM-42 DP dielectric. QM-80 and QM-90 resistors were terminated with Pd/Ag-based QM-21 and Ag-based QM-14 conductors, respectively. Sheet resistivities as a function of temperature were measured. Cold (from -25°C to 25°C) and hot (from 25°C to 125°C) TCRs (temperature coefficient of resistivity) were calculated from resistivity measurements at - 25°C, 25°C and 125°C. Current noise was measured in dB on 100 mW loaded resistors by the Quan Tech method (Quan Tech Model 315-C). Gauge factors (GF) (the ratio of the relative change in resistance and the strain) were measured by the changes in resistivity as a function of substrate deformation with the simple device described in /24/. The results are presented un Table 1. TCRs of resistors, fired on the Q42 -DP dielectric, are, as stated by Du Pont, under $100x10^{-6}$/K. Noise indices and GFs increase with increasing sheet resistivity.

Table 1: Nominal sheet resistivities, cold (-25°C to 25°C) and hot (25°C to 125°C) TCRs, noise indices and gauge factors of the resistors

Resistor	Nominal sheet resistivity (ohm/sq.)	Cold TCR ($x10^{-6}$/K)	Hot TCR ($x10^{-6}$/K)	Noise (dB)	GF
QM-83	1 k	30	70	-18,3	4,5
QM-93	1 k	-55	-5	-21,2	4,0
QM-84	10 k	-5	50	-15,8	11,0
QM-94	10 k	20	75	-17,3	10,0
QM-85	100 k	30	75	-3,4	13,5
QM-95	100 k	35	75	-4,2	13,0

5. Diffusion patterning - experimental results

Based on the technical study and preliminary research /25/ the experimental work was designed to establish the necessary technological knowledge for the successful design and manufacture of multichip modules using diffusion-patterning technology. Two test patterns for the evaluation of diffusion-patterning materials and technology, presented in Figs. 8.a and 8.b, were designed. The first test pattern /26/ was intended for estimating the technological window (the dependence of vias and conductor lines' dimensions on, for example, drying temperature, washing out of the image paste, firing cycle etc.). The second test pattern /27/ was designed to evaluate the possibility of making differently shaped structures as well as specially designed thick-film resistors in a multilayer structure.

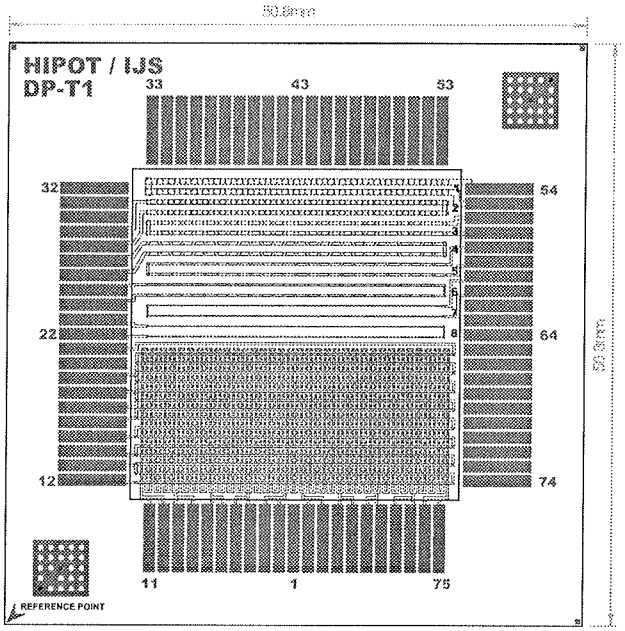

Fig. 8.a: Test pattern for estimation of the technological window of diffusion-patterning technology

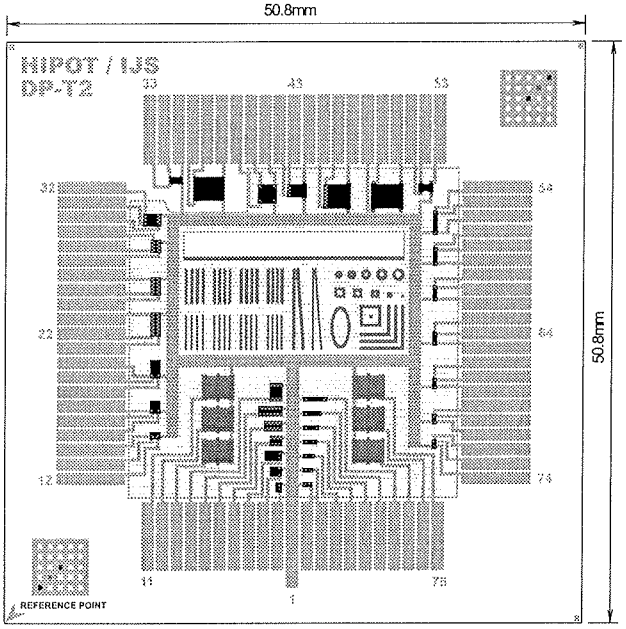

Fig. 8.b: Test pattern for evaluation of the possibility of making differently shaped structures and thick-film resistors in a multilayer structure

Visual and electrical inspection showed that the conductor lines going through vias with a diameter 150 μm or larger were continuous, while for smaller dimensions, conductors on part of the samples were open. Results obtained with the test circuit therefore showed that vias with 150 μm diameter or larger can be made while some of the 100 μm vias and nearly half of the 50 μm vias were closed. However, for high-volume production 200 μm is probably the lower limit. The vias with 50 μm, 100 μm and 150 μm diameter are shown in Fig. 9.

Via-dimension measuring shows that the diameter of the vias in the dielectric is in some cases up to 30% larger than the designed diameter. This can be attributed to the fact that the image paste diffuses not only vertically into the dielectric but also to some extent horizontally. The widening of the designed via dimensions should be taken into account when the multilayer circuit is designed. The results are summarised in Table 2. The ratio between the measered via diameters after firing and via diameters on photo mask are denoted in the Table 1 as the"D/PM increase".

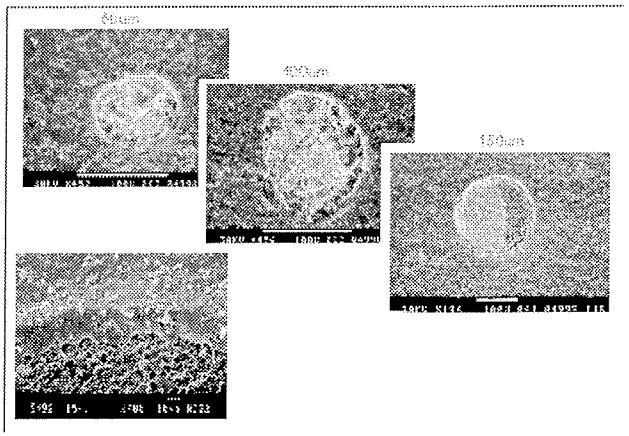

Fig. 9: Diffusion-patterning vias in the dielectric layer. The edge of a 200 μm via is shown in lower left corner.

Standard diffusing time is 10 min at 85°C. To estimate the influence of the time of diffusion at this temperature on the dimensions of vias and lines, the diffusion time was varied for some samples from 5 to 20 minutes. Visual inspection showed that the diameter of the vias, which were already open after 5 minutes, is practically independent of the diffusion time. The width of lines increased with increasing time of diffusion by nearly 50% after 20 minutes. This effect was more pronounced for wider lines.

6. Diffusion patterning - A pressure sensor

In the case of a typical pressure sensor construction before miniaturisation the sensor element (gauge silicon piezoresistive pressure sensor) is integrated on a thick-film substrate with conditioning electronics on the periphery. Electronic conditioning circuit with conventional electronic components is shown in Fig. 10.a. The sensor in is designed for measuring absolute pressure in the range of 1 bar and has 0,5V to 4,5V output voltage with 5V supply voltage.

The common electronic conditioning circuit for pressure sensor applications needs an excitation voltage or current, instrumentation amplifier, voltage reference and an output stage. Before miniaturisation the conditioning electronics

Table 2: Dimension of vias from design to realisation

	Via diameter (μm)							
Layout	500	400	300	250	200	150	100	50
Photo-Mask	540	440	340	290	240	190	140	90
Screen-Mask	550	450	350	300	250	210	150	100
Dielectric	620	550	430	380	300	250	150	
D/PM increase	115%	125%	126%	131%	125%	132%	107%	/

were realised with conventional electronic components in SMD form. To attain the object of miniaturisation a semi-custom ASIC for signal processing AM401 (Analog Microelectronics) was used as an equivalent electronic conditioning circuit. The AM401 is a low-cost monolithic voltage transmitter, designed for flexible bridge input signal conditioning. It contains a high-accuracy instrumentation amplifier for differential input signals, an operational amplifier output stage, and an adjustable voltage reference (5V or 10V). In addition to these functional elements an auxiliary operational amplifier can be used as a current or voltage source. Output range and gain are adjustable over a wide range by external resistors.

Electronic design with ASIC AM401 completely replaces conventional electronics, except for a few passive components. These resistors and capacitors are still needed for temperature compensation of the silicon sensor element, calibration (offset voltage, output range, gain) of the complete sensor and stabilisation of the reference voltage and the first-stage voltage. This means that the passive sensor part is the same, only the amplifier is simplified. The important factor for miniaturisation and lower price is the use of active trimming of thick-film resistors to avoid the discrete trimmer potentiometers for all functional adjustments. Fewer electronic components mean less area required for the complete circuit and proportionally a lower price. The circuit with AM401 has some disadvantages too. For example, the supply voltage should be at least 5V above the maximum output voltage. This means that when using AM401, sensors lose their advantage of low supply voltage.

The new, miniaturised pressure sensor was designed for measuring relative pressure in the range of 1 bar and has 0,5V to 4,5V output voltage with a 12V supply. The pressure sensor was realised with a semi-custom ASIC AM401 for signal processing, silicon piezoresistive pressure sensor SM-21 as a sensing element, and 11 passive components for parameter adjustment and ASIC periphery. The electronic circuit schematic diagram is shown in Figure 10.b.

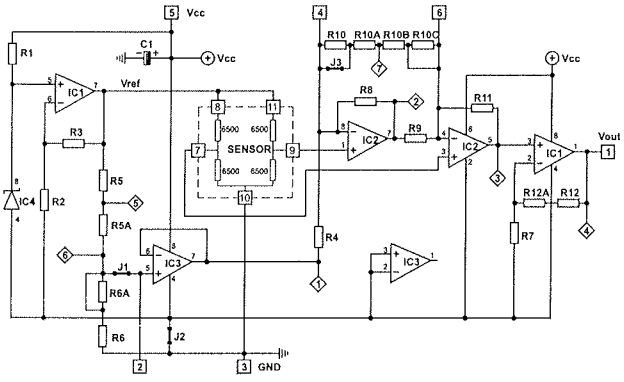

Fig. 10.a: Electronic conditioning circuit with conventional electronic components

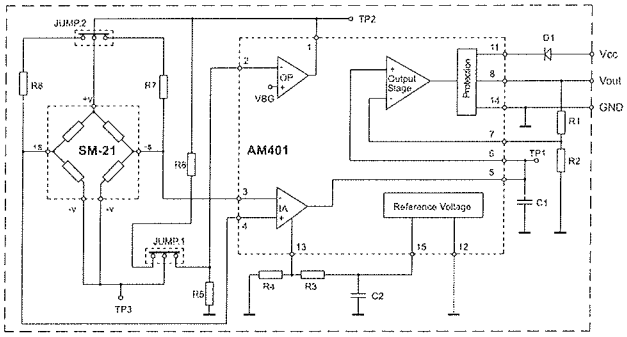

Fig. 10.b: Electronic conditioning circuit with analog ASIC

A thick-film multilayer MCM-C with four conductive layers was designed and produced with diffusion patterning technology. The substrate for the pressure sensor is Al_2O_3 ceramic with dimensions 3.5 mm × 18.0 mm × 0.64 mm. In the ceramic there are four holes, one 1.4 mm square hole for applying the measuring pressure, and three holes (0.2 mm diameter) for electrical interconnection with a through-hole printing technology. The thick-film multilayer interconnection consists of four conductive layers (one on the rear side), two dielectric layers, 38 interconnections between conductive layers, and two overglaze layers. The top conductive layer integrates also 19 gold bonding pads, eight laser trimmed thick-film resistors, three bare dies bonded with aluminium wires, two jumpers, and three terminal pads. On the rear side two multilayer chip capacitors are soldered. The layout and cross-section of pressure sensor are shown in Figure 11. The volume reduction from the conventional thick-film pressure-sensor module to the same module, realised as a MCM-C, is around 20x.

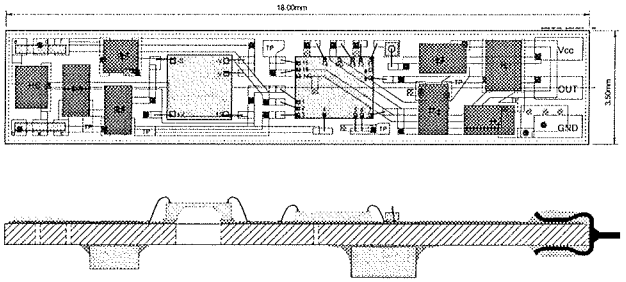

Fig. 11: The layout and cross-section of pressure sensor realised in diffusion patterning technology

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INTRODUCTION TO SENSORS

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POSVET O SENZORJIH V ZAVODU ITC SEMTO
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Key words: sensors, actuators, MEMS, micromachining, sensor parameters, transduction principles, smart sensors

Abstract: An overview of basic definitions and properties related to sensors is given. Key sensor classifications and definitions of some relevant sensor properties such as transfer function, sensitivity, accuracy, resolution, selectivity, noise, nonlinearity and other are emphasized. Some recent applications based on silicon standard and micromachining technology available in Laboratory of Microsensor Structures (LMS) are presented, such as research and development of silicon devices, sensors and microelectromechanical systems (MEMS) as well as integration of sensors and electronics resulting in smart sensor solutions.

Osnovne značilnosti senzorjev

Ključne besede: senzor, aktuator, MEMS, mikroobdelava, parametri, principi pretvorbe, inteligentni senzor

Izvleček: Uvodoma bodo predstavljene nekatere osnovne definicije s področja senzorjev in pomembnejši ključi razdelitve senzorskih družin. Podrobneje bodo razložene izbrane senzorske lastnosti kot so npr. prenosna funkcija, občutljivost, točnost, ločljivost, selektivnost, šum, nelinearnost in drugo. Shematsko bo predstavljen tudi princip zajemanja podatkov na osebnem računalniku. V nadaljevanju prispevka bo predstavljena raziskovalno - razvojna dejavnost na področju mikrosenzorskih struktur v LMS. Poudarek bo na predstavitvi postopkov mikroobdelave in aplikacijah, ki so bile v Laboratoriju zasnovane. Na koncu bomo podali pregled lastnosti inteligentnih senzorjev, ki predstavljajo eno izmed glavnih smernic razvoja modernih senzorskih struktur.

I. INTRODUCTION

Sensor applications today are wide spread and constantly growing, mainly due to the increasing amount of data which is acquired from environment. The data is mainly intended for further computer processing. This giant stride of sensor applications is expected to be continuous at least for five more years and at least proportional to the technological development. Future development will be concentrated in the field of three dimensional (3D) microsensor structures, based on classical microelectronic processes and up-to-date micromachining processes. The preferences for microelectronic approach are evident from the well-known story of integrated microelectronic circuits. Therefore, modern sensors main benefits are: price, quality, mature technologies, miniaturization and compatibility with existing integrated circuits design processes, which leads to integrated sensor designs with smart sensor features that represent today's absolute peak of sensor technology.

II. BASIC TERMS

In this section some basic terms will be discussed which are commonly used in practice, nevertheless their exact definition is often not so evident.

SENSOR: Sensor is defined as a (electronic) device which produces an (electrical) output signal in explicit relation to the value of sensed quantity on its input.

Example: Pressure sensor

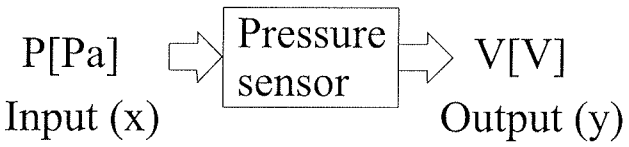


Figure 1: Pressure sensor.

Remarque: Beside original term "sensor", there are also other common names in use for sensor devices such as detector (e.g. photo-detector), meter (e.g. thermo-meter), element (e.g. thermo-element) etc.

ACTUATOR: Actuator is often defined as a (electronic) device which produces an output in the form of mechanic or information signal, which is in explicit relation to the value of (electrical) quantity on its input.

TRANSDUCER: Transducer is often defined as a common name for both sensors and actuators.

III. OVERVIEW OF SENSING PRINCIPLES

Operation of a sensor is always based on a transduction of sensor input signal energy into sensor output signal energy. This transduction, performed in sensor, is one of the basic natural phenomena. Today there are over 350 known types of transduction between various forms of energy, and their number is still increasing. Based on this variety of transduction principles, many types of sensors can be realised.

Example: Photosensor transduces input light energy into output electrical signal energy, based on the principle of photoeffect which is performed inside photosensing element.

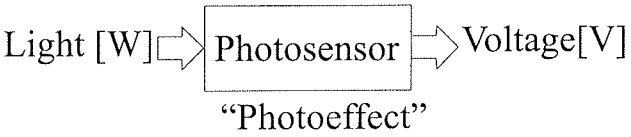


Figure 2: Transduction in photosensor.

Remarque: The term transduction is sometimes replaced by well-known synonyms such as effect, law etc.

Transduction principles are usually classified by the type of input energy. Based on this criterion, sensors are sometimes classified as mechanical, temperature, electrical, magnetic, irradiation, chemical, biological etc.

IV. OVERVIEW OF SENSOR CLASSIFICATIONS

Various sensor classifications are met in the literature, each one having its unique advantages. Brief overviews of some standard sensor classifications are given in Tables 1 - 7. Classification by the conversion phenomena is commonly used for educational purposes, since it emphasizes a conversion principle for various sensor applications. Classification by the output quantity is appropriate for systems designers who need to use sensor output in a particular project. Classifications by the type of input stimulus, price or field of use serve mainly to the end user. Classifications by fabrication technology or sensor material are appropriate for manufacturers.

	Thermoelectric		Chemical transformation		Biochemical transformation
	Photoelectric		Physical transformation		Physical transformation
	Photomagnetic		Electrochemical process		Effect on test organism
	Magnetoelectric		Spectroscopy		Spectroscopy
Physical	Electromagnetic	**Chemical**	Other	**Biological**	Other
	Thermoelastic				
	Electroelastic				
	Thermomagnetic				
	Thermooptic				
	Photoelastic				
	Other				

Table 1: Sensor classification by the conversion phenomena

Resistance	Capacitance	Inductivity	Voltage	Current	Other

Table 2: Sensor classification by the output quantity

Acoustic	Wave amplitude, phase spectrum, wave velocity, other
Biological	Biomass, other
Chemical	Components, other
Electric	Charge, current, potential, voltage, electric field, conductivity, permitivity, other
Magnetic	Magnetic field, conductivity, permitivity, other
Optical	Wave amplitude, phase spectrum, wave velocity, refractive index, emmisivity, reflectivity, other
Mechanical	Position, acceleration, force, stress, pressure, strain, mass, density, moment, shape, stiffness, viscosity, other
Radiation	Type, energy, intensity, other
Thermal	Temperature, flux, specific heat, thermal conductivity, other.

Table 3: Sensor classification by the type of stimulus (input quantity)

Thick film, thin film, bipolar, unipolar, micromachined, other
Semiconductor/silicon, metallic, insulator, ceramic, biological, (in)organic, solid, liquid, gas, other

Table 4: Sensor classification by the fabrication technology and by sensor material

Agriculture	Automotive
Civil engineering	Space
Distribution	Domestic
Energy, power	Environment
Medicine	Information
Military	Marine
Scientific measurement	Other

Table 5: Sensor classification by the field of application

biological	radioactivity and radiation
chemical	heat and temperature
electric, magnetic or electromagnetic	mechanical

Table 6: Sensor classification by the detection means

sensitivity	stimulus range (span)
stability (long and short term)	resolution
accuracy	selectivity
speed of response	environmental conditions
overload characteristics	linearity
hysteresis	dead band
operating life	output format
cost, size, weight	other

Table 7: Sensor classification by some special specification

V. BASIC SENSOR CHARACTERISTICS AND PARAMETERS

In this section some significant sensor definitions, properties and parameters will be reviewed /1/. In the definition of sensor characteristics we will refer to sensor as a "black box" with its stimulus input *x* (i.e. measured input quantity) and (electrical) sensor response (output quantity) *y* (Fig. 3).

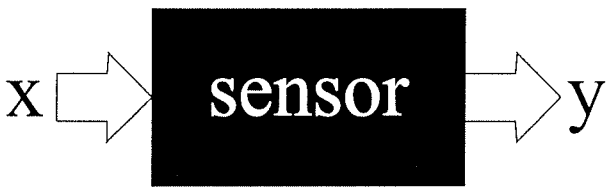


Figure 3: General presentation of a sensor.

Transfer function: is the relationship between input *x* and output *y* of a sensor. This function establishes dependence between the electrical signal *y* and stimulus *x*. (Fig. 4)

$$y = y(x) \tag{5.1}$$

Input stimulus *x* range is from x_{min} to x_{max}, output electrical signal *y* range is from y_{min} to y_{max}.

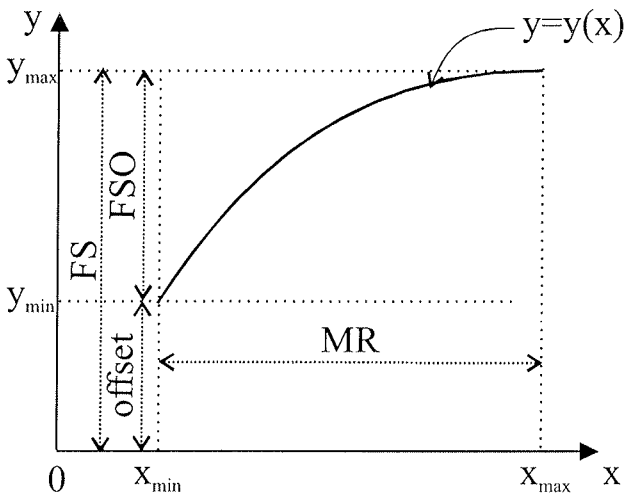


Figure 4: Transfer function of a sensor.

Measured Range (MR), also **Span:** is a dynamic range of stimuli which can be applied to a sensor.

$$MR = x_{max} - x_{min} \tag{5.2}$$

Full Scale (FS): is maximal range for sensor output quantity, given by y_{max}

Full scale output (FSO): is the difference between the electrical output signals y_{max} and y_{min}, measured at minimum applied stimulus x_{min}

$$FSO = y_{max} - y_{min} \tag{5.3}$$

Sensitivity S: is the ratio of the change of sensor output Δy and a according small input stimulus variation Δx (Fig. 5). Therefore sensitivity *S* can be mathematically expressed as a first order derivative of the output *y* to stimulus *x*

$$S(x) = \left.\frac{dy(x)}{dx}\right|_x \tag{5.4}$$

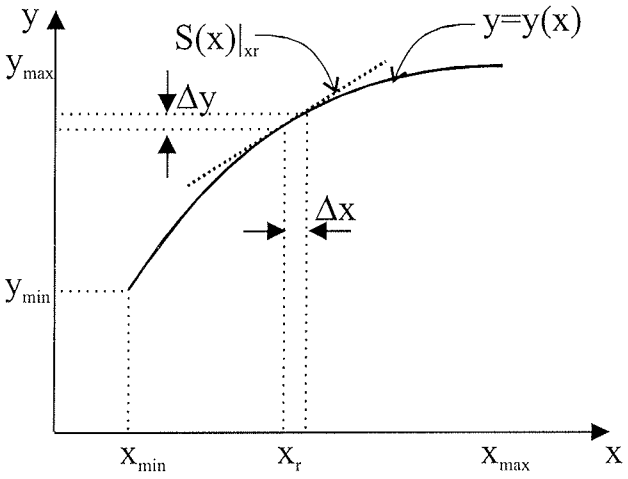
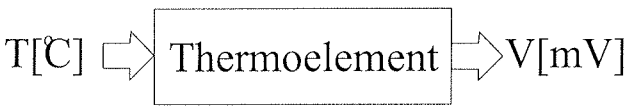


Figure 5: Sensitivity.

Example: Thermoelement sensitivity



$$S = \frac{dV(x)}{dT}\left[\frac{mV}{^{o}C}\right]$$

Offset y_{min}: is the value of transfer function *y(x)* at minimum stimulus x_{min}

$$y_{min} = y(x)\big|_{x=x_{min}} \tag{5.5}$$

Accuracy ε: is the difference between the value of measured input stimulus x_m, obtained from sensor transfer function y_m and the true value x_t of the same stimulus, obtained from high accuracy reference sensor (Fig. 6). Accuracy is usually normalized to the measured range *MR* and then expressed in percent.

$$\varepsilon\ [\%] = \frac{x_m - x_t}{MR} \cdot 100 \tag{5.6}$$

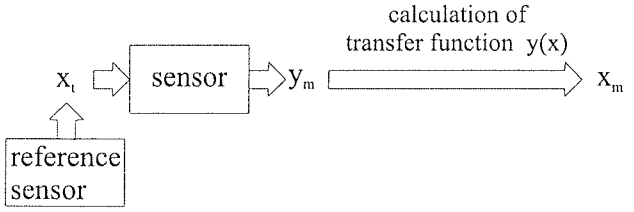


Figure 6: Accuracy determination.

In modern sensor design, accuracy is being replaced by much wider term *uncertainty*, which combines systematic and random errors (see below).

Resolution R: is the smallest change in input stimulus Δx_{min}, which already produces a measurable change in output Δy_{min}. Resolution is often normalized by *MR* and then given in percent.

$$R[\%] = \frac{\Delta x_{min}}{x_{max} - x_{min}} 100 \tag{5.7}$$

Selectivity S_α: is defined as sensitivity of a sensor to the variations of different unwanted input environment parameters x_α such as temperature, humidity, light etc.

$$S_\alpha = \frac{\Delta y}{\Delta x_\alpha} \tag{5.8}$$

Obviously, an ideal sensor has selectivity $S_a = 0$!

Remarque: Other names for selectivity are also drift, instability, cross sensitivity etc.

Noise N: is the RMS (root - mean - square) value of the sensor output signal, measured at minimal stimulus x_{min} on sensor input.

Minimal Detected Signal MDS: is the minimal value of the input stimulus x_{min}, which yields an output response equal to the noise level (S/N ratio=1). Therefore input values below *MDS* cannot be distinguished from noise, and are hencefore not measurable!

Nonlinearity NL: is the deviation of a real transfer function from the ideal linear response (y_{NL}, Fig. 7). There are several ways how to specify nonlinearity, depending on how the approximating ideal linear line is superimposed to the transfer function. Approximating line can be drawn through minimal and maximal characteristics points (terminal points line). Another best-fit line can be obtained by drawing a parallel line through the terminal points and then choosing a best-fit line at the midway of those two lines. The nonlinearity is then calculated as a maximum deviation from the midway line. The type of approximation used dictates a value calculation algorithm, which is performed by signal processing electronics in smart sensors. With prevalent use of microprocessors one can implement more complex value calculation algorithms such as least squares fit which minimizes the square area between approximating line and the transfer function.

Hysteresis H: is the deviation Δy_{HYST} of a sensor when the entire measurement range is scanned in the direction from x_{min} towards x_{max} and opposite (Fig. 8).

Repeatability Rep: is the deviation Δy_{Rep} of the sensor outputs when the entire measurement range is scanned repeatedly in the direction from x_{min} towards x_{max}. So repeatability is similar to hysteresis, only the measurement range is scanned in the same direction (Fig. 9).

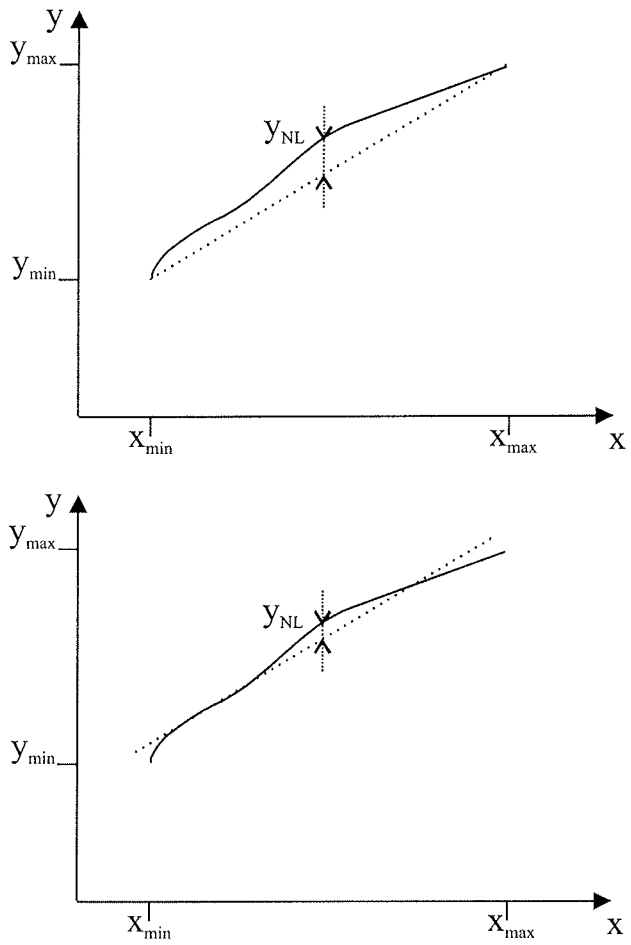


Figure 7: Nonlinearity calculation methods.

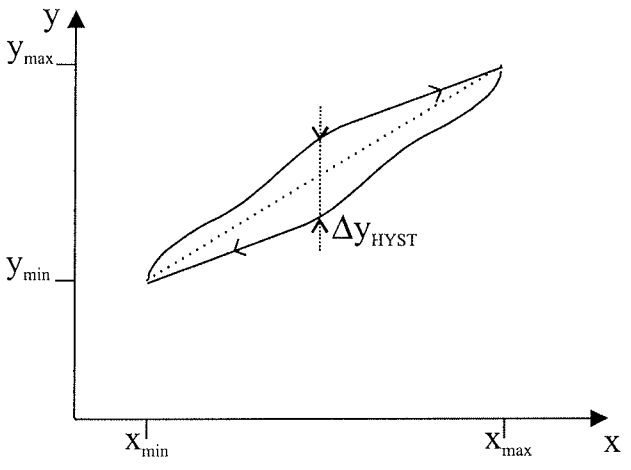


Figure 8: Hysteresis.

Temperature zero drift or **error**, also **offset drift:** is the change of sensors output y_{min}, when the temperature range is scanned from T_{min} to T_{max} with minimum stimulus x_{min} at the input (Fig. 10). Similarly, temperature drift error is sometimes measured at maximum stimulus applied.

Overrange (also **overload) characteristics:** is the maximum permissible limit of the input stimulus, which can be

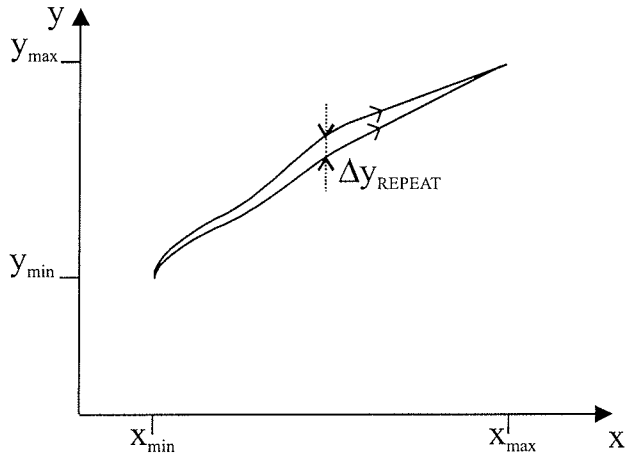


Figure 9: Repeatability.

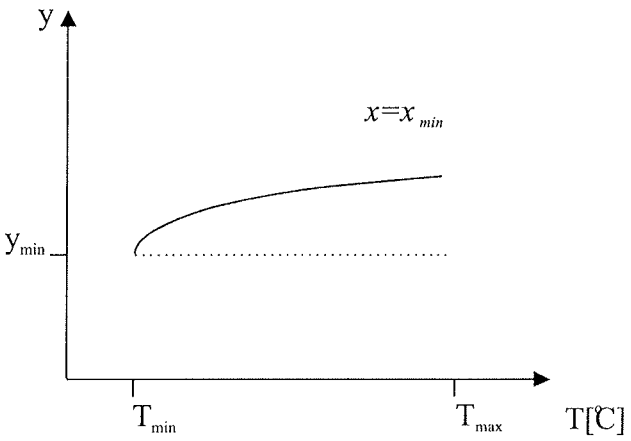


Figure 10: Temperature zero error.

applied to a sensor for a certain period without causing permanent degradation of sensors characteristic.

Recovery time: is the time required for a sensor to regain specified characteristics after being exposed to overload.

Response time: is the time required by a sensor output to reach 90% of the final steady- state response value upon exposure to a step stimulus.

Long-term stability: is given as the maximum deviation in sensor response Δy_{STAB} after longterm operation at constant specified operating conditions (Fig. 11).

Uncertainty: is obtained from an error estimation procedure which considers statistical error sources and error sources that can be determined by measurement or other means. Statistical errors are described by standard deviation s_i and variance u_i. Standard uncertainty (u_i=s_i) represents each component that contributes to the measurement result. Other types of errors can be obtained from previously acquired set of measurements, calibration reports etc. Both sources are associated in combined standard uncertainty by means of RSS method (Root of the Sum of the Squares):

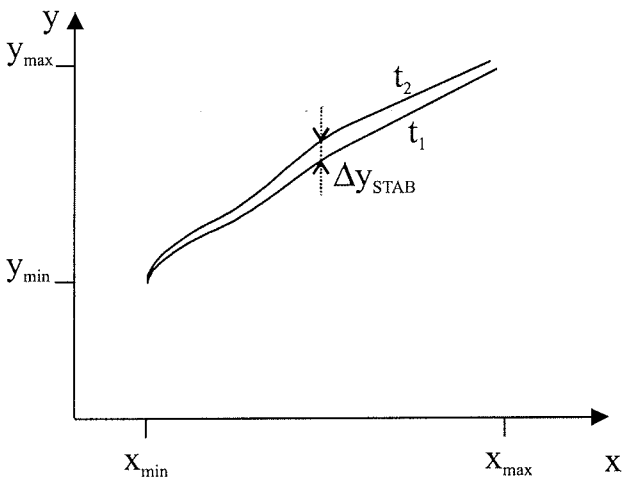


Figure 11: Long-term stability.

$$u_c = \sqrt{u_1^2 + u_2^2 + u_3^2 + ... + u_n^2} \qquad (5.9)$$

VI. SENSOR TECHNOLOGIES

Technologies which are prevalent in modern microsensor structures design and fabrication are commonly divided into two major categories:

1. *Classic microelectronic technologies*, which incorporate standard integrated circuit process technologies such as thick and thin - film technologies and semiconductor technologies (diffusion, implantation, oxidation, photolithography, metal and dielectric layer deposition ...)
2. *Micromachining* is a collective name for a group of modern processes which are devoted to fabrication of 3D microstructures. Some more important micromachining processes are:
   - Etching (dry, wet; isotropic, anisotropic)
   - Laser micromachining
   - EDM (Electro Discharge Machining)
   - Sacrificial film processing
   - Film lift-off method
   - LIGA (Lithographie-Galvanoformung-Abformung)
   - Hole sealing
   - Wafer bonding etc.

Silicon has prevailed as the fundamental material for microelectromechanical systems (MEMS) fabrication due to its excellent electrical, optical and mechanical properties such as:

- Mature and well known microelectronic technology
- Excellent electrical properties (doping, semiconductor properties...)
- Excellent optical properties (photoelectric and photovoltaic effect ...)
- Excellent chemical properties (isotropic, anisotropic etching ...)
- Excellent mechanical properties (Young modulus is comparable to stainless steel, without practically any plastic deformation - devices operate or break)
- Other interesting features (piezoelectricity, piezoresistivity, Hall and Seebeck effect ...)

VII. SIGNAL CONDITIONING

Digital signal conditioning is crucial for a good sensor application. In this section we give a brief review of basic electronics involved.

A typical sensor system with basic building blocks for signal conditioning is shown in Fig. 12. As an example, output signal from temperature sensor is a small voltage in the range of milivolts. This signal is amplified by a high input impedance amplifier, such as instrumentation amplifier. Signal from the amplifier is led to a low pass filter, which removes unwanted high frequency components in sensor signal. Low frequency spectrum of a signal is then presented to the sample & hold circuit for signal discretization. The digital result from A/D converter is then further elaborated, often by a personal computer. In modern sensor systems the signal conditioning circuit is normally integrated with sensor. This arrangement is referred to as "system on chip" (SOC) or "microsystem" (MS) /4/.

VIII. SENSOR ACTIVITIES AND APPLICATIONS IN LMS

Activities in Laboratory of Microsensor Structures at the Faculty of Electrical Engineering, University of Ljubljana consist of basic research in the field of micromachining

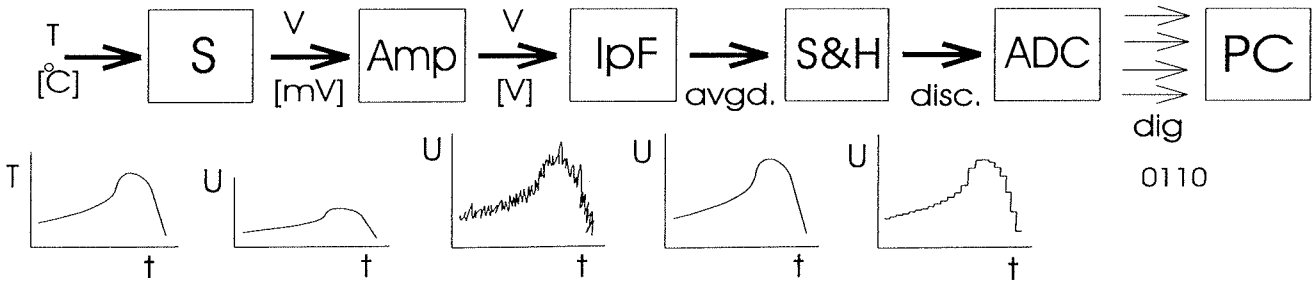


Figure 12: Typical sensor system with basic building blocks for signal conditioning.

and development of different advanced sensor and actuator 3D microstructures and devices. In this section we present a short survey of some results and developed devices.

An/isotropic etching of silicon:

Anisotropic properties of silicon are of utmost importance in micromachining by wet anisotropic etchants such as KOH, EDP, TMAH and others (Fig. 13). These etchants etch different crystal planes by distinct etch rates, which are significantly influenced by etchant concentration, etch bath temperature. Both parameters also strongly influence surface quality of microstructures.

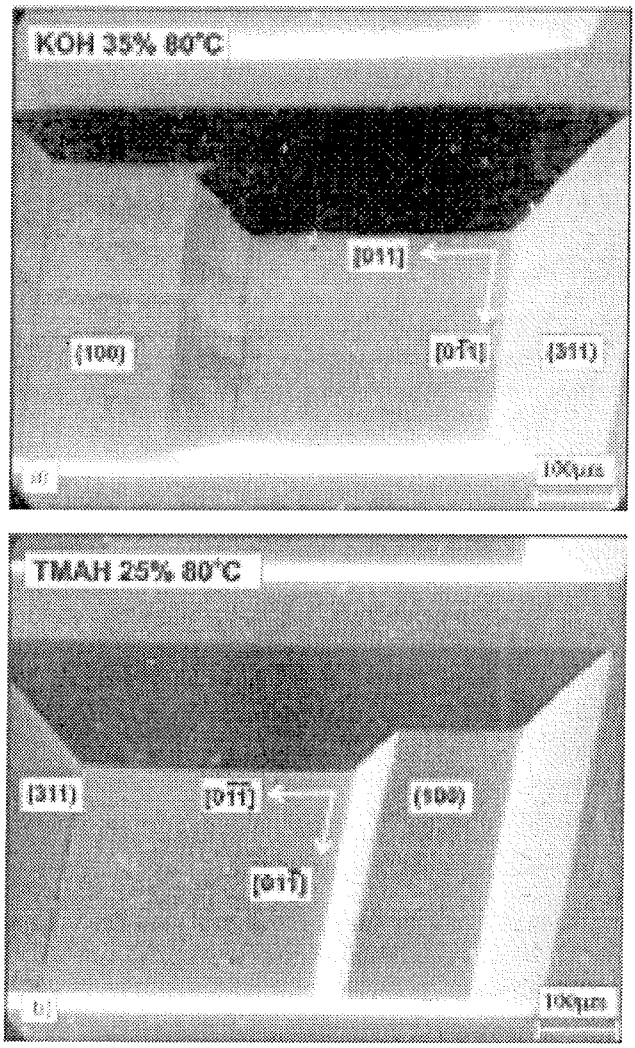


Figure 13: Anisotropic etching of silicon.

Study of compensation structures:

In wet micromachining of silicon microstructures fast etching of high-index crystal planes occur at convex corners. By utilizing different shapes and/or size of compensation structures this effect can be mitigated to a great extend (Fig. 14).

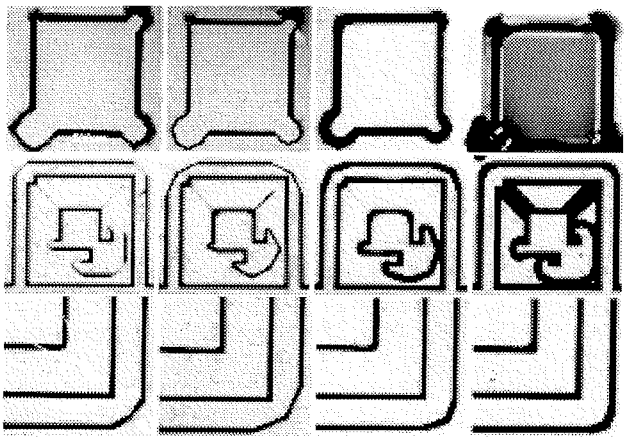


Figure 14: Convex corner compensation technique.

Compensation of convex corners in realization of 3D structures /bossed diaphragms/

In case of bossed diaphragm /5/, used in low-pressure measurement devices, there is a need for proper design of compensation structures that will occupy small footprint and effectively compensate convex corner undercutting to depths beyond 300μm. Various approaches have been studied (Fig. 15).

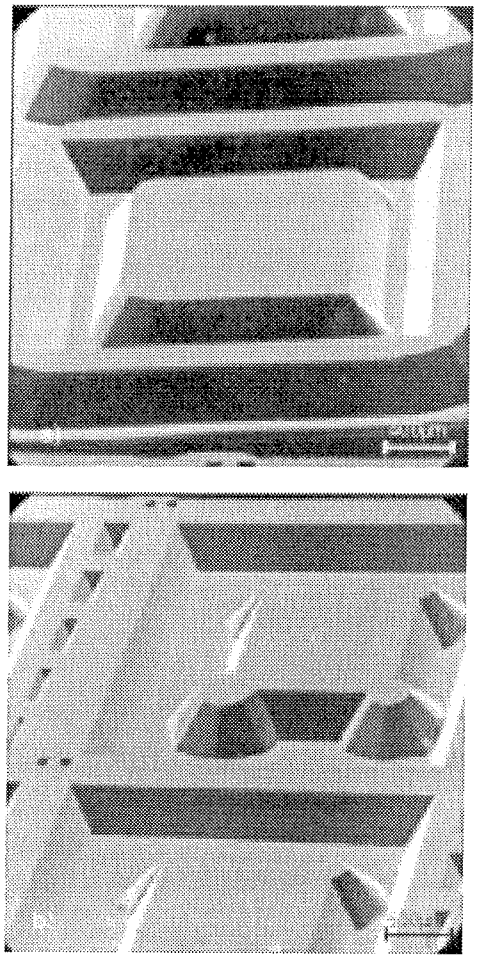


Figure 15: Compensation of convex corners in realization of bossed diaphragms.

Identification of silicon crystal planes:

Recognizing various crystal planes in silicon micromachining is of great importance, because of etch rate dependency (anisotropy). This enables proper microstructure lateral mask design and predictive final shape and size of the microstructure (Fig. 16). Most often, <100> crystal oriented silicon wafers are used, with known orientations of relevant crystal planes.

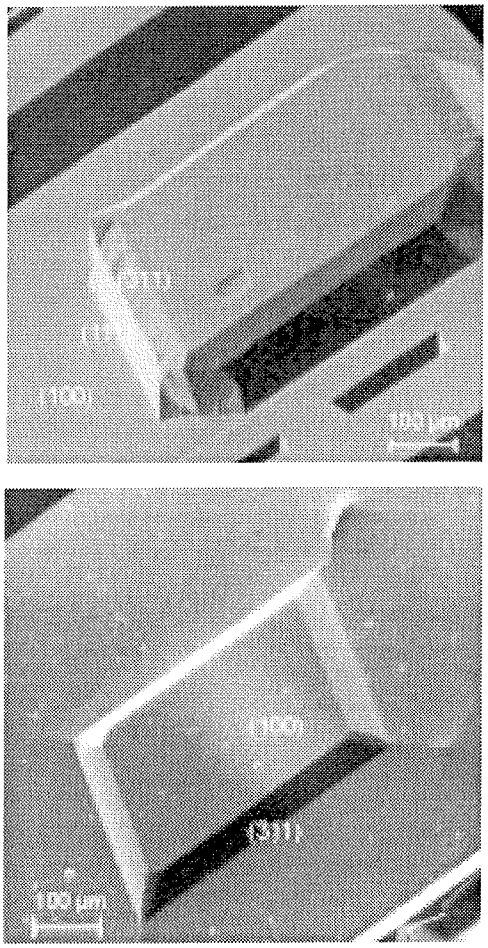


Figure 16: Identification of silicon crystal planes.

Silicon micromachining of microtips for AFM (Atomic Force Microscopy) and FED (Field Emission Displays)

By aid of an/isotropic etching (wet or dry) it is possible to perform very precise etching of silicon micropyramides or cones with apex radius bellow 20nm (Fig. 17). These microtips are successfully used for research and investigating the material physical surface properties in AFM. When fabricated as an array and electrically connected they act as point sources of electrons for light generation, thus realizing an optical display (FED).

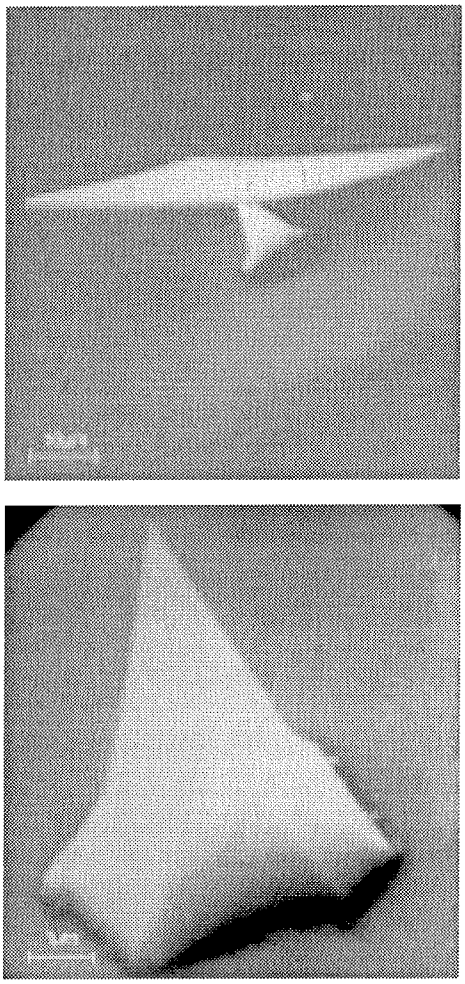


Figure 17: Silicon micromachining of microtips.

Piezoresistive pressure sensor:

In this microstructure /6/ four resistors are diffused on the membrane and connected into the Wheatstone bridge for temperature compensation (Fig. 18). Besides, there are additional resistors diffused outside membrane region, which is important for compensation in smart sensors for accurate pressure measurements.

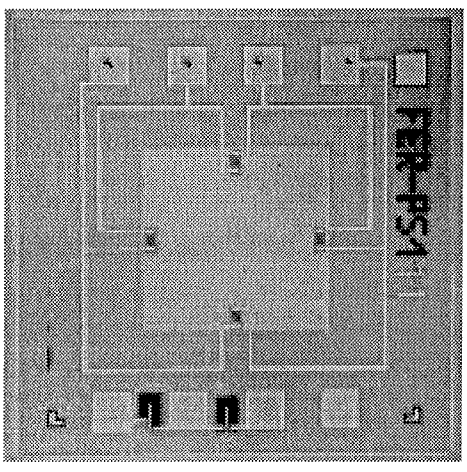


Figure 18: Piezoresistive pressure sensor.

Silicon photosensor: Phototransistor

In LMS designed and fabricated silicon phototransistor is dedicated to specific application requiring fast response and switching times. Besides, it allows high amplification of incident light signal (Fig. 19).

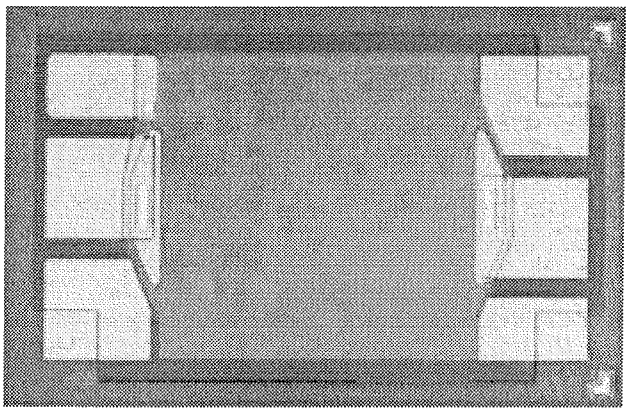


Figure 19: Silicon phototransistor (size 0.9 x 0.6mm^2).

Silicon radiation sensor: microstrip detector

In LMS designed and realized detectors /7/ with on-edge irradiation approach have high sensitivity and high space resolution, appropriate for tissue examination in the mammography and similar (Fig. 20).

Smart pressure sensor

LMS designed in cooperation with HIPOT-HYB a smart pressure sensor with digital temperature compensation and in - system calibration (Fig. 21).

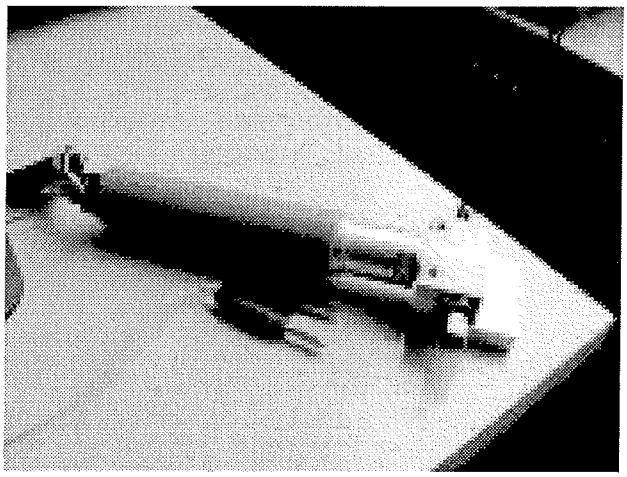


Figure 21: Smart pressure sensor prototype.

SMART SENSORS IN LMS

Smart sensors represent today's peak in sensor applications. In this section we present the essential properties of smart sensors in LMS /8/ and their characteristics during operation and calibration. Using a modern design microcontroller it is possible to implement a smart sensor in a single chip design, however modular smart sensor designs are preferable, since their implementations are more adaptable to end user. Operation of a smart sensor is similar to the operation of a normal sensor. The essence of its intelligence is due to the fact that it incorporates all necessary information in digital description for further use by a remote sensor controller. Smart sensor can be adapted on-site for end user application specific features and can be calibrated on site.

Smart sensor comprises several measurement channels: smart pressure sensor, which was implemented in LMS,

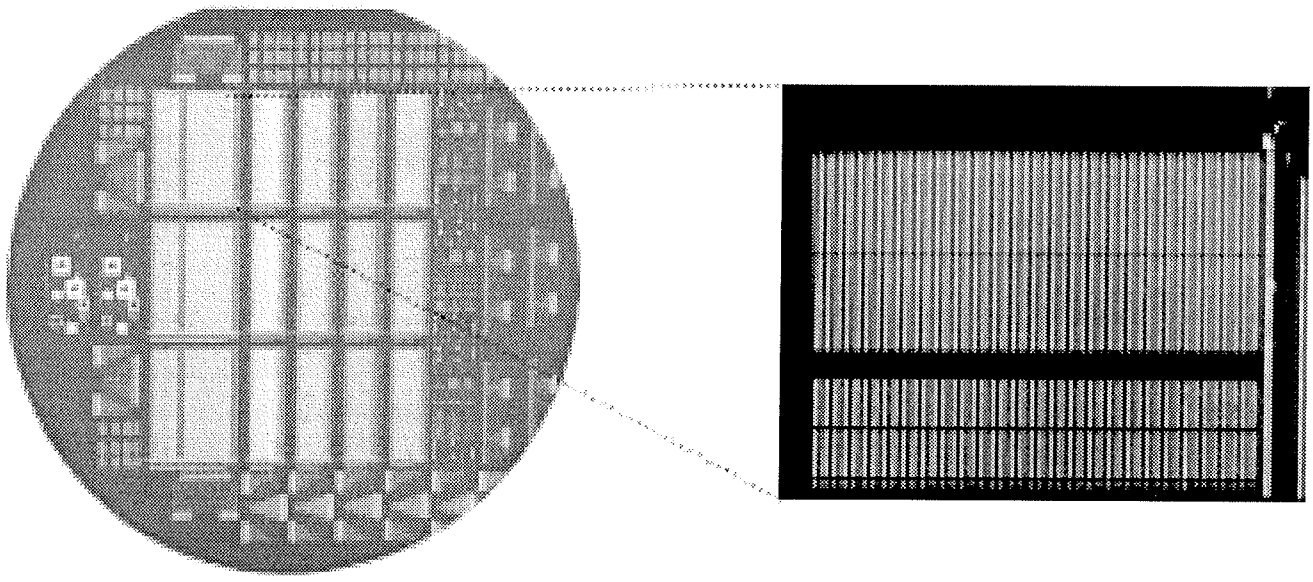


Figure 20: Microstrip detectors on a silicon wafer with a detail (right).

features pressure, temperature and two auxiliary actuator measurement channels. Each measurement channel as well as the smart sensor itself have a dedicated digital description of measurement properties - the TEDS (Transducer Electronic Data Sheet). The TEDS is available to be read and partially written by sensor controller. Smart sensors also feature virtual measurement channels, which gather information from several physical channels.

Additional preference of smart sensors is a standardized algorithm for calculating the raw sampled A/D data into measured pressure value. The scope of value calculation algorithm is very wide. Its conversion methods range from a simple look-up table to multivariate polynomial spline approximation, which can combine results from several measurement channels, resulting in multidimensional sensor compensation. Measured value of a smart sensor is presented strictly in SI units, which can be arbitrarily defined during calibration. Each measurement channel features a combined standard uncertainty. The control and status of a smart sensor can be achieved by a set of dedicated registers, organized hierarchically from individual measurement channel to general control and status. Error reporting is achieved by a unique system of interrupts, which can also be masked to prevent interrupts of known conditions. The smart pressure sensor, which was implemented by LMS and HIPOT-HYB, in excess of standard features, uses a special calibration algorithm, which minimizes the offset voltage impact and compensates temperature dependencies. The starting point of calibration is a raw pressure sensor without any offset or temperature compensation! The calibration procedure also eliminates sensor nonlinearity. Full-scale pressure is totally adaptable to the user needs.

Smart sensors will definitely change the relevance of standard sensor properties, described in section V. Nonlinearity, accuracy, sensitivity variation and selectivity will slowly recede into the background, while noise, resolution, hysteresis and repeatability will rapidly gain on significance.

CONCLUSION

A brief introduction to the elementary characteristics of a vast sensor domain has been given. Sensor terms and definitions were presented and described. An up-to-date sensor classification has been summarized. An overview of some sensor and micromachining technologies, which are implemented by LMS, has been presented. At the end a brief introduction to smart sensors has been given.

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ELEKTRONIKA NA POTI OD DETEKTORJA DO OSREDNJEGA DELA SISTEMA

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POSVET O SENZORJIH V ZAVODU ITC SEMTO
15.03.2002, FE Ljubljana

Ključne besede: detektor, elektronika, senzorski sistem, ojačevalnik, motilni signal, tokovna zanka

Izvleček: Senzorski sistem smo razčlenili na elektronska vezja, ki jih srečamo na poti od detektorja do osrednjega dela. Opredelili smo najpomembnejše osnovne gradnike in izvedbe ojačevalnikov ter opisali način in realizacijo odjema upornosti, napetosti, toka in naboja. Podali smo zgled delovanja optoelektronskega detektorskega polja. Pri prenosu signalov smo se posvetili zmanjševanju vpliva motilnih signalov s tokovno zanko.

Electronics on the Way From a Detector to the Central System Unit

Key words: detector, electronics, sensor system, amplifier, disturbant signal, current loop

Abstract: Sensor system is divided into electronic circuits, which are present on the way from a detector to a central sensor system unit (Fig. 1). In an input stage the transduced physical quantity is amplified within a pre-amplifier. A middle stage serves for further amplification and linear transformations of the electrical signals may occur on the way to the central unit; however, with high insensitivity to the disturbances and minimized drift. In the central unit the analog electrical signal is converted into the digital signal.

Basic types of amplifiers are presented (Fig. 2). Apart from an operational amplifier and its derivative called instrumentation operational amplifier, which amplify the difference of input voltage into an output voltage, an operational transconductance amplifier and an operational transresistance amplifier are introduced and their properties discussed. Utilization of negative feedback leads to stable amplifier stages (Fig. 4 gives examples for the operational amplifier).

Conversion of resistivity into an output voltage signal is demonstrated in two versions: (i) classical bridge configuration followed by a differential amplifier and (ii) active bridge configuration (Fig.5). Conversion of (open-circuit) voltage or (short-circuit) current into a voltage output signal is discussed using a photodiode as a detector of illumination intensity (Fig. 6).

Working principle of charge-to-voltage conversion requires at least two electronic switches (Fig. 7). The concept of optoelectronic detector array (Fig. 8) with common addressing of pixels in each address line and multiplexing of output voltages from charge-to-voltage amplifiers (one per each data line) is explained.

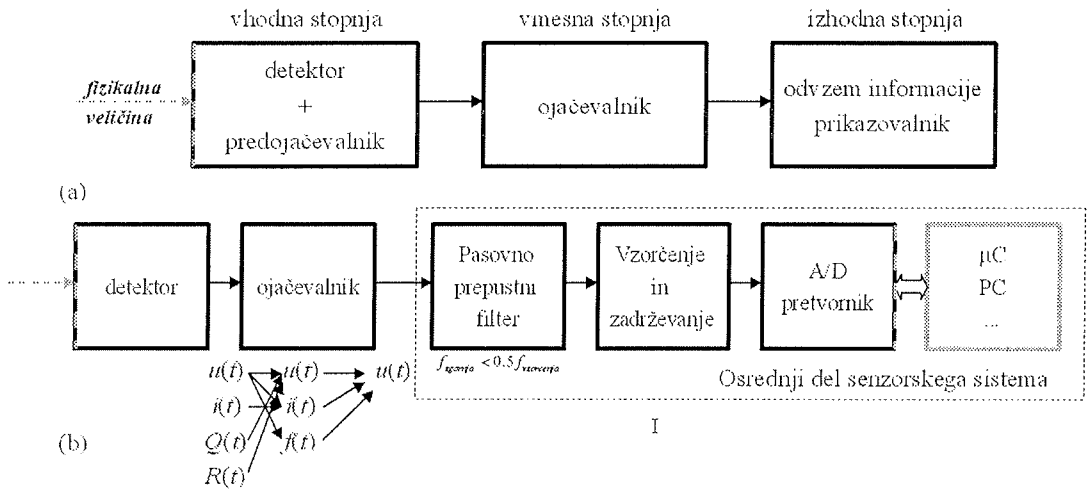
Utilization of current loop (Fig. 9) as a means of diminishing the effect of disturbances on analog transmission path of information signals is highlighted.

1 Uvod

Detektorji pretvarjajo fizikalne veličine v električne. Pretvorba je po večini šibka in električni signal je slaboten ter ranljiv od motenj, šuma ipd., zato ga je treba ojačiti preko več stopenj. Navadno so detektorji dislocirani od osrednjega dela sistema, in na poti od detektorja do osrednjega dela si pomagamo z raznovrstnimi elektronskimi vezji. Nekatere izmed rešitev odjema električnega signala, ojačevanja, pretvarjanja in vzorčenja bomo opisali v tem prispevku.

Senzorski sistem lahko načelno razdelimo na tri stopnje: vhodno, vmesno in izhodno stopnjo (slika 1a). Vhodna stopnja vsebuje detektor, ki fizikalno veličino pretvori v električno, in predojačevalnik, ki šibek električni signal odjema in ga ojači. Predojačevalnik je praviloma malošumni ojačevalnik z majhnim popačenjem. Predojačevalnik izboljšuje in hkrati navzgor omejuje razmerje signal/šum ter se lahko izkoristi tudi za linearizacijo detektorjevega odziva. Vmesna stopnja navadno vsebuje večstopenjski ojačevalnik, ki nam zagotavlja kakovosten prenos električnega signala do izhodne stopnje, kjer se informacija odvzema in se bodisi prikazuje bodisi shranjuje.

Na sliki 1b je senzorski sistem razčlenjen bolj podrobno in vključuje analogno-digitalno pretvorbo. Električna veličina, ki jo generira detektor, je lahko napetost u, tok i, naboj Q ali upornost R. Na poti od odjema detektorskega signala pa do osrednjega dela sistema (mikrokontrolerja, osebnega računalnika, ...) se lahko informacija pretvarja iz ene analogne električne veličine v drugo, ki pa se navadno na koncu analogne poti zaključi kot napetostni signal. Pretvorbe morajo biti čim bolj linearne, čim manj občutljive za motnje iz okolice in s čim manjšim lezenjem (npr. tem-



Slika 1: Shematska prikaza senzorskega sistema

peraturno, časovno lezenje). V osrednjem delu senzorskega sistema analogni napetostni signal frekvenčno omejimo z nizkoprepustnim ali pasovnoprepustnim filtrom, ki ima zgornjo frekvenčno mejo določeno glede na frekvenco vzorčenja A/D- pretvornika. Shannonov teorem /1/ postavlja za spekter vzorčnega signala brez prekrivanja omejitev za zgornjo mejo:

$$f_{zgornja} < \frac{1}{2} f_{vzorcenja}$$

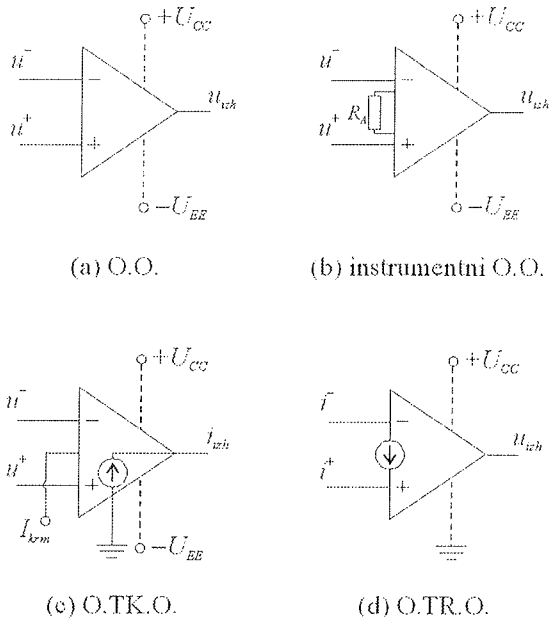
Vezje za vzorčenje in zadrževanje poskrbi, da je v času pretvorbe enega vzorca na vhodu A/D-pretvornika konstantna vrednost. Informacija v digitalni obliki je preko podatkovnega vodila primerna za nadaljnjo obdelavo, prikazovanje ali shranjevanje.

2 Osnovni gradniki in izvedbe ojačevalnikov

Kljub množici elektronskih gradnikov, predvsem v integrirani obliki v enem ohišju, izpostavimo najbolj razširjene. Prvo mesto zagotovo pripada operacijskemu ojačevalniku (O.O.), ki ima napetostni diferenčni vhod z visoko vhodno impedanco in napetostni izhod z nizko izhodno impedanco (slika 2a). V linearnem območju delovanja ima veliko diferenčno napetostno ojačanje (A_d)

$$u_{izh} = A_d (u^+ - u^-)$$

in s tem izvaja matematično operacijo odštevanja dveh vhodnih signalov (od tod tudi ime operacijski ojačevalnik). Hkrati pa se O.O. odlikuje z visokim rejekcijskim faktorjem za sofazne vhodne signale (CMRR ~ 80..120 dB) in z visokim rejekcijskim faktorjem za valovitost napajalne napetosti (PSRR ~ 80..120 dB) /1,2/. Diferenčno napetostno ojačenje je žal frekvenčno omejeno. Merilo frekvenčne zmogljivosti ojačevalnikov je produkt ojačenja in mejne frekvence, ki je pri O.O. praviloma konstanten, ne glede na izbrano velikost ojačenja (slika 3a). Operacijski ojačevalnik ima mnogo izvedb, med katerimi se odlikuje instrumentni operacijski ojačevalnik, ki v enem ohišju združuje 3 operacijske ojačevalnike in ki mu z zunanjim uporom (programirljivo) nastavljamo diferenčno napetostno ojačenje (slika 2b). Instrumentne operacijske ojačevalnike odlikujejo tudi izredno velik CMRR in PSRR. V primerih potrebe po galvanski ločitvi med vhodom in izhodom pa posegamo po izolacijskih operacijskih ojačevalnikih /1/.



Slika 2: Osnovni gradniki ojačevalnikov

Operacijski transkonduktančni ojačevalnik (O.TK.O.) ima napetostni diferenčni vhod z visoko vhodno impedanco in tokovni izhod z visoko izhodno impedanco (slika 2c). V linearnem območju delovanja izkazuje veliko transkonduktanco (g_m):

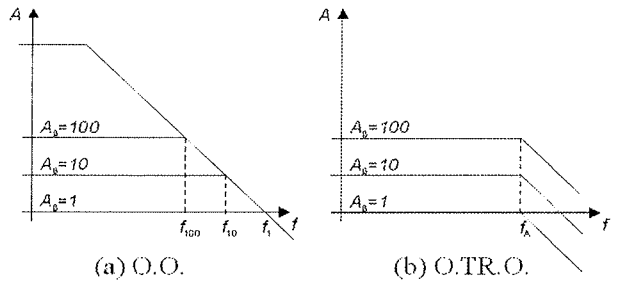
$$i_{izh} = g_m (u^+ - u^-) = k I_{krm} (u^+ - u^-)$$

ki jo lahko spreminjamo (moduliramo) s krmilnim tokom (I_{krm}). Ta ojačevalnik se uporablja v vezjih za vzorčenje in zadrževanje, multipleksorjih, množilnikih in napetostnih sledilnikih z visokim maksimalnim časovnim gradientom izhodne napetosti (ang. »slew-rate«).

Operacijski transrezistivni ojačevalnik (O.TR.O.), ki ga nekateri imenujejo tudi Nortonov ojačevalnik, ima tokovni diferenčni vhod z nizko vhodno impedanco in napetostni izhod z nizko izhodno impedanco (slika 2d). V linearnem območju delovanja izkazuje veliko transrezistivnost (r_m):

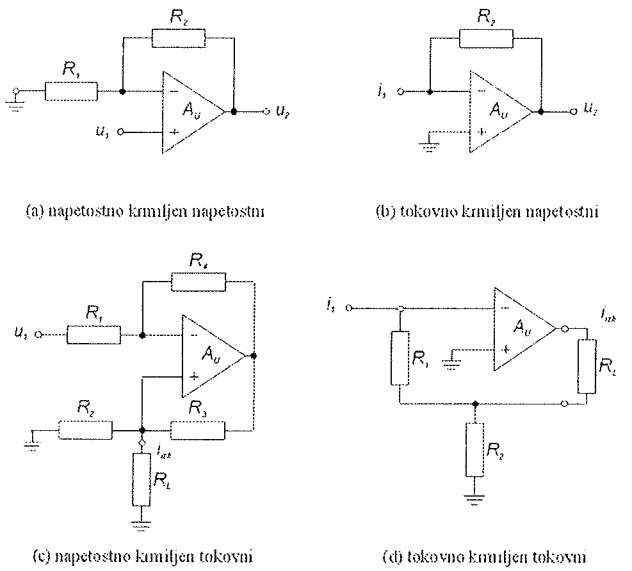
$$u_{izh} = r_m(i^+ - i^-)$$

Zanj je značilno, da nima omejevanja pasovne širine (slika 3b) in maksimalnega časovnega gradienta izhodne napetosti. Navadno zahteva le enojno napajanje.



Slika 3: Frekvenčna odvisnost ojačenja za (a) O.O. in (b) O.TR.O.

Iz vsakega gradnika lahko z negativnim povratnim sklopom realiziramo vse štiri izvedbe ojačevalnikov: napetostno krmiljen napetostni (NN) ojačevalnik, napetostno krmiljen tokovni (NT) ojačevalnik, tokovno krmiljen napetostni (TN) ojačevalnik in tokovno krmiljen tokovni (TT) ojačevalnik. Slika 4 prikazuje vse štiri izvedbe ob uporabi O.O. kot gradnika teh ojačevalnikov.



Slika 4: Štiri izvedbe ojačevalnikov z O.O. kot osnovnim gradnikom: NN, TN, NT, TT

3 Odjem detektorskega signala

Pri opisu različnih odjemov detektorskega signala bomo uporabili realizacije z O.O. kot osnovnim gradnikom.

3.1 Mostični odjem

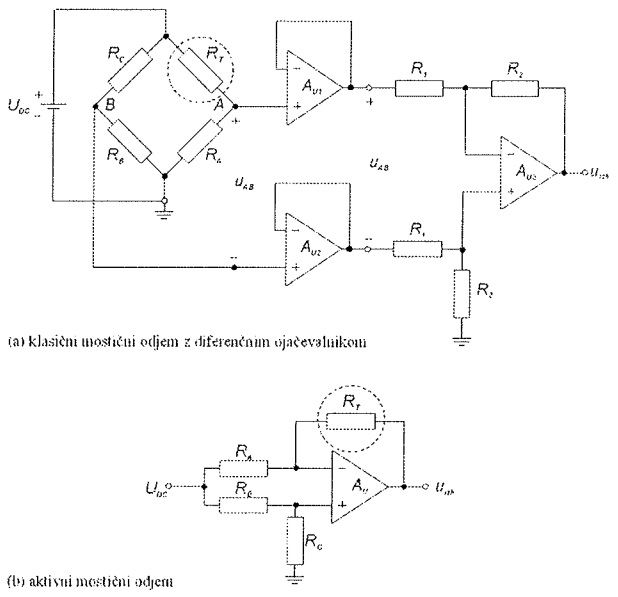
Mostični odjem se uporablja za odjem upornosti na našem detektorju, ki jo preoblikujemo v napetost. Slika 5a prikazuje *klasični mostični odjem*, ki je nadgrajen z diferenčnim ojačevalnikom. Neuravnoteženost uporov v mostiču, ki jo povzroča merjena fizikalna veličina (izberimo $R_A = R_B = R_C = R$ in $R_T = R + \Delta R$), povzroča različen enosmerni tok v obeh vejah mostiča, kar ustvarja napetostno razliko med sponkama A in B:

$$U_{AB} = -\frac{\Delta R}{2(2R + \Delta R)} U_{DC} \cong -\frac{\Delta R}{4R} U_{DC}$$

Odjem napetosti ne sme obremeniti uporovnega mostiča, zato mora biti odjem izveden z enakima in čim večjima vhodnima upornostima, ki ju dosežemo z uporabo dveh napetostnih sledilnikov, ki jima sledi diferenčni napetostni ojačevalnik. Enako dosežemo tudi z uporabo instrumentnega O.O.

Konfiguracijo diferenčnega napetostnega ojačevalnika izkoriščamo pri *aktivnem mostičnem odjemu* (slika 5b), ki ima detektor (upornost R_T) nameščen v povratnem sklopu. Aktivni mostični odjem ima dvakrat boljšo občutljivost, saj zanj velja:

$$U_{izh} = -\frac{\Delta R}{2R} U_{DC}$$



Slika 5: Mostični odjem: (a) klasični in (b) aktivni

3.2 Napetostni odjem

Napetostni odjem bomo opisali na primeru fotodiode. Fotodioda je detektor svetlobnega toka in lahko deluje pri različnih režimih delovanja. Eden izmed njih je režim odprtih sponk, ko ob osvetlitvi skozi fotodiodo ne teče noben tok, med priključnima sponkama pa čutimo napetost odprtih sponk (U_{OC}). Režim odprtih sponk in napetostni odjem fotodiode je zagotovljen z vezjem, prikazanim na sliki 6a. Če je vhodni tok v neinvertirajočo vhodno sponko O.O. zanemarljiv ($i^+ \cong 0$), nam O.O. v linearnem območju delovanja zagotavlja takšno izhodno napetost, da je U_{OC} tudi na invertirajoči vhodni sponki. Od tod sledi ob pogoju $i^- \cong 0$:

$$U_{izh} \cong \frac{R_1 + R_2}{R_1} U_{OC} \propto \ln(I_{ph})$$

Ker je U_{OC} logaritemsko odvisna od vpadnega svetlobnega toka I_{ph}, smo s tem dobili logaritemski merilnik.

3.3 Tokovni odjem

Fotodioda nam v kratkostičnem režimu delovanja ustvarja električni tok, ki je linearno odvisen od I_{ph}. Vezje na sliki 6b nam poleg zagotavljanja kratkostičnega režima fotodiode pretvarja in ojačuje tokovni signal v napetostnega:

$$U_{izh} \cong R_2 I_{SC} \propto I_{ph}$$

Da bi bilo ojačenje čim večje, potrebujemo čim večjo upornost R_2. V realnem O.O. ($i^+ \neq 0$, $i^- \neq 0$) je za izničenje vpliva vhodnega predtoka (sofazne komponente) potrebno tudi neivertirajočo vhodno sponko zaključiti z enako upornostjo, kot jo čuti invertirajoča sponka /2/ (slika 6c). Velika vrednost R_2 pa nam izmika kratkostični režim delovanja fotodiode in hkrati povečuje ničelno izhodno napetost. Rešitev je v ohranjanju velikega ojačenja ob zmanjšanju upornosti, ki jo čuti invertirajoča sponka. To dosežemo z uporovnim T-četveropolom ($R_2 >> R_{2T} >> R_B >> R_A$) v veji povratnega sklopa /3/ (slika 6d), pri čemer izberemo:

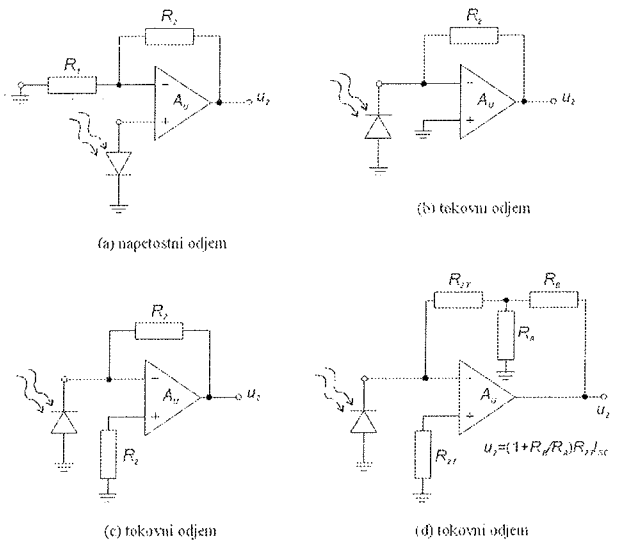
$$R_{2T} = \frac{R_A}{R_A + R_B} R_2$$

3.4 Odjem naboja

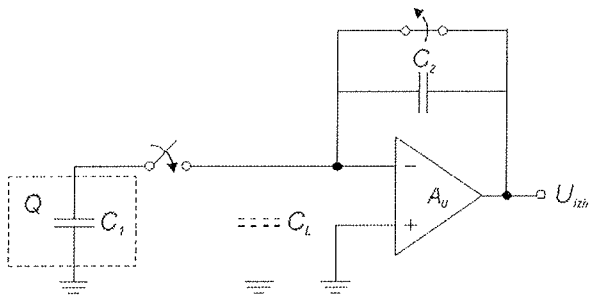
Pri odjemu naboja izkoriščamo O.O. v konfiguraciji ojačevalnika naboja (slika 7), ki pa zahteva najmanj dve elektronski stikali, kajti kondenzator C_2 mora biti inicializiran pred vsakokratnim prenosom naboja z detektorja. Izhodna napetost je tako proporcionalna naboju Q:

$$U_{izh} = -\frac{Q}{C_2}$$

V sliki 7 je črtkano vrisana še kapacitivnost C_L, ki je predvsem posledica kapacitivnosti dovodne linije, in nam idealno nabojno-napetostno zvezo kvari (slabi).



Slika 6: Realizacije: (a) napetostni odjem in (b-d) tokovni odjemi

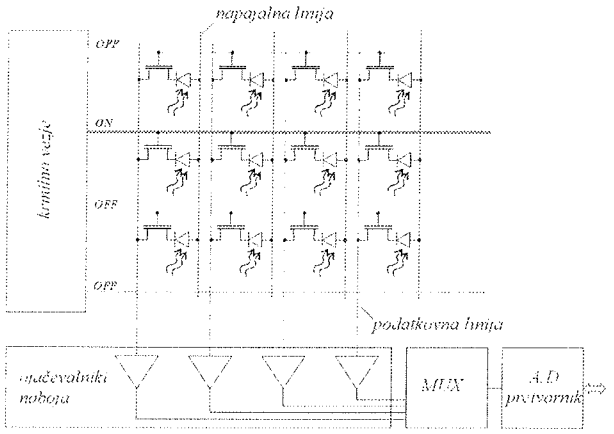


Slika 7: Realizacija odjema naboja

Princip odjema naboja se uporablja pri optoelektronskih detektorskih poljih, kjer imamo dvodimenzionalno razporejene posamične detektorje, t. i. pike (»piksle«) (slika 8). Informacija iz detektorskega polja se prenaša hkrati za eno celotno vrstico hkrati. S primernim naslavljanjem elektronskih stikal s krmilnim vezjem hkrati prenašamo naboj iz vseh detektorjev ene vrstice na ojačevalnike naboja, katerih izhodne napetosti zaporedno združujemo (multipleksiramo) v en signal. Pri multipleksiranju 128:1 potrebujemo na vsakih 128 ojačevalnikov naboja po en analogno-digitalni pretvornik.

4 Zmanjševanje vpliva motilnih signalov

Vpliv motilnih signalov na poti od detektorja do osrednjega dela senzorskega sistema je treba minimizirati. Posamični tipi detektorjev zahtevajo specifične rešitve, pri vseh pa je treba nameniti posebno pozornost predojačevalniku in poskrbeti za neobčutljivost za spremembe napajalnih napetosti. Pri inteligentnih senzorjih skušamo digitalno pretvorbo izvesti čim bliže detektorju, da je analogna pot signala



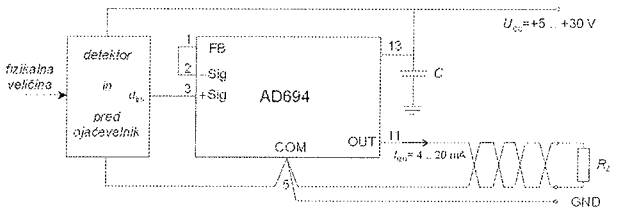
Slika 8: Realizacija odjema naboja v detektorskem polju. V trenutku, ko vrstica dobi od krmilnega vezja potencial ON, *gredo nanjo priključeni stikalni tranzistorji v stanje ON, s čimer lahko naboj detektorjev (informacija posamezne pike (»piksla«)) v tej vrstici odteče na ojačevalnike naboja.*

čim krajša. Zato prevladujejo digitalne motnje, ki pa se jih da uspešno odpravljati (npr. pri prenosu podatkov izvajamo CRC-preverjanje).

Pri dislociranih odjemih analognih detektorskih signalov je zelo razširjena tokovna zanka 4-20 mA. Ta interval od 4 mA do 20 mA ustreza linearnemu preslikanemu intervalu izhodne veličine predojačevalnika. Tokovna zanka se odlikuje po naslednjih lastnostih: (a) neobčutljiva za daljše razdalje (ni napetostnih padcev), (b) hitro zaznavanje napak (mirovni tok 4 mA ob ničtem signalu), (c) na koncu tokovne zanke preprosta zaključitev z uporom R_Z, katerega vrednost je izbrana glede na napajalno napetost in pričakovano maksimalno vhodno napetost osrednjega dela senzorskega sistema. Slika 9 prikazuje uporabo tokovne zanke 4-20 mA, katere jedro je integrirano vezje AD694 /3/ v vlogi linearnega napetostno (0-2 V) - tokovnega (4-20 mA) pretvornika.

5 Sklep

V prispevku smo pregledali nekatera elektronska vezja, ki jih srečamo na poti od detektorja do osrednjega dela senzorskega sistema. Opredelili smo najpomembnejše osnovne gradnike in izvedbe ojačevalnikov ter opisali način



Slika 9: Realizacija tokovne zanke 4-20 mA ob uporabi integriranega vezja AD694

in realizacijo odjema upornosti, napetosti, toka in naboja. Podali smo zgled delovanja optoelektronskega detektorskega polja. Pri prenosu analognih signalov smo se posvetili zmanjševanju vpliva motilnih signalov s tokovno zanko.

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MICROSYSTEMS WITH INTEGRATED CAPACITIVE, MAGNETIC AND OPTICAL SENSORS

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POSVET O SENZORJIH V ZAVODU ITC SEMTO
15.03.2002, FE Ljubljana

Key words: integrated sensors, Hall sensors, optical sensors, capacitive sensors

Abstract: This article discusses microsystems with integrated sensors for measuring various physical values like acceleration, electrical current and motion. An integrated microsystem is presented for all three physical values. These microsystems are composed from the integrated sensor and the processing electronics all on the same silicon die. The emphasis of this article is on the presentation of the integrated sensors.

Mikrosistemi z integriranimi kapacitivnimi, magnetnimi in optičnimi senzorji

Ključne besede: integrirani senzorji, Hall senzorji, optični senzorji, kapacitivni senzorji

Izvleček: Članek obravnava mikrosisteme z integriranimi senzorji za merjenje fizikalnih veličin kot so pospešek, električni tok in gibanje. Za vsako veličino je predstavljen integrirani mikrosistem, ki je sestavljen iz senzorjev in obdelovalne elektronike, ki sta integrirani na istem silicijevem substratu. Poudarek članka je na predstavitvi integriranih senzorjev.

1. INTRODUCTION

We are witnessing an extreme advent in the computer and communication technology. In contrast to these advances the possibility to gather and process information from the physical world lags behind. Great advances in this area are possible with the development of integrated microsystems. These are physical value measuring systems which combine the sensor and the processing electronics on the same silicon die.

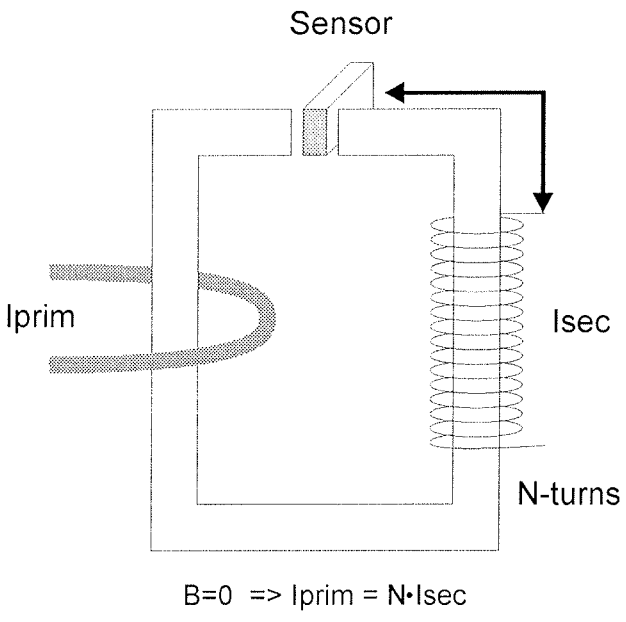

Fig. 1: Closed loop current measuring system

Three various microsystems are presented in this article:

- magnetic microsystem with integrated Hall sensors for electrical current measurement
- capacitive microsystems with micromechanical sensor for acceleration measurement
- optical microsystem with integrated photo diodes for displacement measurement

All three microsystems can replace the traditional discrete sensor and electronics systems and therefore reduce the cost and the area of the measurement system.

2.1 Magnetic microsystem with integrated hall sensors

The Hall magnetic sensors are compatible with the standard CMOS process therefore they can be easily integrated with the use of the n- well layer. The inherent characteristic of the Hall sensor can be largely improved with various techniques as the current spinning, bias current compensation, use of spatially distributed Hall sensors etc.

In the presented system a Hall sensor array is used for measuring the electrical current through the primary coil. This current generates a magnetic field sensed by the microsystem which also drives the secondary coil. The system is in a closed loop configuration and therefore the microsystem with the use of the secondary coil zeroes the magnetic field in the core. The current through the secondary coil is proportional to the primary current. The advantage of the closed loop system is the galvanic separation and high bandwidth (200kHz) of such a system.

An example of such a system is on fig.1. The magnetic sensors, processing electronics and the current driver amplifiers are all on the same silicon die (fig.2).

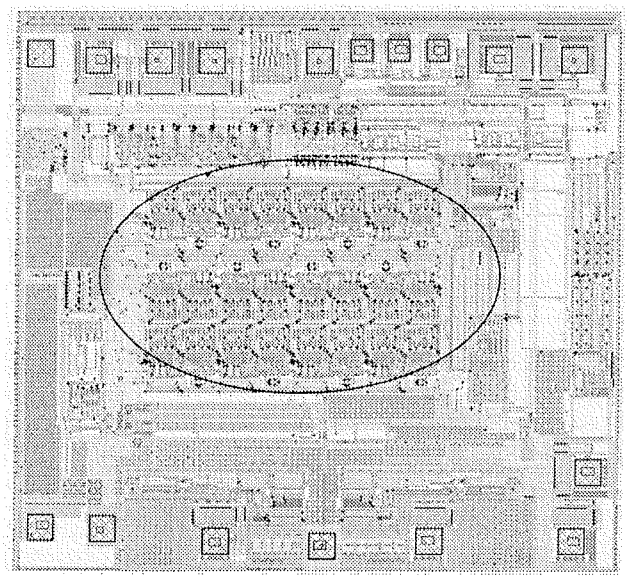

Fig. 2: Die plot with the marked magnetic sensor array

2.2 Capacitive microsystem for acceleration measurement

Various micromechanical objects can be created with the use of micromachining. A moving polysilicon plate can be constructed by underetching. This plate can bend under various forces enabling us to sense mechanical forces on the plate. A capacitor can be constructed using this polysilicon plate. If the system is accelerated the plate bends and therefore the capacitance also changes. A closed loop principle was used in the presented microsystem. A sensing capacitor plate and a actuator plate is needed for that. The actuator plate compensates the mechanical forces on the plate. The sensitivity of such a sensor is only 10aF/g therefore special care must be taken when designing the processing electronics. The resulting output sensitivity of the system is 40mV/g with a SNR of 60dB. On fig. 3 the cross-section through the microsystem is visible, on fig. 4 the layout of the IC with the sensing and actuating plate is visible.

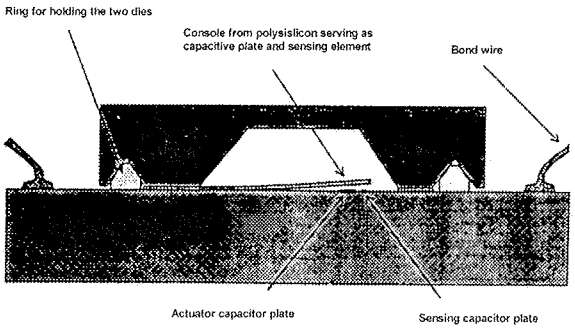

Fig. 3: Capacitive microsystem cross-section

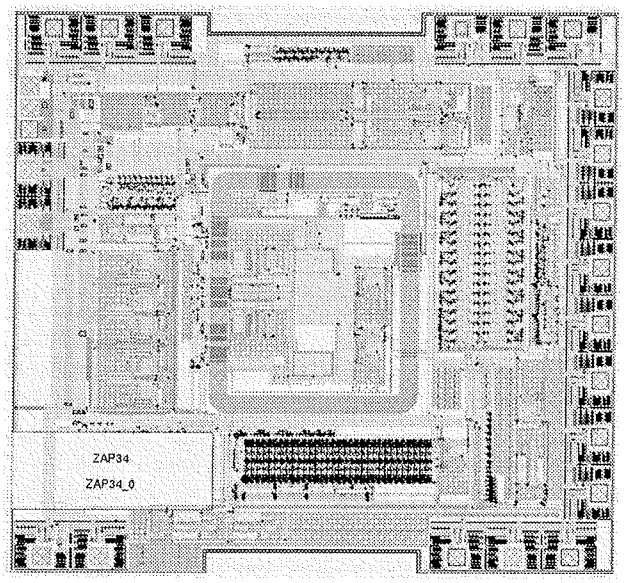

Fig. 4: Layout of the capacitive microsystem

2.3 Optical microsystem for displacement measurement

Such a microsystem combines the integrated photo diodes with the analog front-end and an interpolator for generating digital pulses from the analog information.

The photo diodes are combined into an optical array which senses the light filtered by the code wheel. By sensing the light the displacement of the wheel can be sensed. The integrated electronics amplifies the diode signals and with the use of the interpolator two orthogonal digital incremental output pulses are generated, representing the motion of the wheel.

The schematic of such a microsystem is on fig. 5, the layout of the IC with the photo-diodes and electronics is on fig. 6. The achieved photodiode responsitivity is 0.52A/W, the on chip interpolator division factor is 40.

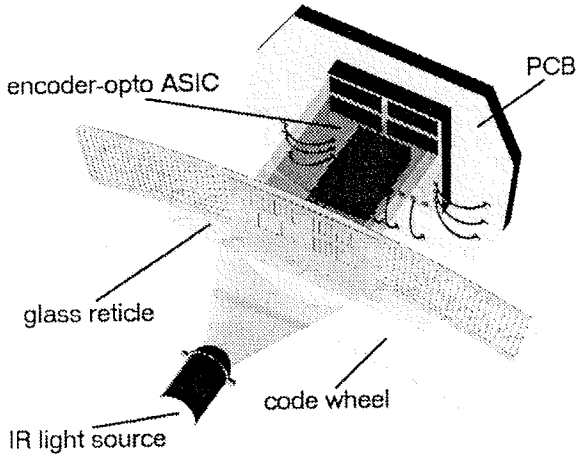

Fig. 5: Optical microsystem for incremental position application

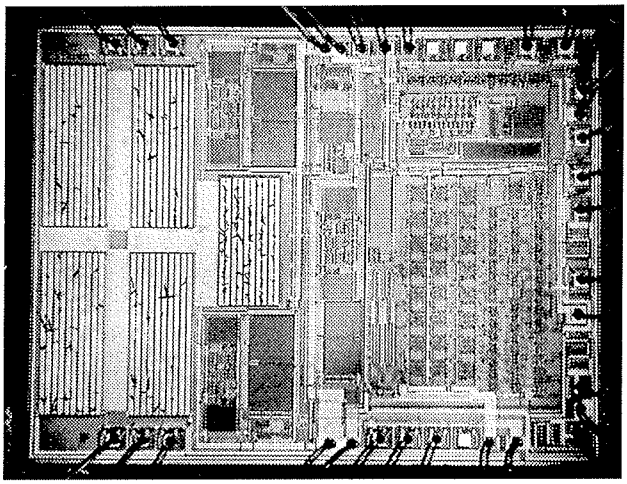

Fig. 6: Optical microsystem IC die plot with the photodiodes on the left side

3. CONCLUSION

Various sensors can be integrated in the standard CMOS technology enabling the development of integrated microsystems. With these sensors various physical values can be measured directly or indirectly.

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REDUCTION OF SWITCHING NOISE AND POWER SUPPLY CURRENTS IN DIGITAL CIRCUITS WITH DIRECTED DATA FLOW

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Key words: mixed design, switching noise, clock distribution.

Abstract: Substrate noise is a serious limiting factor in the design of analogue-digital systems. Distributed clock systems can be used as an efficient method to solve the simultaneous switching noise problems associated with the data processing and clock distribution. We present a short overview of known methods for switching noise reduction and propose a general clock distribution technique for circuits with directed data flows. The clock distribution network is implemented by a clock pipeline. The associated synchronisation problems are solved by reverse clocking scheme and signal latching in feedback loops. The processing of N-bit long data by the proposed system shows that power supply spikes can be reduced by a factor ~1.2N and the associated substrate noise by a factor of ~0.75N comparing to the standard central-clock solutions. This makes this method particularly well suited for measuring systems as noise reduction increments proportionally to precision.

Koncept digitalnega vezja z usmerjenim pretokom podatkov za omejevanje šuma in napajalnih tokov v integriranih vezjih

Ključne besede: načrtovanje analogno-digitalnih vezij, preklopni šum, signal ure.

Izvleček: Eden od pomembnih faktorjev ki omejujejo načrtovanje analogno-digitalnih integriranih vezij je šum, ki nastane zaradi injiciranja nosilcev v substrat vezja. Uporaba porazdeljenega signala ure v digitalnem delu vezja lahko ta problem v veliki meri zmanjša. V tem delu najprej podajamo kratek pregled znanih metod za zmanjševanje preklopnega šuma in nato predlagamo splošno rešitev za sisteme z usmerjenim pretokom podatkov. Krmiljenje signala ure je zasnovano na zakasnilni liniji. Zaradi tega nastane problem sinhronizacije, ki ga rešimo z uporabo obratnega pretoka podatkov in signala ure ter z ustreznimi zakasnitvami v povratnih zankah. V primerjavi s klasičnim sistemom predlagana metoda pri podatkovnih strukturah z dolžino N bitov omogoča zmanjšanje konic napajalnega toka za faktor ~1.2N in zmanjšanje šuma v substratu za faktor ~0.75N. Ker sta obe izboljšavi proporcionalni s preciznostjo obdelave podatkov je opisana metoda zlasti uporabna v merilnih sistemih.

1. Introduction

It is well known that digital circuits generate considerable electrical noise as a result of logic gate transitions from one state to the other. In logic systems the switching noise can cause transient faults while in mixed analog-digital circuits it can seriously limit the performance or even prevent proper operation of analog blocks that share the common substrate. In addition to substrate noise the power supply current spikes cause voltage drops and bouncing that can lead to functional failures and undesirable stressing of materials used to supply power to circuit elements.

With the evolution of VLSI circuits toward smaller feature sizes and higher operating speeds this problem is becoming more and more important. Supply currents in future digital chips are expected to rise dramatically /13/.The gap between transistor and interconnect performances is causing intolerable delays in old fashioned clock distribution networks /7/. At the same time the smaller sizes of basic elements give opportunity to integrate large systems containing analog blocks so that the demand for mixed circuits is increasing as well. As a consequence, the noise, clock and power distribution are becoming of utmost importance for future generations of integrated circuits.

There are many known techniques for reducing effects of the switching noise and switching currents. Examples of known solutions show that that they can be divided roughly into 5 categories:

1. *Isolation techniques* separate sources of noise from areas where they would do most harm.
2. *Additional circuits or devices* cancel effects of the switching noise.
3. *Special circuit techniques and logic topologies* are tailored to generate low switching noise and/or limit switching currents.
4. *Architectural measures* divide the circuit into blocks that are coordinated in such a way that we minimize the influence of noise-generating to noise-susceptible blocks.
5. *Additional data processing* can be used in order to remove noise components from output data.

However, none of the approaches can solve all possible problems. An early paper /1/ and a recent one /2/ present typical isolation techniques. Noise attenuation is possible only to a certain degree, so the methods described are useful when all other means have been exhausted and the level of noise is still expected to be too high. The general drawback of these methods is limited success and the in-

crease of chip area and design time which both reflect on the production cost.

Switching noise reduction devices can be used as additional logic elements driving load replica with the inverted logic function so that the quantity of switching current which flows in an inductance is reduced. Additional circuits can be used also to isolate the noise source logically. Methods of this kind are very specific and can be economically applied only to selected nodes of particular interest or nature that must be identified in each system individually.

Special circuits and logic topologies are most powerful design tools to reduce switching currents and switching noise. Circuit techniques have been invented to limit switching currents in stages that draw significant amounts of current, such as output signal driving stages. Another class of inventions covers the structure of logic operators. On the first place we have to mention various current mode techniques where switching currents are kept constant by means of current generators /16/. The problem with current mode logic families is that supply current is drawn regardless of circuit operating frequency, essentially preventing the power-down mode or power-saving operations in the system. Circuits from this family can be also more complex than known standard CMOS logic, resulting in increased chip area and design time.

Data processing measures are very specific and can be applied only when data processing is possible or already present in the system. In such a case the noise reduction technique is based upon shaping the noise from the digital circuit and concentrating it in a single, or a small number of parts in the frequency spectrum that can be filtered out /15/.

A well known example of architectural measures is the so called 'quiet period sampling' technique. It typically relies on two or more clocks that are separated in time to synchronize analog and digital blocks so that analog data are sampled in intervals when digital blocks do not produce noise. An example of this method comprising two clock signals is described in /14/. By delaying the digital clock signal, noise induced upon the substrate embodying the analog circuitry is shifted by an amount of time necessary to allow the noise to settle before the analog clock samples new data. A similar solution is described in /18/ where the clock system is divided into four clock subsystems, generating two pairs of clock signals so that one pair of signals is delayed with respect to the other pair in order to reduce the switching noise on power bus.

2. The distributed clock approach

The common drawback of known architectural methods is the lack of generality, so our goal is to find a systematic solution that can be used automatically in a broad range of circuits without going into the specifics of individual system timing and architecture. The method is based on directed data and clock flow control as presented on Figure 1. This structure is very general so that it can represent a large number of known building blocks such as counters, shift registers and data pipelines (Figure 2).

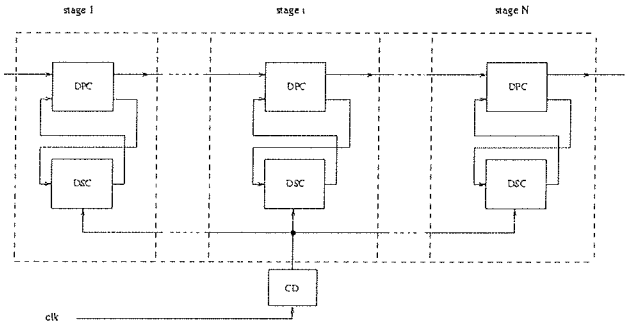
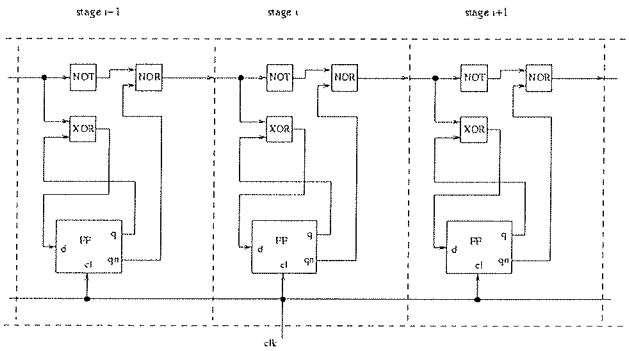
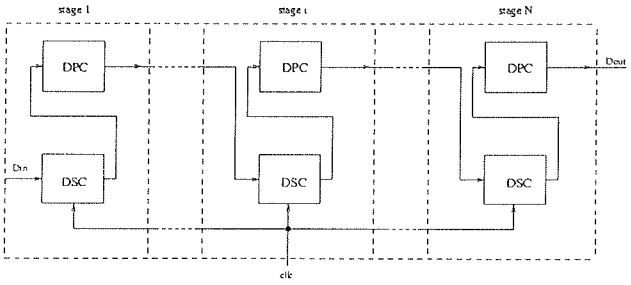


Figure 1. Structure of a synchronous digital system with directed data flow.



(a) Synchronous counter. DPC elements implement binary counting and DSC elements contain single flip-flops.



(b) Data pipeline. DPC inputs are connected to DSC outputs from the same stage while inputs to DSC elements come from DPC outputs from previous stage. The number of flip-flops in DSC elements may vary according to pipeline implementation.

Figure 2. Examples of typical building blocks, presented in the form of the structure from Figure 1.

In classic synchronous systems there is only one central clock driver (CD) while the data can be processed in several stages. The data flow is defined by connections be-

tween the data processing (DPC) and data storing circuits (DSC). Synchronized by the clock, transients occur in all stages simultaneously, causing large current spikes at clock edges. However if we treat the clock also as a data-flow process, the switching currents of most important noise sources (clock driver, flip-flops and logic gates) become controllable by the clock network. They can be distributed in time so that significant peak value reductions become possible. For the same reason, only a fraction of circuit nodes is active at a given time, leading to similar reduction of crosstalk /6/ and parasitic currents in the substrate /4/.

To control the clock flow we propose to replace the central clock driver by the clock pipeline, acting as a delay line. Signals from all stages are used so that we replace the central clock signal by a large number of local clock signals, applied in small circuit clusters. The simplest implementation of such clock delay line is the inverter chain (Figure 3). More complex solutions with delay lock loops can be used if clock delay is to be adapted to some system parameters.

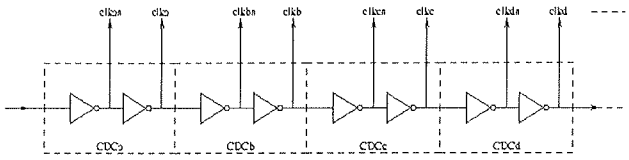


Figure 3. Clock pipeline implemented as a simple inverter chain.

Clock pipelines have been proposed in previous work on high speed clocking as a means for clock skew control in large processing arrays. In /2/,/8/ they were primarily studied as a substitute for the wire interconnect, taking only the signal from the last stage as the clock for a given module. One important property of clock pipelines is that clock skew depends more on transistor properties than on wires. Because of that, reasonable delay modeling is possible by timing or even logic simulation tools.

3. The synchronisation problem

The replacement of clock signal by a large number of delayed signals violates the basic principle of synchronous logic which relies on one single clock, distributed without significant delays to all parts of the system. However safe system operation is possible also under the distributed clock conditions if the data processing flow and the clock signal flow are properly coordinated in the time.

One possible solution is the application of reverse-clocking principle /22/.This technique has been reported mainly to prevent pipeline malfunctions at high speeds when clock lines start to exhibit RC line effects /3/. The idea is to propagate data and clock signals through a pipeline in opposite directions so that false strobing is not possible. In the case of distributed clocking, the clock delays are introduced by purpose so that they play a vital role also at low clock speeds.

The proposed structure is presented on Figure 4. Comparing to Fig. 1, the central clock driver is replaced by N delay line elements (CDC). If feedback data loops are presented in the system they are additionally delayed by the FDSC circuit which is synchronized from the last stage of the clock delay line.

In systems with the central clocking scheme the data to be processed remains stable after the active clock edge so that outputs of DPC circuits stabilize during the clock period. When the next active clock edge arrives, outputs are stored in DSC circuits so that next processing cycle begins. In the system with directed data flow and reverse clock distribution as presented on Figure 4, the same functionality is assured by the fact that active clock edge travels in time along the clock delay line and synchronizes individual data storage circuits sequentially. Stages that are hit first change their outputs. Because of the opposite direction of the data and clock signals these changes cannot influence inputs to stages that have not been hit yet. Processing inputs and the result of a given stage at the time when it is hit by the active clock edge depend exclusively on results from the previous clock cycle, stored in DSC circuits of the stages that have not been hit yet by the same active clock edge.

The reverse clock distribution as described above assures proper synchronization as long as stage inputs are not connected to outputs from the same stage. If such a connection is required by the system, the feedback data does not follow the rule of uniform data direction between stages. In such case additional data storage circuit (FDSC) is required in the feedback loop. The proposed structure with data feedback to stage 1 is presented on Figure 4. Feedback data from stage N (or any other stages) are delayed in the FDSC by the clock signal from the last clock delay line stage. This signal actually characterizes the end of current clock cycle and assures that feedback data will remain stable until the end of next processing cycle. Because of that, delayed feedback data from FDSC can be used as input to any DPC stage.

Another important limitation of the reverse clocking technique is the reduction of the effective clock cycle time. From the description given above it is evident that input to stage 1 must not change while the active clock edge travels along the clock delay line. If t_d is the clock delay in one stage then the effective clock cycle period is reduced for $N \cdot t_d$.

In order to automate the process of clock distribution the clock pipeline can be integrated into the data storage circuits. Each pipeline stage in this case contains the data processing, data storing and clock delay element. The central clock driver is completely removed and replaced by a distributed clock network. A typical example of this concept is presented on Figure 5. Depending on the type of

the logic circuit, various solutions for specific flip-flop and latching circuits are possible in order to provide the necessary delays and clock phases. With appropriate circuit design, transistor dimensions can be optimized to minimize the switching currents and the associated noise /23/.

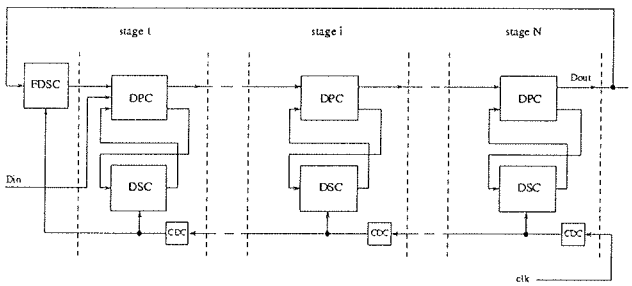


Figure 4. A general solution for switching noise reduction, based on distributed clocks from clock pipeline.

Although the delay and overlapping of the clock signals influence the noise and current spike reduction they are not essential for the spirit of this technique nor they can cause malfunction. The designer can decide upon these parameters on the basis of system speed and noise parameters, leaving the basic architecture unchanged.

4. Circuit solutions and results

Figure 5 illustrates the proposed technique on the shift register example. On Figure 7 we can see the power supply current simulation for N = 24, compared to equivalent register with the central clock. The reduction factor R = 11.2 has been measured for minimum-sized C^2MOS flip-flops operating at Vdd = 3V in a 0.6 um technology. The clock delay line has been integrated inside flip-flops. The register outputs in this example were loaded with 20 fF and the data shifted was 666666h -> CCCCCCh.

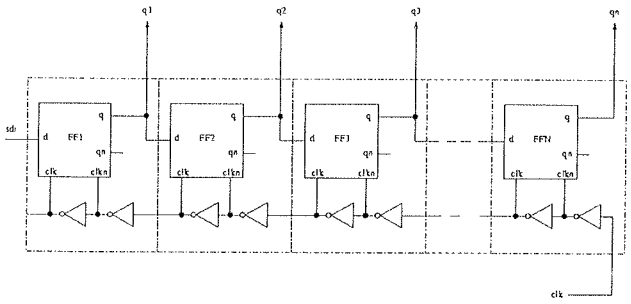


Figure 5. Example of a shift register, implemented according to Figure 4.

The simplicity of reverse clock principle requires also a price to be paid. The clock delay line may consume more power than an equivalent central clock driver may. Another important consideration is the limitation of clock period by the total delay in the clock delay line. This limitation

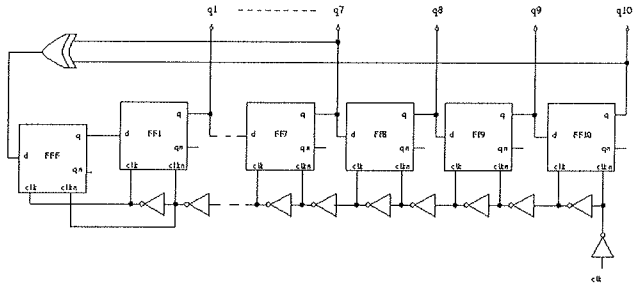


Figure 6. Example of proper feedback handling in the pseudo-random sequence generator, implemented according to Figure 4.

means in a way that circuit speed has been traded for supply current and noise reduction. Best results of the method described can be therefore expected in systems of moderate size and speed.

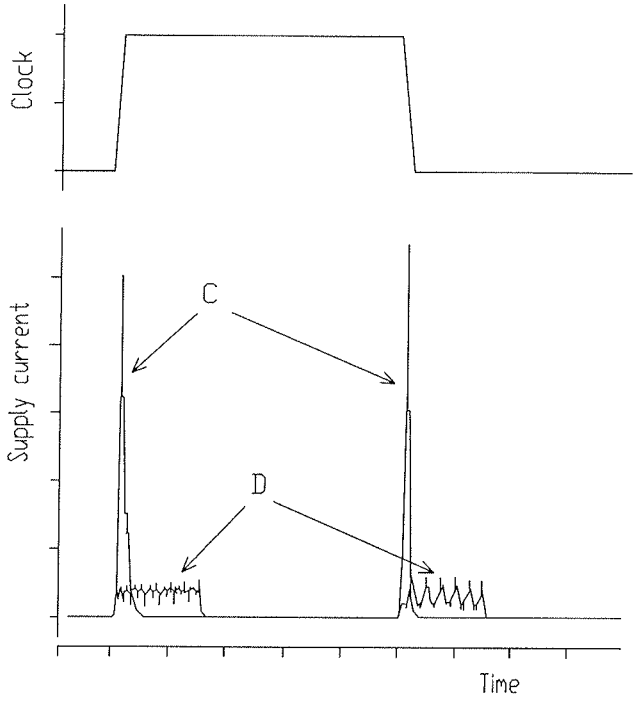


Figure 7. Simulation of power-supply current in the shift register from Figure 5 (waveform D), compared to equivalent circuit with central clock (waveform C).

5. Conclusion

The presented method is a mixture of circuit and architectural measures to reduce noise and switching currents in integrated circuits. It can be applied to digital systems with directed data flow processed in a number of stages. The reduction does not take place in individual logic gates, it comes into effect in larger blocks or the integrated circuit as a whole. Another important feature of the method is the fact that it can be used as an additional measure, together with other known methods for noise reduction and switch-

ing current limitation. It also does not imply any operating frequency limitations other then those given by the logic circuitry, including the power-down mode. The last but not least, the reduction of switching currents and noise does not apply only to logic gates and flip-flops, but also to the clock distribution system. The later is known to be an important source of noise because of large signal buffers and long metal lines. According to /3/, an estimation of power consumption in various chips shows 20-45% of power to be used for clock system. Half of this power can be roughly assigned to flip-flops and the other half to clock buffers. Switching currents and noise can be assumed to follow the same distribution.

If the logic block is composed of N stages, the switching current and switching noise can be reduced proportionally to N. Exact numbers depend on timing relations between clock signal delay, switching characteristics of the logic and data being processed. In simple cases with minimum processing logic, like the one presented on Figure 5, high reduction factors around N/2 can be achieved easily.

A number of well known building blocks, such as counters, shift registers and data pipelines can be built according to the presented method. The supply current spike and substrate noise reductions are proportional to the number of stages if compared to the conventional central clock systems.

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AREA AND POWER CONSUMPTION EFFICIENT VLSI IMPLEMENTATION OF PROGRAMMABLE COMB DECIMATION FILTER WITH LOW SWITCHING NOISE

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Key words: Decimation filters, comb structure, VLSI design, Σ–Δ A/D converters, switching noise reduction, power consumption minimization, IIR-FIR comb decimator.

Abstract: Power consumption, switching noise and area are among the most important parameters of decimation filters used in Σ–Δ A/D converters. We found that IIR-FIR implementation of a comb decimator gives the best compromise regarding this 3 parameters by using systematic method for switching noise and power consumption reduction and besides it is very easy to change the decimation factor. A programmable A/D converter has been built using noise optimized 2nd order modulator and optimized 3rd order comb decimator with f_{ovs}=4MHz and programmable oversampling ratios M=256, 128, 64. The area needed using 0.6μm CMOS technology is slightly less than 0.7mm^2. Average current consumption is approx. 2 times smaller and switching noise injected into the substrate is reduced almost 5 times compared to standard implementation. Measured results suggest that because of very low switching noise it is possible to use such IP block in high-resolution mixed-signal ASICs.

Površinsko in močnostno učinkovite VLSI implementacije programabilnega comb decimacijskega filtra z majhnim preklopnim šumom

Ključne besede: Decimacijski filtri, strukture comb, načrtovanje VLSI vezij, Σ–Δ A/D pretvorniki, zmanjševanje digitalnega šuma, IIR-FIR comb decimacijski filtri.

Izvleček: Najpomembnejši parametri pri načrtovanju decimacijskih filtrov uporabljenih v Σ–Δ A/D pretvornikih so poraba moči, preklopni šum in površina. Ugotovili smo, da struktura IIR-FIR omogoča najboljši kompromis glede navedenih treh parametrov pri uporabi sistematične metode za zmanjševanje porabe moči in "digitalnega" šuma. Poleg tega predlagana struktura omogoča enostavno implementacijo programiranja. Realizirali smo programabilni A/D pretvornik sestavljen iz optimiziranega modulatorja drugega reda in optimiziranega decimatorja comb tretjega reda, ki tečeta z vzorčevalno frekvenco f_{ovs}=4MHz in mu lahko programiramo decimacijski faktor. Površina silicija, ki jo potrebujemo za realizacijo takega comb decimacijskega filtra je manjša kot 0.7mm^2 v tehnologiji CMOS z dolžino kanala 0.6μm. Povprečen napajani tok comb decimatorja je približno 2 krat manjši, "digitalni šum" pa približno 5 krat manjši v primerjavi s standardno VLSI implementacijo. Izmerjeni rezultati dokazujejo, da je zaradi majhnega "digitalnega šuma" tak gradnik mogoče uporabiti pri načrtovanju občutljivih mešanih analogno-digitalnih vezjih z veliko ločljivostjo.

1 Introduction

Decimation filters are used in single or multi-bit Σ–Δ A/D converters to attenuate shaped quantization noise coming from one or multi-bit modulator and to reduce oversampling frequency to the Nyquist rate /5/. Out-of-band quantization noise must be attenuated before decimation in such a way that negligible amount of aliasing occur. Different realizations are possible and one of the most efficient in terms of hardware complexity is comb decimation structure /3/, using only additions, delays and down sampling. The order of a decimator is usually higher than the order of the modulator to be able to efficiently attenuate shaped quantization noise before decimation /5/. Other important concerns are area, power consumption and generation of "digital noise". Digital part of the A/D converter must inject minimum amount of "digital noise" into the substrate, must have as small power consumption as possible and must occupy as small silicon area as possible. In this paper we present such VLSI implementation, which also generates small amount of switching noise and has a possibility to program over-sampling ratio M in a simple and efficient way.

In section 2 short overview of possible implementations is given comparing characteristics regarding silicon area, power consumption, programmability and generation of digital noise. In section 3 we discuss programmability of the decimator, while section 4 shows simulation and measured results of a complete 16-bits A/D converter using programmable oversampling ratio. Section 5 presents the conclusions.

2 COMB decimator implementations

Transfer function of a comb decimator is defined in (1):

$$H(z)=\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^{k} \quad (1)$$

where M is decimation factor and k is the order of the filter. Possible signal processing implementations that do not require any multiplications are presented on figure 1: direct implementation on figure 1a, IIR-FIR implementation on figure 1b /5/, FIR2 cascade: figure 1c /8/. Two other possible implementations, POLY-FIR2 /7/ and RS implementation presented in /4/ are not really useful because they both need multipliers and thus significant amount of silicon area.

Direct implementation is the most straight-forward but not useful in really because the whole filter runs with oversampling frequency and thus consumes a lot of power and in addition it requires too much silicon area. Popular implementation for fixed oversampling ratio is a cascade of IIR-FIR filter and decimation in between, where the IIR part runs with f_{ovs} and FIR section runs with frequency $f_{FIR}=f_{ovs}/M$ taking every M^{th} sample from the IIR as the input for the FIR section. IIR section is composed of cascaded digital integrators. The arithmetics must be so called modulo or wrap-around arithmetics with Word length W defined in equation (2) /6/:

$$W=(W_{in}+k\log_2(M)) \quad (2)$$

where W_{in} is input word length, k is order of the filter and M is decimation factor. During integration the integrator states in IIR section increase until wrap-around happens. Difference realized in cascaded FIR sections gives correct result even if overflow was produced and the number in IIR registers has flipped. This is of course possible only if the register length in IIR and FIR stage conforms to the equation (2) above. The arithmetics used is two's complement modulo or wrap-around arithmetics.

The drawback of presented structure is that the registers of the whole IIR stage are wide (having for example for W_{in} =1, M=128, k=3 : W=22 even if possible resolution of an A/D converter is just 16 bits) and that the whole IIR section runs with oversampling rate f_s. Nevertheless as others have proved all other implementations except FIR2 need bigger area because of multipliers. Besides, other structures are so irregular that it is very hard to use systematic methods for reduction of switching noise defined in /1/. For IIR-FIR structure it is very easy to add programmability as is suggested in next section. The only competing architecture regarding area, power consumption, switching noise and programmability is FIR2 architecture, so let us briefly discuss it. Rewriting equation (1) using commutative rule we get (3):

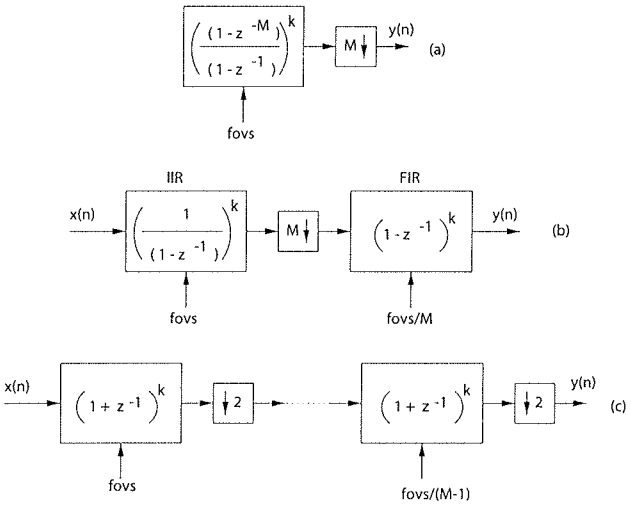

Figure 1: Possible implementations of a comb decimation filter

$$H(z)=\sum_{k=0}^{M-1}z^{-k}=\prod_{i=0}^{k\log_2 M-1}\left(1+z^{-2^i}\right)^{k} \quad (3)$$

It can be implemented as a cascade of equal first order FIR sections and decimation by 2 in between(see figure 1c). The word-lengths are different for every register in a cascade and need to be $W=(W_{in}+k_i)$. The first FIR stage calculates $(1+z^{-1})^k$ running with f_{ovs} and the word length need to be 2, 3 and 4 bits for k=3 and W_{in}=1 followed by decimation by factor 2. It is implemented by taking every 2^{nd} sample to the next stage which calculates again $(1+z^{-1})^k$ running with $f_s/2$ having word lengths of 5, 6 and 7 bits and so on. If we compare IIR-FIR and FIR2 signal processing requirements regarding number of bits in all registers (R), needed bit-additions/sec (A) and bit-shifts/sec (S) neglecting control logic the results are presented in table 1.

Table 1: Comparison of processing requirements for IIR-FIR and FIR2 structure

structure	R	A	S
IIR-FIR	150	$76*f_{ovs}$	$76*f_{ovs}$
IIR2	324	$36*f_{ovs}$	$36*f_{ovs}$

From this table we can easily see that IIR-FIR structure occupies smaller area compared to FIR2 because it needs smaller number of registers, besides the implementation is very regular and easy to design. The power consumption and switching noise seems to be bigger for IIR-FIR implementation if we consider just number of arithmetic operations and shifts. In reality FIR2 implementation is not so regular and up to now it was not possible to use systematic design methodology defined in /1/ for reduction of power consumption and switching noise. In addition, irregular structure requires bigger controller to implement

the algorithm, which further increases the area and also power consumption and switching noise. Since we are interested in area, power consumption, programmability and substrate noise generated in decimator (because modulator is built on the same substrate as the decimator) it seems that the approach giving optimum solution regarding all 4 requests is the IIR-FIR cascade improved in several ways: programmability, using VLSI implementation in which part of the switching energy is recycled /1/ and in this way low power consumption and very small switching noise is achieved. Because of the reasons above we selected suggested approach.

3 Programmable comb decimator

Detailed signal processing block diagram of 3rd order IIR-FIR decimator is presented on figure 2. Higher order is possible by cascading more IIR and FIR stages having decimation in between or by cascading several comb filters. We selected 3rd order decimator because we wanted to built programmable speed/resolution A/D converter using 2nd order modulator and 3rd order decimator. Programmability is achieved simply by extending the word-lengths to the maximum needed according to the variables M, k and W_{in} in equation (2) and taking every M^{th} result from the IIR stage. The new condition for the word lengths is given by equation (4):

$$W \geq (W_{in} + k \log_2(M)) \qquad (4)$$

using only so many bits at the output of the decimator as it is necessary for proper operation of a wrap-around arithmetic without loosing any information under any condition.

In next section some simulation and measured results are presented for programmable A/D converter having programmable oversampling ratio: M=64, 128, 256. In this way it is possible to program the speed and resolution of the A/D converter using only one 2nd order modulator and one 3rd order programmable decimator. Minimum word-length that would be needed for proper calculation is given in table 2 using parameters: k=3, W_{in}=1 and M=64, 128, 256.

Table 2: Word length of a 3rd order decimator for different M's

M	DUB	DLB	W	Wout
256	0	8	25	17
128	3	5	22	17
64	6	2	19	17

The names of the constants are: DUB is number of upper redundant bits at the output, DLB is number of lower redundant bits, W is minimum register lengths and W_{out} is the length of the output word. The decimator's word-length is: W=25 for all M's. Because quantization and thermal noise is constrained by the modulator's 16 bits resolution at M=256 and further signal processing needs, the word length taken out of the decimator is 17 bits for all M's. Each register has a length of 25 bits so wrap around arithmetics in IIR and FIR stage always performs 25 bits modulo arithmetics whatever the M is. We take out 17 bits (we need more bits because of further signal processing) according to figure 3. We could easily take out smaller number of bits for M=128 and M=64 but because of regularity 17 bits are taken out. The principle could be easily extended to other decimation factors M as long as M is a power of 2. The IIR section runs with f_{ovs} and the FIR section runs with f_{ovs}/M and is thus implemented in a serial processor. Because of its very regular structure it was possible to use systematic approach for power consumption minimization and for reduction of switching noise injected into the substrate /1/. Figure 4 shows layout of the decimator. Regular structure is clearly evident from the picture and needs only 0.7mm^2 in 0.6μm CMOS technology.

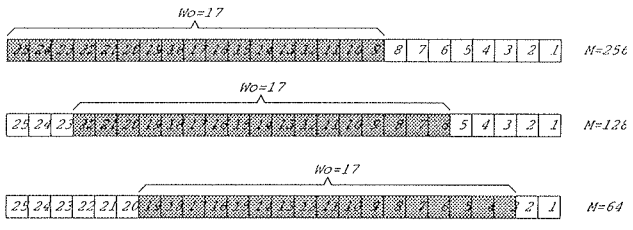

Figure 3: Output word formation

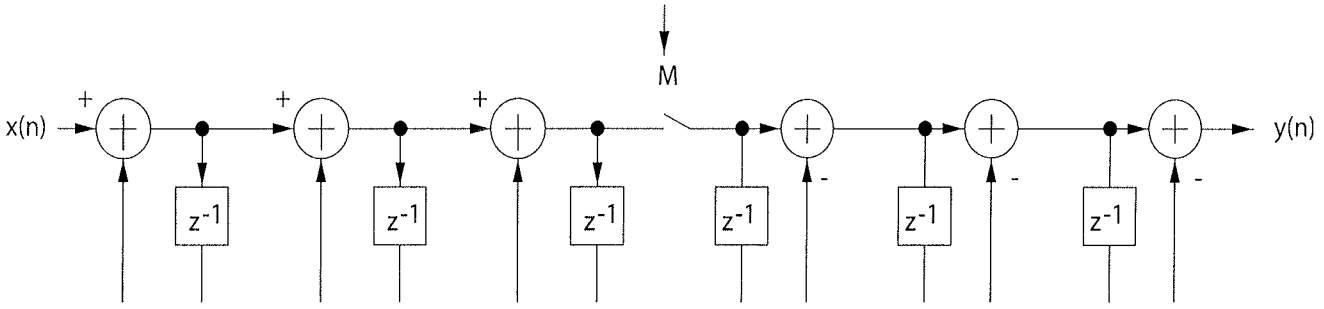

Figure 2: Signal processing block diagram of a 3rd order decimator

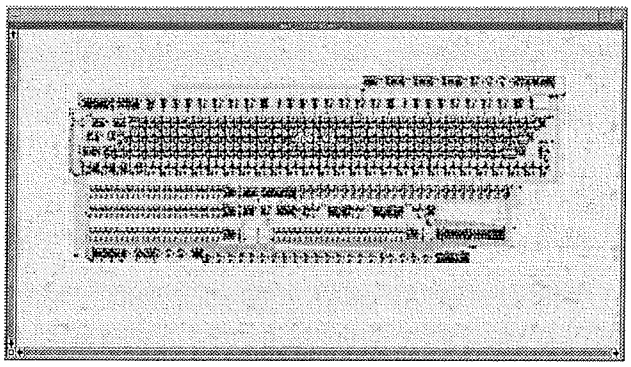

Figure 4: Layout of the decimator

4 Simulation and measured results

Σ–Δ A/D converter using 2nd order modulator optimized for noise performances /2/ and 3rd order decimator described in this article has been implemented in 0.6μm CMOS technology using f_{ovs}=4MHz according to the block diagram on figure 5. Time domain simulation of 1 bit 2nd order Σ–Δ modulator including kT/C and thermal noise sources of the S-C loop filter and making FFT on the bit stream (bs node on figure 5) gives $\frac{S}{N} = 96dB$ for M=256, which is slightly less than 16 bits in 8kHz band. The simulation results are presented on figure 6. 2 characteristics are presented lower, which does not include kT/C noise sources and the upper that includes all circuit noise sources.

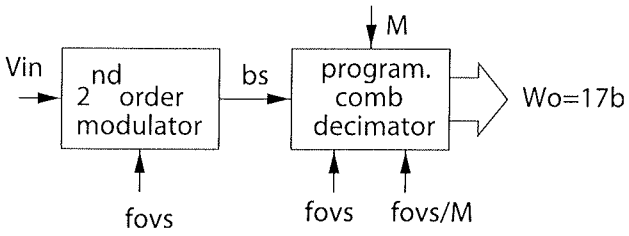

Figure 5: Block diagram of programmable A/D converter

Figure 7 shows transfer functions of a programmable comb decimator with M=256,128,64, which is used to attenuate out of band quantization noise of the bit-stream and to reduce sampling rate to f_s/M. To prove the behavior, a complete A/D converter was built in 0.6μm CMOS technology using systematic methodology to reduce switching noise and power consumption in comb decimator according to /1/. Power consumption and noise of the modulator has been optimized carefully, too. Figure 8 shows measured results of a complete A/D converter consisting of 2nd order modulator and programmable 3rd order decimator. Equal input signal was used for simulation of the modulator (see figure 6) and measurements. On the upper part of figure 8 M=128 is used and on the lower part M=64, that is why we have 1 bit difference in resolution. A factor of 2 difference can be observed between bandwidths of figure 6 and figure 8. This ratio is used for offset cancella-

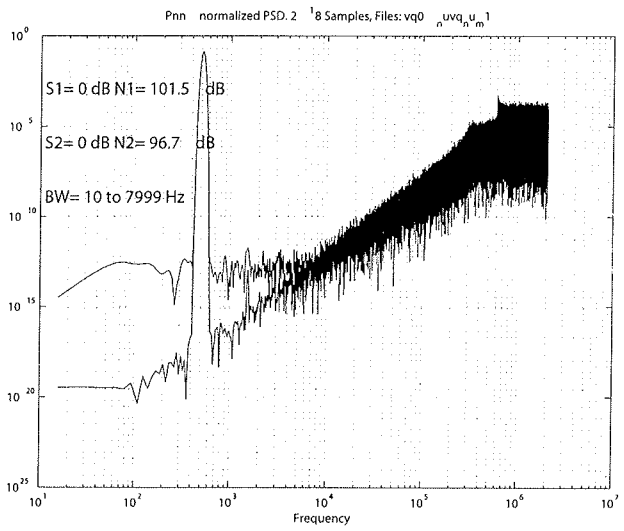

Figure 6: PSD of a bit stream

tion. It is evident that offset and 1/f noise components are highly attenuated. Current consumption of a complete A/D converter running with f_{ovs}=4MHz is less than 600mA at V_{sup}=5V. Measured switching noise observed on the substrate pin of a chip is much smaller (up to 5 times) compared to traditional standard cell approach.

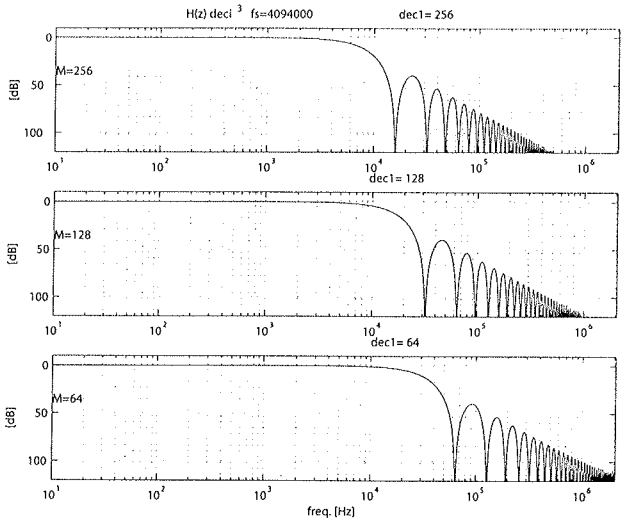

Figure 7: Programmable decimator frequency characteristics

5 Conclusions

Area and power consumption efficient programmable 3rd order comb decimator with very low switching noise has been implemented together with noise optimized 2nd order Σ–Δ modulator using 0.6μm CMOS technology. Several different implementations of a comb decimators have been analyzed. The IIR-FIR decimator architecture was selected because it is easy to implement, it is possible to

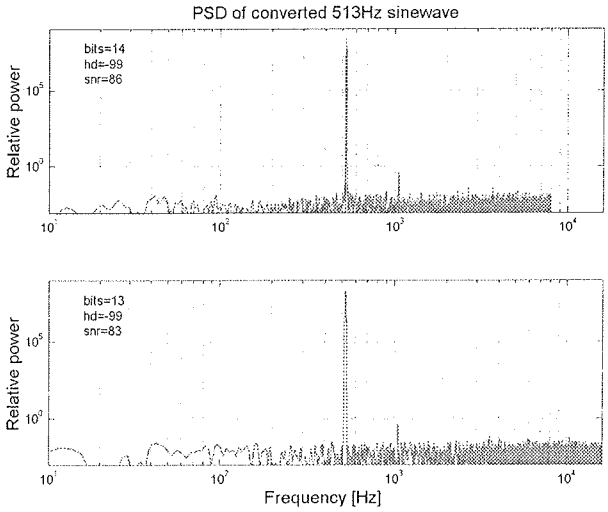

Figure 8: PSD of a measured sine wave

program decimation factor in a simple way, it occupies small silicon area and it is possible to use systematic method to reduce power consumption and switching noise. Measurements of implemented A/D converter show that it is possible to use it in a "low-noise" mixed-signal environment because of very low switching noise.

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DEVELOPMENT AND ANALYZIS OF FAST, POST-PROBE SILICON WAFER INKING ALGORITHMS

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Key words: Wafer prober, inker, inking algorithm, wafer map.

Abstract: Wafer probing is essential process in the semiconductor manufacturing. While performing several electrical tests on chips within the silicon wafer, we can determine devices that don't comply with the predefined electrical parameters. Such devices are usually promptly marked with an ink dot. Sometimes inking can't be performed while testing. For example: when the inker presence disturbs sensitive sensors integrated on the tested device. For that purpose special algorithm for post-probe inking is required. Such algorithm is marking bad dies while reading error data from the wafer map file. Three different approaches for algorithms are presented to solve this problem.

Razvoj in analiza hitrih algoritmov za naknadno označevanje testiranja na silicijevih rezinah

Ključne besede: Testna naprava za silicijeve rezine, naprava za označevanje s črnilom, označevalni algoritem, grafična predstavitev napak na silicijevi rezini.

Izvleček: Končno testiranje silicijevih rezin je pomemben proces v izdelavi polprevodnikov. Tu s pomočjo elektronskega testiranja ugotavljamo količino dobrih čipov na rezini. Tiste mikrosisteme, ki ne ustrezajo vnaprej določenim kriterijem, pa običajno sproti označimo s kapljico črnila. Vendar pa to ni vedno mogoče. Včasih že sama naprava za označevanje s črnilom povzroči velike motnje na občutljivih senzorjih mikrosistemov. Torej potrebujemo poseben program za krmiljenje testne naprave za silicijeve rezine, ki omogoča naknadno označevanje s črnilom. Razvili smo tri različne algoritme za tak postopek.

1. Introduction

Wafer probing is important activity in the process of finalizing semiconductor products. The only way to find out, if a particular chip on silicon wafer is functional, is to perform several electrical tests. Such tests can be performed only after all wafer production steps are finished. However sometimes it happens, that measured electrical parameters are not within the predefined tolerances. When this is the case, bad device must be marked. Quite common approach for this task is to use a small drop of ink for the mark. The most convenient time for inking is a time bracket before moving wafer probe card to the next device. In some cases direct inking is not possible. Inking can only be performed after entire wafer probing is done. For that purpose we developed application specific algorithm for wafer prober control.

The device structures on the chip are getting smaller and smaller on the other hand, 200mm wafers are already standard. This means that we are usually testing several thousand chips per wafer. While optimizing time for the electrical measurements, the time necessary for applying probe card depends on the wafer prober speed and in general can't be optimized due to mechanical reasons. When the test time is short compared to the probe card move, several thousand moves use significant amount of time. Therefore it might happen, that inefficient post-probe inking algorithm actually doubles the test time per wafer.

Post-probe inking is mostly applicable when:

- Presence of the inker disturbs integrated sensors on tested device.
- Adopting multiple probe cards for simultaneous testing of several chips at the same time and there is no possibility to use several inkers.
- Delayed inking is not possible because probe card is preoccupied by test and measuring equipment.
- We are testing very little dies with several pads, which makes inker proper access to wafer surface impossible.

Therefore three different approaches for wafer inking algorithms are presented to solve listed problems and further implementations are proposed.

2. Description of the testing and inking process

Although wafer probing is an important step in the semiconductor production, it does not mean we should use a lot of time doing it. Therefore all wafer manipulation and electrical measurement routines should be optimized for speed. Since the electrical tests are the only way to find out, if certain chip on the silicon wafer is fully functional, we have to test all of them. Figure 1 presents test probe with inker.

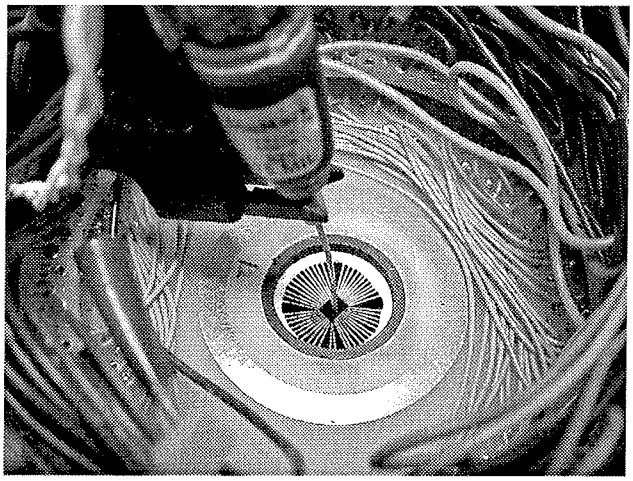

Figure1: Test probe with inker.

There are some methods to drastically increase testing speed. One is to test several chips at the same time. Drawback is, that we need very expensive test probes and several equivalent test stations. Due to high investment in expensive test stations economical aspect of this method is questionable. Another method is called consecutive fail monitoring. It is used to provide feedback information for determining problem areas. When they are determined we can test only the chips of the problem areas. However, such method is not very reliable and becomes quite unuseful, when additional trimming of chip parameters must be performed while testing.

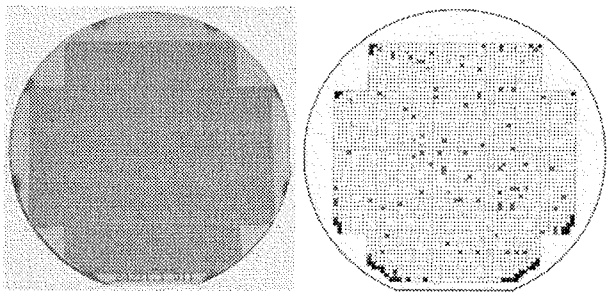

Figure 2: Silicon wafer and corresponding test wafer map.

Therefore it is reasonable to use simple, left to right and right to left test probe marching algorithm. It should be adopted to round shape and size of silicon wafers. Further it should also consider the pattern on the wafer (Figure 2). When we get to the end of the wafer, wafer test is completed and bad dies are inked. In case, when bad dies for some reason could not be inked directly we have three options:

- We can use a standard wafer map file for interface to the die-bonder. This method is called "inkless assembly". Drawback of this method is that it's not widely accepted as standard and that it has so called "first-die integrity" problem. It requires special marks on the wafer. These marks might be partially covered during wafer manufacturing and additional hardware and software is necessary to recognize such partially covered marks.
- We can use a special inking station outside the measuring wafer prober for offline inking, where the bad dies on the wafer are properly marked.
- We can use a standard wafer map file and slightly modified test probe marching algorithm with the same wafer prober setup data. This eliminates problems while matching physical locations on the wafer map file.

Last option can be used without any optimization. In this case, for N tested chips $2 \times N$ test positions must be selected per wafer. However, post-probe inking takes quite significant amount of time when chip test time becomes short, compared to time necessary for the test probe manipulation. And not at least, this method also significantly increases the mechanical wear of the expensive test equipment.

Usual yield per wafer varies from 60% to 90%. This fact offers some freedom for inking optimization since it is not necessary to ink every die on the wafer.

3. Inking process optimization

Inking process optimization is quite similar to the traveling salesman problem in which a salesman wishes to visit a number of cities and return to the starting point, while covering the minimum possible total distance on the way. Each city should be visited only once. If we represent testing algorithm from left to right and vice versa as a Hamiltonian graph (figure 3a), inking process might be introduced as a labeled spanning tree (Figure 3b). Vertices are presented as inked dies and we are trying to find an optimum spanning tree. Cayley's theorem says, that number of different labeled trees with n vertices is n^{n-2} and we usually have to ink a couple of hundred dies. However our problem is fortunately a little bit more specific.

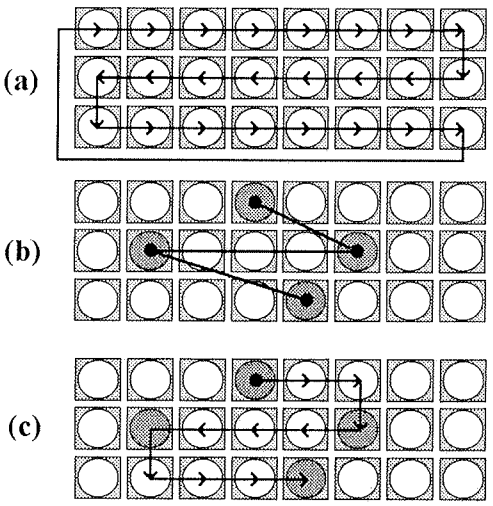

Figure 3: Wafer test probe marching description.

In other words, while inking we can actually decrease marching steps of the testing algorithm, by simply omitting some unnecessary traveling steps (figure 3c). Computer, that controls wafer prober input while inking, uses as input the same setup data as they are used for wafer prober while testing. The difference is, that optimized algorithm determines unnecessary marching steps and calculates appropriate offset moves to avoid unnecessary traveling. We will call this algorithm one pass inking optimization. In this case, time saving compared to $2 \times N$ marching algorithm, is considerable and compatibility with the marching algorithm for testing is preserved. This is, once again very important for achieving test and ink die integrity.

Figure 4 represents two typical wafer ink maps. Wafer ink map on the left actually represents best yield and wafer map on the right presents worst yield example. These two examples were chosen from several hundred tested wafers. We can see, that areas, requiring the most inking job are usually at the edge of the wafer. In the center of the silicon wafer, bad dies are more randomly distributed.

In worst yield case we can quickly realize, that our improved marching inking algorithm can't perform as well as in the best yield case. This is due to too many rows that need inking on the extreme left and right side. Therefore, the algorithm should be improved to perform better in such bad yield cases.

Adopting the feature, that areas requiring the most inking are actually on the edge of the wafer, we decided to ink the wafer in three phases. First phase is for inking dies on the left side, second on the middle and the third on the right side of the wafer. We will call this algorithm three passes inking optimization (figure 5).

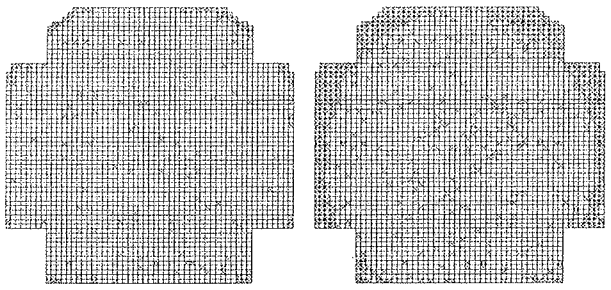

Figure 4: Best and worst-case inking wafer map.

Another problem that arises here is, how to efficiently group failed dies together? For that purpose we developed smart grouping and marking algorithms. Here we analyze three inking paths and use adoptable "near" and "far" functions. They are used to make a decision for grouping bad dies with questionable position. By questionable position we mean the position of all the dies that are geometrically between the two neighboring inking paths. It is quite evident, that when two dies are near each other, it is good to join them in the same group for post-probe inking. On the other hand, if two dies are far from each other, variable "far"

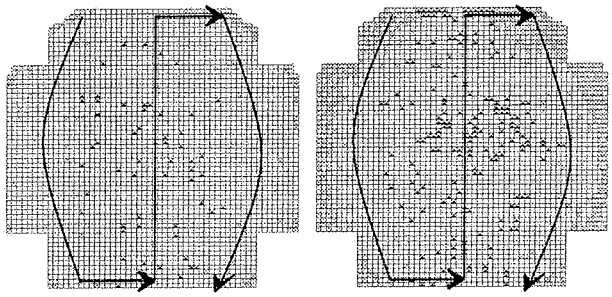

Figure 5: Best and worst-case inking wafer map for three passes inking algorithm.

actually represents our saved steps. "Near" and "far" parameters are variables, defined accordingly to the wafer size and number of dies to ink. This can be described with formulas (1), (2) and (3).

$$N = \frac{\pi r^2}{A} - \frac{2\pi r}{\sqrt{2A}} \quad (1)$$

$$N_b = (N * (1 - Y)) \quad (2)$$

$$Y = e^{-AD} \quad (3)$$

Where: N_b = number of dies to ink and N is number of dies per wafer,

$2r$ = wafer diameter,

Y = yield where A is die area and D is defect density.

Figure 5 presents such grouping for best and worst case yield from figure 4. Three different groups can be distinguished by different grayscales and different die patterns. The main direction of inker traveling is also indicated. Inker actually travels in steps left or right of main direction.

Both optimized inking algorithms are derived from wafer prober test setup files. Computer that controls wafer prober while inking uses HPIB communication protocol for test probe traveling and inker firing. However both algorithms were extensively tested for matching physical positions on wafer.

4. Inking process optimization evaluation

By using three passes inking algorithm we have additionally decreased extensive X marching for up to 66% in the best case. This algorithm is also efficient in previously mentioned worst-case condition, where we decreased inking time for 37%. Figure 6 presents timing diagrams for best and worst case times for all three inking algorithms. It is assumed, that worst-case $2 \times N$ inking algorithm takes 100% of time to finish.

The drawback is additional Y marching. However, additional Y steps are quickly annihilated by extensively decreased X

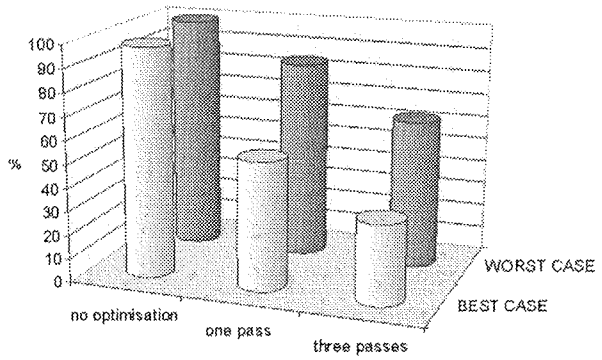

Figure 6: Timing diagram for all three different inking algorithms.

traveling. From mechanical wear of the wafer prober point of view, such algorithm is also much more convenient. This is because most of the job while testing and inking does the X-control machinery. So it's a good idea to increase load on the Y-control machinery while decreasing the load on the X-control machinery.

5. Conclusion

Post-probe inking of not functional chips is time consuming and increases maintenance cost of the expensive equipment. Therefore the effort for inkles testing is reasonable. Some test labs are already using wafer maps instead of ink drops for input to the die-bonders. Unfortunately this approach is probably several years away, to be a widely accepted standard.

There are approximately 20,000 wafer probers in the use worldwide. It is common, that almost every wafer prober has a different method for generating setup files, marking and marching algorithms. So, for achieving very important first-die integrity, old-fashioned inking is still quite common.

When inking for some reason can't be done promptly while testing, it is quite reasonable to use optimized wafer inking routines. When using three passes inking algorithm we can save up to 66% of inking time compared to $2 \times N$ inking algorithm. Beside faster wafer testing time we can also significantly decrease mechanical load on the expensive test equipment. As the wafer sizes grow, we may recommend further improvement to this algorithm by increasing the number of inking passes.

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MIDEM 2002 - CONFERENCE REPORT

38th International Conference on Microelectronics, Devices and Materials

The 38th International Conference on Microelectronics, Devices and Materials, MIDEM 2002, Slovenia, took place from the 9th to the 11th of October 2002, at the Hotel Klub in a small place Lipica, a green oasis in the middle of the Karst, and the home of the beautiful Lipizzaner horses. The official language of the conference was English. The conference was organized by MIDEM, which is the Society for Microelectronic, Electronic Components and Materials. MIDEM is a Slovenian chapter of the IMAPS and a Slovenian section of the IEEE. Conference sponsors were the Ministry of Education, Science and Sport of the Republic Slovenia, and HIPOT-HYB Production of Hybrid Circuits d.o.o., Šentjernej, Slovenia. The conference organizing committee was leading by Dr. Iztok Šorli.

This 38th conference continued the long tradition of annual international conferences organized by MIDEM. These conferences have always involved a large number of Slovenian and foreign experts working in these fields as well as attracting distinguished guest speakers. The number of papers and the number of participants at the MIDEM conferences from 1992 to 2002 are shown in figures 1 and 2. This year the conference attracted about 100 participants and visitors. The participants were from eleven countries: Slovenia, Finland, France, Germany, Ireland, Italy, the Netherlands, Poland, Romania, Czech Republic, and the USA. The Conference Proceedings were published prior to the Conference and contain 378 pages.

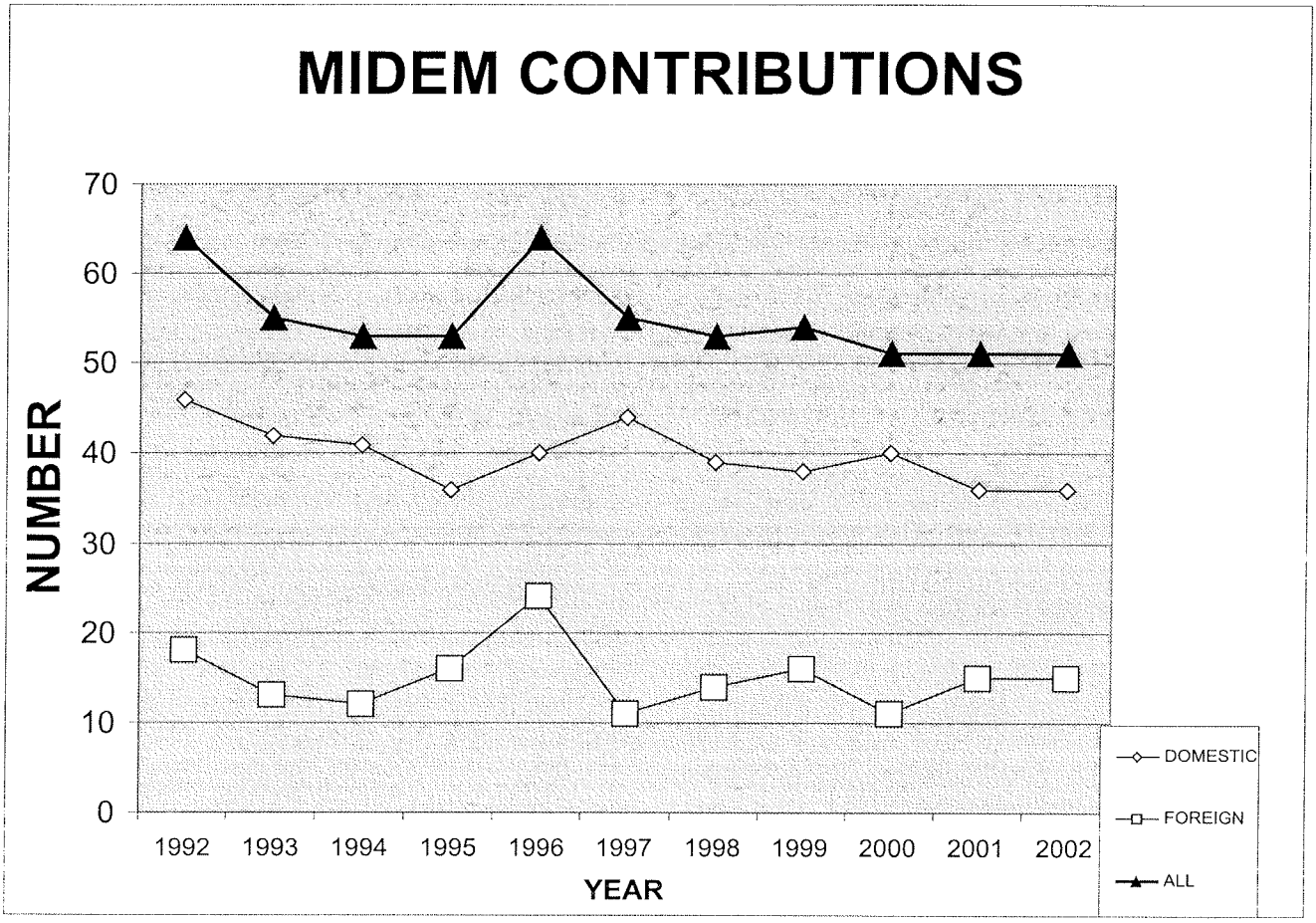
The conference was opened with short welcoming addresses from the conference chairperson and president of the MIDEM Society, Prof. Dr. Marija Kosec, and Dr. Aleš Glamus from the Ministry of Education, Science and Sport. The technical program began with an opening lecture entitled "Solution Synthesis of $Pb(Zr,Ti)O_3$ Ceramic Nano-powders", which was presented by Dr. Barbara Malič. This paper was a substitute for the invited paper of the conference entitled "Template Synthesis of One Dimensional Single and Multilayered Nanowires" because of the illness of the invited speaker Dr. Sima Valizadeh. Forty-seven regular and eight invited papers in the five sessions that included the workshop were presented during the three days from Wednesday to Friday. The presentations at the conference were grouped into the following sessions: Ceramics Metals and Composites; Integrated Circuits; Sensors; Optoelectronics; and Device Physics and Modeling.

Since 1998, workshops dedicated to each year's selected special topic have been added to the program of the MIDEM Conferences. This year the Department of Electronic Ceramics at the Jozef Stefan Institute and HIPOT-R&D organized a workshop entitled "Packaging and Interconnections in Electronics". The workshop was designed and chaired by Darko Belavič. The main focus of the workshop was to review and discuss topics on packaging, interconnecting, and assembling, which are important technologies in the electronic industry. The general technology trends in these segments are towards miniaturization, cost reduction, microsystems, integration, higher reliability, applications on the technology margins, ecologically friendly materials and processes, etc. There are also tendencies towards fast prototyping, new education programs, trans-institution cooperation, etc. Most of these aspects were presented and discussed in the workshop during the eight regular papers and seven invited papers. The invited papers were:

1. J. Ptak, "Business and Technology Challenges in Electronics Industry in the Early 21st Century"
2. H. Quinones, A. Babiarz, "Flip Chip, CSP and WLP Technologies: A Reliability Perspective"
3. P. Svasta, V. Golumbeanu, C. Ionescu, "Electronic Passive Components Training Activity- Demand for Performance Electronic Package Development"
4. J. Mueller, H. Griese, H. Reichl, K.-H. Zuber, "Lead-free Interconnection Technology and the Environment"
5. P. Collander, "Packaging and Interconnect for RF and Microwave"
6. L.J. Golonka, A. Dziedzic, J. Kita, T. Zawada; "LTCC in Microsystems Applications"
7. M. Hrovat, D. Belavic, M. Pavlin, J. Holc, "Diffusion-patterning: One of the Thick-film Interconnections Technologies"

Ljubljana, Nov.2002

Darko Belavič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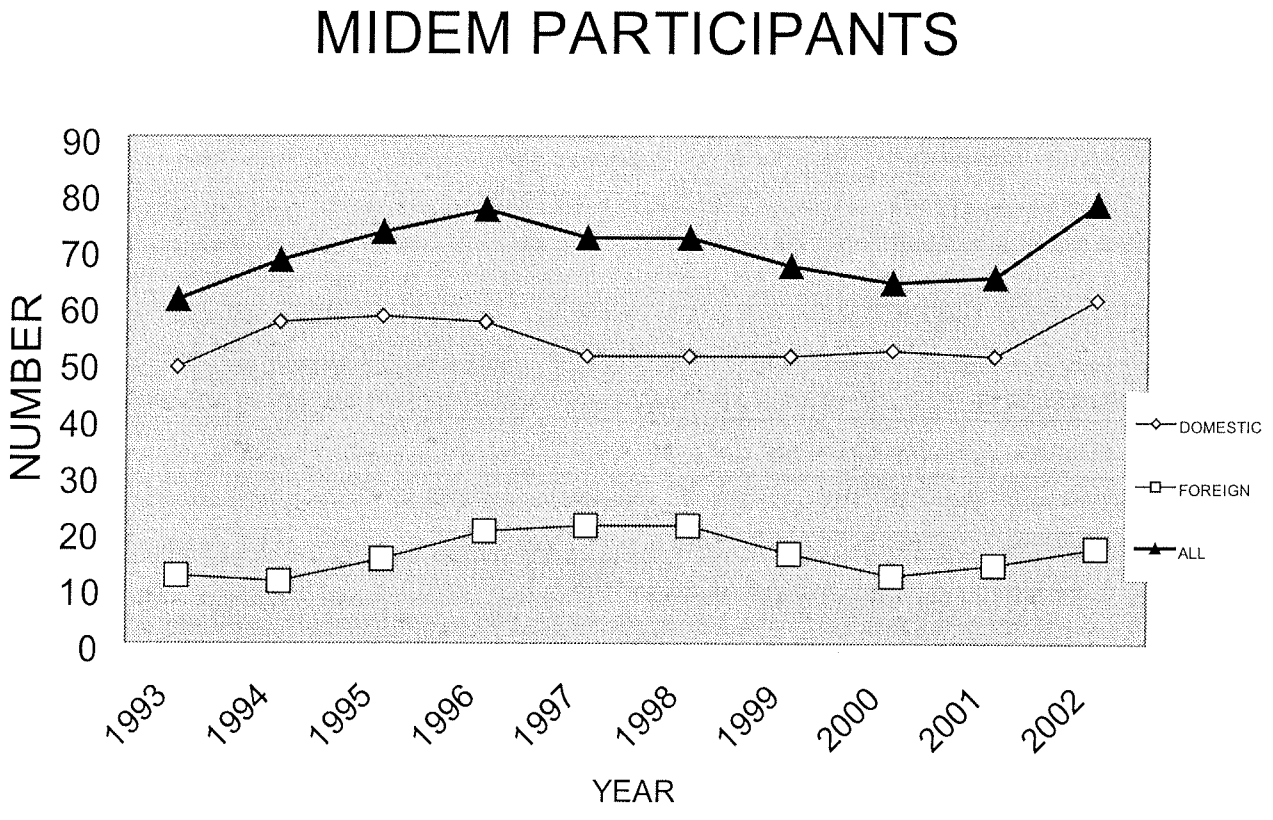
MIDEM PARTICIPANTS
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Informacije MIDEM
Strokovna revija za mikroelektroniko, elektronske sestavine dele in materiale

NAVODILA AVTORJEM

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