PLACEMENT AND ROUTING OF HIGH VOLUME ICs

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Abstract: A place and route tool is an integral part of a modern integrated circuit design environment. It is often that a custom circuit requires a large block of random glue logic for its operation. This paper introduces techniques for manual optimisation of area for blocks of random glue logic. An area reduction of 25 % to 40 % is achievable compared with the results of modern commercial place and route tools.

Nameščanje in povezovanje pri integriranih vezjih za množično proizvodnjo

Ključne besede: polprevodniki, mikroelektronika, IC vezja integrirana, proizvodnja množična, nameščanje, povezovanje, optimizacija površine vezja, geometrija logike nakljućne, geometrija celice brez mreže, orodje za analizo gostote

Izvleček: Orodje za nameščanje in povezovanje je običajno vključeno v moderno okolje za načrtovanje integriranih vezij. Pogosto vezja ASIC vsebujejo večje bloke povezovalne logike. Članek obravnava tehnike za ročno optimizacijo površine vezij povezovalne logike. Predstavljene metode omogočajo izdelavo blokov na 25% do 40% manjši površini kot moderna komercialna orodja za nameščanje in povezovanje.

1. Introduction

The area used for the interconnections in a large block of random glue logic designed for a traditional two level metallization process exceeds the effective area used by the cells. With the increased number of devices this ratio of channel area to cell area deteriorates. Ratios 2 to 3 in favour of the channel width are common. Assuming that the logic can not be optimised there are two common ways to decrease the block area: using a technology with better resolution and using a process with multiple levels of metallization. As the most cost-effective process was selected in the first place it is usually unacceptable to change the process during the layout design.

With the advent of dense processes and useful place and route tools integrated in the design environment a third solution does not seem obvious. With a convenient set of tools one can manually optimise the layout area better than the best place and route tools.

Gain in circuit area is the result of library optimisation, placement optimisation and routing optimisation. The task is labour intensive but for high volume ICs it is cost effective.

In the following text it is assumed that cells are placed in horizontal rows, metal1 (M1) is used for the horizontal wire segments and metal2 (M2) is used for the vertical wire segments as well as for wire segments connecting cell pins with the channel segments.

2. Library

Most commercial place and route tools require cells build with arbitrary grid. All pins must also be placed on the grid. With this constraints it is tedious to design cells and a couple of iterations required with a library conformance checking tool to complete a cell.

A faster grid-less approach is used in the design of optimised cells of the proposed method. Since each cell need not be expanded to the first grid point and less area is lost in on-grid placement of vias an average 10 % area gain is achieved in total area of all cells for a block. This may not look much with the channel area taking 2-3 times the cell area but the decreased width of the row of cells results in smaller width of the entire block.

The second advantage with the grid-less approach is the number of vertical passes through cells. This is increased by over 30 % for grid-less routing. This is a result of lesser constraints in via placement.

The third amelioration in the proposed library is a number of versions of each cell. The versions differ in the number of pins with via and M2, which are accessible from the channel. Observe a cell NAND2 on Figure 1, where all pins have vias (fig. 1a), on (fig. 1b) where only the output pin has vias, and a case with no vias (fig. 1c). As quite a few cells can be connected to the neighbouring cells using metal1 in the area used for the cells without wasting the space in the channel. This calls for some consideration in vertical placement of pins. Attention must also be paid to horizontal metal1 channels to as many pins of the cell as possible.

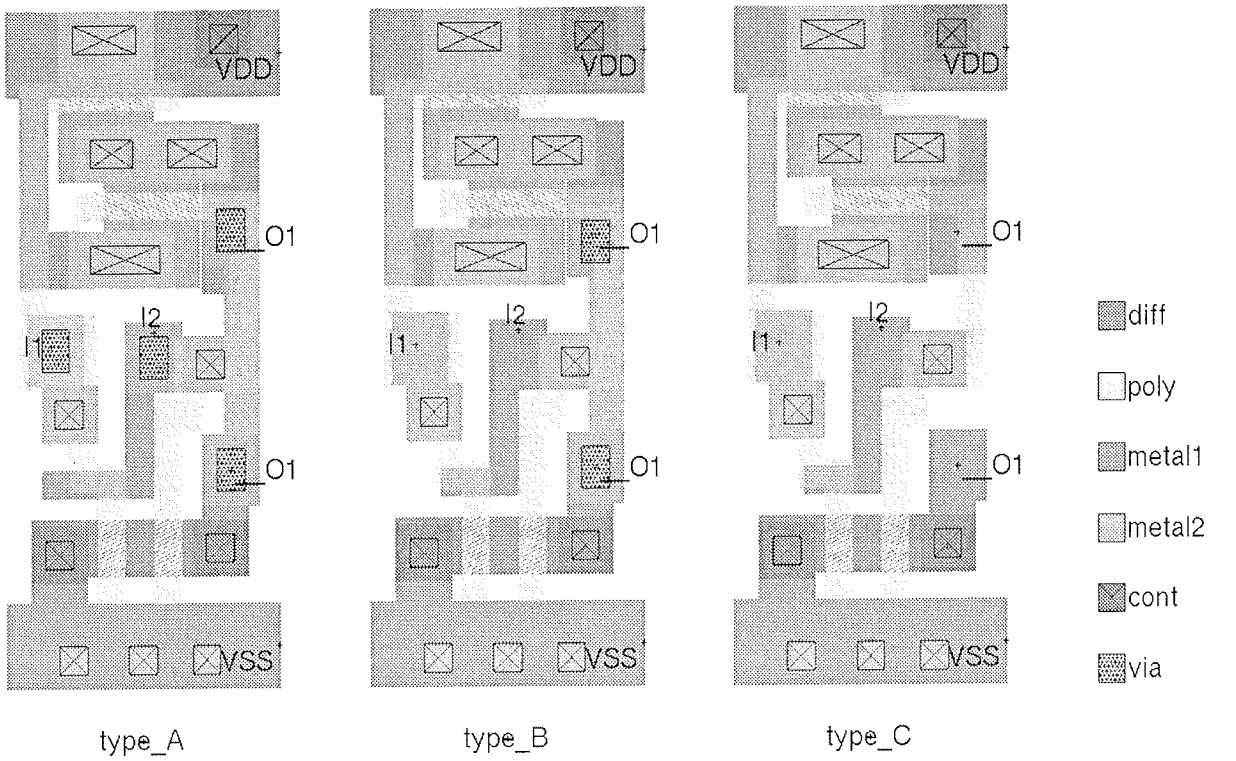

Figure 1: *Three versions of NAND2: (A) every pin is accessible from channel, (B) only output is accessible from channel, (C) all connections must be made in metal1. Well is omitted to improve readability.*

3. Placement

The placement is carried out in four phases: placement using some well known algorithms, visual placement evaluation, local optimisation with using alternative layouts of cells, and another visual placement evaluation.

A graphic density analysis tool (see fig. 2) displaying cell placement and the horizontal and vertical wire density used to evaluate both automatic phases. Entire block is split by a raster with grid spacing in both directions equal to the inter-row spacing. Various intensities of two colours are used to paint each segment depending on the number of wires passing. The number of passes through the row is evaluated for each segment and compared against the number of vertical wires that should pass this segment. The third colour is used to emphasise the segments which lack vertical passes through cells.

One can set a number of parameters with a typical placement tool /1/ to change optimise the placement according to the requirements of the task at hand. A configuration with an appropriate ratio between a small sum of horizontal tracks and a small number of vertical congestions is selected alternately using placer and density analyser. As the tool occasionally produces unacceptable results after minor changes to the set-up parameters the results of the global placement stage are evaluated with the density analyser.

In the local optimisation phase of placement a trade off between wire length increase and number of nets made of metal1 only is made. Converting a few nets to metal1 in the areas of horizontal congestion saves a number of tracks, which decreases the block size even though the overall wire length may not be optimal. Local optimisation is made by changing cell positions and swapping cells (type A) with versions where less metal2 is used (type B/C). Besides saving tracks (1.e. channel area) this increases the amount of vertical metal2 passes, which may cross the area thus improving the vertical congestions. This also decreases the number of feed-through cells, which need to be inserted to feasibility of routing.

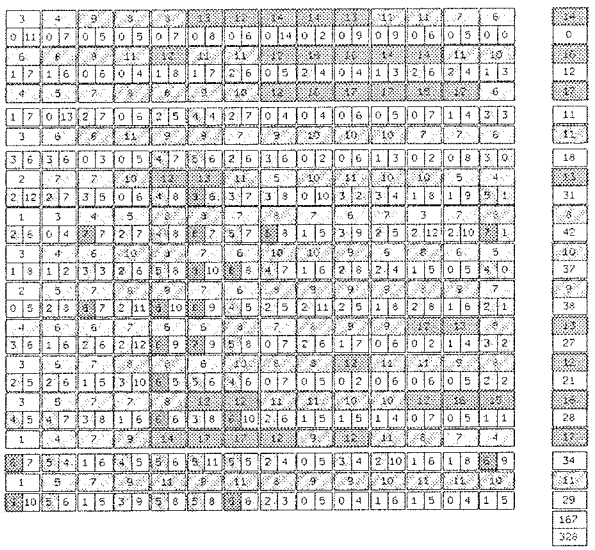

Figure 2: *Density of a circuit*

After placement evaluation with the density analyser manual optimisation of a few critical congestions can improve the placement in a reasonable amount of time to obtain another 5% gain in the block area.

4. Routing

Manual routing can be performed efficiently with a couple improvements in the wiring capabilities of the layout tool /2/. Starting or ending a wire on a label of the current net when a button is pressed close to the label and the obstacle avoiding ability when wiring through a row of cells are in need. A vertical grid is imposed on the channel to improve the quickness of routing.

The routing is started with sorted nets, which can be wired entirely in M1. The additional cells of type A are swapped for cells of type B/C to add vertical passes. Next, long horizontal segments are routed close to the supply rail of the cell rows. This improves compressibility of the channel. Lastly, all other nets a routed sorted by their length, longest first.

When all the nets are connected and the circuit proves to be LVS clean a channel optimisation is started. The horizontal congestions in each channel are identified and improved in the following ways:

- with large distributed nets a horizontal segments can be moved to other channels with no vertical passes used,
- by a horizontal segment being moved a couple of channels away to a non-congested area because of additional vertical passes resulting from metal2-less cell swap,
- by swapping the tracks and moving the contacts one can wire a net entirely in M2.

This actions decreases the worst number of tracks in a channel by 10% to 20%.

The channel compression is the last step in the routing process. This operation is also performed by most routers. Some tools also attempt contact moving to improve compression but manual inspection of critical areas with some track swapping can shrink the cannel an additional 3% to 5%.

5. Conclusions

Cell design in area optimal layout of digital integrated circuits with good metal1 inter-cell connectivity and without metal2 pins can improve block area in two ways: horizontal tracks are saved in the channel and fewer feed-through cells are needed for good vertical connectivity. The local placement optimisation for a metal1 inter-cell connection is more area efficient the minimum wire length. Interactive routing yields smaller block areas and is a valid alternative for very high volume ICs.

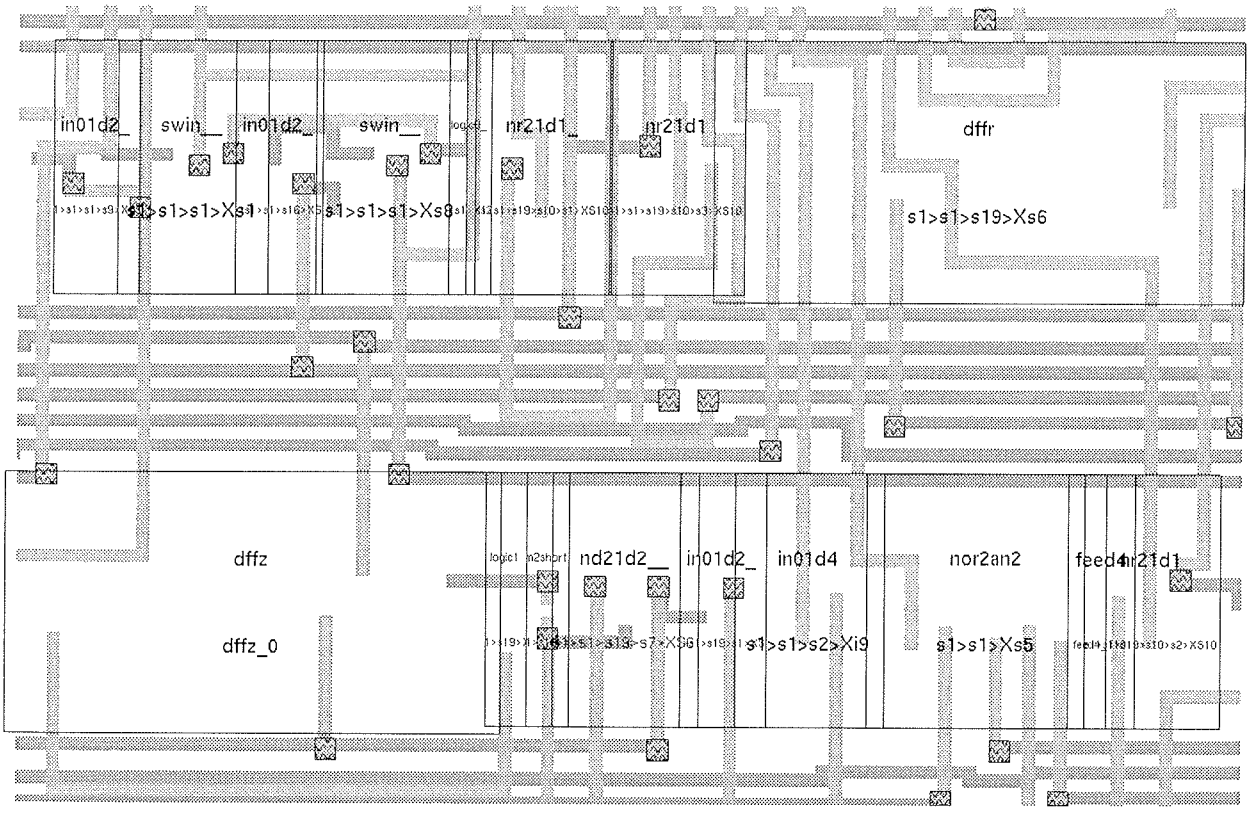

Figure 3: A closer look at the manual wiring.

References

/1/ Ren-Song Tsay and Ernest Kuh, "Proud 1.0: A Package for High Complexity VLSI Circuit Placement", *Elect. Res. Lab. Report*, University of California, Berkeley, 1989

/2/ R. N. Mayo et al, "1990 DECWRL/Livermore Magic Release"

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