NOISE BEHAVIOR OF SC CIRCUITS

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ABSTRACT: Noise behavior of *SC* circuits is analyzed in 'z' domain using simplified noise models for *MOS* switches and operational amplifiers. General mathematical description of *SC* circuit is upgraded by noise properties. Technique for analyzing of noise contributions of each individual noise source and also of spectral noise density of complete *SC* circuit is presented.

Šumne lastnosti vezij SC

KLJUČNE BESEDE: SC vezja, stikala MOS, lastnosti šumne, analiza, porazdelitev šuma, izvori šuma, gostota spektralna, gostota šuma, šumi termični, šum vzorčeni, SC integrator

POVZETEK: Z enostavnimi modeli stikal *MOS* in operacijskih ojačevalnikov so bile analizirane šumne lastnosti vezij *SC* v prostoru stanj. Splošnemu opisu vezij *SC* z diferenčnimi enačbami so bile dodane še šumne lastnosti. V članku je prikazana analiza porazdelitve šuma glede na posamezne šumne izvore kakor tudi spektralna gostota šuma celotnega vezja.

1. Introduction

Noise properties of analog building blocks is important parameter for design of analog systems on the silicon. By decreasing of noise floor of analog circuits the dynamic range is increased and from this view it is very important to reduce the noise of each building block. Noise of SC circuits is analyzed in this paper. For this purpose simplified noise models are prepared and are used in topological description of SC circuit. Noise voltage of each noise source is transferred to the output of SC circuit by its own transfer function. The 'z' domain analysis describes the sampled and held noise, which dominates in the signal frequency range $(f < \frac{f_s}{2})$. Complete behavior of SC circuits is described by topological matrix equations.

2. Basic Noise Models

Basic building blocks of *SC* circuits are switches, capacitors and operational amplifiers and main noise sources are operational amplifiers and switches. There are two basic mechanisms of noise generation:

- wide band noise
- sampled noise

Signals in *SC* circuits are sampled and stored in capacitors. In many cases this is the reason for smaller wide band noise compared to the sampled noise /2/. Sampled noise is divided into two groups:

thermal noise of MOS switches

noise of operational amplifiers.

Thermal noise of *MOS* switches and noise of operational amplifiers (thermal and 1/f noise) is sampled to individual capacitors and transferred to the output of *SC* circuit by its own transfer function. In many applications 1/f noise is eliminated by processing of direct and delayed signal at the same time /3/.

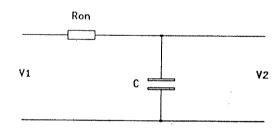


Fig. 1: Closed switch and corresponding capacitor

This allows simplified noise modeling of basic noise sources. Thermal noise of closed switch is sampled and stored in appropriate capacitor, and *RMS* voltage of such simple *RC* circuit shown in fig. 1 is /1/:

$$\overline{V_2^2(t)} = \frac{KT}{C} \tag{1}$$

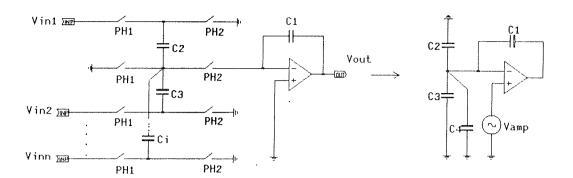


Fig. 2: n - input integrating stage and corresponding schematic at phase ϕ_2 .

where K is Boltzmann constant, T absolute temperature and C capacitance. For noise modeling of SC integrator the equivalent noise resistance R_{eq} of operational amplifier is used.

$$R_{eq} = \frac{\overline{v^2(t)}}{4KT\Delta f} = \frac{S_{amp}(f)}{4KT}$$
 (2)

where $S_{amp}(f)$ is spectral noise density of operational amplifier. This simplified model can be generalized for n - input integrating stage in clock phase φ_2 as shown in fig. 2.

Total thermal noise of the operational amplifier in integrating stage is given by:

$$V_{\text{.int}}^{2}(f) = \frac{KT}{C_{1} + C_{2} + ... + C_{i}} = \frac{KT}{\Sigma C_{i}}$$
 (3)

where $\sqrt{l}_{int}(f)$ is *RMS* noise voltage of integrating stage.

Top frequency for noise of integrating stage is defined by integrating capacitor and equivalent noise resistance of operational amplifier:

$$f_{\rm t} = \frac{1}{2\pi C_1 R_{\rm eq}} \tag{4}$$

Capacitors in *SC* circuits have defined ratio to the integrating capacitor so equation 3 can be transformed to:

$$V_{\text{int}}^{2}(f) = \frac{KT}{C_{1}\left(1 + \frac{C_{2}}{C_{1}} + \frac{C_{3}}{C_{1}} + \dots + \frac{C_{i}}{C_{1}}\right)} = \frac{(5)}{2\pi f_{1} KTR_{eq}}$$

where $\gamma_i = \frac{C_i}{C_1}$

3. Topological description

By using simplified noise modeling mentioned above, noise analysis of complex *SC* circuits can be performed.

Differentional equations transformed into the 'z' domain describe signal transfer into the SC circuits. *n* - stage circuit can be described by the following matrix equation:

$$||A(z)|| \cdot ||V_n|| = ||N|| \cdot \lambda_{inp}(z) \cdot V_{vh}$$
 (6)

Upper equation is valid for sampled signals and for equal duration of both phases of clock signal. Symbols in equation 6 are as follow:

| | | A(z) | | ... matrix of circuit coefficients,

 $|V_n|$... vector of the voltages on the output

of each integrator,

| | N | | ... vector of the input terminals,

 $\lambda_{inp}(z)$... input coefficient,

V_{inp} ... input voltage.

Number of the input terminals is defined by vector |N|. This noise analysis is limited on one input and on one output terminal so vector |N| has the following form:

$$||N|| = \begin{vmatrix} 1\\0\\0\\0 \end{vmatrix}$$
 (7)

Noise analysis of SC circuits is performed by grounded input $(V_{inp} = 0)$ and by adding matrix describing noise sources /4/. Equation 6 is therefore modified:

$$||A(z)|| \cdot ||V_n|| = ||B(z)|| \cdot ||V_{amp.n}|| + ||C(z)|| \cdot ||V_{sw.n}||$$
 (8)

where

... matrix of circuits coefficients describing noise transfer from each

operational amplifier,

... vector of the noise voltages of the operational amplifiers,

... matrix of circuits coefficients describing noise caused by switches and sampled on capacitors and

 $|V_{sw,n}|$... vector of the noise voltages sampled on the groups of capacitors.

Noise behavior of n - stage SC circuit is described by equation 8. Two dominant noise sources are in each integrating stage - the first is operational amplifier noise and second are the switches causing the sampled noise voltage on the same capacitors. Decomposition of the upper matrix equation gives the group of 2n linear equations for n - stage circuit. The noise voltage on the output of circuit is calculated for each uncorrelated noise source by solving of this group of equations. The transfer function from each noise source to the output is defined by this procedure. We have assumed a superposition theorem so only one noise source is active at a time and other are forced to zero. This is the reason for 2n matrix equations. Vector of noise voltages of operational amplifiers have for n - stage circuit the following form:

Noise transfer from each operational amplifier is defined in matrix |B(z)|. Order of this matrix is $n \times n$ and all nondiagonal coefficients are zero.

$$||B(z)|| = \begin{vmatrix} b_1 & 0 & 0 & 0 \\ 0 & b_2 & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & b_n \end{vmatrix}$$
 (10)

Coefficients b_1 , b_2 ... b_n describe noise transfer from corresponded operational amplifier to the output of the circuit. All operational amplifiers except the last amplifier are active by noise transfer to the output of SC circuit in one phase. Only the last amplifier transfer the noise to the output of SC circuit in both phases of clock. This is the reason for special treatment of coefficient b_n :

$$b_{n} \cdot V_{amp,n} = \left| \left| b_{n,1} b_{n,2} \right| \cdot \left| \left| V_{amp,n1} \right| \right|.$$
 (11)

Vectors of noise voltages on individual groups of capacitors have the following form:

$$\left| \begin{array}{c} \left| V_{sw1} \right| \\ \left| V_{sw.n} \right| \\ \left| (1) \right| \\ \vdots \\ 0 \\ 0 \end{array} \right| \left| \begin{array}{c} \left| V_{sw1} \right| \\ 0 \\ \vdots \\ 0 \\ 0 \end{array} \right| \left| \left| V_{sw.n} \right| \\ \left| (2) \right| \\ \vdots \\ 0 \\ 0 \end{array} \right|$$

$$\left| \left| V_{sw,n} \right| \right|_{(n)} = \left| \begin{array}{c} 0 \\ 0 \\ 0 \\ 0 \\ \cdot \\ V_{sw1} \\ V_{sw2} \end{array} \right|. \tag{12}$$

Individual group of capacitors consists of all capacitors at each integrating stage. It is important to take into account the transfer function from each capacitor group to the output of SC circuit in both phases. Vectors of noise voltages caused by switches and matrix ||C(z)|| are defined for ϕ_1 and ϕ_2 . Matrix ||C(z)|| have the following form:

$$||C(z)|| = \begin{vmatrix} c_{1,1} c_{1,2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & c_{2,1} c_{2,2} & 0 & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & c_{n,1} c_{n,2} \end{vmatrix}.$$
 (13)

4. Results

All coefficients needed for calculation of individual spectral noise density are given by solving of 2n systems of matrix equations. These coefficients are the voltages on the output of the circuits caused by individual noise sources. Simplified description of such solutions is presented by the following equations:

where the voltages of individual noise sources ($V_{amp.1}$, ... $V_{sw.n}$) are multiplied by their own transfer function ($F_{amp.1}$, ... $F_{sw.2}$). Individual spectral noise density are calculated from equation 14. For this purpose spectral noise densities of noise sources are used and transfer function is multiplied by its own complex conjugated value. Spectral noise density of complete SC circuit is defined:

$$S_{n} = \sum_{amp,n=1}^{sm,n=n} S_{n,amp,n} + \sum_{sw,n=1}^{sw,n=n} S_{n,sw,n}$$

$$(15)$$

Noise properties of individual noise sources transferred to the output are very important for improved design of *SC* filters. For optimal design the contribution of each noise source should be in the same range. The noise contribution of the switches can be decreased by larger capacitor unit, noise contribution of the operational

amplifiers can be smaller if operational amplifiers have both lower thermal noise and lower unity gain bandwidth.

5. Design example

Matrix equation for noise analysis of *SC* circuits was used for noise analysis of low pass Ladder filter from fig. 3

Three matrix equation describing noise properties of operational amplifiers and additional three for noise of switches was defined for this circuit:

$$\begin{vmatrix} a_{1} & a_{2} & 0 \\ a_{4} & a_{5} & a_{6} \\ 0 & a_{8} & a_{9} \end{vmatrix} \cdot \begin{vmatrix} V_{1} \\ V_{2} \\ V_{3} \end{vmatrix} = \begin{vmatrix} b_{1} & 0 & 0 \\ 0 & b_{2} & 0 \\ 0 & 0 & b_{3} \end{vmatrix} \cdot \begin{vmatrix} V_{amp,n} \\ V_{amp,n} \end{vmatrix} + + \begin{vmatrix} c_{1,1} & c_{1,2} & 0 & 0 & 0 \\ 0 & 0 & c_{2,1} & c_{2,2} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{3,1} & c_{3,2} \end{vmatrix} \cdot \begin{vmatrix} V_{sw,n} \\ 0 & 0 & c_{2,1} & c_{2,2} & c_{3,2} \end{vmatrix}$$
(16)

where the coefficients have the following expressions:

$$a_{1} = z \cdot (1 + \lambda_{2}) - 1 \qquad \lambda_{1} = \frac{C_{2}}{C_{1}} \quad \lambda_{2} = \frac{C_{4}}{C_{1}}$$

$$a_{2} = \lambda_{3} \qquad \qquad \lambda_{3} = \frac{C_{3}}{C_{1}} \quad \lambda_{4} = \frac{C_{6}}{C_{5}}$$

$$a_{4} = -\lambda_{4} \cdot z \qquad \qquad \lambda_{5} = \frac{C_{7}}{C_{5}} \quad \lambda_{6} = \frac{C_{9}}{C_{8}}$$

$$(17)$$

$$\begin{split} a_5 &= z - 1 & \lambda_7 = \frac{C_{10}}{C_8} \\ a_6 &= -\lambda_5 \cdot z \\ a_8 &= \lambda_6 \\ a_9 &= z \cdot \left(1 + \lambda_7\right) - 1 \\ b_1 &= -\left[z \cdot \left(1 + \lambda_1 + \lambda_2 + \lambda_3\right) - 1\right] \\ b_2 &= -\left[z \cdot \left(1 + \lambda_4 + \lambda_5\right) - 1\right] \\ b_3 &= b_{31} + b_{32} & b_{31} = -\left(z - 1\right) \quad b_{32} = -\left(\lambda_6 + \lambda_7\right) \cdot z \\ c_{11} &= z \cdot \left(\lambda_1 + \lambda_2 + \lambda_3\right) & c_{12} &= \left(\lambda_1 + \lambda_2 + \lambda_3\right) \\ c_{21} &= -z \cdot \left(\lambda_4 + \lambda_5\right) & c_{22} &= \left(\lambda_4 + \lambda_5\right) \\ c_{3.1} &= -z \cdot \left(\lambda_6 + \lambda_7\right) & c_{32} &= \left(\lambda_6 + \lambda_7\right). \end{split}$$

RMS noise voltage on the outputs of the operational amplifiers are calculated for first two amplifiers for only one clock phase and for last amplifier for both clock phases:

$$b_{3} \cdot V_{amp,3} = b_{31} \cdot V_{amp,31} + b_{32} \cdot V_{amp,32}$$
 (18)

$$V_{amp,31}^{2} = \frac{2\pi f_{t} \text{ KT R}_{eq}}{1 + \lambda_{1} + \lambda_{2} + \lambda_{3}} \quad V_{amp,2}^{2} = 2\pi f_{t} \text{ KT R}_{eq}$$
 (19)

$$V_{amp,31}^{2} = \frac{2\pi f_{t} \text{ KT R}_{eq}}{1 + \lambda_{6} + \lambda_{7}} \quad V_{amp,32}^{2} = 2\pi f_{t} \text{ KT R}_{eq}.$$
 (20)

From matrix equation 16 six results are obtained, which represent noise contribution of each amplifier and of each group of switches. The following parameters were used for this analysis:

clock frequency of SC circuit ... f=1024 kHz top frequency of operational amplifier ... $f_f=5$ MHz

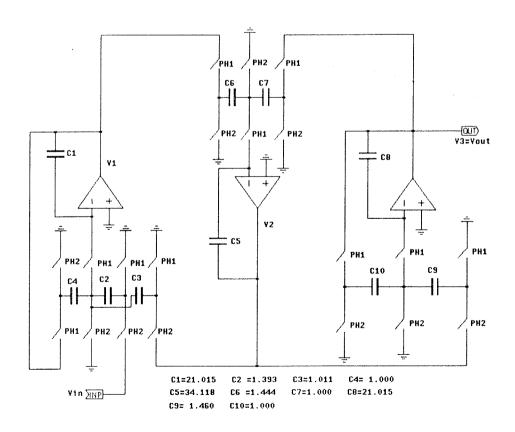


Fig. 3: Low pass Ladder filter (n=3).

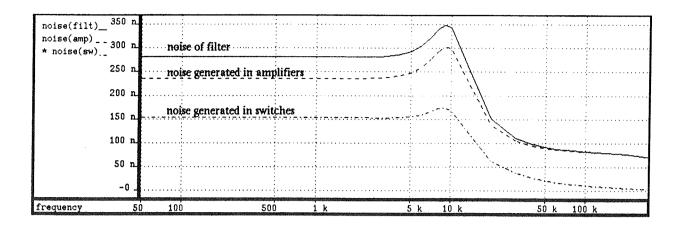


Fig. 4: Noise properties of low pass filter.

thermal noise of operational amplifier ... $u_n = 60 \frac{\text{n V}}{\sqrt{\text{Hz}}}$

unity capacitor ... $c_u = 0.5 \text{ pF}.$

Fig. 4 presents spectral noise density of low pass filter. This filter was realised in high performance integrated telephone set with codec. The measurement in the system prooved good matching to calculated values.

6. Conclusion

The method for noise analysis of *SC* circuits is presented. For this purpose the topological description of main noise sources is added to the general matrix equation. Noise analysis is performed in 'z' domain. Resulted noise voltages are after this procedure transformed to *time* domain. Spectral noise density are calculated for each noise source contribution and for final result the spectral noise density of each individual noise source is summarized.

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