INTEGRAL NONLINEARITY DETERMINED BY SELECTION ORDER OF CURRENT ARRAY UNITS IN DA CONVERTERS

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Key words: CMOS D/A converter, current array, bits-selection-order, thermometric converter

Abstract: This paper analyses characteristic of switching-scheme for the curent source array that was used in 14-bit CMOS DA Converter. It presents 8-bit thermometric bits-selection-order (BSO) analysis results, where the single bit current source is constructed as a group of two equal cell-units. The BSO order algorithm varies position of the group, while the current-cells inside the group are always placed simetrically over the center of the layout area. Bit-selection-order value is a decimal code value of the position selection. The final solution is compared with straight horizontal and straight vertical BSO with different error distributions from which posible integral nonlinearity (INL) of the final product, can be estimated. The analysis of error distribution influence on INL further demonstrates that with bits mixed selection-order INL error is always below 0.05 LSB when average current error is below 1%.

Integralna nelinearnost določena z zaporedjem izbire tokovih virov v DA pretvornikih

Kjučne besede: CMOS D/A pretvornik, polje tokovnih virov, zaporedje preklapljanja bitov, termometričen pretvornik

Izvleček: Ta članek obravnava karakteristiko preklopne sheme za polje tokovnih virov, ki je bilo uporabljeno v 14-bitnem CMOS digitalno - analognem pretvorniku. Predstavljeni so rezultati analize 8-bitnega termometričnega zaporedja izbire (BSO), kjer je bitni tokovni vir zgrajen kot enota dveh enakovrednih osnovnih tokovnih celic. BSO algoritem spreminja mesto bitnega tokovnega vira, medtem ko sta osnovi tokovni celici vedno postavljeni simetrično, glede na center geometrije polja tokovnih virov. BSO vrednost predstavlja decimalno kodo izbire mesta bitnega tokovnega vira. Integralna nelinearnost (INL) končnega izdelka je ovrednotna z različnimi porazdelitvami napake (Slika 3), glede na vodoraven (Slika 1) in navpičen (Slika 2) BSO algoritem. Analiza vpliva porazdelitve napake na INL kaže, da je INL napaka pri mešanem BSO (Slika 4) vedno pod 0,05 LSB, če je povprečna tokovna napaka pod 1%.

1. Introduction

Low integral nonlinearity (INL) in high-bit-count DA Converters is dificult to accomplish with resistor-strings, R2R converters, or binary-weighted current sources /6, 1, 3, 5, 2/. Studies and measurenments indicate that there are non-constant process parameters and region gradient over silicon wafer. In our research we used aproach of two current arrays where each of the array was controlled with thermometer coders.

It is therefore our goal to search for the most suitable organisation of an array, number of current units in one step group and, on the most suitable switching-scheme for 8-bit current array.

As already explained in /4/, to suppress the linear error, the current step must be split into more than one current units per-step. To minimize the silicon area, only two current units per one unit group were used and placed symetrically over center of the array. Considering last statement we have 2 x 256 current units.

Because of technology isues, seperated functional blocks (sources, switches an selectors) would result in an increased circuit area. In our research our goal is to combine all functions in one cell - current logic block (CLB) cell /8/.

CLB cells are composed of:

- current source with cascode devices,
- switches to one of two current outputs and
- digital selection circuit, which determines the state of the switches from horizontal and vertical control signals.

Proportion of CLB dimensions is set to 1:10, so the shape of current array was chosen to be 8 x (32 x 2) with additional columns for biasing circuit.

2. First accession

Two reference selection-orders of the BSO were used in analysis:

- horizontal selection-order (Figure 1) and
- vertical selection-order (Figure 2).

For both reference principles, unit group consists of two CLB cells, placed symmetrically to center.

To find proper solution, we have to cosider which effects have influence on the resulting INL error and how does the gradient of the process parameters effect the INL error (Figure 3 /7/).

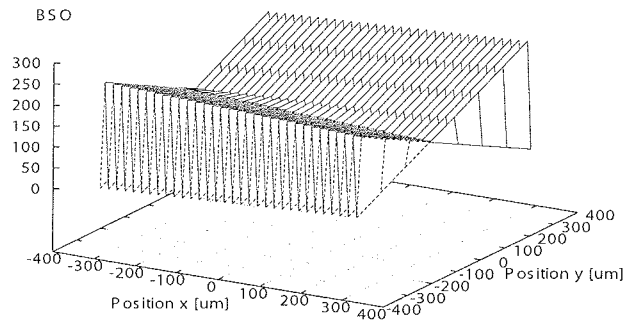

Figure 1: Horizontal selection-order.

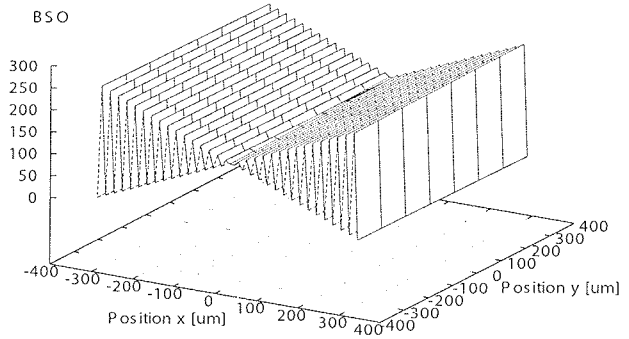

Figure 2: Vertical selection-order.

All the results are found in Figure 5. It is evident that all even order distributions yield zero INL error, as we already assumed when splitting step units in two current cells (CLB's). As can be seen in Figures 3.c and 3.g for 1-D parabolic error distribution INL error results (Figures 5.c and 5.g) are resembling. The main difference is that in Figure 5.g, vertical 1-D error distribution, the ratio between horizontal an vertical BSO is four times higher than in horizontal 1-D distribution (Figure 5.c) which corresponds to CLB array shape 8 x (32 x 2).

Superior results are achieved for vertical selection-order. Selected step order goes more frequently from one edge to the other vertically (8 steps) than horizontally (32 steps) which means that final solution will include best results if selections are distributed through all array area as frequently as possible. Simmilar results are presented in Figure 5.e.

3. Proposed solution - mixed selection-order

To build more flexible BSO algorithm, it is possible to cover more complex parameters gradient over silicon as well as taking into account any CLB array shape. The BSO anal-

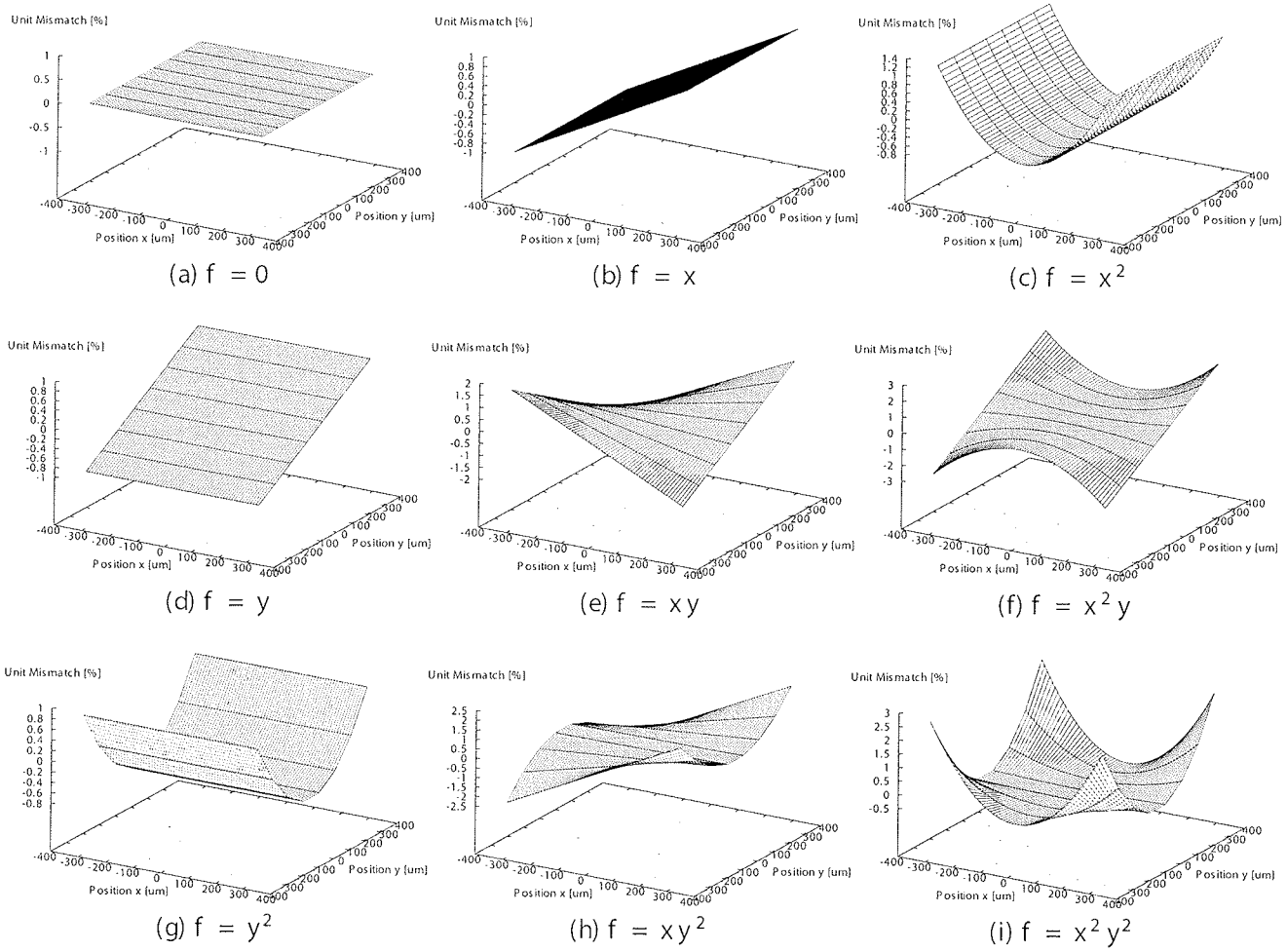

Figure 3: Error distribution through array area.

ysis indicates that the most encauraging results can be achieved by mixing horizontal and vertical bits order. In our research, we proposed bits mixed selection-order (BMSO), as shown in Figure 4.

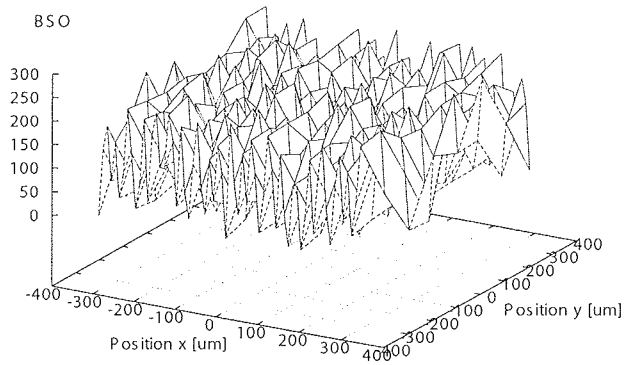

Figure 4: Mixed selection-order.

Using this approach, it is therefore evident that the random parameter distributions are covered much better, even with only two unit cells building the MSB group.The results of INL errors from Figure 5 show that for most common errors (Figure 5c, 5g and 5i), INL error is always below 0.05 LSB when average current error does not exceed 1% thermometric active area (Figure 3).

4. Conclusions

Theoretical analysis supported by the predicted and realistic distribution of the process parameters over the silicon area was implemented on integrated digital to analog converter, costructed by the thermometric 8-bit subblock. After the measuring, results will determine resolution for the overall high resolution D/A. Through we can conclude that the complete converter can be covered only by thermometric subblocks, probably including a less complicated autocallibration block.

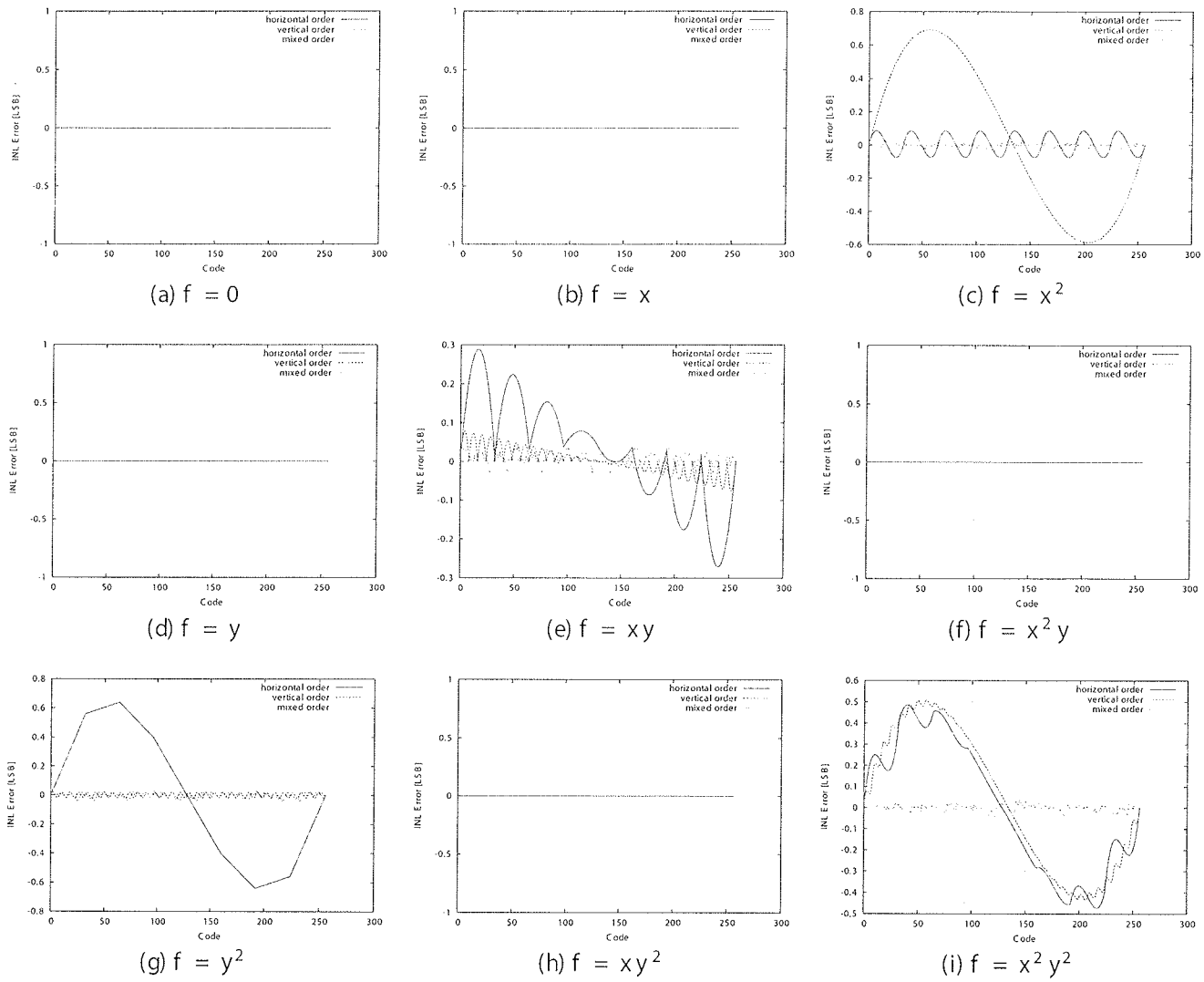

Figure 5: INL vs. selection-order.

5. Acknowledgments

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References:

/1/ Jose Bastos and Michel S. J. Steyaert. A 12-bit intrinsic accuracy high-speed CMOS DAC. IEEE Jurnal of Solid-State Circuits, 33(12):1959–1969, December 1998.

/2/ Jose Bastos, Michel S. J. Steyaert, Benny Graindourze, and Willy Sansen. Matching of MOS transistors with different layout styles. Proc. IEEE Int. Conference on Microelectronic Test Structures, number 12, pages 17–18. IEEE, March 1996.

/3/ Jose Bastos, Michel S. J. Steyaert, and Willy Sansen. A high yield 12-bit 250-ms/s CMOS D/A converter. In Proceedings IEEE 1996 CICC, pages 431–434. IEEE, May 1996.

/4/ Geert A. M. Van der Plas, Jan Vandenbussche, Willy Sansen, Michel S. J. Steyaert, and Georges G. E. Gielen. A 14-bit intrinsic accuracy Q^2 random walk CMOS DAC. IEEE Jurnal of Solid-State Circuits, 34(12):1708–1718, December 1999.

/5/ Kadabar R. Lakshmikumar, Robert A. Hadaway, and Miles A. Copeland. Characterization and modeling of mismatch in MOS transistors for precision analog design. IEEE Jurnal of Solid-State Circuits, 21(6):1057–1066, December 1986.

/6/ Chi-Hung Lin and Klaas Bult. A 10-b, 500-ms/s CMOS DAC in 0.6 mm^2. IEEE Jurnal of Solid-State Circuits, 33(12):1948–1958, December 1998.

/7/ Marcel J. M. Pelgrom, Aad C. J. Duinmaijer, and Anton P. G. Welbers. Matchinh properties of MOS transistors. IEEE Jurnal of Solid-State Circuits, 24(5):1433–1440, October 1989.

/8/ Louis SY Wong, Chee Y. Kwok, and Graham A. Rigby. A 1-v CMOS D/A converter with multi-input floating-gate MOSFET. IEEE Jurnal of Solid-State Circuits, 34(10):1386–1390, October 1999.Roman Benković

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