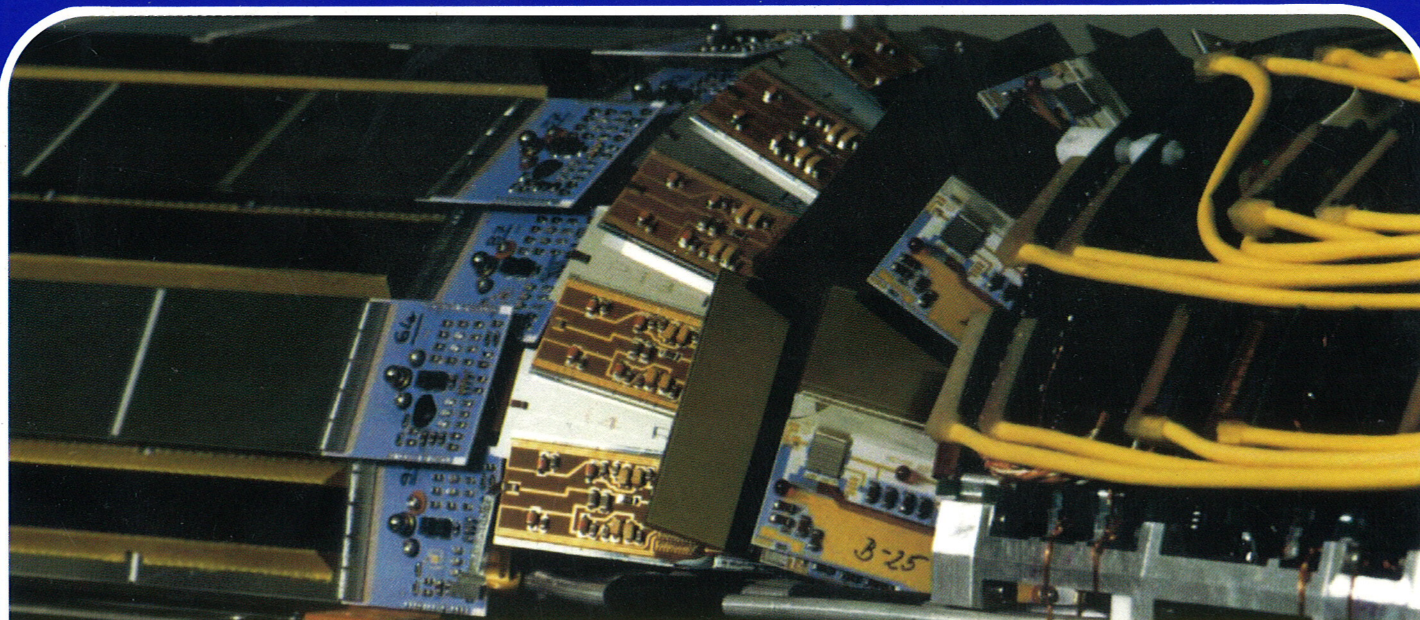
UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 1 ○ 1999

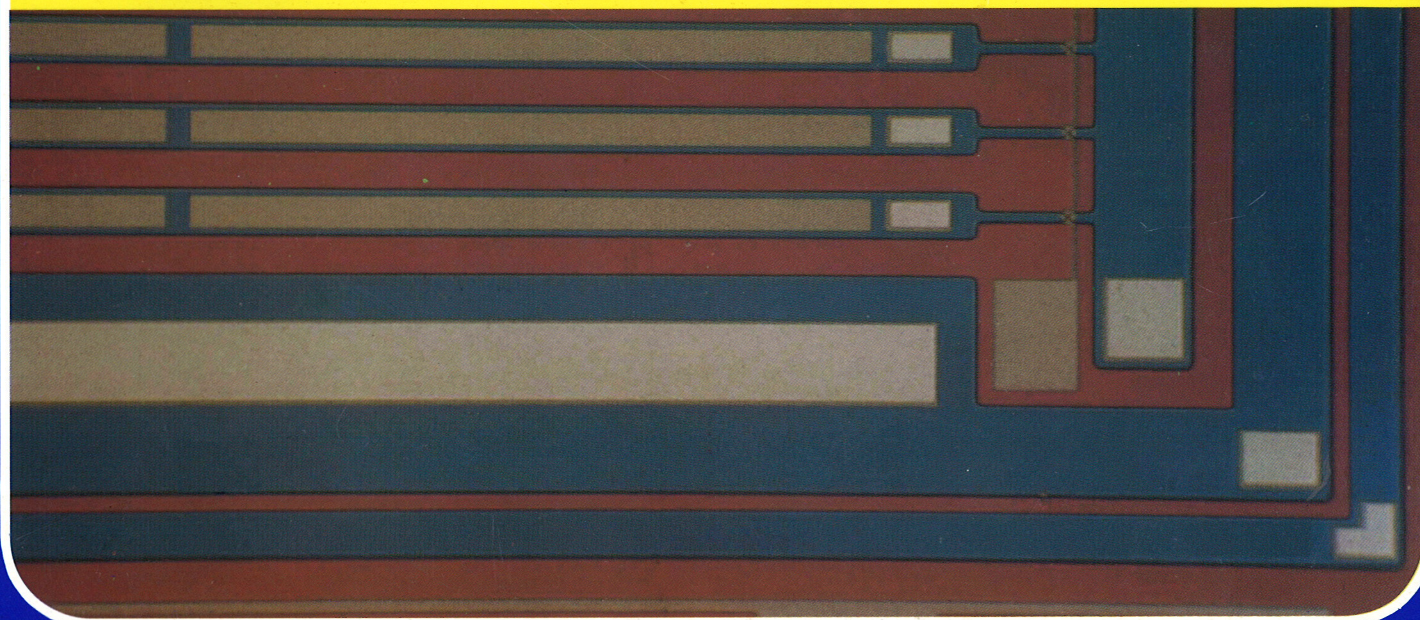
Strokovno društvo za mikroelektroniko elektronske sestavne dele in materiale

Strokovna revija za mikroelektroniko, elektronske sestavne dele in materiale
Journal of Microelectronics, Electronic Components and Materials

INFORMACIJE MIDEM, LETNIK 29, ŠT. 1(89), LJUBLJANA, marec 1999



MIDEM'98 CONFERENCE
whit the Satellite Minisymposium on
Semiconductor Radiation Detectors



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

INFORMACIJE MIDEM 1 ◦ 1999

INFORMACIJE MIDEM LETNIK 29, ŠT. 1(89), LJUBLJANA, MAREC 1999

INFORMACIJE MIDEM VOLUME 29, NO. 1(89), LJUBLJANA, MARCH 1999

Revija izhaja trimesečno (marec, junij, september, december). Izdaja strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale - MIDEM.
Published quarterly (march, june, september, december) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Glavni in odgovorni urednik
Editor in Chief
Dr. Iztok Šorli, dipl.ing.,
MIKROIKS d.o.o., Ljubljana

Tehnični urednik
Executive Editor
Dr. Iztok Šorli, dipl.ing.,

Uredniški odbor
Editorial Board
Doc. dr. Rudi Babič, dipl.ing., Fakulteta za elektrotehniko, računalništvo in informatiko Maribor
Dr.Rudi Ročak, dipl.ing., MIKROIKS d.o.o., Ljubljana
mag.Milan Slokan, dipl.ing., MIDEM, Ljubljana
Zlatko Bele, dipl.ing., MIKROIKS d.o.o., Ljubljana
Dr. Wolfgang Pribyl, Austria Mikro Systeme International AG, Graz
mag. Meta Limpel, dipl.ing., MIDEM, Ljubljana
Miloš Kogovšek, dipl.ing., Ljubljana
Dr. Marija Kosec, dipl. ing., Inštitut Jožef Stefan, Ljubljana

Časopisni svet
International Advisory Board
Prof. dr. Slavko Amon, dipl.ing., Fakulteta za elektrotehniko, Ljubljana, PREDSEDNIK - PRESIDENT
Prof. dr. Cor Claeys, IMEC, Leuven
Dr. Jean-Marie Haussonne, EIC-LUSAC, Octeville
Dr. Marko Hrovat, dipl.ing., Inštitut Jožef Stefan, Ljubljana
Prof. dr. Zvonko Fazarinc, dipl.ing., CIS, Stanford University, Stanford
Prof. dr. Drago Kolar, dipl.ing., Inštitut Jožef Stefan, Ljubljana
Dr. Giorgio Randone, ITALTEL S.I.T. spa, Milano
Prof. dr. Stane Pejovnik, dipl.ing., Kemijski inštitut, Ljubljana
Dr. Giovanni Soncini, University of Trento, Trento
Prof.dr. Janez Trontelj, dipl.ing., Fakulteta za elektrotehniko, Ljubljana
Dr. Anton Zalar, dipl.ing., ITPO, Ljubljana
Dr. Peter Weissglas, Swedish Institute of Microelectronics, Stockholm

Naslov uredništva
Headquarters
Uredništvo Informacije MIDEM
Elektrotehniška zveza Slovenije
Dunajska 10, 1000 Ljubljana, Slovenija
tel.: + 386 (0)61 1512 221
fax: + 386 (0)61 1512 217

Iztok.Sorli@guest.arnes.si
http://pollux.fer.uni-lj.si/midem/journal.htm

Letna naročnina znaša 12.000,00 SIT, cena posamezne številke je 3000,00 SIT. Člani in sponzorji MIDEM prejemajo Informacije MIDEM brezplačno.
Annual subscription rate is DEM 200, separate issue is DEM 50. MIDEM members and Society sponsors receive Informacije MIDEM for free.

Znanstveni svet za tehnične vede I je podal pozitivno mnenje o reviji kot znanstveno strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinanci rajo Ministrstvo za znanost in tehnologijo in sponzorji društva.
Scientific Council for Technical Sciences of Slovene Ministry of Science and Technology has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials.
Publishing of the Journal is financed by Slovene Ministry of Science and Technology and by Society sponsors.

Znanstveno strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC.
Prispevke iz revije zajema ISI ® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™
Scientific and professional papers published in Informacije MIDEM are assessed into COBISS and INSPEC databases.
The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™

Po mnenju Ministrstva za informiranje št.23/300-92 šteje glasilo Informacije MIDEM med proizvode informativnega značaja, za katere se plačuje davek od prometa proizvodov po stopnji 5 %.

Grafična priprava in tisk
Printed by
BIRO M, Ljubljana

Naklada
Circulation
1000 izvodov
1000 issues

Poštnina plačana pri pošti 1102 Ljubljana
Slovenia Taxe Percue

UDK621.3:(53+54+621+66), ISSN0352-9045 | Informacije MIDEM 29(1999)1,Ljubljana

ZNANSTVENO STROKOVNI PRISPEVKI		PROFESSIONAL SCIENTIFIC PAPERS
MIDEM´98 KONFERENCA, Minisimpozij-Polprevodniški detektorji sevanja - POVABLJENI REFERATI		MIDEM´98 CONFERENCE, Minisymposium on Semiconductor Radiation Detectors - INVITED PAPERS
R.H. Richter, G. Lutz: Silicijevi detektorji sevanja – fizika in strukture	1	R.H. Richter, G. Lutz: Silicon Radiation Detectors – Physics and Structures
Valter Bonvicini: Karakterizacija in meritve silicijevih detektorjev	10	Valter Bonvicini: Characterisation and Measurements of Silicon Detectors
Valerio Re, Lodovico Ratti: Čitalna elektronika za meritev pozicije in energije pri polprevodniških detektorjih sevanja	20	Valerio Re, Lodovico Ratti: Front-end Electronics for Energy and Position Measurements with Semiconductor Radiation Detectors
F. Arfelli, V. Bonvicini, A. Bravin, G. Cantatore, E. Castelli, L. Dalla Palma, M. Fabrizioli, R. Longo, A. Olivo, S. Pani, D. Pontoni, P. Poropat, M. Prest, A. Rashevsky, L. Rigon, G. Tromba, A. Vacchi, E. Vallazza: Večplastni silicijev mikropasovni detektor za digitalno mamografijo s štetjem posameznih fotonov	26	F. Arfelli, V. Bonvicini, A. Bravin, G. Cantatore, E. Castelli, L. Dalla Palma, M. Fabrizioli, R. Longo, A. Olivo, S. Pani, D. Pontoni, P. Poropat, M. Prest, A. Rashevsky, L. Rigon, G. Tromba, A. Vacchi, E. Vallazza: A Multi-layer Silicon Microstrip Detector for Single Photon Counting Digital Mammography
APLIKACIJSKI PRISPEVKI		**APPLICATION ARTICLES**
Mitja Hariš: Kako izbrati varistor	32	Mitja Hariš: How to Choose a Proper Varistor
PRIKAZI MAGISTRSKIH DEL IN DOKTORATOV, LETO 1998	36	M. S. and Ph. D. ABSTRACTS, YEAR 1998
Prvo obvestilo KONFERENCA MIDEM´99	**46**	**Announcement and Call for Papers MIDEM´99 CONFERENCE**
VESTI	**51**	**NEWS**
KOLEDAR PRIREDITEV	**55**	**CALENDAR OF EVENTS**
MIDEM prijavnica	57	MIDEM Registration Form

Slika na naslovnici:
Zgoraj: polovica sestavljenega detektorja sledi nabitih delcev z mikropasovnimi silicijevimi detektorji pred vgradnjo v spektrometer DELPHI na trkalniku LEP v Evropskem laboratoriju za fiziko delcev CERN v Ženevi. Z leve proti desni so vidni: sodčasti del detektorjev (črne ploščice), njihova čitalna elektronika na hibridnem vezju (modro), detektorji v smeri naprej (temnozlate ploščice), delno prekriti s hibridnim vezjem (modro in zlato, na enem oznaka B-25), krmilna elektronika in napajanje. Hibridna vezja za prednji del detektorja so bila izdelana na Institutu "Jožef Stefan".
Spodaj: SDX-100S silicijev detektor x-žarkov s stranskim vpadom x-žarkov

Front page:
Upper picture: one half of the assembled silicon microstrip vertex detector before installation in the DELPHI spectrometer on the LEP collider at CERN – European Laboratory for Particle Physics in Geneva. From left to right: detectors of the barrel part (dark plates) their readout electronics on hybrids (blue), forward detectors (dark gold plates), partially covered by hybrids (blue and gold, one marked B-25), electronics drivers and supplies. The forward detector hybrids were produced at the "Jožef Stefan" Institute.
Lower picture: SDX-100S side illumination silicon x-ray strip detector

VSEBINA CONTENT

MIDEM´98 Conference - Minisymposium on Semiconductor Radiation Detectors

A new initiative has been given by the MIDEM Society to expand and promote the MIDEM Conference with specialized satellite minisimposia on selected topics during annual MIDEM conferences. The idea is to strengthen cooperation and gathering of scientists and researchers working in the same research field and to encourage others to join them in their efforts. In order to make this event especially attractive, the minisymposium is incorporating a tutorial session given by established experts in the field giving an overview of the selected topics.

During the last yearžs MIDEM Conference a Minisymposium on Semiconductor Radiation Detectors was organized. The preparation of the minisymposium was carried out by the Laboratory for Electron Devices, University of Ljubljana, Slovenia, who established an ad hoc international organizing committee that helped with the reviewing of regular papers and selection of invited speakers for the tutorial session. The members of the Minisymposium organization committee were:

- *Dejan Križaj and Slavko Amon, Laboratory for Electron Devices, Faculty of Electrical Engineering, University of Ljubljana, Slovenia*
- *Vladimir Cindro and Marko Mikuž, Department for Elementary Particle Physics, Jožef Stefan Institute, Slovenia*
- *Walter Bonvicini and Andrea Vacchi, INFN Trieste and University of Trieste, Italy*
- *Giovanni Soncini and Giorgio Pignatel, IRST Trento and University of Trento, Italy*

We thankfully acknowledge their help.

The papers from three tutorial lectures presented at the Minisymposium are following this foreword. An excellent overview of several radiation detector types and their capabilities is presented in the paper of dr. Rainer Richter and dr. Gerhard Lutz. Most, if not all of the discussed structures, were actively studied by them and produced by "their" MPI Halbleiterlabor in Munchen, Germany. The most frequently used and investigated silicon radiation detectors are probably silicon strip detectors. An overview of their characterization methods was given by dr. Walter Bonvicini of INFN, Trieste, Italy, strengthened by his extensive personal research work and experiences in this field. Proper detector design and application is possible only by understanding of its coupling to the readout electronics. Dr. Valeio Re from the University of Bergamo, Italy, gave an excellent overview of front-end electronics. Unfortunately, the fourth invited lecturer, dr. Peter Walheimer from CERN, Switzerland, was not able to prepare a full version of his inspiring talk on the advances and future of semiconductor radiation detectors. Together with regular papers to the Minisimposium they contributed to an exciting, pleasant and successful event. Thank you all.

Several research groups are working in the field of semiconductor radiation detectors all around the world. The work of European researchers is probably mostly inspired by the projects and demanding needs of the CERN experiments to develop fast, high resolution, reliable, large, cheap etc. radiation detectors for experiments in high energy physics. As a result, several types of detectors have been invented and developed together with unseparable readout electronics. New processing and characterization methods have been developed as well. This vast and inspiring work performed by excellent researchers and scientists will probably not be awarded a Nobel prize, however, it might help the users of the developed devices and techniques to earn one - or even more. But this is not the end of it. From a personal point of view, I am not excited only by the new theories of the Universe they will enable, but also by the outstanding capabilities of radiation detection by the new developed devices that help us (and will certainly help us even more in the future) to better understand the world around us - and inside of us. They deserve our attention and effort.

Dejan Križaj
Faculty of Electrical Engineering,
University of Ljubljana, Slovenia

SILICON RADIATION DETECTORS - PHYSICS AND STRUCTURES

R.H. Richter and G. Lutz
Max-Planck-Institut für Physik, München, Germany

TUTORIAL INVITED PAPER
MIDEM´98 CONFERENCE – Minisymposium on Semiconductor Radiation Detectors
23.09.98 – 25.09.98, Rogaška Slatina, Slovenia

Keywords: Si silicon radiation detectors, Si silicon microstrip detectors, particle physics, astrophysics, spectroscopic devices, signal detection, X-ray analysis, signal amplification, energy resolution, position resolution, tracking detectors, semiconductor tracking devices, physical foundations, semiconductor structures, DEPMOS structures, DEPleted Metal-Oxide Silicon structures, DEPFET structures, DEPleted Field Effect Transistor structures

Abstract: Silicon radiation detectors are used in many fields of application. The development of strip detectors and spectroscopic devices is mainly driven by the research in particle physics and astrophysics. As a result of the progress made in high resolution silicon drift chambers portable spectroscopic systems operating close to room temperature have been developed. They are used for a variety of x-ray analysis methods. In pixel detectors a signal amplification already takes place at the location of signal detection. They have the potential to combine fast signal amplification, high precision and energy resolution with low power consumption.

Silicijevi detektorji sevanja – fizika in strukture

Ključne besede: Si detektorji sevanja silicijevi, Si detektorji silicijevi mikrotrakasti, fizika delcev, astrofizika, naprave spektroskopske, detekcija signalov, X-žarki analiza, ojačenje signalov, ločljivost energijska, ločljivost položajna, detektorji sledilni, naprave sledilne polprevodniške, osnove fizikalne, strukture polprevodniške, DEPMOS strukture silicijeve kovinsko oksidne, DEPFET strukture

Izvleček: Silicijevi detektorji sevanja so našli uporabo na mnogih področjih. Razvoj mikropasovnih detektorjev in spektroskopskih naprav v glavnem spodbujajo raziskave na področju fizike delcev in astrofizike. Kot rezultat napredka pri razvoju visokoločljivih silicijevih drift detektorjev so nastali prenosni spektroskopski sistemi, ki delujejo blizu sobne temperature. Uporabljamo jih pri raznovrstnih analiznih metodah z rentgenskimi žarki. V točkovnih detektorjih signal ojačamo že na samem mestu detekcije signala. Ti detektorji združujejo možnost hitre ojačitve signala, visoke natančnosti in energijske ločljivosti z majhno porabo moči.

1 Introduction

Radiation detectors may be classified according to their use for particle tracking and for spectroscopic applications. Tracking detectors are widely used in the field of particle physics while spectroscopic detectors have their most important applications in material analysis and x-ray astronomy.

At present, the development of tracking detectors is mainly driven by the LHC (Large Hadron Collider) experiments planned to start in 2005 at CERN. Device concepts allowing mass production and providing sufficient radiation hardness are required in this field.

For the category of spectroscopic semiconductor detectors, silicon is the detector material of choice for x-ray detection below 20keV. The focus is put in noise reduction and increase of counting rates in order to minimize the exposure and measurement times.

2 Tracking Detectors

Here the emphasis is on position measurement, although the energy of absorbed (or energy loss of penetrating) particles is sometimes also measured.

The by far most widely used semiconductor tracking devices are strip detectors. These exist in single sided and double sided versions. The readout is either directly or capacitively coupled. Readout of every strip or capacitive charge division readout are possible.

An elegant device, in which the signal charge drifts parallel to the surface to a collecting anode is the semiconductor drift chamber. Here the drift time can be used for determining the position. As these devices provide very small capacitive load to the readout amplifier, the signal charge (or energy) can simultaneously be measured very precisely. For many applications only the energy measurement is used and these devices will (in this presentation) be described in the section of spectroscopic detectors. Similar considerations hold for CCD detectors.

2.1 Strip Detectors

Fast signal readout and good position resolution are the key features of a tracking detector. The typical device being able to fulfill these requirements is a strip detector.

Strip detectors have been developed for the purpose of measuring the position of single particles incident on or traversing the detector. Extremely important progress was made by the development of low-noise, low-power microelectronics which could be directly mounted next to the detectors, connected to it by ultrasonic wire bonding.

The principle of strip detectors at first glance is rather simple. A large area diode is divided into narrow strips, each of them being read out with a separate electronic channel. The position of the ionizing particle incident on or traversing the detector is then given by the location of the strip showing the signal.

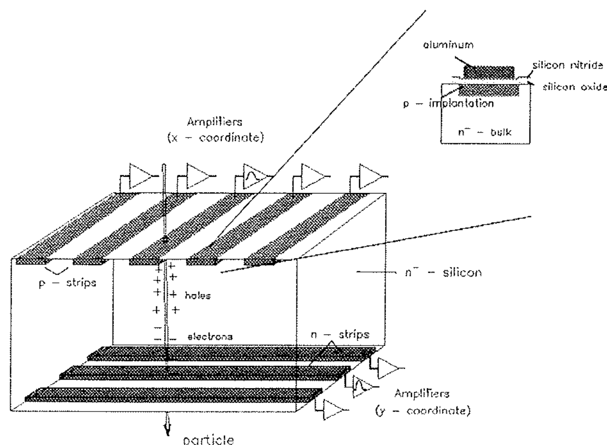


Fig. 1: Schematic drawing of a double sided strip detector. The p-strips on the top side are read out by capacitive coupling (see insert).h The biasing of the p-strips and details on the n-side including the necessary precausions for providing electrical insulation between neighboring n-strips are not shown.

To obtain a two dimensional position information, there is the possibility to glue two strip detectors with different strip directions back to back together. The more natural (elegant) method - reducing simultaneously scattering material - is the use of double sided strip detectors with p-strips on one and n-strips on the other side as schematically indicated in Figure 1. The holes drift to the p-strip while the electrons are collected by the n-strips. Thus both charge carrier types are used for signal formation.

2.1.1 Capacitive coupled readout and bias structures

To decouple the amplifier inputs from the detector leakage current - thereby avoiding channel to channel and time dependent pedestal shifts - capacitively coupled detectors are frequently used. Realization of this readout concept is difficult due to the large values of capacitances and bias resistances needed. The capacitors can be integrated into the detector by inserting insulation layers between the strip implantations and the metal lines. Providing the insulation by the ovelap of two independent layers (as shown in the insert of Figure 1) increases dramatically the strip yield as shorts of the integrated coupling capacitors due to insulator defects are extremely unlikely. In capacitively coupled detectors the strips have to be biassed by additional bias structures which in the simplest case can be resistors located on the ends of the strips. These resistors can be built with poly silicon, by ion implantation in the bulk or by using charge induced layers like the electron accumulation layers that are naturally induced by the always existing positive oxide charges in the transition region of silicon and silicon oxide. However, these methods are either space consuming and/or need additional technological effort. A simple alternative method that needs almost no additional space and no further processing effort is the so called punch through biassing /1/ sometimes also called FOXFET biassing. Here a small gap of about 5 μm between the strip end and a bias line is used to form a potential barrier whose dynamic resistance depends on the leakage current of the individual strip. This leads to a very compact high ohmic bias device which can be implemented for p-strip biassing as well as for n-strip biassing. The only drawback of this structure is its lack on radiation hardness that is caused by the introduction of excess noise /2/ due to the presence of radiation generated bulk traps in the punch through region /3/.

2.1.2 Charge division readout

As the signal charge during collection time will also undergo diffusion, the signal may be spread between neighboring strips. Analog readout of signal charge therefore not only allows simultaneous determination of energy and position but furthermore (by means of interpolation) improves position measurement, provided the strip spacing matches the diffusion width. Charge division may also be used to decrease the number of readout channels. Only a fraction of strips is connected to a readout channel. Charge collected on intermediate (not connected) strips is capacitively coupled to the neighbouring readout strips through the naturally occuring strip to strip capacitances. In order to avoid distortions of the electric field configuration the intermediate strips have to be held at the potential of the readout strips.

2.1.3 Application fields of strip detectors

The development in the field of strip detectors are mainly driven by the LHC (Large Hadron Collider) experiments currently under construction at CERN. The large detection area of more than 150 m^2 leading to about 40000 detectors each of a size of about 40 cm^2 is one of the main challenges in the construction of these experiments. Facing those quantities, robust detector concepts are needed which allow mass production with high yield. For the sake of simplicity of detectors and electronics, single sided p-strip detectors with capacitively coupled readout were chosen as baseline in both multi purpose experiments at LHC (ATLAS as well as CMS). The signal has to read out within two bunch crossings (i.e. 25 ns). This means that the electronics have to operate with a signal peaking time of about 20 ns, a'time that is already in the range of the charge carrier drift time in a 300 μcm thick detector. In this volume a MIP (Medium Ionizing Particle) generates about 24000 electron/hole pairs, a signal that has to be compared with the equivalent noise charge of the system of about 1500 electrons /6/.

The other main challenge is the high radiation environment in which the detectors have to operate over the whole forseen ten years lifetime of the experiments. For example, the innermost barrel layer of the ATLAS SCT (SemiConductor Tracker) has to withstand a radiation dose of 2×10^{14} cm^{-2} 1 MeV equivalent neutrons /6/.

2.1.4 Radiation hardness

Radiation does not only interact with the electrons of the semiconductor, thereby providing the transient signals to be detected, but also with the nuclei of the lattice, thereby creating crystal defects which in the following are referred to as bulk damage.

Furthermore ionizing radiation creates electron-hole pairs not only in the semiconductor but also in the insulating layer (SiO_2). While electrons in silicon dioxide have high mobility and escape almost immediately, holes are extremely slow and may be permanently captured in deep level traps of the oxide and in the oxide semiconductor interface /5/. Thus positive charge is produced and accumulated in the oxide and in the oxide-semiconductor interface, leading to threshold shifts of MOS transistors and to local high field regions in detectors. A saturation of the radiation induced oxide charge is observed which may be explained by the limited number of traps. For the commonly used <111> oriented detector material oxide charge saturation values of about 1.5 to 3×10^{12} cm^{-2} were measured, with results depending on the technological treatment.

In the silicon the dominant primary induced lattice damage is the displacement of atoms from their regular lattice sites, thus creating simultaneously vacancies and (self) interstitials. Most of these primary defects are not stable. Interstitials and vacancies are mobile at room temperature and will therefore partially anneal if, by chance, an interstitial fills the place of a vacancy. However there are also chances for the formation of other (at room temperature) stable defect complexes. Examples are the well known A-center, a combination of a vacancy and oxygen (a certain concentration of oxygen interstitials is present in the crystal after crystal growing), the E-center, a vacancy phosphor complex and the divacancy (two missing silicon atoms right next to each other).

These stable defects locally distort the symmetry of the crystal. They in general may assume two or more charge states corresponding to different types of chemical binding respectively lattice distortion. Change of the defect charge state is accomplished by electron and hole capture or emission. The minimum energy necessary to emit an electron to the conduction band or a hole to the valence band determines the energy level of the particular defect charge state within the band gap.

Depending on the charge states and energy levels of the defects, some of the following effects will be dominant in the space charge region of a detector:

- Generation of leakage current by alternative emission of electrons and holes. This mechanism is dominant for defects with the energy level close to the band gap center.
- Trapping: capture and later reemission of electrons or holes. This process dominates if the defect level is not very close to either band.
- Defects assuming an (on average) non-zero charge state. This effect results in a change of space charge and the required operating voltage for the detector.

The stability of defects is temperature dependent. Heating may make them movable or break up defect complexes. Removing defects this way is termed annealing. Some of it occurs already at room temperature. New types of defect complexes may however be generated in the process.

As the physics of radiation damage is rather complicated and only partially understood, involving many types of defects, one usually restricts oneself to a parameterization of measured changes in material parameters like the generation lifetime (determining the leakage current), the charge trapping probability and the effective doping change (determining the operating voltage). Irradiation of silicon changes the effective doping in the direction of increased p-doping, as found by observing the space charge density. N-type silicon will first change to intrinsic and then to effective p-doping. After ending the irradiation the effective doping will decrease on short time scales but then it will rise again on time scales of months or years. This unpleasant and not satisfactorily understood effect, leading to high required operating voltages has been termed reverse annealing. It can be suppressed by cooling the devices to roughly 0°C.

Some data taken from the ATLAS TDR (Technical Design Report) /6/ should demonstrate the practical relevance of this effect. The operation (and maintenance) temperature scenario of ATLAS leads to depletion voltages of about 220 V for the innermost barrel layer after ten years operation not taking into account the safety margins /6/. The maximum operation voltage is assumed to be 350 V at which the detectors has to run still stable in order to avoid any self heating effects by increased power consumptions. Keeping in mind that commonly used detectors usually operate at voltages below 100 V this implies a new quality of requirements to the detector design and technology[1].

2.1.5 Double sided detectors for high radiation applications

A radiation hard double sided capacitively coupled strip detector developed and produced by the MPI Semiconductor Lab for the HERA-B experiment at DESY Hamburg /8/ is shown in Figure 2. The radiation level in HERA-B is even an order of magnitude higher than in the LHC experiments. This means that the detectors have to be replaced after they reach a damage level which makes a reasonable data analysis impossible. However, although the number of 64 detectors installed in HERA-B is rather small compared with the LHC experiments, it is an important physical and economic issue to provide components which survive at least an operation period of one year. In order to reduce the scattering of the tracks on the detector material, double sided detectors were chosen, thus halving the amount of silicon material seen by the incident particles compared to two single sided detectors. Several features are implemented with the focus to prolonge the survival time of the device in the harsh radiation environment.

1 Very recent results of the ROSE collaboration suggest that intrinsic radiation hardening of silicon can be achieved by the increase of oxygen concentration within the bulk silicon /7/.

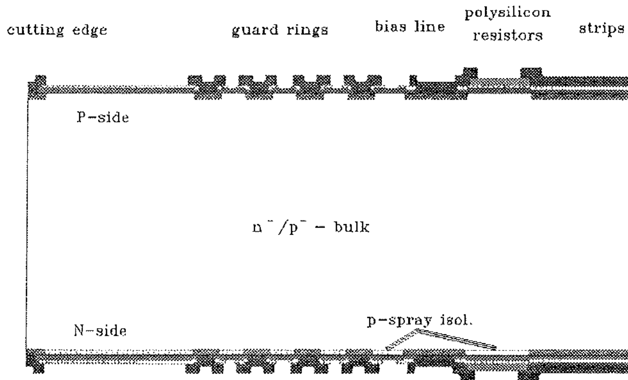


Fig. 2: Schematic cross section through a double sided strip detector designed and produced for HERA-B. For the sake of clearness the real guard ring number of 16 is reduced in the figure.

The detector is designed to operate at bias voltages above 500 V after an exposure to 2 x 10^{14} cm^{-2} 1 MeV equivalent neutrons. On both sides high voltage protection structures provide for a smooth drop of the bias voltage from the rim of the active area towards the cutting edge. The operation of this multi-guard ring structures bases on moderated potential drops between neighboring guard rings that are adjusted by the punch through voltages between the rings /4/. Large gaps between neighboring implantations are avoided in the whole detector area. This measure reduces lateral electric field peaks and increases the break down voltage /10/. The positive oxide charge at the Si/SiO_2 interface usually generates an electron accumulation layer that shorts neighboring implantations. Additional p-stops are usually implanted to interrupt or suppress this electron layer. In the HERA-B detectors an overall p implantation (that does not need a further mask) is used /9/ to provide this isolation. Besides the obvious process simplification this technique implies the feature that the critical lateral electric fields between the n-implants and the p-isolation layer decrease with increasing oxide charges leading to the desired situation of decreasing field maxima after irradiation /10/. An examples for this behavior will be shown in chapter 4. (Pixel detectors). The biassing of the capacitively coupled implanted strips is done by poly silicon in order to avoid the above mentioned excess noise generation.

3 Spectroscopic Silicon Devices

Energy measurement of x-rays is accomlished by determination of the amount of charge that is generated by the converted x-ray. In order to obtain highly precise charge measurements dedicated devices were developed. Here we have to answer the question of the achievable noise minimum. Independent from the optimization of the detector and electronics there exists an minimum noise level wich cannot be lowered (as long as the basic detector material is not changed). This noise is attributed to the charge generation process itself. The energy conversion of an x-ray takes place in a cascade process. Starting with a small number of energetic electrons consecutive impact process leads to a generation of electron/hole pairs, which generates further electron/hole pairs (Figure 3). This process continues until the energy of the charge carriers is lower than the threshold level (E_{th}). In the cascade process not all of the energy is transfered to newly generated charge carriers, a large fraction is transmitted to phonons. This energy splitting undergoes statistical fluctuations resulting in the Fano noise /11/. The Fano noise depends on the x-ray energy

$$\sigma_F = \sqrt{wFE}$$

With the pair creation energy w (3.7 eV for silicon), the Fano factor F (F = 0.12 for Si) and the photon energy E. For example in silicon a Fe^{55} x-ray signal (5.895 keV) is generated with a Fano noise contribution of 118 eV at room temperature.

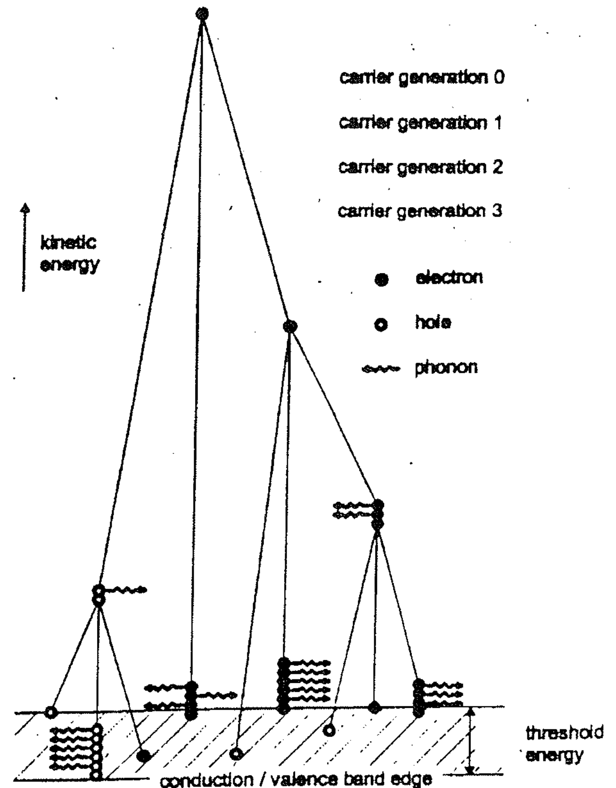


Fig. 3: Ionization casdade after a x-ray conversion. Electron/hole pairs can be generated only above the threshold energy (Courtesy of P. Lechner)

While the Fano noise drops with decreasing energy, other noise contributions remain constant. A usually dominant noise source is the serial noise that is generated by noise sources within the (charge sensitive) amplifier and that increases linearly with the capacitive load at the amplifier input. Reducing the detector capacitance therfore is imperative for low noise spectroscopic detectors. With the silicon drift detector this can be accomplished while keeping large detection volumes.

3.1 Drift Detectors

The working principle bases on the eflect of sidward depletion which may be explained by starting from the diode.

The backside N^+ contact does not have to extend over the full area, but can instead be put at any place of the undepleted conducting bulk (Figure 4a). Then there is space to put diodes on both sides of the wafer. At small voltages applied to the N^+ electrode we have two detectors separated by the conducting undepleted bulk region (hatched in the figure). At high enough voltages (Figure 4b) the two space charge regions touch each other and the conducting bulk region retract towards the vicinity of the N^+ electrode. At this point the capacitance between N^+ electrode the P^+ electrodes drops dramatically and becomes moreover independent on the detector area. A potential valley for electrons is obtained in which thermally or otherwise generated electrons assemble until they (slowly) diffuse towards the N^+ electrode (anode) while holes are drifting (fast) in the electric field towards the P^+ electrodes. Increasing of the voltage leads to an overdepletion and to the isolation of the N+ electrode which now can act as anode in a detector system (Figure 4c).

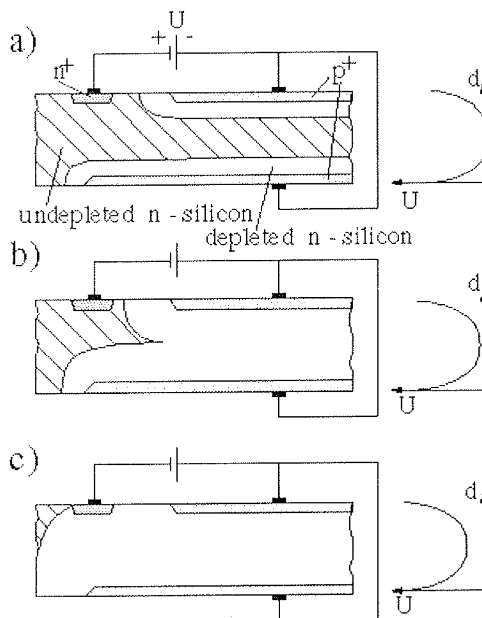


Fig. 4: Basic structures leading towards the drift detector: diode partially depleted from both sides (a); diode just depleted (b); diode overdepleted (c)

In the Silicon Drift Detector (SDD), in its basic form proposed by E. Gatti and P. Rehak /1/) in 1984, an additional electric field component parallel to the surface of the wafer is added so as to provide for a drift of electrons in the valley towards the anode. This is accomplished by dividing the diodes into strips and applying a graded potential to these strips on both sides of the wafer. Drift chambers may be used as position and/or energy sensitive detectors. The position can be obtained from the time between incidence of ionizing particle and formation of the signal on the readout electrode (drift time of signal electrons). Its importance as energy sensitive device is due to the fact that signal charges from a large area device are collected on a small area and therefore small capacitance electrode, thus reducing noise in the readout electronics.

Other drift field configurations (e.g. radial drift) can be obtained by suitable shaping of the electrodes. Drifting towards a central collecting electrode is especially interesting for energy measurement (Figure 5) as the capacitance of the readout electrode may be reduced to the 100 f F range. Drifting outwards towards a segmented ring anode has also been done for a special application /12/. As an example of what can be achieved by combining various features described before a x-ray spectrum measured with a novel drift device is presented. The single sided structured device with the electron potential valley running from the outside bottom to the inside top collecting anode provides a homogeneous entrance window. Cylindrical geometry with radial drift provides small capacitance and low noise.

Integration of a first (Single Sided JFET) transistor /13/ avoids stray capacitances leading to low noise and fast signal shaping in order to take full advantage of the minimized anode capacitance. Further properties are the integration of a voltage divider for the field shaping electrodes and the draining of surface generated leakage currents.

The device is very well suited for (near) room temperature spectroscopy as demonstrated in figure (Figure 6) where the Fe^{55} spectra at 25°C and -13°C obtained with 0.25 respectively 1 μs shaping time constant are shown. An energy resolution of 178 eV respectively 144 eV has been achieved /14/.

These high resolution spectra qualify the silicon drift chamber for applications different x-ray analysis techniques where good spectroscopic features together with high counting rates are required, for instance x-ray flourescence (XRF), electron microprobe analysis

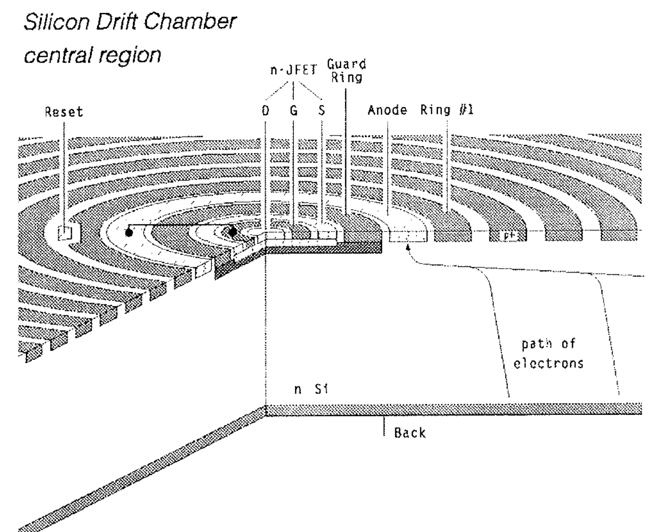


Fig. 5: Drift diode with integrated Single Sided JFET and non structured homogeneous backside entrance window

(EDX) or particle induced x-ray emission (PIXE). An example for a working detector system is the portable XRF spectrometer for non-destructive analysis in archeometry /15/ developed in collaboration of Politecnico di Milano, MPI Semiconductor Lab and Ketek GmbH.

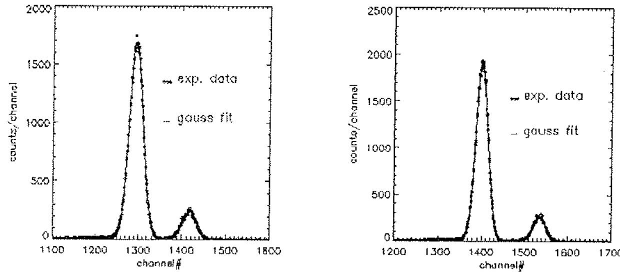


Fig. 6: Drift diode with integrated electronics: Manganese spectrum from an Fe^{55} source recorded at 25°C Shaping time = 0.25 µs, FWHM = 178 eV (left); Manganese spectrum recorded at -13°C Shaping time =1 µs, FWHM =144 eV (right)

3.2 Fully depleted p-n CCD for x-ray applications

The p-n CCD (Figure 7) is based also on the sideward depletion principle. Putting non equal potentials on front and backside diode junctions one moves the electron potential valley close to the top surface. Instead of applying a linearly rising potential to the field shaping electrodes on the top side a periodic potential is used thus creating electron potential minima in which the signal electrons are confined. The backside of the device is a single large area diode, thus providing a homogeneous radiation entrance window for the completely depleted and therefore fully sensitive detector volume. Signal charge is moved towards the N^+ doped collecting anode by a cyclic change of the (three phase) register potentials.

The development of x-ray CCDs is clearly driven by the requirements of the astrophysics. 6 x 6 cm^2 large

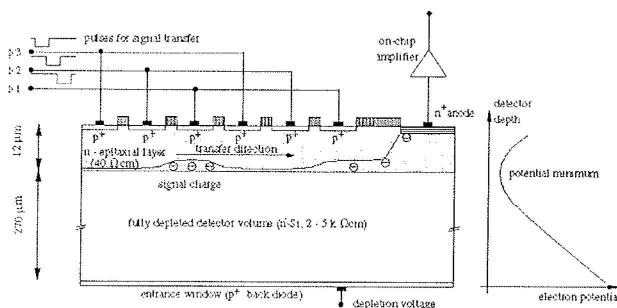


Fig. 7: Schematic cross section of a three phase p-n CCD with integrated JFET amplifier. The register consists of p-n diodes and the charge transfer depth is in the range of 10 µm allowing larger pixel sizes as used in conventional MOS-CCDs.

monolythic devices with a pixel size of 150 x 150 μm^2 will be used as focal instruments in space based X-ray telescopes developed for astronomical observations /19, 20/. The flight models are already qualificated for the launches of the ABRIXAS and XMM satellites scheduled in spring 1999 and 2000, respectively.

4 New Detector Structures - Pixel Detectors

An inherent problem of strip detectors is that in the case of multiple hits occouring in one read out time slot the two dimensional local resolution becomes ambigous. The very high luminosity occuring in the LHC experiments leads to large amount of vertices to be detected especially in the very inner parts of the detectors. Therefore in this regions higher segmented detectors, so called pixel detectors, will be installed. These detectors contain basically diode arrays where the attached electronic channels are mounted on top of the diodes using flip chip bump bond technique /16/. Comparing strip detectors with pixel detectors the advantages of the latter are the definite relation between a small sensor diode and the attached frontend electronics and the reduced input capacitance seen by each input amplifier. The principle is illustrated by the schematic cross section (Figure 8) showing a single diode bumped to its attached electronic channel. The drawback consists in the much more complex technology required.

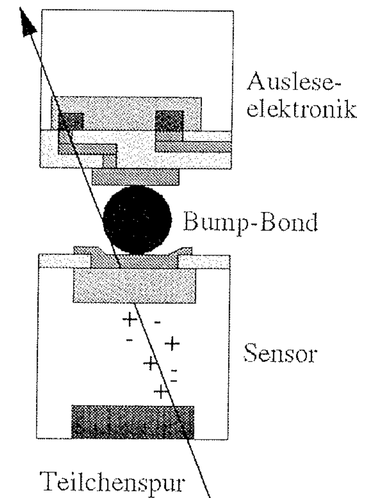


Fig. 8: Principle of sensor diode and amplifier connection via bump bonding used for ATLAS pixel detectors.

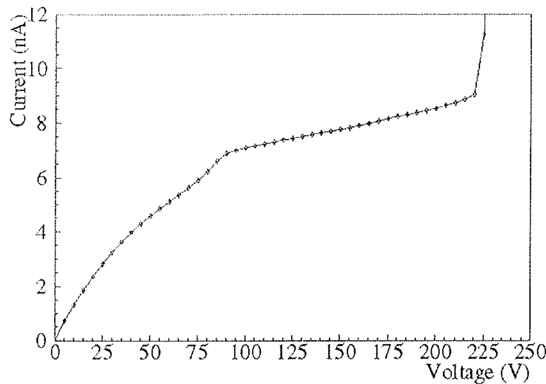
To avoid these complications an alternative concept was proposed. The idea bases on a field effect transistor (MOS or JFET) integrated on the surface of a fully depleted silicon detector. A potential minimum for generated charge carriers is located directly beneath the transistor channel forming an floating internal transistor gate. Charge carrier generated by particles or photons in the detector bulk drift into the potential minimum and control the transistor current /22/. Thus a signal amplification directly at position of detection is achieved. In contrast to the bump bonded device, sensor and related transistor are fabricated within the same technological process.

4.1 Diode Arrays bump bonded to Electronics

The inner detectors of LHC experiments will contain hybrid pixel detectors as described in /6/.

Pixel detectors for LHC experiments are heavily affected by the requirement of extreme radiation hardness (for instance up to 10^{15} hadrons/cm^2 during 10 years operation in the ATLAS-inner region). Here, the emphasis is put on the sensor design and operation while the electronic concept is discussed in detail in /6/.

The pixel cells consist of n-implants placed on n-bulk material (n on n device) /17/ while the junction is situated on the back side of the sensor surrounded by a multi guard ring structure. This choice which in comparison to the standard p^+n detectors requires a more difficult and expensive sensor fabrication technology (due to the needs of double sided processing and n-side inter-pixel isolation) is motivated by two reasons. During operation the radiation damage will increase the full depletion voltage of the pixel sensors to values well above the maximum forseen bias voltage of 600 V. Because of the effective p-doping of the bulk after irradiation the depletion region then extends from the n-pixels into the bulk. Because the electronics does not need the whole signal of the fully depleted detector, the detector can be operated partially depleted as a trade off between a reduced operation voltage and a smaller signal. Furthermore the n on n concept allows to use pside guard structure only. That keeps the whole n-side of the sensor on ground potential. Thus the danger of disruptive discharges between the sensor and the very closely spaced front-end chip /17/ is avoided. For n-side interpixel isolation, the already mentioned p-spray technique was used. Figure 9 shows the IV-curves of 1 cm^2 large test detectors before and after irradiation /18/. The irradiation was done with 1.1 x 10^{15} pions/cm^2.



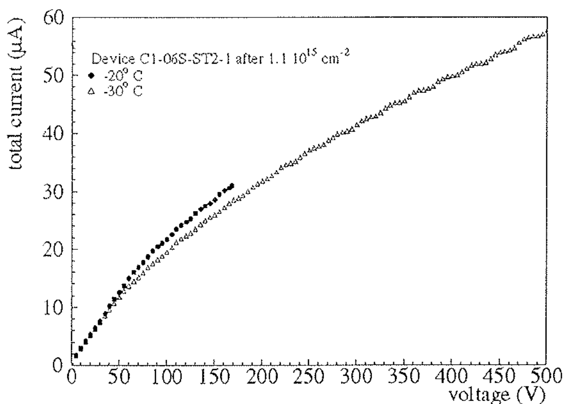


Fig. 9: IV-curves of 1 cm^2 n on n ATLAS-Pixel test detectors before and after an irradiation of 1.1 x 10^{15} pions/cm^2. The devices were fabricated by CiS (Germany).

The break down voltage of the unirradiated device is about 200V. Breakdown occurs at the electric field maxima located at the n pixel - p-spray junction. After irradiation, much higher operating voltages be used as a result of the reduced electric fields /10/. A further publication, especially of source measurements of irradiated sensors with flip-chip bonded ATLAS pixel electronics is in preparation /21/.

4.2 DEPMOS, DEPFET as detectors

The DEPleted Field Effect Transistor structure simultaneously has the functions of detector and amplifier. Its working principle is most easily explained by comparing it to a standard field effect transistor (Figure 10). Out of the various types of FET structures which can be used for this new device we have chosen the p-channel MOS enhancement transistor. The standard transistor shown on the top part of the figure is located on an undepleted n-doped bulk kept at substrate potential V_{bias}. The p-doped source and drain are connected through an inversion layer, the transistor channel. The transistor current is steered by the potential of the metal gate on top of the insulating gate oxide. It is worth noting that this current may also be modulated by varying the substrate potential. This usually unwanted feature is called bulk effect.

Adding a large area diode on the back, one may deplete the bulk from the backside, similarily as was done with the structure shown in Figure 4 which lead us to the drift

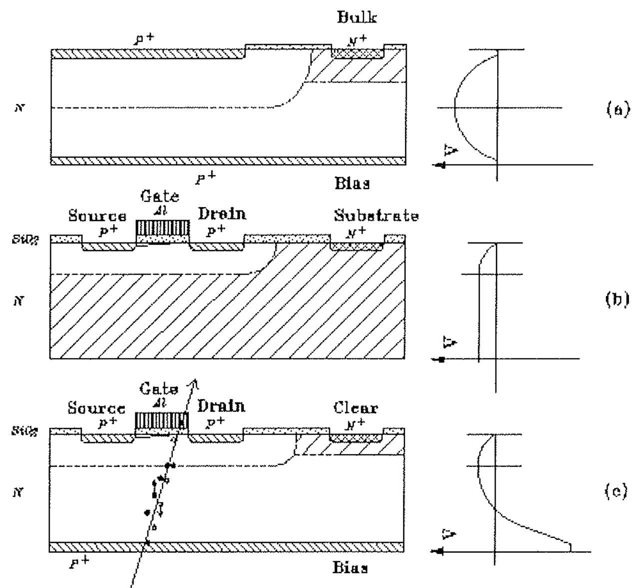


Fig. 10: Operation principle of a DEPMOS detector. The structure is arranged on a fully depleted high ohmic bulk acting as conversion volume for incident irradiation. The generated electrons drift to the potential minimum beneath the transistor channel steering its current.

chamber concept. Once a sufficiently negative voltage has been applied on the back the bulk underneath the transistor structure will be fully depleted of charge carriers and a potential energy minimum will be present underneath the transistor. Obviously for functioning of the transistor only the potential at the valley is important independent of the depletion status in the region below it.

If we now have an ionizing particle incident e.g. from the bottom side, the signal holes will move towards the large area diode while the electrons are caught in the potential minimum below the transistor (with suitable doping in the region below the gate). They will by influence induce opposite charge in the channel and thus increase the transistor current.

The DEPFET structure has some extraordinary properties which make it extremely interesting for detector applications:

- As it is simultaneously detector and amplifier, the problem of matching the amplifier to the detector does not arise and parasitic capacitances due to connections between detector and amplifier are absent. This gives at least a factor of two improvement in noise performance.
- The signal size is proportional to the ratio of the transconductance over the (external) gate capacitance, the thermal (output) noise proportional to the square root of the transconductance. Thus a very high signal to noise ratio may be obtained by shortening the gate length and width and increasing the oxide thickness.
- The signal charge located in the energy minimum underneath the gate can be completely cleared by a short pulse on a nearby clearing electrode. Thus clearing does not contribute to noise.
- As the measurement of signal charge is based on a change of the transistor current by means of influence, the signal charge is not destroyed and repeated readout is possible.

The detector principle has been experimentally confirmed /23, 24/ and provided immediately very good noise performance. Here a p-channel JFET was used as basic device in order to reduce the inherent channel noise. Equivalent noise values of about 20 electrons have been achieved at room temperature.

Due to the special properties of the DEPFET structure a variety of applications is possible ranging from readout devices for drift detectors and CCDs to completely new devices. For instance, a pixel detector can be composed by an array arrangement of DEPFET transistors. Such a device has already been proposed in the original paper /22/ and the proper functioning of a 8 x 8 pixel prototype has been demonstrated in /23/.

5 Technological Challenges

In the radiation detectors discussed so far, the whole silicon bulk acts as conversion volume for incident radiation or particles. For a fast charge loss free signal detection the bulk has to be completely depleted and this requires the use of rather high ohmic silicon substrates produced by flow zone technique.

The relationship between the depletion voltage and the detector thickness is simply given by the dependence of the depletion width versus applied reverse bias voltage for an asymmetric abrupt pn-junction. For instance, to deplete a 280 μm thick detector with a bulk doping of 10^{12} cm^{-3} a bias voltage of about 60 V is needed.

A major breakthrough in the field of semiconductor detectors was the first implementation of the planar technology /25/ which allows to take full advantage of the technological progress made in microelectronics. Especially the use of photolithography and ion implantation as doping technique leads to much more advanced detector devices. However, there are still many special processing steps required that forbid detector processing on standard microelectronics production lines. The detector backside has to be protected against scratches and other mishandling. More than this, many device concepts need photolithographic steps on both wafer sides. The large generation volumes and the in most circumstances not allowed implementation of classical gettering techniques require a very clean processing in order to achieve leakage currents below 1 nA/cm^2 for a full depleted device at room temperature. In the meantime the detector sizes start to extend an area of 35 cm^2 and more. This means that there is only one device at a 4 inch wafer. For such situations the yield problem has to be addressed in a new way. One serious defect systematically introduced at a critical position may not only cause malfunctioning of devices on many wafers but can even ruin a whole production run. To produce even larger devices the entry into the 6 inch technology is expected rather soon.

6 Summary - Outlook

We wanted to give an overview about the current status of silicon detectors. In the field of tracking detectors silicon detectors are very established due to their fast response time and high position resolution. They are able to cover a large detection area requiring a moderate number of electronic read out channels. The main challenges to strip detectors mainly driven by the LHC experiments at CERN are the improvement of radiation hardness and the reduction of production costs. To avoid ambiguities in vertex detection the very inner regions of high luminosity detectors will be equipped with pixel diode arrays bump bonded to electronics. For highly irradiated double sided strip detectors and n on n devices like the ATLAS pixel sensors the p-spray isolation technique is a good method to provide excellent high voltage operation capapility without producing excess noise induced by impact ionization.

In the last decade there was significant progress in the field of spectroscopic detectors. The silicon drift chamber has been elaborated in a way that an on chip amplification transistor and a voltage devider were integrated. These devices achieve energy resolutions at moderate temperatures provided by Peltier cooling. Simultaneously the signal rate capabilities have been increased by order(s) of magnitude. The avoidance of bulky nitrogen cooled apparatuses which were needed earlier allow the building of portable measurement systems for a variety of x-ray analysis techniques. Detectors based on the DEPMOS/DEPFET principle have the

potential to cover both fields of application, tracking as well as spectroscopy providing fast signal amplification together with high energy and position resolution.

References

/1/ J. Kemmer and G. Lutz, *New structures for position sensitive semiconductor detectors*, Nucl. Instr. & Meth. A 273 (1988) 588-598

/2/ P. Azzi et al.: Radiation *damage experience at CDF with SVX,* Nucl. Instr. & Meth. A 383 (1996) 155-158

/3/ L. Andricek et al., *Single sided p^+n and doubLe sided silicon strip detectors exposed to fluences up to 2x 10^{14}/cm^2 24 Ge V protons.,* presented at the 7th Pisa meeting on advanced detectors, La Biodola, Isola d'Elba, May 25-31, 1997, Nucl. Instr. & Meth. A 409 (1998) 184-193

/4/ A. Bischoff et al, *Breakdown protection and long term stabilisation for Si-detectors,* Nucl. Instr. & Meth. A 326 (1993) 27-37

/5/ E.H. Nicollian and J.R. Brews: *MOS (Metal Oxide Semiconductors) Physics and Technology.* John Wiley and Sons, New York, Chichester, Brisbane, Toronto, Singapore,1982.

/6/ The ATLAS collaboration, *ATLAS TDR 11,* CERN/LHCC/98-13

/7/ 2nd RD4B STATUS REPORT; CERN/LHCC 98-39, 21 October 1998

/8/ HERA-B Design Report, DESY-PRC 95/01,1995

/9/ J. Kemmer and G. Lutz, *Concepts of simplification of strip detector design and production,* Nucl. Instr. & Meth. A 326 (1993) 209-213.

/10/ R.H. Richter et al., *Strip detector design for ATLAS and HERA-B using two-dimensional device simnlation,* Nucl. Instr. & Meth. A 377 (1996) 412-421

/11/ R.C. Alig, S. Bloom, C.W. Struck, *Scattering by ionization and phonon emission in semicondnctors,* Phys. Rev. B, Vol. 22, No.12 (1980) 5565.

/12/ E. Gatti and P. Rehak, *Semiconductor Drift Chamber - An Application of a Novel Charge Transport Scheme,* Nucl. Instr. & Meth. 225 (1984) 608-614

/13/ E. Pinotti et al., *The pn-CCD- on-chip electronics,* Nucl. Instr. & Meth. A326 (1993) 85-91

/14/ L. Strüder et al., *High resolution X-ray Spectroscopy Close to Room Temperature to* be published in Microscopy and Microanalysis, 4, No 6,1999

/15/ A. Longoni et al., *A portable XRF spectrometer for non-destructive analyses in archeometry,* NIM, A 409 (1998), 407-409

/16/ K.H. Becks et al., *The Delphi pixels,* NIM A386 (1997) 11-17

/17/ T. Rohe et al., *Sensor design for the ATLAS-pixel detector,* Nucl. Instr. & Meth. A409 (1998) 224-228

/18/ F. Hügging et al., *Design and test of pixel sensors for operation in severe radiation environments,* presented at Elmau '98, to be published in Nucl. Instr. & Meth.

/19/ L. Strüder et al., *A 36 cm^2 large monolythic pn-charge coupled device x-ray detector for the European XMM satellite mission,* Rev. Sci. Instrum. 68(11), Nov. 1997, 4271-4274

/20/ H. Soltau et al., *Fabrication, Test and Performance of Very Large X-Rag CCDs Designed for Astrophysical Applications* presented at Elmau '98, to be published in Nucl. Instr. & Meth.

/21/ M.S. Alam et al, *The ATLAS silicon pixel sensors,* to be published in Nucl. Instr. & Meth.

/22/ J. Kemmer and G. Lutz, *New semiconductor detector concepts* Nucl. Instr. & Meth. A 253 (1987) 356-377

/23/ P. Klein et al., Nucl. Instr. & Meth. A305, 517 (1991)

/24/ G. Cesura et al., *New Pixel Detector Concepts Based on Junction Field Effect Transistors on High Resistivity Silicon.* Nucl. Instr. & Meth. A 377 (1996) 521-528

/25/ J. Kemmer, *Fabrication of low noise silicon radiation detectors by the planar process,* Nucl. Instr. & Meth. A169 (1980) 499-502

Dr. Rainer Richter
MPI Halbleiterlabor, Paul-Gerhardt-Allee 42,
81245 München, Germany

Dr. G. Lutz
Max-Planck-Institut für Physik,
München, Germany

Prispelo (Arrived): 15.02.1999 Sprejeto (Accepted): 03.03.1999

CHARACTERISATION AND MEASUREMENTS OF SILICON DETECTORS

Valter Bonvicini
INFN-Sezione di Trieste, Italy

TUTORIAL INVITED PAPER
MIDEM'98 CONFERENCE – Minisymposium on Semiconductor Radiation Detectors
23.09.98 – 25.09.98, Rogaška Slatina, Slovenia

Keywords: silicon radiation detectors, electrical parameters, parameter measurements, parameter influence on performance, energy resolution, position resolution, bias circuits, ENC, Equivalent Noise Charge, FOXFET, Field OXide Field Effect Transistors, GCD, Gate-Controlled Diodes

Abstract: An overview of the principal techniques and methods used to characterise silicon radiation detectors is given. These techniques allow to measure the most important electrical parameters of the detectors (leakage current, junction and inter-electrode capacitance, depletion voltage, etc.). The influence of these quantities on the detector's performance and on the achievable energy and position resolutions is discussed. Their knowledge is also of fundamental importance for the construction and understanding of the detector functional models. Experimental measurements illustrating the characterisation in the laboratory of some of the most used types of silicon detectors are given.

Karakterizacija in meritve silicijevih detektorjev

Ključne besede: detektorji sevanja silicijevi, parametri električni, merjenje parametrov, vplivi parametrov na zmogljivost, ločljivost energijska, ločljivost položajna, vezja napajalna, ENC naboj šumni ekvivalentni, FOXFET transistorji z učinkom polja poljsko-oksidni, GCD diode z vrati krmiljenimi

Izvleček: Prispevek podaja pregled glavnih tehnik in metod za karakterizacijo silicijevih detektorjev sevanja. S pomočjo teh metod lahko izmerimo najbolj pomembne električne parametre detektorjev (zaporni tok, kapaciteta spoja in med elektrodami, napetost osiromašenja itn.). Obravnava tudi vpliv teh parametrov na delovanje detektorja in na dosegljivo energijsko in pozicijsko ločljivost. Poznavanje teh parametrov je v osnovi pomembno za načrtovanje in razumevanje funkcijskih modelov detektorja. Podani so tudi eksperimentalni rezultati, kot primer karakterizacije nekaterih najbolj uporabljenih silicijevih detektorjev v laboratorijskem okolju.

1. INTRODUCTION

Semiconductor detectors are nowadays one of the most powerful tools for radiation detection and measurement in many experimental physics research fields. High Energy Physics, Nuclear Physics, Cosmic and Gamma-ray Astrophysics, Medical Imaging, X-ray spectroscopy, have all taken great advantage from the impressive development of the semiconductor detector technology during the last 20 years. Although germanium is still widely used, for its high efficiency, in gamma and X-ray spectroscopy, and although research and development in other semiconductor materials (such as GaAs, for instance) are giving encouraging results, silicon remains undoubtedly the most used and reliable semiconductor material for detector fabrication. The possibility to realise high-resistivity, high-purity substrates with very high mobility and lifetime of the charge carriers and the existence of an advanced, reliable and continuously upgraded technology (the planar process of the microelectronics) have determined its success. Actually, the application of the planar process to the production of silicon detectors (first introduced by J. Kemmer in 1972 /1/) was a landmark in the development of these devices. Since then, starting from the simple single-sided microstrip detectors, increasingly sophisticated detectors for position and energy measurements have been produced and employed: microstrip detectors with integrated coupling capacitors and DC-biasing structures /2/, double-sided microstrip detectors with both p-implant /3, 4/ and field-plate separation /5, 6/ of the n^+ strips, silicon pixel detectors /7, 8, 9/, Charge Coupled Devices (CCDs, /10/), Silicon Drift Detectors (SDDs, /11, 12, 13/), fully-depleted p-n CCDs /14, 15/. Whatever the type of the device, an accurate laboratory measurement of its electrical parameters is of fundamental importance for a correct detector operation in the experiment and for obtaining the desired performance. Basically, the laboratory characterisation has to allow for:

1) ensure that, for a given device, all the functional parameters are within the previously fixed acceptance limits;
2) study and understanding the electrical model of the detector;
3) control the technology and possibly give a feedback for improving some processing steps.

In the next Section, the influence of the detector's parameters on the overall signal-to-noise ratio and, hence, on the achievable resolution of the system (detector + readout electronics) will be reviewed. In Section 3, the basic techniques for detector characterisation will be illustrated with examples of measurements performed on different detector types. Section 4 briefly illustrates the importance of the measurements performed on *ad hoc* designed "test structures" for the determination of extremely important quantities (such as the charge carrier generation lifetime, for instance). Finally, conclusions are drawn in Section 5.

2. DETECTOR, BIAS NETWORKS AND EQUIVALENT NOISE CHARGE

Figure 1 sketches the layout of a generic charge measuring system. The detector is modelled as a capacitive current source, delivering in a very short time a charge Q on the parallel of the total detector capacitance C_D and the preamplifier input capacitance C_i. It should be noticed that the real preamplifiers usually differ from the simple voltage-sensitive configuration of Figure 1, but the general concepts introduced hereafter are practically independent on the preamplifier's configuration.

The noise sources of the system can be represented by a series voltage generator with a spectral power density $a(\omega)$ and by a parallel current generator with a spectral power density given by $b_1(\omega) + b_2(\omega)$ /16/.

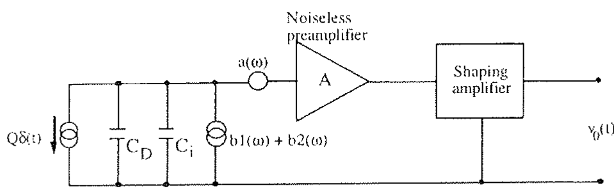


Fig. 1. General representation of an analogue front-end for charge measurement, with the noise sources represented by the equivalent generators a(ω) and b1(ω) + b2(ω).

The term $a(\omega)$ is characteristic of the preamplifier and in general we have:

$$a(\omega) = a_1(\text{white}) + \frac{a_2}{|\omega|} \qquad (1)$$

where the term a_1 is due, depending on the type of input active device employed, whether to the shot noise in the collector current for a BJT or to the thermal noise in the channel for an FET (both junction and MOS). In Eq. 1, the "$1/\omega$" part of the series spectral power density is negligible for BJTs, small for JFETs and rather important for MOSFETs and GaAs MESFETs /16, 17/.

The parallel noise is split into two terms: b_1, which is again a contribution of the preamplifier (shot noise in the base current or in the gate current for a BJT or a JFET, respectively; it is virtually negligible for a MOSFET) and b_2, which is contributed by the detector and by the bias networks. Focusing now our attention on b_2, we have in general to distinguish two cases:

a) the detector is DC-coupled to the preamplifier (Figure 2a);

b) the detector is AC-coupled to the preamplifier (Figure 2b).

For the sake of simplicity, in both cases of Figure 2 the preamplifier uses as input active device a JFET and again the preamplifier is sketched as a voltage-sensitive one. Independently on the type of coupling, the detector contributes to the term b_2 in the power spectral density of the parallel noise source of Figure 1 with a term

$$\Sigma_{det} = qI_L \qquad (2)$$

describing the shot noise associated to the detector's leakage current. Moreover, in the AC-coupling of Figure 2b there are two sources of thermal noise: one associated with the JFET bias resistor R_G and the other associated with the detector bias resistor R_P. The resulting spectral power density is given by

$$\Sigma_T = 2kT\left(\frac{1}{R_G} + \frac{1}{R_P}\right) \qquad (3)$$

Therefore, from Eqs. (2) and (3) we have that, in the case of AC-coupling, the parallel noise generator b_2 of Figure 1 has the following expression:

$$b_2 = qI_L + 2kT\left(\frac{1}{R_G} + \frac{1}{R_P}\right) \qquad (4)$$

Clearly, for the configuration of Figure 2a (DC-coupling), the expression is

$$b_2 = qI_L + \frac{2kT}{R_G} \qquad (5)$$

So far we have seen that two parameters of the detector (namely, its leakage current and, when present, its bias resistor) represent two noise sources that enter into the formulae describing the parallel noise. But another detector parameter, though being not a physical noise

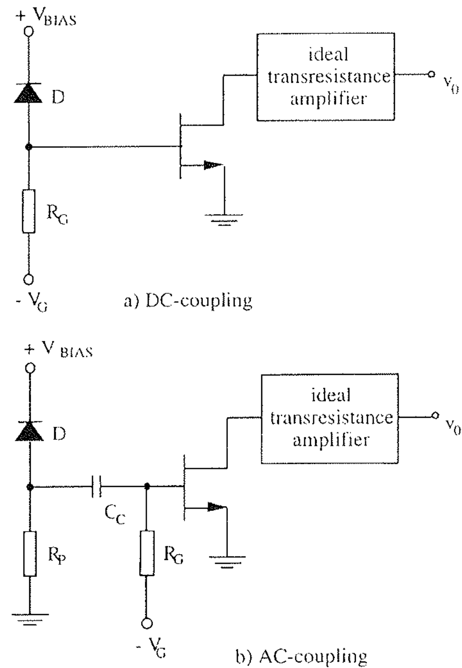


Fig. 2. Schematic illustration of the two types of coupling between detector and preamplifier. The detector is modelled as a diode D reverse-biased by the applied voltage V_{BIAS}.
a): DC-coupling; b): AC-coupling.

source, is of key importance in determining the noise level of the read-out electronics. This is the detector load capacitance C_D, i. e. the total capacitance presented by the detector at the preamplifier's input. It can be shown /16/ that the general expression for the Equivalent Noise Charge (ENC, that is the amount of charge at the input for which the signal-to-noise ratio at the output reduces to unity) for a system like that of Figure 1 can be written as:

$$ENC = \left[h_1 \frac{a_w}{\tau_M}(C_D + C_i)^2 + h_2 a_{1/f}(C_D + C_i)^2 + h_3(b_1 + b_2)\tau_M\right]^{1/2} \quad (6)$$

where h_1, h_2 and h_3 are numerical constants whose values depend on the particular type of shaping and τ_M is the shaping time. In Eq. (6) the explicit form of a_w, $a_{1/f}$, b_1 and b_2 depends, as we have seen, on the type of active input device in the preamplifier and on the type detector-preamplifier coupling. Therefore, the detector parameters play an essential role both in the series white noise (through the detector capacitance C_D) and in the parallel noise (through the spectral power density b_2).

The relative amount of signal charge and noise determines the energy and position resolution (and even the detectability of the signals) in all devices mentioned in Section 1. In the case of detectors with segmented electrodes (such as silicon microstrips) it is well known that analogue readout of the signals collected by the strips permits the use of interpolation methods that greatly enhance the position resolution /18/. For example, let us consider a microstrip detector having an amplifier pitch p_a; if the centre-of-gravity method is used as interpolation algorithm, than the achievable position resolution σ is given by /19, 20/:

$$\sigma \approx \frac{a_{cf} \cdot ENC \cdot p_a}{Q_s} \quad (7)$$

where ENC is the equivalent noise charge for one amplifier, Qs is the signal charge produced by the ionising particle and a_{cf} is a constant called "centroid finding constant", which determines the error in centroid finding and whose value depends on the correlation of the noise from adjacent preamplifiers and on the number of preamplifiers used in centroid finding. For example, for uncorrelated noise and using the outputs of 3 adjacent preamplifiers, $a_{cf} \approx 2$.

3. MEASUREMENT OF DETECTOR PARAMETERS

3.1 General considerations

As it is well known, analysis and characterisation of semiconductor "bare" (i. e. not encapsulated) devices should be performed in adequate environments ("clean rooms") with dedicated equipment and adopting precise precautions for handling. Silicon radiation detectors do not constitute an exception to this rule. The basic instrumentation for silicon detector tests consists of a "probe station", i.e. a micrometric table with a microscope mounted on top of it. The DUT (device under test) is mounted on a special support (the "chuck") and held in place by vacuum. Special coaxial probes terminating with tungsten (or tungsten carbide) needles are used to contact the micrometric structures on the device. The needles can be moved accurately under the microscope by micrometric screws. Probe stations can be either manual or automatic and in the last case the movements are executed by computer-programmed stepping motors. Often, when dealing with highly segmented detectors (e. g. microstrips), special printed circuit boards, called "probe cards", are used. These boards can house a large number of needles with the same pitch as the structures to be contacted on the DUT, thus speeding up and simplifying the measurements.

The probe station is usually enclosed in a grounded metallic box that has the twofold function of keeping the DUT in a dark ambient and acting as a Faraday's cage. Coaxial cables are used to connect the probes (hence, the DUT) to the measuring instruments. A very basic equipment should consist of a voltage source-measuring unit (with a very high input impedance, in order not to affect the voltage measurements), a current source-measuring unit, a high-frequency C-V analyser and a quasi-static C-V meter. Often, some of these functions are performed by units integrated into a single instrument. Clearly, besides the above mentioned "minimal" instrumentation, other instruments usually equip a silicon detector laboratory. Unless otherwise specified, all the examples of measurements described in the next Subsections were performed in the Laboratory for Silicon Detectors of the Trieste INFN Section.

3.2 Leakage current measurements

Basically, all measurements of leakage current consist in doing an I-V characterisation of the diode(s). The number of contacts to be implemented on the device clearly depends on its type, biasing scheme and complexity.

For example, Figure 3 shows the results of a measurement performed on a DC-coupled pad detector de-

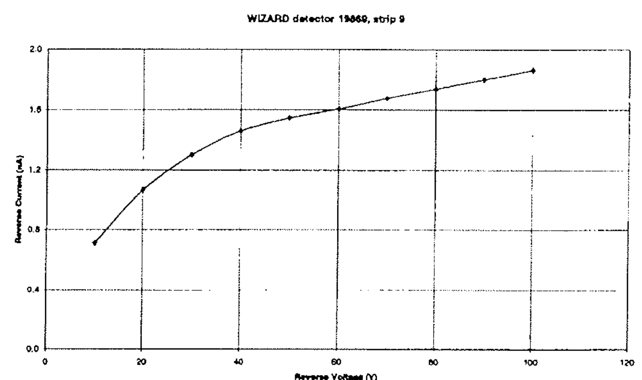


Fig. 3. Example of the measured leakage current as a function of the reverse voltage for one strip (implantation area of 59 x 3.6 mm²) of a WiZard detector (manufactured by Canberra Semiconductors N.V., Belgium)

signed and realised for the silicon-tungsten imaging calorimeter of the balloon-borne experiment WiZard for the search of anti-matter in Cosmic Rays /21/. The whole calorimeter is made by 1024 detectors arranged in 8 planes (each plane has two "views", one X and one Y), for a total surface of 3.68 m^2 of silicon. Each detector has dimensions of 6x6 cm^2, is 380 μm thick and has 16 pads or large strips with a pitch of 3.6 mm. A metallized p^+ implantation, the guard ring, surrounds the whole sensitive area and serves to collect the edge currents. For the strip shown, the current is about 1.5 nA/strip at full depletion, that was measured to be 55 V. The fact

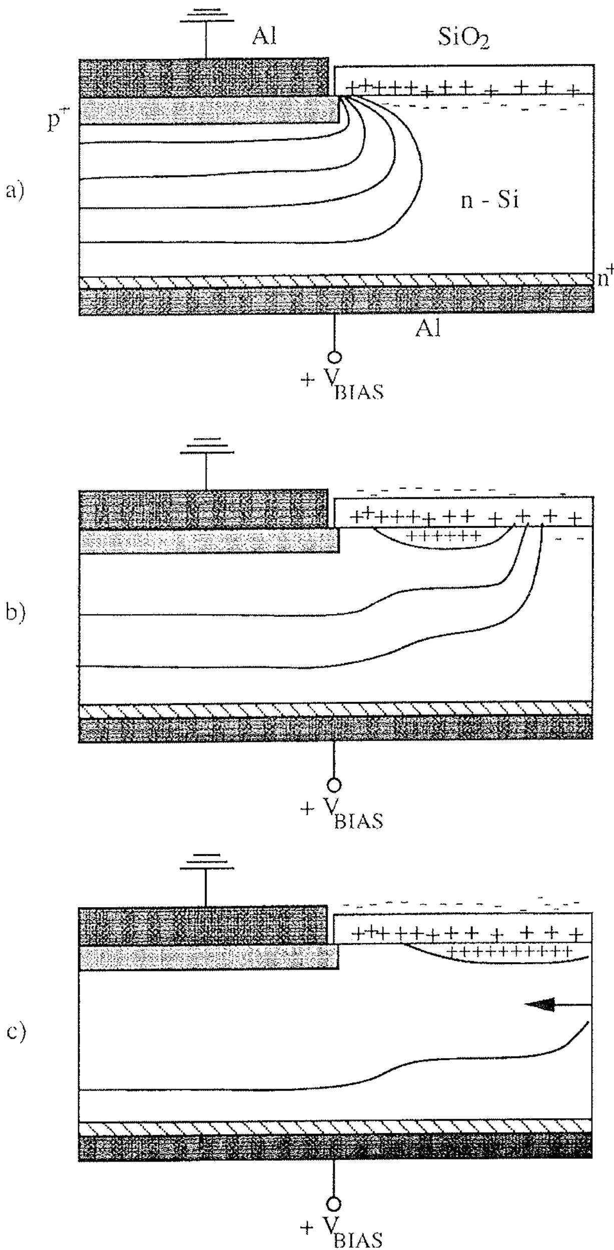


Fig. 4. Influence of environmental conditions on detector characteristics: a) without negative charge accumulation on outer silicon surface (high field at the junction edge); b) inversion layer due to accumulation of negative charge on the surface; c) extension of the depletion region to the damaged detector edge.

that the current does not saturates after the full depletion voltage indicates that, besides the bulk generated current, there is a non negligible contribution from the surface generation. A discussion of the contributions from bulk and surface generation to the leakage current is done in Section 4.

An important item to be controlled when analysing the leakage current is its stability in time. It is in fact well known that the reverse currents in a silicon detector may vary of orders of magnitude depending on the environmental conditions, sometime even many hours after having biased a seemingly perfect detector /22/.

These phenomena can be attributed to the charges trapped on the outer oxide surface. For example, if an uncovered oxide surface is exposed to humidity, typically negative charges are collected on that surface. These charges provoke the formation of an inversion layer under the oxide and this leads to an extension of the depletion region towards the detector's edge (Figure 4 a, b, c). If the depletion region reaches this edge, the current may increase by orders of magnitude due to the generation of electron-hole pairs in the crystal lattice damaged by the cut. On the other hand, in the presence of no or positive charges on the oxide surface (that may happen for instance in a very dry environment or in vacuum), the positive oxide charge at the Si-SiO2 interface is undisturbed in creating an electron accumulation layer in the silicon below the oxide. This may lead to very strong electric fields at the junction edges, and even to a junction breakthrough for potentials lower than the full depletion one. Again, the detector's surface may be protected by a highly resistive layer (such as polyimide), which may be charged by the metal electrodes in an unpredictable way because of local variations in the material's resistivity. Therefore, a careful stability measurement of the leakage current is mandatory. Figure 5 shows the result of such a measurement performed on a WiZard detector for 112 hours at the operating bias voltage (that in this case was defined as 10% above full depletion). As it can be seen, the reverse current presents an excellent stability.

Usually, the selection of detectors is made on the basis of the current in the active area, this means that the current collected by the guard ring(s) is of no matter in the acceptance or rejection of a device. Nevertheless, this is not the case for balloon or satellite-borne devices.

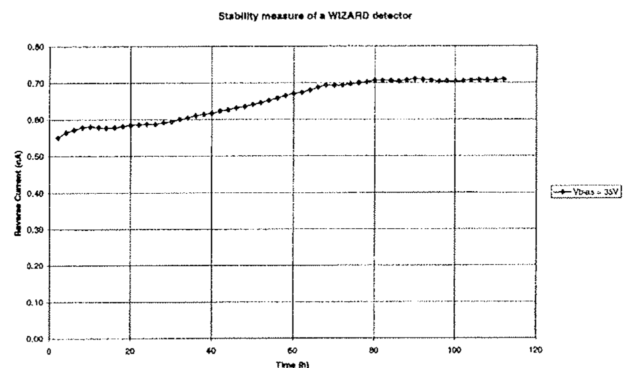


Fig. 5. Result of a stability measurement (112 h) performed on a WiZard strip detector (manufactured by SINTEF, Oslo, Norway). The current on a single strip is shown.

Since in these experiments a very limited power budget is available, a large or unstable (continuously increasing) current is not acceptable, even if it does not affect the detector's performance.

3.3 Integrated biasing structure measurements: the FOXFET

In case of AC-coupled strip detectors, a DC-biasing structure for the strip leakage currents has to be provided. This can be accomplished either with polysilicon resistors of suitable value, which connect each strip to a common bias line /2/, or by a punch through effect from a guard ring /23/. With this last technique it is possible to avoid the polysilicon steps in the processing, thereby using for capacitively coupled detectors the same technology as for direct coupled ones. Sometimes, a metal gate electrode is placed on the oxide that covers the gap between the strips and the guard ring (Figure 6). In this way, by varying the gate potential, one can control the strip voltage. This gated punch through structure is usually referred to as a FOXFET (Field OXide, Field Effetct Transistor) /23, 24/. Since the gated punch through biasing technique presents more interesting items of discussion from the point of view of the measurements, it will be used as an example in this Subsection. In order to introduce the measurements to be performed on this structure, a brief and qualitative summary of its working principle is given hereafter. The interested reader can find a detailed, quantitative analysis in the literature /24-31/. The measurements shown here were performed on AC-coupled microstrip detectors designed and realised for the SYRMEP experiment (SYnchrotron Radiation for MEdical Physics), a digital radiology program which is in operation at the ELETTRA Synchrotron light source in Trieste, Italy. All details about the detector's design and performance can be found in Ref. /32/.

In the usual biasing scheme, the drain (i.e. the biasing guard ring) is held at ground potential with respect to the positive bias voltage applied to the backplane. As V_{BIAS} increases, the depletion layer of the drain junction

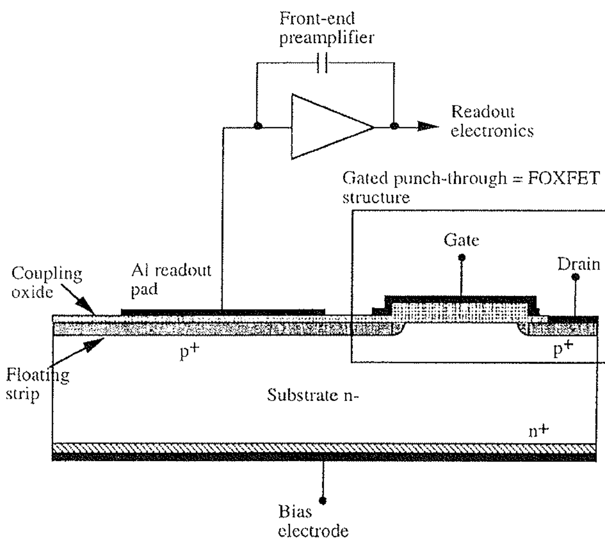


Fig. 6. Schematic illustration of a detector structure with AC-coupled floating strip junction and FOXFET biasing structure.

extends both towards the bulk and laterally towards the floating p+ strip. At the surface, a strong accumulation layer of electrons exists, which is due to the positive oxide charge in the field oxide /28/; obviously, this accumulation layer effectively inhibits the spreading of the depletion layer at the surface. Therefore, the two junctions are "isolated" and a potential difference is established between them as V_{BIAS} increases. Hence, since the strip is floating, its potential initially "follows" the bias voltage: Figure 7 shows a typical measured strip voltage as a function of V_{BIAS}, with the gate voltage (V_{GATE}) as parameter.

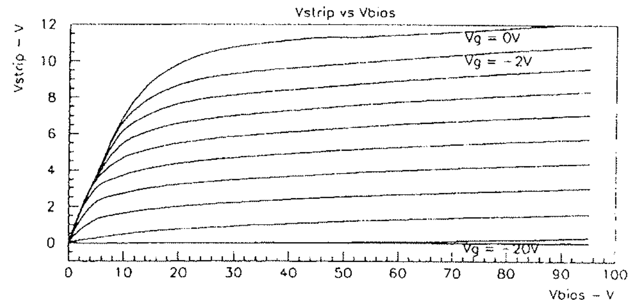


Fig. 7. Typical result of a strip voltage vs. bias voltage measurement (with the gate voltage as a parameter) performed on a Syrmep microstrip detector (manufactured by Canberra Semiconductors N.V., Belgium)

The input impedance of the measuring instrument (Hewlett Packard 4142B) was $> 10^{12}\ \Omega$, and therefore the strip voltage was practically not affected by the measurement. When the punch through between the two junctions (the strip and the drain junctions) is reached, the strip voltage tends to settle and an effective reverse bias exists between the strip and the n bulk. In terms of current, the mechanism can be described in the following way: since the strip junction is reverse biased towards the substrate, it needs to be forward biased in a certain point in order to satisfy Kirchhoff's Current Law (condition of zero net current entering and escaping the strip). As a result, the strip leakage current (holes from the n-type substrate) is injected back into the substrate and flows through the channel into the drain junction as punch through current /31/. It should be noticed that this current flow does not take place at the silicon-oxide interface, but rather in the bulk of the device, a few microns below the surface, due to the presence of the electron accumulation layer /29, 31/.

By applying a negative voltage to the gate electrode, the punch-through voltage gets smaller, since the applied field partly compensates the one due to the positive oxide charge, thereby reducing the electron accumulation layer. At a certain gate voltage (- 20 V in Figure 7), the applied field is strong enough to fully compensate the positive oxide charge; the accumulation layer at the Si-SiO_2 interface vanishes and the strip voltage is zero, indicating that the channel is close to the inversion mode and therefore the transistor is turning on. The biasing structure showed excellent results for all the measured detectors; the maximum variation of the strip voltage over 256 strips was 3.1 V, while the

local variations among neighbouring strips were always below 0.4 V. The resulting distortions in the drift field are practically negligible.

A very important parameter in the FOXFET is the so-called dynamic resistance, defined as

$$R_d = \frac{\partial V_{STRIP}}{\partial I_{STRIP}} \quad (8)$$

where V_{STRIP} is the strip voltage and I_{STRIP} the current flowing from the strip to the drain. As we have seen in Section 2, the value of the bias resistor in AC-coupled detectors enters into the expression of the spectral power density of the parallel noise generator b_2 (see Eq. 4). In order to minimise this contribution, the value of R_d has obviously to be large. In the case of the Syrmep detector-electronics system, values of dynamic resistance below 20 MΩ start to contribute significantly to the total noise /32/ The dynamic resistance value is known to be determined (for a given FOXFET geometry) almost entirely by the leakage current: it is extremely high at low currents and it decreases as the current increases approximately as I^{-1}; the dependence of R_d on the gate voltage is very poor, at least until the transistor threshold voltage is reached /28, 31/. When characterising FOXFET-biased detectors, one is mainly interested in measuring the dynamic resistance in operating conditions, i.e. as determined by the leakage current flowing in the strip at operating bias voltage. This means to force small variations of strip current around the "quiescent" value I_L and record the corresponding changes in strip voltage V_{STRIP}. To do so, we used the measurement set-up schematically illustrated in Figure 8; the current monitor/source that was used can measure currents down to 100 fA.

A typical result is shown in Figure 9; here, $I_S = 0$ means that no current flows from or to the external current source, i.e. the strip current is the quiescent leakage current I_L. For negative values of Is the instrument acts as a current sink, while for positive values of Is the instrument adds current to I_L. The dynamic resistance,

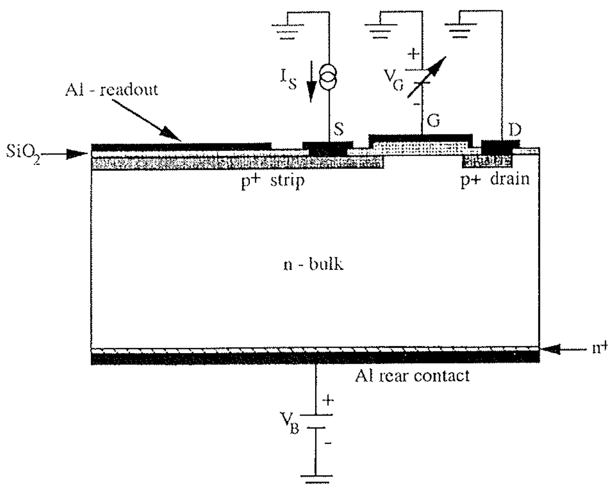


Fig. 8. Schematic illustration of the set up used to perform the I-V and dynamic resistance measurements of the biasing structure.

obtained as the slope of a linear fit of the measured points, was about 60 MΩ for this strip, which corresponded to a leakage current of ≈ 1.5 nA.

3.4 Capacitance measurements

As it was evidenced in Section 2, load capacitance is one of the most significant parameters determining the noise level of the readout electronics. Let us first consider the case of microstrip detectors. In this case, the significant contributions are those from the other strips on the detector surface and also from the backplane. The relative importance of these two contributions depends on the detector characteristics: implant and metal strip pitch and width, capacitive or direct coupling to the readout electronics, type of doping, etc. /33/. As a general statement, one can say that if the strip pitch is much smaller than the detector thickness, the interstrip capacitance C_{is} between two adjacent strips dominates over the junction capacitance C_j of a single strip to the backplane.

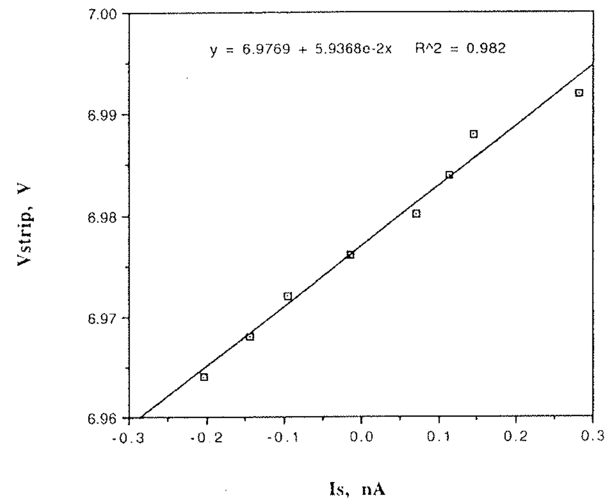


Fig. 9. Result of a dynamic resistance measurement: the value of R_d is obtained from a linear fit of the measured data.

It is important to simulate the detector operation in real experimental conditions, where every strip is held at a well defined potential through an amplifier. To do so, one can use the stitchbonding technique to connect together all the strips except those which have to be measured (Figures 10 and 11). In this way, both junction and interstrip capacitance can be measured correctly. Figure 10 shows a diagram of the experimental set up employed to measure C_j on DC-coupled microstrip detectors /34/. The devices (manufactured by Canberra Semiconductors) had 52 strips each, having a length of 10 mm and a pitch of 200 μm. The implant width was 160 μm and the metal width 140 μm. The wafer thickness was 300 μm. A Keithley 590 CV Analyser was used; the measuring signal had a signal of either 100 kHz or 1 MHz and an amplitude of 15 mV rms. Data were taken at 100 kHz, but no significant differences were observed at 1 MHz. The strip under measurement was biased by keeping the backplane at a positive voltage with respect to the CV Analyser input.

When measuring low level capacitances, special attention must be paid to reduce parasitic effects. A subtraction of the parasitic capacitances (i.e. cables capacitance and capacitance between the probe contacting the measured strip and all other strips on the detector plane) has to be performed. With the above mentioned set up, this was done using the "open circuit correction" feature of the instrument. This consists in raising the probe tip of the strip under measurement at a fixed height (about 50 μm) and leaving all the rest equal. The

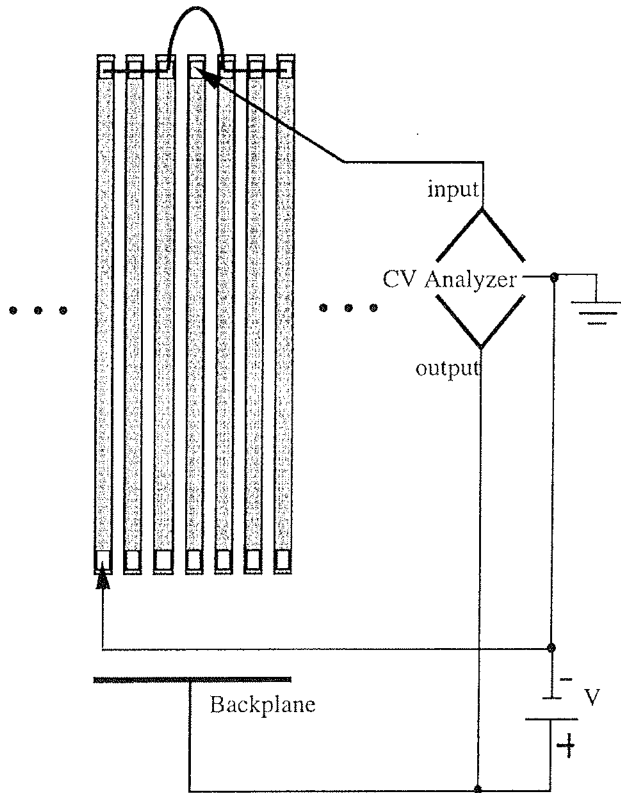


Fig. 10. Diagram of the experimental set up used for junction capacitance measurements.

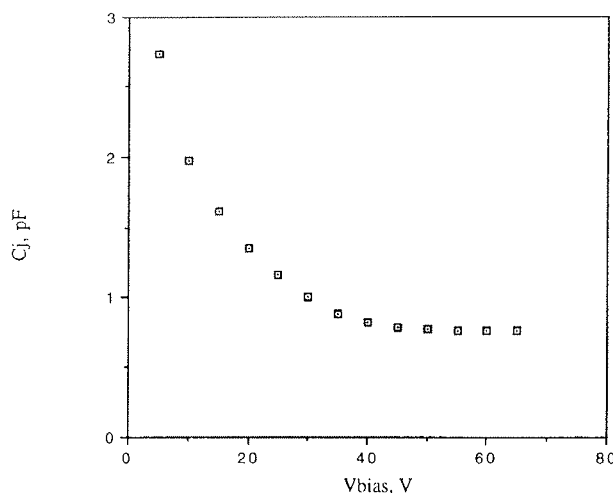


Fig. 11. Result of a junction capacitance measurement on the microstrip structures described in the text.

resulting parasitic capacitance measured is automatically taken by the instrument as the reference value ("zero") for the next measurements.

The typical junction capacitance measured is shown in Figure 11. The curve clearly shows the well known dependence on $1/\sqrt{V}$ expected for an abrupt junction (see Section 4). The measured C_j at full depletion was $\approx$ 0.75 pF.

Figure 12 shows the circuit used for interstrip capacitance measurements. The stray capacitance subtraction method is the same. One central strip (the one under test) was left out and 50 strips (25 on both sides of the central one) were stitchbonded together. In that way it was possible to evaluate the contribution of farther strips by disconnecting strips or groups of strips starting from the outer ones. Hence one can measure the interstrip capacitance as a function of the number of adjacent strips. The results obtained experimentally are plotted in Figure 13 versus the number of strips connected. It is apparent from that plot that, for these particular detectors, more than 90% of the total interstrip capacitance is contributed by the two closest neighbours and that the contribution of the strips beyond the fourth neighbours is completely negligible.

The measuring techniques described so far in this Subsection obviously apply also to other types of segmented silicon detectors, like e. g. pixel detectors. The interpixel capacitance measurements are nevertheless more complicated, due to the geometry of the system. Moreover, if one tries to disentangle the different contributions to the measured total interpixel capacitance, there is the difficulty represented by the diagonal pixels, whose contribution is not trivially evaluable. The interested reader can find in Ref. /35/ a discussion of the

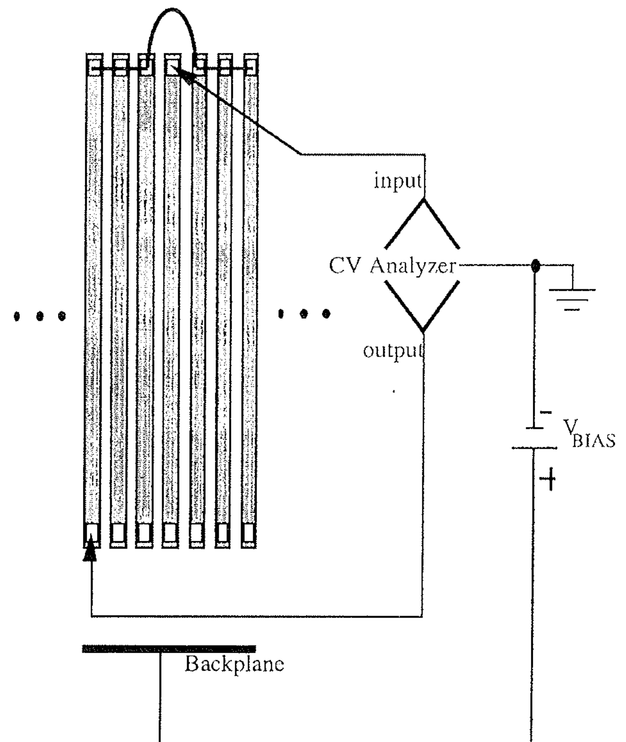


Fig. 12. Diagram of the experimental set up used for interstrip capacitance measurements.

pixel capacitances, together with a modellization of the interpixel capacitance on the geometry and experimental results on test structures.

When dealing with AC-coupled strip detectors, the basic considerations expressed so far still apply. Nevertheless, it should be clear that now that the quantity obtained by stitchbonding the metal readout lines (see Figure 12) and performing the above described measurement is effectively the capacitance of one strip with respect to its neighbours in real experimental conditions (that is what is more important for real applications), but is NOT, strictly speaking, the mere interstrip capacitance. In fact, what is measured in this case is a convolution of the coupling and interstrip capacitances. By constructing an adequate equivalent circuit of the capacitive network of the detector and knowing the value of the coupling capacitance, it is possible to calculate the true value of C_{is}. A measurement of the coupling capacitance C_c is therefore necessary. Anyway, besides the understanding of the capacitive model of the detector, this kind of measurement should be performed in order to control that the design value for C_c is met and to control the number of "pinholes", i.e. pierces in the coupling oxide. In AC-coupled detectors with integrated coupling capacitors, the rate of strips with pinhole defects is a key indicator of the quality of the oxide. The circuit to be used for coupling capacitance measurements is sketched in Figure 14. The coupling capacitance should be much larger (about 10 times at least) than between junction or interstrip capacitances, in order to avoid charge losses. For a correct measurement of C_c, a quasi-static CV meter has to be used.

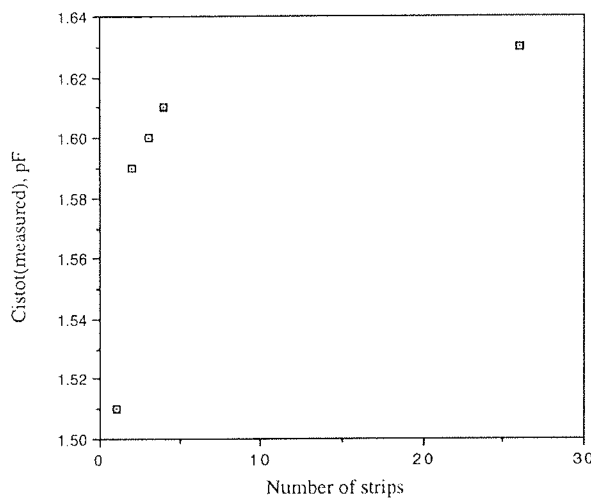


Fig. 13. Result of an interstrip capacitance measurement on the microstrip structures described in the text.

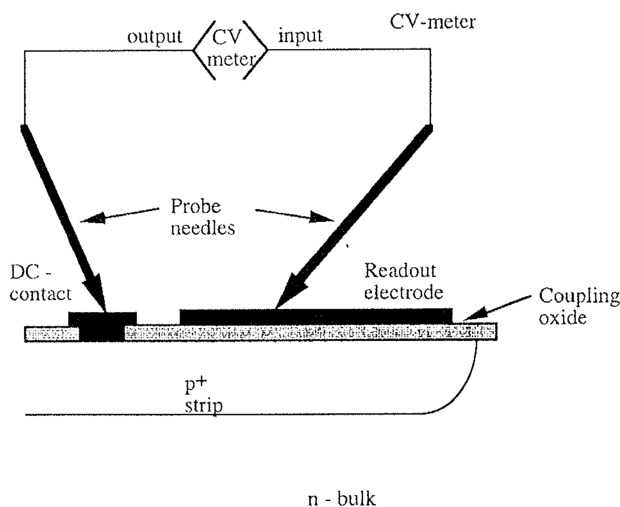


Fig. 14. Schematic of the circuit used to measure the coupling capacitors.

4. MEASUREMENTS ON DEDICATED TEST STRUCTURES

A certain number of devices (called "test-structures") is always realised on the detectors' wafers, usually around the main detector. Their purpose is to allow measurements of important physical quantities that ultimately determine the detector performance. The most important of these parameters are the bulk doping density, the charge carrier generator lifetime, the surface generation velocity and the oxide charge density at the Si-SiO_2 interface. The first two can be measured using diodes, the third using gate-controlled diodes and the last using MOS capacitors /36/.

In a p-i-n diode a measurement of the junction capacitance versus the bias voltage shows the well-known dependence given by the following formula /37/:

$$C(V) = \frac{\varepsilon_0 \varepsilon_r S}{t\sqrt{V / V_d}} \qquad (9)$$

where V is applied reverse voltage, V_d the total depletion voltage, t the substrate thickness, S the diode surface, $\varepsilon_0 = 8.85 \cdot 10^{-12}$ F·m^{-1} is the vacuum permittivity and $\varepsilon_r = 11.8$ is the relative dielectric constant of silicon. The depletion voltage is better evaluated by plotting $1/C^2$ versus V (Figure 15, where $1/C^2$ is expressed in $1/pF^2$ and V in volts). The linear dependence up to the depletion voltage clearly indicates that the bulk doping is constant.

Another measurements that is usually performed on p-i-n test diodes is the I-V curve. For a good junction,

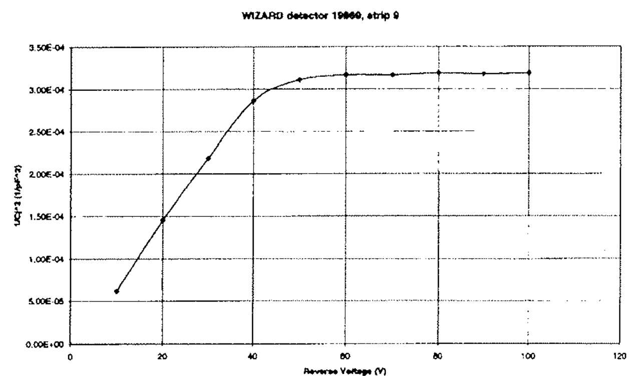


Fig. 15. Reverse bias voltage dependence of $1/C^2$: the full depletion voltage is clearly visible.

the reverse current should reach a plateau at total depletion; this would indicate that the current is practically due totally to bulk generation. If this is the case, the carrier generation lifetime τ can be evaluated according to the formula:

$$\tau = \frac{qn_iSt}{2I_L} \quad (10)$$

where q is the electron charge, n_i the intrinsic carrier concentration, S the diode surface, t the wafer thickness and I_L the measured asymptotic value of the current.

With a gate-controlled diode (GCD) it is possible to measure the surface generation velocity. In this structure, a metal gate partially overlaps, on top of the oxide, the bulk and implant regions of a diode (see Figure 16). For gate voltages positive with respect to the flat band voltage V_{fb}, the surface of the n region is accumulated and the surface depletion layer is minimum /38/. Therefore, the leakage current is determined by the generation of electrons and holes in the "metallurgical" junction, whose area (in section) is indicated by S_M in Figure 16. By calling I_{GB} this bulk generated current, one has immediately from Eq. 10:

$$I_{GB} = \frac{qn_i}{2\tau} S_M x_{db} \quad (11)$$

where x_{db} is the bulk depletion layer, that becomes equal to the wafer thickness τ at full depletion, and all other symbols are defined after Eq. 10.

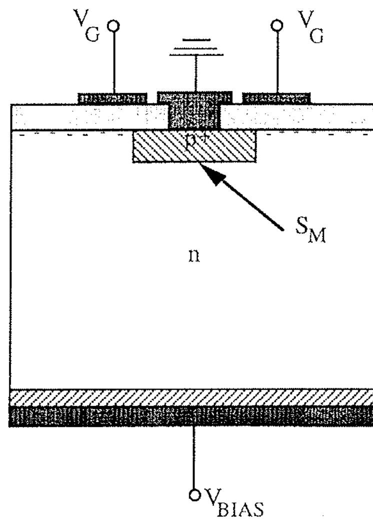


Fig. 16. A schematic cross section of a gate controlled diode structure for $V_G > V_{fb}$. In this case, the diode leakage current is virtually determined only by the generation in the "metallurgical" junction.

If the gate voltage V_G becomes more negative than the flat band voltage, the surface of the n region below the gate electrode is brought to depletion. Therefore, in addition to the current I_{GB}, there are now two other current components. First of all, there is a current due to the generation of carriers in the depletion region induced by the gate. This component, called "field induced junction current", is given by

$$I_F = \frac{qn_i}{2\tau} S_F x_{ds} \quad (12)$$

where x_{ds}, the thickness of the surface depletion region, is a function of the applied gate voltage, and S_F, the area of the surface depletion region, is determined by the over-lapping of the gate electrode on the n region. The second current component which takes place when the surface is depleted, is due to the activity of the surface generation centres. This component is given by

$$I_S = \frac{qn_i s_0 S_F}{2} \quad (13)$$

where s_0 is the surface generation velocity when the surface and the bulk are equi-potential /38/. The value of s_0 is directly proportional to the density of surface generation - recombination centres and is therefore strongly influenced by the process with which the device has been fabricated. Hence, the knowledge of s_0 is of great importance for the control and the improvement of the fabrication technology.

If the gate voltage is further decreased until the surface is brought to inversion, I_F in Eq. 12 increases to a maximum value when x_{ds} increases to its maximum value $x_{d,max}$. On the other hand, once the inversion has taken place, the surface hole density p_s is much larger than n_i and the surface generation velocity decreases strongly from the value s_0 /38/. Typically, $I_F < I_S$ when the surface is depleted; after inversion I_S becomes negligible and the reverse current becomes the sum of I_{GB} and I_F. In Figure 17 is reported the typical behaviour of the current experimentally measured in a GCD /36/. The three regions are clearly visible.

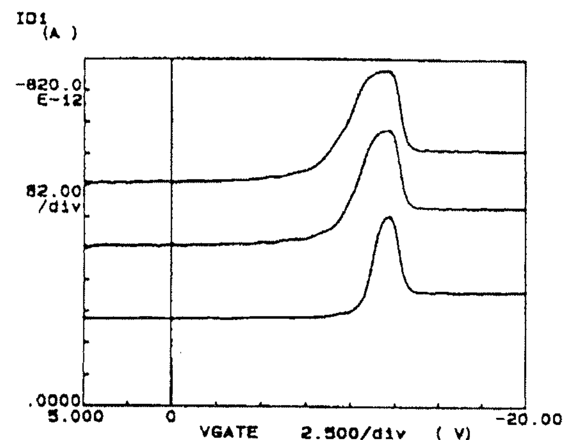


Fig. 17. GCD current versus gate voltage for three values of bias voltage (courtesy of L. Bosisio).

With MOS capacitors, an estimation of the oxide charge density Q_{ox} is possible by measuring the capacitance C as a function of the applied voltage V. The behaviour of the capacitance of an MOS structure as a function of the applied voltage is well known (/37, 38/): at low

voltages, the bulk is not depleted and the electron accumulation layer at the surface under the oxide is not perturbed. Increasing the reverse voltage V, the metal gate starts to be sufficiently negative (with respect to the bulk) to partially compensate the positive oxide charge, thereby reducing the electron accumulation layer. When the flat-band voltage (V_{fb}) is reached, the surface is brought in depletion mode. From the curve, the flat-band voltage Vfb can be determined and, assuming that the fixed oxide charges are concentrated at the interface, one can write /39/

$$V_{fb} \approx \frac{Q_{ox}}{C_0} = \frac{qN_F}{C_0} \quad (14)$$

where N_F is the number of oxide charge at the $Si\text{-}SiO_2$ interface, q is the electron charge. C_0 is the geometrical capacitance per unit area, which is given by

$$C_0 = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}} \quad (15)$$

where $\varepsilon_{ox}(SiO_2)=3.9$ and t_{ox} is the oxide thickness. From Eqs. (14) and (15) one can therefore estimate Q_{ox}.

5. CONCLUSIONS

This paper presented an elementary discussion about the laboratory characterisation of silicon radiation detectors. The relevance of the detector's parameters on the ENC, hence on the achievable energy and position resolution, has been overview. Some of the most important laboratory measurements have been illustrated with examples taken from experimental results. It has been shown that important physical properties of the silicon devices under test, that play a key role in determining the detector's performance, can be derived from standard measurements on simple structures.

ACKNOWLEDGEMENTS

The author thanks A. Vacchi (INFN Trieste) and L. Bosisio (University of Trieste and INFN) and A. Rashevsky (INFN Trieste) for useful discussions. Many thanks also to N. Zampa (INFN Trieste) for providing some of the plots shown in the article.

REFERENCES

/1/ J. Kemmer, Nucl. Instr. and Meth. 169 (1980) 499.
/2/ M. Caccia et al., Nucl. Instr. and Meth. A260 (1987) 124.
/3/ P. Holl et al., Nucl. Instr. and Meth. A257 (1987) 587.
/4/ G. Batignani et al., Nucl. Instr. and Meth. A326 (1993) 183.
/5/ R. Brenner et al., Nucl. Instr. and Meth. A326 (1993) 198.
/6/ R. Brenner et al., Nucl. Instr. and Meth. A326 (1993) 189.
/7/ S. Gaalema, IEEE Trans. Nucl. Sci. NS 32 (1985) 417.
/8/ H. Heijne et al., Nucl. Instr. and Meth. A273 (1988) 615.
/9/ P. E. Karchin, Nucl. Instr. and Meth. A305 (1991) 497.
/10/ C. Damerell, Nucl. Instr. and Meth. 226 (1984) 26.
/11/ E. Gatti and P. Rehak, Nucl. Instr. and Meth. 225 (1984) 608.
/12/ E. Gatti, P. Rehak and J. T. Walton, Nucl. Instr. and Meth. 226 (1984) 129.
/13/ P. Rehak et al., Nucl. Instr. and Meth. A248 (1986) 367.
/14/ L. Struder et al, Nucl. Instr. and Meth. A253 (1987) 386.
/15/ E. Gatti et al., Nucl. Instr. and Meth. A288 (1990) 168.
/16/ E. Gatti and P.F. Manfredi, Riv. Nuovo Cimento 9, ser. 3, no. 1 (1986).
/17/ W. Buttler et al., Nucl. Instr. and Meth. A288 (1990) 140.
/18/ R. Turchetta, Nucl. Instr. and Meth. A335 (1993) 44.
/19/ V. Radeka and R. Boie, Nucl. Instr. and Meth. 178 (1980) 543.
/20/ V. Radeka, Nucl. Instr. and Meth. 226 (1984) 209.
/21/ M. Bocciolini et al., Nucl. Instr. and Meth. A370 (1996) 403.
/22/ A. Bischoff et al., Nucl. Instr. and Meth. A326 (1993) 27.
/23/ J. Kemmer and G. Lutz, Nucl. Instr. and Meth. A273 (1988) 588.
/24/ C. Bauer et al, IEEE Trans. Nucl. Sci. NS-36(1) (1989) 267.
/25/ P. Holl et al., IEEE Trans. Nucl. Sci. NS-36(1) (1989) 251.
/26/ P. P. Allport et al., Nucl. Instr. and Meth. A310 (1991) 155.
/27/ P. P. Allport et al., Nucl. Instr. and Meth. A348 (1994) 416.
/28/ M. Laakso et al., Nucl. Instr. and Meth. A326 (1993) 214.
/29/ N. Bacchetta et al., IEEE Trans. Nucl. Sci. NS-40(6) (1993) 2001.
/30/ N. Bacchetta et al., IEEE Trans. Nucl. Sci. NS-40(6) (1993) 1602.
/31/ D. Križaj, V. Bonvicini and S. Amon, Nucl. Instr. and Meth. A384 (1997) 482.
/32/ F. Arfelli et al., Nucl. Instr. and Meth. A385 (1997) 311.
/33/ S. Masciocchi et al., Proceedings of the 1992 IEEE NSS, Orlando (USA).
/34/ V. Bonvicini et al, INFN /TC-94/14.
/35/ V. Bonvicini et al., Nucl. Instr. and Meth. A365 (1995) 88.
/36/ G. Batignani et al., Nucl. Instr. and Meth. A360 (1995) 98.
/37/ S. M. Sze, *"Physics of Semiconductor Devices"*, Wiley, 1981.
/38/ R. S. Muller and T. I. Kamins, *"Device electronics for Integrated Circuits"*, Wiley, 1977.
/39/ D. K. Schroder, *"Semiconductor Material and Device Characterisation"*, Wiley, 1990.

Valter Bonvicini
INFN-Sezione di Trieste
via A. Valerio 2, 34127 Trieste, Italy
e-mail: bonvicini@trieste.infn.it

Prispelo (Arrived): 25.09.1998 Sprejeto (Accepted): 03.03.1999

FRONT-END ELECTRONICS FOR ENERGY AND POSITION MEASUREMENTS WITH SEMICONDUCTOR RADIATION DETECTORS

Valerio Re
Dipartimento di Ingegneria, Università di Bergamo, Italy
Lodovico Ratti
Dipartimento di Elettronica, Università di Pavia, Italy

TUTORIAL INVITED PAPER
MIDEM'98 CONFERENCE – Minisymposium on Semiconductor Radiation Detectors
23.09.98 – 25.09.98, Rogaška Slatina, Slovenia

Keywords: solid-state detectors, solid-state radiation detectors, energy measurement, position measurement, FEE, Front-End Electronics, X-ray spectrometry, GAMMA-ray spectrometry, X-ray imaging, GAMMA-ray imaging, particle tracking, HEP, High Energy Physics, state-of-the-art, problem solutions, design of implementations, ultra low noise, signal preamplification

Abstract: Semiconductor radiation detectors are presently used in many areas of physics research, from X and γ- ray spectrometry and imaging to particle tracking in high energy physics experiments. Front-end electronics have to comply with the requirements set by the different detector applications, such as low noise, to get high energy and position resolution, high speed, radiation tolerance and operation at cryogenic temperatures. Highly segmented detectors stimulated the development of readout circuits in monolithic form, and special integration technologies were purposely developed to achieve optimum performances. After reviewing the basic problem of front-end design, the paper presents solutions which have been adopted in specific applications, such as ultra low noise preamplification for X and γ- ray spectrometry, and analog processing of signals delivered by silicon microstrip detectors. The examined circuits range from all-JFET monolithic charge-sensitive preamplifiers, where a non resistive feedback technique can be used for minimum noise performances, to a mixed-signal multichannel CMOS integrated circuit containing the complete readout electronics for a silicon vertex tracker in a collider experiment.

Čitalna elektronika za meritev pozicije in energije pri polprevodniških detektorjih sevanja

Ključne besede: detektorji polprevodniški, detektorji sevanja polprevodniški, merjenje energije, merjenje položaja, FEE elektronika čelna, spektrometrija X-žarkov, spektrometrija GAMA-žarkov, upodabljanje X-žarkov, upodabljanje GAMA-žarkov, sledenje delcev fizikalnih, HEP fizika energij visokih, stanje razvoja, rešitve problemov, snovanje izvedb, šum ultra mali, predojačenje signala

Izvleček: Polprevodniške detektorje sevanja uporabljamo na mnogih področjih raziskovanja v fiziki, od spektrometrije in slikanja z žarki X in γ do sledenja delcev pri eksperimentih v visokoenergijski fiziki. Čitalna elektronika mora ustrezati zahtevam, ki jih postavljajo različne uporabe detektorjev, kot so nizek šum za dosego visoke pozicijske in energijske ločljivosti, visoka hitrost, odpornost proti sevanju in delovanje pri nizkih temperaturah. Močno segmentirani detektorji so vzpodbudili razvoj monolitnih čitalnih vezij, medtem ko je bilo potrebno razviti prav posebne integracijske tehnologije za dosego optimalnega delovanja. Po predstavitvi osnov načrtovanja čitalne elektronike, v prispevku opisujemo rešitve, ki smo jih uporabili v posebnih primerih, kot so ultra nizkošumno predojačevanje za spektrometrijo z žarki X in γ ter analogno obdelavo signalov iz silicijevih mikropasovnih detektorjev. Vezja, ki jih opisujemo, segajo od nabojno občutljivih predojačevalnikov, izvedenih z JFET monolitnimi tranzistorji, kjer s posebno tehniko povratne vezave brez uporov dosežemo minimalen šum, do večkanalnih CMOS analogno-digitalnih integriranih vezij, ki vsebujejo kompletno čitalno elektroniko za silicijeve detektorje sledi v spektromerih na trkalnikih visokih energij.

1. INTRODUCTION

Semiconductor detectors are widely used to obtain information about various properties (such as energy, momentum, time of occurrence, position) of nuclear particles and radiation, that produce ionisation in the detector material. A measure of the information appears as an electric charge, induced on a set of two electrodes, characterised by their capacitance. The detector is connected to front-end electronic circuits, which include an amplifying device (usually a charge-sensitive preamplifier) and a filter, performing a shaping of the signal in the time domain to optimise the measurement of a desired quantity such as signal amplitude as a measure of the energy loss of the particle. The problem of the measurement of the charge delivered by a capacitive source with the best possible accuracy compatible with noise intrinsically present in the amplifying system has been widely discussed in the literature /1, 2, 3, 4, 5/, also taking into account the constraints (power dissipation, event rate) set by the different applications. The main results will be reviewed here, to derive the basic criteria for the design of low-noise front-end electronics.

Figure 1 shows a schematic model of an analog channel processing the signal from a semiconductor detector. The detector itself is modelled as a current source delivering in a very short time a charge Q across its capacitance C_D. The detector signal is integrated by a charge-sensitive preamplifier (with a feedback capacitance C_F and an input capacitance C_i) and then shaped

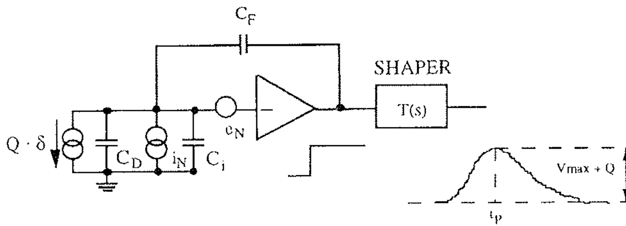


Fig. 1. Analog processing channel for the measurement of the charge Q delivered by a semiconductor detector.

by a filter with transfer function T(s). The filter allows the measurement of a quantity, for example signal peak amplitude, related to the charge released in the detector, minimising the error due to noise and to signal pileup due to a high event rate, which may set constraints on the signal duration and peaking time t_P.

The noise in the amplifier system arises from two uncorrelated sources at the input, a series voltage source e_N and a parallel voltage source i_N, each of which generates a spectral density with a white (independent of frequency f) and a non-white component:

$$\frac{\overline{de_N^2}}{df} = A_W + \frac{A_f}{f} \qquad (1)$$

$$\frac{\overline{di_N^2}}{df} = B_W + B_f \cdot f \qquad (2)$$

The white term in equation (1) is mostly determined by the white noise in the main current of the preamplifier input device, that is drain current for an FET or collector current for a bipolar transistor. g_m is the transconductance, while k is the Boltzmann's constant and T is the absolute temperature. Γ is a coefficient equal to 0.5 in bipolar transistors; it is about 2/3 for JFETs, and may exceed 1 for short-channel MOSFETs.

$$A_W = 4kT\frac{\Gamma}{g_m} \qquad (3)$$

The second term in the series noise is given by the 1/f noise in the drain or collector current. The white term in (2) is determined by the shot noise in the detector leakage current I_{det}, by the shot noise in the input device gate (base) current $I_{G(B)}$ and by the thermal noise in the preamplifier feedback resistor R:

$$B_W = 2qI_{det} + 2qI_{G(B)} + \frac{4kT}{R} \qquad (4)$$

where q is the electronic charge. The second term in (2) arises form dielectric losses in the components connected to the preamplifier input, and mainly depends on the detector - preamplifier assembly. It will be neglected in the following.

2. EFFECT OF NOISE ON CHARGE MEASUREMENTS FROM SEMICONDUCTOR DETECTORS

The effect of noise on the charge measurement is usually characterised by the standard deviation or Equivalent Noise Charge (ENC). This is the charge which injected at the input produces at the output of the linear processor a signal whose amplitude equals the root mean square noise. ENC is given by the quadrature sum of contributions from series and parallel noise terms described in the previous paragraph:

$$ENC = \sqrt{ENC_{A_W}^2 + ENC_{A_{1/f}}^2 + ENC_{B_W}^2} \qquad (5)$$

The contribution to ENC given by white series noise can be expressed in the following way:

$$ENC_{A_W} = \sqrt{\frac{A_1}{\tau}}\sqrt{4kT\frac{\Gamma}{f_T}}\sqrt{C_D}\left(m^{1/2} + m^{-1/2}\right) \qquad (6)$$

Several design criteria for achieving low-noise performances can be extracted from relationship (6). This term is directly proportional to the factor A_1/t, which is determined by the signal-shaping filter. τ is a parameter related to the time scale of the signal, and can be assumed to be the peaking time t_P. A long measurement time has to be used to minimise ENC_{AW}. The preamplifier input device has to feature a high transition frequency f_T, and to be capacitively matched to the detector. Equation (6) has a minimum at m=1, where $m=C_D/C_i$ is the capacitive matching coefficient. A low capacitance detector is also needed if very low noise performances must be achieved. The two latter conditions are also valid for the 1/f series noise contribution to ENC:

$$ENC_{A_{1/f}} = \sqrt{A_2}\sqrt{H_f}\sqrt{C_D}\left(m^{1/2} + m^{-1/2}\right) \qquad (7)$$

where A_2 is a coefficient depending on the filter. No dependence on t_P is present in this term, so its minimisation is essential both at short and long measurement times. The parameter $H_f = A_F C_i$ is a constant for a given technology and device gate length /6/. The need of reducing the effect of 1/f noise may determine the choice of the input device, reminding that typical values are $H_f = 10^{-27}$ J for silicon JFETs, $H_f = 10^{-25}$ J for P-channel MOSFETs and $H_f = 10^{-23}$ J for N-channel MOSFETs.

The parallel noise contribution to ENC is:

$$ENC_{B_W} = \sqrt{A_3\tau}\sqrt{2qI_D + 2qI_{G(B)} + \frac{4kT}{R}} \qquad (8)$$

It is proportional to $\sqrt{A_3\tau}$, which is determined by the filter: therefore it has a larger influence at long peaking times. Its minimisation requires a small detector leakage current I_D, which may limit the maximum active area of the detector, and may also force to operate it at low temperature. As it appears from (8), because of their base current I_B, standard bipolar transistors do not

permit high resolution spectroscopy, instead allowed by FETs with a small gate current I_G, which can also be reduced by cooling. A main source limiting the achievable signal-to-noise ratio is the preamplifier feedback resistor. Several non resistive techniques have been developed to discharge the feedback capacitor, allowing to approach the ultimate resolution limits /7, 8, 9, 10, 11/.

The previous discussion shows that the energy resolution of the detection system is given, as far as electronic noise is concerned, by the detector itself, by the preamplifier input device and by the signal processor setting the values of the coefficients A_1, A_2, A_3 and of the signal peaking time t_P. It was shown that several measures can be taken to minimise the noise. If allowed by the counting rate, operation at the optimum t_P (usually several μs), determined by both series and parallel noise, is mandatory. In high rate applications adequate resolution can be achieved by operating with a low capacitance detector-FET system.

The following section describes a charge-sensitive preamplifier, where technology and design parameters are optimised to the achievement of very low noise in view of applications in high resolution spectroscopy. Section 4 presents a multichannel integrated circuit for the readout of silicon microstrip detectors in an accelerator experiment: here the design choices had to cope with severe constraints set by detector geometry and operating environment.

3. MONOLITHIC JFET PREAMPLIFIER FOR HIGH RESOLUTION SPECTROMETRY

The Junction Field-Effect Transistor (JFET) is considered to be the best choice in X and g-ray spectrometry applications for several reasons /12, 13, 14/. Among the FET devices, it has the smallest amount of low frequency noise and its white noise has a reliable dependence on the transconductance. It has intrinsic properties of radiation hardness, and it can operate at cryogenic temperatures, with a considerable reduction of the leakage current and of the series noise.

It is worth pointing out here that very good results were recently obtained also with CMOS devices, especially in applications requiring relatively short peaking times, such as room temperature operated detectors having non negligible leakage currents or low-capacitance detectors /15, 16, 17, 18/.

The excellent characteristics of the JFET suggested the development of the monolithic buried layer process, where N-channel JFETs of outstanding noise performances are integrated on the same substrate. This process provided the basis for the realisation of several preamplifiers /19, 20, 21, 22/. One of them (IPA4) /23/ was conceived for γ-ray spectrometry in association with large germanium detectors. For this purposes the front-end device was designed with W = 1820 μm and L = 5 μm, yielding an input capacitance of about 10 pF.

This circuit achieves the best noise performances /24/ when operated with a non resistive, continuous-type charge reset based on the forward-biased JFET principle /7/, as shown by the schematic in figure 2.

The preamplifier consists of an input cascode (J_1, J_2), a bootstrapped active load (J_3, J_4, J_7) and a source follower output stage (J_8), with an integrating feedback capacitance C_F. The detector leakage current and the signal charge from the feedback capacitor are fed to the gate of the input transistor. These currents add to the reverse current of the gate-to-drain junction and force the gate-to-channel junction to be forward-biased. A low frequency feedback loop is employed to stabilise the operating point of the preamplifier in presence of the forward-biased gate-to-source junction. It goes from the central point of the R_1, R_2 divider to the gate of J_2. The current needed to operate the input JFET with a forward-biased gate is provided by the resistor R_{BL}.

The benefit brought about by the non-resistive charge reset becomes apparent from the comparison of curves a) and b) in fig. 3, both obtained with the preamplifier

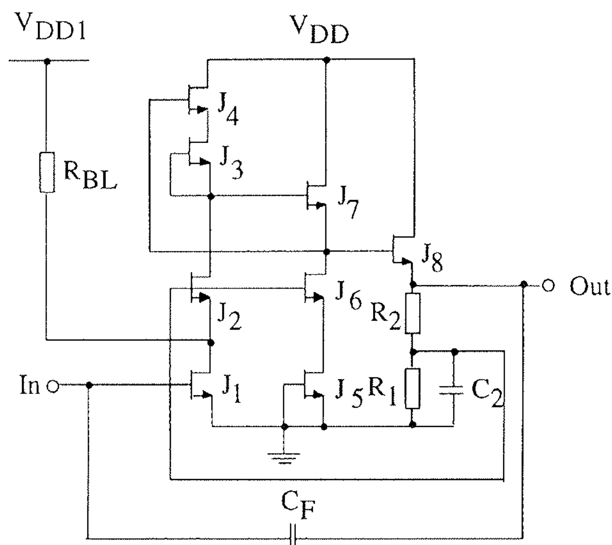


Fig. 2. IPA4 preamplifier with forward biased gate-to-source junction in the front-end device.

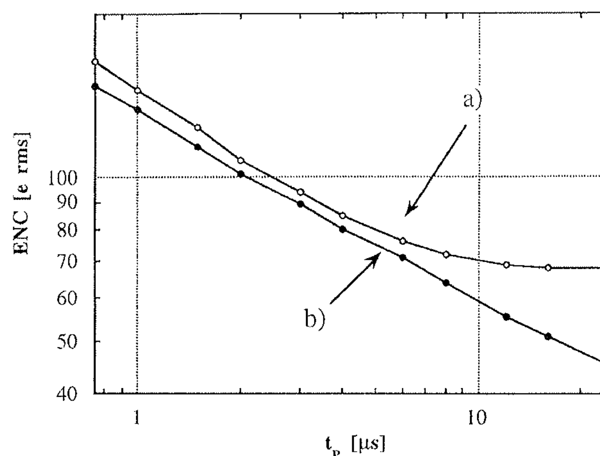


Fig. 3. Equivalent noise charge as a function of the peaking time tp, at zero detector capacitance, for the buried layer IPA4 charge-sensitive preamplifier. (a) Preamplifier with resistive feedback. (b) Preamplifier with non-resistive charge reset.

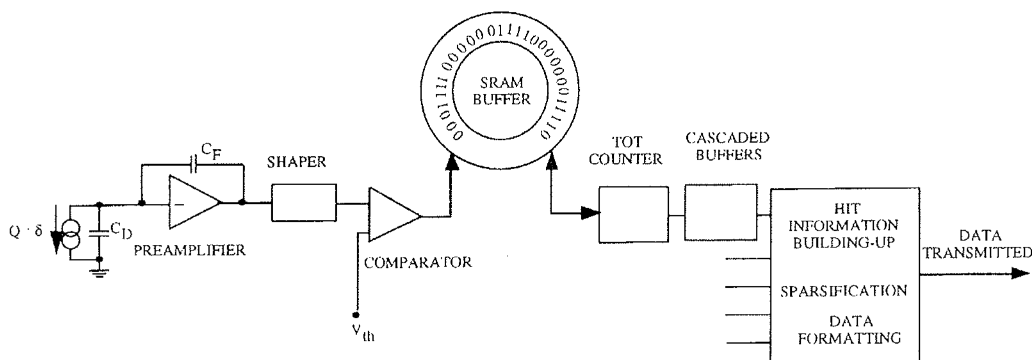


Fig. 4. Block diagram of the front-end chip intended for signal processing in BaBar vertex detector.

followed by a unipolar semigaussian shaper. In order to enhance the relative importance of the ENC contribution coming from parallel sources, among them dielectric noise, from that due to series sources, the measurements were done with no external detector simulating capacitance. Curve a) in fig. 3, relevant to the preamplifier with resistive feedback, shows that ENC tends to level off to about 70 e rms at peaking times t_P beyond 10 μs and even shows a gentle rising trend at 24 μs. The ENC behaviour at long peaking times results from the combined effects of dielectric and thermal noise associated with the feedback resistor. In the case of the preamplifier with non-resistive feedback, where these effects are eliminated, ENC keeps decreasing as t_P is increased and reaches 45 e rms at the longest explored peaking time. This value is certainly very good for a preamplifier which employs at the input a device with a 10 pF input capacitance. These considerations bring favour to the buried-layer process as a very suitable basis for the realisation of monolithic preamplifiers with noise characteristics adequate to high resolution spectrometry.

4. A CMOS MULTICHANNEL READOUT INTEGRATED CIRCUIT FOR A SILICON VERTEX TRACKER

Very high granularity semiconductor position-sensitive detectors such as silicon microstrip or pixel detectors are used in applications ranging from tracking in elementary particle physics experiments to medical imaging. The readout of these detectors has to be carried out by high density multichannel mixed-signal ASICs, combining analog processing functions and high speed digital circuits. Low-power design techniques are used, and the choice of the technology is restricted to CMOS or BiCMOS processes. The latter are usually preferred in very high rate applications, where signal shaping times are of the order of a few tens of ns, because of the high values of the parameters g_m/I_C, g_m/C_i featured by bipolar transistors used as input devices /25, 26, 27, 28, 29/. In lowerrate applications ($t_p \geq 100$ ns) and with low capacitance detectors ($C_D \leq 1$ pF) purely CMOS Ics are commonly used /examples are given in references 30, 31, 32, 33/. In many applications radiation hardness is also a very important issue, especially in experiments at high luminosity colliders, where the front-end electronics has to stand high doses of ionising radiation and neutron fluences without performance degradation.

One of the readout ICs most recently developed is a low-noise, mixed-signal CMOS chip containing the complete readout electronics for the Silicon Vertex Tracker based on double-sided microstrip detectors in the BaBar experiment at SLAC. The chip has 128 channels that process in parallel the signals coming from an equal number of strips. The strip signals are amplified, shaped and then digitised using a range compression method, based on the Time-over-Threshold technique /34/. To do this, the signal at the shaper output is presented to a comparator with a preset threshold. The duration of the signal at the comparator output is the Time-over-Threshold (ToT), that is the time during which the shaper output signal exceeds the threshold.

The block diagram of the BaBar SVT front-end chip is shown in figure 4. The charge information carried by the ToT value is stored into trigger latency buffers, one for each channel, to compensate for delay and jitter in the time of arrival of the first-level trigger. Upon receipt of a trigger, the data are retrieved from the latency buffers, and after passing through two cascaded derandomizing buffers they end up in a sparsifying unit, where the final hit information is built up, providing, for each channel which has recorded a signal, the channel number, the hit time stamp and the value of the charge. This information is transmitted by the chip in serial format upon receipt of a readout command. The previous functional description gives an oversimplified view of the actual readout chip, named AToM (A Time-over-threshold Machine). Many more functions are implemented as described in a detailed way in references /35, 36, 37/. Among them, the possibility of selecting the value of the charge sensitivity of the analog channel (LOW = 150 mV/fC, HIGH = 250 mV/fC) and of the signal peaking time t_P (from 100 ns to 400 ns), and of operating on both detector signal polarities (n-side and p-side).

During the operational lifetime of the detector, the chip will be exposed to considerable levels of ionising radiation. A worst-case estimate of the ionising dose in the inner layers of the detector is 2 Mrad (Si). To achieve

the required degree of radiation tolerance, the chip was fabricated in a rad-hard technology (Honeywell RICMOS IV bulk CMOS, 0.8 μm minimum gate length).

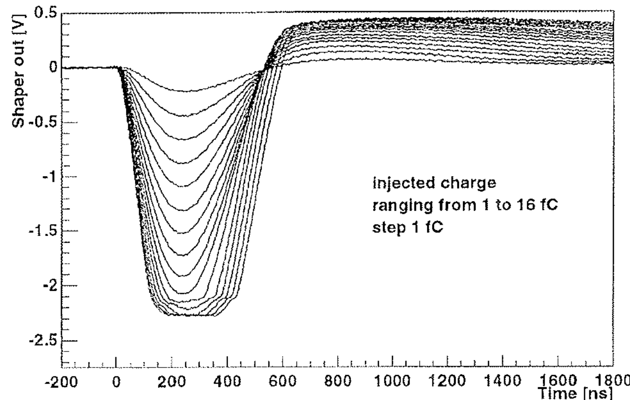


Fig. 5. Waveforms at the shaper output at 200 ns peaking time for the AToM chip.

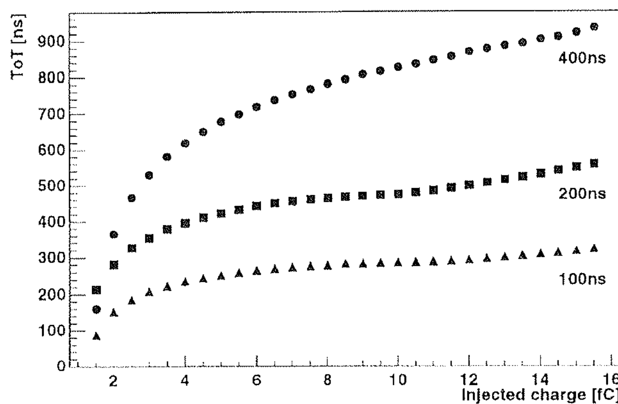


Fig. 6. ToT at the comparator output at three different peaking settings for the AToM chip.

Figure 5 shows the signals at the shaper output at the 200 ns peaking time setting with the input charge as a parameter. Three ToT curves at three different peaking times are shown in figure 6. The range-compression features obtained with the ToT technique are evident. Noise measurements at 200 ns peaking time and 3.5 mW total power dissipation per channel yield an ENC of 700 electrons rms at 12 pF detector capacitance.

5. CONCLUSIONS

This paper presented a review of the design criteria of front-end electronics for semiconductor radiation detectors, especially targeting low-noise specifications. As an example of available front-end circuits, two designs for very different applications were described. As a conclusion, it is worth pointing out that research in this field is stimulated by the severe requirements of future physics experiments and extending medical and industrial applications of semiconductor detectors. To this purpose, attention is focused on the technological developments in the fields of III-V devices, such as MESFETs or HEMTs /38/, of short-channel ("deep submicron") MOSFETs /39/ and of electronics for cryogenic temperature operation /40/.

6. ACKNOWLEDGEMENTS

The front-end circuits presented in this paper were designed and characterised by the Electronic Instrumentation group at the Department of Electronics of the University of Pavia, under the supervision of Pier Francesco Manfredi and Valeria Speziali.

7. REFERENCES

/1/ E. Gatti, P.F. Manfredi, "Processing the signals from solid-state detectors in elementary particle physics", La Rivista del Nuovo Cimento, Vol. 9, 3 (1986), p. 140.

/2/ V. Radeka, "Low-noise techniques in detectors", Ann. Rev. Nucl. Part. Sci. 1988. 38: 217-77.

/3/ P.F. Manfredi, V. Speziali, "Noise limits in detector charge measurements", Techniques and Concepts of High Energy Physics VI. Plenum Press, New York (1991), 381.

/4/ A. Pullia, G. Bertuccio: "Resolution limits of silicon detectors and electronics for soft X-ray spectroscopy at non cryogenic temperatures", Nucl. Instr. and Meth. in Phys. Res. A380 (1996), 1.

/5/ G. Bertuccio, A. Pullia, G. De Geronimo: "Criteria of choice of the front-end transistor for low-noise preamplification of detector signals at sub-microsecond shaping times for X- and γ-ray spectroscopy", Nucl. Instr. and Meth. in Phys. Res. A380 (1996), 301.

/6/ G. Lutz, P.F. Manfredi, V. Re, V. Speziali: "Limitations in the Accuracy of Detector Charge Measurements set by the 1/f Noise in the Front-end Amplifiers". Nucl. Instr. and Meth. in Phys. Res., A277 (1989), 194.

/7/ G. Bertuccio, P. Rehak, D. Xi, "A novel charge sensitive preamplifier without feedback resistor". Nucl. Instrum. and Meth. in Phys. Res. A 326 (1993), 71.

/8/ G. Bertuccio et al.: "Silicon drift detector integrated P-JFET for continuous discharge of collected electrons through the gate junction". Nucl. Instrum. and Meth. in Phys. Res. A377 (1996), 352.

/9/ F.S. Goulding, J. Walton, D.F. Malone, "An opto-electronic feedback preamplifier for high-resolution nuclear spectroscopy", Nucl. Instr. and Meth. in Phys. Res., 71 (1969), 273.

/10/ T. Nashashibi, G. White, "A low-noise FET with integrated charge restoration for radiation detectors", IEEE Trans. Nucl. Sci., Vol. 37, No. 2 (1990), 452.

/11/ D.A. Landis, F.S. Goulding, R.H. Pehl, J.T. Walton, "A low-noise FET with integrated charge restoration for radiation detectors", IEEE Trans. Nucl. Sci., Vol. 18, No. 1 (1971), 115.

/12/ P.F. Manfredi, V. Speziali, "Silicon junction field-effect transistors in low noise circuits: research in progress and perspectives", Techniques and Concepts of High Energy Physics VI. Plenum Press, New York, (1991), 423.

/13/ G. Cesura, V. Re, A. Tomasini: "Radiation Sensitivity of Noise in Monolithic JFET circuits exposed to 60Co γ-rays", Nucl. Phys. B (Proc. Suppl.), 32, 546 (1993).

/14/ G. Cesura, V. Re, "Effects of γ-rays and Neutrons on the Noise Behaviour of Monolithic JFET Circuits", IEEE Trans. Nucl. Sci., Vol. 41, No. 3 (1994), p. 577.

/15/ P. O'Connor, G. Gramegna, P. Rehak, F. Corsi, C. Marzocca, "Ultra low noise CMOS preamplifier-shaper for X-ray spectroscopy", Nucl. Instr. and Meth. in Phys. Res., A409 (1998), 315.

/16/ B. Ludewigt, J. Jaklevic, I. Kipnis, C. Rossington, H. Spieler, "A high rate, low noise, X-ray silicon strip detector system", IEEE Trans. Nucl. Sci., Vol. 41, No. 4 (1994), 1037.

/17/ R. Turchetta et al, "High spatial resolution silicon read-out system for single photon X-ray detection", IEEE Trans. Nucl. Sci., Vol. 41, No. 4 (1994), 1063.

/18/ M.L. Prydderich, P. Seller, "A 16 channel analogue sparse readout I.C. for INTEGRAL (International Gamma-Ray Astrophysics Laboratory)", IEEE Trans. Nucl. Sci., Vol. 42, No. 4 (1994), 776.

/19/ M. Demicheli, P.F. Manfredi, S. Rescia, V. Radeka, V. Speziali, "Design of monolithic preamplifiers employing diffused N-JFETs for ionization chamber Calorimeters", Nucl. Instrum. and Meth. in Phys. Res. A289 (1990), 418.

/20/ V. Radeka, S. Rescia, L.A. Rehn, P.F. Manfredi, V. Speziali, "Monolithic Junction Field-Effect Transistor Charge Preamplifier for Calorimetry at High Luminosity Hadron Colliders", IEEE Trans. Nucl. Sci., NS-40 (1993), 1321.

/21/ V. Radeka, S. Rescia, P.F. Manfredi, V. Speziali, F. Svelto, "JFET Monolithic Preamplifier with Outstanding Noise Behaviour and Radiation Hardness Characteristics", IEEE Trans. Nucl. Sci. NS-40 (1993), 744.

/22/ F. Lanni, P.F. Manfredi, V. Radeka, S. Rescia,V. Re, V. Speziali, "Monolithic silicon JFET front-end for calorimetry". Nucl. Instrum. and Meth. A 360 (1995), 158.

/23/ P.F. Manfredi, V. Re, V. Speziali, "JFET-based monolithic preamplifiers for spectrometry applications", Nucl. Instrum. and Meth. A 380 (1996), 308.

/24/ P.F. Manfredi, V. Re, V. Speziali: "Monolithic JFET preamplifier with non-resistive charge reset", IEEE Trans. Nucl. Sci. Vol. 45, No. 4 (1998), p. 2257-2260.

/25/ I. Kipnis, H. Spieler, T. Collins, "A bipolar analog front-end integrated circuit for the SDC silicon tracker", IEEE Trans. Nucl. Sci., Vol. 41, No. 4 (1994), p. 1095.

/26/ E. Spencer et al, "A fast shaping low power amplifier - comparator integrated circuit for silicon strip detectors", IEEE Trans. Nucl. Sci., Vol. 42, No. 4 (1995), p. 796.

/27/ W. Dabrowski et al: "Low-noise monolithic bipolar front-end for silicon drift detectors", Nucl. Instr. and Meth. A 420 1-2 (1999), 270.

/28/ F. Anghinolfi et al, "SCTA - A rad-hard BiCMOS analogue readout ASIC for the ATLAS semiconductor tracker", IEEE Trans. Nucl. Sci., Vol. 44, No. 3 (1997), 298.

/29/ W. Dabrowski, J. Kaplon, R. Szczygiel, "SCT128B - A prototype chip for binary readout of silicon strip detectors", Nucl. Instrum. and Meth. A 421 1-2 (1999), 303.

/30/ T. Zimmermann et al, "SVX3: a deadtimeless readout chip for silicon strip detectors", ", Nucl. Instrum. and Meth. A 409 (1998), 369.

/31/ F. Anstotz at al, "Performance of a CMOS mixed analogue-digital circuit (APVD) for the silicon tracker of CMS", Proceedings 4th Workshop on Electronics for LHC experiments, Rome, September 21 - 25, 1998. CERN/LHCC/98-36.

/32/ L. Blanquart et al, "Pixel analog cell prototypes for ATLAS in DMILL technology", Nucl. Instrum. and Meth. A 395 (3) (1997), 313.

/33/ M. Campbell et al, "Development of a pixel readout chip compatible with large area coverage", Nucl. Instrum. and Meth. A 342 (1994), 52.

/34/ R. Becker et al, "Signal processing in the front-end electronics of BaBar vertex detector", Nucl. Instr. and Meth. in Phys. Res., A 377 (1996), p. 459-464.

/35/ I. Kipnis et al, "A Time-over-Threshold Machine: the Readout Integrated Circuit for the BaBar Silicon Vertex Tracker", IEEE Trans. Nucl. Sci., Vol. 44, No. 3 (1997), p. 289-297.

/36/ V. Re et al: "The rad-hard readout system for the BaBar silicon vertex tracker", Nucl. Instr. and Meth. in Phys. Res., A 409 (1998), p. 354-359.

/37/ P. F. Manfredi et al: "Functional characteristics and radiation tolerance of AToM, the front-end chip of BaBar Silicon Vertex Tracker", presented at 1998 IEEE Nuclear Science Symposium, Toronto, November 10-12, 1998, to be published on IEEE Trans. Nucl. Sci.

/38/ G. Bertuccio, G. De Geronimo, E. Gatti, A. Longoni, J. Ludwig, K. Runge, W. Webel, S. Lauxtermann, "About the use of HEMT in front-end electronics for radiation detection", Proc. 20th Internat. Symp. GaAs Related Compounds, Freiburg, Germany: IOP Publishing, Sept. 1993, p. 111.

/39/ A. Marchioro, "Deep submicron technologies for HEP", Proceedings 4th Workshop on Electronics for LHC experiments, Rome, September 21 - 25, 1998. CERN/LHCC/98-36.

/40/ Proceedings 3rd European Workshop On Low-Temperature Electronics 3, San Miniato, Tuscany, Italy, June 24-26, 1998. Journal de Physique IV, Vol. 8, Pr 3, June 1998.

Dr. Valerio Re
Dipartimento di Ingegneria, Università di Bergamo
Via Marconi, 5, 24044 Dalmine, Italy

Dr. Lodovico Ratti
Dipartimento di Elettronica, Università di Pavia
Via Ferrata, 1, 27100 Pavia, Italy

Prispelo (Arrived): 18.01.1998 Sprejeto (Accepted): 03.03.1999

A MULTI-LAYER SILICON MICROSTRIP DETECTOR FOR SINGLE PHOTON COUNTING DIGITAL MAMMOGRAPHY

F. Arfelli[1], V. Bonvicini[1], A. Bravin[1], G. Cantatore[1], E. Castelli[1], L. Dalla Palma[2], M. Fabrizioli[3], R. Longo[1], A. Olivo[1]*, S. Pani[1], D. Pontoni[3], P. Poropat[1], M. Prest[1], A. Rashevsky[1], L. Rigon[3], G. Tromba[3], A.Vacchi[1] and E. Vallazza[1].
[1] Dipartimento di Fisica - Università di Trieste and INFN - Sezione di Trieste
[2] Istituto di Radiologia - Università di Trieste
[3] Sincrotrone Trieste SCpA
* Corresponding Author (olivo@trieste.infn.it)

PAPER PRESENTED AT
MIDEM´98 CONFERENCE – Minisymposium on Semiconductor Radiation Detectors
23.09.98 – 25.09.98, Rogaška Slatina, Slovenia

Keywords: Si silicon microstrip detectors, single photon counting, synchrotron radiation, digital mammography, contrast resolution, spatial resolution, detection efficiency, counting rate, Si silicon microstrip detectors, FOXFET, Field OXide Field Effect Transistors, two-dimensional images, synchrotron radiation, imaging devices, digital imaging devices, CT, computer tomography, MTF, Modulation Transfer Functions

Abstract: The SYRMEP / FRONTRAD (SYnchrotron Radiation for MEdical Physics / FRONTier RADiology) collaboration has developed a digital X-Ray imager for the mammography beamline at ELETTRA, the synchrotron radiation facility in operation in Trieste, Italy. This imaging device is composed of three stacked layers of FOXFET-biased silicon microstrip detectors, positioned with the strips along the beam direction. In this way a very high absorption efficiency is guaranteed, since the strip length (1 cm) absorbs nearly all the incoming photons in the energy range of interest (15 - 30 keV). Furthermore, the active surface is by construction subdivided into pixels, the dimensions of which are determined by the strip pitch (200 μm) in one direction and by the thickness of the single layer (300 μm) in the other. Each layer has 256 implanted strips, and therefore the whole device has an active surface of ~50x1 mm^2 subdivided into 764 pixels (the inter-layer distance is nearly equal to 100 μm).
The electronic chain reading out the detector signal operates in "single photon counting" mode: this gives the possibility of extracting the maximum information from the radiation beam, since the only limitation to the signal-to-noise ratio in the images is the quantum noise.
Two-dimensional images are obtained by scanning the samples through the synchrotron laminar beam, while the detector is kept stationary with respect to the beam itself. The desired statistics is obtained by combining the information from the three layers, thus reducing the overall acquisition time by a factor of three.
Results from extensive tests carried out on this imaging device by means of a synchrotron radiation beam are reported on this paper.

Večplastni silicijev mikropasovni detektor za digitalno mamografijo s štetjem posameznih fotonov

Ključne besede: Si detektorji silicijevi mikrotrakasti, štetje fotonov posameznih, sevanje sinhrotronsko, mamografija digitalna, ločljivost kontrastna, ločljivost prostorska, učinkovitost detekcije, hitrost štetja, Si detektorji silicijevi mikrotrakasti, FOXFET transistorji z učinkom polja, poljsko-oksidni, slike dvodimenzionalne, sevanje sinhrotronsko, naprave upodabljalne, naprave upodabljalne digitalne, CT tomografija računalniška, MTF funkcije prenosne modulacijske

Izvleček: V okviru projekta SYRMEP/FRONTRAD je bila razvit sistem za digitalno slikanje z rentgenskimi žarki za mamografsko žarkovno linijo ELETTRA, sinhrotronskem izvoru pri Trstu v Italiji. Sistem sestavljajo tri plasti mikropasovnih detektorjev, napajanih preko FOXFET struktur, postavljenih s pasovi v smeri žarka. Na ta način zagotovimo visoko stopnjo absorpcije, saj dolžina pasu (1 cm) zagotavlja absorpcijo skoraj vseh vpadnih fotonov v energijskem območju, ki nas zanima (15 – 30 keV). Nadalje, aktivna površina je razdeljena na slikovne elemente, katerih dimenzija je določena s širino in razdaljo med pasovi (200 μm) v eni smeri in z debelino ene plasti (300 μm) v drugi smeri. Vsaka plast vsebuje 256 implantiranih pasov tako, da ima celoten element aktivno površino okoli 50x1 mm^2 razdeljeno na 764 slikovnih elementov (razdalja med notranjimi plastmi je okoli 100 μm).
Elektronika, ki odčitava signale iz detektorja, šteje posamezne fotone, kar predstavlja maksimalno informacijo o prepuščenih žarkih, saj omejujejo signal šum na sliki le statistične fluktuacije.
Dvodimenzijske slike dobimo s premikanjem vzorca znotraj laminarnega sinhrotronskega žarka, med tem ko detektor miruje glede na curek. Željeno statistiko dobimo z upoštevanjem informacije iz treh plasti, s čimer skrajšamo čas meritve za trikrat.V pričujočem prispevku podajamo rezultate testov, ki smo jih opravili z opisanim sistemom v sinhrotronski žarkovni liniji.

INTRODUCTION

Since the introduction of computed tomography by Housenfield (1973), digital radiology has been acquiring more and more relevance /1/. The wide dynamic range of digital imaging devices brings great advantages with respect to the low dynamic range of conventional film-screen systems: it allows one to eliminate exposure constraints and to amplify the contrast of all the regions of interest in the image by means of computer processing. Furthermore, all storage and archival procedures of radiological images would be dramatically simplified if digital data (instead of analogical films) were handled.

Recently, research has also been carried out on the "source side", demonstrating that a laminar monochromatic synchrotron radiation beam allows great improvements in image quality, together with a reduction in the dose delivered to the sample (see for example /2/). The SYRMEP/FRONTRAD collaboration is carrying out a project that aims at improving the quality of mammographic examinations by operating both on the source and on the detector side. A synchrotron radiation monochromatic X-ray beam is used as the illuminating source, and a silicon pixel detector is utilized to collect the photons transmitted through the sample.

The monochromaticity of the radiation beam gives us the possibility of selecting the appropriate energy for each imaging requirement, thus maximizing the image contrast while minimizing the dose delivered to the sample. The intrinsic high collimation of synchrotron laminar beams highly suppresses the defocusing effect that occurs when the source size is large, as in conventional radiology where X-ray tubes are used. Finally, since the laminar beam cross section can be matched (by means of a slit system) with the detector active surface, the detection of scattered radiation is highly reduced.

Silicon microstrip detectors used in a "edge-on" geometrical configuration, i.e. with radiation impinging on the side rather than on the surface of the chip, allow a very high absorption efficiency (~80% @ 20 keV): since the delivered dose is inversely proportional to the detection efficiency, this last parameter is of primary importance for dose minimization purposes. Furthermore, the single photon counting capability of the readout electronics maximizes the device contrast resolution, the only limitation being the quantum noise.

Several detector prototypes have been tested and utilized to produce digital images of mammographic phantoms and of *in vitro* breast tissue specimens /3-6/. The present prototype has been obtained by stacking three silicon layers one upon the other, in order to form a wider sensitive area covering a large part of the beam cross-section and, above all, in order to reduce by a factor of three the overall duration of the examination. The results of the tests carried out on this prototype are discussed in the present article.

MATERIALS AND METHODS

The tests described in this paper have been carried out at the SYRMEP beamline /7/ at the ELETTRA storage ring in Trieste, Italy. The source is one of the 24 bending magnets of the ring. The white beam, with a spectrum ranging from 0 to ~35 keV, is first filtered by a water cooled beryllium window, which takes away the low energy components. Then a channel-cut, Si(1,1,1) crystal is used to filter the spectrum by means of Bragg reflection. This monochromator device provides a monochromatic, tuneable energy beam in the energy range 8-35 keV with an energy resolution of about 0.2%. A tungsten slit system is placed in the vacuum tube immediately before the monochromator, in order to reduce the cross section of the beam impinging on the crystal. At the entrance of the experimental hutch a second tungsten slit system, moved by 1 μm resolution stepping motors, determines the cross section of the beam reaching the detector active surface, which is kept stationary with respect to the beam itself. An ionization chamber, read out by a Keithley amperometer, is placed immediately after the slit system to monitor the photon flux in order to evaluate the dose delivered to the samples. In order to obtain the twodimensional images a micropositioning stage (1 μm resolution), placed between ionization chamber and detector, scans the samples through the beam. A dedicated C/C++ software developed on a LINUX operating system running on a Pentium PC controls both the sample movement and the readout system. The core of the front-end electronics consists in a series of 32-channel mixed analog-digital VLSI chips (CASTOR /8/) housed on 7-layer ceramic hybrid circuits. Each VLSI channel features a charge sensitive preamplifier, a CRRC shaper, a high-pass filter, a threshold discriminator and a 16 bit counter which counts the signals from single photons with a rate of ~10^4 counts/s. A modular set of PCB cards allows the prompt expansion of the front-end electronics in order to run imager versions with an increasing number of channels. The same choice has been made for the readout electronics, which is based on a CAMAC board.

The detector prototype discussed in this paper has been obtained by stacking three single microstrip detectors one upon the other. The peculiar trapezoidal shape of these silicon chips allows the connection of each strip to the front-end electronics by means of flexible upilex fan-outs. Two full trapezoidal structures (each one featuring 256 200 μm channels) and two half structures (featuring 128 200 μm channels) have been assembled (see Fig. 1), in order to leave enough space for wire bonding behind the assembled prototype. This device has been used to produce digital images of several test objects, in order to determine its perform-

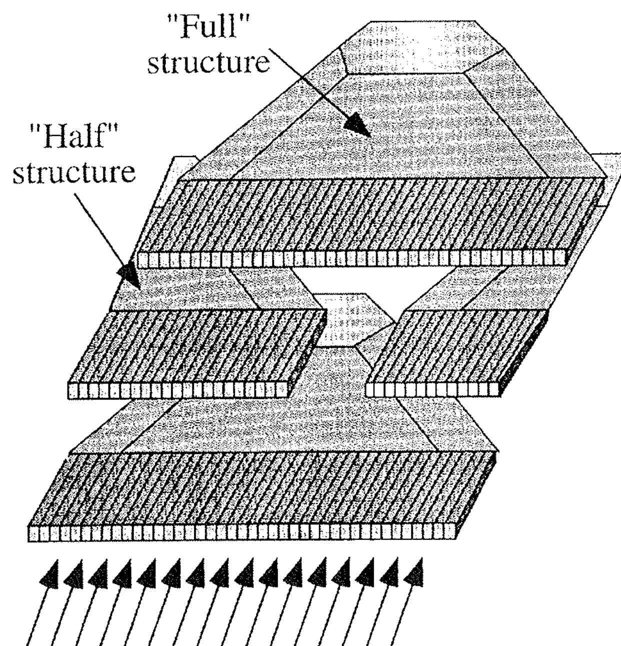


Fig. 1. Schematic layout of the three-layer detector assembly. Two "full" and two "half" trapezoidal structures are used, in order to leave enough space for the wire bonding behind the assembled structure.

ances in terms of contrast and spatial resolution. In particular a "Contrast-Detail Phantom", consisting in a plexiglass slab containing several air disks of different thicknesses and diameters, has been used to measure the contrast resolution, and a bar pattern test object, i.e. a lead mask in which several line patterns of different size and spacing are carved, has been imaged in order to test the spatial resolution.

RESULTS AND DISCUSSION

The detector prototype, aligned with the incoming synchrotron beam, has been tested at the SYRMEP beamline. All the results described below have been obtained with a beam energy equal to 20 keV, and with the slit system set to obtain a beam cross-section equal to 50x1.1 mm^2, matching the detector active surface.

First of all, the detector has been illuminated with different values of the incoming flux, obtained by placing several aluminum filters of different calibrated thicknesses in front of the ionization chamber and of the detector system. The detected rate (counts/pixel/s) has been plotted against the incoming rate, measured using the previously calibrated ionization chamber (a cross-check on these values has been done by taking into account the aluminum absorption coefficient and the thickness of the filters). The result of this preliminary measurement is shown in Fig. 2. The experimental points have been fitted assuming a non paralyzable model for the detector behavior /9/:

$$M = \frac{\varepsilon \cdot R}{1 + \varepsilon \cdot R \cdot \tau} \quad (1)$$

where M is the detected rate per pixel (counts/pixel/s), R the incident rate per pixel (counts/pixel/s), ε the detection efficiency @20 keV (assuming a very low rate: it is practically the slope of the curve at the origin) and τ the dead time of the prototype. As can be seen from Fig.2, the assumed model fits very well the experimental data (the reduced χ^2 is equal to 0.78). The estimates for dead time and efficiency obtained from the fit are τ=16.7±0.3 μsec, ε=80±2%, respectively. The limitation in the detection efficiency stems from the presence of a dead zone in the active volume of the detector:

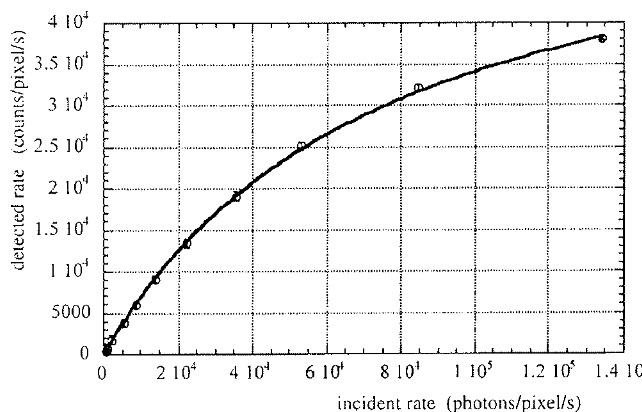


Fig. 2. Detected rate VS. incident rate. The experimental points (dots) have been fitted by means of a non-paralyzable model (solid line, see text for description).

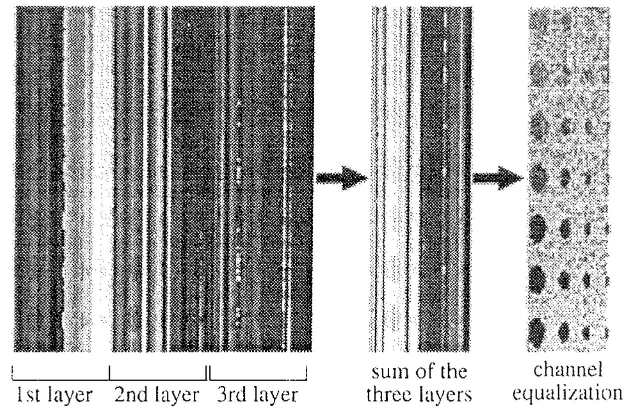


Fig. 3. Image reconstruction procedure. The processed image is obtained by summing the images acquired by each one of the three layers and by equalizing the different gains of each channel (see text).

photons absorbed in the first slice of the detector, where the electric field is veiy low, are not detected. This is due to the necessity of preserving a certain distance between the implanted strips and the physical edge of the chip, in order to avoid a dramatic increase of the reverse dark current. Several tests have been carried out to find the "cut" distance that maximizes the detection efficiency while minimizing the reverse dark current /10/, resulting in a "cut" distance of the present prototype equal to 250 μm, which is fully compatible with an efficiency of 80% at 20 keV. As it can be seen in Fig. 2, the first counting losses occur already at about 10^4 counts/pixel/s: as discussed below, this has a non negligible influence on imaging results.

The image reconstruction process is illustrated in Fig. 3, where three different stages of the procedure are shown for an image of the "Contrast-Detail" phantom. Fig. 3a shows the raw data: the three different images of the phantom, each one acquired by a different layer of the detector, are shown. Fig. 3b shows the sum of these three images: the number of counts per image pixel is increased by a factor of three, reaching the desired statistics of 10^4 photons per pixel. Obviously, in order to obtain the same statistics with a single layer detector, an exposure time increased by a factor three would be necessary. The image still presents some artifacts - due to the gain differences between different channels obscuring the details: in order to correctly visualize the imaging result a channel equalization is necessary. Fig. 3c shows the result of this equalization procedure: the artifacts are eliminated and the details are clearly visible.

As discussed above, images of a Contrast-Detail phantom are used to estimate the contrast resolution of the imaging device. Due to the saturation effect shown in Fig. 2, the incident rate will have a strong influence on the detected contrast. Fig. 4 demonstrates this effect: images of the Contrast-Detail phantom have been acquired at three different values of the incident rate: 5, 16 and 65 kHz, and the corresponding values of the contrast of each disk have been measured for a set of disks

of increasing thicknesses. The contrast is estimated by applying the following definition /11/:

$$\frac{N_1 - N_2}{(N_1 + N_2)/2} \cong \frac{N_1 - N_2}{N_1} \qquad (2)$$

where N_2 are the counts per unit surface occurring in the image in correspondence of the detail and N_1 the counts per unit surface immediately outside it. The introduced approximation works well when low contrasts are examined.

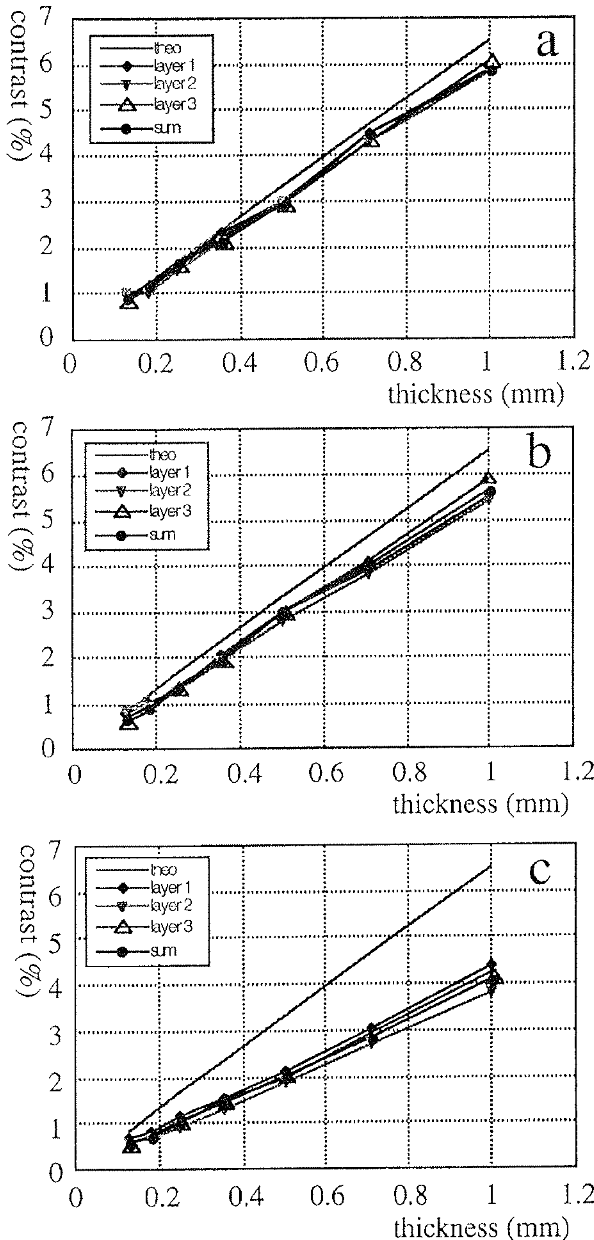


Fig. 4. Detected VS. theoretical contrast as a function of the disk thickness, extracted from the processed image visible in Fig. 3. The same procedure has been applied for three data sets acquired at three different counting rates: 5, 16 and 65 kHz. The loss in the detected contrast grows as the rate is increased (see text).

In Fig. 4a (5 kHz), 4b (16 kHz) and 4c (65 kHz) five point series are represented: the theoretical contrast of the disks, the contrast measured by means of each single detector layer and the contrast estimated from the image obtained by summing the three layers. First of all, one notices that the contrast obtained from the sum of the three layers always lays in the middle of the values obtained from each single layer, meaning that no contrast resolution is lost when the image reconstruction procedure is applied. On the other hand, the contrast resolution losses that occur as the rate is increased are apparent. At present, the maximum counting rate that can be accepted in order to avoid relevant contrast resolution losses is of the order of 10 kHz. It is however important to notice that in all cases contrast values of the order of 1 % are detected, while with conventional screen-film systems contrast values lower than 2-3% are undetectable.

The last part of this discussion deals with spatial resolution measurements. It is important to notice that - even if the pixel size is equal to 200x300 μm^2 - it is possible to obtain images with improved spatial resolution, at least in the direction in which the samples are scanned through the beam. In fact, if a scanning step smaller than the pixel size is chosen, the acquired "raw" image will consist of the convolution between the "real" image and the Point Spread Function of the detector /12/. By applying then simple algorithms performing deconvolution and filtration, it is possible to obtain an image with a spatial resolution determined by the scanning step rather than by the pixel size. Fig. 5 shows an example of this procedure: the same portion of the bar pattern test object discussed above has been imaged both with a sampling step equal to the pixel size (300 μm, Fig. 5a), and with a sampling step much smaller than the pixel size (20 μm, Fig. 5b: the presented image has already been deconvoluted and filtered). All the bar patterns are indicated by their spatial frequency expressed in line pairs per mm: 3 lp/mm indicates for instance lead bars having dimensions equal to ~167 μm. According to the Nyquist theorem /13/, all these details are invisible if the spatial sampling is equal to 300 μm, as demonstrated by Fig. 5a; while with a sampling step equal to 20 μm all the details must be detected, as shown in Fig. 5b.

The bar pattern test object inputs a fixed spatial frequency to the imaging device, allowing an estimate of the Modulation Transfer Function (MTF, /12/) of the device itself. Fig. 6 shows the comparison between the theoretical MTF of a 300 μm pixel (dashed line) and the theoretical MTF of a 20 μm pixel (solid line). The dots represent the experimental points extracted from the measurement made with a sampling step equal to 20 μm, and demonstrate that our procedure approximates very well the spatial resolution that would be provided by a pixel having dimensions equal to the selected sampling step. Values extracted from measurements obtained by each detector layer are presented for each spatial frequency, and they are compared to the values extracted from the sum of the images acquired by each layer. As in the case of the contrast resolution, the fact that values coming from the reconstructed image lay always within values coming from each layer demonstrates that no spatial resolution is lost when the image reconstruction procedure is applied.

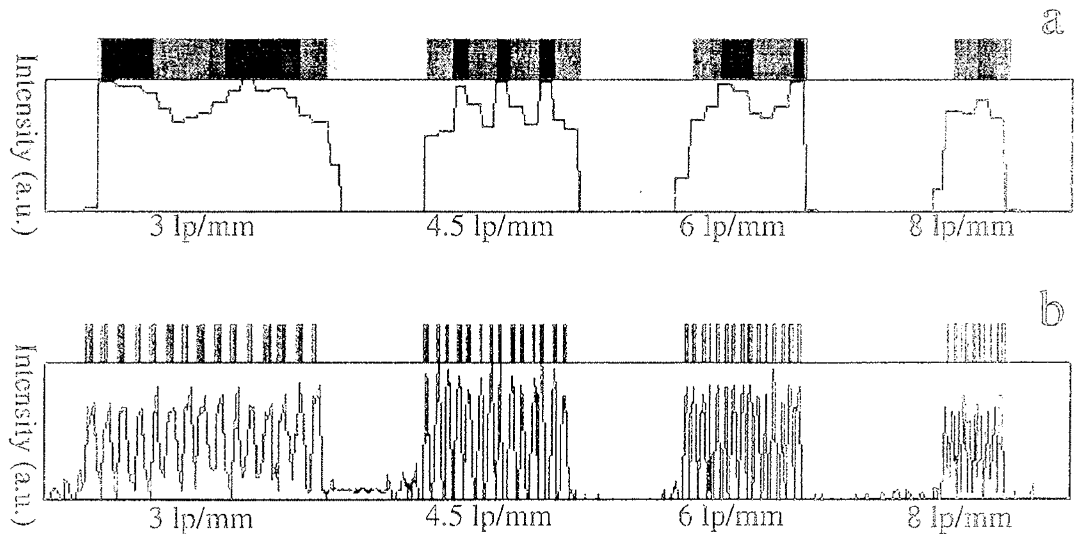


Fig. 5. Images of a bar pattern test object. The first one (a) has been acquired with a sampling step equal to the pixel size (300 μm), while the second one (b) has been acquired with a sampling step much smaller than the pixel size (20 μm), and then deconvoluted and filtered.

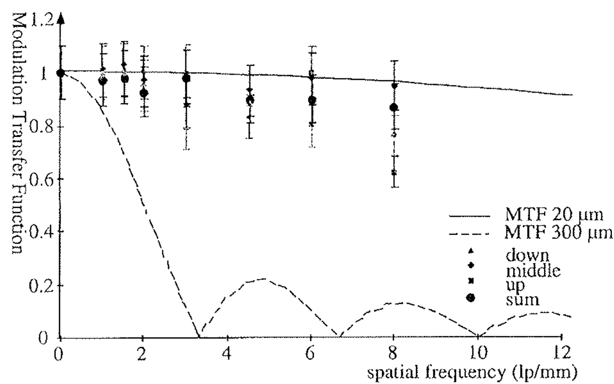


Fig. 6. Modulation Transfer Function of the device when samples are imaged with a scanning step equal to 20 μm, compared to the theoretical MTF of a 300 μm pixel. The plot demonstrates the possibility of achieving enhanced spatial resolution by applying the deconvolution procedure (see text).

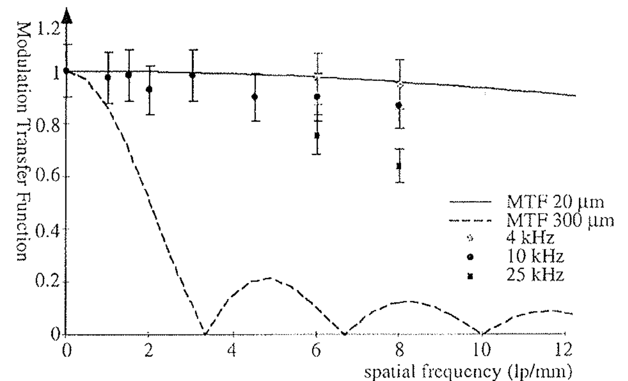


Fig. 7. Modulation Transfer Function of the device (when samples are radiographed with a scanning step equal to 20 μm) as a function of the incident rate. Saturation problems that occur at high rates affect also the spatial resolution of the device (see text).

Finally, the effect of high-rate saturation on spatial resolution has been estimated. The results presented in Fig. 5 and Fig. 6 have been obtained with a counting rate equal to 10 kHz; for comparison purposes the higher spatial frequencies of the bar pattern test object have been also acquired at counting rates equal to 4 and 25 kHz. The results are presented in Fig. 7: only data coming from the sum of the three layers are shown. As it can be easily seen, there is a slight improvement in spatial resolution if the acquisition is performed at 4 kHz, while a non negligible loss occurs if the counting rate is increased to 25 kHz.

CONCLUSIONS

A three layer single photon counting silicon microstrip detector has been developed by the SYRMEP/FRONTRAD collaboration, in order to perform feasibility studies on digital mammography with synchrotron radiation. The device has been extensively tested at the SYRMEP beamline, in order to evaluate its imaging performances. Due to the single photon counting capability of the readout electronics, the contrast resolution is very high, limited in practice only by the quantum noise. The spatial resolution can be very good, since it is possible to increase it by selecting a sampling step smaller than the pixel size. Images are almost scatter free, since the laminar synchrotron beam is matched to the detector active surface by means of a micrometric

slit system. The detection efficiency is high (80% @ 20 keV), and this results in a dose delivered to the samples much lower than doses delivered in conventional mammographic examinations (even if this aspect has not been discussed in the present paper, detailed dose considerations can be found in /3/ and in /6/).

The tested device shows relevant limitations in the counting rate, due to the single photon counting modality chosen for the readout electronics. As discussed in this article, the single photon counting capability is of primary importance in digital mammography, since it maximizes the contrast resolution. In order to solve this problem, two strategies are under investigation. The first one - discussed in the present paper - is the possibility of stacking several detector layers one upon the other: the overall duration of the examination is reduced by a factor equal to the number of stacked layers. Secondly, a faster, second generation single photon counting readout electronics is currently under test: the design features and the simulations predict the possibility of reaching a counting rate at least 30 times higher than the present one.

REFERENCES

/1/ M.J. Yaffe and J.A. Rowlands, *X ray detectors for digital radiography,* Phys. Med. Biol. 42 (1997) 1-39

/2/ E. Burattini, E. Cossu, C. Di Maggio et al., *Mammography with synchrotron radiation,* Radiology 200 (1996) 659-663

/3/ F. Arfelli, V. Bonvicini, A. Bravin et al., *Linear array silicon pixel detector: images of a mammographic test object and evaluation of delivered doses,* Phys. Med. Biol. 42 (1997) 1565-1573

/4/ F. Arfelli, V. Bonvicini, A. Bravin et al., *Design and evaluation of AC-coupled, FOXFET biased, "edge-on" silicon strip detector for X ray imaging,* Nucl. Instrum. Meth. Phys. Res. 385 A (1997) 511-520

/5/ F. Arfelli, V. Bonvicini, A. Bravin et al., An *"edge on" silicon strip detector for X ray imaging,* IEEE Trans. Nucl. Sci. 44 (1997) 874-880

/6/ F. Arfelli, V. Bonvicini, A. Bravin et al., *Mammography of a phantom and breast tissue with synchrotron radiation and a linear-array silicon detector,* Radiology 208 (1998) 709-715

/7/ F. Arfelli, A. Bravin, G. Barbiellini et al., *Digital mammography with synchrotron radiation,* Rev. Sci. Instrum. 66 (1995) 1325-1328

/8/ C. Colledani, G. Comes, W. Dulinsky et al., *CASTOR* I.O, *a VLSI analog-digital circuit for pixel imaging applications,* Nucl. Instrum. Meth. Phys. Res. 395 A (1997) 435- 442

/9/ G.F. Knoll, *Radiation detection and measurements* (II edition), Wiley, New York, 1989

/10/ F. Arfelli, V. Bonvicini, A. Bravin et al., *New developments in the field of silicon detectors for digital radiology,* Nucl. Instrum. Meth. Phys. Res. 377 A (1996) 508-513

/11/ S. Webb ed, *The physics of medical imaging,* IOP publishing, Bristol,1988

/12/ A.L. Evans, *The evaluation of medical images,* Adam Hilger Ltd, Bristol,1981

/13/ E.O. Brigham, *The Fast Fourier Transform,* Prentice Hall, Englewood Cliffs. New Jersey,1974

F. Arfelli, V. Bonvicini, A. Bravin, G. Cantatore, E. Castelli, A.Vacchi, E. Vallazza, R. Longo, A. Olivo, S. Pani, P. Poropat, M. Prest, A. Rashevsky
Dipartimento di Fisica - Università di Trieste and INFN - Sezione di Trieste

L. Dalla Palma,
Istituto di Radiologia - Università di Trieste

L. Rigon, G. Tromba, M. Fabrizioli, D. Pontoni
Sincrotrone Trieste SCpA

Corresponding Author (olivo@trieste.infn.it)

Prispelo (Arrived) : 29.01.1999 Sprejeto (Accepted) : 03.03.1999

APLIKACIJSKI PRISPEVKI - APPLICATION ARTICLES

KAKO IZBRATI VARISTOR

Iskra VARISTOR d.o.o. proizvaja napetostno spremenljive upore (v nadaljevanju varistorje), ki se zaradi vse večje uporabe elektronike v vsakdanjem življenju in občutljivosti le-te na prenapetosti, uporabljajo skoraj v vseh vezjih.

Ime varistor izhaja iz angleških besed VARiable resISTOR. Ker je njegova glavna sestavina cink oksid (ZnO), ki je kovinski oksid, se za ta element uporablja tudi ime MOV (Metal Oxide Varistor), v angleški literaturi pa se dostikrat uporablja okrajšava VDR (Voltage Dependent Resistor).

Zaradi pravilnega delovanja naprave ali vezja v katerega je vključen varistor in zaradi same življenjske dobe varistorja je pri projektiranju prenapetostne zaščite potrebno izbrati pravi varistor.

Na kratko izbiramo v treh korakih:

1. Izberemo varistor glede na delovno napetost v naši aplikaciji.
2. Nato izbiramo še:
   a) udarni tok
   b) energijo
   c) povprečno moč na varistorju
   (Pri a in b moramo upoštevati tudi število ponovitev)
3. Na koncu preverimo še maksimalno preostalo napetost, ki ne sme biti večja od prebojne napetosti za izbrano vezje.

PRVI KORAK

Da bi zagotovili čim boljši zaščitni nivo, izberemo varistor, ki ima isto napetostno področje kot naša aplikacija ali le malce višje. Pri izbiri moramo upoštevati možen porast napetosti (približno10% na napajalno napetost), ker se disipacija moči na varistorju občutno poveča (10% povečanje napajalne napetosti pomeni 15-kratno povečanje disipacije moči).

Opomba: Seveda lahko izberemo vsak varistor z višjo delovno napetostjo. Tako postopamo, kadar nam je izjemno nizek prepustni tok bolj pomemben, kot pa čim nižji zaščitni nivo.

DRUGI KORAK

Z izbiro maksimalne možne delovne napetosti v prvem koraku smo zmanjšali število ustreznih varistorjev na maksimalno 8 tipov (npr. za 220V AC, 8 tipov V250, V250K5 - V250S40).

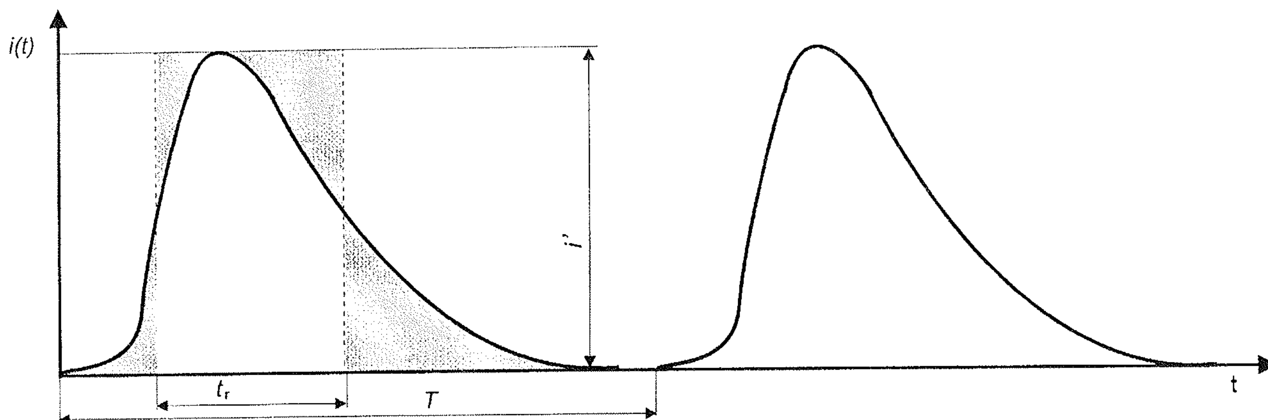
Sedaj moramo določiti energijo, moč in maksimalni tok, ki jih mora prenesti varistor glede na delovne pogoje. Te vrednosti moramo primerjati z maksimalnimi vrednostmi, podanimi v tabelah. Izberemo lahko vse varistorje, katerih vrednosti za maksimalni udarni tok, energijo in moč ležijo nad vrednostmi za določeno aplikacijo.

Da bi se izognili dvomom in napakam pri izračunavanju vrednosti za določeno aplikacijo, moramo upoštevati naslednje:

- maksimalne obremenitve varistorja, ki so odvisne od okolja (temperatura), bomo označili z " ´ "
- maksimalne mejne vrednosti, ki so omejene z udarnim tokom in absorbcijo energije, bomo označili z "max".

$$i' \leq i_{max}$$
$$E' \leq E_{max}$$
$$P' \leq P_{max}$$

Ko določamo obremenitve na varistorju, moramo vedno upoštevati maksimalne možne obremenitve (npr. varistor mora absorbirati vso shranjeno energijo $1/2\ Li^2$ tuljave). Tak izračun bo potem vedno imel določeno rezervo zaradi izgub v ostalih komponentah vezja.



Slika 1

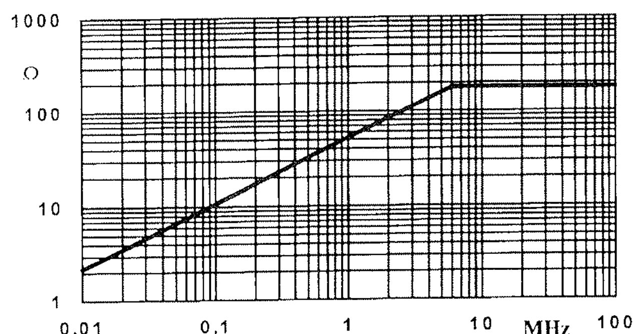
a) Udarni tok

Vrednost maksimalnega toka varistorja je odvisna od dolžine impulza in števila ponovitev. To vrednost lahko razberemo iz U/I krivulj. Maksimalni možni udarni tok varistorja v določeni aplikaciji nam tako služi kot osnova za primerjavo.

U/I krivulje nam prikazujejo maksimalne vrednosti toka pravokotne oblike. Da bomo lahko pravilno primerjali maksimalne vrednosti, moramo dejansko obliko vala pretvoriti v pravokotni impulz. Najbolj preprost način je grafična metoda.

Ohranjajoč vršno vrednost, udarni tok pretvorimo v pravokotnik z isto površino. Tr predstavlja dolžino impulza in je identičen dolžini impulza v U/I krivuljah. Periodo T potrebujemo za izračun povprečne izgube moči kot rezultat periodičnih energijskih impulzov.

Opomba: To pomeni, da za izbiro potrebujemo tok in ne napetost, ki povzroča tok. Zelo nizka impedanca napajalnih linij pri delovnih frekvencah je največkrat napačno uporabljena za izračun amplitude toka potujočega vala na močnostnih ali podatkovnih linijah.Upoštevati moramo, da pri frekvencah v kHz in MHz področju (tranzientni tokovi) občutno višje karakteristične impedance linije določajo razmerje med tokom in napetostjo.



Slika 2

Na zgornjem grafu lahko vidimo vrednosti impedance v odvisnosti od frekvence za omrežje.

b) Energija

Če teče tok skozi varistor, ga največkrat navezujemo na energijsko absorbcijo. Na splošno velja sledeče:

$$\int_{t_0}^{t_1} v(t)i(t)dt$$

Ta integral je najbolj preprosto rešljiv z grafičnim načinom (pretvorba v ekvivalentni pravokotni tok in napetost):

Če je bil tok, ki teče skozi varistor ugotovljen s pomočjo spominskega osciloskopa in pretvorjen v ekvivalentni pravokotnik, lahko absorbcijo energije varistorja izračunamo s preprostim zmnožkom toka in padca napetosti, ki se pojavi na varistorju:

$E' = v' \, i' \, t_R$ [J] $\qquad v'$ [V]
i' [A]
t_R [s]

v' lahko vzamemo iz pripadajoče U/I krivulje kot vrednost napetosti v odvisnosti od i' ali pa jo določimo s pomočjo spominskega osciloskopa kot maksimalni padec napetosti na varistorju.

Če je prenapetost posledica preklopa induktivnih bremen, moramo pri izračunu energijske absorbcije upoštevati induktivni tok.

Energija, absorbirana v varistorju, ne more biti večja od energije, shranjene v tuljavi:

$E = 1/2 \, Li^2$ [J] $\qquad L$ [H]
I [A]

Ta izračun vedno upošteva rezervo glede na izgube drugih komponent v vezju, ki ga ščitimo. Impulzi, ki se pojavljajo pri preklopih induktivnih bremen, navadno ležijo v področju milisekund.

Energijo, določeno na podlagi zgornjega izračuna, lahko primerjamo z vrednostmi energije (2ms), podanimi v tabeli 1. V tem primeru je maksimalna energija, ki jo varistor lahko absorbira, skoraj neodvisna od trajanja energijskega impulza.

Tabela 1

Tip	Maksimalne vrednosti T_A=+85°C (+185°F)						Karakteristika T_A=+25°C (+77°F)			
	RMS Napetost	DC Napetost	Izgubni faktor moči	Maks. tok (8/20μs)	Energija (2ms)		Nazivna napetost (1mA)	Toleranca	Maximum Clamping Voltage at Test Current (8/20μs)	
	V_{RMS} (V)	V_{DC} (V)	P_{max} (W)	I_{max} (A)	E_{max} (J)	$E_{neskončno}$ (J)	V_N (V)	(%)	U (V)	I (A)
V250D25 V250D32 V250D40	250	320	1.0	15000 25000 40000	390 800 1440	0,1 0,2 0,2	430	±10	340	150 200 300

Ostale vrednosti, ki niso navedene v zgornji tabeli, lahko najdete v katalogu Iskre VARISTOR .

Primerjava vrednosti energij pomeni, da ni vedno potrebno določiti udarnega toka in časa trajanja impulza (glej a. Udarni tok).

c) Izgubni faktor moči (trajna moč, ki se lahko troši na varistorju)

Če je bil varistor določen glede na prvi korak, je to zagotovilo, da bo moč na varistorju pri delovni napetosti zanemarljivo nizka.

Če je zahtevano, da varistor absorbira energijo periodično, je to povezano s povprečno močjo, ki se lahko troši na varistorju:

$$P = \frac{E}{T} = \frac{v \; i \; t_r}{T} \qquad [W]$$

T [s] = dolžina periode

E je vrednost posameznega energijskega vala (izračunanega na podlagi "metode pravokotnika"), T pa predstavlja čas med eno in drugo ponovitvijo impulza. Iz enačbe lahko izračunamo minimalni čas, ki mora preteči med enim in drugim impulzom, ne da bi presegli maksimalno moč disipacije:

$$T_{min} = \frac{E}{P_{max}} \qquad [s]$$

ZnO varistorji so manj primerni za statične obremenitve (npr. napetostna stabilizacija). Za te namene raje uporabljamo Z diode.

TRETJI KORAK

Maksimalno preostalo napetost na varistorju v primeru prenapetosti lahko razberemo iz U/I krivulje. To vrednost lahko razberemo direktno, če poznamo udarni tok.

Če razbrana vrednost presega prebojno trdnost komponent, ki jih ščitimo, imamo na voljo sledeče možnosti, da znižamo zaščitni nivo:

- zmanjšamo varnostni nivo pri izbiri napetosti (npr. za mrežno napetost 220V uporabimo V230 namesto V250.)
- izboljšamo ujemanje varistorja z napetostjo mreže (npr. za 320 AC napetost +10% dobimo 350V). Glede na prvi korak izberemo varistor V385. Lahko pa vežemo dva varistorja V175 v serijo in s tem dobimo V350, kar pomeni za 35V boljši zaščitni nivo.
- izberemo lahko tudi specialno toleranco varistorja (npr. samo spodnji del tolerančnega območja, kar izboljša zaščitni nivo za 10%).
- lahko pa izberemo varistor z večjim K - jem (npr. V250K20 namesto V250K14). S tem smo pridobili večji zaščitni nivo, ker ima varistor pri istem udarnem toku nižjo preostalo napetost in nenazadnje tudi daljšo življenjsko dobo, ker je manj obremenjen.

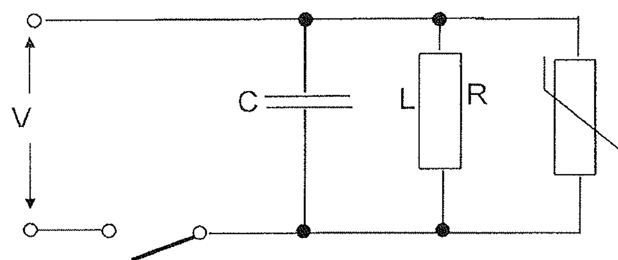
PRIMERI

PREKLAPLJANJE INDUKTIVNIH BREMEN

Pri odklopu induktivnih bremen se pojavijo prenapetosti, ki lahko poškodujejo stikalo (npr. tranzistor) ali pa celo samo tuljavo. Glede na enačbo je energija shranjena v tuljavi 1/2 Li^2. Pri odklopu ta energija napolni kondenzator, ki je vezan paralelno tuljavi (ta kondenzator je seveda lahko tudi kapacitivnost same tuljave). Če ne upoštevamo izgub, to pomeni: 1/2 C v^2 = 1/2 L i^2

$$v' = i'\sqrt{\frac{L}{C}} = \sqrt{\frac{0.1}{250x10^{-12}}} = 20000V$$

Varistor mora biti vezan paralelno tuljavi, da lahko zniža prenapetost.



V = 24 V_{DC}
L = 0,1 H
R = 24 Ω
I = 1 A
C = 250 pF
št. preklopov > 10^6

PRVI KORAK

Za dosego čim nižjega zaščitnega nivoja, izberemo varistor V20 glede na njegovo maksimalno enosmerno napetost (glede na katalog Iskre VARISTOR so ti varistorji primerni za enosmerne napetosti do 26V), kar pomeni da lahko izberemo katerikoli varistor od V20K5 do V20K20.

Tip	Maksimalne vrednosti T_A=+85°C (+185°F)						Karakteristika T_A=+25°C (+77°F)			
	RMS Napetost	DC Napetost	Izgubni faktor moči	Maks. tok (8/20μs)	Energija (2ms)		Nazivna napetost (1mA)	Toleranca nazivne napetosti	Maximum Clamping Voltage at Test Current (8/20μs)	
	V_{RMS} (V)	V_{DC} (V)	P_{max} (W)	I_{max} (A)	E_{max} (J)	$E_{neskončno}$ (J)	V_N (V)	(%)	U (V)	I (A)
V20K5					0,8	0,05				1
V20K7			0,02	250	1,6	0,12				2,5
V20K10	20	26	0,05	500	3,8	0,33	33	±10	65	5
V20K14			0,10	1000	7	0,34				10

Ostale vrednosti, ki niso navedene v zgornji tabeli, lahko najdete v katalogu Iskre VARISTOR

DRUGI KORAK

a) Tok skozi varistor

Ko izključimo tuljavo, se tok skozi tuljavo in varistor ne spremeni v trenutku. Nekaj časa se še vzdržuje delovni tok 1A, nato pa eksponencialno začne padati proti ničli. Ta tok lahko določimo z osciloskopom ali z eksponencialno krivuljo. Po pretvorbi v ekvivalentno kvadratno obliko impulza lahko to vrednost uporabimo za primerjavo z U/I krivuljami ter za določitev tipa varistorja. Seveda pa je najlažje izbrati pravi tip varistorja glede na energijo.

b) Energijska absorbcija varistorja

Iz enačbe lahko razberemo, da mora varistor absorbirati energijo

$E' = 1/2\, Li^2 = 1/2 \times 0.1H \times 1A^2 = 0{,}05\ J$

za en preklop.

Take prenapetosti ležijo v področju milisekund, zato izberemo vrednosti pri 2ms za izračun ter neskončno preklopov. Za te vrednosti odgovarja varistor V20K5, vendar brez varnostne rezerve. Zato je bolje, da izberemo V20K7.

c) Povprečna izgubna moč

Maksimalna povprečna izgubna moč za varistor V20K7 je 0.02W. Glede na enačbo je minimalni čas med dvema intervaloma:

$$T_{min} = \frac{E'}{P_{max}} = \frac{0.05J}{0.02W} = 2.5s$$

Če so intervali pogostejši, je potrebno izbrati varistor z višjo močjo (glej katalog Iskra VARISTOR, stran 8).

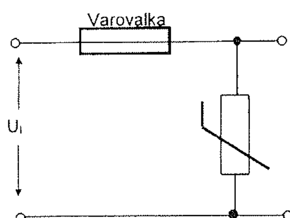
TRETJI KORAK

Zaradi toka skozi varistor (1A) dobimo na tuljavi maksimalno napetost 60V (za varistor na zgornji tolerančni meji). To vrednost razberemo iz U/I krivulj v katalogu Iskre VARISTOR, stran 17.

ZAŠČITA PROTI OMREŽNIM PRENAPETOSTIM

Risba spodaj kaže zaščito proti omrežnim prenapetostim, ki jih lahko pričakujemo v izpostavljenih omrežjih.

Omrežna napetost	U_L =220V
Prenapetostna amplituda	U_T =5kV
Karakteristična impedanca mreže . .	Z = 25Ω
Širina tokovnega impulza	t_R = 500μs
Maksimalno število prenapetosti v življenjski dobi	<100 krat



PRVI KORAK

Za napetost 220V lahko glede na katalog Iskre VARISTOR izbiramo med osmimi tipi V250 (če upoštevamo 10% toleranco mreže):

VARISTOR-V250K5
.
.
VARISTOR-V250S40

DRUGI KORAK

a) Tok skozi varistor

Amplitudo toka lahko izračunamo iz vrednosti prenapetosti in karakteristične impedance Z_{ch} - (predpostavimo, da je ta vrednost 25Ω, slika 2).

$$i' = \frac{V_T}{Z_{ch}} = \frac{5kV}{25\Omega} = 200A$$

Obliko in trajanje tokovnega vala (po pretvorbi v pravokotno obliko) moramo preračunati tako, da je rezultat širina impulza 500μs. Za trajanje in število prenapetosti lahko rečemo, da so naključna, zato moramo upoštevati vsaj 100 impulzov v življenjski dobi.

Vrednostim 200A, 500μs, 100-krat ustreza varistor V250D32 i_{max} = 350A (kar razberemo iz krivulj v katalogu Iskra VARISTOR, stran 35).

b) Energijska absorbcija varistorja

Kot smo že ugotovili, je maksimalna energija, ki jo varistor lahko sprejme, v odvisnosti od maksimalnega toka. Zato varistor, ki ga izberemo na osnovi toka, ustreza tudi zahtevam za energijsko absorbcijo $E' \leq E_{max}$.

Vseeno pa moramo določiti energijsko absorbcijo varistorja V250D32 glede na enačbo:

$E' = v'\, i'\ t_R = 620V \times 200A \times 500\mu s = 62J$

c) Maksimalna povprečna moč disipacije

Zaradi narave omrežne napetosti ne moremo predvideti, da se neka prenapetost z zgoraj navedeno amplitudo periodično ponavlja. Iz tega je razvidno, da ni nujen pogoj $P' \leq P_{max}$. Minimalni čas med dvema energijskima impulzoma bomo izračunali le zaradi popolnosti izračuna:

$$T_{min} = \frac{E'}{P_{max}} = \frac{62J}{1.2W} = 51.6s$$

TRETJI KORAK

Zaščitni nivo (za varistor na zgornji tolerančni meji) smo že določili v poglavju b. To pomeni, da je prenapetost omejena na vrednost nekaj odstotkov od začetne vrednosti.

Opomba: Prenapetosti ne moremo natančno izračunati ali predvideti in jih zato ne moremo simulirati v laboratorijih. Zato je vedno pametno izbrati večji varistor kot smo izračunali (v našem primeru V250D40).

Iskra Varistor d.o.o.
Hariš Mitja
Stegne 35, 1000 Ljubljana
SLOVENIJA

PRIKAZ MAGISTRSKIH DEL IN DOKTORATOV V LETU 1998
M. S. and Ph. D. ABSTRACTS, YEAR 1998

MAGISTRSKA DELA

Naslov naloge: **Izračun transparence z metodo stopničaste aproksimacije poljubne oblike potencialne bariere ter njena uporaba v polprevodniških strukturah**

Avtor: **Matej Kamin,** dipl.ing.
Mentor: **prof. dr. Jože Furlan**
Univerza v Ljubljani, Fakulteta za elektrotehniko

Veliko eksperimentov je pokazalo, da se v nekaterih primerih svetloba obnaša kot gibanje delca, medtem ko se npr. elektroni v nekaterih primerih obnašajo kot valovanje. Ta dvojni karakter svetlobe in gibanja materialnih delcev ne moremo razložiti z enačbami klasične fizike kot so Newtonove in Maxwellove enačbe, ampak je potrebno formulirati neko novo enačbo.

Gibanje teles obravnavamo z Newtonovimi zakoni klasične mehanike. S pomočjo teh zakonov izračunamo lego teles v poljubnih trenutkih in tudi predvidimo njihovo bodoče obnašanje. Gibanje atomarnih delcev pa je statistično nedoločeno, lahko govorimo le o verjetnosti, da je delec v nekem trenutku na določenem mestu. Materialni delci se obnašajo podobno kot fotoni, katerih pot je ravno tako nedoločena. Z elektromagnetnim valovanjem sicer ne moremo predvideti, kako fotoni kot posamezniki potujejo, dobro pa popisujemo povprečno obnašanje velikega števila fotonov. Po analogiji s fotoni in EMV pričakujemo, da obstaja valovanje, ki popisuje povprečno obnašanje materialnih delcev. Takšno valovanje imenujemo materialno valovanje, katerega opišemo s Schrödingerjevo diferencialno enačbo. Pot, ki vodi do nastanka te enačbe, njena rešitev, valovna funkcija ter lastnosti valovne funkcije, so opisane v prvem poglavju

Gostota verjetnostne porazdelitve delcev igra pomembno vlogo pri opazovanju in gibanju delcev. Ta pove, s kakšno verjetnostjo se delec nahaja na določenem mestu v prostoru. Izkaže se, da tudi materialni delec z neko maso m lahko najdemo kjerkoli v prostoru, če je le njegovo gibanje neomejeno. V primeru, da delec naleti na neko oviro, se zaradi lastnosti valovanja od nje popolnoma ali deloma odbije oziroma delno nadaljuje svojo pot, odvisno od prepustnosti ovire. V naših primerih elektroni prehajajo preko ali skozi določeno potencialno bariero. Verjetnost, da se bo delec znašel tudi na drugi strani bariere, določa transparenca ali transparentnost potencialne bariere. O transparenci in odbojnosti ter o energijskih razmerah pri prehodu delcev skozi bariero govorimo v drugem poglavju.

V tretjem poglavju nekoliko bolj podrobno analiziramo pravokotno potencialno bariero in pravokotni potencialni lijak. Že v prvem poglavju ugotovimo, da je krajevni del Schrödingerjeve diferencialne enačbe relativno enostavno rešiti le v primeru, če se potencial oziroma potencialna energija krajevno ne spreminjata. Le na ta način hitro pridemo do točne rešitve. V primeru, da potencialna energija ni konstantna, pa je Schrödingerjevo enačbo razmeroma težko rešiti. Z nekaterimi poenostavitvami se sicer analitično da priti do rešitev, vendar so te le aproksimativne. Če hočemo priti do precej natančnih rezultatov, moramo v takšnih primerih uporabiti numerično metodo reševanja. Tako poljuben potek potenciala aproksimiramo s stopničasto funkcijo, kjer je vsak segment zase pravokotna bariera določene širine. Prav zato si lastnosti pravokotne bariere v tretjem poglavju nekoliko bolj natančno ogledamo. Prikazan je potek izračuna transparence in analiza razmer pri prehodu delcev skozi in preko bariere. Pri prehodu preko bariere v določenih primerih naletimo na resonančni pojav. Poleg tega analiziramo tudi pravokotni lijak, ki nam pomaga razložiti pojav diskretnih energijskih nivojev v atomih in kasneje tudi resonančni pojav pri prehodu delcev skozi dvojno pravokotno bariero.

Sledi četrto poglavje, v katerem je predstavljena numerična metoda izračuna transparence za poljubno obliko potencialne bariere. Najprej smo zapisali matrično enačbo za pravokotno potencialno bariero. Dokazali smo enakost transparence v obeh smereh, tudi za nesimetrično strukturo. Sledi splošen zapis matrike koeficientov in končne matrične enačbe ter seveda izraza za izračun transparence. Na osnovi tega zaključimo, da enakost transparence v obeh smereh velja tudi za povsem poljubno obliko bariere. Na koncu poglavja analiziramo še razmere, ko upoštevamo tudi spremembo efektivne mase delcev m. Obe matriki koeficientov med seboj tudi primerjamo.

Uporabo numerične metode prikažemo v zadnjem poglavju na treh različnih primerih potencialnih barier. Prva je trikotna bariera. V primeru močno dopirane polprevodniške strukture lahko potek potenciala aproksimiramo z linearno funkcijo. Na ta način lahko pri analizi tunelskega efekta obravnavamo trikotno obliko bariere, ki zaradi svoje oblike omogoča precej enostaven izračun transparence po aproksimativni WKB (Wentzel Kramers Brillouin) metodi. Ta metoda je na kratko predstavljena v dodatku B, njena uporaba pa v tem poglavju. Na primeru trikotne bariere, ki modelira tuneliranje nosilcev v lokalizirane nivoje prepovedanega pasu n^+p^+ spoja, dobljene izračune po numerični poti in WKB metodi med sabo primerjamo in na ta način ugotavljamo veljavnost že omenjene aproksimativne metode.

Sledi analiza Schottkyeve bariere, ki nastane na spoju kovina-polprevodnik. Obravnavamo konkreten primer Schottkyeve diode in vpliv zunanje prevodne napetosti. Opazimo lahko močno odvisnost velikosti transparence od koncentracije primesi v polprevodniku in tudi od velikosti prevodne napetosti. Od transparentnosti bariere pa močno zavisi velikost tunelskega toka in s tem celotnega toka skozi diodo. Tudi tu rezultate primerjamo z WKB metodo, ki se v literaturah pogosto uporablja.

Nazadnje obravnavamo še primer dvojne pravokotne bariere kot resonančne strukture. Najprej analiziramo bariero izven termičnega ravnovesja. Preko izrazitega resonančnega efekta transparence opazujemo kvazi-energijske nivoje /20/, pri katerih se delci skozi strukturo gibajo brez slabljenja. Te nivoje primerjamo s pravimi diskretnimi nivoji, dobljenimi z analizo pravokotnega potencialnega lijaka. Strukturo nato priključimo na zunanjo napetost in ugotovimo, da pri določenih velikostih napetosti, kvazi-nivoji oziroma vrhovi transparence, kjer nastopi resonančni efekt, postopoma izginejo. To pa v tokovno-napetostni karakteristiki povzroči upad toka z naraščajočo napetostjo oziroma pojav negativne upornosti. Takšen potek je značilen tudi za tunelsko diodo.

Naslov naloge: **Prenos programa SPICE v okolje Windows in njegova nadgradnja**

Avtor: **Janez Puhan,** dipl. Ing.

Mentor: **prof. dr. Franc Bratkovič**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Načrtovanje analognih elektronskih vezij zahteva ogromno inženirskega znanja in izkušenj. Že dalj časa so načrtovalcem v pomoč računalniki. Ti so sposobni hitro opraviti analizo vezja in simulirati določeno dogajanje v njem. Tako so se že pred več desetletji pojavili prvi programi za analizo elektronskih vezij. Kot zmagovalec se je iz množice programov izšel program SPICE, ki danes nesporno predstavlja industrijski standard na tem področju.

Sprva so računalniške analize vezij opravljali predvsem na velikih računalnikih. S prihodom zmogljivejših osebnih računalnikov pa veliki računalniki v ta namen niso bili več potrebni. V tem trenutku se pojavi tudi več komercialnih ponudnikov SPICE-a. Komercialni ponudniki so se usmerili predvsem v izdelavo pre- in post-procesorjev, ki so močno poenostavili in pohitrili vnos vezja in prikaz rezultatov.

Za interaktivno delo s SPICE-om je bil razvit interpreterski programski jezik NUTMEG. Vendar pa nihče izmed komercialnih ponudnikov NUTMEG-a ni ponudil, oziroma le v močno okrnjeni obliki. Zato se v delu ukvarjamo s prenosom originalne izvorne kode iz matičnega operacijskega sistema UNIX na osebni računalnik z operacijskim sistemom Windows 95 ali Windows NT. S prevajanjem originalne izvorne kode za ta dva operacijska sistema dobimo na osebnem računalniku delujočo različico SPICE-a s polno podporo NUTMEG-u. Prevedena je bila najnovejša različica Berkeley jevske izvorne kode, to je SPICE 3f4.

Da je SPICE skupaj z NUTMEG-om na osebnem računalniku resnično zaživel, je bilo treba izdelati ustrezen program za grafični prikaz rezultatov v zgoraj omenjenih operacijskih sistemih. Izdelan program je v delu podrobneje opisan.

Naslednji korak pri načrtovanju elektronskih vezij s pomočjo računalnika pa je optimizacija elektronskih vezij. V program za analizo vezij je v tem primeru potrebno vgraditi optimizacijski algoritem. Nekatere komercialne različice SPICE-a že ponujajo nekatere zelo omejene možnosti optimizacije vezij. V delu so preizkušene različne možnosti pristopov k optimizaciji analognih elektronskih vezij s SPICE-om. Pri tem je bil cilj nadgradnja SPICE-a s povsem splošno optimizacijsko zanko, kjer bi uporabnik lahko poljubno izbiral parametre, eksplicitne in implicitne omejitve, kriterijsko funkcijo itd.

Če pustimo ob strani samo optimizacijsko metodo, je pri optimizaciji za praktično uporabnost predvsem pomemben računski čas. Pri tem je mišljen predvsem čas, ki ga računalnik porabi za določevanje naslednje iteracije, komunikacijo z jedrom programa za analizo vezij itd. Računski časi različnih pristopov so izmerjeni in podani.

V delu je poraba računskega časa za različna opravila v optimizacijski zanki podrobneje razčlenjena. Rezultati so obrazloženi in ovrednoteni. Izkazalo se je, da je za nadaljnji študij in praktično uporabo zanimiva optimizacijska zanka, ki bi bila narejena v NUTMEG-u. Morda bi bilo vredno podrobneje razmisliti še o optimizacijski zanki zakodirani v samostojnem programu, ki bi uporabljal SPICE kot podprogram.

Naslov naloge: **Prototipni sistem za digitalno obdelavo slik**

Avtor: **Andrej Trost**, dipl. Ing.

Mentor: **prof. dr. Baldomir Zajc**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Za obdelavo digitalnih slik v realnem času uporabljamo specializirane procesorje ali digitalna vezja. Digitalna vezja za obdelavo slik načrtujemo kot naročniška ali pol-naročniška integrirana vezja ali pa jih zgradimo z uporabo programirljivih vezij. Tehnologija programirljivih vezij danes omogoča emulacijo kompleksnih digitalnih vezij v enem samem programirljivem vezju. Programirljiva vezja se uporabljajo za izdelavo prototipnih sistemov, na katerih načrtujemo in preizkušamo digitalna vezja.

Delo prikazuje prototipni sistem na osnovi programirljivih vezij, ki se uporablja za načrtovanje in strojno verifikacijo vezij za digitalno obdelavo slik. Prototipni sistem sestavlja računalniška kartica z dvema FPGA vezjema XC4010. Povezava z osebnim računalnikom omogoča enostavno konfiguriranje programirljivih vezij in izvedbo strojne verifikacije načrtanega prototipnega vezja. Na računalniško kartico sta priključeni še dodatni vezji z mikrokrmilnikom in zunanjim pomnilnikom. Dodatni vezji tvorita, skupaj z vmesnikom v programirljivih vezjih, sistem za emulacijo neodvisnih pomnilnikov, ki jih potrebujemo v vezjih za obdelavo slik.

Prototipni sistem omogoča izvedbo posameznih operatorjev za obdelavo slike v realnem času. V programirljivih vezjih je tudi vmesnik za testiranje prototipnega vezja preko ISA vodila v osebnem računalniku. Vmesnik se naredi posebej za vsako prototipno vezje, kar zelo poveča prilagodljivost sistema. Napisali smo programe za avtomatsko sintezo vmesnika za testiranje vezij in vmesnika za emulacijo pomnilnikov. Programi so vključeni v potek načrtovanja vezij v programirljivi

tehnologiji in omogočajo izvedbo načrtovanega vezja na prototipnem sistemu brez poznavanja podrobnosti v zgradbi sistema. Za testiranje oz. strojno verifikacijo prototipnih vezij smo napisali program, s katerim interaktivno nastavljamo testne vektorje, opazujemo rezultate in vsebino pomnilnikov ter testiramo vezja za obdelavo slik s testnimi slikami.

Pokazali smo, da je prototipni sistem kljub majhni velikosti dovolj prilagodljiv, da omogoča izvedbo operatorjev za segmentacijo slike. Algoritme najprej preizkušamo v simulacijskem okolju s programskim jezikom C, potem pa načrtujemo vezja z orodji za shematski vnos ali pa z orodji za opis vezja v jeziku VHDL in sintezo vezja.

Naslov naloge: **Referenčna temperaturna tarča za preskus pasivnih in infrardečih detektorjev**

Avtor: **Mihal Kiselja**, dipl. ing.
Mentor: **prof. dr. Peter Šuhel**
Univerza v Ljubljani, Fakulteta za elektrotehniko

Pričujoče delo poskuša predstaviti možnost izdelave referenčne temperaturne tarče za preskus funkcionalnega delovanja pasivnih infrardečih detektorjev. Referenčno temperaturno tarčo in postopek preskusa definira standard IEC836-2-6:1990. V delu je podana analiza prenosa toplote na tarči. Izdelan je diskretni model toplotnega polja tarče, ki omogoča izračun stacionamega in nestacionamega stanja toplotnega polja.

Nakazana je možnost rešitve tarče, ki zagotavlja razliko temperature na poljubni točki manjše od 0.2°C od povprečne temperature na tarči. Možna rešitev tarče uporablja bakreno pločevino debeline 1.5 mm, meritev temperature s pomočjo termočlena baker-konstantan in segrevanje z grelci nameščenimi na hrbtni strani tarče.

Za predlagano rešitev je podana problematika merjenja temperature na tarči in med tarčo ter površino ozadja. Na podlagi izračuna stacionarnega stanja toplotnega polja je podana analiza razlike temperature poljubne točke tarče od povprečne temperature na tarči, in razlike povprečne temperature na tarči od temperature ozadja.

Naslov naloge: **Model dielektričnega preboja**

Avtor: **Aleš Berkopec**, dipl. ing.
Mentor: **prof. dr. Vojko Valenčič**
Univerza v Ljubljani, Fakulteta za elektrotehniko

Uvod smo namenili splošnemu pojmu preboja, nadaljevali pa z detaljnim opisom procesa v atmosferi, ker je njegov razvoj najdlje opisovan ter najbolje dokumentiran.

Za geometrijsko izolirane, maloštevilne prevodnike v tridimenzionalnem modelu z vmesnim homogenim prevodnikom smo diskretizirali prostor v duhu momentne metode, algoritem pa naslonili na znanje o atmosferskem preboju. Uporabili smo kvazistatični približek reševanja električnega polja, kjer čas kot spremenljivka eksplicitno ne nastopa, temveč ga simuliramo s koraki v algoritmu. V ostanku poglavja o zasnovi modela smo vpeljali posplošeno temperaturo izolatorja in strukturo prevodnega kanala z dopustnimi cepitvami. V prostoru rešitev za dano geometrijo ostaneta prosta parametra širina prevodnega kanala in temperatura izolatorja.

Med rezultati smo posvetili zajeten kos testnim primerom iz elektrostatike in oceni napake. Iz množice slik, ki so nastale v času oblikovanja naloge, smo jih nekaj predstavili v rednem delu in dodatku. V bistvu algoritma se skriva utežna funkcija naključnih števil, ki jo zaganjamo z vsakič drugačnim semenom, zato so rezultati modelov za enake vhodne podatke praviloma vedno različni.

Na koncu smo pokazali, da temperaturna opredelitev modelnega izolatorja vodi do rešitev, ki zajemajo večino tistih iz narave. Težave s primernim vrednotenjem rezultatov ne reši navidezna podobnost s preboji v naravi, a je na žalost v tem primeru neizogibna. Od hladnega preboja brez cepitev, do emisije elektronov s površine prevodnika nas v modelu vodi en sam parameter. Rezultati tako namigujejo na možnost sinteze prebojev, ker so različne razelektritve, vsaj v plinastih sistemih, lahko posledica enotnega mehanizma.

Naslov naloge: **Zasnova protokola zveze nosilnega kanala za vmesnik V5.2**

Avtor: **Matjaž Žibert**, dipl.ing.
Mentor: **prof. dr. Janez Trontelj**
Univerza v Ljubljani, Fakulteta za elektrotehniko

1 Namen

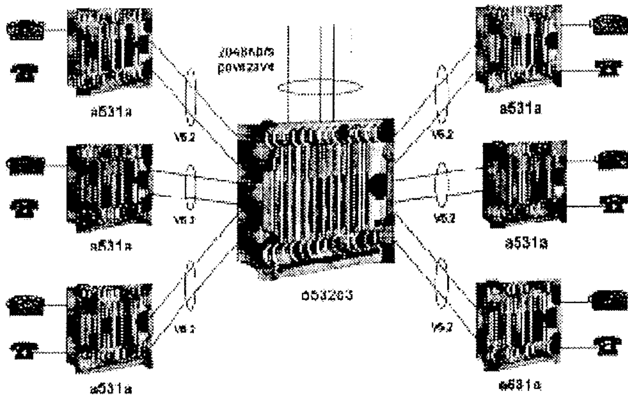
Namen tega magistrskega dela je prikazati razvoj, realizacijo in integracijo vmesnika V5.2 v že obstoječo ISDN telefonsko centralo SI2000 - verzije 5. ki je bila realizirana v podjetju ISKRATEL v Kranju.

Dokument predstavlja specifikacijo zasnove programske opreme protokola BCC vmesnika V5.2 v sistemu SI2000 verzije 5 in služi kot vhodni dokument za izdelavo programske opreme.

Sistem SI2000 - verzije 5 trenutno vsebuje več produktov verzije 5, vendar pa v tej dosedanji verigi produktov manjka produkt, ki bi imel funkcionalnost velike centrale. To pomeni, da bi produkt vseboval veliko uporabniških priključkov in veliko 2048kb/s priključkov za priključevanje centrale v telefonsko omrežje. Trenutno je v sistemu SI2000 - verzije 5 možno takšno funkcionalnost doseči s pomočjo produkta o541a in AXM-ov (verzija 4), le ti pa ne podpirajo ISDN funkcionalnosti.

Za realizacijo telefonske centrale, ki bi zadoščala tem zahtevam (veliko analognih in priključkov ISDN ter veliko 2048kb/s povezav), je primeren vmesnik V5.2. Za centralno enoto bi lahko vzeli produkt o532c3, za perif-

erne enote pa produkt a531a. Periferne enote bi na centralno enoto povezali preko vmesnikov V5.2.



Slika 1: Zasnova velike centrale

Vmesnik V5.2 je sestavljen iz dveh strani:
- dostopovnega omrežja in
- krajevne centrale

S stališča vmesnika V5.2 bi bila centralna enota (o532c3) krajevna centrala, periferne enote (a531a) pa dostopovna omrežja.

Vmesnik V5.2 je sestavljen iz naslednjih zaključenih celot:

-podatkovna povezovalna plast	- Data Link Layer
-protokol za analogno telefonijo	- PSTN Protocol
-krmilni protoko	- Control Protocol
-protokol zveze nosilnega kanala	**- BCC (Bearer Channel Connection) Protocol**[1]
- protokol krmiljenja povezave	- Link Control Protocol in
-zaščitni protokol	- Protection Protocol.

Naloge teh posameznih enot so podane v uvodu tega dokumenta. Glede na to, da sta zadnja dva protokola (protokol krmiljenja povezave in zaščitni protokol) namenjena zaščiti vmesnika V5.2 (morebitni izpadi linijskih plasti) in glede na to, da ima zgoraj navedena centrala kratke 2048kb/s povezave[2], izpadi povezav skoraj niso možne, bosta oba protokola v sedanjem produktu zaenkrat še izpuščena.

V tem magistrskem delu je moja naloga zasnova in realizacija protokola zveze nosilnega kanala (BCC - Bearer Channel Connection), zato je v nadaljevanju poudarek na delovanju in realizaciji protokola BCC[3].

1 V nadaljevanju dokumenta je opisana celotna realizacija protokola BCC.
2 Centralna enota in vse periferne enote se nahajajo v enem samem zaključenem sistemu.
3 V podjetju ISKRATEL se ukvarjam z razvojem in kodiranjem protokola BCC.

2 Pregled

Dokument na začetku podaja defnicije izrazov in kratic, ki so pogosto uporabljena v nadaljevanju. Vsa imena procesov, stanj končnih avtomatov, časovnikov in podatkovnih struktur, katera so uporabljena v izdelani programski kodi, so pisana s poševnim tiskom, imena sporočil pa z velikimi črkami.

V uvodnem poglavju je najprej prikazana uporaba in delovanje vmesnika V5.2 (poglavje 3).

V nadaljevanju je prikazana arhitektura protokola BCC vmesnika V5.2.

Za tem sledi zasnova programske opreme, katera je razdeljena na bloke in procese protokola BCC. Podane so tudi naloge posameznih procesov s pripadajočimi procedurami, podatkovnimi tipi in operatorji.

Za blok protokola BCC so določeni vmesniki z okolico. Prav tako so določeni vmesniki med samimi procesi bloka protokola BCC s signali in parametri, uporabljeni časovniki ter pripadajoči informacijski tokovi. Natančno so definirani vsi signali SDL in sporočila med posameznimi procesi SDL, ki se uporabljajo v izdelani programski opremi; ločeno na strani dostopovnega omrežja in krajevne centraleSledi potek inicializacije procesov protokola BCC ob zagonu celotnega sistema. Podan je potek signalov in kreacij procesov na strani dostopovnega omrežja in krajevne centrale.

V osrednjem delu dokumenta (poglavja 8 do 12) so podane analize delovanj posameznih procedur protokola BCC. Te procedure so:

ALLOCATION	za dodelitev prostega nosilnega kanala uporabniškemu priključku
DEALOCATION	za sprostitev zasedenega nosilnega kanala ob ručenju telefonske zveze
AUDIT	za obveščanje o zasedenosti uporabniških in nosilnih kanalov
AN FAULT	za obveščanje o interni okvari dostopovnega omrežja

Sledijo še poteki signalov med procesi SDL v posameznih procedurah BCC, ločeno v AN in LE strani. K signalom so dodani tudi njihovi parametri, ki so v obliki podatkovnih struktur SDL

Proti koncu dokumenta (poglavje 14) pa je prikazano še krmiljenje PCM-stikala v procedurama Allocation in Deallocation z vsemi potrebnimi podatkovnimi strukturami SDL in operatorji, ki izvajajo preslikave nad njimi.

V zaključku so podani rezultati, ki so bili doseženi v času nastajanja magistrskega dela. Pod literaturo so našteti dokumenti in standardi, na osnovi katerih je izdelana specifikacija izvedbe programske opreme protokola BCC vmesnika V5.2.

V prilogi so podane izvorne datoteke, ki so izdelane v oviru tega magistrskega dela in so napisane v programskem jeziku SDL. Za tem sledijo še realni rezultati sledenja delovanja procesov SDL na dveh testnih centralah (maketah). Pri tem je bilo uporabljeno orodje "SDL sledilnik", ki je del dosedanje programske opreme sistema SI2000 verzije 5. Na koncu so še

podani rezultati meritev realenega poteka sporočil vmesnika V5.2, ki so bila izmerjena z analizatorjem protokolov Alcatel a8619 pri vzpostavljanju in rušenju ISDN telefonske zveze preko vmesnika V5.2 med krajevno centralo in dostopovnim omrežjem. Izpisi vsebujejo sporočila protokolov BCC, krmilnega protokola in protokola DSS1.

Naslov naloge: **Procesorski modul za odčitavanje, shranjevanje, obdelavo in prenos podatkov o porabi električne energije**

Avtor: **Marko Podberšič**

Mentor: **red. prof. dr. Bogomir Horvat**

Somentor: **izr. prof. dr. Zmago Brezočnik**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

Magistrsko delo predstavlja razvoj mikroprocesorskega modula za komunikator. Komunikator je nekoliko cenejša in manj zmogljiva izvedba podatkovnega registrirnika, to je naprave za odčitavanje, shranjevanje, obdelavo in prenos podatkov o električni ali kakšni drugi energiji. V delu so opisani tako potek razvoja, zgradba in delovanje mikroprocesorskega modula, razvoj testnega programa zanj, kakor tudi funkcijski opis programa, ki je shranjen v EPROM pomnilniku. V začetnih poglavjih pa so prikazani celostni sistem nadzora energije, komunikator kot celota in vloga komunikatorja v tem sistemu.

Mikroprocesorski modul je popolnoma prilagojen za vgradnjo v komunikator. Komunikacijski vmesniki in optična komunikacija mu omogočata komunikacijo z ostalo periferijo in okolico. Vsi komunikacijski vmesniki so galvansko ločeni. Te ločitve in vsi gonilniki so izvedeni na osnovni plošči.

Naslov naloge: **Sistematski pristop h konstruiranju in gradnji visokonapetostnega napajanika s posebno U-I karakteristiko**

Avtor: **Igor Grašič**, dipl. ing.

Mentor: **prof. dr. Alojz Paulin**

Somentor: **doc. dr. Rudolf Babič**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

Namen tega magistrskega dela je prikazati konstrukcijo in gradnjo dveh praktičnih naprav: **visokonapetostnega napajalnika za ionsko getrsko črpalko** in **visokonapetostnega napajalnika za visokovakuumski merilnik s hladno katodo**. Za obe napravi veljata posebni zahtevi po obliki in višini izhodne napetosti, zahtevane so podobne lastnosti, kar se tiče časovnega poteka obremenitve napajalnika in se soočata s približno enakimi problemi na področju generiranja visoke napetosti. Osnovni mehanizemje pri obeh enak: s pomočjo visoke napetosti v merilni glavi ali črpalki vzpostavimo ionizacijo. Pri merilniku je posledično nastali ionski tok merilo za tlak, pri črpalki pa povzroči črpalne procese. Oba napajalnika morata imeti določeno obliko izhodne karakteristike. Le-ta zagotavlja trajno kratkostično obratovanje, ter se vede približno tako, kot napetostni vir z visoko notranjo upornostjo. Poseben problem predstavljajo elementi, ki so pod visoko napetostjo, visokonapetostne ter hkrati visokovakuumske prevodnice.

Ionsko getrska črpalka ne prenaša dolgotrajnih toplotnih obremenitev v času zagona črpalke. Zato mora napajalnik imeti pretokovno zaščito, ki kontrolira ionski tok na poseben način in poskrbi za pravočasni izklop napajalnika. Generirane moči so v razredu 100W. Ker gre za robustno napravo, mora biti čim preprostejša za izvedbo in kasneje tudi za uporabo.

Pri razvoju visokovakuumskega merilnika s hladno katodo smo morali zraven problema generiranja visoke napetosti, rešiti še merjenje majhnih tokov pri visokih napetostih. Osnovne zahteve so minimalne dimenzije in majhna poraba, poleg tega pa mora zagotoviti razred točnosti indikatorskih instrumentov. Merilniki vakuuma s hladno katodo namreč ne nudijo velike natančnosti zaradi za naš namen neugodnih fizikalnih procesov, zato tudi zahteve za konstrukcijo postavimo nekoliko bolj ohlapno. Poskrbeti je potrebno tudi za pretvorbo nelinearnega razmerja $i=f(p)$ med dejanskim tlakom v sistemu in merjenim ionskim tokom merilne glave. Generirane moči napajalnika na izhodu so v razredu 1W.

Naslov naloge: **Verifikacija končnih avtomatov s simboličnim preverjanjem modelov**

Avtor: **Aleš Časar**, dipl. ing.

Mentor: **izr. prof. dr. Zmago Brezočnik**

Somentor: **red. prof. dr. Bogomir Horvat**

Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

Magistrsko delo predstavlja učinkoviti orodji za obdelavo logičnih funkcij in končnih avtomatov. Učinkovitost algoritmov za iskanje dosegljivih stanj in simbolično preverjanje modelov s CTL lahko pripišemo predvsem uporabi ločenih prehajalnih relacij pri preiskovanju prostora stanj in izboljšanemu algoritmu za zamenjavo spremenljivk stanja. Ločevanje prehajalnih relacij je povsem avtomatično. Podani so eksperimentalni rezultati za množico testnih vezij ter analiza časovne in prostorske zahtevnosti programskih paketov.

DOKTORSKE DISERTACIJE

Naslov doktorske disertacije: **Načrtovanje testnih struktur za izbrane razrede analognih vezij**

Avtor: **Marina Santo Zarnik**

Mentor: **prof. dr. Franc Bratkovič**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Problem testiranja nove generacije elektronskih vezij je zelo kompleksen in njegova rešitev postaja vse bolj povezana z načrtovanjem vezja. Zato je potrebno ob načrtovanju vezja hkrati načrtovati tudi njegovo prikladnost za testiranje. Načrtovanje testiranja analognih vezij predstavlja še poseben izziv. Zaradi kompleksnosti problematike ni pričakovati ene same splošne rešitve za vsa analogna vezja, ampak je bolj smiselno iskati učinkovite metode, primerne za posamezne razrede analognih vezij. V disertaciji so obravnavane rešitve za načrtovanje testiranja aktivnih RC filtrov in kristalnih oscilatorjev.

Novejša literatura poroča o uporabi oscilacijske testne strategije za testiranje izbranih razredov analognih vezij. Tak princip je možno uporabiti tudi pri testiranju aktivnih RC filtrov. Testni postopek temelji na transformaciji obravnavanega vezja v testnem stanju v oscilator. Napake v vezju se kažejo kot sprememba frekvence osciliranja. Ker v splošnem velja, da vse komponente filtrskega vezja vplivajo na pozicijo pola v frekvenčni ravnini, zagotavlja preverjanje frekvence nedušenega pola zelo dobro pokritost napak.

V disertaciji obravnavam pristop k načrtovanju testnih struktur, namenjenih za oscilacijsko testiranje aktivnih RC filtrov. Predstavljena metodologija predvideva modifikacijo filtra z vstavljanjem testnih stikal v strukturo originalnega vezja. Pogoji, ki jih je potrebno izpolniti za transformacijo vezja v testnem stanju v oscilator, so izpeljani iz prevajalnih funkcij filtrskih vezij, oziroma položajev polov in ničel v kompleksni frekvenčni ravnini. Pri obravnavi različnih filtrskih konfiguracij se je izkazalo, da ni možno načrtati oscilacijske testne strukture na enak način za vse primere. Zato predvideva predstavljena metodologija načrtovanje dveh različnih tipov testnih struktur. Za strukture prvega tipa ja značilno, da vsebujejo eno ali več vgrajenih testnih stikal. Z ustreznim krmiljenjem stikal transformiramo filter v testnem stanju v oscilator frekvence nedušenega pola. Take testne strukture so načrtane v primeru resonatorskega filtra, KHN filtra, Sallen-Keyevega filtra ter izbrane konfiguracije ozkopasovno-zapornega filtra. Testne strukture drugega tipa vsebujejo dodatno zunanje vezje v povratni zanki. Za realizacijo zunanjega vezja se lahko uporabijo različne vezave, najbolj pa so primerne tiste konfiguracije, pri katerih je možno nastavljati poljubno amplitudo in fazo pri izbrani frekvenci. Kot predstavnika sta opisani testni strukturi za aktivne filtre z večkratno povratno zvezo v invertirajočem sistemu in filtre s frekvenčno odvisnimi negativnimi upori. V obravnavanih primerih je uporabljena za zunanje vezje posebna izvedba izenačevalnika faze.

Teoretične osnove za načrtovanje oscilacijskih testnih struktur so izpeljane ob predpostavljenih idealnih lastnostih operacijskih ojačevalnikov in vgrajenih testnih stikal. Realne karakteristike aktivnih komponent vedno nekoliko odstopajo od idealnih, zato se spremenijo tudi pogoji za transformacijo vezja v testnem stanju. Analiza teh pogojev je na primeru resonatorskega filtra pokazala, da predstavljajo testne strukture, načrtane z upoštevanjem idealnih aktivnih komponent, sprejemljivo osnovo za praktično realizacijo vezja.

V skladu s predstavljeno metodologijo smo načrtali in izdelali več različnih testnih struktur. Eksperimentalni rezultati so potrdili njihovo izvedljivost in uporabnost v praksi.

Naslednji problem, ki ga obravnavam v disertaciji, je povezan z lokalizacijo napak v kristalnih oscilatorjih. Vezje kristalnega oscilatorja lahko obravnavamo kot zaprtozančni sistem, ki ga sestavljata ojačevalnik in frekvenčno selektivno vezje s kristalom v povratni zanki. Testna struktura takega sistema omogoča prekinitev sklenjene zanke, ko je vezje v testnem stanju in ločeno preverjanje izbranega funkcijskega bloka. Opisano situacijo je možno doseči z vgrajevanjem MOS stikal na določenih mestih v originalnem oscilatorskem vezju. Z ustreznim krmiljenjem stikal se oscilator postavi v različna testna stanja, v katerih se preverjajo posamezni funkcijski deli ali komponente vezja. Pri tem se uporabijo kot vhod in izhod testne strukture obstoječi zunanji priključki oscilatorskega vezja. Število testnih stikal in njihove pozicije v strukturi vezja so odvisni od konfiguracije kristalnega oscilatorja. Zaradi nezanemarljivega vpliva vgrajenih stikal na normalno delovanje vezja postaja vprašljiva izvedljivost predlaganih testnih struktur v praksi. Iz tega razloga je namenjena analizi vpliva vgrajenih testnih stikal na normalno delovanje oscilatorja še posebna pozornost.

Metoda načrtovanja testnih struktur je predstavljena na primeru testne strukture Piercovega kristalnega oscilatorja. Eksperimenti so pokazali, da je omenjena testna struktura z vgrajenimi MOS stikali izvedljiva, vendar je potrebno vpliv testnih stikal upoštevati že pri načrtovanju vezja. Posebno pozornost je potrebno nameniti kapacitivnim vplivom testnih stikal.

Postopek testiranja temperaturno kompenziranih kristalnih oscilatorjev zahteva preverjanje normalnega delovanja vezja v širšem temperaturnem področju.

Na potek temperaturne karakteristike kristalnega oscilatorja najbolj vpliva kristalna enota, vendar pa tudi vpliv ostalih komponent, vključno s testnimi stikali, ni zanemarljiv. Eksperimentalna analiza vpliva vgrajenih testnih stikal na temperaturno karakteristiko oscilatorja je pokazala, da je tudi v tem primeru možno uporabiti za načrtovanje kompenzacijskega vezja obstoječe algoritme za temperaturno kompenzacijo kristalnih oscilatorjev brez stikal.

Pri testiranju zahtevnejših kristalnih oscilatorjev lahko naletimo na specifične napake v kristalnih enotah, ki se kažejo kot nezveznosti v temperaturni karakteristiki oscilatorja. S poglobljenim eksperimentalnim delom sem pokazala, da je take napake možno odkriti s posebnim merilnim postopkom, zasnovanim na uporabi Peltierovega elementa in senzorja temperature. Doseženi rezultati so potrdili, da je omenjena merilna metoda sprejemljiva tudi v praksi.

Na osnovi analize rezultatov eksperimentalnega dela, opravljenega na primeru Piercovega kristalnega oscila-

torja, sem predlagano metodo načrtovanja testnih struktur posplošila, tako da je uporabna tudi za druge konfiguracije kristalnih oscilatorjev.

Naslov doktorske disertacije: **Vektorska metoda širjenja snopa na osnovi končnih elementov za numerično analizo elementov integrirane optike**

Avtor: **Edvard Vovk**

Mentor: **prof. dr. Jožko Budin**

Somentor: **prof. dr. Gabrijel Tomšič**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Širjenje elektromagnetnega valovanja skozi dano strukturo analiziramo po metodi širjenja snopa. Pri reševanju parcialnih diferencialnih enačb večina avtorjev uporablja končne diference. V nekaterih primerih so geometrijo prečnega prereza strukture že opisali s končnimi elementi, medtem ko diskretizacija v vzdolžni smeri še vedno temelji na končnih diferencah. Uporaba končnih elementov enake dimenzije, kot je dimenzija obravnavanega prostora, pomeni novost in obogatitev metode širjenja snopa.

V uvodu je podan kratek pregled različnih izvedb metode širjenja snopa, ki predstavljajo izhodišče za izpeljavo nove metode. Prednost nove metode, ki uporablja končne elemente v prečni smeri in tudi v smeri širjenja svetlobe, se kaže v možnosti boljšega prilagajanja geometriji struktur, katerih geometrija prečnega prereza se spreminja vzdolž smeri širjenja svetlobe. S končnimi elementi enake dimenzije, kot je dimenzija obravnavanega prostora, lahko natančno opišemo geometrijo takih struktur.

Sledi izpeljava osnovnih enačb za opis elektromagnetnega valovanja. Predpostavljamo, da je snov linearna, izòtropna, brez izgub. Ima konstantno magnetno permeabilnost $\mu=\mu_0$ in se s časom ne spreminja. Za elektromagnetno polje upoštevamo, da v obravnavanem prostoru ni virov, časovna odvisnost pa je harmonična ($\exp(j\omega t)$) s krožno frekvenco ω. Predpostavljamo počasno spreminjanje amplitude elektromagnetnega polja v smeri koordinate z, tako da lahko zanemarimo drugi odvod po tej koordinati. Izpeljani enačbi (18) in (19) predstavljata skupno izhodišče za vektorsko metodo širjenja snopa na osnovi končnih elementov in vektorsko metodo širjenja snopa na osnovi končnih diferenc, ki služi za primerjavo rezultatov /42/.

Osrednji del predstavlja izpeljava nove metode za analizo 2-dimenzionalnih struktur. Analizirano področje strukture v vsakem koraku analize razdelimo na končne elemente trapezne oblike. Za opis elektromagnetnega polja uporabimo bazne funkcije 1. reda (39). Uporaba končnih elementov daje možnost, da upoštevamo razlike lomnega količnika na področju končnega elementa. Krajevno funkcijo lomnega količnika zapišemo z linearno kombinacijo baznih funkcij, ki smo jih uporabili tudi za opis elektromagnetnega polja.

Pri analitičnem izračunu integralov Galerkinovega postopka uteženih ostankov sprva predpostavljamo, da so vrednosti električnega polja v vseh vozliščnih točkah elementov neznane. Po tej izpeljavi dobimo dvojno število enačb, ki jih potrebujemo za določitev novih vrednosti trenutnega koraka analize. Če ne izberemo pravih enačb za končni sistem enačb, ne dobimo uporabnih rezultatov. Zato je bilo potrebno poiskati pravilo, po katerem sestavimo sistem enačb. Povzamemo ga iz preprostega zgleda širjenja planega vala skozi homogen prostor. Po izpeljanem pravilu seštejemo po dve enačbi, ki pripadata vozliščnima točkama na istem kraku končnega elementa trapezne oblike. Iz izpeljanih enačb postopka uteženih ostankov sestavimo sistem enačb za končne elemente trapezne oblike. Dobimo tridiagonalen sistem enačb, ki ga lahko učinkovito rešimo po direktni metodi.

Poenostavljene enačbe za končne elemente pravokotne oblike lahko primerjamo z enačbami, ki jih dobimo po metodi širjenja snopa z uporabo končnih diferenc. Prispevki drugega parcialnega odvoda po koordinati x so v obeh sistemih enačb enaki. Če bi pri izračunu ostalih prispevkov končnih enačb namesto vrednosti A_y v vozliščni točki (i) uporabili vsoto $1/6A_y(i-1)+4/6A_y(i)+1/6A_y(i+1)$, bi na področjih homogene snovi z $n_{i-1}=n_i$ dobili popolnoma enake enačbe po obeh metodah.

Na robu analiziranega področja postavimo prepustne robne pogoje, ki preprečujejo nefizikalne odboje izhajajočega elektromagnetnega valovanja nazaj v analizirano področje. Enostaven testni problem, z njim preverimo postopek prepustnih robnih pogojev, je širjenje Gaussovega snopa skozi homogen prostor.

Prednosti nove metode širjenja snopa na osnovi končnih elementov pred metodo širjenja snopa, ki temelji na končnih diferencah, prikažemo na zgledu poševnega valovoda. Širjenje elektromagnetnega valovanja po poševno postavljenem valovodu lahko analiziramo, če področje razdelimo na majhno število 2-dimenzionalnih končnih elementov. Če analizirano področje razdelimo z enako gosto mrežo končnih diferenc, ne dobimo uporabnih rezultatov. Izhodno polje, izračunano po novi metodi, se dobro ujema z analitično rešitvijo, medtem ko so odstopanja rezultatov metode širjenja snopa na osnovi končnih diferenc zelo velika.

Rezultati analize zoženega valovoda in Y-spoja so podobni rezultatom v viru /7/, ki so izračunani po Fresnelovi enačbi. Porazdelitev izhodnega polja se dobro ujema tudi z analitično rešitvijo porazdelitve polja osnovnega rodu.

Krivine analiziramo na dva načina: različne dolžine krožnih lokov v odvisnosti od polmera r kompenziramo z ustrezno spremembo lomnega količnika strukture; v vsakem koraku analize zavrtimo koordinatni sistem za kot $\Delta\varphi$. Oba načina obravnave krivin najprej preverimo na analitično rešljivem zgledu. V valjni koordinatni sistem postavimo raven valovod. Odstopanja porazdelitve absolutne vrednosti izhodnega polja od analitične rešitve so majhna, kar potrjuje uporabnost obeh načinov obravnave krivin.

Mikrokrivine lahko analiziramo v kartezičnem koordinatnem sistemu, saj so naključna periodična odstopanja osi valovoda od koordinatne osi z dovolj majhna.

Metoda širjenja snopa na osnovi končnih elementov je primerna za analizo optičnih sklopnikov različnih geometrij. Rezultati analiz simetričnih sklopnikov se

dobro ujemajo z rezultati analitičnih metod in rezultati metode širjenja snopa na osnovi končnih diferenc. Prednosti nove metode širjenja snopa na osnovi končnih elementov pred metodo širjenja snopa na osnovi končnih diferenc pridejo močno do izraza pri analizi nesimetričnih optičnih smernih sklopnikov, katerih geometrija prečnega prereza se spreminja vzdolž smeri širjenja svetlobe. Metoda širjenja snopa na osnovi končnih diferenc potrebuje za primerljivo natančne rezultate kar petkrat več točk v prečnem prerezu.

Nova metoda širjenja snopa na osnovi končnih elementov se je na številnih zgledih pokazala kot stabilna metoda, primerna za analizo struktur, katerih geometrija prečnega prereza se spreminja vzdolž smeri širjenja svetlobe.

Naslov doktorske disertacije: **Zaznavanje prostora z video kamero**

Avtor: **Jure Skvarč**

Mentor: **prof. dr. Peter Šuhel**

Univerza v Ljubljani, Fakulteta za elektrotehniko

Zaznavanje prostora pomeni določanje koordinat točkam v prostoru, glede na izbrani (referenčni) koordinatni sistem. Zaznavanje prostora je ključni element, ki omogoča interakcijo naprave ali živega bitja z okoljem in je pogoj za uspešno navigacijo in gibanje v prostoru. Umetna zaznavala prostora so nepogrešljiva pri rehabilitaciji slepih in slabovidnih, pri robotiki za vodenje robotskega prijemala, pri avtonomnih vozilih za odkrivanje preprek in še bi lahko naštevali. Obstoječi mobilni roboti uporabljajo številna optoelektronska in mehanska zaznavala, s katerimi odkrivajo prepreke na svoji poti. Najpogosteje uporabljajo laserske pregledovalnike prostora, video kamere in ultrazvočna zaznavala. Pri študiji smo se omejili na zaznavala, ki temeljijo na principu stereo vida. Ključni problem stereo vida ni računanje razdalj, temveč iskanje homolognih (istorodnih, istoizvornih) točk. Poiskati je treba preslikavo prostorske točke v slikovno ravnino leve in desne kamere. Problem je zahteven, vendar poznamo več možnih rešitev.

Postopki iskanja homolognih točk so računsko zahtevni. Cilj doktorske disertacije je poiskati algoritem robustne fazne stereo metode, pri kateri bi z uporabo dostopnih sredstev dosegli izvajanje algoritma v dejanskem času. Čas, potreben za izračun rezultatov, je kriterij, ki odloča o uporabni vrednosti postopka.

Pri frekvenčnih (faznih) stereo metodah se originalni signal (slika) najprej pretvori v fazni prostor in nato del transformiranega signala uporabi za računanje točkovnega zamika. Najpogosteje se kot merilo za točkovni zamik uporabi argument (faza) kompleksnih koeficentov faznega prostora. Fazni prostor smo izračunali z zvezno valčkovo transformacijo, ki smo jo vzorčili le pri vrednostih dilacijskega parametra, ki zagotavljajo stabilno fazo. Te vrednosti smo določil z diskretno Fourierovo transformacijo. Predlagana hitra fazna stereo metoda je kombinacija in nadgradnja poznanih delnih rešitev. Dosežena hitrost metode je posledica selektivne izbire vrednosti dilacijskega parametra pri zvezni valčkovi transformaciji in uporabe učinkovitih računskih postopkov.

Predlagani algoritem smo preizkusili na osebnem računalniku in vzporednem računalniku z digitalnimi signalnimi procesorji. Uspešnost algoritma smo preverili s stereoskopskimi pari slik, s poznano referenčno mrežo točkovnih zamikov. Pokazali smo, da lahko v primerjavi s faznimi metodami, ki izkoriščajo celotno fazno polje, čas računanja občutno skrajšamo, in da s tem ne vplivamo bistveno na točnost rezultatov.

S praktično izvedbo algoritma, z upoštevanjem vseh postopkov pohitritve smo demonstrirali izvajanje algoritma v dejanskem času in s tem napravili metodo uporabno.

Naslov doktorske disertacije: **Uporaba akustične resonance v meritvah in detekciji nivoja fluidov**

Avtor: **Denis Đonlagić**

Mentor: **prof. dr. Anton Jeglič**

Univerza v Ljubljani, Fakulteta za elektrotehniko

V mnogih vejah industrije, posebej procesne industrije, je potrebno meriti in zaznavati nivo fluidov. Merilniki nivoja in nivojski detektorji (stikala) so tako nepogrešljivi členi raznolikih tehnoloških procesov. Zelo pogosto imamo opraviti z visoko viskoznimi fluidi, fluidi, katerih viskoznost je odvisna od tehnološkega procesa, fluidi z nedefiniranimi lastnostmi (npr. odpadne vode), kjer je nujna uporaba brezkontaktnih merilnih postopkov. Značilen problem, ki ga srečamo pri procesnih merilnikih nivoja, so različne zamašitve, obloge, pene, itd. Tovrstnih problemov ni možno prebroditi s klasičnimi merilnimi postopki, ki temeljijo na mehanskih, prevodnostnih, ultrazvočnih ali mikrovalovnih principih. Tako je večina današnjih merilnikov in detektorjev nivoja omejena le na določene vrste fluidov in specifične delovne pogoje. V industrijski praksi se pogosto pojavlja dodatna zahteva po popolni električni pasivnosti merilnika, bodisi zaradi zahtev po eksplozijski varnosti ali pa visoki stopnji elektromagnetne imunosti.

Doktorsko delo predstavlja rešitev, ki sloni na uporabi pojava akustične resonance akustičnega valovoda. Akustična resonanca omogoča uporabo relativno dolgih akustičnih valov. Valovna dolžina zvoka je lahko tako celo večja od razdalje med pokrovom merilnika in nivojem fluida. Akustični valovi z relativno veliko valovno dožino se ne odbijajo od ovir, ki so manjše od njihove valovne dolžine. Dodaten pojav, ki prispeva k zmanjšanju občutljivosti na obloge in ovire znotraj resonančnega prostora, je značilna porazdelitev tlačne in hitrostne amplitude znotraj resonatorja. Akustična resonanca ponuja tudi možnost za realizacijo povsem električno pasivnega merilnika nivoja fluidov.

Obravnavane so bile teoretične osnove akustičnih resonatorjev, izvedena je bila ocena dosegljivega razreda točnosti, opravljena je bila analiza možnosti za kompenzacijo determinističnih vplivov (kompenzacija hitrosti zvoka), proučene so bile osnovne omejitve in možnosti za realizacijo merilnikov in detektorja nivoja fluidov.

V okviru doktorske disertacije so bile praktično realizirane naslednje delujoče naprave: akustični resonančni merilnik nivoja fluidov, akustični resonančni detektor nivoja fluidov električno pasivni akustični resonančni merilnik nivoja fluidov.

Realizirana merilnika in detektor so nedvoumno potrdila veliko uporabnost akustične resonance v merilni tehniki.

Cilj realizacije je bil tudi neposreden prikaz možnosti za cenovno učinkovito realizacijo vseh treh naprav. Vse tri izvedbe zahtevajo naprednejši pristop k obdelavi merilnih signalov, ki je bil učinkovito izveden s pomočjo relativno cenenega mikrokrmilnika. V ta namen je bila razvita ustrezna programska oprema. Izdelana programska oprema predstavlja neposredno osnovo za razvoj industrijskih merilnikov in detektorjev.

Za vse tri realizacije je značilna uporaba preprostih, relativno cenenih in lahko dostopnih komponent. S stališča cenovno učinkovite realizacije, je bilo posebej zahtevno načrtovanje in realizacija električno pasivnega merilnika nivoja.

Tako je bila podrobno obdelana možnost za realizacijo električno pasivnega merilnika nivoja ob uporabi mikrofona s Sagnacovim interferometrom v minimalni konfiguraciji. Podrobno je bila proučena tudi možnost za dovajanje akustičnega valovanja v resonator s pomočjo akustičnega valovoda. Akustičen valovod se je izkazal kot učinkovita, cenena in predvsem praktična rešitev.

Realizirana merilnika in detektor so bili osnova za neposredno ovrednotenje uporabnosti akustične resonančne metode ter verifikacijo teoretičnih napovedi in modelov. Eksperimentalni rezultati se dobro ujemajo z teoretičnimi modeli in napovedmi.

Lastnosti realiziranih merilnikov so: realiziran merilnik je neobčutljiv na parazitne odboje, ki so posledica oblog, usedlin, površinske valovitosti fluida, hrapavosti sten resonatorja, itd., dosežena je relativno visoka ločljivost: 0.12%, pogrešek merilnika je manjši od 0.35% v električno aktivni izvedbi ter 0.6% v električno pasivni izvedbi, realizirani merilni sistemi so izjemno robustni.

Naslov doktorske disertacije: **Kompenzacija odmeva po frekvenčnih pasovih pri sistemih avtomatskega telefonskega govornega dialoga**

Avtor: **Andrej Miksić**
Mentor: **prof. dr. Bogomir Horvat**
Somentor: **izr. prof. dr. Zdravko Kačič**
Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

Pri sistemih avtomatskega telefonskega govornega dialoga, kjer želimo zagotoviti možnost uporabnikovega odziva tudi v času sistemskega sporočila (polni - dupleks komunikacija), je za zagotovitev zadovoljive stopnje avtomatskega razpoznavanja govora potrebno kompenzirati vplive odmeva sistemskega sporočila.

Kompenzacija odmeva za potrebe avtomatskega razpoznavanja govora ima določene specifične značilnosti in potrebe. V okviru disertacije smo pokazali, da je pri takih sistemih smotrno uporabiti adaptivno kompenzacijo odmeva po frekvenčnih pasovih. Kompenzacijo smo izvedli v fazi izločanja značilk govornega signala uporabnika. Z razdelitvijo kratkočasovnega Fourierjevega frekvenčnega magnitudnega spektra smo dobili signale frekvenčnih pasov, ki so predstavljali magnitude signalov po melodičnem spektru govora. S tem smo zmanjšali motilni vpliv prekrivanja frekvenčnih komponent dobljenih s hitro Fourierjevo transformacijo in posredno povečali hitrost konvergence adaptivnih filtrov.

Zaradi časovne spremenljivosti impulzne karakteristike poti odmeva je potrebno zagotoviti adaptivno oceno koeficientov kompenzatorja odmeva. Uporabili smo v praksi zelo uveljavljen stohastični gradientni algoritem, pri katerem je bistvenega pomena primerna izbira koraka adaptacije. Večji korak zagotavlja hitrejšo konvergenco adaptivnega filtra, vendar tudi večjo občutljivost sistema na šum in na stanje hkratnega govora. Pomembna je torej hitra in zanesljiva detekcija hkratnega govora in motečega šuma.

Analizirali smo obstoječe metode detektiranja hkratnega govora. Le-te so v večini izpeljane za potrebe prostoročne telefonije in niso povsem primerne za potrebe kompenzacije odmeva pri sistemih govorno krmiljenega telefonskega dialoga. Izpeljali smo časovno funkcijo, ki za detekcijo hkratnega govora uporablja funkcijo napake gradientnega algoritma.

Izpeljali smo tudi enačbo optimalne nastavitve koraka adaptacije, ki tudi med časom hkratnega govora zagotavlja stabilnost kompenzatorja odmeva. Na ta način smo odpravili potrebo po ločenem detektorju hkratnega govora.

Naslov doktorske disertacije: **Modeliranje in sinteza vodenja linearnega asinhronskega motorja**

Avtor: **Ludvik Kumin**
Mentor: **prof. dr. Karel Jezernik**
Somentor: **prof. dr. Drago Dolinar**
Univerza v Mariboru, Fakulteta za elektrotehniko, računalništvo in informatiko

V delu je predstavljena izpeljava dinamičnega modela in sinteza vodenja linearnega asinhronskega motorja. Model je dobljen s pomočjo Lagrangeovega postopka na osnovi magnetne energije, akumulirane v zračni reži motorja in kinetične energije gibljivih delov motorja. Za podano navitje motorja je zapisana tokovna obloga primarja. Uporabljena je bila za reševanje Laplaceove parcialne diferencialne enačbe, s katero so opisane magnetne razmere v zračni reži motorja. Opisan postopek daje kot rešitev osnovno harmonsko komponento jakosti magnetnega polja. Na osnovi dobljenega izraza za jakost magnetnega polja je nato izpeljan izraz za akumulirano magnetno energijo v zračni reži motorja. S pomočjo Lagrange-Eulerjevih enačb je izpeljan dinamični trifazni model linearnega asinhronskega motorja s koncentriranimi parametri. Ta model ni primeren

za sintezo vodenja, zato je najprej opravljena trifazno-dvofazna transformacija, nato pa še dq transformacija modela motorja. Dobljen dq model je nato uporabljen kot osnova za sintezo vodenja. Prikazana je izpeljava dveh regulacijskih struktur: vektorske regulacije in vodenja na osnovi vhodno-izhodne linearizacje modela motorja. Pri slednji je pokazano, da lahko z uporabo sledilnih regulatorjev zagotovimo popolno sledenje (perfect tracking). Ker obe shemi temeljita na dq modelu motorja, je prikazana še izpeljava estimatorja sekundarnega magnetilnega toka, opravljena analiza dinamičnih lastnosti in vpliva spremembe upornosti sekundarja na izračun sekundarnega magnetilnega toka.

Rezultati simulacijskih izračunov vodenja linearnega motorja kažejo, da regulacijska shema na osnovi vhodno-izhodne linearizacije modela motorja zagotavlja popolno sledenje reguliranih veličin referenčnim trajektorijam in boljše dinamične lastnosti pogona kot vektorska regulacija. Na podoben način kot za linearni motor, sta bili izpeljani vektorska regulacija in vodenje na osnovi vhodno-izhodne linearizacije modela motorja tudi za rotacijski asinhronski motor in preizkušeni na laboratorijskem pogonu. Primerjava simulacijskih rezultatov vodenja linearnega in rotacijskega motorja kaže na podobne dinamične lastnosti obeh pogonov. Poleg tega je vidno tudi zelo dobro ujemanje rezultatov simulacijskih izračunov in meritev na rotacijskem motorju.

35th INTERNATIONAL CONFERENCE ON MICROELECTRONICS, DEVICES AND MATERIALS MIDEM'99

and

WORKSHOP on MICROSYSTEMS

CONFERENCE '99

Slovenia Section

Slovenia Chapter

First Announcement and Call for Papers

October 13. - 15. 1999
Ljubljana, SLOVENIA

ORGANIZER

MIDEM - Society for Microelectronics, Electronic Components and Materials

Dunajska 10, 1000 Ljubljana, SLOVENIA

CONFERENCE SPONSORS

- **Ministry of Science and Technology**, Republic of Slovenia
- **IMAPS**, Slovenia Section
- **IEEE**, Slovenia Section

CONFERENCE PROGRAMME COMMITTEE

- Slavko Amon, Faculty of Electrical Engineering, Ljubljana, Slovenia, chairman
- Lojze Trontelj, Faculty of Electrical Engineering, Ljubljana, Slovenia, cochairman
- Marko Hrovat, Jožef Stefan Institute, Ljubljana, Slovenia,
- Dejan Križaj, Faculty of Electrical Engineering, Ljubljana, Slovenia
- Cor Claeys, IMEC and KU Leuven, Belgium
- Gerhard W. Herzog, Technische Universitaet, Graz, Austria
- Bruno Cvikl, Faculty of Civil Engineering, Maribor, Slovenia
- Marija Kosec, Jožef Stefan Institute, Ljubljana, Slovenia
- Miloš Komac, Ministry of Science and Technology, Republic of Slovenia
- Wilhelm Kusian, SIEMENS Corporate R& D Department, Muenchen, Germany
- Peter Panjan, Jožef Stefan Institute, Ljubljana, Slovenia
- Stane Pejovnik, National Institute of Chemistry, Ljubljana, Slovenia
- Wolfgang Pribyl, Austria Mikro Systeme Intl.AG, Graz, Austria
- Nava Setter, Ecole Polytechnique Federal de Lausanne, Lausanne, Switzerland
- Giovanni Soncini, University of Trento, Trento, Italy
- Giorgio Pignatel, University of Trento, Trento, Italy
- Iztok Šorli, MIKROIKS d.o.o., Ljubljana, Slovenia
- Jiri Toušek, Charles University, Prague, Czech Republic
- Anton Zalar, ITPO, Ljubljana, Slovenia
- Miloš Simora, Technical University, Košice, Slovakia
- Leszek J.Golonka, Technical University, Wroclaw, Poland
- Zsolt Vitez, Technical University, Budapest, Hungary
- Monika Jenko, Institute for Metals and Technology, Ljubljana, Slovenia

CONFERENCE ORGANIZING COMMITTEE

- Meta Limpel, MIDEM, Ljubljana, Slovenia,
- Drago Resnik, Faculty of Electrical Engineering, Ljubljana, Slovenia,
- Radko Osredkar, Faculty of Electrical Engineering, Ljubljana, Slovenia
- Iztok Šorli, MIKROIKS d.o.o., Ljubljana, Slovenia

GENERAL INFORMATION

35th International Conference on **Mi**croelectronics, **De**vices and **M**aterials MIDEM'99, continues the tradition of annual international conferences organized by MIDEM Society. These conferences have always attracted a large number of Slovene and foreign experts working in these fields.

Topics covered by the conference are quite diverse, as well as presenting about 60 papers in seven sessions in three days also seems rather demanding. However, once a year scientists and engineers have the opportunity to present their work to the international public and to meet and discuss trends, news and problems related to their field of work. We believe that this at least balances the effort required by the attendees and the organizer.

The conference is very well known in the electronic community. Hundreds of distinguished scientists from all over the world took part in the MIDEM conferences in the past. The goal of establishing contacts, collaboration and friendship among scientists and their companies remains the keystone for the organizer.

Therefore, you are kindly invited to take part in the forthcoming

35th International Conference on Microelectronics, Devices and Materials - MIDEM'99 Conference

The conference will be held at the Faculty of Electrical Engineering, Ljubljana, Slovenia, October 13. – 15.1999

ORIGINAL PAPERS IN THE FOLLOWING AREAS (BUT NOT LIMITED TO) ARE SOLICITED:

- Novel monolithic and hybrid circuit processing techniques
- New device and circuit design
- Process and device modeling
- Semiconductor physics
- Sensors and detectors
- Electromechanical devices
- Microsystems

- Optoelectronics
- Photovoltaic devices
- New electronic materials and applications
- Electronic materials science and technology
- Materials characterization techniques
- Reliability and failure analysis
- Education

Presentation of companies, laboratories and conference sponsors active in the field of microelectronics, electron devices and materials are planned to be held on Thursday, 14.10.99, after the afternoon session.

MIDEM'99 CONFERENCE INVITED PAPERS

The following invited papers will be presented before the related session:

Leszek J.Golonka, Wroclaw University of Technology, Poland

"Application of Thick Films in LCC Technology"

Abstract: Low Temperature Cofiring Ceramics (LTCC) technology gives a possibility of further miniaturisation and improvement of the properties of microelectronics elements. It is very important especially in the case of passive elements. These elements often determine the size of the whole device. Number of thick film materials used in LTCC technology is growing. The properties of these elements are very promising.

The paper presents methods of making fine line thick films in LTCC technology. Moreover, the construction and properties of thick film passive elements and devices made in LTCC technology are shown.

Thick film resistor, thermistor, varistor, inductor and capacitor are described. The results of investigation of buried, cofired and surface resistors are shown. Their properties, possibility of trimming, and a new method of the miniaturisation are presented.

Non conventional utilisation of thick film materials (for example: heaters, physical and chemical sensors) is a new, very interesting and increasing area of their application. The construction and properties of such devices are described in details.

S. Kobe, S. Novak, I. Škulj, P.J. McGuiness, IJS, Ljubljana, Slovenia

"Surface Coating of HDDR Processed and Mechanically Alloyed Powders Based on RE-TM"

Abstract: Chemical surface modification can be used as a method for corrosion protection of sensitive powders based on intermetallic alloys between rare earth and transition metals. Surface coating is used for preventing fine powders, based on Nd-Fe-B, $Sm_2Fe_{17-x}Ta_x$ and $Sm_2Fe_{17-x}Ta_xN_{3-\delta}$ prepared by HDDR processing and mechanically alloying, from hydrolysis. Powders coated by chemisorbed organic substance, after exposing to a humid atmosphere, do not show any chemical or physical change.

Different coating agents were used and the sufficient amount of various materials was optimised with the emphasis on minimising their quantity. Simple experiment shows that the surfactant is successfully chemisorbed on the powder surface and that the coated powders are hydrophobic indefinitely.

Magnetic properties were measured on samples after they were exposed to the same corrosion tests. Measurements on coated and bonded samples were compared with the measurements of non-coated samples. By using Auger electron spectroscopy the thickness of the coating was controlled. In order to distinguish the nature of the bonding between the powder surface and the surface-active substance FT-IR spectroscopy in absorbance and diffuse reflection modes was used.

The protection of the fine particles is based on the formation of a covalent bond between the hydroxyl groups at the particle surface and the surface-active substance. The monomolecular layer of organic substance does not damage the magnetic properties of the powder, but successfully protect the powder against humidity.

Kenway Smith, Glasgow, UK

"Pixel detectors"

Abstract: Recent developments in CMOS processing and in infra-red imaging have provided new read-out options for highly segmented, hybrid semiconductor detectors with pixel dimensions of around 200 microns square which are connected to the matching read-out chip by "flip-chip" bump-bonding techniques. Examples of "typical" silicon and GaAs pixel detector performance are discussed and a number of potential applications described. Potential limitations to even finer segmentation are indicated.

WORKSHOP on MICROSYSTEMS

Starting in 1998, to the programme of the MIDEM Conferences were added workshops, dedicated to each year's selected special topic. In the framework of the workshop, four to six invited speakers present the chosen topics from different aspects, thus offering the audience valuable informations. Time for thorough discussions is provided between invited presentations, and the Conference attendees are encouraged to present their research results in the Conference session dealing with the same topic. For Conference participants, attendance to the workshop is covered in the Conference registration fee with no extra charge. For the year 1999, we are pleased to announce a

Workshop on MICROSYSTEMS

Selected topics associated but not limited to CMOS main stream fabrication technology covering the design, fabrication and testing of different types of MEMS and MOEMS and other structures will be discussed.

Volume production aspects of some microsystems and its future market development will be considered.

The workshop is organized by Laboratory of Microelectronics of the Faculty of Electrical Engineering.

The program committee is announcing the following invited speakers who will give their presentations in the following subjects:

Dr.L. Hermans, Head of Microsystems Department, IMEC, Belgium

"CMOS Technology as a Basis for Micrsystems Fabrication"

Abstract: At IMEC we built for our R&D work in the field of microsystems technology (MST) as much as possible on the know-how and infrastructure available for the development of CMOS process steps, modules and fully integrated processes. Monolithic integration is pursued for mass-produced transducers or for microsystems with large array of sensors or actuators. Today's monolithic devices include visible and IR images, miniature displays, biochemical, pressure, flow and acceleration sensors. The applications of technologies developed for CMOS are not limited to monolithic integration alone. They can also be used to improve the performance of the more classical micromachining technologies. The commercialization of microsystems will certainly benefit from a more intensive usage of the processing capacity and capabilities offered by CMOS foundries.

Dr. Volker Kempe, R&D director, AMS, Austria

"Microsystems at Austria Microsysteme"

Abstract: Production criteria for volume fabrication of microsystems at AMS are described. Special bulk micromachining microtechnologies emerging at AMS are discussed. Mechanical accelerator sensors and their production aspects are shown. The present and future role of custom ASIC foundry in the new evolving field of microsystems is predicted.

Dr. Alexander Lechner, Head of Carinthian Tech Research GmbH, Austria

"The Chances for Microsystems"

Abstract: Microsystem technologies offer new possibilities to increase functionality, utilize cost efficient mass-production technology and thus explore new applications. These technologies combine electronic, mechanical, optical and chemical elements and use several physical effects. Applications can be found in industrial process control, automobiles, medicine, and consumer articles. The multidisciplinary requirements offer chances especially for innovative companies and networks. The presentation gives an overview of technologies and applications with emphasis on some outstanding examples.

Dr.B.Margesin, DrG.Soncini, Dr.G.Verzellesi, Dr.M.Zen, ITC-IRST, Italy

"Silicon Bulk Micromachining for Sensor Technologies"

Abstract: A report on activities in the field of bulk micromachining with TMAH-water solutions for sensor applications in ITC-IRST is given. Full characterization of this anisotropic etching with respect to temperature and concentration is reported. Additives have been tested, allowing for a higher etch rate and aluminum passivation. The optimized etchant formulation has been employed in the development of technological modules for the fabrication of several typologies of sensors. These include piezoresistive pressure sensors, microheaters for metal-oxide based gas sensors, microwave devices, bolometers and filters and dedicated structures for biological applications. These microstructures have been extensively modelled by means of 3D fine element thermo-electro-mechanical simulations.

Dr. Janez Trontelj, University of Ljubljana, Slovenia

"Integrated Magnetic Sensors Design Examples"

Abstract: Various design examples for integrated magnetic sensor ASICs are presented. They include current and energy metering, proximity switches, position and angle measurements and complex two-dimensional magnetic field measurements.

Design approach based on Hall element array is introduced. Sensor properties optimization by design approach is analyzed. Potentials of micromachining sensor element are discussed.

SUBMISSION OF PAPERS

PREPARATION OF ABSTRACTS

An one A4 page abstract is required. It must clearly state what new results have been obtained and what techniques used.

ABSTRACT DEADLINE

Deadline for receiving the abstracts is **May 15th, 1999.**

NOTIFICATION OF ACCEPTANCE:

Deadline for the notification of paper acceptance is **June 20th, 1999.**

DEADLINE FOR RECEIPT OF PAPERS

Deadline for the camera ready manuscript of a paper is **September 20th, 1999.**

PREPARATION OF PAPERS

Papers should be prepared on a maximum of 6 pages in A4 format, camera ready for reproduction in the Conference Proceedings. Invited papers are not limited to 6 pages. Further detailed information will be given in the notification of acceptance.

CONFERENCE PROCEEDINGS

Invited papers and accepted papers will be published in the Conference Proceedings distributed at the Conference registration.

LANGUAGE

The official Conference language is English.

IMPORTANT DATES

Abstract deadline: **May 15th**

Notification of acceptance: **June 20th**

Advance Program: **September 20th**

also on Conference Web page **http://pollux.fer.uni-lj.si/midem/conf99.htm**

Paper deadline: **September 20th**

Final conference program: on registration, **October 13th**

REGISTRATION

The registration fees are as follows:

- MIDEM members who are also employees of MIDEM or Conference sponsors: 200 US$
- MIDEM Society members: 250 US$
- Employees of MIDEM or Conference sponsors : 250 US$
- FULL registration fee: 300 US$

The fee includes Conference Proceedings and free access to all Conference events. A welcome cocktail party will be held on October 13th and the Conference Dinner on October 14th.

Undergraduate students have free access to all Conference sessions on submitting their study papers. For other Conference events there will be an additional charge.

ACCOMMODATION

There are several hotels in Ljubljana where you can find appropriate lodging. A list of the recommended hotels will be distributed to all who register. Please, see also our Web page:

http://pollux.fer.uni-lj.si/midem/conf99.htm

Programme and Organizing Committee, MIDEM'99 Conference

MIDEM at MIKROIKS
Mrs. Meta Limpel
Stegne 11
1521 Ljubljana, SLOVENIA

tel.+386-61-1512 221, fax.+386-61-1512 217

email: Iztok.Sorli@guest.arnes.si

Conference Web page:
http://pollux.fer.uni-lj.si/midem/conf99.htm

Contact person for Workshop on Microsystems:

Prof. Dr. Lojze Trontelj, workshop chairman

Laboratory for Microelectronics, Faculty of Electrical Engineering, University of Ljubljana

Tržaška 25

1000 Ljubljana, Slovenia

tel.+386-61-176 84 90, fax.+386-61-126 46 44

Email: lojze@kalvarija.fe.uni-lj.si

VESTI - NEWS

News from AMS

CHIPS FOR THE CAR OF THE FUTURE

Austria Mikro Systeme and TTTech have set a new technological standard in the field of safety for the next generation of automobiles with their co-developed TIME-TRIGGERED PROTOCOL CONTROLLERCHIP (TTP/C).

In a project which was supported by the European Commission, Austria Mikro Systeme and TTTech together with the "Institut für technische Informatik" at the Technical University Vienna, developed the first semiconductor chip for this new TTP/C.

The desire for increased safety and reliability, as well as increased comfort, has created the need for special kinds of "Electronic Architecture". The process which began ten years ago in the aeroplane industry has been incorporated by today's leading car manufacturers, who are working on the next stage of creating an intelligent and therefore safer vehicle by employing so-called "by-wire" systems.

With a by-wire-system the hydraulic and mechanical connections between individual automobile components are replaced by electrical connections. Each component is linked to the various systems via a central data-bus. As a result, automobile manufacturers gain entirely new dimensions in active safety control through of a continuous exchange of information. For example, should a car swerve in a bend and lose control, this information is passed on almost instantaneously via the data-bus to the stability-controller, which is then activated. When this new system is installed and each component is fitted with a TTP/C Controllerchip, sudden steering problems which, up until now, could have been caused by a mechanical fault beetween the steering and the front axle can, be avoided.

The advantages of this technology have subsequently been recognised beyond the area of leading automotive manufacturers and their suppliers. The incorporation of many "Embedded Systems" is also a feature of air and rail transport as well as of industrial automation techniques. Austria Mikro Systeme and TTTech plan to further expand their leadership in this field through the development of TTP/C Communication Chips to serve these areas.

Delivery of 1.5 Million Slave Chips for AS-Interface®

Austria Mikro Systeme International AG wishes to announce that by January 1999 the delivery of a total of 1.5 million AS-Interface® chips has taken place. This is an outstanding success five years after the availability of the first chip and four years after the actual startup as a complete system, which underlines the unique position of AS-Interface® at the lower level in industrial automation.

The AS-Interface® is based on an unshielded 2-wire-bus for the transmission of information between digital actuators or sensors and a central processor. Up to 31 Slave Chips can be connected at any point to this two-wire communication line, for instance one running through a production hall, thereby replacing a large multi-core cable. Each of these Slave Chips can receive digital signals from up to 4 actuators or sensors and makes these available to a central processor via the bus. The AS-Interface® can be linked to the central processors of various manufacturers and operates below the well-known field busses with which it is not in competition.

The AS-Interface®, having initially been started by 11 competitors as a joint project, has established itself as a European Norm (EN 50295) and as an Industrial Standard and has brought about the creation of more than 500 products by many different manufacturers. AS-Interface® is the simplest way of networking in automation and, as an absolutely open system, has prevented fragmentation into different systems. For the user of the system, AS-Interface® is extremely simple, and its implementation is very flexible and cost-effective. Customers have received the system with great enthusiasm; the application of AS-Interface® has become as much a strategic decision to many of them as it has to the manufacturers.

The commercial organisation AS-International Association markets the AS-Interface® technology world-wide. Today, more than 100 organisations and institutions are involved, among others the large SPS-manufacturers such as Allen Bradley/USA, Bosch/Germany, Crouzet Automatismes/France, Fuji Electric/Japan, Klöckner-Moeller/Germany, Mitsubishi/Japan, Omron/Japan, Groupe Schneider/France, Siemens/Germany, Toyoda/Japan.

News from CMP

0.25 μ CMOS: first projects back from the foundry

STMicroelectronics has just returned the circuits from the first CMP run organised on the 0.25 μ CMOS process.

The first run had collected 7 projects from 7 Institutions: LEPSI from France, LIRMM from France, CERN from Switzerland, ETH IIS from Switzerland, HUT from Finland, DTU from Denmark and Tohoku University from Japan.

Applications addressed by designers were:

- Analog memories
- Amplifier and MOSFETs for characterization
- Analog circuits for RF front-ends

- Test circuit for studying interconnection propagation, inductance effects and capacitances
- Neural network circuit (2.7 million transistors in 11 mm^2)
- RF circuitry using various inductances
- Large MOSes and analog amplifier for noise and radiation characterization

The second run is presently being assembled to go for fabrication, 8 research projects are submitted from France, Denmark, and Switzerland.

The 0.25 μ CMOS process from STMicroelectronics has the following features:

- Gate length (0.25 μ drawn, 0.2 μ effective)
- Shallow trench isolation process
- Up to 6 levels metal layers with fully stackable contacts and vias
- Power supply: 2.5 V
- Threshold voltage: VTN = 0.5 V, VTP = -0.5 V
- I_{on}: TN@2.5 V : 600 μA/μm
- I_{on}: TP@2.5 V : 300 μA/μm

Since it has been announced, about 50 Institutions have been provided with the design rules. This is the most advanced process presently available from MPW to Education Institutes and Research Laboratories worldwide. The process is available for prototyping to Education Institutions and Research Laboratories, on a cooperation basis. No commercial designs are accepted at this stage. It is expected that later on, the process will be available on a commercial basis for small volume production to Education Institutions, Research Laboratories and specified Companies. A 0.18 μ process will then be made available for Education and Research.

WHO IS CMP

Aim

To serve Universities, Research Laboratories and Industry in ICs, MCMs and MEMS fabrication. CMP acts as a broker for a number of technologies, for prototyping and low volume production.

Basic facts

Since 1981, about 270 Institutions from 40 countries have been served, more than 2700 projects have been prototyped through 280 runs, and 27 different technologies have been interfaced

Integrated circuits

- 0.8 μ CMOS DLP/DLM from AMS
- 0.6 μ CMOS DLP/TLM from AMS (high resistive poly)
- 0.35 μ CMOS DLPITLM from AMS (4LM optional)
- 0.8 μ, 0.6 μ BiCMOS DLP/DLM from AMS
- 0.8 μ SiGe from AMS
- 0.25 μ CMOS 6LM from STMicroelectronics
- 0.2 μ GaAs HEMT from PHILIPS (up to 90 GHz).

Pricing for prototyping

(15 samples delivered as a minimum including 5 samples packaged)

AMS	CMOS DLP/DLM	0.8 μ	200 Euro / mm^2
	CMOS DLP/TLM	0.6 μ	270 Euro / mm^2
	CMOS DLP/TLM	0.35 μ	490 Euro / mm^2
	BiCMOS DLP/DLM	0.8 μ	400 Euro / mm^2
	BiCMOS DLP/DLM	0.6 μ	460 Euro / mm^2
	CMOS DLP/DLM	0.8 μ	550 Euro / mm^2
STMicro-electronics	SiGe	0.25 μ	460 Euro / mm^2
PHILIPS	HEMT GaAs	0.2 μ	900 Euro / mm^2

Pricing for low volume production: upon request.

Design kits for IC design: available for most of the processes for:

ALLIANCE	EXEMPLAR	SYNOPSYS
CADENCE	MAGIC	TANNER
COMPASS	MDS	VIEWLOGIC
DOLPHIN	MENTOR GRAPHICS	

Packaging: S0, DIL, FP, COFP, JLCC, PGA and others.

MCM and 3D packaging

MCM-L, MCM-C, MCM-D, MCM-V (3-D packaging).

Pricing for prototyping and low volume production: upon request.

CAD software for IC and MCM design

CADENCE, MENTOR GRAPHICS, TANNER,...

Micro Electro Mechanical Systems (MEMS)

- 0.8 μ CMOS DLP/DLM from AMS, compatible front-side bulk micromachining
- 0.8 μ BiCMOS DLP/DLM from AMS, compatible front-side bulk micromachining
- 0.2 μ GaAs HEMT from PHILIPS, compatible front-side bulk micromachining
- Multi-User MEMS Processes (MUMPs) from MCNC, three-layer polysilicon, surface micromachining
- Diffractive Optical Elements (DOE) from CSEM.

Engineering kits for MEMS design

- Basic kits for AMS and PML for CADENCE, free of charge

- MEMSCAP generic MEMS Engineering Kit, including:
  - behavioral model to layout generator
  - physical layout to 3D solid model translator
  - solid-model to behavioral model translator
- MEMSCAP MCNC CRONOS Foundry Module: Customization of the generic kit for MUMPs, including fully characterized MEMS components: sensors, actuators, building blocks, test structures,...

Pricing for prototyping

(15 samples delivered as a minimum)

AMS	CMOS Bulk Micromachining	0.8 μ	270 Euro / mm^2
	BiCMOS Bulk Micromachining	0.8 μ	470 Euro / mm^2
PHILIPS	HEMT GaAs Bulk Micromachining	0.2 μ	1,020 Euro / mm^2
MCMN	NUMPs		3,900 Euro / mm^2 (fixed size)
CSEM	Diffractive Optical Elements		upon request

Pricing for low volume production: upon request.

News from European Semiconductor, March 1999

Al/Cu 0.15 μm mix

VLSI Technology has introduced 0.15 μm L_{drawn} gate process (VSC11).

Fully contacted metal is 0.46/0.52 μm pitch. Up to five metal layers are used for signal routing. A sixth layer supports signal redistribution for flip-chip applications. At 80% silicon use, there are 7.2m logic gates/cm^2 for five-layer designs. This doubles the density of VSC10 now entering full production.

For high speed, the process uses low-k dielectric and copper on the top two levels. VLSI studies indicate aluminium remains competitive for deeper levels. The company plans to go full copper after VSC11. Internal voltage is 1.5 V with I/Os optimised for 3.3 V with tolerance for 5 V signals. For low-power, internal voltages can be pushed to 1 V.

Two types of logic transistor are available: high performance with a ring oscillator gate delay of 21 ps and standard, low stand-by power with a 26 ps delay. Evaluation design libraries will be available Q1 and production libraries Q3/99. Process prototypes will be ready Q3 and production in Q4.

VLSI Technology is converting its San Antonio fab to 8" wafers, giving reduced costs and the ability to quickly add capacity. VSC11, coupled with the conversion, will have the effect of doubling potential production from this facility with no increase in headcount or floor space. Qualification is planned for Q3 and full production for Q1 2000.

Sub-λ resolution

Argon-argon lasers (126 nm) could be used to extend optical lithography to 50 nm (presumably with "optical enhancement" - i.e. phase-shifted mask and optical proximity correction), according to Nikon Precision Europe's Winfried Meier ("Optical Lithography Extension"), speaking at Olin Microelectronic Materials' 5th Advanced Litho Seminar in Antwerp. That fluorine-fluorine laser lithography (157 nm) is now being seriously discussed after long being seen as "impractical" makes the suggestion intriguing. A possible lens material for Ar_2 is magnesium fluoride (MgF_2).

Closer in time (2005-06) Nikon has plans for 100 nm tools. Japanese companies also have plans for extreme UV through the ASET consortium.

ASM Lithography´s Richard George ("150 nm Lithography and below") described the resolution factors for scanners - due to movement of reticle and wafer. The Rayleigh equation (resolution=$k_1\lambda$/NA) is modified: resolution=$k_1\lambda/NA/(1-\pi^2/2(MSD/resolution)^2)$ MSD is the moving standard deviation.

Graham Pugh, Intel assignee at SEMATECH International, reported the recent proposal to concentrate efforts on EUV and SCALPEL (e-beam) for "Next Generation Lithography" and the state of play with the lithography roadmap. Post-optical technology will not arrive before 2008; 193 nm will be used in production 2001 and 157 nm 2005. For resolution, 130 nm is due 2002, 100 nm 2005 and 70 nm 2007-8. The end of the CMOS road seems to be 45 nm. But executives, not technologists, set the roadmap and Pugh is sceptical about pushing optical litho this far - "some NGL is needed".

The right resist also increases resolution. Bell Labs/Lucent's Frank Houlihan described his efforts in producing a "193 nm single-layer resist based on norbonene-maleic anhydride acrylate derivatives, recent advances". Organic molecules are built to give the right balance between sensitivity dissolution inhibition and adhesion. The photo-acid generator was based on the artificial sweetner sodium cyclamate - a "sweet PAG".

OMM´s own work is concentrated on organic chemically amplified resists, such as acetals. OMM's speakers were Tom Sarubbi ("Low shrinkage DUV resist") and Sanjay Malik ("Design and performance of contaminant-insensitive 248 nm resist"). Tadayoshi Kokubo from the FujiFilm OMM JV in Japan spoke on a "Deep UV positive photoresist for contact hole application with half tone phase-shift masks".

Linard Karklin (Numerical Technologies) showed how feature sizes had descended faster than illumination wavelength ("OPC & PSM for sub Wavelength Designs:

Mask Error Attenuation"). Printing 0.18μm features with 248 nm light would have been viewed as "crazy" just a few years ago. He predicted enhancement techniques (OPC & PSM) would be used in production by four to five companies in the next year.

While some thought mask enhancement was too expensive to be commercial, the possibility was raised that it could push NGL´s entry to beyond the breakdown of CMOS.

* OMM is now Arch Chemicals (p.13).

How to build a million dollar minifab

Leading-edge devices may require billion-dollar fabs, but European entrepreneurs are making power and MEMS devices in minifabs costing millions. Gail Purvis talks to two: Drix and FaSTec.

Drix NV near Antwerp, Belgium is probably unique in Europe. The fab, built by a team of five people, has been custom-designed as a small facility operating efficiently at low volumes with limited staff, but the minifab is suitable for making products such as MOSFET and IGBT power devices, low-density CMOS digital and analogue, high-voltage CMOS as well as sensors and microelectromechanical systems (MEMS).

Drix founder Maarten Rymenans started the business in 1990 as an electronics component distributor. Recognising the niche market for power devices, it was decided to move into wafer processing. To be economically efficient at low-to-medium volumes, Rymenans says that the target was for a minifab with:

- limited investment;
- low overheads;
- low energy and supplies consumption;
- small wafer size;
- small and large wafer batch capability;
- low set up cost for each batch;
- operable by limited numbers of staff.

DESIGN CONSIDERATIONS. Groundbreaking started in early 1995, with the Drix team of five working on building the 235 m^2 facility in the summer. The cleanroom is Class 10 in the wafer processing areas and Class 1000 in the alleys. "We made several conscious choices in building the fab," says Rymenans. "The design was highly compact to save on land and building space. Our air-handling system was designed for maximum energy efficiency and located on top of the cleanroom, shortening airflow loops and conserving space. We chose a 4" wafer line to limit the cost of small runs, and all equipment works in automatic as well as manual mode to allow for small wafer runs." Process resolution is 3.0 μm but the fab is easily upgradeable to 1.0 μm.

"Any equipment that requires expensive maintenance contracts was banned," he adds. "Lithography is g-line, with coating and developing on fab-specific tracks. We created an in-house mask shop. Non ebeam technology allows very cheap mask production at a small expense in yield. It allows a drastic cut in small-run production costs, though its not used for large runs."

Equipment used in Drix's fab

Cleanroom equipment:

- Censor steppers
- Home-adapted tracks using Milipore pumps
- Thermco oxidation and diffusion furnaces
- Varion ion implanter
- Sloan metal deposition unit
- Thermco LPCVD furmace
- Oxford Plasma deposition equipment
- Tegal plasma etching equipment
- Home-made wet benches
- Leitz inspection mieroscopes
- JEOL Scanning Electron Microscope
- Sentech ellipsometer
- Stolz rinser-dryers
- Laflow Reunraumtechnik flow boxes
- Luwa air filters.

Contractors used:

- Lamers Nijmegen for the gas distribution system
- Teblick for the DI-water loop.

All other equipment/plant has been built and installed by Drix.

Wanting low-volume production and low overheads meant that fab construction lasted from mid-1995 to 1997 with equipment installation in the 1997-98 period. "That's a long time for the IC industry" says Rymenans, "but it allowed us to cut costs drastically by not being under time pressure. It also allowed us to fully test all facilites and equipment before use, with some customising of equipment to handle both small and large runs.

Using a mix of new and refurbished equipment, the fab was built and kitted out for a $3m investment and has single-shift capacity of 1,000 wafers per month, fairly easily expandable to 6,000 wpm. Device assembly is subcontracted.

Rymenans is now seeking partnerships to allow Drix to broaden its power device product line as soon as power MOSFET production starts in 1999. Drix then plans to enter the MEMS and sensor markets.

FaSTec's EX-GARAGE SITE HOUSES THIN-FILM FACILITY

When Peter Anastasi, on contract staff with London's King's College X-ray team, set up his company Fabrication Services and Technology (FaSTec) in April 1994 he ran it from his home in Northampton, UK. For the first couple of years FaSTec bought time in other labs to produce ultra-thin films (typically 100 nm thick) used by the synchrotron-based x-ray researchers. Now the membranes are also used in transmission electron

microscopy (TEM) due to their high transmission and in MEMS because of their ability to flex under pressure.

In October 1997 Anastasi acquired a former garage site. "The entire unit is probably only 1,400 ft^2 [140m^2]. We selected it because its low eaves meant it was ideal for hanging a cleanroom" With help from a local builder, Anastasi and his sister, Pandora Rogerson, who runs FaSTec administration, proceeded to self build a clean-room facility; half for wet processing and half for dry work. "It's probably less than 1,000 ft^2 in total," he say "We Teflon-coated the walls, laid the vinyl floors and put up the ceilings, and installed a temperature-controlled clean-air system" It became operational in May '98 at a cost of about 50,000 £.

"We still subcontract out nitride film deposition to foundries but do all wafer patterning and wet/dry etch in-house". Resist spinner and hotplate are supplied by Electronic Micro Systems; Olympus optical inspection microscope and Elga deionised water system are second-hand; a Biorad plasma etcher has been upgraded by fitting MKS MFCs; and metrology is by 20-year-old Applied Materials ellipsometer.

It's an unconventional site. "People still try to pay for petrol at the office," jokes Anastasi who is cheerfully flippant about his "cookery approach to standard chemistry". Even the name FaSTec still attracts the local car racing fraternity hunting for spares. But the undeniable magic to FaSTec's clean-garage-production is that of a rapidly growing turnover: 75% is exported to the US, Japan and Europe.

KOLEDAR PRIREDITEV - CALENDAR OF EVENTS

MARCH

March 9-12, 1999
DESIGN, AUTOMATION AND TEST IN EUROPE,
MUNICH, GERMANY
Contact European Conferences.
Tel: +44131225 2892
Fax: +44131225 2925
e-mail: sue.menzies@ec.u-net.com
web: www.date-conference.com

March 15-18,1999
ADVANCED MATERIALS AND PROCESSES FOR MICROELECTRONICS,
SAN JOSE, CA, USA
First international conference organised by the American Vacuum Society
Covers dielectrics, metallisation, CMP, interconnect integration, silicides, contact and junction technology.
Contact American Vacuum Society
Tel: +1212 248 0200
Fax: +1212 248 0245
e-mail: avsnyc@vacuum.org
web: www.vacuum.org

March 16-18,1999
MICROELECTRONIC TEST STRUCTURES,
GOTEBORG, SWEDEN
Contact Ivan Ring Nielsen.
Tel: +45 38 880 600
Fax: +45 38 880 611
e-mail: technoconsult@technodata.dk
web: www.ee.ed.ac.uk/ICMTS/

March 17,1999
INDUSTRIAL MATERIALS FOR THE 21ST CENTURY: ELECTRONICS AND DISPLAY
EDINBURGH, SCOTLAND, UK
Including a presentation on indium gallium nitride by Dr Shuji Nakamura of Nichia Chemicals.
Contact The Royal Society of Edinburgh.
Tel: +44131240 5000
Fax: +44131240 5024

March 23-25, 1999
EMV 99, DÜSSELDORF
International exhibition with workshops on electromagnetic compatibility (EMC).
Includes "EMC on Chiplevel".
Contact MESAGO.
Tel: +49 711 61946 49
Fax: +49 71161946 90
e-mail: dunja@mesago.de
web: www.mesago.de

March 30-April 1, 1999
DESIGN, TEST AND MICROFABRICATION OF MEMS/MOEMS,
PARIS, FRANCE
Contact Bernard Courtois, TIMA.
Tel: +33 4 76 57 4615
Fax: +33 4 76 47 3814
e-mail: Bernard.Courtois@imag.fr

APRIL

April 12-16, 1999
SEMICON EUROPA,
MUNICH,GERMANY
Includes conferences (Cleanroom. . .),
seminars (SECS and GEM, Silane Safety. . .),
exhibition. . .
Contact Beatrix Doser, SEMI Europe Tel: +32 2 289 64 93 Fax: +32 2 51143 45
e-mail: bdoser@semi.org
web: www.semi.org

April 13-15, 1999
NEPCON UK, BIRMINGHAM
Includes Electronic Design Solutions and
Euro-EMC events.
Contact Moira Edwards, Reed Exhibitions
Tel: +44181910 7831
Fax: +44181334 0567
e-mail: moira.edwards@reedexpo.co.uk
web: www.nepcon.co.uk

April 13-14, 1999
VACUUM APPLICATIONS EXPO 99,
SALFORD, MANCHESTER
Technical conference on thin films, coatings and surfaces.
Contact Siobhan Wood, Institute of Phyics
Tel: +44171470 4930
Fax: +44171470 4931
e-mail: exhibitions@iop.org
web: www.iop.org

April 18-20, 1999
RUSSIAN ELECTRONICS 99,
MOSGOW Seventh East-West Electronics Forum
Contact Future Horizons
Tel: +441732 762896
Fax: +441732 763914
e-mail: mail@future-horizons.net
web: www.fixture-horizons.net

April 20-22, 1999
EXPO ELECTRONICA 99, MOSCOW
Second international trade fair for the electronic components and production equipment industry.
Contact ITE King's House
Tel: +441787 372345
Fax: +441787 372275
e-mail: info@ite-king.co.uk
web: www.expo-web.net/elec

April 26-27, 1999
MICRO ENGINEERING AND NANOTECHNOLOGY LONDON, UK
Current and near future commercial and industrial applications (ten years and beyond)
Aims to facilitate technology transfer from academia and R&D.
Contact Tanja Raaste, Access Conferences.
Tel: +44171463 2112
Fax: +44171793 4047
e-mail: look@access-conf com
web: www.access-conf com

MAY

May 4-6, 1999
SYSTEM fNTEGRATION IN MICRO ELECTRONICS, NUREMBERG
Includes sessions on packaging roadmap, BG design and assembly flip-chip. etc.
Contact MESAGO
Tel: +49 711619 46 0
Fax: +49 711619 46 90
e-mail: smt@mesago.de
web: www.mesago.de

May 6,1999
UK MICROSYSTEMS TECHNOLOGY CONFERENCE,
RUTHERFORD APPL.ETON
LABORATORY OXFORDSHIRE, UK
Based on nine-month survey of R&D in microsystems technology to give comprehensive picture of UK activities.
Contact David Topham, UKMSTS
Tel: +4418907 81663
Fax: +4418907 81667
e-mail: dt@artscience.scotborders.co.uk
web: www.summit.rl.ac.uk

May 17-23,1999
SIXTH SEMI GIS EXEGUTIVE MISSION AND EXHIBIT, ZELENOGRAD, RUSSIA
Includes market seminars, symposiums, tours.
Contact Alla Famitskaya, SEMI Moscow
Tel: +7 502 224 5847
Fax: +7 502 224 5848
e-mail: semimoscow@semi.org
web: www.semi.org