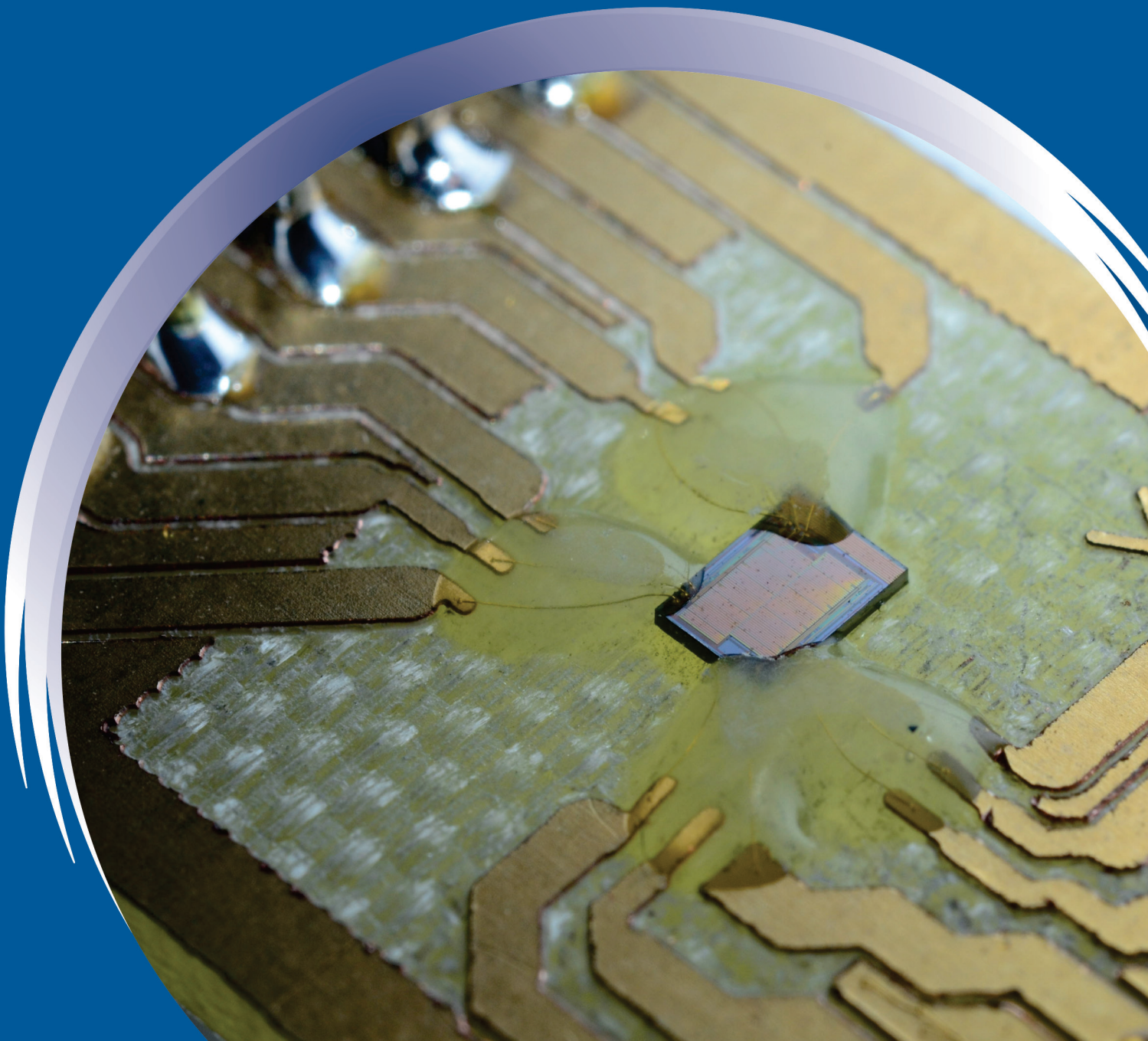
ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 46, No. 1(2016), March 2016

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 46, številka 1(2016), Marec 2016



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *1-2016*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 46, NO. 1(157), LJUBLJANA, MARCH 2016 | LETNIK 46, NO. 1(157), LJUBLJANA, MAREC 2016

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.
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Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 46, No. 1(2016)

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Editorial | Uvodnik

Dear Reader,

This issue brings seven original scientific papers. Among them are the first few which were submitted through the on-line submission platform based on Open Journal System. We started with the on-line submission on 1st Jan 2016. Based on the first three month statistics with over 70 submissions we proudly report that the on-line system works well. We expect that the system will enable faster review times and higher satisfaction by authors.

This issue also bring the Call for paper at the 52nd MIDEM conference that the MIDEM Society organizes in Slovenia in late September every year. The conference will be organized in a picturesque hotel at the Adriatic seaside in the vicinity of town Koper. A highlight of the conference will be the Workshop on Biosensors and Microfluidics. The organizers invite you to join them at the inspiring invited talks and full three-day programme. Readers of the journal will get a chance to read selected papers from the conference in Issue 4 in December.

Page charges for papers published in the journal that were introduced in 2015 to cover publishing costs and to secure continuation of quality growth have been accepted with understanding. We noticed no decrease in submission rate. Implementing European open science / open access policy we will continue to provide a free electronic access to all papers published in *Informacije MIDEM* –Journal of Microelectronics, Electronics Components and Materials (since 1986).

We look forward to receiving your next manuscript(s) in our on-line submission platform:
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Enjoy reading the Issue 1/2016!

Prof. Marko Topič
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Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 1(2016), 3 – 12

Exploration and optimization of a homogeneous Mesh of Clusters-based FPGA architectures

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Abstract: This paper presents an efficient interconnect network for Mesh of Clusters (MoC) Field-Programmable Gate Array (FPGA) architecture. Compared to conventional MoC-based FPGA, proposed architecture improves the MoC-based interconnect in 2 ways. First, we optimize the intra-cluster interconnect topology by depopulating the intra-cluster full crossbar. Then, we propose a new multi-levels interconnect for the Switch Box (SB) which unifies a downward and an upward unidirectional networks based on the Butterfly-Fat-Tree (BFT) topology. The comparison with the common MoC-based VPR-Style shows that the proposed MoC-based architecture has better area and power efficiency. To optimize the interconnect flexibility of the proposed MoC-based FPGA, we explored and analysed the effect of different architecture parameters on performance, power consumption and density. Experimental results show that architecture parameters can be tuned and adapted to satisfy different specific applicative constraints. Results also show that cluster size 8 presents the best trade-off.

Keywords: FPGA; Mesh of Clusters FPGA architecture; Computer Aided Design (CAD) tools; Power estimation; Power analysis.

Raziskava in optimizacija homogene mreže FPGA arhitekture na osnovi grozda

Izvleček: Članek opisuje učinkovito povezovalno omrežje za mrežo grozdov FPGA arhitekture. Predlagana rešitev, glede na klasično FPGA strukturo na osnovi MoC, izboljšuje povezovanje na dva načina. Najprej, z razseljevanjem povezav, optimiziramo povezovanje med grozdi. Nato predlagamo novo večnivojsko Switch Box povezovanje, ki poenoti enosmerna omrežja na osnovi Butterfly-Fat-Tree (BFT) topologije. Predlagana topologija izkazuje boljšo izrabo prostora in izkoristek. Za optimizacijo povezav smo analizirali vpliv različnih arhitekturnih parametrov na učinkovitost, porabo in gostoto. Rezultati so pokazali učinkovito nastavljanje arhitekturnih parametrov za različne specifične aplikacije, pri čemer najboljšo rešitev predstavlja grozd velikosti 8.

Ključne besede: FPGA; mreža grozdov FPGA arhitekture; CAD; analiza moči; ocena moči

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1 Introduction

Compared to full custom ASIC design, FPGAs have become one of most attractive platforms since they enable a fast emulation of design alternatives and lead to a faster design cycle. However compared to ASIC, FPGA architectures are still facing serious challenges in term of performance, power and area due to their high programming overhead. To provide the required reconfigurable functionality, homogeneous FPGAs provide a large amount of programmable interconnect resources which occupy 90% of the total FPGA area [1]. Since FPGA area denotes one of main factors which control the manufacturing costs, reducing the silicon area of the programmable routing resources can lead to considerable improvement in manufacturing cost. In addition, FPGAs devices include a large number of prefabricated routing tracks and programmable switches allowing to route different placement solutions. These tracks can be long and consequently dissipate an important amount of energy every time they switch. Furthermore, the capacitance of programmable switches attached to each track is added which further increases

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FPGA power consumption. Consequently, power consumption is becoming a major concern for FPGA vendors and customers. FPGA design big challenge is to find a good trade-off between flexibility and performance in terms of power consumption, area and delay.

2 Motivation and problem formulation

Modern Mesh FPGA architectures are based on a clustered architecture where several Look-Up-Tables (LUTs) are grouped together to act as a Configurable Logic Block (CLB). Experiments show that using these architectures allows exploiting signal sharing among LUTs and then improving overall performance of the FPGA [2]. The best characterization to date which reliably estimates interconnect requirements is Rent's Rule [3]. Rent's rule can be applied as follows to MoC-based cluster architecture: $IO = c*k^p$ where IO is the number of inputs/outputs of the cluster, c is the number of inputs/outputs of a Logic Block (LB), k is the cluster arity and p is the Rent's parameter. Intuitively, p quantifies the locality of interconnect requirements. It has small value when most connections are purely local and only few of them come in from the exterior of the cluster. We can distinguish two families of MoC-based FPGAs [4,5,6]: fully populated and depopulation intra-cluster crossbar. A VPR-style interconnect [4] has a sparsely populated Connection Block (CB) and a fully populated intra-cluster crossbar with low Rent's parameter. The fully populated intra-cluster crossbar is simple and ensures a complete local routability, but it takes no advantage of the logical equivalency of LUT inputs and induces a significant area overhead. An improved VPR-style interconnect was proposed by Lemieux and Lewis [5] by depopulating the intra-cluster crossbar. This depopulation achieves an area saving of 18%. However, all these studies consider the CB interconnect level and the intra-cluster crossbar separately. An improved VPR-style topology was proposed by Feng [6]. He investigated joint optimization of CBs and intra-cluster crossbars depopulation while using a high Rent's parameter (p = 1). He achieved an area saving of 28%. However, he optimized only connection of external signals to LB inputs and kept the use of a full crossbar to connect feedbacks (LB outputs) to LB inputs, which can be very penalizing. In addition, he did not experiment neither new Switch Boxes (SBs) topologies nor lower clusters Rent's parameter.

In this paper, we propose an improved MoC-based architecture with new hierarchical SB and depopulated intra-cluster interconnect based on the Butterfly-Fat-Tree (BFT) topology with flexible Rent's parameter. Based on analytical method, we identified architecture parameters that control the interconnect flexibility of the proposed MoC-based FPGA. Then, we explored how theses parameters interact in order to balance different trade-offs and satisfy application constraints. A set of CAD tools including metric model to map circuits on the proposed architecture is developed to explore efficiency in terms of power consumption, area and delay. The remaining of this paper is organized as follows. Section 3 presents the proposed MoC-based FPGA architecture. Section 4 presents the used exploration methodology. Section 5 details the experimentation platform and used metric model to estimate power consumption, area and delay. Experimental results are discussed in sections 6 and 7.

3 Proposed MoC-based FPGA architecture overview

Inspired from the Tree topology [7], we propose an improved MoC-based architecture with new hierarchical SBs and depopulated intra-cluster interconnect. This architecture is a mesh of clusters placed into regular 2D grid.

3.1 Cluster architecture

The cluster architecture contains local LBs connected with a depopulated local switch block. Figures 1.a and 1.b illustrate an example of cluster with respectively 8 and 4 LBs. Each LB consists of a 4-input LUT and a Flip-Flop (FF). The depopulated local switch block is divided into Mini Switch Blocks (MSBs). The local interconnect is composed of a downward network and an upward network. The downward network is based on the BFT topology which connects Downward MSBs (DMSBs) outputs to LBs inputs. Each DMSB connects each LB in only one input and hence the number of DMSB is given by equation (1) and the number of DMSB outputs is given by equation (2). The upward network connects LB outputs to an Upward MSB (UMSB) and allows all LBs outputs to reach all DMSBs and cluster outputs. Thus, LBs inside the same cluster are equivalent and their ordering has no impact on routing quality. The number of DMSB inputs is given by equation (3). The number of UMSB inputs and outputs are given respectively by equation (4) and equation (5).

$$Nb\_DMSB(CLB) = Nb\_inputs(LB) \quad (1)$$

$$Nb\_DMSB\_outputs(CLB) = Cluster\_size \quad (2)$$

$$Nb\_DMSB\_inputs(CLB) = \frac{Nb\_inputs(CLB) + Nb\_UMSB\_outputs(CLB)}{Nb\_DMSB(CLB)} \quad (3)$$

$$Nb\_UMSB\_inputs(CLB) = Cluster\_size \quad (4)$$

$$Nb\_UMSB\_outputs(CLB) = Cluster\_size \quad (5)$$

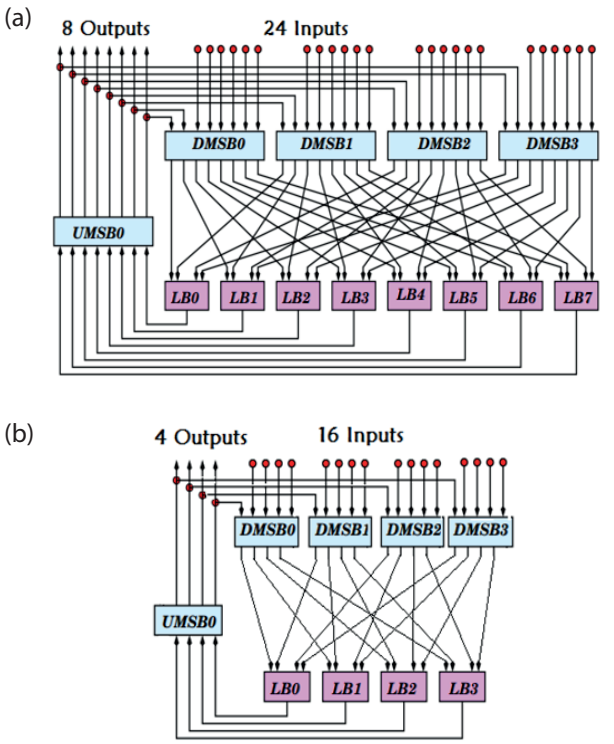

Figure 1: Cluster interconnect with different arity factors. a. Cluster arity 8 (Rent's parameter = 1 and Clusters Inputs = 24). b. Cluster arity 4 (Rent's parameter = 1 and Clusters Inputs = 16).

3.2 Mesh routing interconnect

Mesh routing interconnect of basic VPR MoC-based FPGA architectures use SBs and CBs to assure different interconnections. In fact, SBs are used to assure connection between horizontal and vertical adjacent routing channels and CBs are used to connect channel tracks to cluster inputs and outputs. In the proposed mesh routing interconnect, a new multi-levels interconnect of the SB is proposed to assure connection between horizontal and vertical adjacent routing channels and also between clusters inputs/outputs and adjacent routing channels. As illustrated in Figure 2, each cluster is surrounded by 4 unidirectional routing channels and 4 SBs. Each cluster is connected to 8 neighbouring clusters through adjacent SBs. Figure 3 shows a detailed view of the interconnect of a SB and a global view of the 4 adjacent SBs (Top, Bottom, Right, Left) and the 4 adjacent clusters (A, B, C, D) highlighted in Figure 2. Similarly to cluster, the SB has a multilevel topology including 3 main Boxes organized as follows:

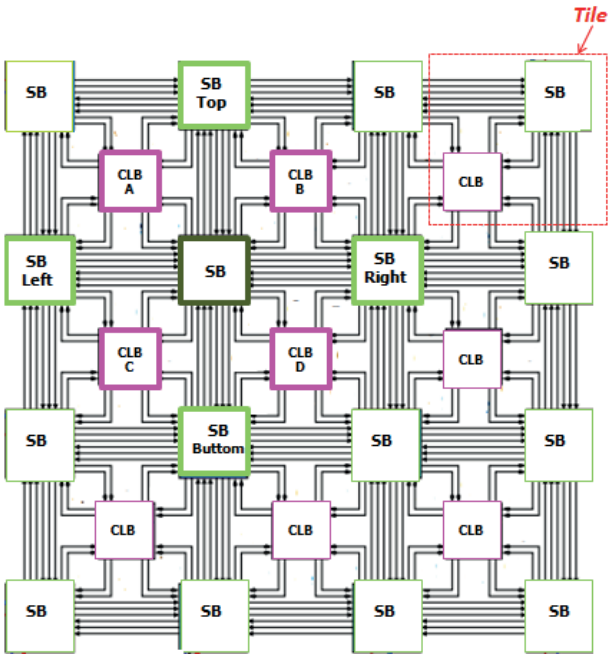

Figure 2: MoC-based FPGA architecture: Unidirectional interconnect.

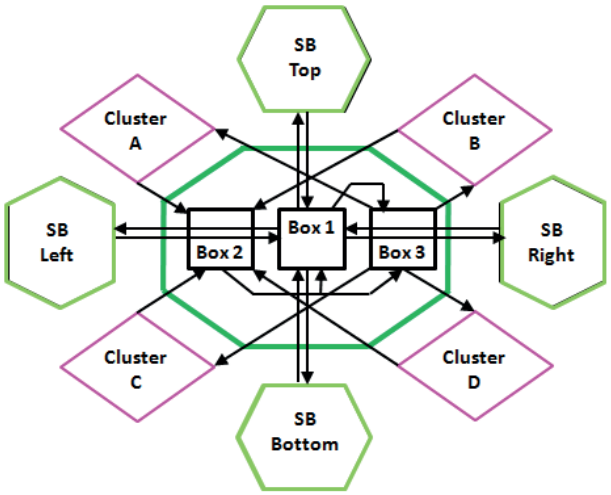

Figure 3: Multilevel SB interconnect.

SB to SB: Each SB is connected to the 4 adjacent SBs using global wires through Box 1. Box 1 is composed of MSB each one drives only one track in each 4 neighbouring channels. This topology is similar to VPR disjoint SB [4]. The number of MSB in Box 1 is given by equation (6):

$$Nb\_MSB(Box\_1) = \frac{Channel\_width}{2} \quad (6)$$

SB to Cluster: Each SB is connected to the 4 neighbouring clusters through 2 interconnect levels. Outputs of MSB located at Box 1 drive MSB located at Box 3 whose outputs drive 1 input of each of the 4 neighbouring clusters. Since the cluster is connected to the 4 neigh-

bouring SBs, the number of MSB located at Box 3 is given by equation (7).

$$Nb\_MSB(Box\_3) = \frac{Nb\_inputs(CLB)}{4} \quad (7)$$

The number of outputs per MSB in Box 3 is given equation (8):

$$Nb\_MSB\_ouputs(Box\_3) = 4 \quad (8)$$

The number of MSB outputs in Box 1 is given by equation (9):

$$Nb\_MSB\_ouputs(Box\_1) = 1 + Nb\_ajd\_SBs = 5 \quad (9)$$

Cluster to Cluster: Each cluster is connected to the neighbouring clusters through 2 interconnect levels. Cluster outputs drive MSB located at Box 2 whose outputs drive MSB located at Box 3. Since the cluster is connected to the 4 neighbouring SBs, the number of MSB located at Box 2 is given by equation (10):

$$Nb\_MSB(Box\_2) = \frac{Nb\_outputs(CLB)}{4} \quad (10)$$

The number of inputs per MSB in Box 2 is given equation (11):

$$Nb\_MSB\_inputs(Box\_2) = 4 \quad (11)$$

The number of inputs per MSB in Box 3 is given equation (12):

$$Nb\_MSB\_inputs(Box\_3) = \frac{2 * Channel\_width}{Nb\_inputs(CLB)} \quad (12)$$

Cluster to SB: Outputs of MSB located at Box 2 drive MSB located at Box 1 whose outputs drive 1 input of each of the 4 neighbouring SBs. Therefore, cluster outputs which drive Box 2 are connected to 4 neighbouring SBs through 2 interconnect levels. The number of outputs per MSB in Box 2 is given by equation (13).

$$Nb\_MSB\_outputs(Box\_2) = \frac{2 * Channel\_width}{Nb\_outputs(CLB)} \quad (13)$$

The number of inputs per MSB in Box 1 is given by equations (14).

$$Nb\_MSB\_inputs(Box\_1) = 1 + Nb\_ajd\_SBs = 5 \quad (14)$$

3.3 Clock network

The clock network is modelled as H-Tree distribution network, similar to the topology used in Xilinx Virtex II Pro [8]. The clock network contains buffers separated by a distance equal to the size of a tile (cluster and SB) in the FPGA (see Figure 2).

4 Exploration methodologies

4.1 Analytical model

To identify architecture parameters that control the flexibility of proposed MoC-based FPGA, we evaluate switches requirement. We consider a MoC arranged in a N x N array with k cluster size and W channel width. The total switch number in the MoC-based FPGA is given by equation (15):

$$Nb\_switch = Nb\_switch(SB) * (N+1)^2 + Nb\_switch(CLB) * N \quad (15)$$

Since MSBs are full crossbar, the number of switch per SB is given by equation (16):

$$Nb\_switch(SB) = \sum_{i=1}^{i=3} Nb\_switch(Box\_i) = 16 * W \quad (16)$$

The number of switch per CLB is given by equation (17):

$$Nb\_switch(CLB) = Nb\_switch(DMSBs) + Nb\_switch(UMSB) \quad (17)$$

Since DMSBs and UMSB are full crossbar, the number of switch in DMSBs and UMSB are given respectively by equation (18) and equation (19):

$$Nb\_switch(DMSBs) = Nb\_inputs(CLB) * k + k \quad (18)$$

$$Nb\_switch(UMSB) = k^2 \quad (19)$$

Based on Rent's rule, we have: Nb_inputs (CLB) + Nb_outputs (CLB) = $c*k^p$. Where c is the number of inputs/outputs of a LB and p is the Rent's parameter. As Nb_outputs (CLB) = k, the number of CLB inputs can be modeled by equation (20):

$$Nb\_inputs(CLB) = c * k^P - k \quad (20)$$

As consequence, the total number of switch in the FPGA can be modeled with the equation (21):

$$Nb\_switch = 16 * W * (N+1)^2 + (c * k^{p+1} + k) * N^2 \quad (21)$$

As illustrated in equation (21), the interconnect flexibility of the proposed MoC-based FPGA is controlled by the following architecture parameters: Rent's parameter (p), cluster size (k), channel width (W), LB inputs/outputs (c) and matrix size (N). Rent's parameter and cluster size control local clusters interconnect whereas channel width controls external clusters interconnect.

4.2 Experimental comparison

Rent's rule provides an empirical estimation of switching requirements. Nevertheless, this is not sufficient

since it does not give accurate information about interconnect routability. The best way to verify this point is to implement different benchmark circuits with CAD tools and explore the effect of architecture parameters described in equation (21) on performance. Performance of each solution is evaluated in terms of power consumption, required area and clock frequency.

5 Design and implementation methodology and metric models

We investigate the CAD flow illustrated in Figure 4 to explore proposed architecture. First, the circuit passes though T-VPack tool [9] to achieve the packing phase which consists in grouping N LBs together to form CLBs. Once packing is completed, we use the simulated annealing algorithm [4] to place the CLBs and IOs instances of the circuit on the CLBs and IOs blocks of FPGA. Then, we use the PathFinder [10] to successfully route all nets in a circuit. In our approach, we determine the minimum number of the channel width (Wmin) that routes the circuit, we decrease continuously the tracks number per channel and route the circuit until it fails. Once the Wmin is determined and routing phase is achieved, we estimate resulting power consumption, area and delay with developed models.

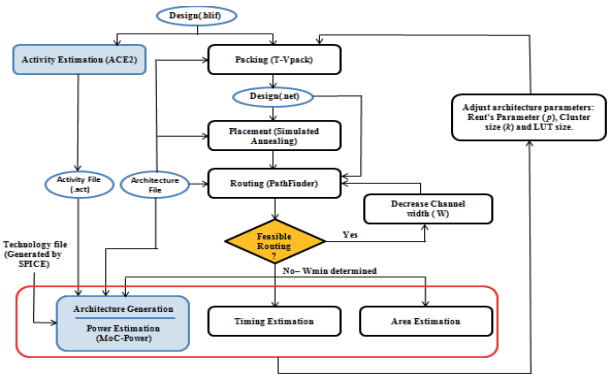

Figure 4: Proposed MoC CAD flow.

To estimate power consumption, we integrated in the proposed CAD flow activity estimator ACE2 and MoC-Power modules. The first module, the activity estimator (ACE2) [11], employs a transition density method to determine the switching density of all nets. The second module, the MoC-Power, estimates the power consumption at transistor level. It incorporates two components: architecture generator and Low-Level Power Estimation. The architecture generator uses the routing resource graph to decompose the entire MoC-based FGPA circuit into low-level components which are inverters, multiplexers and wires using same assumptions of VersaPower model [12]. Then, the Low-Level dynamic and static powers of each component is estimated as defined in [12].

Used area model is based on transistor-counting function consistent with the methodology used in [12] to compute components area. We use routing graph resource to parse all FPGA components (MSBs, LBs and buffers) to accurately compute the total number of transistor in the FPGA. The area is expressed as function of λ which is equal to the half of the minimum distance between source and drain of transistor.

Timing analysis allows evaluating performances of a circuit implemented on a FPGA in term of functional speed. The length of local wires is determined by approximating the size of entities through transistor-counting functions. In addition, proposed model accounts also the effect of the resulting LUT delay as a function of the LUT size to be consistent with experimentation done in [2]. Wire LUT and switch (crossbar, multiplexer) delays are extracted from the SPICE circuit simulator using ST Micros 130nm Technology node.

6 Comparison with basic VPR MoC-based FPGA architectures

In this section, we perform detailed exploration comparison between basic VPR and proposed MoC-based FPGA architectures. In this experimentation, we used largest MCNC [13] and IWLS [14] benchmarks presented in Table 1. The size of these circuits ranges from 1064 to 10437 primitives (LBs, FFs etc). We used VPR7.0 [15] and proposed MoC configuration CAD tools while using same packing options and same place and route algorithms. For both architectures, we determined the smallest architecture implementing every benchmark circuit and we considered homogeneous architecture with $k = 8$, LUT size 4, unidirectional routing network with single length segments and a disjoint switch block. VPR cluster architecture contains 18 inputs and 8 outputs to achieve full logic connectivity [4] and CB population is defined by Fcin and Fcout parameters, where Fcin is routing channel to cluster input switch density and Fcout is cluster output to routing channel density. Fcin and Fcout are chosen equal to respectively 0.5 and 0.25 to be consistent with work presented in [2]. For the proposed MoC-based FPGA, the cluster architecture contains 32 inputs (p=1). Table 1 illustrates comparison results in term of power, area, critical path delay, Wmin and total buffer used to drive global wires. Table 1 shows that the proposed MoC-based architecture can implement all circuits with lower Wmin than VPR architecture. In fact, the maximal Wmin used is equal to 86 and 56 in respectively the VPR and the pro-

posed MoC-based architecture. This induces an average reduction of 24% in total buffer used to drive global wires. Most of the power and area savings (respectively 30% and 32%) obtained in the proposed MoC-based FPGA are due to the reduction in total buffer number. We also note that the power and area gains are achieved at the cost of an increase in critical path delay by an average of 6%.

Table 1: Comparison results: VPR and proposed MoC-based FPGA.

Circuit	Primitives	VPR MoC					Proposed MoC					Gain		
		Power nW	Area E+6(λ)^2	Delay ns	Total Buff	W_{min}	Power nW	Area E+6(λ)^2	Delay ns	Total Buff	W_{min}	Power %	Area %	Buff %
Clma	8416	264	2560	31.51	175032	78	170.3	1593	45.56	116688	52	37	38	33
Elliptic	4726	100.8	970	24.93	52624	60	71.2	650	32.18	44528	44	29	33	15
ex1010	4898	142.2	1368	26.95	75400	70	86.95	810	29.85	57600	48	39	41	24
ex5p	1064	36.1	272	13.55	16224	54	26.39	211	15.45	15600	50	27	22	4
Frisk	1397	110.4	1204	24.24	62744	68	72	666	31.86	46552	46	35	45	26
misex3	4575	46.2	352	13.75	18480	50	31	246	15.73	15960	38	33	30	14
Pdc	1930	170.1	1601	30.29	96200	86	96	886	38.63	67200	56	44	45	30
s298	6406	38.3	345	28.62	19584	34	32.41	295	28.65	17408	32	15	14	11
s38417	6447	168.7	1501	22.80	83520	52	109.8	986	26.35	59160	34	35	34	29
s38584	6537	188.9	1479	17.30	87000	50	126.4	1266	19.57	59160	34	33	14	32
USB_ Funct	5293	127.5	1344	41.51	88400	68	102.0	905	20.68	65000	50	20	33	26
B22_C	10437	429	4632	41.51	291648	62	376.3	3179	48.91	206976	44	12	31	29
AVA2	9378	227.9	2406	41.51	160512	76	158.9	1507	42.34	109824	50	30	37	32
AES_ core	8416	243	2293	41.51	142800	60	177.4	1592	49.46	104720	44	27	31	27
Average												30	32	24

7 Architecture optimization

The flexibility of proposed MoC-based FPGA depends on architectures parameters described in equation (21). The effect of these parameters is not predictable and can only be determined by experimentation. In this section, we explore and analyse how theses parameters interact in order to balance different tradeoffs. Results correspond to interconnect area and the average power consumption and delay of MCNC benchmarks using the biggest FPGA array and Wmin which implement all circuits. Benchmarks are packed, placed and routed through the CAD flow with power, delay and area model described in section 5. For all experimentations, wire capacitances were obtained from the ITRS Interconnect Roamap [16]. The used transistor technology is 130nm PTM models [17]. Table 2 illustrates the variation of the FPGA size with k and also the variation of the Wmin and total buffer obtained with k and p. The Wmin and total buffer decrease when we increase p.

Figure 5 shows the variation of the total power consumption with p for different k. For all k values, the power consumption is reduced until we reach a certain p (the break point p=1) from which the increase of p induces an increase in power consumption. In fact, at this point, the reduction of Wmin with the increase of p becomes insufficient to route circuits (see Table 2). We can also see that Wmin remains the same for many p but the architecture area increases. This is due to the increasing number of cluster inputs with p.

Table 2: FPGA size, channel width and total buffer.

Cluster Size ($_k$)	FPGA Size (N^xN)	Channel Width (W_{min}) vs. Rent's parameter ($_p$)						Total Buffer vs. Rent's parameter ($_p$)					
		0.83	0.89	1	1.05	1.09	1.16	0.83	0.89	1	1.05	1.09	1.16
4	49x49	NR	30	30	30	30	30	NR	147000	147000	147000	147000	147000
8	36x36	48	46	44	44	44	44	127872	122544	117216	117216	117216	117216
16	28x28	NR	60	58	58	58	56	NR	97440	94192	94192	94192	90944

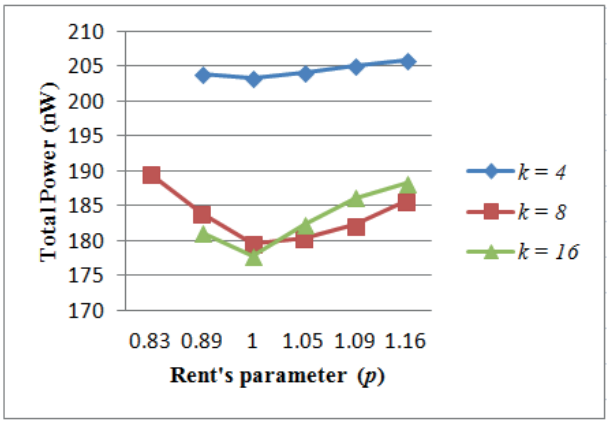

Figure 5: Total power vs. Rent's parameter and cluster size.

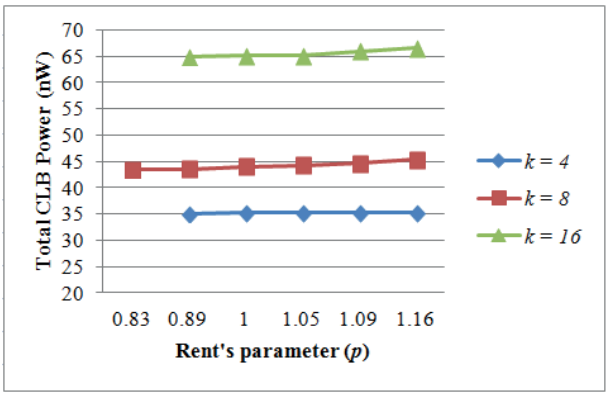

Figure 6: Total CLB power vs. Rent's parameter and cluster size.

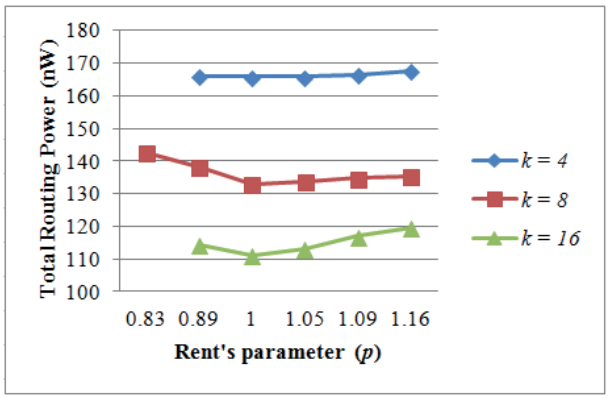

Figure 7: Total routing power vs. Rent's parameter and cluster size.

We notice that the total power consumption is reduced when we increase k. As shown in Figure 5, clusters of size 8 and 16 are more power-efficient than 4. This behaviour is due to the fact that the total number of buffer, used to drive global routing wires, is reduced (see Table 2). In fact, increasing k results in more BLEs being added to a CLB and then circuit can be implemented in smaller FPGA size (see Table 2). In addition, the number of connections routed externally to the CLB is reduced and then the resulting total number of buffer decreases. According to [12], buffers used to drive global routing wires are the major factors behind power dissipation.

To understand why total power consumption of clusters size 8 and 16 are quite close, it is instructive to break out the power components of the data in Figure 5. The total power can be broken into two major parts: the total routing power and CLB powers. Figures 6 and 7 plot respectively the total routing and CLB power with p for different k. By increasing k, we increase CLB multiplexers number to connect LUTs and consequently increase the total CLB power. That is why total CLB power of cluster size 16 is higher than cluster size 8 (see Figure 6). However, with larger k, we can absorb larger number of nets and communication becomes local and then the total number of buffer decreases. Consequently, the total routing power of cluster size 16 is lower than cluster size 8 (see Figure 7). These two opposite effects make the total power of cluster arity 8 and 16 quite close. It is also important to note that with high p, the number of buffer of cluster size 16 increases more rapidly than cluster size 8. Therefore, routing power of cluster size 16 grows more rapidly than cluster size 8 and that is why total power of cluster size 16 becomes higher than cluster size 8 with higher p.

According to results shown in [12], the major source of power dissipation comes from routing resources. This result is also confirmed in our experimentations. In fact, routing power denotes the major factor behind power dissipation in all experimentations done. However, we note that the percentage of routing power drops slightly when we increase k. For example, routing power denotes 80% of the total power for cluster size 4, while it drops to 63% with cluster size 16. Figure 8 plots the variation of the total power of buffers used to

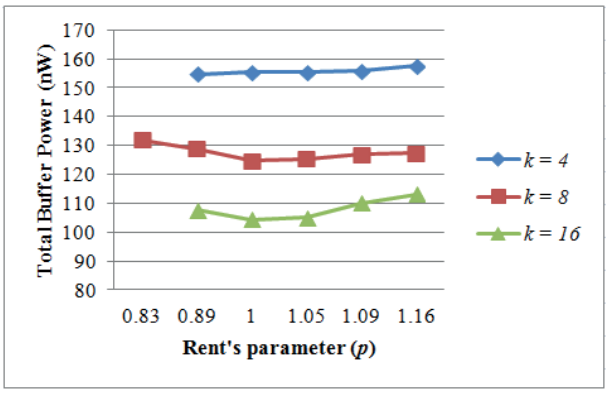

Figure 8: Total buffer power vs. Rent's parameter and cluster size.

drive global routing wires with p for different k. Figure 8 shows that the total buffer power takes up to about 90% of the total routing power. In addition, when we increase k from 8 to 16, the total buffer number is reduced by an average of 20% and then we reduce the total buffer by an average of 17%. All these analyses clearly confirm once again that the number of buffer is the major source of power.

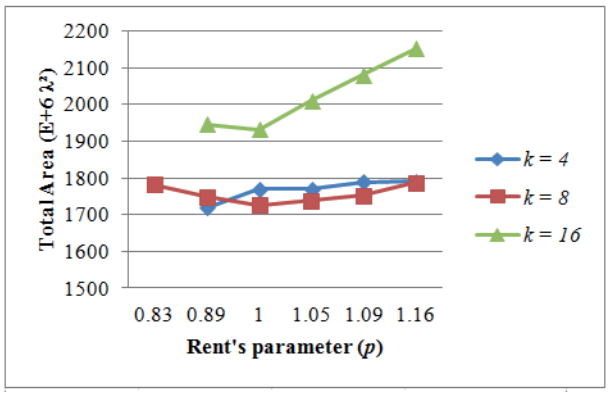

Figure 9: Total area vs. Rent's parameter and cluster size.

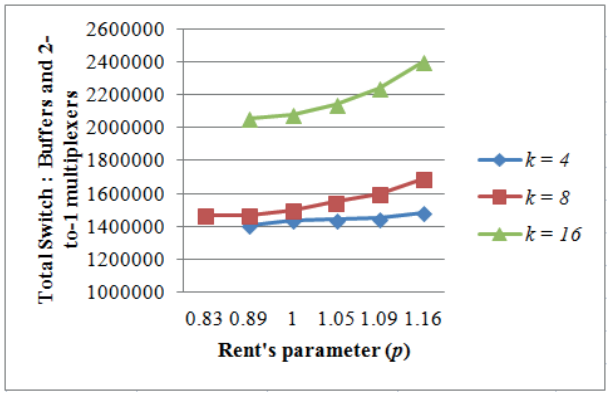

Figure 10: Total switch number vs. Rent's parameter and cluster size.

Figures 9 and 10 illustrate the variation of the total area and number of switch with p for different k. We notice that the total area is increased when we increase k (see Figure 9). Clusters of size 4 and 8 are more area-efficient than 16. In fact, when we increase k, the required multiplexers grow larger and then switches number increases (see Figure 10). Total required switches is a sum of all buffers and 2-to-1 multiplexers used to implement different m-to-1 multiplexers of MSB. Even if the number of buffer decreases with the increase of cluster size, the total number of 2-to-1 multiplexers increases.

To understand why total area of clusters size 4 and 8 are quite close, it is instructive to break out the area components of the data in Figure 9. The total area can be broken into two major parts: the routing area and CLB areas. Figures 11 and 12 plot the total routing and CLB area with p for different cluster size. Since the area depends especially on the number of switch, we extracted also the variation of the total number 2-to-1 multiplexers used in routing and CLB respectively in Figures 13 and 14 with p for different k.

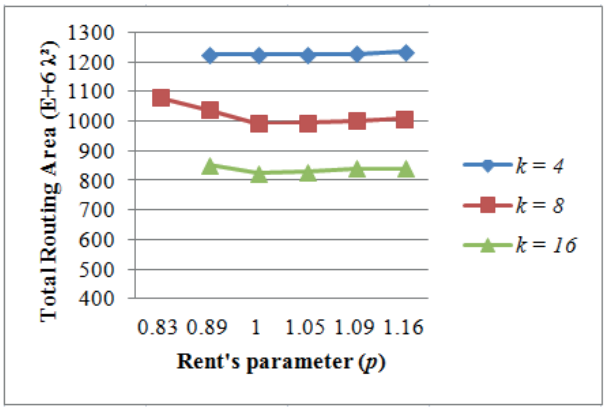

Figure 11: Total routing area vs. Rent's parameter and cluster size.

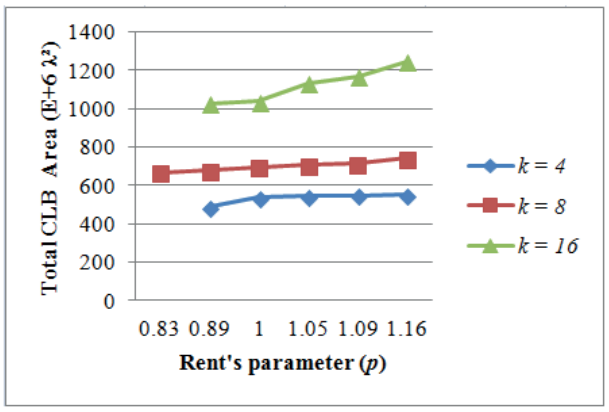

Figure 12: Total CLB area vs. Rent's parameter and cluster size.

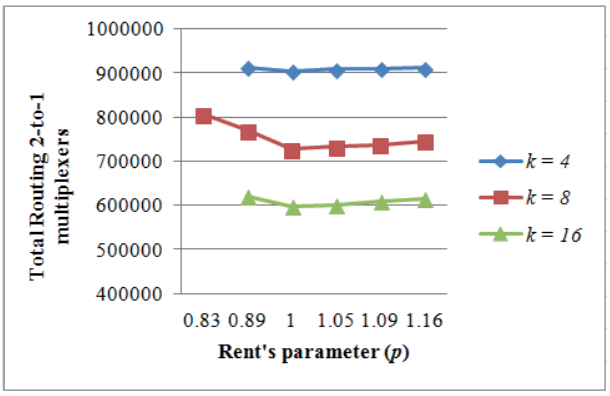

Figure 13: Total routing 2-to-1 multiplexers vs. Rent's parameter and cluster size.

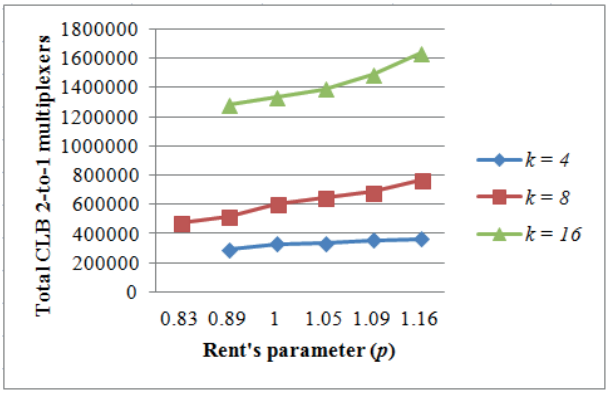

Figure 14: Total CLB 2-to-1 multiplexers vs. Rent's parameter and cluster size.

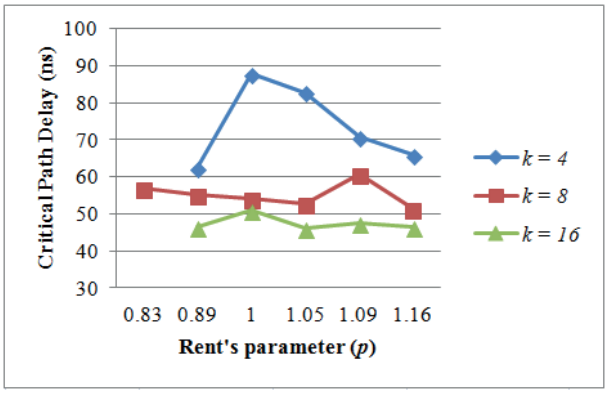

Figure 15: Total critical path delay vs. Rent's parameter and cluster size.

By increasing k, the number of 2-to-1 multiplexers and buffers in SBs decrease (see Figure 13) and then total routing area decreases (see Figure 11). Thus, routing area of cluster size 8 is lower than cluster size 4. However, the required CLB multiplexers grow larger and consequently the bound on area efficiency goes down. As shown in Figure 1, for p=1, in the case of architecture with clusters arity 8, we use 10-to-1 multiplexers within DMSB, 8-to-1 multiplexers within UMSB and 4-to-1 multiplexers to implement LUTs. In total, we use 368 2-to-1 multiplexers to implement the cluster arity 4. With cluster arity 4, we use 5-to-1 multiplexers within DMSB, 4-to-1 multiplexers within UMSB and 4-to-1 multiplexers to implement LUTs. In total, we use 88 2-to-1 multiplexers to implement the cluster arity 8. Therefore, as shown in Figure 14, the total CLB 2-to-1 multiplexers increases when we increase k from 4 to 8 and then total CLB area increases (see Figure 12). These two opposite effects make that clusters 4 and 8 have close resulting number of switch and then total area. Similarly to pervious observations contestations, for all k, the area is reduced until we reach the break point (p=1) from which the increase of p penalizes the resulting area (especially for k=16).

In terms of performance, Figure 15 shows the variation of critical path delay with p for different k. The critical path delay decreases when we increase k. In fact, using larger clusters arity allows reducing external communications and then reduces the number of crossed switch in the critical path delay.

8 Conclusion

In this paper, we presented a new MoC-based FPGA architecture. We showed that the proposed MoC-based architecture has better area and power efficiency than the common MoC VPR-Style. Based on analytical and experimental methods, we showed also that the flexibility of proposed MoC-based architecture is controlled by architecture parameters. The choice of clusters arity must be consistent with the application specifications and constraints. For applications requiring high speed performance and low power dissipation, it is recommended to use clusters with high arity (8-16). If we need to reduce silicon area, using small clusters arities seems to be more efficient. We note from experimentation that cluster size 8 presents the best trade-off between area and power compared to cluster sizes 4 and 16. This is achieved due to the equitable sharing of resource between CLB and routing. As a future work, we plan to add long routing segments which span multiple SBs in every row and column in order to avoid crossing multiple switches to connect clusters, which are not neighbours and to improve the flexibility and routability.

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Arrived: 09. 06. 2015
Accepted: 09. 02. 2016

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 1(2016), 13 – 23

A Ka-band Satellite Beacon Receiver for Propagation Experiment

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Abstract: The design of a low-cost beacon receiver based on software defined radio is presented. The motivation for such a receiver is to investigate atmospheric impairments at the Ka frequency band. The receiver has been tested by the Hotbird 13A, ASTRA 3B and Alphasat satellite beacon signals. A GNU Radio software development toolkit and a USRP device were used for the development of a beacon receiver application. We have tested and validated the beacon receiver operation by the linearity test, by comparing the received signal levels with the corresponding rainfall data, and by comparing the measurement results with the appropriate ITU-R models. The low-cost beacon receiver passed all these tests successfully, confirming that we established a reliable measuring system. After the validation period we were monitoring the measured data on a daily basis, excluding erroneous data and regularly implementing system improvements. The validated data was further processed by a MATLAB tool where statistical analysis is performed. In particular, we developed procedures for attenuation and scintillation analysis as well as procedures for the analysis of second order statistics, corresponding to the fade duration and fade slope distribution. Measurement data processing was performed in three phases, each phase giving predefined output results. These results range from raw propagation data via intermediate propagation data and analysed experimental statistics up to the graphical statistical representation.

Keywords: satellite signal propagation; Ka-band; beacon measurements; software defined radio

Satelitski sprejemnik v Ka frekvenčnem pasu za preizkus razširjanja radijskih valov

Izvleček: V članku je predstavljen načrt nizko cenovnega sprejemnika satelitskega svetilniškega signala na osnovi programirljivega radia. Sprejemnik je namenjen raziskavam vpliva vremena na sprejem signala v Ka frekvenčnem pasu. Testirali smo ga s signali iz satelitov Hotbird 13A, ASTRA 3B in Alphasat. Pri razvoju sprejemnika smo uporabili programsko razvojno orodje GNU Radio in USRP napravo. Delovanje sprejemnika smo preizkusili in ocenili s pomočjo testa linearnosti. Nivo satelitskega signala smo primerjali z ustreznimi podatki o padavinah, poleg tega pa smo izmerjene vrednosti primerjali tudi z izračuni na osnovi ITU-R modelov. Nizkocenovni sprejemnik je uspešno prestal vse teste, kar potrjuje, da je primeren za izvajanje meritev svetilniških satelitskih signalov. Z njim smo dnevno pregledovali izmerjene podatke, izključevali napačne podatke in stalno izboljševali sistem. Preverjene podatke smo nato obdelali z orodjem MATLAB in izvedli statistično analizo. Razvili smo postopke za analizo slabljenja in migljanja ter postopke za statistično analizo drugega reda ob upoštevanju trajanja in hitrosti spreminjanja presiha. Obdelavo izmerjenih podatkov smo izvajali v treh fazah tako, da smo v vsaki fazi dobili rezultate v predpisani obliki. Ti rezultati obsegajo osnovne podatke o razširjanju radijskih valov, statistično analizo meritev in tudi njihovo grafično predstavitev.

Ključne besede: razširjanje satelitskega signala; Ka-pas; meritve svetilnika; programirljivi radio

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1 Introduction

Satellite is the only viable means of providing connectivity that can reach anybody nearly anywhere. In the middle of the ocean, on an airplane in the sky or in a small village, satellite can ensure ubiquitous access and coverage on a global scale.

As the satellite transmissions at frequencies below 15 GHz are becoming congested, it is necessary to use higher frequency bands to provide wide range of broadband communication services. However, signal transmission at Ka and Q/V bands is more sensitive to atmospheric impairments, especially to attenuation due to rain, which severely affect link availability [1].

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Real-time estimation and possibly short-term prediction of such impairments can be helpful. In order to enable the design of advanced fade mitigation techniques over a wide satellite coverage area, a satellite channel modelling is required. For improved accuracy and geographical expansion of the models, a coordinated set of measurements is required on a wide scale, comprising several measurement locations. To achieve this goal, several Ka/Q-band (20/40 GHz) beacon receivers have been developed and installed across Europe to receive the signal from the Alphasat Aldo Paraboni TDP#5 payload, mostly encouraged by ESA and COST Action IC0802 [2, 3, 4].

Four Ka-band beacon receivers, based on SDR (Software Defined Radio) technology, as has been the practice in a few other similar experiments [5, 6, 7], were installed recently in Ljubljana, Lisec, Graz and Krvavec in the scope of ESA PECS project SatProSi which results are presented in this paper. In June 2012 we started with the measurements of the 19.7 GHz beacon from the Eutelsat Hotbird 13A, formerly known as Hotbird 6, at the JSI site in Ljubljana. In July 2013 we switched to the ASTRA 3B satellite, which transmits the beacon at the carrier frequency of 20.2 GHz. In August 2013 we installed the second receiver on Lisec, Slovenia, also receiving the beacon from the ASTRA 3B satellite. Finally, in February 2014 we installed the third receiver at the Hilmwarte site in Graz, Austria, and started with measurements of the Alphasat beacon at 19.7 GHz. The measurement network was additionally extended after the project completion, in February 2015. At Krvavec, Slovenia, another ASTRA 3B beacon receiver was installed.

At the level of software design, actions are being taken towards the development of a common data processing tool. At COST Action IC0802 several such tools, dealing with propagation measurements and modelling for the design of prediction and impairment mitigation techniques have been presented. The goal of such tool is to design procedures for processing the measured data, thus increasing the reliability of obtained statistical data, while remaining its usage user friendly, possibly by increasing the application of standalone automatic procedures. With the motivation to make the procedures standardized, thus achieving comparability of obtained results, the activities are being further upgraded and extended within the Group of the AlphaSat Aldo Paraboni propagation Experimenters (ASAPE) [8].

In this paper, the design and development of a SDR satellite beacon receiver is described. The beacon receiver operation was tested and validated by the linearity test, by comparing the received signal levels with the corresponding rainfall data, and by comparing the measurement results with the appropriate ITU-R models.

2 Beacon receiver

Beacon receiver, developed at Jozef Stefan Institute, is based on the Software Defined Radio (SDR) platform. USRP platform in combination with GNU Radio software framework was chosen. The measurements are collected on a PC and stored in the cloud storage. This approach is both flexible and low-cost. The receiver was improved gradually until satisfying and reliable performance was reached.

The following requirements have been defined for the beacon receiver design:
- tracking capability of the signal in the case of frequency drift,
- capability of signal reacquisition after temporal loss of signal during deep fades,
- sampling rate high enough for adequate scintillation tracking,
- robustness, high reliability and long-term operation with minimal or no periods of interruption.

The basic block scheme of the beacon receiver is depicted in Figure 1. The received signal is fed to Low Noise Block (LNB) which down-converts the signal to the IF (Intermediate Frequency) at L-band. Signal is then lead through coaxial cable to USRP, equipped with DBSRX2 daughterboard, where it is further down-converted, sampled and sent to a PC over Ethernet. DBSRX2 daughterboard ensures that signal is sent to the baseband and filtered before sampling to avoid aliasing. Signal is quadrature-sampled with 400 kHz sample rate and resolution of 14 bits. On PC, Ubuntu Linux and GNU Radio are installed.

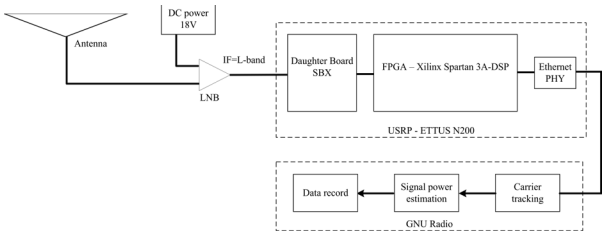


Figure 1: Beacon receiver for signal measurement

2.1 Hardware design

Based on available literature, market analysis and experience, the following hardware configuration was chosen for satellite ground station:
- outdoor unit composed of Ka-band receive only antenna system - Prodelin 3120 Series and LNB Norsat 9000HB-2,
- indoor unit composed of USRP N200/N210 box with the DBSRX2 daughterboard and

- control PC (Ubuntu linux OS, GNU radio framework) running signal processing and data logging.

2.1.1 Antenna and low noise block

The beacon receiver chain begins with an offset dish antenna manufactured by Prodelin [9]. The antenna measures 1.2 m in diameter and provides a gain of 45.8dBi at 19.701 GHz (Ka-band). It is mounted on a weighted iron stand, vertically to the floor. Figure 2 shows one of the receiver stations located at the Jozef Stefan Institute in Ljubljana.

a)

b)

Figure 2: 1.2m antenna (a) and LNB with feed (b)

In antennas focal point, an aluminium corrugated horn is mounted as a signal receptor which is connected to the LNB (shown in Figure 2 b). Since the feed's output is round waveguide the waveguide shape converter to LNB WR42 coverage flange is used. The LNB 9000HB-2, manufactured by NORSAT [10], with a frequency range of 19.2–20.2 GHz filters, amplifies and down coverts the received signal. Its block scheme is shown in Figure 3.

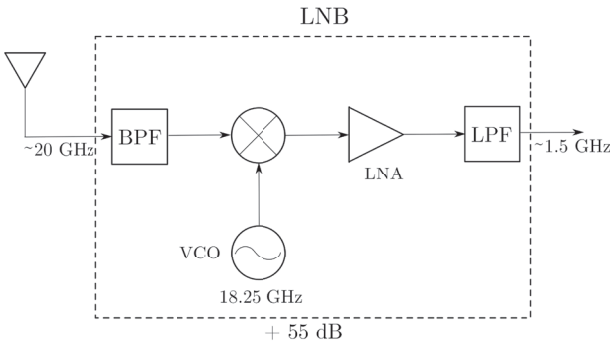


Figure 3: LNB configuration

The signal carrier at about 20 GHz is filtered in order to remove the mirror frequency and mixed with LNB's local oscillator (LO) which is locked at 18.25 GHz. Next, it is filtered to cut off signal sum and other harmonics. Finally, the signal is amplified with low noise amplifier (LNA) and filtered again to increase the carrier to noise ratio (CNR). The total gain provided by LNB is 55 dB and its noise Figure is 1.4 dB. The LNB's output 50 Ω N-type connector is joined to the indoor unit by a coaxial cable. In addition, through the coaxial cable also an 18 V DC voltage is supplied to the LNB.

2.1.2 Universal Software Radio Peripheral

The indoor unit is composed of the Universal Software Radio Peripheral (USRP) which is a range of software-defined radios manufactured by Ettus [11], now a member of the National Instruments group, and personal computer running Ubuntu linux and GNU Radio for data acquisition and logging software. In particular, the Networked series model (N200/N210) is installed in the receiver chain and controlled by GNU Radio framework [12]. An USRP includes motherboard which contains ADC, DAC and FPGA with connection to the Ethernet bus. It supports different daughterboards which are used as RF front-ends and can operate as receivers, transmitters or transcievers, depending on the model.

The USRP N210 series motherboard contains Xilinx FPGA, 100 MS/s dual analog to digital converter (ADC), 400 MS/s dual digital to analog converter (DAC) and an Ethernet interface. Motherboard gets pre-processed signal from DBSRX2 daughterboard and samples it with dual ADC. Samples are sent to computer over Ethernet.

For the RF front-end USRP DBSRX2 [11] daughterboard is used. It contains a programmable filter with a range up to 60 MHz, a mixer and a low noise amplifier. It can operate at frequencies between 800 - 2300 MHz. The block scheme of DBSRX2 is shown in Figure 4. Additionally, DBSRX2 also supplies LNB with 18 DC voltage.

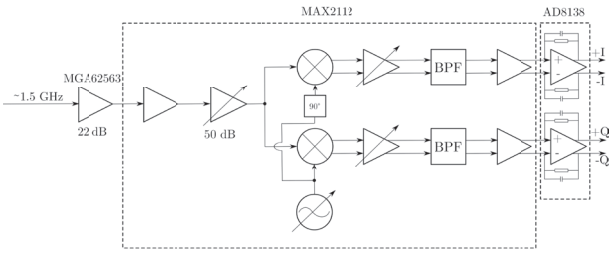


Figure 4: Daughterboard DBSRX2 block scheme

2.2 Signal processing

Software development was performed in GNURadio. It is an open-source framework with digital signal processing blocks which works with different types of data streams processed by signal processing blocks. Signal processing blocks are written in C++ or in Python, and connected by Python script.

Figure 5 depicts receiver high level software architecture. Signal samples received on ethernet bus are exposed to GNURadio via USRP Source block. Samples in the form of stream of complex numbers are sent to high pass filter (HPF) where unwanted DC spurs are compensated. HPF is a standard finite impulse response (FIR) filter performing the convolution in the time domain. Its cut-off frequency is at 60 kHz with transition width of 5 kHz. Next, the HPF samples are sent to the PLL block for compensating the short-term frequency drifts caused by DBSRX2 daughterboard, which can result in power misestimating.

PLL loop has been implemented by the GNURadio block "pll carrier tracking". The block mixes a received signal with its carrier frequency and outputs a signal on baseband as shown in Figure 6. The bandwidth, minimum frequency and maximum frequency are required as input parameters. They were set to 5000 Hz, 197000 Hz and 210000 Hz, respectively. Since the parameters must be given in rad/samp they are converted by the following equation

$$x = \frac{2\pi f}{f_{samp}} [rad / samp] \quad (1)$$

Minimum and maximum frequencies are set with respect to the beacon signal frequency.

The PLL output signal in a baseband is passed to the stream-to-vector block where the stream of complex samples is transformed into a stream of complex vector of 65536 elements. The vector is passed on to a

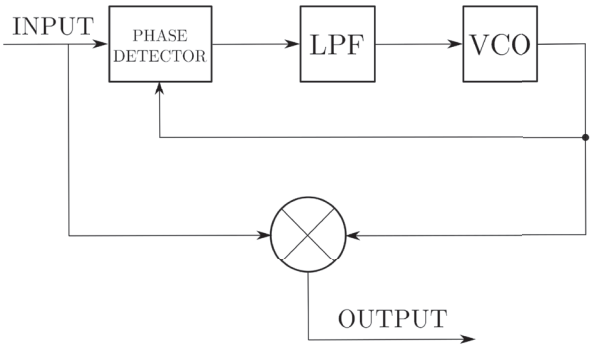


Figure 6: GNU Radio Phase-locked loop module block diagram

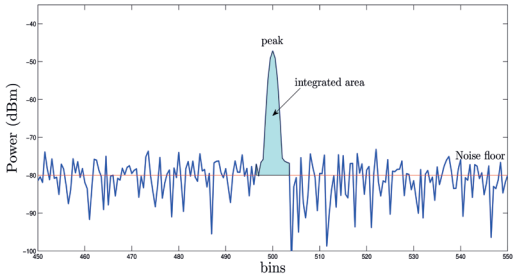


Figure 7: GNU Radio power calculation module [25]

block where FFT calculation is performed. Hanning window is used to reduce spectral leakage. The stream of complex spectrums is further sent to "mag squared block" which outputs a vector of squared spectral components magnitudes as real numbers. In the next step power estimation block takes a vector representing the signal's power spectrum, finds the signal and computes the power. Power calculation is performed by coherently adding the samples left and right of the spectrum's maximum, as shown in Figure 7. Therefore, output of this block is a real number which is written to a text file, along with a time stamp.

3 Receiver validation tests

In the development phase the receiver noise Figure has to be calculated, calibration of the receiver parameters must be performed, the dynamic range of the system has to be determined, measurement results have to be compared with parallel rain intensity measurements and scintillation characteristics must be estimated.

Figure 5: SDR signal processing block scheme [25]

3.1 Noise figure

The ADCs used in USRP N210 are ADS62P45 from Texas Instruments. The specified SNR is 73.8 dB and the maximum range is 2 V_{pp} on 50 Ω input which gives P_{max} = +10 dBm. Thus, the noise floor is calculated as

$$P_{nf} = P_{max} + SNR + ProcessGain \tag{2}$$

In our case, vector size for FFT computation and power estimation is 65536 elements, which gives

$$10\log\left(\frac{N}{2}\right) = 45.15\,dB \tag{3}$$

of process gain. Therefore, the noise floor is

$$P_{nf} = +10dBm - 73.8dB - 45.15dB = -109dBm. \tag{4}$$

The quantities described above are schematically illustrated in Figure 8. The MAX2112 chip on DBSRX2 has adjustable gain and it was set to 50 dB. Along with 22 dB gain provided by the LNA (MGA62563) allows reaching a full scale range on the AD converter at clear sky conditions. The received signal to noise ratio (SNR) is degraded by the receiver parts. Total noise temperature of the receiver is expressed as

$$T = T_A + T_{LNB} + \frac{T_C}{G_{LNB}} + \frac{T_{DBSRX2}}{G_{LNB}G_C} \tag{5}$$

where the noise temperatures of the antenna T_A and LNB T_{LNB} are 94.7 K and 101.2 K, respectively, while the noise temperatures of the cable T_C and dautherboard T_{DBSRX2} are 290 K and 627 K. Note that the noise temperature values are taken from the elements' datasheets and can vary from their actual values. The gains of the LNB G_{LNB} and cable Gc are 55 dB and -3 dB, correspondingly. The gain of the dautherboard G_{DBSRX2} is set to 50 dB. Therefore, the total noise temperature of the system is 196 K which gives, according to the receiver noise figure expressed as

$$NoiseFigure(dB) = 10 * log10\left(\frac{T(K)}{T_{ref}(K)} + 1\right) \tag{6}$$

where Tref = 290K, the total receiver noise figure of 2.24 dB.

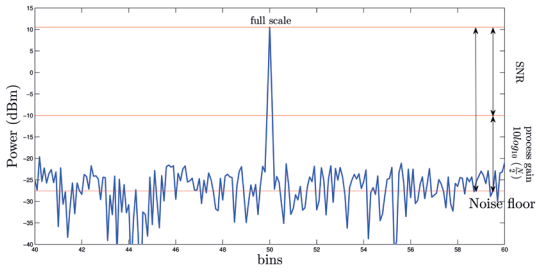


Figure 8: Noise floor limit [25]

3.2 Linearity test with dynamic range determination

The linearity and dynamic range of the USRP and daughterboard were verified by two test measurements.

In the first test the signal generator, generating continuous wave, was connected to the USRP with DBSRX2 daughterboard. Signal power was decreased from -50dBm to -130dBm in 1dB steps. The software flow graph used for this test is depicted in Figure 5 and the results are plotted in Figure 9. The results show satisfactory performance for the type of measurement that receiver is intended to perform.

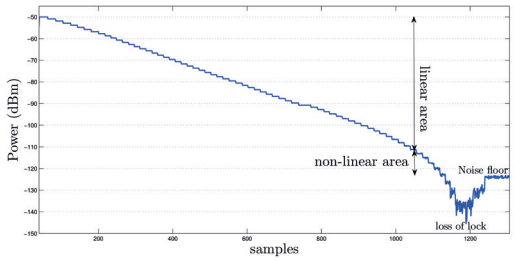


Figure 9: Linearity test with PLL block and high pass filter

During the second test the USRP with DBSRX2 daughterboard (with gain set to 50 dB) was connected to signal generator generating a continuous wave. Signal power was decreased from -50dBm to -130dBm in 1dB steps. The block scheme used for this test is depicted in Figure 10, note that the signal processing chain is without PLL processing block.

The plot of the results is presented in Figure 11. As it is seen, in this configuration the receiver is able to trace the range of around 60 dB. The result is obviously better than the previous; however, the problem is that this configuration cannot be used in real operation of the

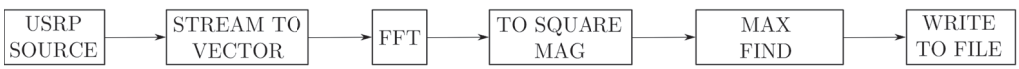


Figure 10: Linearity test block scheme [25]

receiver, due to unstable frequency reference in the MAX2112 tuner on the DBSRX2 daughterboard. We decided to circumvent this problem by designing our own additional down-conversion stage and then using the BasicRX daughterboard.

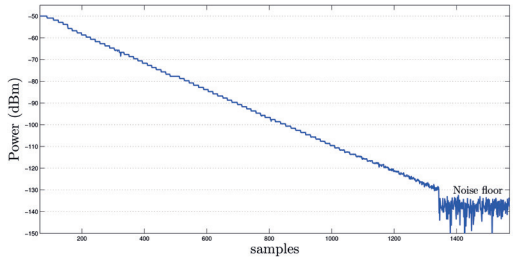


Figure 11: Linearity test without PLL block and high pass filter [25]

3.3 Receiver parameters calibration

For the purpose of optimal parameter settings, tests with waveguide attenuators and long-term frequency drift estimations were applied. In order to accurately determine dynamic range, waveguide attenuators were used. The attenuators have been placed in-between the LNB and the feed, as shown in Figure 12.

Figure 12: Waveguide attenuators for dynamic range determination

The experiment was started with full attenuator conductivity and typical receiver settings. Afterwards, the variations to various receiver parameters were applied and the attenuation was slowly increased until the signal was lost, thus checking the obtained dynamic range of new parameter settings. The experiment was repeated several times, applying variations to the number of FFT bins, sampling frequency, PLL bandwidth and gain. As a result of this test, we set values for the number of FFT bins to 65536 and the sampling frequency to 400 Hz. The frequency drift was causing occasional traverse of the carrier frequency out of the bandwidth borders, determined by the sampling frequency. To avoid occasional instability in received signal strength the PLL bandwidth value was set 5 kHz and minimum and maximum locking frequencies to 197 kHz and 210 kHz, respectively. However, to avoid this problem in the future, a routine for keeping the track of the carrier frequency was added.

3.4 Comparison with parallel rain intensity measurements at a nearby site

The main purpose of the designed receiver is to detect the atmospheric attenuation of the received beacon signal that is caused mainly by rain. Therefore, the measurements were compared with the rainfall intensity measurements made in parallel at a nearby site by a meteorological research group [13]. The measurements are recorded by a tipping-bucket rain gauge, which is about 170 m away from our station [14]. The resolution of the rainfall intensity measurements is 5 minutes. The two observed data sets are highly correlated, as seen in the example measurement day, 21st May 2012, shown in Figure 13.

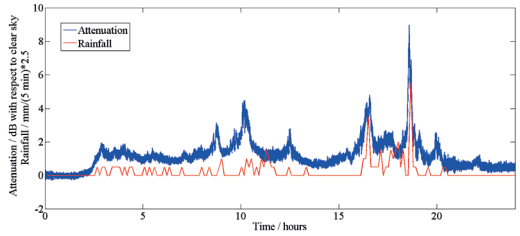


Figure 13: Comparison of attenuation time series with rainfall measurements on May 21, 2012

3.5 Estimation of scintillation characteristics

Data from a newly set up receiver were analysed by observing fast-fading events such as amplitude scintillation. The sampling rate performed by our receiver is sufficient for the study of scintillation characteristics.

We have written two procedures for scintillation analysis. The first procedure calculates the power spectral density of the signal in order to compare it with expected signal behaviour. The power spectral density of

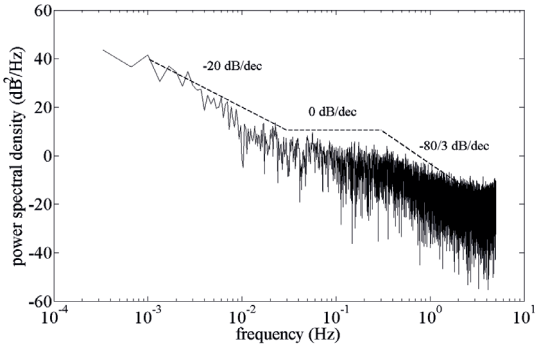


Figure 14: The measured signal spectrum on 24th May 2012 (solid line) compared to the theoretical model (dashed line)

scintillation can be described typically by a -20 dB/dec slope followed by a flat region and another slope with -80/3 dB/dec [15]. The theoretical spectrum is seen to agree well with the measurements. An example comparison for the measurements performed on a typical rainy day on 24th May 2012 is shown in Figure 14.

The second procedure was used to evaluate the long-term scintillation behaviour by comparison of cumulative distribution functions of measurements and existing scintillation models. The ITU-R P.618 [16] model provides a complementary cumulative distribution function (CCDF) of fade depth, based on long-term averages of atmospheric parameters and communication link characteristics. For our needs, the wet term of surface refractivity, which is one of the inputs to ITU-R P.618, has been expressed with the ITU-R P.453 model [17]. The modelled CDF has been compared to the measurements obtained in the time interval 24th May – 8th June 2012. In order to separate the scintillation phenomenon from the long-term attenuation variations, the measured signal has been filtered with a high pass filter with a cut-off frequency of 0.025 Hz [18]. The results in Figure 15 confirm receiver adequacy for scintillation detection.

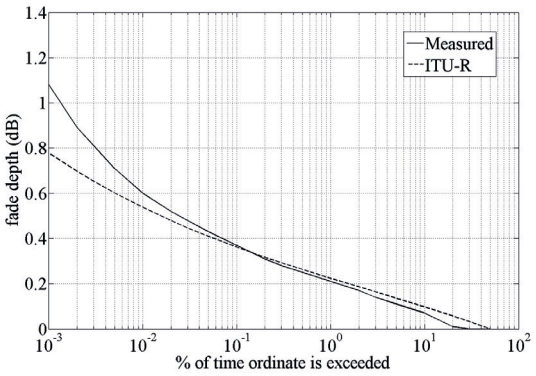


Figure 15: Complementary cumulative distribution function of the measured scintillation fade depth compared to the ITU-R model

4 Data processing procedure

The data obtained from the receiver are processed in 3 phases, where each phase represents a conversion from one data format to another. After each phase, a new intermediate result is obtained and saved in files. The last phase returns statistical results presented graphically. Figure 16 illustrates the whole process [19].

In the data processing tool, four data types exist and are processed in three data processing phases, namely:
- Raw Propagation Data (RPD),
- Intermediate Propagation data (IPD),
- Analysed Experimental Statistics (AES),
- Graphical Statistical Representation (GSR).

4.1 Data processing phases

The presentation of propagation experiment is performed in three different phases. In the *input data preparation phase (RPD – IPD)* the measured data is read, spikes are detected and operations which require interactions with the user (visually inspect signals and perform template extraction and calculate co-polar in-excess attenuation time series) are performed. The *statistical analyses phase (IPD – AES)* calculates complementary cumulative distribution functions (CCDF) of attenuation from a series of processed data, calculates second order distributions, i.e. fade slope and fade duration, and write the results in text files. In the last *visualisation and result validation phase (AES – GSR)* the visualisation of the obtained results as plotted graphs is performed and the results are compared to ITU-R models results.

The main tasks, performed in the *input data preparation phase* are spike detection, visual inspection and template extraction. In the beacon signal measurements, samples with obvious deviation from local average, so-called outliers or spikes, may occur. Their detection is performed automatically and they are flagged as doubtful. The method for spike detection is based on 2 min moving average based standard deviation, which is calculated continuously by:

$$\varepsilon(i) = \sqrt{\langle CPL(i)\rangle^2 - \langle CPL(i)\rangle^2} \tag{7}$$

where the *CPL(i)* is the i-th beacon level sample within the day (dB) and $\langle CPL(i)\rangle$ mean value of *CPL(i)* using 2 minutes moving average filter (dB). The standard deviation serves as a threshold for comparison with actual samples. When the difference between the signal strength and its moving average $|CPL(i) - \langle CPL(i)\rangle|$ is larger than the threshold, defined as standard deviation, multiplied by a selected value *thresh_scale*, the sample is recognized as an outlier. Formally expressed, outliers are samples, for which the following equation holds:

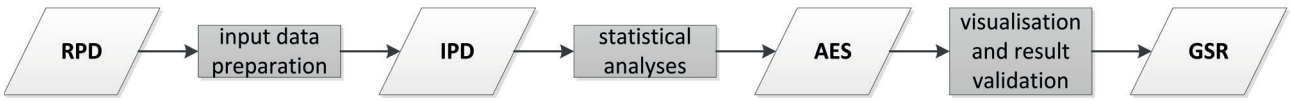


Figure 16: Data processing procedure steps

$$\left|CPL(i) - \langle CPL(i)\rangle\right| > 5\sqrt{\langle CPL(i)^2\rangle - \langle CPL(i)\rangle^2} \quad (8)$$

The operation is illustrated in Figure 17 with selected value *thresh_scale* = 5. The detected outliers are marked by red circles.

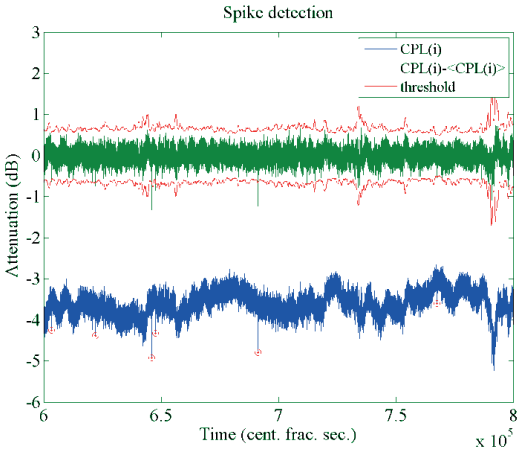


Figure 17: Spike detection example - spikes are marked by red circles

In order to assure correctness of automatically determined validity flags the measured values of beacon signal level are inspected visually on a daily basis. In case of irregular signal behaviour (saturation, fluctuation, missing samples, etc), the observed time frame is selected, its validity flags are changed from valid to invalid and samples are excluded from further analysis. Figure 18 (a) shows an example of regular behaviour of measured signal, where no actions are necessary while the signal shown in Figure 18 (b) is highly attenuated and reached saturation. In this case marked samples were excluded from statistical analysis.

Since the radiometer measurements are not available, the template extraction has to be used as a method for 0 dB level estimation. The procedure finds a function which corresponds to system-dependent received signal variations, and subtracts it from the beacon signal level. The purpose of this step is to eliminate all potential systematic errors, which deteriorate accurate evaluation of atmospheric impairments. Example sources of such errors are pointing errors due to satellite movements, gain instabilities in RF chains and other phenomena such as the wet antenna effect. While it is impossible to guarantee exactness of such a procedure, it is estimated that the systematic error is limited within a margin of maximum 1 dB. Experimental evaluation of the described effects has been performed in [4]. At the end of the procedure, the resulting signal corresponds to a sum of background attenuation in clear sky conditions and recorded atmospheric impairments.

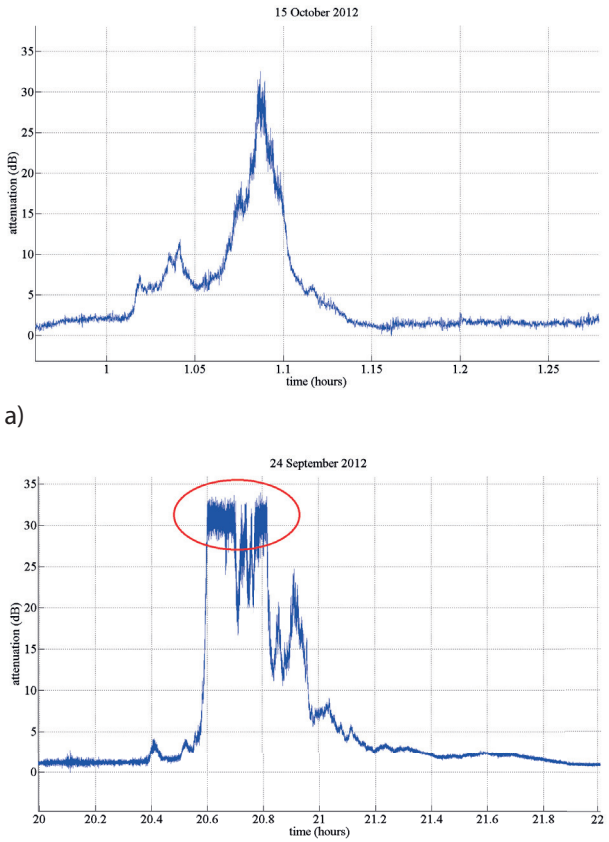


Figure 18: Regular deep fade with no saturation (a) and with saturation (b)

The search for template function represents finding a moving average of the received beacon signal in clear sky conditions and finding of a proper interpolation for the time intervals with rain events. The procedure is divided into three steps: (i) determination of events, (ii) finding template function, (iii) subtraction.

In the first step, the events with strong fluctuations are identified and flagged. The second step depends on the form of the beacon signal (i.e. clear sky with no oscillations, rain event presence and oscillating signal) which dictates the selection of the adequate method (i.e. maximum probable value detection, polynomial fitting and FFT based interpolation). Maximum probable value detection sorts detected signal levels according to their frequency of appearing. The most frequent value is selected. In polynomial fitting, a polynomial function of a selected order is found to fit the measured beacon signal. In FFT based interpolation, a Fast Fourier Transform is used for this purpose, and is especially suitable for oscillating signals with periodic behaviour. In practice, the polynomial fitting method is mostly used. Finally, in the last step, the obtained template function is subtracted from original beacon signal.

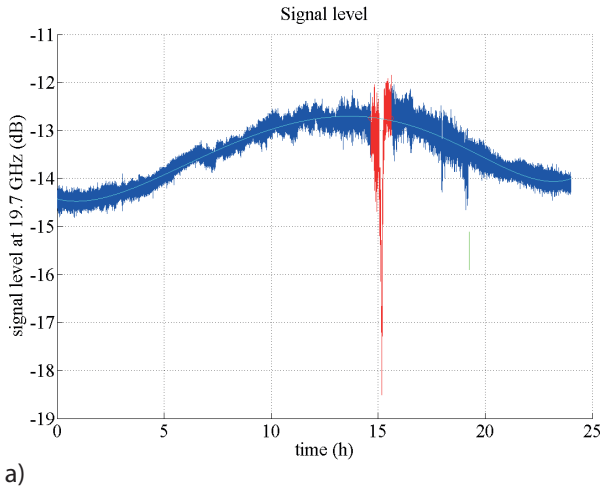
Figure 19 depicts an example template extraction for the measurements, obtained on the day with rain event. In the first step, an interval not to be considered is chosen (Figure 19 a, red colour) while in the second step, a polynomial function of 6th order is determined according to remaining beacon signal (Figure 19 a, cyan line). The obtained signal is shown in Figure 19 (b). In this example, the mispointing error due to the inclined orbit of the satellite may be clearly observed as a periodic signal fluctuation. If the polynomial fitting was not applied, a systematic error of about 2 dB would have been added. It is clearly seen how the procedure eliminates the error, such that the clear-sky levels are correctly represented, while the rain-induced attenuation remains.

The task of the *statistical analyses phase* is to calculate statistics from the obtained attenuation time series. In this phase the co-polar attenuation analysis, fade duration analysis and fade slope analysis are performed. Co-polar attenuation analyses include reading the long term attenuation data and calculating their complementary cumulative distribution function (CCDF). For the fade duration analysis long term attenuation data are read and relative number of event CCDF and relative fade time CCDF are calculated. Fade slope statistics are calculated by determination of signal dynamics (derivative) and their expression in terms of cumulative distributions.

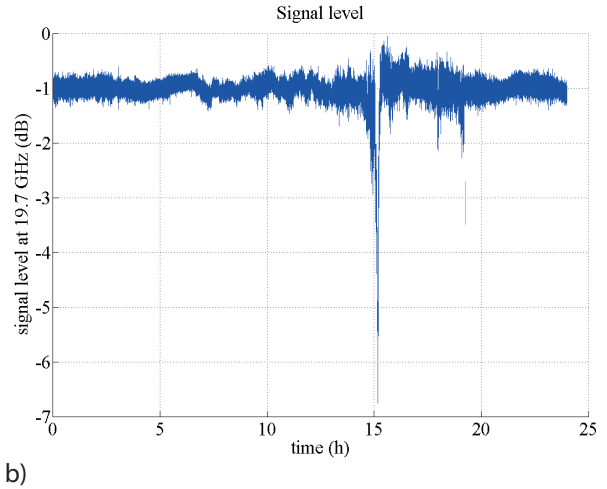
In the final phase, *visualisation and result validation phase,* the statistical analyses results, namely CCDF of attenuation, CCDF of relative number of fades, CCDF of relative fade times and CCDF of measured fade slopes, are graphically presented.

5 Analyses of the measurement results

In this section, the results are presented for one full year of analysed data. In addition to attenuation analysis, also the rain rate analyses for the same time period have been performed. The complementary cumulative distribution functions (CCDF) have been calculated for various time scales, i.e. for 1 full year and for 4 different

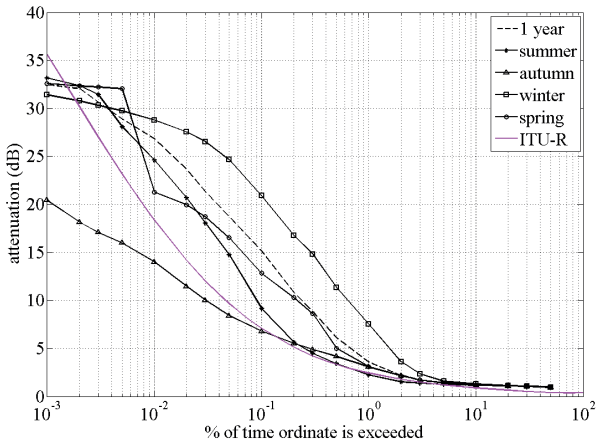


a)

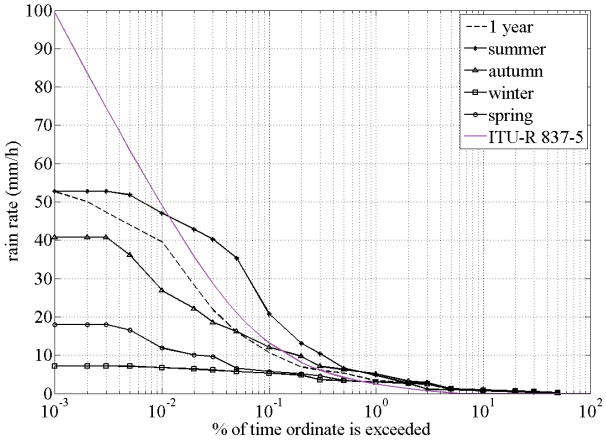


b)

Figure 19: Determination of event and the template function (a), resulting signal (b)



a)



b)

Figure 20: CCDF of attenuation (a) and CDF of rain rate (b)

seasons (summer, autumn, winter, spring). The results are depicted in Figure 20. In Figure 20 a, the cumulative distribution functions of attenuation are given in comparison to ITU-R P.618 model [16], while graph in Figure 20 b, depict cumulative distribution functions of rain rate compared to the ITU-R 837-5 model [20].

In general, the results comply well with expectations, both in terms of comparison to the ITU-R models as well as in terms of seasonal variations (more severe rain and consequently attenuation in summer months) for low probabilities. The comparison of attenuation distributions with rain rate distributions also reveals similarities, especially for autumn and summer months.

However, in winter and spring there are some deviations, which are due to the snow. While the rain gauge cannot correctly measure the snow quantities, the snow still affects the received signal strength, which may be even further deteriorated if snow sticks to the satellite dish. Although the snow from the dish was cleaned regularly and the measurements with obvious deviations were discarded later, the effect could not be completely eliminated.

Second order statistics analysis has been made for the same time period as for the attenuation statistics. Fade duration is defined as the time interval between two crossings above the chosen attenuation threshold, while the fade slope represents the rate of change of attenuation with time. Both for the fade duration and fade slope statistics, a filter with cut-off frequency 25 mHz has been applied. For the fade slope calculations, the time interval to consider was set to 2 s. The ITU-R P.1623-1 model [21], proposed by Van de Kamp [22], has been used for comparison.

The fade slope statistics are depicted in Figure 21. The distributions for 5 dB attenuation level match quite well the model. For the other chosen attenuation levels, a slight deviation may be observed, similarly as in some other studies [23], [24].

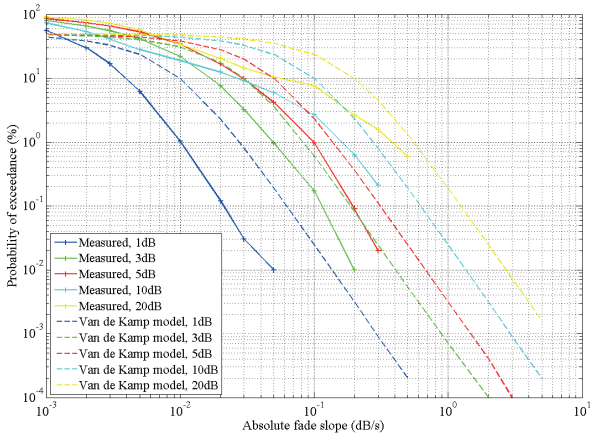
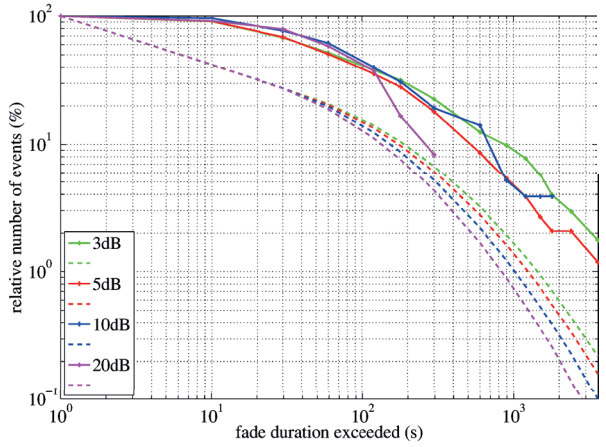
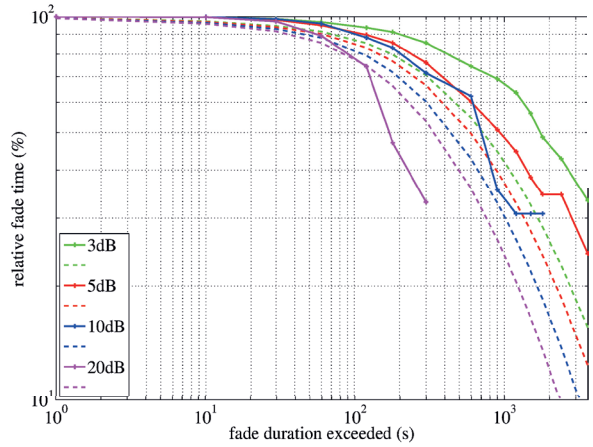


Figure 21: CCDF of measured fade slopes in comparison to Van de Kamp model

The fade duration distributions in Figure 22 show some discrepancy between the measured values and the model, but the trend is similar. Also variations due to differently chosen attenuation thresholds follow similar rules. For lower thresholds, the relative number of fades and relative fade times are proportionally higher.



a)



b)

Figure 22: CCDF of measured relative number of fades (a, solid lines) and relative fade times exceeding given fade durations (b, solid lines) in comparison to ITU-R P.1623 model (dashed lines)

6 Conclusion

The low-cost SDR beacon receiver passed all tests successfully, confirming that we established a reliable measuring system. In general we confirmed that the obtained results comply well with expectations, both in terms of comparison to the ITU-R models as well as in terms of seasonal variations.

Although focusing on the beacon measurements in Slovenia, the project results are important and interesting also for the broader satellite communications research community. On the European scale, we contributed with the project to the ESA scientific experiment which aims at a coordinated acquisition of propagation measurements in Europe.

7 Acknowledgement

This work has been funded in part by the European Space Agency through the PECS programme, project SatProSi. We thank Mr. Sebastijan Mrak for technical support.

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Arrived: 29. 10. 2015
Accepted: 28. 01. 2016

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 1(2016), 24 – 28

Temperature and process compensated RF power detector

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Abstract: This paper describes the design of process and temperature compensated wide band radio frequency power detector in a standard UMC 0.13-µm RF CMOS process. Proposed power detector core consists of two RF NMOS transistors biased for operation in weak inversion and output signal of the power detector core is a linear function of input RF peak voltage and residual temperature dependence. Additional compensation circuit is designed in order to make the output voltage less sensitive on temperature and process variation. Power detector circuit has 20 dB of the dynamic range and is especially suitable for use in transmitter chain applications. The temperature compensation provides typical reduction of 50% in temperature sensitivity of the circuit.

Keywords: RF power detector; temperature compensation; weak inversion; Bessel function; compensation circuit

Temperaturno in procesno kompenziran RF detector moči

Izvleček: Članek opisuje dizajn procesno in temperaturno kompenziranega detektorja moči širokopasovne radio frekvence v standardni UMC 0.13-µm RF CMOS tehnologiji. Jedro detektorja se sestoji iz dveh RF NMOS tranzistorjev za delovanje v slabi inverziji. Izhodni signal detektorja je linearna funkcija vhodne RF napetosti in ostanka temperaturne odvisnosti. Dodatno kompenzacijsko vezje znižuje temperaturno in procesno odvisnost. Dinamično območje detektorja moči je 20 dB in je posebej primeren za uporabo v prenosnih verigah. Temperaturna kompenzacija tipično za 50 % zmanjša vpliv temperature.

Ključne besede: RF detektor moči; temperaturna kompenzacija; šibka inverzija; Besselova funkcija; kompenzacijsko vezje

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1 Introduction

Power detectors are widely used in wireless communication systems, in receiver and transmitter chain. Optimal gain setting of the receiver chain is highly dependent on the power level of the input signal. In order to meet optimum gain, power level of the input signal should be measured in real time and appropriate gain adjustment of the receiver chain should be performed. Characteristic for this application is that it requires the dynamic range of power detector circuit exceeding 50 dB or more.

In many applications transmitter should be capable to operate with variable peak level of the output power. In order to obtain accurate power gain control, power detector should be employed in the control feedback loop [1]. Power detectors are also used for: power amplifier emergency shutdown in case of high VSWR [2], predistortion linearization of power amplifier using envelope-feedback [3], or as a part of system for envelope elimination and restoration power amplifier [4].

Power detectors for transmitter applications have relaxed dynamic range requirements compared to those employed in receiver, but other factors may be of importance. Self-heating of the power amplifier affects the performance of power detectors by changing their accuracy [5]. In order to have temperature independent behavior, power amplifier and power detector are usually designed together due to the large mutual influence [5]. Another constraint for power detectors is requirement for low power consumption in order to keep high level efficiency of the overall system.

There are few groups of the power detectors – mixer based [6], Schottky diode [7] and monolithic low power

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RF peak detector [8]. First two topologies are not quite suitable for CMOS RF IC implementation regarding: unavailability in standard CMOS RF process, bandwidth limitation, large chip size, high power consumption, etc.

Monolithic low power RF peak detector is most suitable for RF IC implementation due to its advantages of simplicity, wide bandwidth, low power and small chip area [8]. However, it has temperature and process dependence and wideband precision power detectors are mostly implemented in expensive bipolar technology [8].

In this paper, monolithic, low power, process and temperature independent RF peak detector has been developed. It uses NMOS transistors biased in weak inversion in order to get the exponential transistor behavior. Additional circuit for temperature and process compensation has been proposed. The new detector uses inexpensive RF CMOS technology and provides temperature and process independent power detection without post-fabrication trimming.

The paper structure is as following: the design of the power detector core circuit is presented in Chapter 2. Topology and design of the new temperature compensation circuit is presented in Chapter 3. Obtained simulation results and post processing with possible applications are presented in Chapter 4 and 5, respectively. Finally, conclusion is introduced in Chapter 6.

2 Proposed RF power detector

The core of the RF power detector is shown in Figure 1.

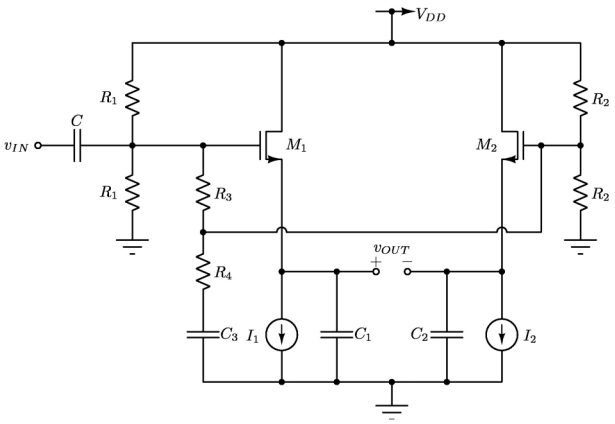

Figure 1: RF power detector core schematics

In order to obtain exponential behavior, transistors M_1 and M_2 are biased for operation in weak inversion. Transistors have the same channel width, number of fingers, length and their bias currents are equal $I_1=I_2=I_{DC}$. Corresponding resistors and capacitors are matched, namely, $R_1=R_2$, $R_3=R_4$, $C_1=C_2$. In this case, the AC signal magnitude at gate M_1 is two times greater than at the M_2 gate.

With given assumptions, instantaneous and average drain currents of transistor M_1 are:

$$i_{D1} = I_S e^{\frac{V_{gs1}-V_t}{nV_t}} = I_S e^{\frac{V_Q-V_T}{nV_t}} e^{-\frac{V_{OUT}^+}{nV_t}} e^{\frac{V_m\cos(\omega_0 t)}{nV_t}}, \quad (1)$$

$$\overline{i_{D1}} = I_1 = I_{DC} = I_S e^{\frac{V_Q-V_T}{nV_t}} e^{-\frac{V_{OUT}^+}{nV_t}} \frac{1}{T}\int_0^T e^{\frac{V_m}{nV_t}\cos(\omega_0 t)}\,dt = I_S e^{\frac{V_Q-V_T}{nV_t}} e^{-\frac{V_{OUT}^+}{nV_t}} I_0\left(\frac{V_m}{nV_t}\right). \quad (2)$$

Average drain current of transistor M_2 is:

$$\overline{i_{D2}} = I_2 = I_{DC} = I_S e^{\frac{V_Q-V_T}{nV_t}} e^{-\frac{V_{OUT}^-}{nV_t}} I_0\left(\frac{V_m}{2nV_t}\right). \quad (3)$$

Where:

V_m - peak amplitude of AC input signal
V_Q - gate DC voltage$I_0(x)$ - modified Bessel function of order zero
n - technology dependant sub-threshold slope parameter

From (2) and (3) it can be seen that average drain current is increased by a factor $I_0(V_m / V_t)$ when RF signal is present. Since the modified Bessel function of order zero is monotonically increasing, the average drain current monotonically increases with RF signal amplitude.

However, the average (DC) current of transistors M_1 and M_2 is constant, and set by current sources I_1 and I_2. Therefore, the average gate-source voltage V_{gs} must decreases for (2) and (3) to hold. This change in average V_{gs} due to input RF signal amplitude is the basis of power detector operation.

For large values of x, $I_0(x)$ has an asymptotic approximation:

$$I_0(x) \approx \frac{e^x}{\sqrt{2\pi x}}. \quad (4)$$

Using equations (2) and (3), the output voltage can be written as:

$$V_{OUT} = V_{OUT}^+ - V_{OUT}^-, \quad (5)$$

$$V_{OUT} = nV_t \ln\left(\frac{I_0\left(\frac{V_m}{nV_t}\right)}{I_0\left(\frac{V_m}{2nV_t}\right)}\right). \quad (6)$$

If we apply approximation (4) on the equation (6), we can get:

$$V_{OUT,PD} = \frac{V_m}{2} - \frac{nV_t}{2}\ln(2). \quad (7)$$

Where:

$$V_t = \frac{kT}{q}. \quad (8)$$

From equation (7), it can be recognized that the average output voltage consists of two factors. First term is proportional to the peak value of the input signal, and the second term is proportional to the temperature. Temperature-dependent term can be cancelled by including an additional circuit in the design, which produces the output voltage proportional solely to the temperature. Temperature dependence of the signal described in equation (7) may be minimized to a large extent by subtracting the power detector voltage from compensation circuit output. Design of temperature compensation circuit is presented in the following section.

3 Compensation circuit

Figure 2 presents topology of the compensation circuit that is used for compensation of the temperature dependent part in equation (7). Like in the core of the RF power detector, transistors M_A and M_B are operating in weak inversion. Transistor M_A has the same dimensions and the same biasing conditions as transistors M_1 and M_2 in the power detector core. The width of the transistor M_B is two times greater than the width of M_1 and they have same value of bias currents. Transistors M_C, M_D and M_E operate as current mirrors and should be perfectly matched. In order to keep same drain voltages in current mirrors, transistor M_F has been employed and it has to be matched with M_A. Additionally, the bias resistors should also be matched, $R_A = R_B = R_E$. The output current I_D of the circuit in the Figure 2 is given by the equation (9).

$$I_D = \frac{V_{GS1} - V_{GS2}}{R_3}. \quad (9)$$

Since transistors M_A and M_B are operating in the weak inversion, the output current is given with:

$$I_D = \frac{V_{GS1} - V_{GS2}}{R_3} = \frac{nV_t \ln\left(\frac{I_D}{I_{S1}}\right) - nV_t \ln\left(\frac{I_D}{I_{S2}}\right)}{R_3}, \quad (10)$$

$$I_D = \frac{nV_t \ln\left(\frac{I_{S2}}{I_{S1}}\right)}{R_3} = \frac{nV_t \ln(2)}{R_3}, \quad (11)$$

resistor value R_C should be set in a way that currents I_D and I_{DC} from detector circuit core shown in Figure 1 are equal. Furthermore, compensation circuit could be used as a current source for the power detector core.

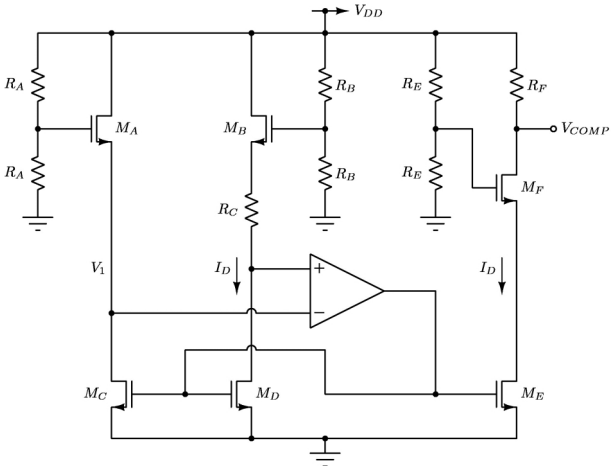

Figure 2: Compensation circuit

Output voltage of the circuit in Figure 2 is given with the following equation:

$$V_{COMP} = V_{DD} - \frac{nV_t R_F \ln(2)}{R_E}. \quad (12)$$

In order to get temperature independent signal, signals at the outputs of the power detector core and calibration circuit (given with equations (7) and (12)) should be subtracted, given the value for the compensated output voltage of the power detector circuit.

$$V_{OUT} - V_{COMP} = V_{DD} - \frac{V_m}{2} + nV_t \ln(2)\left(\frac{1}{2} - \frac{R_F}{R_E}\right). \quad (13)$$

If the value of the resistor R_F is two times smaller than value of R_B, we can get:

$$V_{OUT} - V_{COMP} = V_{DD} - \frac{V_m}{2}. \quad (14)$$

From last equation it can be recognized that the output voltage is temperature and process independent.

4 Simulation results

Based on the previous discussion power detector core and compensation circuit are designed in standard UMC 130nm CMOS RF technology. Parameters of all components are shown in Table 1.

Table 1: Parameters of the components

Components	Parameter	Value
M1, M2, MA, MF	W/L [µm/µm]	2*(5/0.34)
MB	W/L [µm/µm]	4*(5/0.34)
MC, MD, ME	W/L [µm/µm]	4*(4/2.5)
RC	Resistance [Ω]	3922
RF	Resistance [Ω]	1961
RA, RB, RE, R1, R2	Resistance [Ω]	60000
R3, R4	Resistance [Ω]	25
C, C1, C2, C3	Capacitance [pF]	10
I1, I2	Current [µA]	10

Layout of complete chip is presented in Figure 3.

Figure 4 presents voltage sensitivity $\partial V_{OUT}/\partial V_m$ of the output signal performed at frequency of 5GHz. The dynamic range of the input signal amplitude can be estimated from this figure. Lower limit is determined by modified Bessel function approximation given in the equation (4). Namely, this approximation is valid for input AC amplitude greater than 0.2 V. Upper limit presents the highest peak level of the voltage input signal for which all transistors are in saturation. This voltage is determined to be 2 V, giving the operation range of the power detector of approximately 20 dB.

It can be concluded that power detector works with high amplitude level of the input signal, what is desirable for RF transmitters.

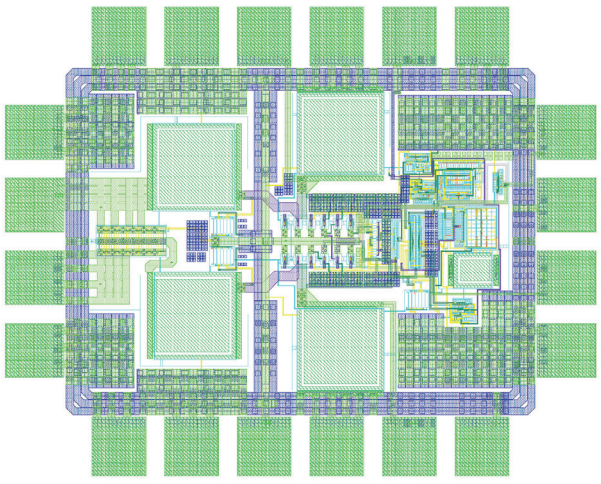

Figure 3: Power detector with calibration circuit

The power detector is simulated with and without the compensation circuit, in order to demonstrate the improvement. Simulations were performed for AC signal magnitude of 1 V and frequency of 5 GHz. Improvement is reached in industrial temperature range of -40 ^{0}C to 100 ^{0}C. Maximum temperature coefficient $(\partial V_{OUT}/\partial T)_{MAX}$ is decreased about two times using this technique.

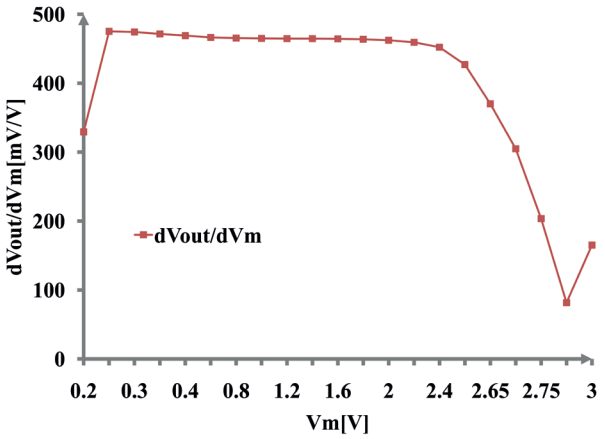

Figure 4: Voltage coefficient of the signal at the output of the power detector

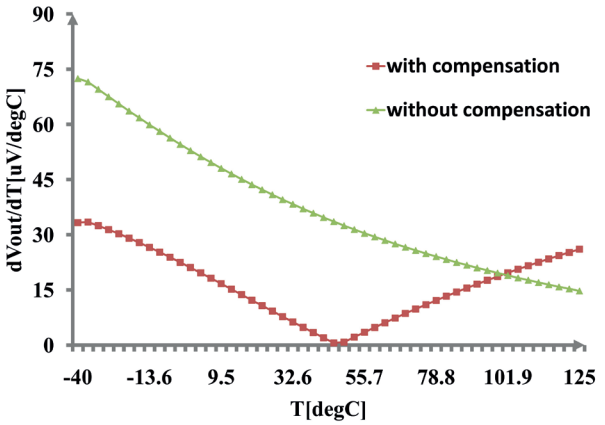

Figure 5: Compensated (red) and non-compensated (green) temperature coefficient of the output signal

5 Post processing and applications

Post processing can be done in analog or digital domain. Each of these options will be discussed in the details including advantages and drawbacks as well as possible applications.

5.1 Analog post processing

Straightforward way to combine the power detector core with the compensation circuit is to use instrumentation amplifiers to perform subtracting and amplifying.

The most important parameter for the amplifiers would be input offset in order to keep high level of accuracy. Clear advantage is simple design and ability to detect input amplitude independently of process or temperature variation. Main disadvantage is small dynamic range 20dB. Although, there are some applications

where this might be enough as; amplifier linearization techniques [9] including polar loop system [10] and amplitude envelope feedback system [10].

5.2 Digital post processing

Dynamic range might be increased using digital post processing. Power detector output voltage (6) and compensation circuit output voltage (12) could be sampled and post processed in digital domain. Parameter nV_t might be extracted from (12) and be used in (6) for extraction of the amplitude V_m. Dynamic range is extended since there is no need for the asymptotic Bessel function approximation (4). Drawback would be complex design. This technique could be used for broad range of applications where temperature and process independent amplitude detection is needed.

6 Conclusion

Today, inexpensive scaling CMOS technology allows large level of integration and operation of the circuits at high frequencies. Its main disadvantage is limitation of the process control, which leads to large variation of component parameters. Wide temperature operation range limits the accuracy of power detector due to temperature-dependent terms in output voltage. In some particular cases, this limitation can be solved by using such circuit topologies which performance depends only of well controlled component matching. This paper presented design of such power detector including compensation circuit.

Using the proposed and described circuit topology, significantly lower temperature dependence of the power detector circuit has been achieved. Namely, maximum temperature coefficient is decreased about two times for input signal level between 0.2 V and 2 V. Power detector temperature dependency is minimized to the extent that it can be neglected in many industrial applications, enabling its widespread use in further designs. For applications which require higher dynamic range, digital post processing could be applied.

7 Acknowledgment

This work has been supported by SENSEIVER project founded by European Commission as a part of Marie Curie Program.

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Arrived: 04. 12. 2015
Accepted: 02. 03. 2016

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 1(2016), 29 – 35

An Integrated Microtransformer System for Displacement Measurement

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Abstract: The paper discusses the design and prototype evaluation of an integrated inductive microsystem used for displacement measurement, realized in the form of an ASIC. The advantage of the system is in its ability to operate without external stimulation such as a magnetic field source or an optical source used in conventional position encoders. The system comprises multiple microtransformers with corresponding analog front-end electronic circuits and is fabricated in an unmodified 350 nm CMOS process. The microtransformers consist of two concentric microcoils with their magnetic coupling dependent on the position of an external metal object, i.e. a target or a scale. The primary microtransformer winding is excited by an AC signal with a frequency of several MHz. This signal induces the secondary voltage, which has its amplitude and phase modulated by a moving metal scale. The modulation is then measured by the analog front-end as a differential output signal of two series of adjacent microtransformers geometrically shifted by a half of the scale period. The paper introduces the design and the construction of the microsystem, presents the results of the microtransformer characterization with a resolution of 100 µm, and explains the output characteristics shape due to the asymmetry in the microtransformer pair.

Keywords: inductive sensor; eddy-current sensor; displacement sensor; ASIC; microtransformer

Integriran mikrotransformatorski sistem za merjenje pomika

Izvleček: Prispevek obravnava zasnovo in evalvacijo testnega induktivnega mikrosistema za merjenje pomika, realizirano kot namensko integrirano vezje (ASIC). Prednost sistema je možnost delovanja brez zunanjega magnetnega ali optičnega vira, kot se uporabljajo pri konvencionalnih enkoderjih položaja. Sistem, ki je izdelan v nemodificiranem 350 nm CMOS procesu, obsega več mikrotransformatorjev ter ustrezen analogni vmesnik. Mikrotransformator sestavljata dve koncentrični mikrotuljavici, na magnetni sklop katerih vpliva položaj zunanjega kovinskega objekta (tarče oz. merilne letve). Primarno navitje mikrotransformatorjev je vzbujano z izmeničnim signalom frekvence nekaj MHz. Ta signal inducira sekundarno napetost, ki je amplitudno in fazno modulirana s premikanjem tarče. Analogni vmesnik izmeri modulacijo kot diferencialni izhodni signal dveh zaporedij mikrotransformatorjev, ki sta geometrijsko zamaknjeni za polovico periode merilne letve. Prispevek razloži zasnovo in zgradbo mikrosistema, predstavi rezultate karakterizacije mikrosistema z ločljivostjo 100 µm, ter pojasni obliko izhodnega signala z vidika asimetrije v paru mikrotransformatorjev.

Ključne besede: induktivni senzor; senzor na vrtinčne tokove; senzor pomika; namensko integrirano vezje; mikrotransformator

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1 Introduction

Beside optical encoders, various types of magnetic position encoders are widely used in position sensing applications. The most common sensor mechanisms employed in these applications are based on the effect of Lorentz force onto charge carriers: Hall or magnetoresistive effect. These devices can be produced as monolithic integrated circuits using microelectronic technologies [1].

Magnetic position encoders deliver information about the linear or rotary displacement by measuring the variations in the magnetic field strength in the environment. The spatially variable, position-dependent time-stationary magnetic field is commonly generated using a magnetized scale or a fixed magnet. The availability and cost, as well as environmentally questionable production [2] of rare earth elements, which are currently the key magnetic materials, can present an issue for the

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position encoder industry. Additionally, conventional optical encoders also require an external light source (e.g. a LED) [1].

Since the industry is in constant search for reliable, precise, robust, dimension- and cost-effective position encoders, research in unconventional sensor principles is strongly encouraged. It is our belief that encoders fabricated in the form of an ASIC, without requiring additional components and/or costly wafer postprocessing for their fabrication, will play an important role in the future. The presented issues of conventional sensors, as well as expected trends in position sensor industry, have led us into research of the possibilities of ASIC implementation of the inductive position sensing, which is also common in industrial applications [1].

The main difference of inductive sensing concept in comparison to magnetic encoders is in the fact that a time-variable magnetic field of a certain frequency is employed instead of a stationary magnetic field.

For detecting the presence of the object (i.e. without precise determination of an object position), two major types of inductive proximity sensors are in widespread use:

1. A dual-coil structure; the first coil, connected to an AC source, induces the voltage in the second coil. If a conductive object (the target) is moved into the vicinity of the coils, eddy currents are induced in the conductor, generating a magnetic field opposing the field of the first coil. The voltage in the secondary coil is thus reduced due to the eddy current energy loss in the target [1,3].
2. An oscillatory type, where a coil (or in some cases, a transformer) is used as the inductive part of a resonant circuit. When the target is approached, the inductance of the coil changes, resulting in the change of the oscillator resonant frequency [1,4].

Another benefit of inductive sensors beside the aforementioned lack of need for permanent magnetic elements, is their insensitivity to dust, which presents a strong advantage in an industrial environment in comparison to the optical sensors [3].

2 Microsystem design

2.1 Differential operation of a microtransformer

The paper addresses the topic of integrating an inductive position sensing microsystem on a single silicon die. The discussed system employs a concept of operation similar to a linear variable differential transformer (LVDT) [5], and also to an eddy current sensor [6–8]. The sensor is scaled to a dimension of a typical integrated circuit (several square millimeters). The design of the microtransformer arrangement used in the sensor is shown in Figure 1.

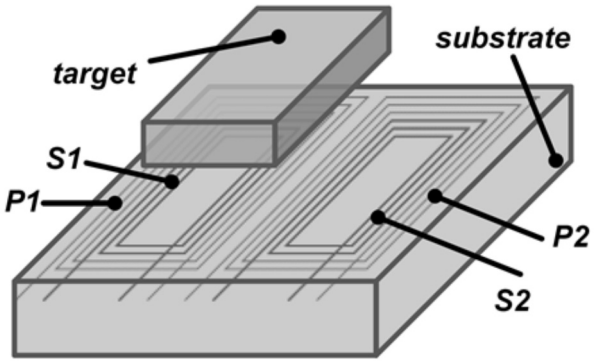


Figure 1: The structure of the discussed sensor, comprising two microtransformers, P denoting a primary winding and S denoting a secondary winding.

Figure 2 explains the differential operation of the microtransformer. When the full half-period of the ferromagnetic scale is positioned centrally over the first microtransformer, the coupling between the primary and the secondary is the strongest for this microtransformer. Contrarily, the coupling is then the weakest for the second microtransformer as the void half-period is positioned over it. The differential voltage V_{diff} of the microtransformer pair is obtained by subtracting the secondary voltages of microtransformers V_a and V_b [8]. In the described situation, V_{diff} amplitude is maximal. As the scale moves, the outputs change periodically. It should be noted that for a conductive (non-ferromagnetic) scale, the operation is adversary [7], shifting the signals for 180°; when a microtransformer is completely covered with a part of metal, its induced voltage is minimal due to eddy-current dissipation of the field energy in the scale.

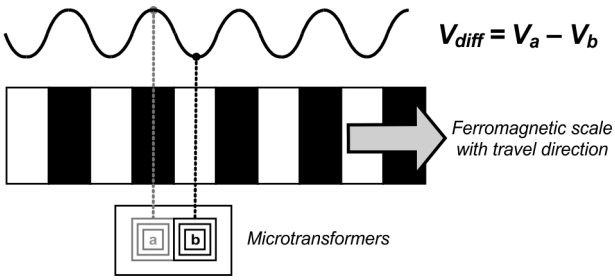


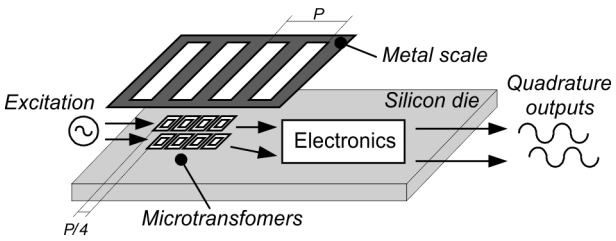
Figure 2: The differential operation of the microtransformer.

Using the presented differential principle, the signals which are common to both microtransformers in a

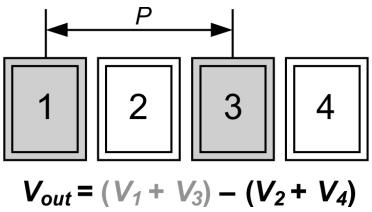
pair, e.g. electromagnetic interference and, most importantly, the capacitively transferred voltage between the primary and secondary winding, are subtracted [7]. This capacitively transferred voltage can easily exceed the inductively coupled voltage [6]. The previously described subtraction of the two signals can be carried out using either opposite connection of the secondary windings or a differential amplifier. The second option is used in the presented design, since it proves being less demanding to ensure the symmetry of the signal paths from the winding outputs to the amplifier [8].

2.2 Microsystem construction

The design of the microsystem is presented in Figure 3 (a). It consists of a silicon die comprising the microtransformers along with analog front-end electronics for the generation of the differential signal. The microtransformers are fabricated using standard CMOS technology metal layers. The total layer count is four. The typical external dimensions of the microtransformer primary and secondary windings are 755 by 500 µm and 576 by 314 µm, respectively. Therefore the adequate scale period *P* is 1 mm. Each winding of a microtransformer has 45 turns: three layers with 15 turns per layer are used, while one metal layer is used for routing the interconnections [8].



a)



b)

Figure 3: a) A block representation of the presented microsystem with a metal scale of period *P* and quadrature output signals. b) The summation scheme of the presented microsystem comprising four microtransformers per channel.

The number of the microtransformers can be increased, thus improving the signal-to-noise ratio by summing the output voltages of coils with same position inside a distinct scale period, while the primary windings are connected in parallel, thus being synchronously excited [8]. The summation scheme used in the presented system comprising four microcoils per channel is presented in Figure 3 b).

As presented in Figure 3 a), the sensor comprises two channels shifted for a quarter of the scale period, thus yielding quadrature output signals [6].

The quadrature principle is commonly employed by position encoders (e.g. optical encoders [9] and Hall sensors [10]), relying on two sensor elements with their position shifted by a half of the primary coil width (i.e. ¼ of the scale period). Quadrature signals are important since observing their phase shift allows the determination of the movement direction. Moreover, if the signals have a sinusoidal shape, the arctangent function of their amplitude ratio

$$x = \arctan\left(\frac{\sin x}{\cos x}\right) \tag{1}$$

provides the linear information about the positon *x* inside one scale period [10] .

The schematic of the integrated circuit with the realized analog front-end is shown in Figure 4. The circuit comprises operational amplifiers in the first stage (generating signals y_1 and y_2) with a DC gain of 10 and a transconductance amplifier (OTA) used for the generation of the differential signal *d* (followed by voltage buffer, which is not shown in the figure). The reason for the use of the transconductance amplifier is in its lack of need of feedback circuit, since its gain and thus the output voltage is mainly determined by the amplifier load (not shown) and its transconductance [11]. As the modulation of the signals is relatively weak (e.g. 5 % of amplitude, which, for example, results in target period full voltage swing of 250 µV at a microtransformer

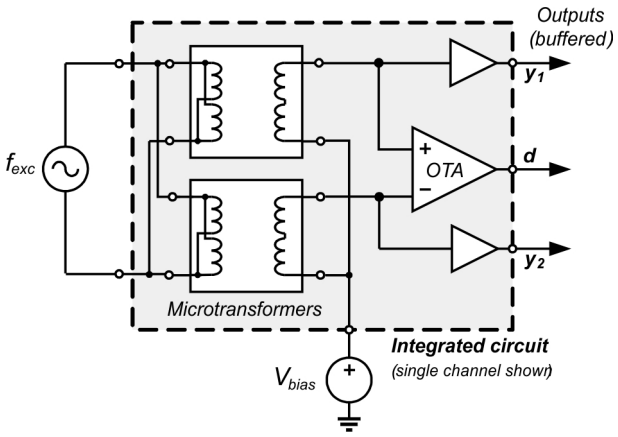
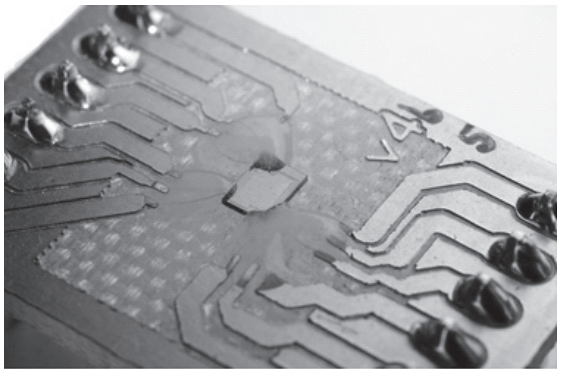


Figure 4: The block diagram of the integrated circuit, also presenting the summation scheme of the microtransformers.

output of 5 mV), the input impedance of an amplifier should remain the same for the positive (y_1) and the negative signal (y_2). The gain of the implemented OTA is in the range of 100-300, falling with the rise of the excitation signal frequency.

a)



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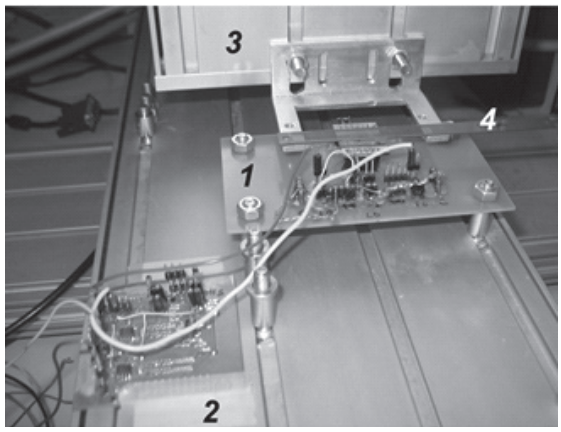

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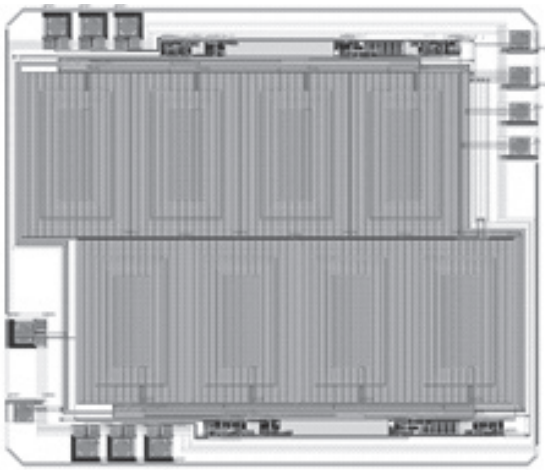

Figure 5: (a) A close photograph of the test IC on its prototype PCB board. (b) A photograph of the evaluation system comprising a two-channel IC on a mounting board (1), an external processing circuit (2), motorized mechanical manipulator (3) and the ferromagnetic target scale (4). (c) The layout of the IC, comprising eight microtransformers and the described integrated electronics.

The fabricated IC is shown mounted on a evaluation board in Figure 5 a). The complete evaluation system comprising the board is shown in Figure 5 b), while the layout of the integrated circuit is shown in Figure 5 c).

3 System evaluation

The performance of the presented version of the microsystem was evaluated using a system presented schematically in Figure 6, while its photograph is shown in Figure 5 b).

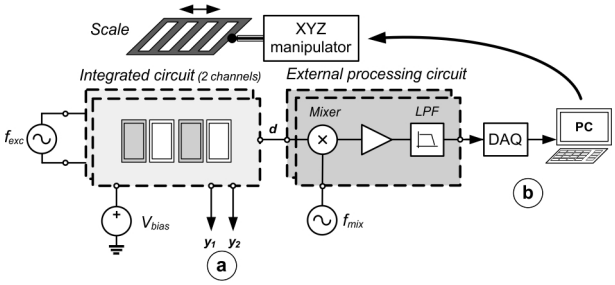

Figure 6: The microsystem evaluation configuration. The measurement setup is shown for a single channel (the IC comprises two quadrature channels).

The summed output signal of two odd-positioned microtransfomers (i.e. signal y_1 in Figure 6), amplified by a non-inverting on-chip operational amplifier with a DC gain of 10) was measured first. This measurement is represented by "a" in Figure 6. The results are graphically presented in Figure 7. The transfer characteristic of the microsystem was recorded using a network analyzer HP 3577A. The amplitude and phase characteristics (in relation to the excitation signal of 1 V) were recorded for uncovered IC ("No target"), for silicone steel (transformer core lamination sheet material of 0.35 mm thickness) and aluminum targets (a relatively large block of 0.5 mm approximate thickness). A large piece of material (i.e. at least ten times the IC area) was used as the target, completely covering the IC. The shape of the curves after 3 MHz is unrelated to the target, as the integrated amplifier transfer function starts to prevail, its pole strongly reducing the amplifier gain at higher frequencies [11]. The measurement data at 2 MHz are given in Table 1.

The sensor performance was then evaluated with a moving ferromagnetic scale (transformer core lamination sheet material of 0.35 mm thickness), perforated with void areas of 0.5 mm width (measurement "b" in Figure 6). In this evaluation, the differential sensor outputs were downmixed to a low-frequency signal which was then acquired by a computer. A photograph of the complete evaluation system is shown in Figure 5 b).

Table 1: The measured network analyzer data at 2 MHz; see Figure 7. The modulation and the phase difference are calculated relative to the "No target" situation.

Material	Amplitude [mV]	Phase [°]	Modulation M [%]	Phase difference [°]
No target	21.8	-169.3	-	-
Aluminum	19.6	-173.5	-10.1	-4.2
Steel	29.6	-164.3	35.8	5.0

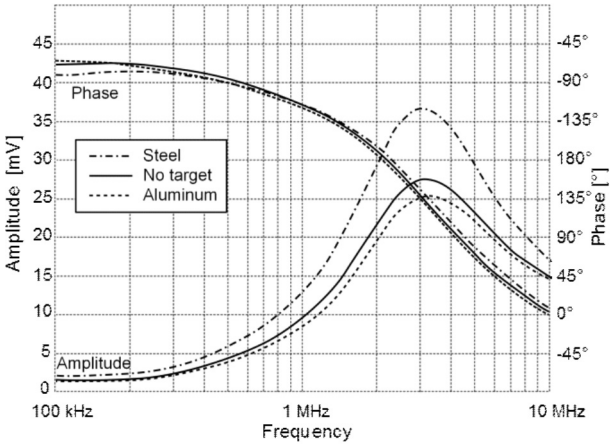

Figure 7: Network analyzer measurements of different target effects performed on a prototype microsystem.

In the reported evaluation, the excitation frequency f_{exc} was 1.8 MHz and the excitation signal was sinusoidal with 5 V_{pp}. The mixing frequency f_{mix} was 1.801 MHz, thus resulting in the output intermediate frequency (IF) of 1 kHz. This output IF signal was acquired using a 12-bit Data Acquisition (DAQ) interface. A computer (running MATLAB) was used to determine the peak-to-peak value of the voltage at each position of the scale, which is graphically presented in Figure 8. The scale position was also controlled by the computer through a motorized manipulator with a PC interface. The positioning step was 100 µm. Figure 8 presents the evaluation results for three samples of the IC prototype. Two quadrature channels were measured. In both described measurements, the distance between the silicon die surface and the scale was approximately 200-300 µm. This distance is determined by the height of bonding wires connecting the IC to its prototype board (Figure 5 (a)), which are covered with a gel protective coating, as they need to be mechanically protected from tearing.

A rectified signal shape with an offset, as well as large differences between the two channels on a same IC and also between the samples are evident from Figure 8, especially in the second measurement channel. To understand the sources of this signal shape, the modeling of the scale modulation was carried out, which is presented in the next chapter.

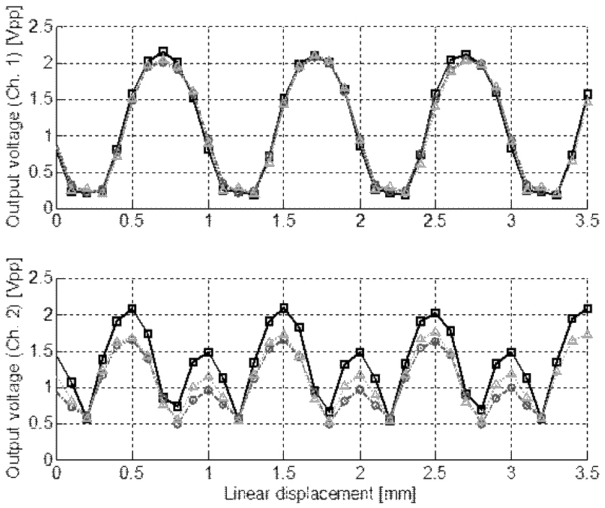

Figure 8: The recorded dependence between the linear displacement and the output voltage for three IC samples and for the two channels on each IC. Linear interpolation between the points is used.

4 The modeling of the scale modulation

The effect of the target is modeled by amplitude modulation of the excitation signal (also named the carrier signal) with a frequency f_{exc}. A frequency 100 times lower than the carrier frequency is chosen as the modulation frequency. In a physical system, this frequency ratio could be much higher – the modulation signal can be also thought of as a static (DC) multiplication signal, when the system is not in the movement. Actually, the modulation signal's periodicity and the actual shape are associated to the physical structure and the position of the scale. In this analysis, the sinusoidal modulation is transformed into the time domain as an arbitrary frequency signal for modeling purposes.

Two counterphase modulated signals y_1 and y_2 with amplitudes A_1 and A_2 (representing the positive and the negative microtransformer outputs), are used as the representation of the microtransformer output signals.

$$y_1 = A_1\left(1+m_1\sin\left(2\pi f_m t+\varphi_{m1}\right)\right)\sin\left(2\pi f_c t+\varphi_{c1}\right) \quad (2)$$

$$y_2 = A_2\left(1-m_2\sin\left(2\pi f_m t+\varphi_{m2}\right)\right)\sin\left(2\pi f_c t+\varphi_{c2}\right) \quad (3)$$

The modulation indices m_1 and m_2 correspond to the intensity of the modulation. The phase shift angles φ_{xx} of the carrier and modulation signals are also included in the equations. Then, the output signal is obtained as the difference between the two microtransformer output signals:

$$d = y_1 - y_2 \tag{4}$$

It is necessary to remark that the amplifier also produces gain, while this is not significant to this analysis.

Supposing all phase angles φ_{xx} in Equations (2) and (3) are zero, and the modulation factor is the same for the both signals ($m_1 = m_2 = m$), Equation (4) yields through the use of prosthaphaeresis formulae:

$$\begin{aligned} d = &\left(A_1 - A_2\right)\sin\left(2\pi f_c t\right) + \\ &+ m\frac{A_1 + A_2}{2}\left(\cos\left(2\pi\left(f_c - f_m\right)t\right) - \right. \\ &\left. - \cos\left(2\pi\left(f_c + f_m\right)t\right)\right) \end{aligned} \tag{5}$$

The shape of the difference signal *d* for several illustrative combinations of the carrier signal amplitude asymmetries ($A_1 \neq A_2$) and modulation factors is shown in Figure 9. In the bottom part of the figure, it can be seen that the asymmetry has less effect on the signal shape if the modulation index is high. Contrarily, if the modulation index is low and asymmetry is strong enough (examples in the upper right quarter of the figure), the signal never reduces to zero. The shape of the curve starts to resemble a harmonic signal.

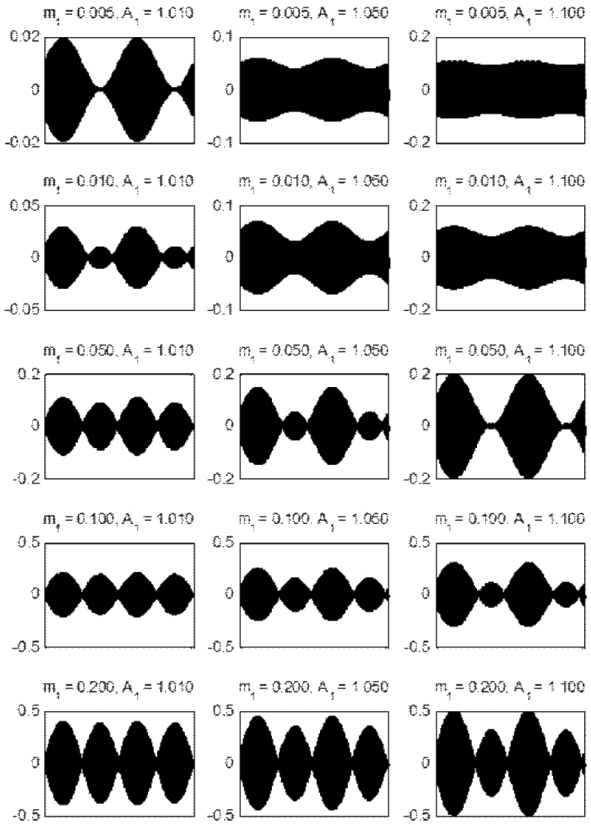

Figure 9: Examples of differential signal *d* shapes with different asymmetries and modulation factors. A_1 and m_1 are varied, while A_2 and m_2 are set to 1.

The analysis was carried out using sinusoidal modulation functions, since the shape of the measured signals (Figure 8) resembled a (rectified) sinusoidal. However it has been proven valid also for other shapes of modulation functions, e.g. triangular. It is also necessary to remark that the asymmetry of the modulation indices ($m_1 \neq m_2$) has a similar effect on the shape of the difference signal as the amplitude asymmetry ($A_1 \neq A_2$).

The measurements on the fabricated prototypes (presented in Figure 7 and Table 1) show that the phase of the signals y_1 and y_2 also changes in the presence of the target. Therefore, in reality, a combination of amplitude and phase modulation is present, introducing distortions in the envelope of the difference signal, which is desired to have a shape as close to sinusoidal as possible. The reason for this is in the method for the calculation of the position using the arctangent function (Equation 1). Evidently, expression (5) would be considerably more complex if it also accounted for the phase differences and additional real effects, such as non-symmetric target scale geometry and especially the scale misalignment, which would introduce the modulation factor asymmetry.

5 Conclusion

The paper first presented the basic concept of inductive sensors for position measurement and some disadvantages of conventional position encoders which can be alleviated using the proposed integrated sensor concept. The presented design has the sensing elements (i.e. the microtransformers) integrated along with the analog front-end, using the identical metal layers as the CMOS circuits, which differs from the previous work [12,13]. The system design and operation were presented and supported with measurements on fabricated prototypes. The measurements have shown the feasibility of the design, confirming the appropriateness of the proposed sensor design for an ASIC realization. The expected modulation characteristics for both ferromagnetic and conductive targets were experimentally demonstrated using solid targets covering the entire microsystem.

Further evaluation using a measurement scale has shown the need for the investigation of the modulation effects of the difference signal. The signal has a shape of a pulsating curve, which is heavily dependent on the asymmetry between the two signals subtracted in the process of differential signal generation. The

signal needs further processing to be converted into a smooth sinusoidal signal, which will allow the determination of the linear position from the quadrature signals using arctangent interpolation, as described in [8].

6 Acknowledgments

The authors thank to Boštjan Fink and Daniele Bertocchi for preparing the layout of prototype integrated circuits and to the remaining staff of the LMFE Laboratory and Letrika Lab d.o.o. for fruitful discussions, support and pleasant working atmosphere.

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Arrived: 31. 12. 2015
Accepted: 26. 04. 2016

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 1(2016), 36 – 41

A 3.0 – 3.6 GHz LC-VCO with ETSPC Frequency Divider in 0.18-micron CMOS technology

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Abstract: This paper proposes the design, implementation, and measurement of a fully integrated voltage controlled oscillator (VCO) and frequency divider for multi-band transceivers in 0.18-micron IBM 7RF CMOS technology. The VCO is composed of a cross-coupled NMOS transistor-pair and LC tank as a core circuit and 4-bit digitally-switched capacitor block with linearly varying varactors for enhancement of the wide oscillation frequency bandwidth. A design of frequency divider is based on extended true-single-phase-clock (ETSPC) flip-flops with divide values ranging from 2 to 256 for very wide output frequency range. The measured results indicate that the LC-VCO frequency range is from 3.02 GHz to 3.55 GHz, and the phase noise is -108.89 dBc/Hz at 1 MHz offset from 3.55 GHz carrier. The power consumption of the LC-VCO with ETSPC frequency divider including all the buffers and other circuits is about 212 mW for 2.49 dBm of output power. The active area of the test chip occupies only 0.65×0.65 mm^2 and the whole chip size including the ESD protection circuits and pads is 1.5×1.5 mm^2.

Keywords: Frequency divider; integrated circuits (IC); phase noise; transceivers; tuning range; voltage controlled oscillator (VCO).

3.0 – 3.6 GHz LC-VCO z ETSPC frekvenčnim delilnikov v 0.18 mikronski CMOS tehnologiji

Izvleček: Članek obravnava dizajn, implementacijo in meritve polno integriranega napetostno krmiljenega oscilatorja (VCO) in frekvenčnega delilnika za več pasovne sprejemno oddajne enote v 0.18 mikronski IBM 7BF CMOS tehnologiji. VCO je sestavljen iz sklopljenega para NMOS tranzistorjev, vezja LC, 4 bitnega digitalno preklopnega kondenzatorskega bloka z linearno spremenljivo kapacitivnostjo za izboljšanje frekvenčnega območja oscilatorja. Frekvenčni delilnik temelji na razširjenem ETSPC flip flopu v razponu vrednosti od 2 do 256. Merive izkazujejo frekvenčno območje LC-VCO od 3.02 – 3.55 GHz in fazni šum -108.89 dBc/Hz pri 1 MHz odmika od nosilne frekvence 3.55 GHz. Poraba moči LC-VCO skupaj s frekvenčnim delilnikom in ostalim vezjem je 212 mW pri 2.49 dBm izhodne moči. Aktivna površina čipa je 0.65×0.65 mm^2, celotno vezje pa 1.5×1.5 mm^2

Ključne besede: frekvenčni delilnik; integrirana vezja; fazni šum; sprejemno oddajna enota; nastavljivo območje; napetostno krmiljen oscilator

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1 Introduction

With the rapid growth of wireless communication systems, standards, and very wide frequency bands, the demand of fully-integrated, multi-band, multi-standard RF transceivers becomes significant in recent years [1], [2]. Existing multi-band, multi-standard RF transceivers provide a variety of services ranging from basic mobile telephony to ubiquitous broadband internet access. However, most modern multi-band, multi-standard RF transceiver architectures consist of several LNAs, LC-VCOs, PLLs, Mixers, and PAs for each frequency band. For this reason, it leads to large chip area, high cost, and high power consumption. Therefore, IC designers encounter many challenges in developing new architectures of the basic blocks of multi-band, multi-standard RF transceivers.

In a RF transceivers, a voltage-controlled oscillator (VCO) is a crucial building block that is used as local oscillator in high-frequency phase locked loops (PLLs) whose output is used to up- and down-convert signals. In general, high-frequency VCOs can be classified into two main types: the ring-VCO and the LC-VCO. The ring-VCOs occupy a small chip area and offer a wide tuning range. Despite these advantages, LC-VCOs are more common in high performance transceiver chips due to

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usually better phase noise performance, lower power consumption and less sensitive to temperature- and supply-variations compared to ring-VCOs. For these reasons, in this paper the LC-VCO is designed.

Another challenge for designers of RF transceivers is high frequency clock division. Common types of clock dividers, such as CML, are becoming inefficient with rapid improvement of CMOS technologies [3], [4]. The true-single-phase-clock (TSPC) and extended TSPC (ETSPC) topologies are becoming more popular because of lower occupied chip area and power consumption [5]. Therefore high-speed ETSPC frequency divider is employed in proposed design.

The goal of this work is the design, implementation and experimental characterization of a 3.0 – 3.6 GHz LC-based VCO and and its output frequency ETSPC divider with divide values ranging from 2 to 256, in a 0.18 µm IBM 7RF CMOS technology. The reconfigurable LC tank can simply adjust oscillation frequency of VCO by the combination of a digitally-switched capacitors for coarse frequency tuning and tuned varactor blocks for fine tuning. This architecture and wide range of divide values make this LC-VCO suitable to multi-band, multi-standard RF transceivers.

This paper is organized as follows: Section 2 describes the analysis of the proposed 3.0 – 3.6 GHz LC-VCO architecture and design of circuits. In Section 3, the design of the divide-by-2…256 frequency ETSPC frequency divider is given. The following Section 4 describes the measurement results, and finally, Section 5 summarizes the most important conclusions of this work.

2 LC-LDO Architecture

Fig. 1 shows the proposed LC-VCO architecture, which consists of the following elements: LC-VCO circuit with digitally-switched capacitor and tuned varactor blocks, DC decoupling stage, differential to single-ended stage, and output buffer. Each of these elements are discussed in more detail below.

LC-VCO core circuit. Fig. 1 also shows a differential-pair negative-impedance LC-VCO circuit, which provides better phase noise characteristics and faster switching of the cross-coupled NMOS differential pair [6]-[8]. The proposed LCVCO consists of the following elements: high-quality inductor (L), digitally-switched capacitors block, varactors block, cross-coupled transistors. The cross-coupled pair consists of NMOS transistors M1 and M2, and generates the negative impedance to cancel the energy loss in the LC tank. The inductor of the LC tank is realized using a two turn spiral differential inductor of 1.97 nH.

Frequency tuning is achieved by two steps: coarse-tuning through a digitally-switched capacitor block and the fine-tuning by the bias of varactors block from the node V_{tune}. In this design, a 4-bit switched capacitor block is used. The block consists of 4 arrays of capacitors connected in parallel, which individually can be turned on or off depending on the required capacity. All switches, that used to turn on or off capacitors, are realized using NMOS transistors. Thus, the sixteen curves of the sub-band cover the wide frequency range.

The fine-tuning is obtained using the varactors block in order to get more precise operation frequency. This block consists of matrix of 12×2 parallel connected multi-finger structure NMOS varactors to enhance the Q-factor and to maximize the tunability of the proposed LC-VCO. The external voltage V_{tune} is used for linear variation of the equivalent capacitance of NMOS varactors.

Similar architectures of the LC-VCO are presented in our previous works and the work of others [9]-[12].

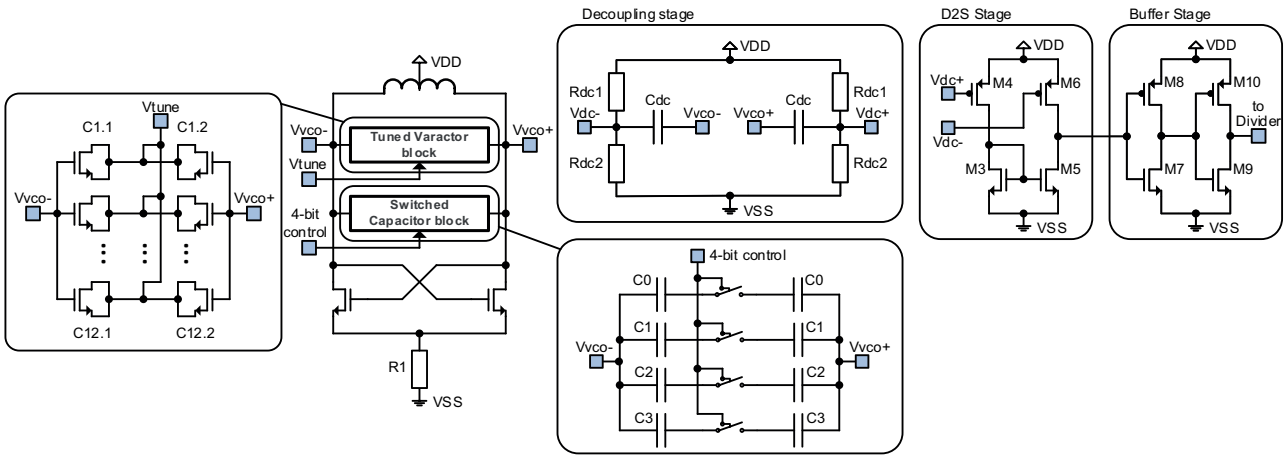


Figure 1: The proposed LC-VCO architecture

DC decoupling stage. The DC output of this proposed LC-VCO topology is biased at V_{DD} through the inductor, so that the output swing of the LC-VCO can reach as high as twice V_{DD}. For this reason, this architecture requires the DC decoupling circuit. The decoupling capacitors C_{dc} removes the DC voltage at the output of the proposed LC-VCO, and the resistances R_{dc} fixes the DC voltage at the input of the differential to single-ended stage circuit.

Differential to single-ended stage. The proposed LC-VCO circuit is implemented with a differential to singleended (D2S) converter. Since input of the frequency divider is single-ended and the LC-VCO output is differential, D2S converter is used as interface between two circuits. This D2S circuit converts the differential signal to single output and produce waveforms that swing rail-to-rail.

Buffer stage. The proposed LC-VCO circuit includes also a buffer stage to drive large capacitive loads with high speed, to increase high input-output isolation and wide output swing range.

3 Frequency Divider

The frequency divider operates at high frequency, equal to the frequency of signal, generated by the LC-VCO. It results in increased chip power consumption. So choosing topology of main block in the divider – flip-flop, is classical engineering task – searching of compromise between operating frequency and power consumption.

There are many suitable topologies of CMOS Flip-flops, which can achieve high operating frequency. Most common are Razavi [3], Wang [4] and CML topologies. Disadvantage of these circuits are high power consumption. In recent years, because of CMOS technology scaling, true-single-phase-clock (TSPC) and extended TSPC (ETSPC) topologies are becoming more popular choice for flip-flops, working at multi-gigahertz frequencies. Advantage of these flip-flops are much simpler schematics and low power dissipation. [13] extensively covers different TSPC and ETSPC structures.

In this paper proposed divide-by-N (where N = 2, 4, 8, 16, 32, 64, 128, 256) frequency divider is based on ETSPC flip-flops. Structure of this divider is shown in Fig. 2. It is made of eight divide-by-2 divider stages, connected in daisy-chain.

Each divide-by-2 divider stage lowers frequency of the signal by half, also relaxing requirements for following divider. So three different divide-by-2 dividers are used: first flip-flop, operating at highest frequency (Fig. 2 [H]), 2nd and 3rd dividers, operating at intermediate frequency (Fig. 2, [I]), and 4th – 8th dividers working at low frequencies (Fig. 2, [L]). Usage of different dividers in daisy-chain allows minimization of power consumption and occupied chip area.

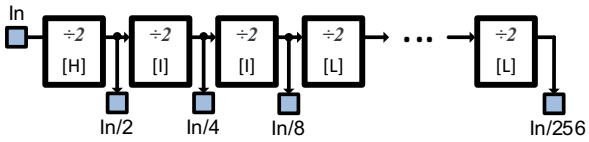


Figure 2: Structure of divide-by-N frequency divider. ÷2 [H]– divideby2 divider working at highest frequency, ÷2 [I]– divideby2 divider working at intermediate frequency, ÷2 [L]– divideby2 divider working at low frequency. In – input signal, In/N– input signal divided by N, where N = 2, 4, 8, 16, 32, 64, 128, 256

Schematics of divide-by-2 dividers are shown in Fig. 3. All divider stages share same structure. Different operating frequency is achieved by different transistor sizing.

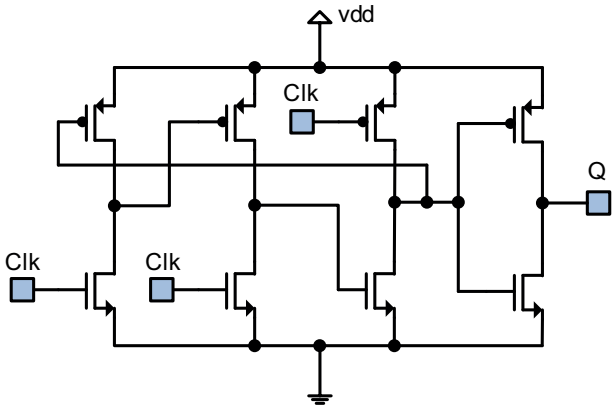


Figure 3: Structure of ETSPC divide-by-2 frequency divider. Clk – input signal. Q – divided by 2 output signal

As we can see from the schematics, ETSPC divider consists of three branches (ETSPC flip-flop), made of two transistors, and output inverter. This inverter is used, because minimal configuration of ETSPC flip-flop has only inversed output. Output inverter also serves as output buffer. Inversed output is connected to the input of the flipflop, hence clock division by 2 is achieved.

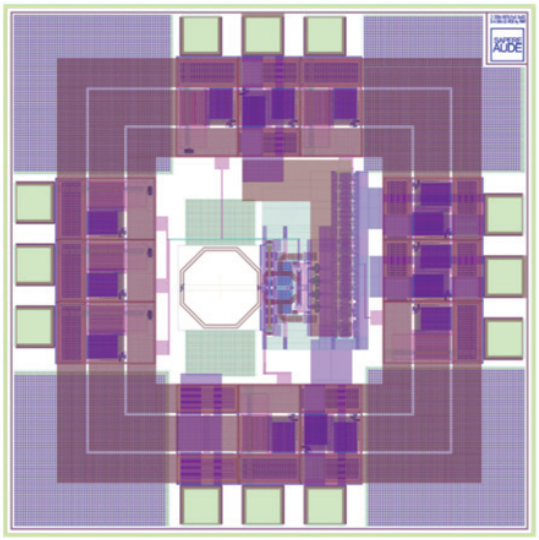
It is also seen from Fig. 3, that there can be situations, when both transistors of branches, consisting clock transistor, are open during half of the clock period. In such situation, output level of the branch is determined by ratio of PMOS and NMOS transistor sizes. This means, that static power dissipation exists in ETSPC flip-flops and it is higher at lower input frequencies.

4 Measurement Results

The proposed LC-VCO with frequency divider chip was designed and fabricated in a 0.18 µm IBM 7RF CMOS technology. The layout and micro-photography of the chip is shown in Fig. 4. The total chip area, including the ESD protection circuits and pads, is 1.5×1.5 mm^2, where the active area occupies only 0.65×0.65 mm^2. The chip was packaged in a 12-pin OCP-QFN package. For testing and measurement purposes, the chip was assembled with standard SMD reflow and chip-on-board technology on Rogers RO4000 high frequency laminate.

It should be noted that all measurement results, which presented in this paper are obtained when division ratio of the ETSPC frequency divider is 8.

a)



b)

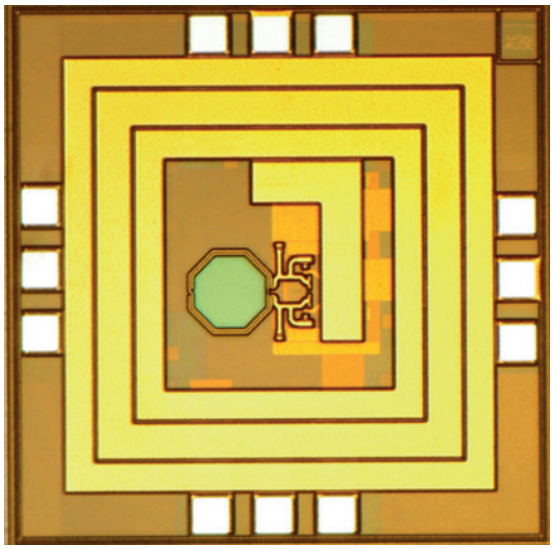


Figure 4: The layout (a) and micro-photograph picture (b) of the proposed LC-VCO with frequency divider

The measured tuning characteristics of the proposed LCVCO with frequency divider, when changing the V_{tune} voltage and the digitally switched capacitor block code, are shown in Fig. 5. These characteristics were obtained by multiplying the measurement results of 8. The tuning range extends from 3.02 GHz up to 3.55 GHz among 16 subbands. With a tuning voltage V_{tune} ranging from 0 V to 2.5 V, the upper sub-band achieves a tuning range from 3.44 GHz to 3.55 GHz and the lower sub-band achieves a tuning range from 3.02 GHz to 3.09 GHz.

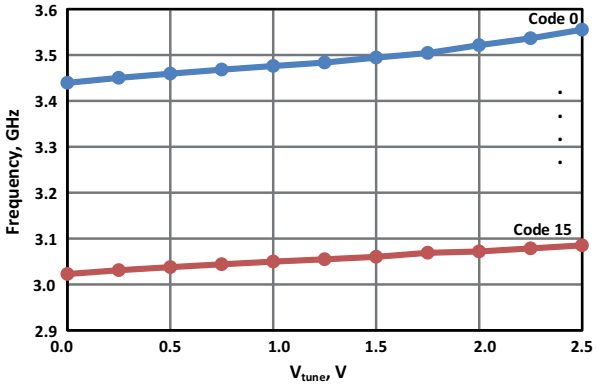


Figure 5: The measured tuning range of the proposed LC-VCO with frequency divider

Fig. 6 shows the measured frequency spectrum of the proposed LC-VCO with frequency divider, when V_{tune} = 2.5 V and the code of digitally-switched capacitor block is set to 0. This combination gives the highest possible frequency of the LC-VCO tuning range. All measurements were performed using a Tektronix RSA5126B real-time spectrum analyzer. The output power spectrum at divide-by-8 output frequency of 444.38 MHz is about 2.49 dBm.

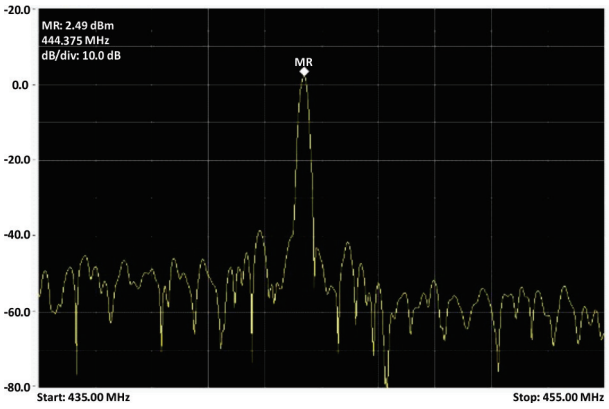


Figure 6: The measured frequency spectrum, when V_{tune} = 2.5 V and the switched capacitor block code = 0

Fig. 7 shows the measured phase noise. The phase noise is about -108.89 dBc/Hz at 1 MHz offset from 3.6 GHz carrier. A summary of the measurement results are shown in Table 1.

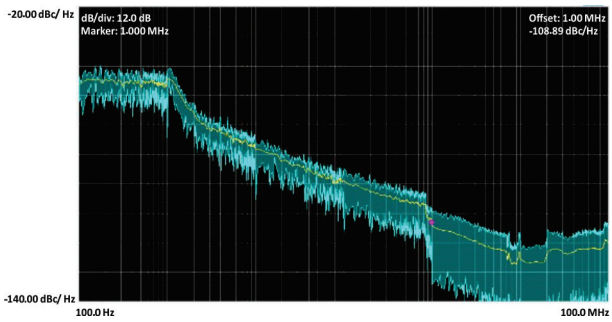


Figure 7: The measured phase noise, when V_{tune} = 2.5 V and the switched capacitor block code = 0

Table 1: Performance summary of the LC-VCO with frequency divider

Characteristics	Value
Technology	0.18 µm RF CMOS
Supply Voltage	2.5 V
Operating Current	85 mA
LC-VCO Tuning Range	3.02 GHz ~ 3.55 GHz
Phase Noise @ 1MHz Offset from 3.6 GHz carrier	-108.89 dBc/Hz
Active area of the test chip	0.65×0.65 mm2

5 Conclusions

A fully integrated 3.0 – 3.6 GHz LC-VCO with an ETSPC frequency *divider* is designed and fabricated in a 0.18 µm IBM 7RF CMOS technology. The total chip area, including the ESD protection circuits and pads, is 1.5×1.5 mm^2. The active part of this fabricated chip occupies *only* 0.65×0.65 mm^2. Using 4-bit switched capacitor block and linearly varying varactors, the LC-VCO achieves a tuning range from 3.02 GHz to 3.55 GHz. The output signal of the LC-VCO is divided down through ETSPC divider, with divide values ranging from 2 to 256. The measurement results of the proposed LC-VCO with frequency divider show a phase noise better than -108.89 dBc/Hz @ 1 MHz offset from 3.6 GHz carrier and a total power consumption of about 212 mW for 2.49 dBm of output power.

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Arrived: 21. 01. 2016
Accepted: 26. 04. 2016

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 1(2016), 42 – 52

Prediction of Radiated Emissions of Automotive Electronics Early in the Design Phase based on Automotive Component Level Testing

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Abstract: A method of predicting radiated emissions levels of automotive component level testing in the early design phase of an automotive electronics from a cable harness is presented. Instead of the time consuming and inaccurate common-mode current measurements on a cable harness with a radio frequency (RF) current probe, this paper proposes a novel common-mode current distribution prediction on a cable harness with the multi conductor transmission line model from imported boundary line currents or voltages from an electromagnetic (EM) simulator taking into the consideration a printed circuit board (PCB) layout and components, connectors, 2 D model of cable harness, cable harness loads etc. Radiated emissions levels are calculated from predicted common-mode current distribution on cable harness. This paper uses a component level CISPR25 cable harness layout for radiated emissions levels prediction. A radiated emissions prediction model enables an engineer to evaluate radiated emissions levels in the early design phase, when the product is still in the design phase prior to the first available prototype. As a result, radiated emissions levels can be optimised and lower cost solution can be obtained. This approach lowers the overall cost and time needed for automotive component design. The model substitutes a 3D model of cable harness above the ground plane in EM simulator and is thus much faster and uses less resources with same or even better prediction accuracy. The proposed method is validated in two absorber lined shielded enclosures (ALSE) both with an accreditation according to ISO/IEC 17025. The differences between prediction and measurements in both ALSE are explained.

Keywords: cable harness; CISPR25; common-mode current; EMC; radiated emissions

Ocena nivojev sevalnih emisij avtomobilske elektronike v zgodnji fazi njenega razvoja na podlagi testiranja avtomobilskih komponent

Izvleček: Predstavljena je metoda za oceno nivojev sevalnih emisij ožičenja avtomobilske elektronike na podlagi testiranja avtomobilskih komponent v zgodnji fazi razvoja. Namesto časovno potratnega in netočnega merjenja porazdelitve sofaznega toka na ožičenju z uporabo radio frekvenčne (RF) tokovne sonde, predlagamo metodo za oceno porazdelitve sofaznega toka na ožičenju z uporabo teorije več vodniških prenosnih linij in uvoženih robnih linijskih tokov ali napetosti iz elektromagnetnega (EM) simulatorja z vključenimi vplivi tiskanega vezja in njegovih gradnikov, priključkov, 2D modela ožičenja, bremen ožičenja itd. Nivoji sevalnih emisij so izračunani iz ocene porazdelitve sofaznega toka na ožičenju. Model za oceno nivojev sevalnih emisij je zgrajen na podlagi merilne postavitve ožičenja avtomobilske komponente iz standarda CISPR25. Model omogoča inženirjem oceno nivojev sevalnih emisij v zgodnji fazi razvoja, ko prototipi elektronike niso še na voljo. Na podlagi rezultatov je mogoča optimizacija nivojev sevalnih emisij in doseg najcenejšega dizajna elektronike. Takšen pristop omogoča nižje stroške in manj vloženega časa za načrtovanje elektromagnetno združljive avtomobilske elektronike. Predlagani model je hitrejši, potrebuje manj resursov z enako ali boljšo točnostjo kot 3D model ožičenja nad prevodno ploščo v EM simulatorju. Predlagani model smo preverili v dveh pol neodbojnih sobah, katere so akreditirane po standardu ISO/IEC 17025. Razlike med oceno in meritvami v obeh pol neodbojnih sobah smo pojasnili.

Ključne besede: ožičenje; CISPR25; sofazni tok; EMC; sevalne emisije

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1 Introduction

An electronic device has to be designed according to electrical, thermal, mechanical, functional and safety requirements. An automotive electronic device has to withstand extreme temperature conditions, temperature shocks, humidity, chemicals, mechanical shocks etc. In spite of high requirements the final product has to be inexpensive, reliable, safe and with low power consumption. The final product also has to pass the component level testing for electromagnetic compatibility (EMC). One among several EMC component level tests is also the radiated emissions measurement using antennas in an absorber lined shielded enclosure (ALSE) according to the standard CISPR 25 [1], which specifies the limits and methods of measurement for the protection of vehicles on-board receivers. In order for the product to pass the radiated emissions testing, the measured radiated emissions levels have to be below the automotive OEM specified limits in the frequency range from 150 kHz to a few GHz. Measuring radiated emissions only on the final product is risky and expensive, since about 90% of the products fail on the first radiated emissions measurements. Radiated emissions measurements conducted in the early design phase, before the testing phase, enable the designer to implement measures to reduce radiated emissions more easily, with a lower impact on the overall product cost.

Automotive OEM's specify the strictest (lowest) limit lines for radiated emissions in a frequency range from 30 MHz up to 500 MHz. The main reason for automotive OEM's high requirements for low levels of radiated emissions in this frequency range is to keep the receivers communication in these bands (e.g. 2m TAXI band, FM radio, etc.) interference-free from vehicle on-board electronics.

In the frequency range 30 MHz – 500 MHz printed circuit board (PCB) traces are small compared to the wavelength and cannot radiate efficiently. A cable harness length comparable to the electromagnetic field wavelength in a free space radiates efficiently. Common-mode currents on a cable harness have already been proven to cause the highest radiated emissions [2].

Various methods for predicting the radiated emissions from a cable harness carrying common-mode currents were already presented in [3–6]. The goal of the methods was to measure the common-mode current distribution on a cable harness in the laboratory, and to predict the radiated emissions from the measured common-mode currents. Using these methods, radiated emissions measurements in an expensive ALSE are not needed in the design phase.

The approach presented in [3] predicts the radiated emissions using multiple transfer functions, which relates the measured common-mode current distribution on a cable harness and the measured radiated emissions with an antenna. The approach takes into consideration the effect of an ALSE, test setup and an antenna on levels of radiated emissions. The calculation is only valid for an ALSE and an antenna used in the paper in frequency range from 30 MHz to 125 MHz.

The method presented in [4] specified in CISPR 25, is commonly used for emission measurements. Components or modules are required to be connected with a test cable bundle for evaluating radiated emissions. The radiation is often mainly dominated by the common mode current along the cable bundle. In order to predict radiated emissions from setups according to ALSE method, without using a large anechoic chamber, this paper presents an alternative and innovative method. The presented approach determines radiated fields from a cable bundle without phase information. It is only based on the amplitude of common mode current from phaseless measurements using a RF current probe. Firstly, radiation model of a cable bundle is simplified to a single equivalent transmission line (TL predicts radiated emissions by measuring the common-mode currents distribution on a cable harness. Common-mode current amplitude is measured along the cable harness with an RF current probe. The common-mode current phase is calculated from the measured common-mode amplitude with phase retrieval algorithm. Radiated emissions are calculated by splitting the cable harness to infinitesimal Hertzian dipoles and summing the contribution of all Hertzian dipoles at the antenna tip. The effect of the ground plane on levels of radiated emissions is taken into account by using the mirror method of Hertzian dipoles. The proposed method suffers from errors in the phase retrieval algorithm, especially in the lower frequency range. The same authors improved the calculation of the radiated emissions from the common-mode current distribution in [5]. A major improvement is related to the levels of radiated emissions in horizontal antenna polarization by implementing a method of calculating the current distribution on the surface of the ground plane. In this way the effect of the finite size of the ground plane on the levels of radiated emissions is considered. The same authors again improved the calculation of radiated emissions in [6]. The authors propose current scanning in the time domain to improve the phase retrieval algorithm in the lower frequency range. In addition, a prediction of radiated emissions is also improved by considering the ALSE and antenna effects with a calibration procedure.

The disadvantage of all the previous methods is the need for common-mode current distribution measurement, which can be time consuming and requires additional equipment for RF current probe positioning. An RF current probe also adds insertion impedance to the cable harness common-mode impedance and thus influences measurement results [7]. The RF current probe positioning on the cable harness affects the accuracy of common-mode current distribution. The method also cannot be used in the early design phase, when a prototype is not yet available.

The common error of the presented papers is also in modelling the straight cable harness 10 cm from the ground plane front edge, without the 90 degrees bends, which is not equal to the cable harness layout as specified in the CISPR25 [1]. This cable layout [3–6], which is not according to the standard, is illustrated in fig. 1.

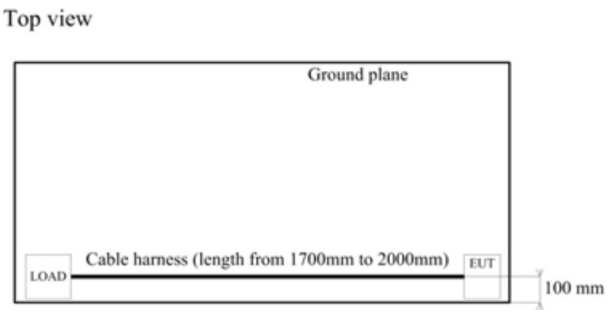

Figure 1: Straight cable harness located 100 mm from the front edge of the ground plane.

It is well known that a cable harness layout has an impact on radiated emissions levels.

This paper presents a method of predicting radiated emissions levels of automotive component level testing in the early design phase of a product. The cable harness currents and voltages are imported from an EM simulator taking into the consideration a PCB layout and components, cable harness connector, 2D model of the cable harness, cable harness loads (artificial load for power supply lines, load simulators for data/signal lines). The model predicts a common-mode current distribution on a cable harness using the multi conductor transmission lines (MTL) method and boundary line currents or voltages imported from an EM simulator. The cable harness is divided into infinitesimal current elements (Hertzian dipoles), which represent a radiating structure. Vertical grounding connections are also added to the radiating structure. The cable harness layout, as specified in the CISPR25 [1], is modelled in this paper.

Sections of the rest of the paper are organized in the following manner. Section II introduces the CISPR25 test setup as the basis for the radiated emissions prediction model in section III. Prediction of the common-mode current distribution on the cable harness is presented in section IV. Proposed radiated emissions prediction model is validated in section V. Simulation results are compared with the radiated emissions and common-mode current measurements in two semi-anechoic chambers. The conclusion is presented in Section VI.

2 CISPR25 test setup

Fig. 2 shows a test setup for automotive radiated emissions measurements according to CISPR25 [1] in the lowest frequency range 150 kHz – 30 MHz using a rod antenna. Fig. 3 also shows the test setup for automotive radiated emissions measurement according to CISPR25 [1], but in the frequency range of 30 MHz – 1000 MHz using a logarithmic antenna. The difference between both setups is only in the type of the antenna. Radiated emissions are measured with a rod antenna only in vertical polarization, while with a logarithmic antenna measurements are done with both horizontal and vertical antenna polarization.

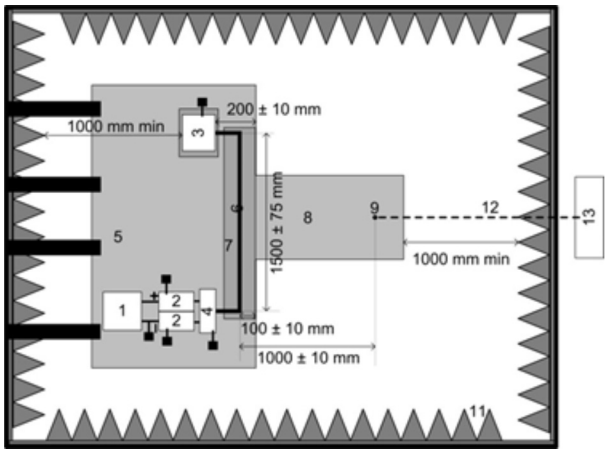

Figure 2: Test setup for radiated emissions measurements from an automotive component with an attached cable harness according to CISPR25 [1] in the frequency range of 150 kHz – 30 MHz using a rod antenna.

Test setup according to CISPR25 [1] has to be known down to details in order to be able to build a good simulation model for predicting radiated emissions levels in automotive component level testing.

3 Radiated emissions prediction model

The radiated emissions prediction model consists of a large number of Hertzian dipoles, which represents the

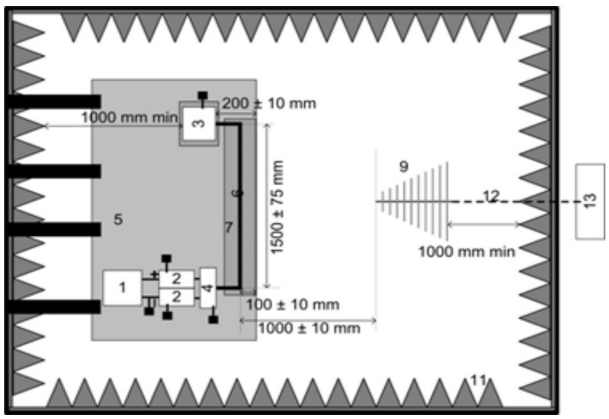

Figure 3: Test setup for radiated emissions measurements from an automotive component with an attached cable harness according to CISPR25 [1] in the frequency range of 30 MHz – 1000 MHz using a logarithmic antenna.

structures, where the currents are flowing. A Hertzian dipole is a current element with a length small enough to have a constant current amplitude along its length at the highest frequency of interest. The Hertzian dipole radiated fields (electric and magnetic fields) equations in a Cartesian coordinate system in the frequency domain are used, which enables a simple way of summing the radiated fields in a specific point in space.

Fig. 4 shows a simplified geometry of the cable harness with the vertical ground connections to the ground plane and the ground plane created according to CISPR25 [1] that enables calculation of radiated emissions in the observation point – at the tip of the antenna T_{ANT}.

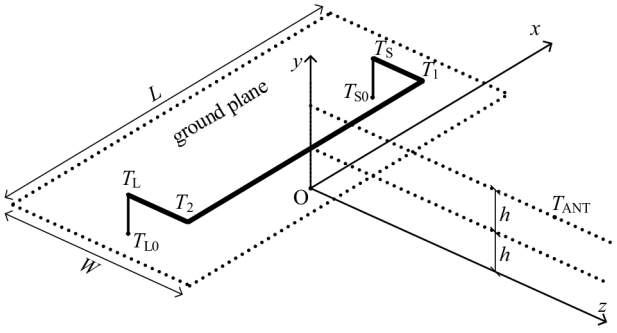

Figure 4: Simplified CISPR25 geometry used for radiated emissions calculations

The cable harness has a total length of *l*, which has to be smaller than 2000 mm according to CISPR25 [1], but according to some automotive OEM's requirements the length of the cable harness has to be in a range from 1700 mm to 2000 mm. The ground plane has a defined width *W* and length *L*. Cable harness is routed from the front side of the equipment under test (EUT) located at point T_S to load simulators located at point T_L. Detailed cable harness positioning is presented below.

The point T_S = (750, 50, -100) mm represents the EUT front side, where the cable harness starts. The point T_{S0} = (750, 0, -100) mm represents the nearest EUT connection to the ground plane, the location where the common-mode current returns back to the EUT. The cable harness first bends at the point T_1 = (750, 50, 0) mm at preferable 90 degrees according to the standard [1]. The cable harness is laid 100 mm from the front edge of the ground plane at 50 mm height above the ground plane in a total length of 1500 mm from the point T_1 to the point T_2 = (-750, 50, 0) mm. This is also the point where the second bend of the cable harness is done. The rest of the cable harness length (*l* - 1600) is then connected to the load simulators and artificial networks (ANs), at point T_L = (-750, 50, - (*l* – 1600)) mm. The grounding connection from AN or a load simulator is modelled between points T_L and T_{L0} = (-750, 0 - (*l* - 1600)) mm. Point T_{L0} is the point, where common-mode current is injected from the cable harness to the ground plane.

The cable harness is split into small segments, which are modelled as Hertzian dipoles. The Hertzian dipole current is equal to the cable harness common-mode current, where the Hertzian dipole is located on the cable harness. Vertical grounding connections at EUT from the point T_{S0} and T_S and at load simulator or AN side from points T_{L0} and T_L are also modelled as the Hertzian dipole and their current is equal to the cable harness current at each vertical grounding connection.

In order to be able to use the radiated fields' equations at an arbitrary point along the cable harness, a Cartesian coordinate system rotation has to be performed. Rotation of each Hertzian dipole Cartesian coordinates must be performed so that the direction of the Hertzian dipole is directed in the direction of the transformed z axis. In the transformed Cartesian system the radiated fields are calculated. The calculated radiated fields have to be again transformed back to the original Cartesian coordinate system, where contributions from all Hertzian dipoles are added together.

The ground plane effects to the radiated emissions can be modelled by implementing the mirror theory to the cable harness. This is done at a lower frequency range 150 kHz – 30 MHz, where the mirror theory perfectly predicts radiated emissions levels. Fig. 5 shows workflow to calculate the radiated emissions in vertical antenna polarization in the frequency range 150 kHz – 30 MHz using mirror theory.

However, mirror theory poorly predicts vertical and horizontal radiated emissions levels in the frequency range of 30 MHz – 1000 MHz, therefore radiated emissions are modelled by implementing the PO-model as was already presented in [6].

The PO model calculates the induced current (return common-mode currents) on the surface of the ground plane, due to the common-mode currents on the cable harness and mirrored cable harness [6]. The calculation is done by slicing the ground plane into small rectangular surfaces, whose dimensions are sufficiently small compared to the wavelength at the highest frequency of interest. Contribution of the current distribution on the ground plane to radiated emissions is modelled by a Hertzian dipole in each cell in x and z directions [5].

The radiated emissions levels are predicted with the highest accuracy by summing the radiated electric field due to the common-mode current in the cable harness and vertical ground connections as well as the currents on the surface of the ground plane. Fig. 6 shows workflow to calculate the radiated emissions in horizontal and vertical antenna polarization in the frequency range 30 MHz – 1000 MHz using PO model.

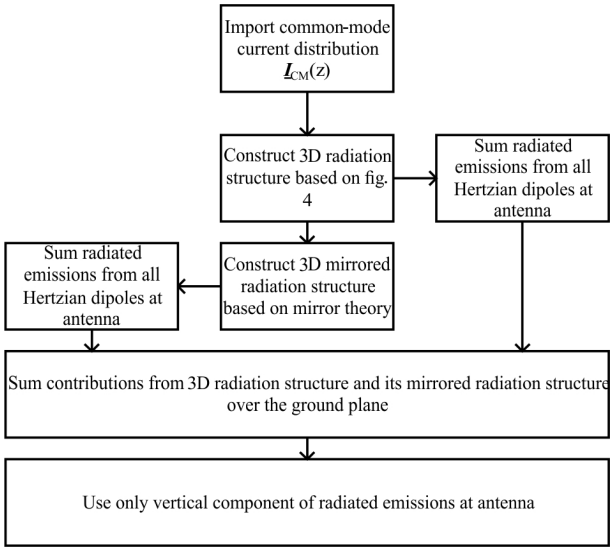

Figure 5: Workflow to calculate the radiated emissions in the frequency range 150 kHz – 30 MHz using only mirror theory.

4 Common-mode current distribution on the cable harness

Common-mode current distribution on a cable harness is predicted using the multi conductor transmission lines (MTL) model in the frequency domain [8].

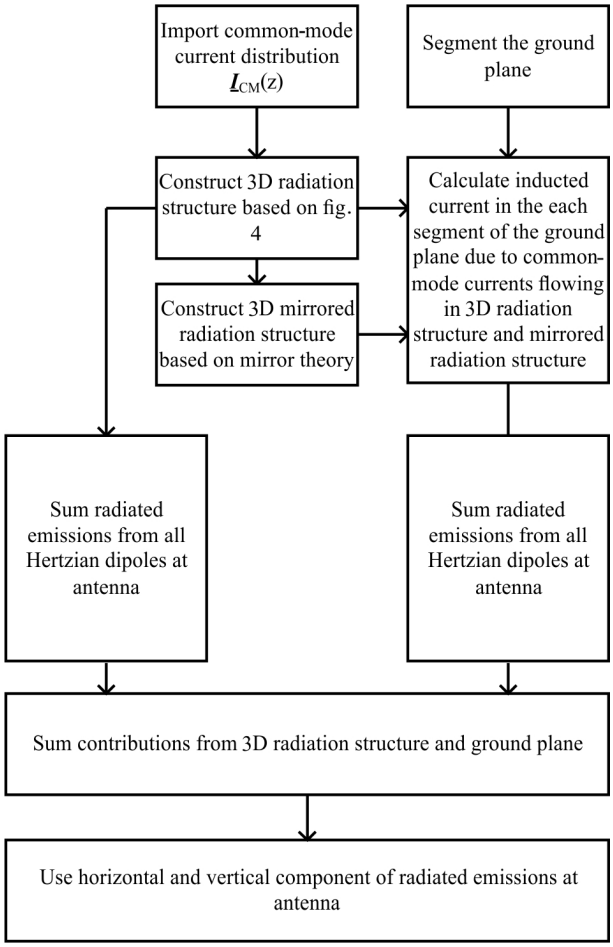

Figure 6: Workflow to calculate the radiated emissions in the frequency range 30 MHz – 1000 MHz using PO method.

Fig. 7 shows the definition of differential-mode currents (the ones with return path on the reference conductor in a cable harness) and common-mode currents (the ones with return path on the reference ground plane). This definition enables the calculation of common-mode current distribution along the cable harness with the MTL.

The height of a cable harness above the ground plane (50 mm in this case) is the limiting property for the highest frequency for which the transmission line model of the common-mode current distribution is still valid. The highest frequency for the transmission line model is around 500 MHz, where the distance of the cable harness above the ground plane violates the rule that the distance should be smaller than the wavelength, e.g. smaller than $\lambda/10$.

Transmission lines properties are modelled by the parameters defined per unit length: resistance, inductance, capacitance and conductance (RLGC). MTL are modelled as lossy. The transmission line parameters

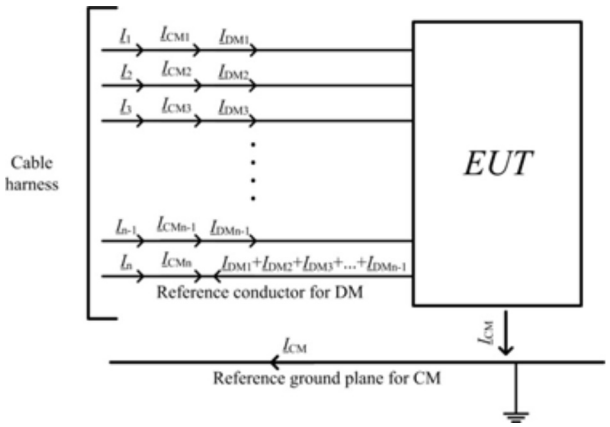

Figure 7: Definition of differential-mode and common-mode cable harness currents from cable harness line currents.

are obtained from a 2D model of a cable harness in an EM simulator.

The voltages $\underline{\mathbf{V}}(z)$ and currents _( ) on each line of the multi conductor transmission line can be calculated by decoupling the coupled transmission lines by modal analysis [8]. The line currents $\underline{\mathbf{I}}(z)$ and voltages $\underline{\mathbf{V}}(z)$ at various distances from the source z are transformed to the modal currents $\underline{\mathbf{I}}_m(z)$ and voltages $\underline{\mathbf{V}}_m(z)$ on MTL. The line currents and voltages at various distances from the source can be calculated [8]

$$\underline{\mathbf{I}}(z) = \underline{\mathbf{T}}_I \underline{\mathbf{I}}_m(z) = \underline{\mathbf{T}}_I \left(\mathbf{e}^{-\underline{\gamma}_m z} \underline{\mathbf{I}}_m{}^{+} - \mathbf{e}^{\underline{\gamma}_m z} \underline{\mathbf{I}}_m{}^{-} \right) \tag{1}$$

$$\underline{\mathbf{V}}(z) = \underline{\mathbf{T}}_V \underline{\mathbf{V}}_m(z) = \underline{\mathbf{Z}}_0 \underline{\mathbf{T}}_I \left(\mathbf{e}^{-\underline{\gamma}_m z} \underline{\mathbf{I}}_m{}^{+} + \mathbf{e}^{\underline{\gamma}_m z} \underline{\mathbf{I}}_m{}^{-} \right) \tag{2}$$

where $\underline{\mathbf{T}}_V$ is the voltage transformation matrix and $\underline{\mathbf{T}}_I$ is the current transformation matrix, $\underline{\mathbf{Z}}_0$ is the line characteristics impedance matrix and $\underline{\gamma}_m$ is the diagonal modal propagation constant matrix. The vectors $\underline{\mathbf{I}}_m{}^{+}$ and $\underline{\mathbf{I}}_m{}^{-}$ representing the constant values are defined by incorporating the boundary conditions at the beginning (source side – EUT side) $\underline{\mathbf{I}}(0)$ or $\underline{\mathbf{V}}(0)$ and at the end (load side) $\underline{\mathbf{I}}(L)$ or $\underline{\mathbf{V}}(L)$ of the multi conductor transmission line. The boundary conditions are obtained by constructing the whole simulation model consisting of: PCB layout and components, connectors, housing, a 2 D model of a cable harness and cable harness loads (artificial load for power lines and load simulator for data/signal lines) in an EM simulation software. The boundary voltages or currents are exported to the common-mode current distribution prediction model. The boundary conditions written for the currents on lines are

$$\underline{\mathbf{I}}(0) = \underline{\mathbf{T}}_I \underline{\mathbf{I}}_m(0) = \underline{\mathbf{T}}_I \left(\underline{\mathbf{I}}_m{}^{+} - \underline{\mathbf{I}}_m{}^{-} \right) \tag{3}$$

$$\underline{\mathbf{I}}(L) = \underline{\mathbf{T}}_I \underline{\mathbf{I}}_m(L) = \underline{\mathbf{T}}_I \left(\mathbf{e}^{-\underline{\gamma}_m L} \underline{\mathbf{I}}_m{}^{+} - \mathbf{e}^{\underline{\gamma}_m L} \underline{\mathbf{I}}_m{}^{-} \right) \tag{4}$$

and for the voltages on lines

$$\underline{\mathbf{V}}(0) = \underline{\mathbf{Z}}_0 \underline{\mathbf{T}}_I \left(\underline{\mathbf{I}}_m{}^{+} + \underline{\mathbf{I}}_m{}^{-} \right) \tag{5}$$

$$\underline{\mathbf{V}}(L) = \underline{\mathbf{Z}}_0 \underline{\mathbf{T}}_I \left(\mathbf{e}^{-\underline{\gamma}_m L} \underline{\mathbf{I}}_m{}^{+} + \mathbf{e}^{\underline{\gamma}_m L} \underline{\mathbf{I}}_m{}^{-} \right) \tag{6}$$

Using the exported values from an EM simulator software the vector $\underline{\mathbf{I}}_m{}^{+}$ and $\underline{\mathbf{I}}_m{}^{-}$ representing the constant values can be easily calculated from the boundary currents of the MTL

$$\underline{\mathbf{I}}_m{}^{+} = \underline{\mathbf{T}}_I{}^{-1} \underline{\mathbf{I}}(0) + \underline{\mathbf{I}}_m{}^{-} \tag{7}$$

$$\underline{\mathbf{I}}_m{}^{-} = \left(\mathbf{e}^{-\underline{\gamma}_m L} - e^{\underline{\gamma}_m L} \right)^{-1} \left(\underline{\mathbf{T}}_I{}^{-1} \underline{\mathbf{I}}(L) - e^{-\underline{\gamma}_m L} \underline{\mathbf{T}}_I{}^{-1} \underline{\mathbf{I}}(0) \right) \tag{8}$$

or from the boundary voltages of the MTL

$$\underline{\mathbf{I}}_m{}^{+} = \underline{\mathbf{T}}_I{}^{-1} \underline{\mathbf{Z}}_0{}^{-1} \underline{\mathbf{V}}(0) - \underline{\mathbf{I}}_m{}^{-} \tag{9}$$

$$\underline{\mathbf{I}}_m{}^{-} = \left(\mathbf{e}^{\underline{\gamma}_m L} - \mathbf{e}^{-\underline{\gamma}_m L} \right)^{-1} \left(\begin{array}{l} \underline{\mathbf{T}}_I{}^{-1} \underline{\mathbf{Z}}_0{}^{-1} \underline{\mathbf{V}}(L) - \\ \mathbf{e}^{-\underline{\gamma}_m L} \underline{\mathbf{T}}_I{}^{-1} \underline{\mathbf{Z}}_0{}^{-1} \underline{\mathbf{V}}(0) \end{array} \right) \tag{10}$$

The common-mode current distribution on a cable harness according to our definition in Fig. 5 can be obtained from the calculated line currents on the MTL by summing all the line currents $\underline{I}_k(z)$ at the desired distance *z* from the source side (EUT side)

$$\underline{I}_{cm}(z) = \sum_k \underline{I}_k(z) \tag{11}$$

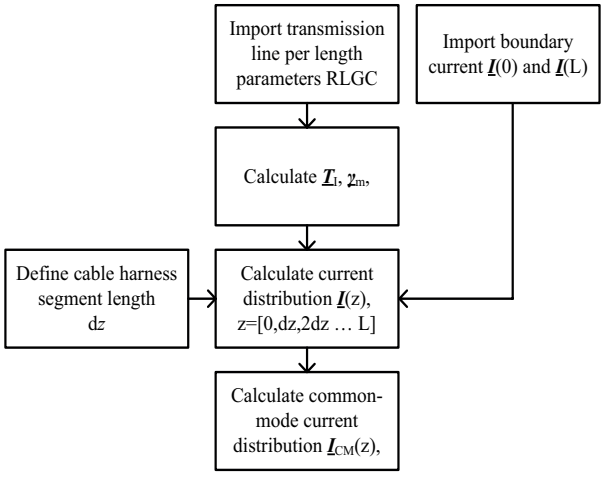

Figure 8: Workflow to calculate the common-mode current distribution on cable harness in frequency range 150 kHz – 1000 MHz using MTL model.

Fig. 8 shows the workflow to calculate the common-mode current distribution on cable harness in the frequency range 150 kHz – 1000 MHz using MTL model.

5 Validation

The proposed prediction models of the common-mode currents on a cable harness and automotive component radiated emissions testing are validated by measurements in two ALSEs with the accreditation according to ISO/IEC 17025 [9]. Firstly, the validation is done in the EMC Laboratory at MAHLE Letrika d.o.o., and secondly the validation is repeated in the EMC Laboratory at SIQ Laboratory for Electromagnetics. Two validations in separate absorber lined shielded enclosures are performed to show the high level of measurement inaccuracy and uncertainty in radiated emissions measurements according to CISPR25 [1].

Fig. 9 shows the simulation model we constructed in an EM simulator to predict the common-mode current distribution on a cable harness. Only common-mode voltage source excitation was used for the cable harness.

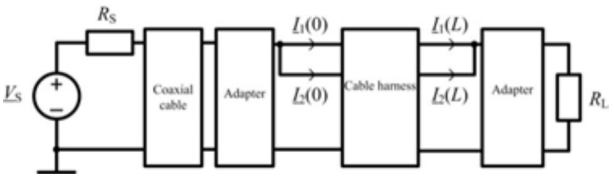

Figure 9: Simulation model used for predicting the common-mode current distribution on cable harness constructed in an EM simulator.

The EMI receiver's tracking generator, represented by the voltage source V_S and the equivalent generator resistance R_S, is used to excite the cable harness built from two parallel conductors of the type FLRY-B with a 0.75 mm^2 cross section area and which are two meters long. The tracking generator output power is set to -20 dBm during measurements. An adapter with a female N connector had to be mounted on each side of the cable harness to enable cable harness termination and excitation. The adapter is modelled in an EM simulator to include all parasitics. The cable harness is modelled as 2 D structure in an EM simulator. The coaxial cable is also modelled in an EM simulator to include attenuation and a velocity factor. The load side adapter of the cable harness is terminated with a 50 Ohm load. A coaxial cable ECOFLEX15 14 meters long connected the tracking generator to the cable harness source side adapter.

Time required to build a complete model in EM simulator is about 4 h in 4000 frequency points. The time required to simulate the complete model is about 40 minutes in 12704 frequency points with interpolation. Common-mode current distribution on cable harness and radiated emissions simulation are finished in 5 minutes. We are running simulations on system with the following specifications: 2 XEON processors eight core, sixteen threads, E5-2680 running at 2.7 GHz clock with 128 GB ram on a 64 bit operating system.

5.1 Common-mode current distribution on cable harness

Figs. 10–12 show the predicted and measured common-mode currents at three locations on a cable harness. The measurements are done at MAHLE Letrika d.o.o. and at SIQ using Fischer F-52 RF current probe. The figures show minor deviations between the predicted and measured common-mode currents at frequencies of up to 400 MHz at MAHLE Letrika d.o.o. Higher deviations are seen between measurements at MAHLE Letrika d.o.o. and SIQ. The reason for the deviation is the tracking generator's typical output level deviation of 1.9 dB in the frequency range 150kHz – 1 GHz.

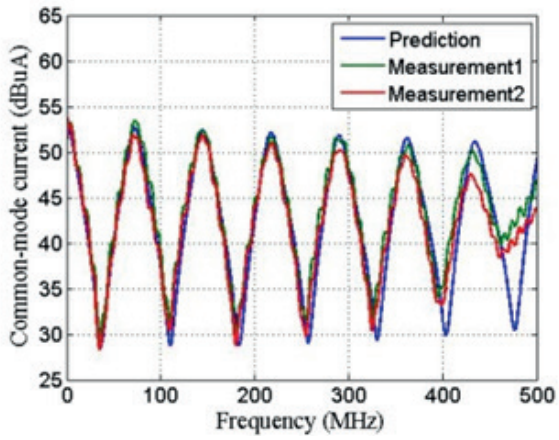

Figure 10: Comparison of the predicted and measured common-mode currents at the source side of the cable harness at MAHLE Letrika d.o.o. (Measurement1) and at SIQ (Measurement2).

The tracking generator output level was modelled with a nominal level (-20 dBm) and the output impedance as 50 Ω resistance, without taking into consideration the output port VSWR. The cable harness termination 50 Ω load was also modelled as a 50 Ω resistance, without taking into account the load VSWR. Above the frequency of 450 MHz the cable harness cannot be modelled anymore with the MTL model. Higher modes of propagation besides the TEM mode exist and the current dis-

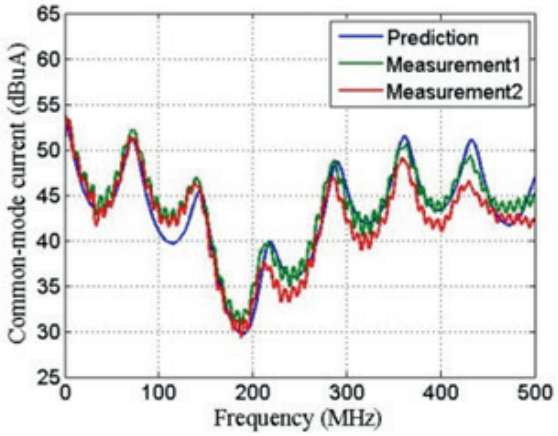

Figure 11: Comparison of the predicted and measured common-mode currents at 167 cm along the cable harness from the source side at MAHLE Letrika d.o.o. (Measurement1) and at SIQ (Measurement2).

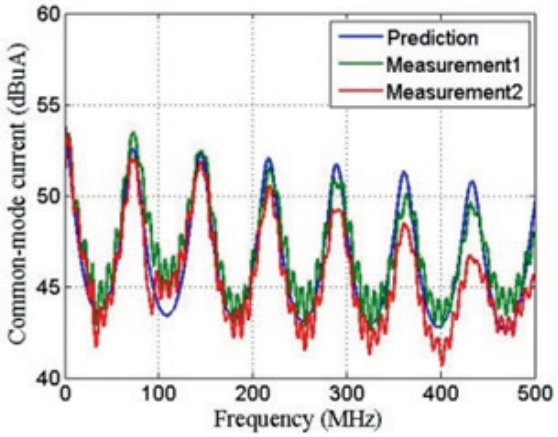

Figure 12: Comparison of the predicted and measured common-mode currents at the load side of the cable harness at MAHLE Letrika d.o.o. (Measurement1) and at SIQ (Measurement2).

tribution on a cable harness can be predicted only by a full-wave model.

5.2 Radiated emissions levels from cable harness

Fig. 13 shows a comparison of the predicted radiated emissions levels and measured radiated emissions levels at MAHLE Letrika d.o.o. and SIQ in the frequency range 150 kHz – 30 MHz in vertical antenna polarization. The ground plane height above the chamber floor was 95 cm at MAHLE Letrika d.o.o., 84 cm at SIQ and 7 cm at SIQ when the ground plane was lowered closer to the chamber floor. The deviation occurring at higher frequencies is due to resonances occurring between the ground plane and chamber floor via grounding of the ground plane to the chamber floor [6]. We have confirmed these findings by positioning the ground plane closer to the chamber floor at SIQ (Fig. 10, Measurement3). The deviation between the Measurement3 and the prediction is minimal and is within ± 2 dB. We can expect deviations up to 20 dB in radiated emissions levels between a different ALSE using the test setup according to CISPR25 [1] in the frequency range 15 MHz – 30 MHz.

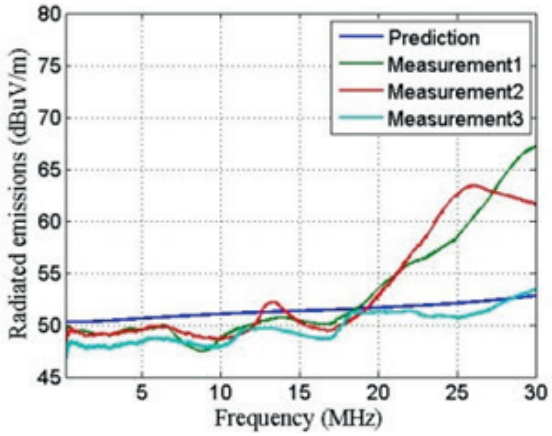

Figure. 13: Comparison of the predicted and measured radiated emissions levels at MAHLE Letrika d.o.o. (Measurement1), at SIQ (Measurement2) and additional measurement at SIQ by lowering the ground plane closer to the chamber floor (Measurement3).

Fig. 14 – 16 show the predicted and measured radiated emissions levels in the frequency range 30 MHz – 1000 MHz at MAHLE Letrika d.o.o. and at SIQ. Fig. 14 and 15 show radiated emissions levels in vertical and horizontal antenna polarization, respectively. Fig. 16 shows the maximum radiated emissions levels in both antenna polarisations.

Fig. 17 shows deviations between the predicted and measured radiated emissions levels in the frequency range 30 MHz – 1000 MHz in both antenna polarizations at MAHLE Letrika d.o.o. and SIQ. The deviations are calculated by subtracting the predicted maximum radiated emissions level in both antenna polarizations from those measured at MAHLE Letrika d.o.o. (Deviation1) and at SIQ (Deviation2).

The deviations between the prediction and measurements occur in the lower frequency range below 100 MHz due to grounding resonances, ground plane size, and ALSE resonances [10]. The ground plane used at MAHLE Letrika d.o.o. and at SIQ was not the same size. The ground plane size used in testing at MAHLE Letrika was 2.5 m long by 1.25 m wide. At SIQ the size of the ground plane was 2.2 m long by 1.2 m wide. The ground plane height used at MAHLE Letrika d.o.o. was 95 cm, while at SIQ it was 84 cm. A completely different

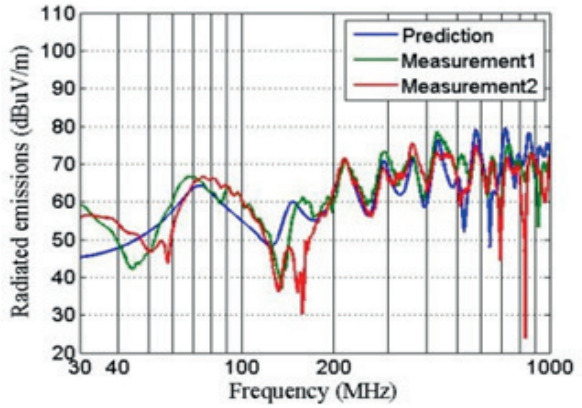

Figure 14: Comparison of the predicted and measured radiated emissions levels in the frequency range 30 MHz – 1000 MHz in vertical antenna polarization at MAHLE Letrika d.o.o. (Measurement1) and at SIQ (Measurement2).

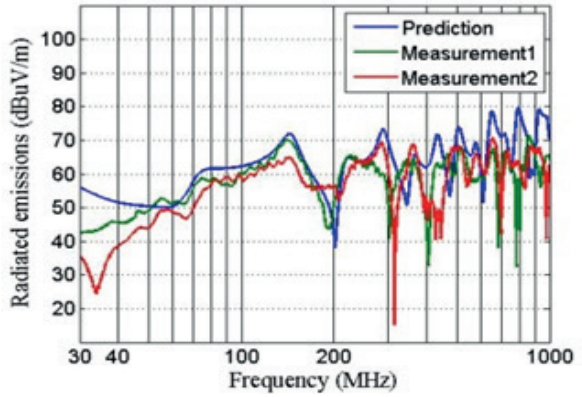

Figure 15: Comparison of the predicted and measured radiated emissions levels in the frequency range 30 MHz – 1000 MHz in horizontal antenna polarization at MAHLE Letrika d.o.o. (Measurement1) and at SIQ (Measurement2).

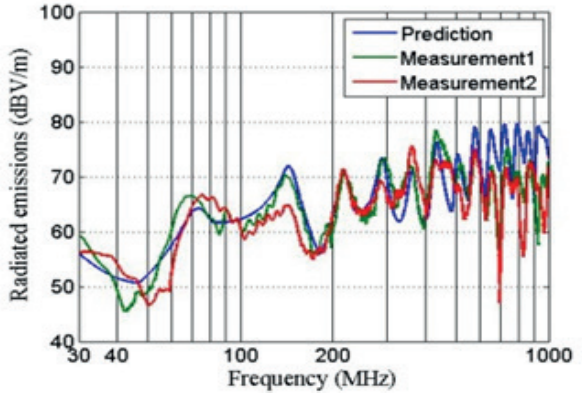

Figure 16: Comparison of predicted and measured radiated emissions levels in the frequency range 30 MHz – 1000 MHz in both antenna polarizations at MAHLE Letrika d.o.o. (Measurement1) and at SIQ (Measurement2).

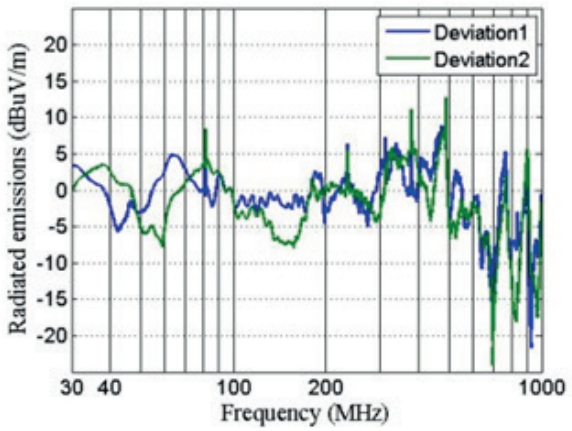

Figure 17: Deviations between the predicted and measured radiated emissions levels in the frequency range 30 MHz – 1000 MHz in both antenna polarizations at MAHLE Letrika d.o.o. (Deviation1) and at SIQ (Deviation2).

ALSE was used at MAHLE Letrika d.o.o. compared to the ALSE at SIQ. The difference is in the size of the ALSE, absorbers performances, etc. All of the presented parameters have an impact on measured radiated emissions levels in the frequency range below 100 MHz.

Additional deviations between the prediction and measurements can be seen at frequencies around 150 MHz. We believe that high sensitivity of radiated emissions levels to variance in cable harness position above ground plane can be seen in this frequency range. A small difference (in order of a few milimeters) in the distance of the cable harness from the edge of the ground plane has a high effect on radiated emissions levels around 150 MHz.

The deviations between the prediction and measurements above 450 MHz frequency are caused by an inaccurate common-mode current distribution on a cable harness using the MTL model. The cable harness height of 50mm above the ground plane limits the maximum frequency for which the MTL model is still valid. Above 500 MHz the product PCB and inside connections will also contribute to overall radiated emissions if the product housing is plastic.

Deviations up to 10 dB could be seen between the measurement at MAHLE Letrika d.o.o. and at SIQ. This means that if radiated emissions levels are measured above automotive OEM's limit lines, the source of the radiated emissions is reduced and the levels are reduced 2 – 3 dB below the automotive OEM's limit lines in the ALSE1, there is no guarantee that the product will also pass radiated emissions measurement in the ALSE2. A higher margin of about 6 dB is recommended

in order to guarantee that the product will also pass radiated emissions testing in other ALSE.

6 Conclusion

A radiated emissions prediction model is developed to estimate the radiated emissions levels from a cable harness above the ground plane according to CISPR25 [1] in the frequency range 150 kHz – 1000 MHz. The dominant radiated emissions result from common-mode currents on the cable harness, currents in the ground plane and the current on vertical grounding connections. The common-mode current distribution on a cable harness is predicted with good accuracy, up to 450 MHz using the multi conductor transmission line model (MTL) and MTL boundary conditions obtained from EM simulation software, where PCB layout, component, connectors, housing, cable harness 2D model and cable harness loads are modelled by appropriate numerical methods (FEM or BEM). The effect of the ground plane on radiated emissions levels above 30 MHz is considered by calculating the current on the surface of the ground plane. The surface current is calculated using Ampere's law from the common-mode current distribution on a cable harness and mirrored common-mode current distribution over the ground plane (mirror theory). The radiated emissions from the common-mode current distribution, currents in the ground plane, and currents of the vertical grounding connections can be predicted using Hertzian dipoles for frequencies above 30 MHz. The radiated emissions levels below 30 MHz are predicted from the common-mode current distribution on the cable harness, mirrored common-mode current distribution on the mirrored cable harness over the ground plane, and the current on the vertical grounding connections.

The presented radiated emissions prediction obtained by the predicted common-mode current on a cable harness offers insight into the source of emissions of a product, and enables an engineer to reduce the radiated emissions of a product below automotive OEM's limits in the product design phase prior to the first prototype. It also reduces the need to model the CISPR25 radiated emissions test setup in a 3D EM simulator and thus reduces the calculation time and the computer resources needed. An EM simulator is needed to calculate the voltages or currents at the beginning and at the end of the cable harness, which are imported to novel common-mode current distribution prediction model. Boundary voltages or currents on cable harness are then imported into the radiated emissions prediction model, which calculates the levels of radiated emissions according to CISPR25 setup. The radiated emissions prediction model could even be integrated into an EM simulator as an option to calculate CISPR25 radiated emissions levels.

This workflow reduces the resources needed to repeat testing in an ALSE and to build numerous prototypes. It even enables a radiated emissions levels prediction in the early design phase, when the product prototype is not available for testing.

The presented method is much faster compared to other numerical methods (FEM or MOM) often used for radiated emissions evaluations of CISPR25 test setup in 3D space. It enables radiated emissions prediction in a few minutes in over ten thousand frequency points.

A validation was done with an automotive cable harness consisting of two cables, 50 Ohm termination load, and a tracking generator as a source. Our next task is to model an automotive electronic component together with the cable harness and load in an EM simulator and use the presented model to predict radiated emissions levels.

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Arrived: 11. 03. 2016
Accepted: 13. 04. 2016

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 1(2016), 53 – 53

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Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
ISSN 0352-9045

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MIDEM Society / Društvo MIDEM
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