TRENDS IN MIXED SIGNAL ASIC DESIGN

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Key words: integrated circuits, ASIC, circuit design, technology progress, future development, design methodology, new applications, new requirements

Summary: The paper presents an overview of some future trends in mixed signal ASIC design due to the progress of technology, new applications requirements and new design approaches. Some examples demonstrating such trends are presented.

Smernice razvoja načrtovanja analogno/digitalnih vezij ASIC

Ključne besede: IC vezja integrirana, ASIC vezja, projektiranje vezij, napredek tehnologije, razvoj bodoči, metodologije projektiranja, aplikacije nove, zahteve nove

Povzetek: Članek obravnava pregled nekaterih smernic razvoja v načrtovanju vezij ASIC, ki so pogojena z napredkom tehnologije, z novimi zahtevami za integracijo in z novimi načrtovalskimi prijemi. Podani so nekateri zgledi, ki prikazujejo nakazane smernice.

INTRODUCTION

ASIC designers are challenged to cope with three major directions of future development: progress in technology, new application requirements and design methodology improvements.

Progress in technology. Although presently the volume IC production (except for memories) is still in CMOS technology with typical one micrometer minimal dimension we see a fast trend towards submicron (typically 0.6 μm to 0.8μm) processes. The consequences of this trend and associated problems and benefits are discussed. Higher cost of BiCMOS processes compared to CMOS processes is being compensated by the advantages of having unipolar and bipolar active devices available. Wider availability of BiCMOS processes requires upgrading of the designers skills and knowledge to be able to optimize the circuitry and to use all the benefits available in such process.

New application requirements. Battery operation at the user's end is very difficult requirement which emerges from the need of portable electronic devices, presently portable telephones and in future personal intelligent terminal and a number of medical electronic aids.

The other extreme addressed is very high frequency ASIC design which is used mainly for information distribution on coaxial and fiber optic cables.

Complex electronic systems including various sensors and other transducers incorporated to the ASIC is another trend requiring new design approaches.

Design methodology improvements. It is clear that the mentioned design tasks demand more powerful design methodologies and design tools. CAD hardware being more and more capable to support very demanding algorithms contributes to the development of new design tools. Mixed signal ASIC design expertise has become the most desirable and on the other hand the most difficult.

PROGRESS IN TECHNOLOGY

Trends in processing technology are towards process modularisation. This means that specific process steps will be developed independent and controlled by the set of target features. Such process module can be used in a variety of standard and non standard ASIC production simply by verifying the process module parameters. Specific process module parameters will be translated to manufacturing tools setting. Wafer fab will therefore become universal wafer fab consisting of so called cluster tools where the complete manufacturing process will be completely robotized. Such wafer fab will be suited to manufacture according to application specific process enabling the designer not only to optimize the

IC to the application function but also to select the optimal process.

Such trend is shown in the present status of BiCMOS processes. The designer can select from at least three different varieties of BiCMOS process for ASICs:

- CMOS based BiCMOS for improved speed
- Digital BiCMOS for high frequency and static RAM
- Mixed mode BiCMOS for having the selection of full range of active and passive devices for analog design

BiCMOS based processes seem to be the basis for future ASIC designs due to various advantages offered by both types of active devices.

Some of advantages of bipolar transistors are:

- Transconductance of the bipolar transistor is larger by an order of magnitude compared to the unipolar transistor.
- The high frequency behaviour of bipolar transistors is much better than unipolar transistors.
- Noise of bipolar transistors is lower especially at low frequency since the 1/f noise phenomena is almost negligible.
- Matching characteristics of bipolar transistor are superior due to the low variation of V_{BE} on the same chip.

The most important advantages of unipolar transistors are:

- No input bias current is needed, so very high input impedance is achievable.
- Zero power supply quiescent current in fully complementary structures at dc conditions.
- Full power supply swing available for both analog and digital signals with simple electrical topology allowing high functional density at high noise immunity.
- Unipolarity allows more circuit design freedom, e.g. circuits with bi-directional switches, circuits operating in weak inversion region etc.

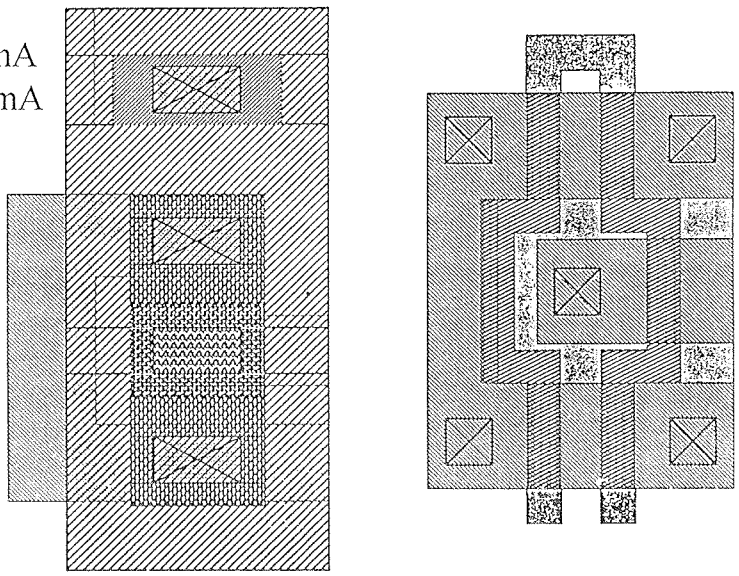
Fig.1 shows the layout of equal area unipolar and bipolar transistors to demonstrate the fact that minimum size bipolar transistors is compared to unipolar transistors with W/L ratio much larger than minimum size. Nevertheless at the same operating current g_m of bipolar transistors is still 18 times higher.

Minimum geometry scaling down is one other trend in process technology development. Effects of geometry scaling down are the following:

- Packing density increase
- Circuit complexity increase
- Parasitic capacitance decrease
- Switching speed increase
- Contact resistance increase
- Interconnection resistance increase

To demonstrate the drastic increase of packing density of a standard digital cell, D flip-flop with asynchronous reset with the schematic shown in fig. 2 was used. Fig. 3 shows the layout of the same cell when using 5μm, 3μm, 2μm, 1.2μm and 0.6μm CMOS processes.

$$g_m \text{ bipolar} \approx 18\text{mA/V at } I_C \approx 0.5\text{mA}$$
$$g_m \text{ unipolar} \approx 1\text{mA/V at } I_D \approx 0.5\text{mA}$$



a b

Fig. 1: Bipolar and unipolar transistor comparison example: a) layout of minimum emitter area of bipolar transistor, b) layout of equal size MOS transistor

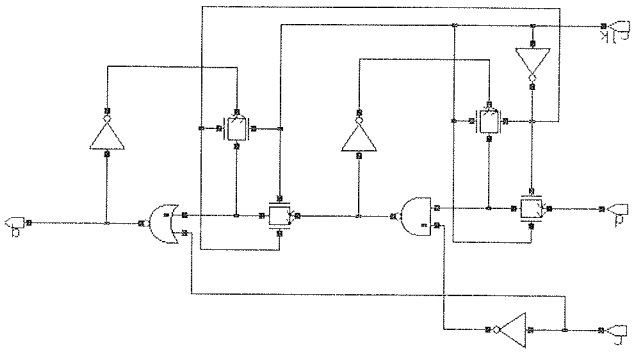


Fig. 2: Schematic diagram for D flip-flop with reset used for packing density comparison

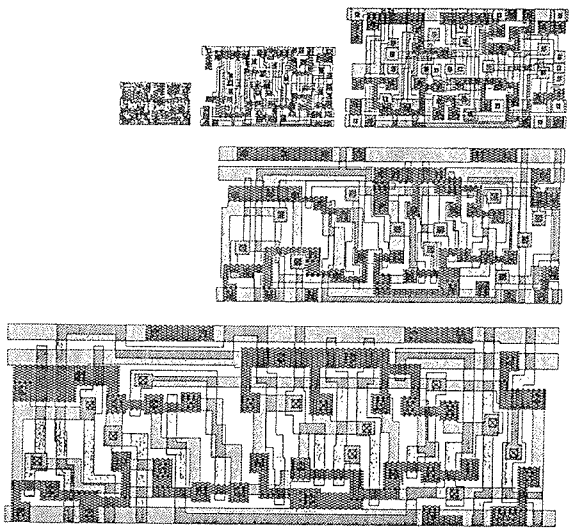


Fig. 3: Packing density comparison for 5μm, 3μm, 2μm, 1.2μm and 0.6μm CMOS processes

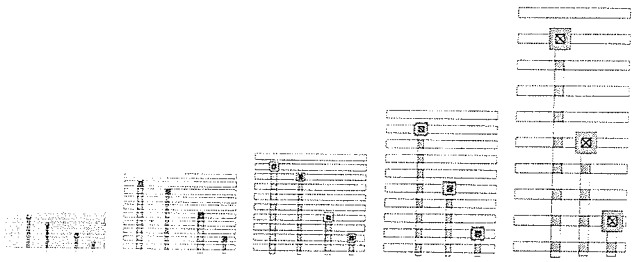


Fig. 4: Packing density comparison for 5μm, 3μm, 2μm, 1.2μm and 0.6μm CMOS processes

Fig. 4 shows typical interconnection channel for the same technologies.

Table 1 shows area and speed comparisons for the listed technologies.

Table 1: Packing density and switching speed comparison for 5μm, 3μm, 2μm, 1.2μm and 0.6μm CMOS processes

CMOS Process	5μm	3μm	2μm	1.2μm	0.6μm
Cell area (μm^2)	28000	14000	6720	2680	756
Cell area factor	37	18.5	8.8	3.5	1
Channel width (μm)	131	76	51.6	40.2	19.8
Channel width factor	6.6	3.8	2.6	2	1
Propagation delay (ns)	17.6	4.3	2.8	1.5	1.15

The effect of scaling down in analog design is most important in the following areas:

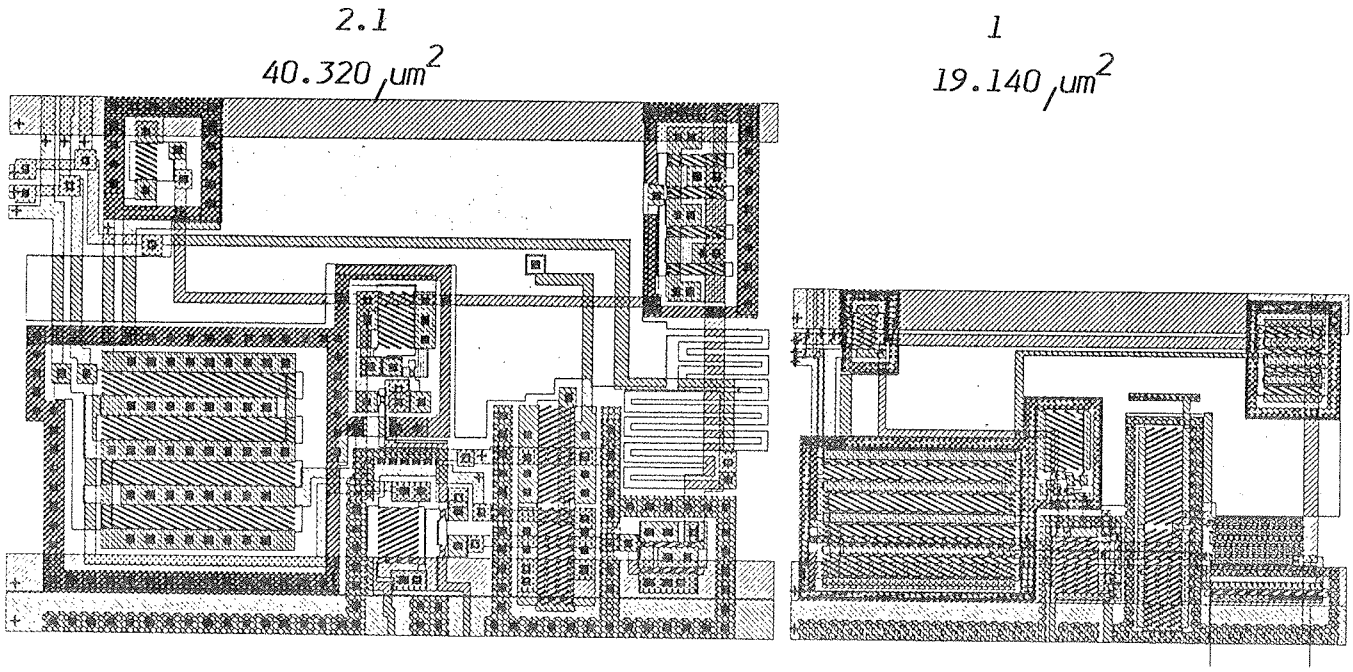


Fig. 5: Design example of operational amplifier with equal performance and topology using 2μm CMOS and 0.8μm CMOS

- Matching characteristics scaling coefficient proportional to lithography
- 1/f noise scaling coefficient proportional to t_{ox}
- Interconnection parasitics

To achieve approximately the same performances and using the same electrical topology two operational amplifiers were designed using 2μm and 0.8μm technology. The outcome is presented in fig. 5 showing packaging density improvement factor 2.1 which is much less that it would be for digital cell.

NEW APPLICATION REQUIREMENTS

We are facing a rapid demand of new ASICs designs in the area of:

- Low voltage low power battery operation ASICs
- High frequency operation
- Integrated electronic systems

For the low voltage design the following design specific should be observed:

- Decrease the noise floor to maintain input signal dynamic range or digital noise immunity levels
- Decrease the input offset voltage
- Avoid any stacking techniques (cascoding)
- Improve slew rate or switching speed
- Improve fan-out and output voltage range
- Use charge pumping and other boosting techniques

Table 2 shows design example of low noise low power realizations of battery operated microphone amplifier using both CMOS and BiCMOS technology.

Table 2: Comparison of CMOS and BiCMOS realization of the microphone differential amplifier

Feature	CMOS realization	BiCMOS realization
Min power supply voltage/current	± 1.2V / 1mA	± 1.2V / 1mA
Silicon area	1.672 mm x 0.567 mm 0.948 mm^2	0.416 mm x 1.304 mm 0.542 mm^2
Total harmonic distortion at 2 Vpp output voltage	0.25%	0.3%
Input referred psophometric noise voltage	0.406μV	0.502μV
Input current	< 10^{-9}A	3μA

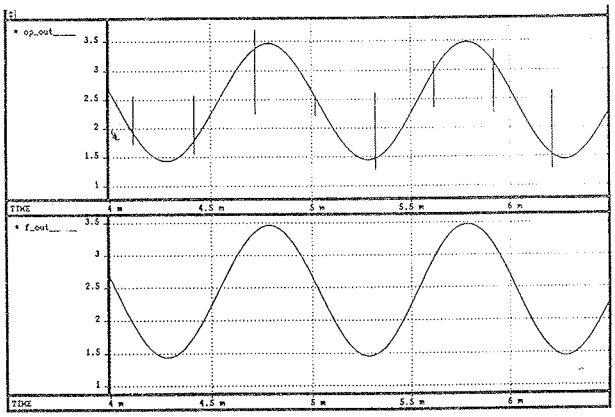


Fig. 7: Result of "out of signal frequency band" offset cancellation

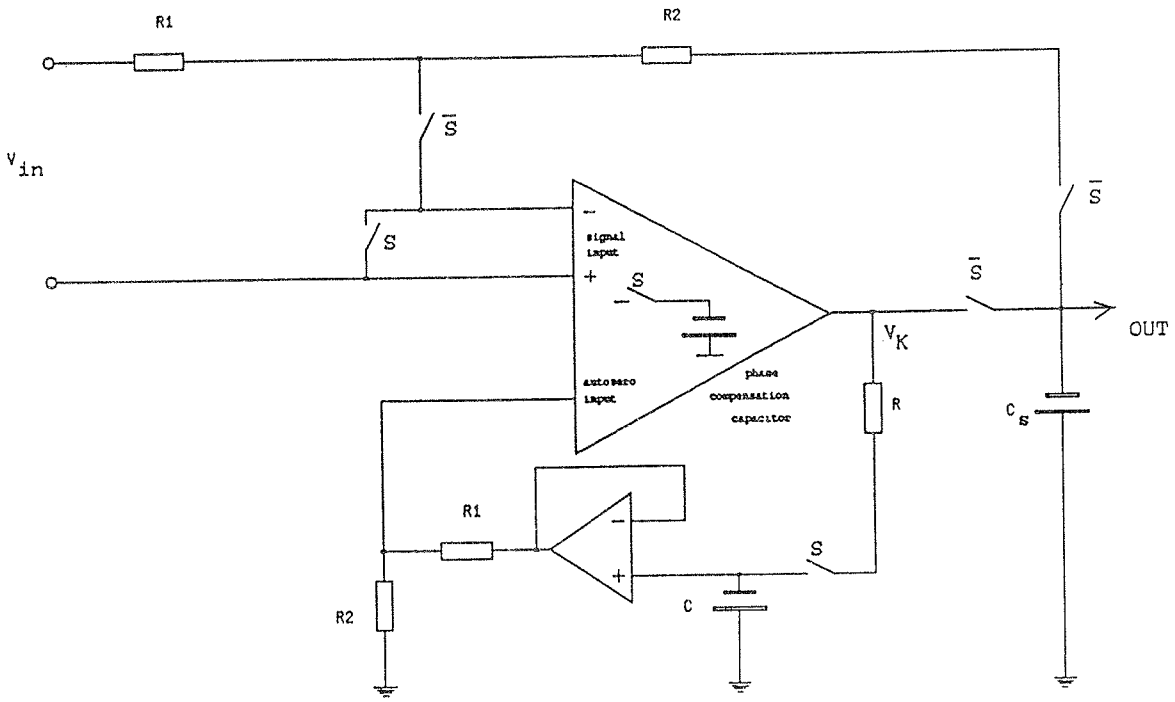


Fig. 6: Principal schematic of "out of signal frequency band" offset cancellation

An example of novel approach to input offset voltage cancellation technique is shown in fig. 6. This approach provides automatic offset voltage cancellation without any disturbances of the signal. This is achieved by shortening the offset measurement time to shift the disturbance out of signal frequency band. This can only be achieved by switching the operational amplifier into a "fast" ie comparator mode. The resulting signal of such cancellation is shown in fig. 7.

DESIGN METHODOLOGY IMPROVEMENTS

In mixed signal design simulation will remain a major design tools specially for the analog part of the design.

The simulation phase of the design will not be used only for functional and parametric verification but to perform design centering and specially to predict and improve yield loss caused by process variations and operation conditions variations.

Efficiency of simulation depends on

- Simulation models
- Simulation method
- Simulation coverage
- Interpretation of simulation result

Conservative approach to design centering used to be as follows:

- Design according to specification fabrication according to matrix of technology parameters
- Characterize to find the correlation of ASIC parameters to process parameters
- Redesign if necessary
- Determine the best process parameters and fabricate as close as possible to given process parameters

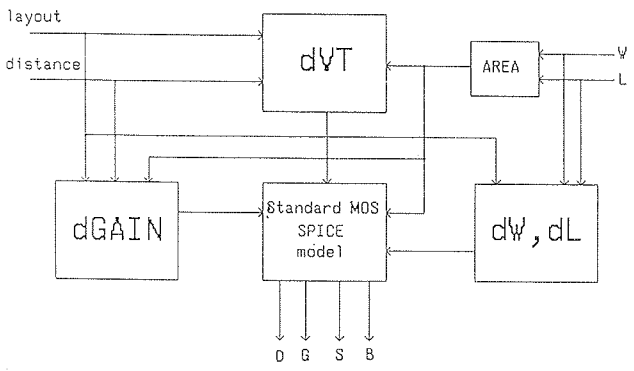


Fig. 8: Block diagram of the MOS transistor matching model

Much more effective approach is to shift the design centering and yield prediction in the design phase, without doing costly and time consuming fabrication.

To do this the following activities are necessary:

- Simulation with typical parameters
- Simulations using Monte-Carlo approach
- Simulation using four (all corners)
- Post-layout simulation with layout parasitic extracted
- Post-layout simulation with extended parasitics and with extended models

For real high volume production this approach can be extended to the following procedures:

- Design according to specifications using described approach
- Fabrication
- Characterization of the ASIC
- Resimulation with actual parameters and comparison to measured results

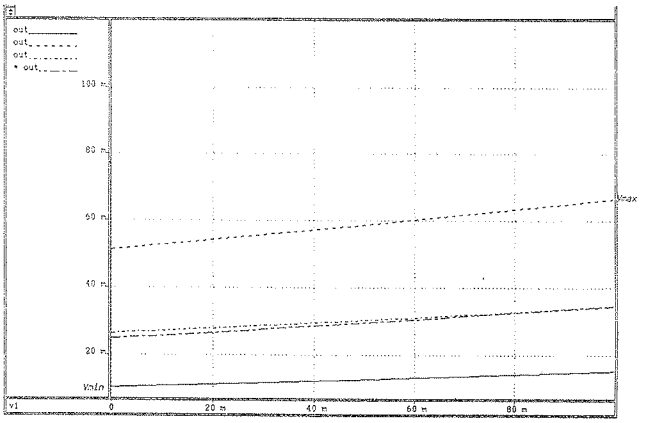


Fig. 9: Simulation result of four corner active device Vin analysis. Vout max / Vout min ≈5. No. of simulations = 4

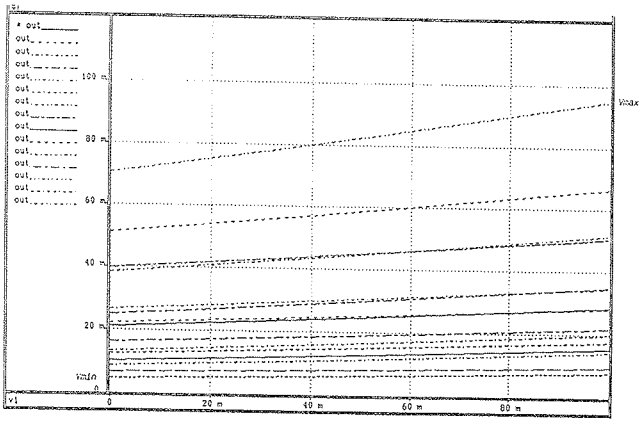


Fig. 10: Results of full corner analysis with four transistor corners, two resistor corners, two temperature corners and two power supply corners. Vout max / Vout min ≈22. No. of simulations = 32

- Optimization of the simulation models
- Optimization of the design

The simulation procedure should take into account the following effects:

- Process parameters variations influence on active devices
- Process parameters variations influence on passive devices
- Power supply voltage variations
- Temperature variation
- Other external conditions (load variation, input common mode and differential mode voltages etc.)

The importance of verifying all possible conditions is shown in figs. 9 and 10. Fig. 9 shows simulation result of only four corner process variations giving $V_{out\ max}$ to $V_{out\ min}$ ratio approximately 5. Fig. 10 shows full corner analysis where this ratio has increased to 22. It is important to mention that simulation models should be enhanced in the following areas:

- Models of interconnections
- Models of integrated resistors
- Models of integrated capacitors
- Models of active devices

Interconnection models take into account: ground interconnections, power supply interconnections, sensitive interconnections and interconnections carrying high speed signals.

Parameters of enhanced model of integrated resistor are: contact resistance, distributed resistor capacitance, resistor matching factor (worst case corners).

The parameters of extended model for integrated capacitor depend on:

- Matching factor as a function of
  - capacitor size
  - capacitor shape
  - capacitor position
  - capacitor border conditions
- Capacitor quality as a function of
  - capacitor layout
  - capacitor connection network

Fig. 8 shows block diagram of matching model of MOS transistor.

CONCLUSION

Future mixed signal ASIC designers will be challenged to design in much richer variety of processes, possibly in application specific processes. To do that the designer should have better knowledge of the available technologies. This requires:

- Deep understanding of all passive and active devices offered by modern "universal" ASIC technology
- Know-how to select the most effective subprocess for the selected application. The designer should have also the ability to adapt to novel application requirements, i.e. his electronic and mechanical systems knowledge has to widen.
- In the area of design methodology he has to concentrate to effective simulation for verification of each design step, to use extended device modeling and to become familiar with new and efficient simulation tools.

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