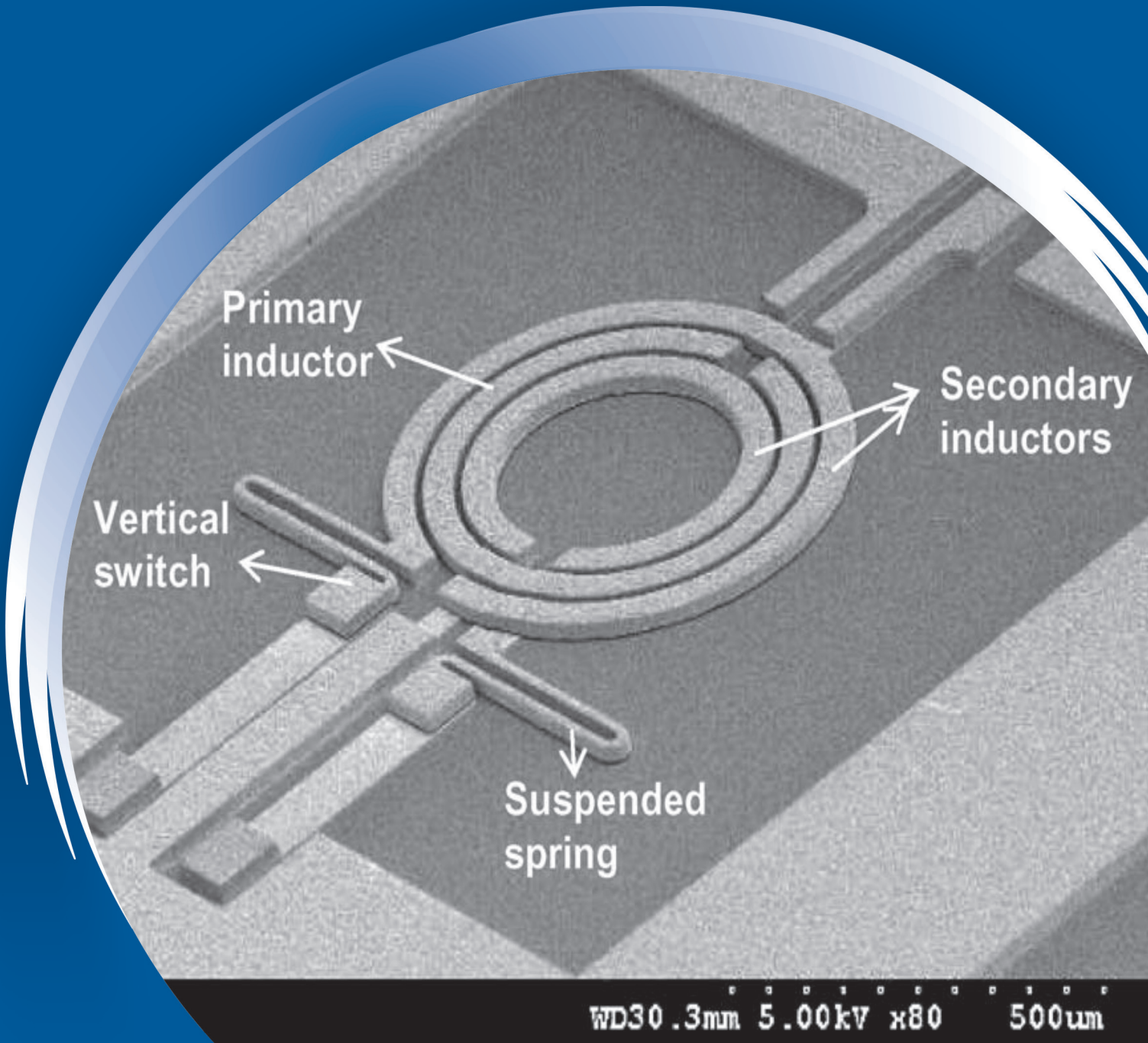
ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 44, No. 2 (2014), June 2014

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 44, številka 2 (2014), Junij 2014



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *2-2014*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 44, NO. 2(150), LJUBLJANA, JUNE 2014 | LETNIK 44, NO. 2(150), LJUBLJANA, JUNIJ 2014

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Headquarters | Naslov uredništva
Uredništvo Informacije MIDEM
MIDEM pri MIKROIKS
Stegne 11, 1521 Ljubljana, Slovenia
T. +386 (0)1 513 37 68
F. + 386 (0)1 513 37 71
E. info@midem-drustvo.si
www.midem-drustvo.si

Annual subscription rate is 100 EUR, separate issue is 25 EUR. MIDEM members and Society sponsors receive current issues for free. Scientific Council for Technical Sciences of Slovenian Research Agency has recognized Informacije MIDEM as scientific Journal for micro¬electronics, electronic components and materials. Publishing of the Journal is cofinanced by Slovenian Book Agency and by Society sponsors. Scientific and professional papers published in the journal are indexed and abstracted in COBISS and INSPEC databases. The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™. |
Letna naročnina je 100 EUR, cena posamezne številke pa 25 EUR. Člani in sponzorji MIDEM prejemajo posamezne številke brezplačno. Znanstveni svet za tehnične vede je podal pozitivno mnenje o reviji kot znanstveno-strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinancirajo JAKRS in sponzorji društva. Znanstveno-strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC. Prispevke iz revije zajema ISI® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™.
Po mnenju Ministrstva za informiranje št.23/300-92 se šteje glasilo Informacije MIDEM med proizvode informativnega značaja.

Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
44, No. 2 (2014)

Content | Vsebina

Review scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 44, No. 2 (2014), 87 – 103

Evaluation and analysis of methods for fixed and variable MEMS inductors design

Fatemeh Banitorfian[1], Farshad Eshghabadi[1], Asrulnizam Abd Manaf[1], Patrick Pons[2], Norlaili Mohd Noh[1], Mohd Tafir Mustaffa[1], Othman Sidek[1]

[1]Advanced Integrated System Device Group (AISDe), School of Electrical and Electronic Engineering, Universiti Sains Malaysia, Engineering Campus, Nibong Tebal, Malaysia
[2]CNRS, LAAS, Toulouse, France

Abstract: This paper investigates fixed and tunable MEMS inductors. A detailed technical discussion is given on those parameters that influence the inductance, quality factor, resonance frequency, and tuning range. Based on these parameters, the available methods are reviewed and categorized for both fixed and tunable inductors to improve the quality factor and tuning range. The major research issues in fixed MEMS inductors are the quality factor and the resonant frequency. The tuning range, in addition to the quality factor, is the main research issue of tunable MEMS inductors. Several comparison graphs are given to show the performance of each method. The parameters and their effect on the performance of the inductor were analyzed and simulated by MATLAB to present their pros and cons, their effectiveness, and their failures. This exploration can assist the designers to choose the appropriate methods for developing fixed and tunable inductors in terms with their desired application and specification. In this technical review paper, a detailed comparison between the inductors parameters for different techniques of development and adjustment gives the researchers a deep understanding of available solutions.

Keywords: Passive circuits, Inductors, Q factor, Simulation, Microelectromechanical devices

Evaluacija in analiza metod za oblikovanje fiksnih in variabilnih MEMS tuljav

Izvleček: Članek raziskuje fiksne in nastavljive MEMS tuljave. Podana je natančna tehnična razlaga parametrov, ki vplivajo na induktivnost, faktor kvalitete, resonančno frekvenco in območje nastavljanja. Na osnovi teh parametrov so predstavljene in kategorizirane obstoječe metode povečanja faktorja kvalitete in območja nastavljanja za fiksne in nastavljive tuljave. Glavni raziskovalna izziva pri fiksnih MEMS tuljavah sta faktor kvalitete in resonančna frekvenca. Območje nastavljanja je poleg faktorja kvalitete najpomembnejši raziskovalni faktor pri nastavljivih tuljavah. Podani so številni grafi, ki prikazujejo prednosti vsake metode. Z namenom prikazovanja prednosti in slabosti ter učinkovitosti metod so bili parametri in njihovi vplivi na delovanje tuljave analizirani in simulirani s simulatorjem Matlab. Ta raziskava lahko pomaga načrtovalcem pri razvoju fiksnih in nastavljivih tuljav. V tem preglednem članku obsežna primerjava parametrov tuljav razvitih z različnimi tehnikami podaja raziskovalcem razumljiv in celosten vpogled v delovanje in razumevanje obstoječih rešitev.

Ključne besede: pasivna vezja, tuljave, Q faktor, Simulacije, MEMS strukture

** Corresponding Author's e-mail: banitorfian.f@gmail.com*

1 Introduction

Recently, rapidly increasing interest for small-sized high-performance wireless systems has led to a high demand for integrated passive devices in radio-frequency integrated circuit (RFIC) applications. Inductors play a key role in radio frequency (RF) circuits. Conventional on-chip inductors are spiral inductors that are utilized in portable wireless communication circuits to meet the desired system specifications, such as: low cost, low voltage supply, small size, low power dissipation, low noise, high frequency of operation, and low distortion [1, 2]. The most important applications for inductors are in: impedance matching networks, a voltage controlled oscillator (VCO), LC tanks in a VCO, multi-band RF filters, multi-band monolithic microwave integrated circuitry (MMIC), power amplifiers in radio transmitters,

low-noise amplifiers (LNAs), and double-balanced Gilbert-cell mixers [3-6].

Currently, there are several drawbacks that limit the performance when employing conventional planar MMIC inductors, such as substrate parasitics and the conductivity of silicon substrate [2], which cause low resonance frequency and low *Q* factor [6-8]. The best approach to reduce the effect of substrate conductivity is to use MEMS technology with which high *Q* and high performance can be achieved [2, 9]. The MEMS inductor gives a very high *Q* factor compared with the MMIC inductor. This can improve sufficiently the noise figure in LNAs and the phase noise in VCOs. Also, the MEMS inductor can be implemented to be tunable, whereas the MMIC inductor cannot.

The most important parameter in fixed MEMS inductors is the quality factor, which can be improved by several techniques. These methods can be listed briefly as: substrate effects reduction by removing the substrate under the coil or increasing the distance between the substrate and the metal coil, in order to reduce the capacitive and inductive coupling [8, 10, 11] or decoupling (such as vertical planar inductor) [12, 13]; the use of 3D inductors to reduce losses inserted by the eddy current that is generated in the substrate [14]; the use of a patterned-ground layer between the spiral and substrate [15]; the use of high resistivity substrate [16]; the use of high conductivity metal for inductors [17, 18]; and changes to the thickness and width of the metal [19].

In tunable MEMS inductors, in addition to the *Q* factor, the tuning ratio is a research issue. Briefly, the methods to improve the tuning range are: change the number of turns [9, 20], change of coupling capacitance [21-24], switched inductor [5, 25], change of mutual inductance (in transformer type) [3, 4, 26, 27], change of the permeability [28-31], and counteractive magnetic field induction [32, 33].

In this paper, the advantages and disadvantages of each method are considered and a detailed comparison and analysis among these methods is presented. Section II discusses around the MEMS inductors' geometry, equivalent model and corresponding equations for inductance and quality factor. A detailed discussion for fixed-tuned MEMS inductor with available methods of quality factor enhancement and their relative analysis is given in section III. In section IV, available methods to implement a tunable MEMS inductor and tuning range increase are described with the corresponding detailed analysis. Finally, the conclusion is given in section V.

2 MEMS Inductors

The growing market of the wireless and communication industry has caused a remarkable demand for integrated passive elements. Conventional MMIC inductors do not provide sufficient quality factor or the capability of tuning. However, MEMS inductors are suitable for replacing conventional MMIC inductors. The conventional form of on-chip inductor is spiral. There are different possible shapes for the fabrication of inductors such as square, hexagonal, octagonal and circular. The effect of these shapes on inductance was investigated in [34]. The circular type shows the best *Q* factor; because in the square type, the current distribution is crowded into the edge of the corners, such that the effective series resistance is increased. MEMS inductors are designed depending on application; integrated MEMS inductors on Si wafer appear to be very interesting for future RF and microwave functions and communication systems. Currently, the most demanded application for MEMS inductors is in reconfigurable wireless systems such as satellite communication and mobile handsets [35]. The general model showing planar inductor performance is illustrated in Figure 1. L_s indicates the low-frequency inductance and R_s gives the series resistance of the coil. The capacitance between the different windings of the inductor is shown by C_s, including the air core as the covering dielectric layers. C_{ox} is the oxide (or polyamide) capacitance layer between the windings and the silicon (or GaAs) substrate, C_{Si} is the capacitance between the coil and the ground through the silicon substrate, and R_{Si} is the eddy current losses in the substrate [36].

Considering the inductor model in Figure 2, the quality factor *Q* of the inductor is given by [10]:

$$Q = \frac{\omega L_s}{R_s} \times \frac{R_p}{R_p + R_s\left[\left(\frac{\omega L_s}{R_s}\right)^2 + 1\right]} \times \left[1 - \frac{R_s^2\left(C_s + C_p\right)}{L_s} - \omega^2 L_s\left(C_s + C_p\right)\right] \tag{1}$$

$$Q = \frac{\omega L_s}{R_s}\left(\text{substrate loss}\right).\left(\text{self resonance loss}\right) \tag{2}$$

$$R_p = \frac{1}{\omega^2 C_{ox} R_{si}} + \frac{R_{si}\left(C_{ox} + C_{si}\right)^2}{C_{ox}^2} \tag{3}$$

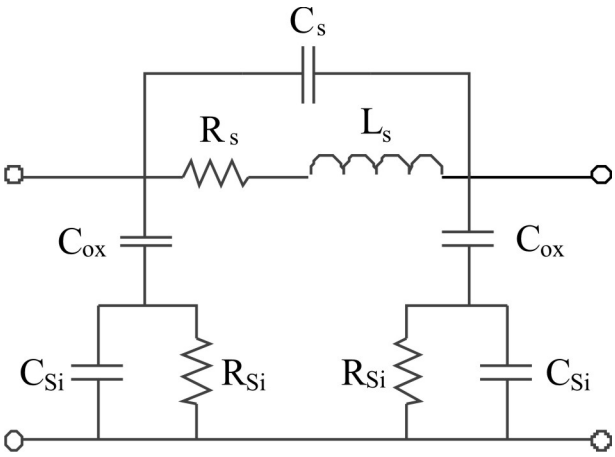
$$C_p = C_{ox} \times \frac{1 + \omega^2\left(C_{ox} + C_{si}\right) C_{si} R_{si}^2}{1 + \omega^2\left(C_{ox} + C_{si}\right)^2 R_{si}^2} \tag{4}$$

$$R_s = \frac{\rho}{\delta w} \tag{5}$$

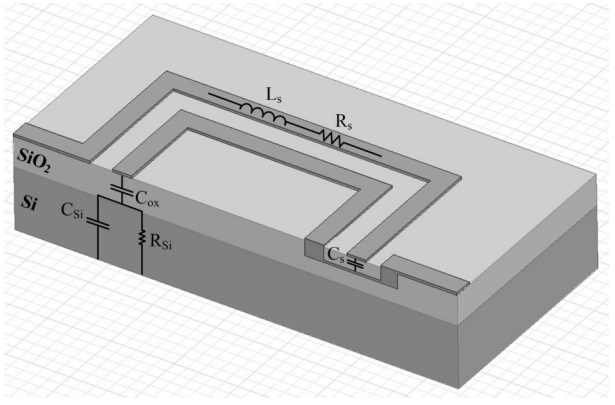
$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{6}$$

where R_s is the resistance per unit length (R_s) and ρ is the metal resistivity in Ω-cm, W is the width of the inductor line, δ is the skin depth, $\mu = 4\pi \times 10^{-7}$ and is the free space permeability, and f is the operating frequency.

Equation (1) is used to calculate the Q factor for the pie model shown in Figure 1. This equation can be divided into three terms: the first term is the simplified equation for Q while all parasitics are neglected. In this term, the Q factor is found from the frequency inductance and series resistance. Hence, the only effective parameter in this term is series resistance, which depends on the metallization. The second and third terms are the substrate loss factor and self-resonance loss factor. For an ideal inductor, these two terms show a value of unity because no parasitic are considered.



(*a*)



(*b*)

Figure 1: General model for planar spiral inductor (*a*) schematic view, and (*b*) perspective view.

According to (1) and (4), the metallization thickness W and the parasitic capacitance C_p are two effective parameters in the Q factor equation. This means that an increase in Q is directly achieved by reducing the series resistance. Using (5), it can be seen that R_s is directly proportional to $\sqrt{f}$ and that reactance is proportional to f (equation 9). Thus, Q is also approximately proportional to $\sqrt{f}$ [36]. Therefore, this parameter is usually more effective when the frequency is low enough. There are several methods to enhance the Q factor using metallization, which will be described in the next section.

In addition to the Q, the parasitic capacitance affects the resonance frequency; the resonance frequency can be achieved by:

$$f_r = \frac{1}{2\pi\sqrt{L_s(C_s + C_p)}} \tag{7}$$

From (7), it can be observed that series resistance has no influence on resonance frequency. The inductor impedance Z_L and corresponding quality factor Q, is achieved by:

$$Z_L = R_s + j\omega L \tag{8}$$

$$Q = \frac{L\omega}{R_s} \tag{9}$$

A reduction in the parasitic capacitance not only pushes the resonant frequency higher (equation 7), but also results in a large reactance (equation 8), and therefore, a high Q inductor (equation 9) at high frequencies.

In a tunable MEMS inductor, in addition to the quality factor, the tuning inductance range is another important parameter. The inductance value depending on the shape of the inductor is calculated using different equations. Most previous works discuss the square shape due to its easy fabrication, but the best results are achieved for a circular spiral inductor. For a single-layer spiral inductor, regardless of its layout shape (square, hexagonal, octagonal, and circular form), a generalized equation for inductance is [37]:

$$L = \left[\frac{\mu_0 N^2 D_{AVG} C_1}{2}\right]\left[\ln\left(C_2/\rho\right) + C_3\rho + C_4\rho^2\right] \tag{10}$$

where N represents the number of turns; μ_0 is the vacuum permeability and is equal to $4\pi x10^{-7}$; ρ is the fill ratio; D_{AVG} shows the average diameter; D_{in} and D_{out} are the inner and outer diameter, respectively, and can be found from Figure 1. C_1–C_4 are the coefficients depending on the layout and their values can be found from [37], depending on whether the inductor is a square, hexagonal, octagonal, or circular type.

Generally, the main parameters in an inductor are: the Q factor, the inductance value (L), the resonance frequency, and the size. Each of these parameters is dependent on some other factors such as metallization

and parasitic capacitances. According to these relations, several methods to enhance the *Q* factor and the tuning range were presented. In the following sections, most of these methods will be discussed.

3 Fixed MEMS inductors and methods to enhance the quality factor

The main research issue for fixed-value MEMS inductor is the quality factor. According to (1) and the discussion in section II, previous works have employed several methods improve the *Q* factor. Here, based on equation (2), the quality factor enhancement methods were divided into three categories: series resistance reduction, substrate loss reduction, and self-resonance loss.

3.1 Series Resistance Reduction

The first term of equation (1) shows that the only effective parameter in this term for improving the *Q* factor is series resistance (R_s). Equation 5 shows that (R_s) is dependent on other parameters, such as: metal resistivity, length, skin depth, and effective area. The effects of these parameters and the relevant previous works were studied.

3.1.1 The Skin Effect Reduction

Applying a time-varying voltage to the spiral inductor, a magnetic field arises from the time-variant current. This causes a current induction in the substrate and tracks. The induced eddy current in the substrate causes the substrate loss. By increasing the frequency from lower frequency to higher frequencies, the domination of a dc current density and its corresponding magnitude of fields exponentially decrease, while the opposing penetrated electric field increases due to the growing eddy current. This is called the skin effect, which cancels the current flows at the center of the conductor and forces it to flow in the outer area (skin). This reduces the effective sectional area of the conductive metal, which results in frequency-dependent growth in the series resistance R_s. The increase rate can be found by the skin depth, which is the effective depth of penetration (δ) of the current [38] and its equation is given in (6). In addition, the flux coupling reduction causes the decrease in the self-inductance value at higher frequencies. The series resistance R_s in (5) can be found with (5), which neglects the skin effect induced by the substrate, but not the skin effect induced by the coil segments. For frequencies of 2 GHz and below, the skin effect is negligible; whereas for frequencies above 2 GHz, the inverse-frequency-dependent skin depth is much less than the conductor's width.

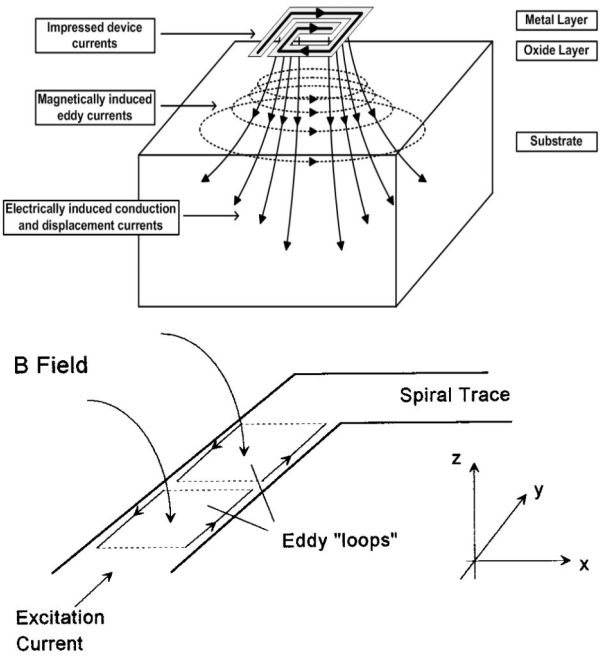


Figure 2: Eddy and displacement current in the substrate induced by the current flow in spiral inductor [39] (top), and self-induced current by skin effect [40] (bottom).

Two spiral inductor circuit models considering the skin effect induced by the substrate were developed by [40] and [41], which are more intuitive and accurate. The estimation of the effective series resistance $R_{s,\text{eff}}$ was given by [40] as:

$$R_{s,\text{eff}} = R_{\text{DC}}\left[1+\frac{1}{10}\left(\frac{\omega}{\omega_{\text{crit}}}\right)^2\right] \tag{11}$$

where R_{DC} is the dc series resistance of the coil and ω_{crit} is the frequency at which the current crowding begins to become significant.

Based on [40], this model was modified by [41] and the following equation for substrate-induced series resistance was developed as:

$$R_{s,\text{eff}} = R_{\text{DC}}\left[1+\frac{\omega^2\left(0.035W^4T^2\sigma^2\mu_0^2\right)}{P^2}\sum_n\left(\frac{n-M}{N-M}\right)^2\right] \tag{12}$$

Figure 2 shows the currents induced by the skin effect and the substrate into the planar inductor. Using the available models based on equations (5), (11), and (12), the quality factor of a spiral inductor was plotted in Figure 3 to compare the calculated *Q*s versus frequency. The top plot in Figure 3 is based on calculated R_S with (5), in which induced skin effect by the substrate is ne-

glected. *N* increase in *Q* can be observed in the given frequency range; however, the *Q* slope shows a decrease because of the induced skin effect by its own segments. The middle and bottom plots show the calculated *Q* from (11) and (12), which show a decrease in *Q* as the frequency increases. This means that the induced skin effect by the substrate cannot be neglected after a determined frequency.

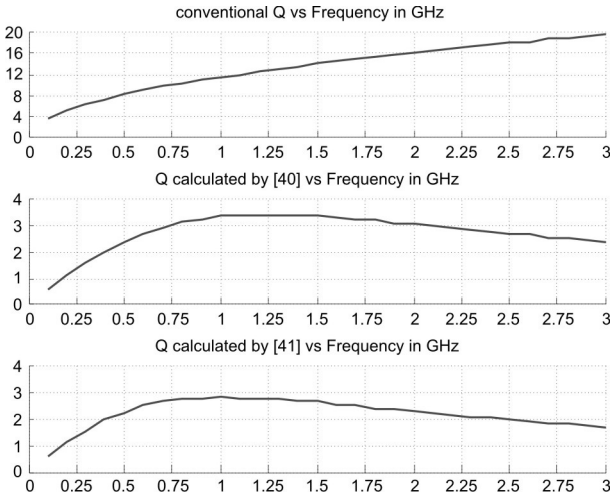


Figure 3: Calculated Q based on self-induced skin effect and substrate-induced skin effect.

Recently, stressed-metal high-*Q* 3-D inductors have been introduced. Dissimilar to the spiral inductors, the magnetic field in these inductors is not perpendicular to the substrate, which causes a reduction of losses associated with eddy currents generated in the Si substrate; thus, very high quality factors up to 1 GHz frequency were achieved. At higher frequencies, the magnetic field penetration into the lossy Si substrate causes a significant decrease of the quality factor. Employing a stressed-metal technology, silicon-based high-*Q* 3-D inductors were fabricated by [14]. The existence of low-k dielectric (SU-STM) materials under the inductors showed the increase in the self-resonance frequency. The simplicity and full compatibility with silicon and compound-semiconductor technologies are the two main advantages of this technique. This also allows the post-processing implementation. In [8], the *Q* factor was controlled with eddy current reduction. Here, the angular distance of the coil θ was displaced from 0 degrees to 90 degrees, as shown in Figure 4. This led to fewer magnetic flux lines, associated with the excitation current, penetrating through the silicon substrate. This results in a decrease of the skin effect and hence, the inductive loss and then quality factor can be tuned. In this work, using the decoupling effect, the *Q* factor was controlled between 2.9–5.2 at 2 GHz with an inductance variation between 8–16 nH.

When θ is 90 degrees, the maximum value for the *Q* factor is achieved because the substrate effect on the skin depth is a minimum; therefore, the inductor displacement can be categorized as two categories of coupling reduction ($\theta < 90^o$) and de-coupling ($\theta = 90^o$). The increase of the distance is an approach for coupling reduction. To achieve the de-coupling, the inductor is displaced in the vertical position, such as in [12]. This approach was based on a fully parallel batch process. Another vertical inductor fabricated by [13] shows the improvement in *Q* factor; in this work, plastic deformation magnetic assembly (PDMA) technology was employed to implement the inductor vertically (see Figure 5).

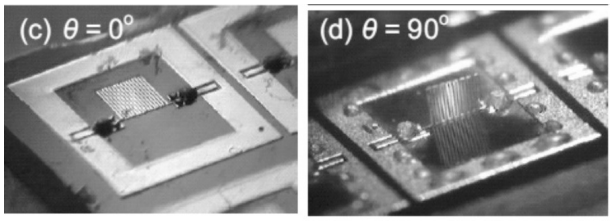


Figure 4: *Q*-controlled spiral inductor by variable angular distance [8].

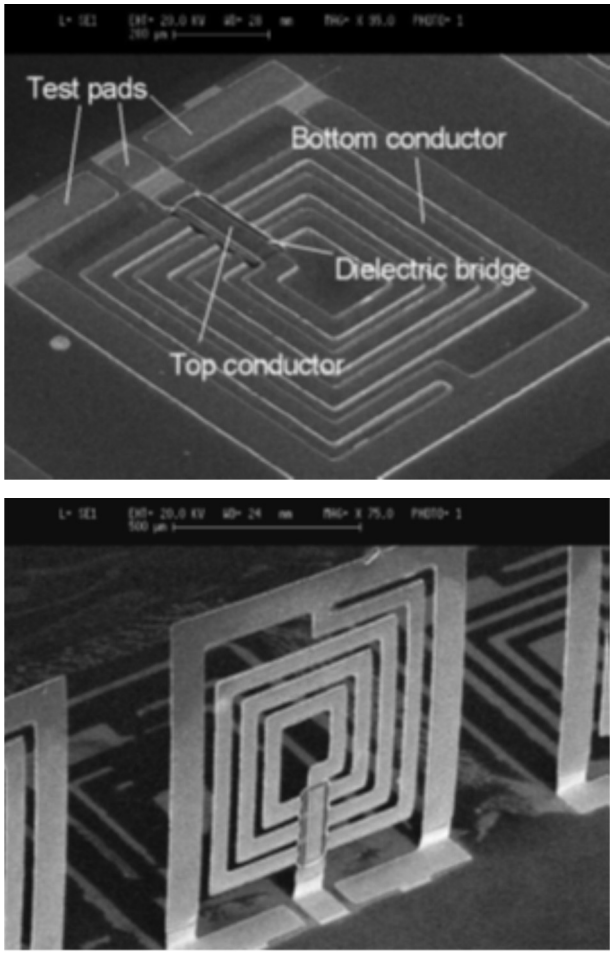


Figure 5: PDMA vertical spiral inductor [13].

When the inductor lies on the substrate without any distance, a *Q* factor of 3.5 is achieved at 1 GHz; this is the minimum value for the Q of this inductor. However, in the vertical position, the *Q* factor is 12 at the same frequency.

The approaches in [12] and [13] can be analyzed for their extensive separation between coil and substrate (a few hundreds of μm); in this case, it is possible to analyze these approaches in the suspended inductor technique in the substrate loss reduction section.

3.1.2 High Conductivity Metal

According to equations (1) and (5), the metal resistivity influences the *Q* factor. Figure 6 presents the calculated *Q* while various metals are employed for implementation of the coil segments. Here, copper shows the highest conductivity compared with gold, and aluminum shows the highest *Q* factor because $\omega L/R_s$ increases with a decrease in series resistance R_s.

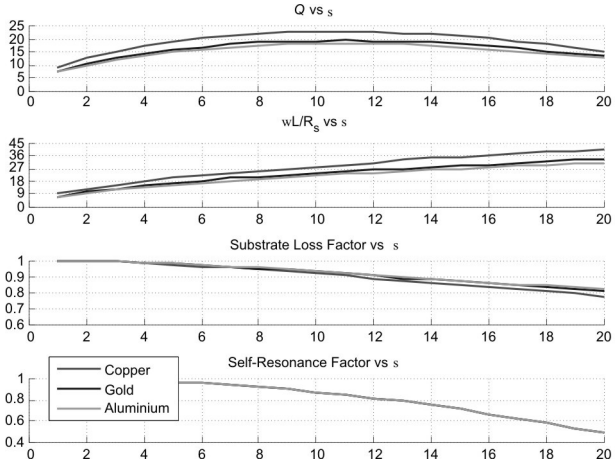


Figure 6: Calculated Q based on different conductive coil metals

Using high conductivity metal such as copper in the inductor is the most common technique to reduce metal loss in the inductor [42]. In addition to the material, the limited metallization thickness is one of the parameters that strongly influences the RF performance [17].

3.1.3 Width and Length Optimization

In addition to the conductivity of metal, the thickness and the width of the metal are also effective parameters to improve the *Q* factor because they influence the series resistance of the coil. Figure 7 shows the quality factor while the ratio of L/W sweeps from 50 to 450. The term $\omega L/R_s$ increases with a decrease of the L/W ratio; however, any increase in the L/W ratio causes an increase in the substrate loss factor and the self-resonance factor. It can be observed that the quality factor follows the behavior of the term $\omega L/R_s$ because it is more dominant than the other two factors in this specific case.

An optimum width and *Q* ratio was studied by [19]. In this work, a 3D inductor with different widths of metal was fabricated and measured. It was shown that the increasing width leads to an increasing quality factor while the resonance frequency remains constant. A comparison of the *Q* factor between several fabricated inductors was presented in terms of the change of their turn and width (see Table 1).

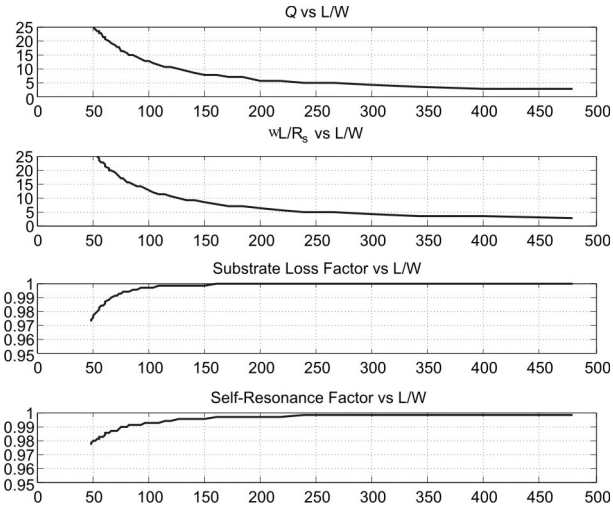


Figure 7: Calculated Q versus swept L/W ratio

Table 1: A comparison of q factor between fabricated inductors with different l/w ratio by [19]

Number of turns	Width (μm)	L (nH)	Quality factor	SRF (GHz)
1	25	1.23	38.2@7GHz	>40
1	35	1.22	51.6@7.5GHz	>40
1	45	1.16	137.5@12GHz	>40
2	25	2.60	30.5@3GHz	33
2	35	2.45	32.8@3.5GHz	35
2	45	2.20	66.1@7.5GHz	38

It should be noted that this method has some disadvantages, which should be considered in the calculation and design. Increasing the width causes an increase in the capacitive coupling; this might result in an undesirable performance of *Q*. [43] has mentioned this problem based on results of two identically fabricated inductors with different widths. The inductors were fabricated on silicon with a silicon oxide substrate. The metal used was copper, the number of turns was two, and the space between the two metals was 10 μm. The achieved *Q* factor for the inductor with a width of 80

μm was 10; however, the Q factor for the other inductor with a width of 50 μm was 17 at the same frequency of 1 GHz.

3.2 The Substrate Loss Reduction

According to equation (1), when the term for substrate loss factor is unity, the maximum quality factor can be achieved. To approach the unity value for the substrate loss factor, it is required that R_p be a very large value ($R_p \to \infty$) Equation (2) shows that when R_{Si} is equal to zero or infinity, R_p will limited to infinity. In addition, $C_{ox} = 0$ can cause an infinite-value of R_p. Based on this knowledge, to increase the value for R_p, four methods are conventional: (a) using high resistivity silicon [16], (b) etching away the silicon substrate [10, 19], (c) patterned grounded shields [15], and (d) increase the distance between the substrate and metal by suspending the coil [11]. The first two methods are usually used to realize $R_{Si} = \infty$, the third method is used to realize $R_{Si} = 0$, and the final method is used to realize $C_{ox} = 0$.

Figure 8 presents the effects of methods (a) to (c) on the quality factor. As can be observed, the high-resistivity substrate and patterned-grounded shields improve the quality factor compared with the conventional low-resistivity silicon substrate without any shields.

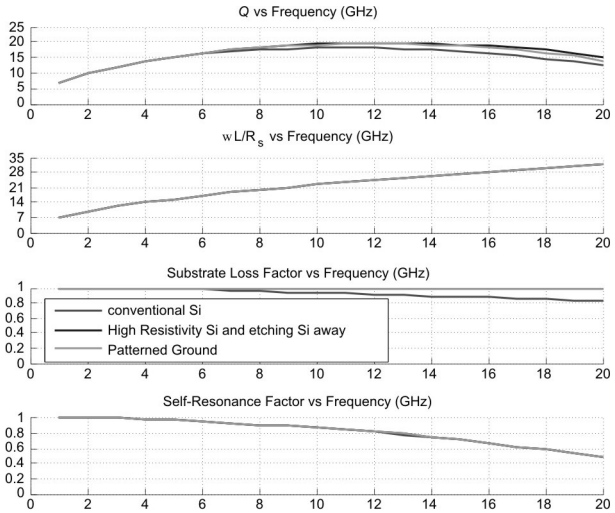


Figure 8: The calculated *Q* for different methods of substrate loss reduction

3.2.1 High-Resistivity Substrate

Increasing the substrate resistivity has the greatest effect on the second term in (1). As much of the substrate resistivity approaches infinity, it causes this term to approach unity. A low-resistivity substrate results in an inductor with high loss and therefore, low quality factor. In addition, the self-resonant frequency is very low because the Si substrate with its high dielectric constant introduces increased parasitic capacitances [16]. The resistivity of substrate R_{Si} is dependent on the employed substrate material. The substrate can be chosen from materials such as SiO_2/Si, high-resistivity silicon (HRS), glass, and quartz, the resistivity of each is increasing, respectively [38]. To obtain high-performance inductors, many approaches using: highly-resistive silicon with micro-machining technique [4], a glass layer [5], a thick polyimide layer [6], and a multilevel interconnection in the silicon substrate [7]–[9] have been reported, but their results are much lower than in [44].

In [44], a thick lower-cost and lower-process-time oxidized porous silicon (OPS) layer on s silicon substrate to fabricate a high-performance planar inductor was proposed. As a replacement for direct oxidation of bulk silicon, the short-time oxidation process of porous silicon was employed to make the oxide layer thicker than 30 μm by the reaction of the side wall of pores. This thick oxide layer prevents any harmful effects on the performance of the fabricated inductor because of the silicon.

In [45], to reduce the undesired effects of silicon, SOS (silicon on sapphire) technology was employed, which is from the SOI (silicon on insulator) family of CMOS technologies. In this approach, a hetero-epitaxial process for integrated circuit manufacturing that consists of a thin layer (typically thinner than 0.6 micrometers) of silicon was grown on a sapphire (Al_2O_3) wafer. As conventional models are less accurate for inductors created in newer RF-compatible processes with very high resistivity bulk material such as SOS, appropriate modeling for this approach was carried out by [45]. In this work, the simple four- and five-element frequency independent models with small-to-moderate sized (< 300 um) inductors to be fabricated in SOS and a six-element model for larger, high-*Q* spirals (e.g., 600 μm) were introduced. They accurately model the increase in resistance versus frequency from current crowding. The models show that substrate loss is reduced to negligible values relative to trace resistance loss.

A new inductive coupled plasma (ICP) etcher was employed by [17], dedicated to dielectrics anisotropic deep dry etching in order to discover a new method based on patterning the inductor directly in a quartz substrate. The major benefit of this method is the high resistivity of the quartz (2×10^{14} Ωcm at 20 °C), which greatly decreases the substrate-induced RF losses.

3.2.2 Etching Substrate Away

Etching a cavity underneath the inductor is another approach to meet $R_{Si} \to \infty$ and hence, $R_p \to \infty$. This technique greatly improves the quality factor. [43] used a

dry etching technique to remove the seed layer while it is perfectly contacted to the pillars. This approach produced a great improvement with a peak *Q*-factor of 17 at a frequency of 1 GHz. The inductance is about 3.2 nH in the frequency range between 50 MHz and 3 GHz while the resonance frequency is about 6 GHz.

Sheng-Hsiang Tseng proposed a fully CMOS-compatible MEMS inductor in TSMC 0.18-μm 1P6M CMOS process and also Chip Implementation Center (CIC) micromachining post process to remove the oxide between the coil metals and the silicon substrate under the inductor by utilizing dry reactive ion etching (RIE). In this work, a 1.88-nH micro machined inductor with a *Q* factor of over 15 was achieved at 8.5 GHz, and the improvement is up to 88% in maximum quality factor [46].

In [10], the Silicon substrate of an MMIC inductor in 0.35 μm CMOS process was removed using a post-process silicon dioxide RIE. TMAH (tetra methyl ammonium hydroxide) is then used to remove the silicon substrate underneath the inductor to achieve a suspended spiral inductor. The advantage of the post processing is its compatibility with the CMOS process.

There are several works that have used identical techniques to improve the *Q* factor; however, they have applied different processes [26, 47, 48]. The main issue in these approaches is the restricted separation that can be obtained (only tens of μm or less). In addition, substrate etching must be carried out in a compatible process, but the concerns about the reduced mechanical stability of the substrate remain [7].

3.2.3 Patterned Grounded Shield

Another method to reduce the substrate effect is to use a patterned grounded layer between the spiral coil and the substrate in order to cause $R_{Si} \to 0$ and thus, $R_p \to \infty$. Hence, the substrate loss factor moves to the unity value. Using this method, an enhancement in the *Q* factor was achieved by employing patterned ground by [15]. The effect of using a patterned ground can also be clarified from the effects of increasing the effective area of the segments. However, this increases the parasitic capacitive coupling to ground [49].

3.2.4 Increase of Distance between the Substrate and the Coil (Suspended Inductor)

One of the effective parameters in the substrate loss factor is C_{ox}; this parameter can make the substrate loss factor close enough to unity while it itself limits to zero. By knowing the basic equation of capacitance, C = $\varepsilon A/d$, where ε, *A*, and *d* are the dielectric, area of windings, and distance between windings and the substrate, respectively, it can be observed that any increase in distance causes a decrease in capacitance. Figure 9 illustrates the quality factor of a spiral inductor with different windings-substrate distances. It simply shows that the substrate loss factor improves when the distance increases.

A suspended spiral inductor, shown in Figure 10, was fabricated with MEMS technology on a glass substrate by [11], in which the coil was sustained with T-shaped pillars.

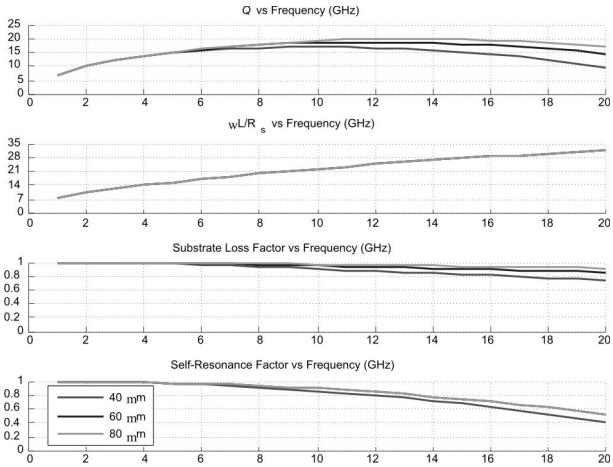


Figure 9: The calculated *Q* for different displacement distances

In the fabrication process, fine polishing of the photoresist was used to simplify the processes and ensure that the seed layer and the pillars made perfect contact. Dry etching techniques were employed to remove the seed layer. The inductor operates in a frequency range of 0.05–10 GHz, when the suspended height is 60 μm, the maximum *Q* factor is 37 for 4.2nH at 2 GHz. The result of this study is that the maximum quality factor grows gradually with an increase of the suspended height.

A substrate removal process using CMOS_MEMS can be found in [10]. In this work, a post-process was adopted to remove the silicon substrate under the manufactured spiral inductor in order to enhance the *Q*-factor of the inductor. This post-process utilizes CHF_3/O_2 RIE to etch the sacrificial layer of silicon dioxide, and then TMAH is used to remove the underlying silicon substrate. The suspended spiral inductor achieved a measured *Q*-factor of 15 at 11 GHz and a measured inductance of 4 nH at 25.5 GHz.

3.3 Self-Resonance Loss Factor

In the third term of equation (1), there are two main parameters C_s and C_p, which cause the self-resonance loss (SRL) factor to approach unity. In this case, the unity

SRL factor occurs when these two parameters are zero or near to zero.

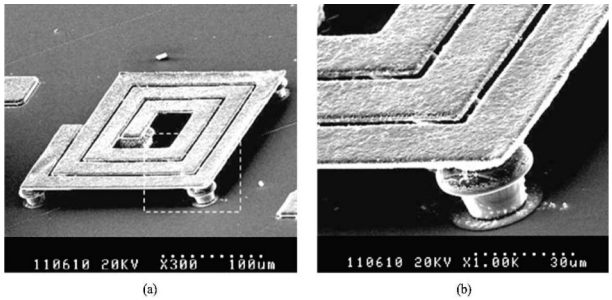


Figure 10: Suspended spiral inductor by [11]

The parasitic capacitance C_s is limited to zero when the spaces between the segments of the winding are not that close. In addition, C_p depends on C_{ox}, such that a zero-value C_{ox} leads to a zero-value C_p; the methods are very similar to the ones described for substrate loss factor when C_p approaches to zero, such as substrate removal and suspended spiral inductor.

4 Tunable MEMS inductor and methods to increase the tuning range

Tunable MEMS inductors will find their way to market by 2015 in reconfigurable mobile handsets, reconfigurable satellite communications and base stations, and 60 GHz WLAN applications [35]. A tunable MEMS inductor of a small size with high *Q* factor and ability of tuning is the required component in most wireless applications, such as reconfigurable LNAs, VCOs, and Filters.

In previous discussions, the quality factor of the inductor was discussed in detail. Here, a discussion around the tuning range will be presented. The tuning range parameter is the other important value for inductor design. There are some factors that affect the tuning range and are used as methods to enhance it. These methods are discussed in the following.

4.1 Change of the Number of Turns

Here, equation (10) is used as the reference equation for the inductance of the spiral inductor. From (10), the factors that can affect the inductance in order to control the inductance and hence, the tuning range, can be extracted. Inductance is directly proportional to the square of the number of the turns N^2. Therefore, controlling the number of turns can provide control of the inductance value. Some previous works used this property to tune the inductance by their own techniques. Figure 11 illustrates the inductance variation while the turns are switched.

$$M^{+} = \frac{\mu_0 L(N-1)}{4\pi} \times \ln\sqrt{1+\left(\frac{L}{4NS}\right)^2} + \frac{L}{4NS} - \sqrt{1+\left(\frac{4NS}{L}\right)^2} + \frac{4NS}{L} \quad (13)$$

$$M^{-} = \frac{\mu_0 LN}{4\pi \times 214} \quad (14)$$

4.1.1 Switched Turns of Inductor

In this method, inserting switches (or relays) between the turns of the inductor causes it to bypass a specific number of turns and hence, change the inductance. The structure of such an inductor is shown in Figure 12(*a*) [25].

This method was improved by using MEMS switches instead of the micro-relays in [9]. The model of the fabricated tunable MEMS inductor can be found in Figure 12(*b*). Here, an RF MEMS switch was employed to bypass a determined number of turns. The proposed tunable inductor was used to reconfigure the bandwidth of Bulk Acoustic Wave (BAW) ladder filters. From the simulation, it was realized that use of this method increases the filter bandwidth by 25%.

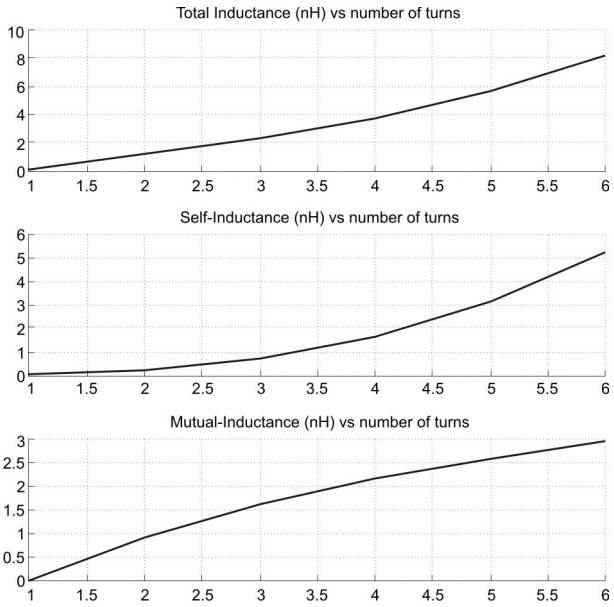
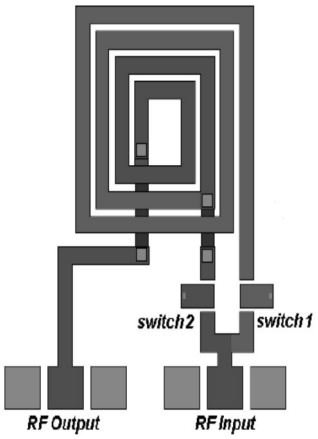


Figure 11: Inductance variation versus number of turns

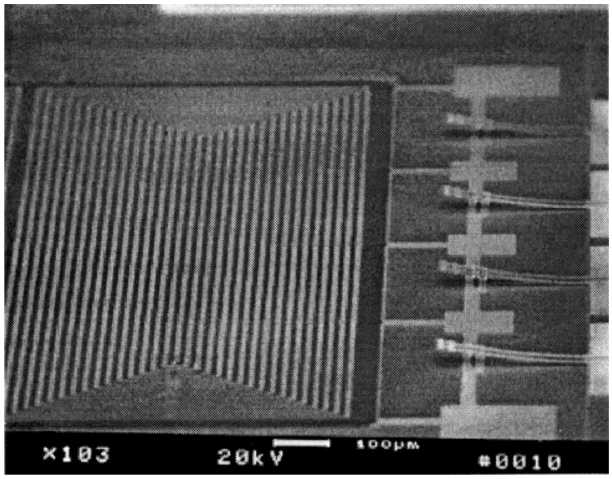
The measurement results showed an inductance of 4 nH when the first switch was activated and an inductance of 1 nH when the second switch was activated at a frequency of 3 GHz. The switches gave a sufficient operation for a frequency range of 1–5 GHz.

4.1.2 Use of Conductive Liquid

One of the novel methods for tunable inductor implementation is to use conductive material in order to by-



(a)



(b)

Figure 12: *(*a) A switched-turn variable inductor by [25], (b) A MEMS switched-turn variable inductor by [9]

pass the specific number of the turns. This method can be found in [20], in which the variable inductor contains a planar spiral inductor, a micro pump, and conductive liquid metal (Mercury), and all of these were implemented in one single chip. According to the direct proportionality between the inductance and the square of the number of turns, using voltage electrodes makes the mercury move between the spaces of the intercoil, such that part of intercoil becomes short-circuited. This phenomenon results in a reduction of stored magnetic energy and indeed, the inductance. The tuning range in this work is above 100% at 8 GHz (see Figure 13).

4.2 Change of Coupling Capacitance

4.2.1 Change of Dielectric Value (Cross-Talk Strength)

Another novel method was introduced by [20] in which the capacitive coupling between the inter-spires is varied by a reduction of the stored magnetic energy; this occurs when liquid moves between the metal spires.

The liquids that can be employed in this method are divided in two categories: liquid metals and ionic liquids. Liquid metals have conductivity a thousand times higher than ionic liquids, but ionic liquids are much easier to handle. Mercury is the most famous and most often used liquid metal in previous works, but it is toxic and harmful to the environment.

In [22, 23], this method was implemented with various liquids. A very high tuning range of up to 107% was achieved by employing salted water at 1.6 GHz frequency with a *Q* factor of 12. The structure of this variable inductor is shown in Figure 14.

The effect of salts on water permeability varies depending on the salts and the species (Figure 15). While most salts, such as: KCl, KNO_3, $(NH_4)_2SO_4$, $NaNO_3$, NaCl, NH_4Cl, $AlCl_3$, and NH_4NO_3) had no pronounced effect, $CaCl_2$, K_2CO_3, and Cs_2CO_3 were very efficient in increasing cuticular water permeability's of *H. helix, P. laurocerasus*, and *L. esculentum* (Figure 16). The effects of $CaCl_2$ were 2.41 ± 0.26, 1.29 ± 0.11, and 1.55 ± 0.31 for the three measures. The effects of K_2CO_3 were 1.43 ± 33, 1.68 ± 0.13, and 2.63 ± 0.28, and the effects of Cs_2CO_3 were 1.52 ± 0.18, 2.60 ± 0.29, and 2.50 ± 0.48 [50].

Figure 16 presents the simulation for a liquid tunable inductor using salted water. The salted water is injected in a tunable liquid inductor, such as in Figure 14.

As the liquid moves in the turns of the inductor, the total inductance, including the self-inductance and mutual inductance, changes. In Figure 16, the top plot shows the variation of the total inductance when the water is injected in turns 1 to 6.

The middle plot shows the self-inductance for the turns that salted water is injected and the turns in which air still remains. The bottom plot shows the mutual inductance variation when more salted water is injected.

4.2.2 Changing Coupling between the Substrate and the Coil

When the coil is implemented on a low-resistivity substrate, the planar inductor geometries present both a desired inductance and a parasitic capacitance. A reduction in the size of the winding metals leads to a reduction in parasitic capacitance, but in addition, to an increase in the resistive loss. This method is useful for improving the tuning range and also the *Q* factor, and is based on the coil structure displacement away from the substrate. This causes a reduction in capacitance between the coil and the substrate while the resistance remains constant.

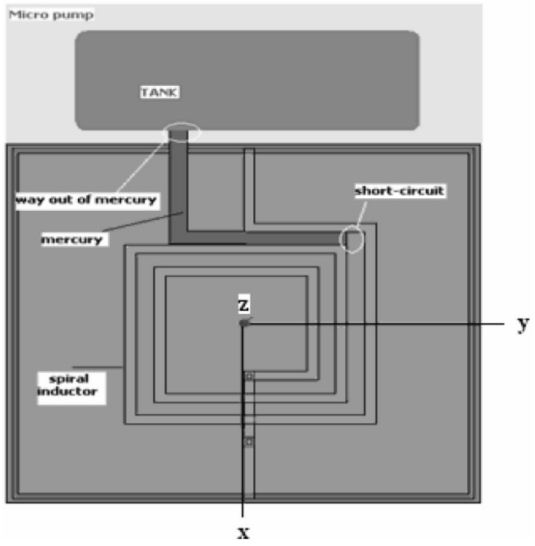


Figure 13: Conductive liquid inductor by [20]

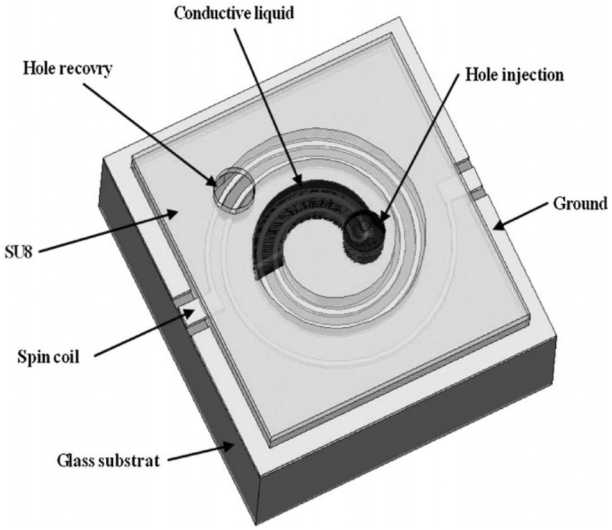


Figure 14: Liquid variable inductor with salted water [22, 23]

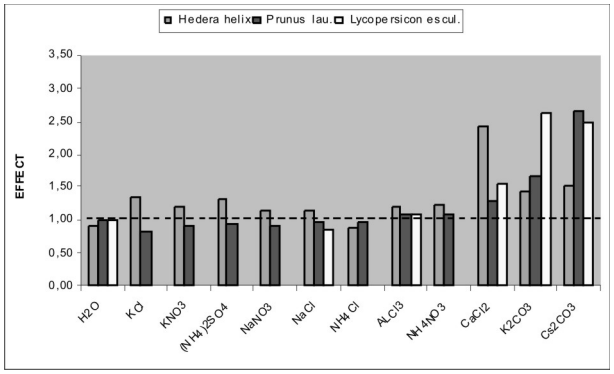


Figure 15: Effects of different salts on water permeability [50]

In [24], a MEMS tunable inductor was assembled using an interlayer stress, such that it causes portions of the inductor to bend away from the substrate in a controlled manner. This is allowed by fabricating the inductor in the substrate plane over a sacrificial layer with anchor points at both ends connecting through to the substrate.

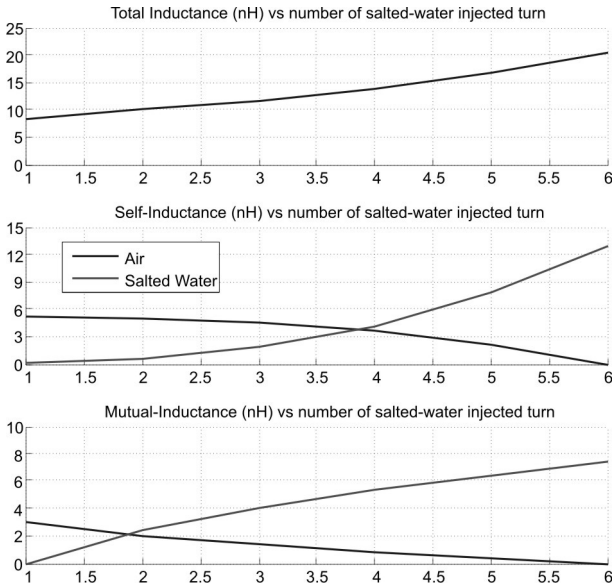


Figure 16: Inductance variation versus number of turns with injected salted water

Employing two or more deposited material layers with dissimilar stresses, the inductor can be forced to curl away from the substrate while the sacrificial layer is removed.

Following the same method, an spiral inductor was fabricated by [21]. A tunable inductor was achieved based on the structure shown in Figure 17. In this work, the tunable MEMS inductor, based on the bimorph effect, was fabricated with amorphous silicon (a-Si) and aluminum structure layer on a-Si and c-Si substrates at low temperature (150 °C). Because of interlayer stress between the two layers (films), the coil warps. This stress is controllable by film thickness and hydrogen content. When a voltage is applied between the terminals, due to the difference in thermal expansion coefficient (TEC) of the two materials, the structure deforms in a controllable manner. A tuning range of 32% (5.6–8.2 nH) was achieved at a frequency of 4 GHz with a *Q* factor of 15 and resonance frequency of 7 GHz.

4.3 Change of the Mutual Inductance (Coupling Coefficient) between Two Coils

By controlling the magnetic coupling coefficient between two different inductors, a tunable inductor is

achieved. Usually, for two identical inductance L_0, the mutual inductance *M*, can be achieved by [51, 52]:

$$M = L_0 \times K \tag{15}$$

where the coupling factor is given by *K*. No matter if the inductors are connected in parallel or series, when the current flows in two adjacent lines, the same or opposite direction will happen.

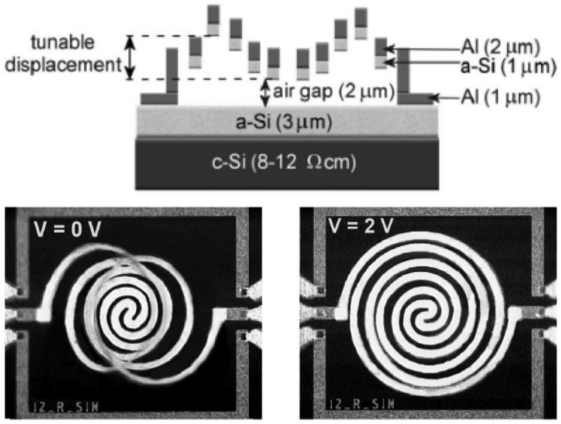


Figure 17: Tunable MEMS inductor based on bimorph effect by [21]

For the same direction, M is positive and for opposite, M is negative. In theory, the value of *K* is between 0 and 1.

In this method, two or several parallel inductors are fabricated, one of which is in flow and the other are switched off or moved away with different actuators. The motion/switching of one inductor changes the mutual inductance between that inductor and the fixed inductor by changing the coupling factor between two coils. This results in a change in the overall inductance by $L = M / K$. Figure 18 shows work by [5] that uses switched inductors to control the mutual inductance and hence, the overall inductance. When all the micromechanical vertical switches are open, the inductance seen from port one is L_1. Inductors at port two are different in size and thus, have a different mutual inductance effect on port one when activated. The number of different possible states *P* of the inductance can be achieved by:

$$P = 1 + n(n+1)/2 \tag{16}$$

where n represents the number of the inductors at port two.

Equivalent inductance and series resistance, seen from port one, can be achieved as follows [5]:

$$L_{eq} = \left(L_1 - \sum_{i=2}^{n+1} \frac{b_i K_i^2 L_i^2 \omega^2}{R_i^2 + L_i^2 \omega^2} \right) \tag{17}$$

$$R_{eq} = \left(R_1 - \sum_{i=2}^{n+1} \frac{b_i R_i K_i^2 L_1 L_i^2 \omega^2}{R_i^2 + L_i^2 \omega^2} \right) \tag{18}$$

where $b_i = 0$ or 1, L_i gives the inductance value of the secondary inductors, R_i denotes the series resistance of each secondary inductor in addition to the contact resistance of its corresponding switch, k_i represents the coupling coefficient, b_i is the state of the switch with a value of 1 or 0 depending on whether the switch is on or off, respectively, and ω gives the angular frequency. The maximum effective inductance happens when all the switches at port two are on. Here, the tuning range can be achieved from [5]:

$$\%tuning = \sum_{i=2}^{n+1} \frac{b_i K_i^2 L_i^2 \omega}{R_i^2 + L_i^2 \omega^2} \times 100 \tag{19}$$

using this method with two inductors at port two, the maximum tuning range of 47% was achieved at 6 GHz for a 1.1 nH silver inductor [5].

Using equation L_{eq}, the variation of inductance when four inductors on port two are switched into the circuit, is plotted in Figure 19. The x-axis shows the state of the switches for inductors L_2 to L_5, which are sorted by descending inductance values. The maximum inductance happens when no inductor is switched ('0000'), which is equal to L_1. When all inductors are switched into the circuit ('1111'), the minimum inductance occurs. Theoretically, it can be seen that by switching inductors, a linear variation of inductance can be achieved to some extent. In this simulation, a tuning range of 98% was achieved with four switched inductors, while a value of 68% for the tuning range can be achieved for two switched inductors. This is a value close to the tuning range achieved by measurement in [5]. Using the mutual inductance adjusting method, a tunable inductor was proposed by [53, 54]. In this work, a MUMPS process was employed, which is used for thin metal layers deposited on polysilicon. The main idea in this work is the displacement of the moving inductor away from the substrate.

Two inductors in parallel were fabricated, in which the inner inductor is fixed on chip and the outer inductor is moving off the substrate by outstanding stress between the metal and the polysilicon layer. The outer inductor is attached to a beam that is connected to an array of thermal actuators. By actuating the array, the beam bends and the outer inductor is lifted up. The mutual inductance and hence, the total inductance are

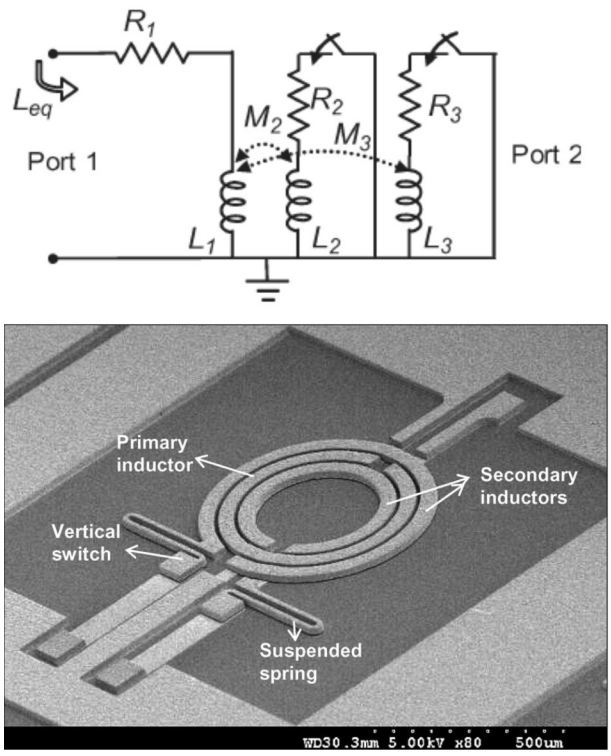


Figure 18: Tunable inductor using mutual inductances activated by micromechanical switches to achieve four discrete values [5].

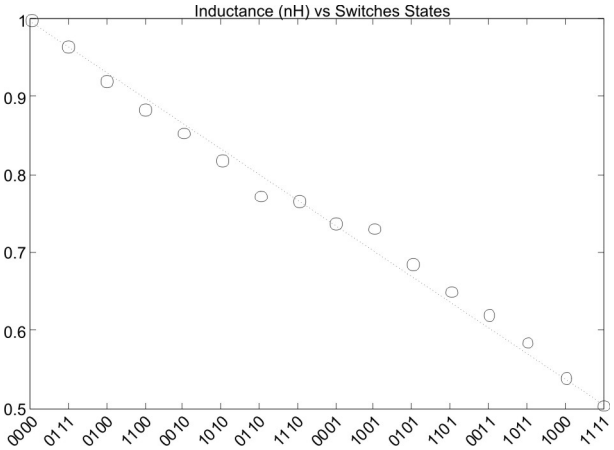


Figure 19: Inductance variation versus different states of mutual-controlled inductor with four peripheral coils

tuned by the control of the angle that separates the two inductors.

Using the same method, a tuning range of 30% was achieved by [55] at a frequency of 7 GHz with a resonance frequency of 35 GHz. The maximum *Q* factor was 25. A CMOS-compatible process was used for the fabrication of this inductor. This inductor also works with thermal bimorph structures; however, it can be replaced with electrostatic or piezoelectric actuators.

Using an identical technique, a tunable inductor was implemented by [27]. In this work, the inductance is controlled by the primary coil. The secondary short-circuited coil is magnetically coupled to the primary one. The magnetic flux relation between the coils induces eddy currents in the secondary coil. By changing the magnetic coupling between the inductors, the equivalent inductance seen at the primary port is changed (see Figure 20).

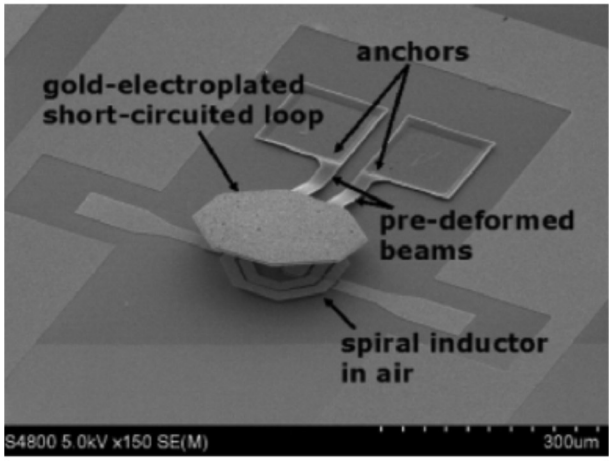


Figure 20: Mutual-controlled variable inductor with magnetic flux control of the secondary coil by [27]

4.4 Change of the Magnetic Flux

4.4.1 Change of the Permeability

Changing the permeability of the core is another approach to implement a tunable inductor. This method has been used mostly for 3D solenoid inductors in previous works. In this type of inductor, the core material can be air, but also any ferromagnetic metal. With different core materials, different inductance values can be achieved. In addition, moving the core changes the magnetic field and hence, changes the inductance.

Using this property, several different types of tunable MEMS inductor were implemented. One of the earlier works was [31], in which an electrically tunable RF inductor, based on a planar solenoid with a thin-film ferromagnetic (FM) core (NiFe), was realized. Variation of inductance was achieved by employing an additional dc current through the same device and thus, altering the effective permeability of the FM core caused a shift in inductance. For inductance ranges of 1 to 150 nH, tuning ranges of 85%, 35%, and 20% were attained at 0.1, 1, and 2 GHz, respectively.

Figure 21 shows another work by [29, 30] in which a solenoid inductor with a Piezomagnetic core was fabricated. The central part of the PZT bridge extends or shortens depending on the sign of the DC voltage V

(typically from 1 to 10 volts) applied on each pair of sided-electrodes. This causes a transfer of uniaxial tensile or compressive planar stress σ_{uniax} to the ferromagnetic core, whose permeability μ_{dc} alters as a result of the magnetoelastic effect. The permeability and consequently, the inductance was controlled through the magnetoelastic field, denoted here as the H_p pressure field.

$$\mu_{dc}(V) = \frac{M_s}{H_{eff} + H_p(V)} \tag{20}$$

$$H_p(V) = \frac{3}{M_s}\lambda_s \times \sigma_{uniax}(V) \tag{21}$$

$$H_{eff} = H_K + H_d \tag{22}$$

where H_k and H_d are the induced uniaxial anisotropy, and the demagnetizing field determined by the composition of the material and by the geometry of the core, respectively. Based on the sign of σ_{uniax}, H_p can be positive or negative, having a high saturation magnetization M_s = 1.8 T and an intermediate positive saturation magnetostriction λ_s=20x10^{-6}.

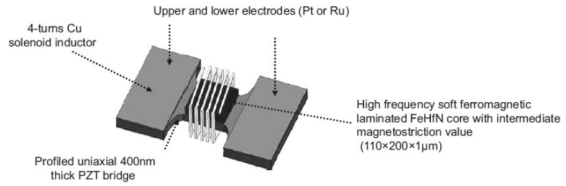


Figure 21: Solenoid inductor with permeability-controlled Piezomagnetic core [29, 30]

The following equation shows the relationship between the frequency and the permeability by using the general Landau-Lifshitz-Gilbert (LLG) equation achieved for thin film ferromagnetic film:

$$\mu(\omega) = 1 + \gamma M_s \left[\frac{\gamma H_{eff} + \gamma M_s + j\omega\alpha}{[\gamma H_{eff} + j\omega\alpha][\gamma M_s + j\omega\alpha] - \omega^2} \right] \tag{23}$$

where Ms gives the saturation magnetization and Heff is the total effect field, α is phenomenological damping constant, γ is the gyromagnetic ratio, and *ω* is the frequency of operation.

In the latest work, using the permeability property, a spiral planar inductor with a movable magnetic core of Ferrofluid, shown in Figure 22, was implemented by [28]. A variable planar inductor based on Ferrofluid actuation was reported. Here, the distribution of the permeability over the spiral inductor was adjusted by the movable Ferrofluid magnetic core. Ferrofluid in a reservoir created on the inductor is displaced using magnetic field gradients produced by another planar coil (actuation coil) aligned to the inductor. A bias field is used to enable repelling of the fluid from the inductor. The tuning range is 16% at 320 MHz and a maximum quality factor is 23 at 60 MHz.

4.4.2 Counteractive Magnetic Field Induction

In this technique, variable inductance is achieved by moving a metal plate on top of the coil. A MEMS actuator is usually used to move this plate. The controlled shielding of the magnetic flux varies the inductance. The parallel-plate actuator forms a capacitor and thus, current does not flow between the electrodes. A counteractive magnetic field according to Lenz's law is induced by entering the magnetic flux of the spiral inductor into the metal plate and introducing eddy currents.

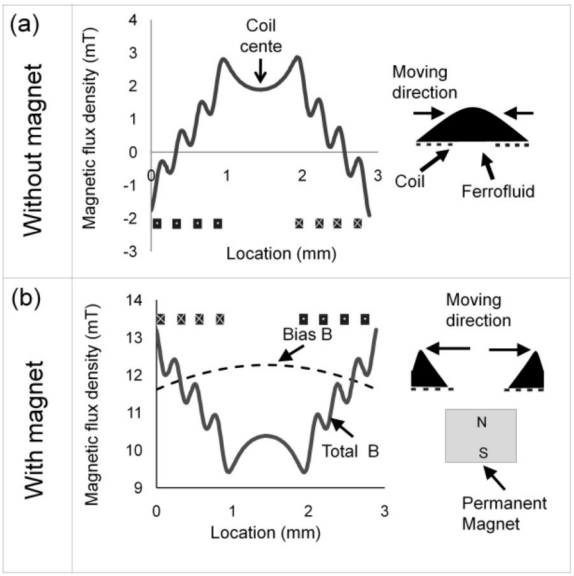
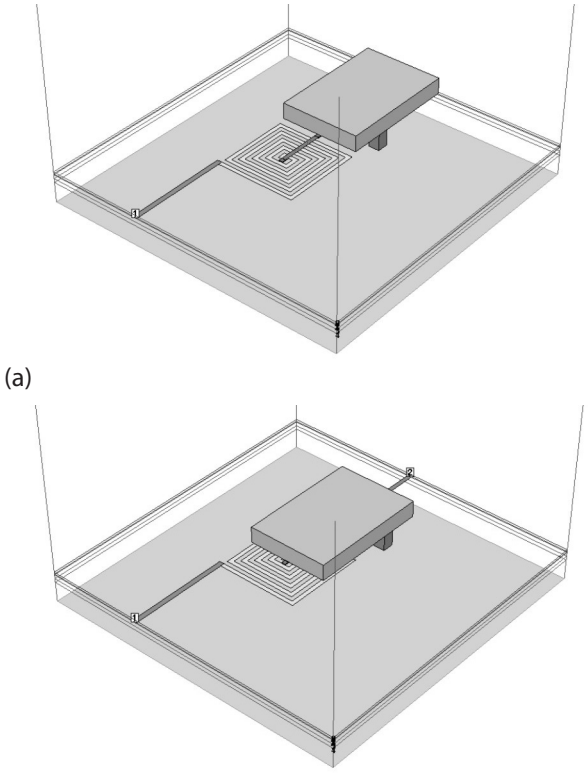


Figure 22: Variable planar inductor with movable Ferrofluid magnetic core [28].

The magnetic flux is shielded by the metal plate. This causes the metal plate's height h to decrease and inductance varies according to *h* [33].

An on-chip high-*Q* variable spiral inductor embedded in a wafer-level chip-scale package (WL-CSP) was proposed by [32] with a MEMS-actuated moving metal plate. At 2 GHz, the measured inductance varies from 4.80 to 2.27 nH, i.e., the variable ratio is 52.6%. The maximum value of the quality factor is 50.1. Figure 23 shows this inductor modeled in Sonnet EM simulator. The simulated inductance and quality factor for two different position of the shield are given in Figure 24.



(a)

(b)

Figure 23: Variable inductance with controlled shielding of the magnetic flux: (*a*) not shielded, (*b*) half shielded in Sonnet.

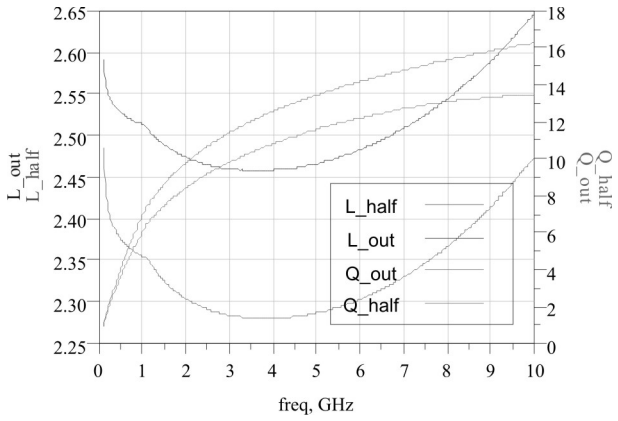


Figure 24: simulated inductance and quality factor for non-shielded (indexed with *out*), and half shielded (indexed with *half*)

5 Conclusion

This paper focused on exploration of the existing methods for the improvement of *Q* factor and tuning range of novel MEMS inductors. Based on the equations for *Q* and inductance values, these methods were categorized and various analyses were given in MATLAB and Sonnet to show their partial and overall performance. The achieved simulation results were close enough to the measurement results of inductors previously fabricated in earlier works, which were reviewed. Thus, the reader can choose the appropriate method based on the performance and complexity and then, study the equations and simulation results for any future enhancement.

6 Acknowledgment

Authors would like to thank Universiti Sains Malaysia research university (RU) grant No. 1001/PELECT/814168. Special acknowledgment to Universiti Sains Malaysia research university (RU) grant No. 1001/PELECT/814107 and Universiti Sains Malaysia ERGS grant No. 203/PELECT/6730112 for the funding of this work.

7 References

1. W. C. Tang and Y. L. Chow, "Inductance formula of a square spiral inductor on grounded substrate by duality and synthetic asymptote," 2002, pp. 2069-2072.
2. J. Zeng, A. Pang, C. Wang, and A. Sangster, "Flip chip assembled MEMS inductors," *Electronics Letters,* vol. 41, pp. 480-481, 2005.
3. I. Zine-El-Abidine, M. Okoniewski, and J. G. McRory, "A new class of tunable RF MEMS inductors," 2003, pp. 114-115.
4. I. Zine-El-Abidine, M. Okoniewski, and J. G. McRory, "RF MEMs tunable inductor using bimorph microactuators," 2005, pp. 436-437.
5. M. Rais-Zadeh, P. A. Kohl, and F. Ayazi, "MEMS switched tunable inductors," *Microelectromechanical Systems, Journal of,* vol. 17, pp. 78-84, 2008.
6. S. Pinel, F. Cros, S. Nuttinck, S. W. Yoon, M. Allen, and J. Laskar, "Very high-Q inductors using RF-MEMS technology for System-On-Package wireless communication integrated module," 2003, pp. 1497-1500 vol. 3.
7. G. W. Dahlmann, E. M. Yeatman, P. R. Young, I. D. Robertson, and S. Lucyszyn, "MEMS high Q microwave inductors using solder surface tension self-assembly," 2001, pp. 329-332 vol. 1.
8. Y. C. Huang, B. H. Jang, and W. Fang, "Implementation and characterization of a quality-factor-controllable micromachined inductor," 2011, pp. 1168-1171.
9. S. Aliouane, A. Kouki, and R. Aigner, "RF-MEMS switchable inductors for tunable bandwidth BAW filters," 2010, pp. 1-6.
10. C. L. Dai, J. Y. Hong, and M. C. Liu, "High Q-factor CMOS-MEMS inductor," 2008, pp. 138-141.

11. X. N. Wang, X. L. Zhao, Y. Zhou, X. H. Dai, and B. C. Cai, "Fabrication and performance of a novel suspended RF spiral inductor," *Electron Devices, IEEE Transactions on,* vol. 51, pp. 814-816, 2004.
12. G. W. Dahlmann, E. M. Yeatman, P. R. Young, I. D. Robertson, and S. Lucyszyn, "MEMS high Q microwave inductors using solder surface tension self-assembly," in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, 2001, pp. 329-332 vol.1.
13. J. Chen, J. Zou, C. Liu, J. E. Schutt-Ainé, and S. M. K. Kang, "Design and modeling of a micromachined high-Q tunable capacitor with large tuning range and a vertical planar spiral inductor," *Electron Devices, IEEE Transactions on,* vol. 50, pp. 730-739, 2003.
14. W. Dae-Hee, J. Jong-Hyeok, K. Jeong-Il, S. Mohammadi, and L. P. B. Katehi, "High-Q integrated 3-D inductors and transformers for high frequency applications," in *Microwave Symposium Digest, 2004 IEEE MTT-S International*, 2004, pp. 877-880 Vol.2.
15. C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *Solid-State Circuits, IEEE Journal of,* vol. 33, pp. 743-752, 1998.
16. D. H. Weon, J. I. Kim, and S. Mohammadi, "Design of high-Q 3-D integrated inductors for high frequency applications," *Analog Integrated Circuits and Signal Processing,* vol. 50, pp. 89-93, 2007.
17. C. Leroy, M. B. Pisani, C. Hibert, D. Bouvet, M. Puech, and A. M. Ionescu, "High quality factor copper inductors integrated in deep dry-etched quartz substrates," *Microsystem technologies,* vol. 13, pp. 1483-1487, 2007.
18. P. J. Chen, W. C. Kuo, W. Li, Y. J. Yang, and Y. C. Tai, "Q-enhanced fold-and-bond MEMS inductors," 2008, pp. 869-872.
19. D. H. Weon, J. I. Kim, J. H. Jeon, S. Mohammadi, and L. P. B. Katehi, "High performance micro-machined inductors on CMOS substrate," 2005, p. 4 pp.
20. I. Gmati, H. Boussetta, M. A. Kallala, and K. Besbes, "Wide-range RF MEMS variable inductor using micro pump actuator," 2008, pp. 1-4.
21. S. Chang and S. Sivoththaman, "A tunable RF MEMS inductor on silicon incorporating an amorphous silicon bimorph in a low-temperature process," *Electron Device Letters, IEEE,* vol. 27, pp. 905-907, 2006.
22. I. El Gmati, P. F. Calmon, A. Boukabache, P. Pons, R. Fulcrand, S. Pinon, H. Boussetta, M. A. Kallala, and K. Besbes, "Fabrication and evaluation of an on-chip liquid micro-variable inductor," *Journal of micromechanics and microengineering,* vol. 21, p. 025018, 2011.
23. I. El Gmati, P. Calmon, A. Boukabache, P. Pons, H. Boussetta, M. Kallala, and K. Besbes, "Liquid RF MEMS variable inductor," *Procedia Engineering,* vol. 5, pp. 1380-1383, 2010.
24. V. M. Lubecke, B. Barber, E. Chan, D. Lopez, M. E. Gross, and P. Gammel, "Self-assembling MEMS variable and fixed RF inductors," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 49, pp. 2093-2098, 2001.
25. S. Zhou, X. Q. Sun, and W. N. Carr, "A monolithic variable inductor network using microrelays with combined thermal and electrostatic actuation," *Journal of micromechanics and microengineering,* vol. 9, p. 45, 1999.
26. I. Zine-El-Abidine, M. Okoniewski, and J. McRory, "A MEMS tunable inductor," pp. 340-2.
27. J. I. Kim and D. Peroulis, "Tunable MEMS spiral inductors with optimized RF performance and integrated large-displacement electrothermal actuators," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 57, pp. 2276-2283, 2009.
28. B. Assadsangabi, M. S. M. Ali, and K. Takahata, "Ferrofluid-based variable inductor," in *Micro Electro Mechanical Systems (MEMS), 2012 IEEE 25th International Conference on*, 2012, pp. 1121-1124.
29. O. Casha, I. Grech, J. Micallef, E. Gatt, D. Morche, B. Viala, J. P. Michel, P. Vincent, and E. de Foucauld, "Utilization of MEMS tunable inductors in the design of RF voltage-controlled oscillators," 2008, pp. 718-721.
30. M. El Bakkali, F. Chan Wai Po, E. De Foucauld, B. Viala, and J. P. Michel, "Design of a RF matching network based on a new tunable inductor concept," *Microelectronics journal,* vol. 42, pp. 233-238, 2011.
31. M. Vroubel, Y. Zhuang, B. Rejaei, and J. N. Burghartz, "Integrated tunable magnetic RF inductor," *Electron Device Letters, IEEE,* vol. 25, pp. 787-789, 2004.
32. K. Okada, H. Sugawara, H. Ito, K. Itoi, M. Sato, H. Abe, T. Ito, and K. Masu, "On-Chip High-$ Q $ Variable Inductor Using Wafer-Level Chip-Scale Package Technology," *Electron Devices, IEEE Transactions on,* vol. 53, pp. 2401-2406, 2006.
33. H. Sugawara, Y. Yoshihara, K. Okada, and K. Masu, "Reconfigurable CMOS LNA for software defined radio using variable inductor," in *Wireless Technology, 2005. The European Conference on*, 2005, pp. 547-550.
34. S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *Solid-State Circuits, IEEE Journal of,* vol. 34, pp. 1419-1424, 1999.
35. S. Lucyszyn, *Advanced RF Mems*: Cambridge Univ Pr, 2010.

36. M. Gabriel and R. Rebeiz, "RF MEMS Theory, design and technology," *Hoboken: John Wiely and Sons,* 2003.
37. J. Zhao, "A new calculation for designing multilayer planar spiral inductors," *EDN (Electrical Design News),* vol. 55, p. 37, 2010.
38. J. Lee, S. Park, H. C. Kim, and K. Chun, "Substrates and dimension dependence of MEMS inductors," *Journal of micromechanics and microengineering,* vol. 19, p. 085014, 2009.
39. J. J. Liou, "On-chip spiral inductors for RF applications: an overview," *JOUNAL OF SEMICONDUCTOR THCHNOLOGY AND SCIENCE,* vol. 4, pp. 149-167, 2004.
40. W. B. Kuhn and N. M. Ibrahim, "Analysis of current crowding effects in multiturn spiral inductors," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 49, pp. 31-38, 2001.
41. O. Ban-Leong, X. Dao-Xian, K. Pang-Shyan, and L. Fu-jiang, "An improved prediction of series resistance in spiral inductor modeling with eddy-current effect," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 50, pp. 2202-2206, 2002.
42. C. Jinghong, Z. Jun, L. Chang, J. E. Schutt-Aine, and S. M. K. Kang, "Design and modeling of a micromachined high-Q tunable capacitor with large tuning range and a vertical planar spiral inductor," *Electron Devices, IEEE Transactions on,* vol. 50, pp. 730-739, 2003.
43. X. N. Wang, X. L. Zhao, Y. Zhou, X. H. Dai, and B. C. Cai, "Fabrication and performance of novel RF spiral inductors on silicon," *Microelectronics journal,* vol. 36, pp. 737-740, 2005.
44. C. M. Nam and Y. S. Kwon, "High-performance planar inductor on thick oxidized porous silicon (OPS) substrate," *Microwave and Guided Wave Letters, IEEE,* vol. 7, pp. 236-238, 1997.
45. W. B. Kuhn, X. He, and M. Mojarradi, "Modeling spiral inductors in SOS processes," *Electron Devices, IEEE Transactions on,* vol. 51, pp. 677-683, 2004.
46. S. H. Tseng, Y. J. Hung, Y. Z. Juang, and M. S. C. Lu, "A 5.8-GHz VCO with CMOS-compatible MEMS inductors," *Sensors and Actuators A: Physical,* vol. 139, pp. 187-193, 2007.
47. H. Lakdawala, X. Zhu, H. Luo, S. Santhanam, L. R. Carley, and G. K. Fedder, "Micromachined high-Q inductors in a 0.18-μm copper interconnect low-k dielectric CMOS process," *Solid-State Circuits, IEEE Journal of,* vol. 37, pp. 394-403, 2002.
48. H. Lakdawala, X. Zhu, H. Luo, S. Santhanam, L. Carley, and G. Fedder, "Micromachined high-Q inductors in 0.18 μm Cu interconnect low-K CMOS," in *Custom Integrated Circuits, 2001, IEEE Conference on.*, 2001, pp. 579-582.
49. D. Athreya, V. Sundaram, M. Iyer, and R. Tummala, "Ultra high Q embedded inductors in highly miniaturized family of low loss organic substrates," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, 2008, pp. 2073-2080.
50. S. A. Elshatshat, "Effects of inorganic salts on water permeability of isolated cuticular membranes," PhD Thesis, University of Bonn, 2004.
51. C. M. Tassetti, G. Lissorgues, and J. P. Gilles, "New tunable RF MEMS microinductors design," *Journal of micromechanics and microengineering,* vol. 14, p. S17, 2004.
52. C. Tassetti, G. Lissorgues, and J. Gilles, "Tunable RF MEMS microinductors for future communication systems," 2003, pp. 541-545 vol. 1.
53. I. Zine-El-Abidine, M. Okoniewski, and J. G. McRory, "RF MEMS tunable inductor," 2004, pp. 817-819 Vol. 3.
54. I. Zine-El-Abidine, M. Okoniewski, and J. McRory, "A Tunable RF MEMS Inductor," 2004, pp. 636-638.
55. I. Zine-El-Abidine, M. Okoniewski, and J. G. McRory, "Tunable radio frequency MEMS inductors with thermal bimorph actuators," *Journal of micromechanics and microengineering,* vol. 15, p. 2063, 2005.

Arrived: 03. 10. 2013
Accepted: 27. 01. 2014

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 44, No. 2 (2014), 104 – 108

Fast One-Time Programming (OTP) and a Programming Verification Solution using Zener Diodes in a Standard CMOS Process

Janez Trontelj

Faculty of Electrical Engineering, Ljubljana, Slovenia

Abstract: This article describes an effective, low-cost solution for sequential, one-time programming (OTP) and verification of zener diodes in an electronic micro-system. Using the proper structures of zener diodes (also known as 'zener zap') in a standard CMOS process, it is possible to achieve better accuracy in high-precision integrated circuits. For this purpose a solution has been developed for fast programming and programming verification of several zener zap structures on the ASIC (Application Specific Integrated Circuit). The entire zapping process for 250 zener zap structures is completed in the range of a few tens of milliseconds. This solution has been implemented for wafer sorting, and as well for packaged integrated circuits. It was successfully verified in the industrial production of more than ten million- high precision, electronic micro-systems with a remarkable overall yield of 97%.

Keywords: OTP, Zener zap, ASIC, DAQ, burn pulse, antifuse

Hitra metoda za enkratno programiranje in preverjanje pravilnosti programiranja s pomočjo zener diod v standardnem CMOS procesu

Izvleček: Članek opisuje učinkovit, nizko cenovni pristop za zaporedno, enkratno programiranje kakor tudi preverjanje pravilnega programiranja zener diod v elektronskem mikrosistemu. Z uporabo posebnih struktur integriranih zener diod (zener zap – zener antivarovalke) je v standardnem CMOS procesu mogoče doseči večjo natančnost integriranih vezij. V ta namen je bila razvita metoda za hitro, zaporedno programiranje več zener antivarovalk. Celoten postopek programiranja in verifikacije za 250 zener struktur je končan v času nekaj deset milisekund. Rešitev je bila uporabljena za meritve elektronskih mikrosistemov na silicijevih rezinah in tudi na posameznih čipih v ohišjih. Uspešno smo jo preverili v industrijski proizvodnji več kot deset milijonov visoko občutljivih integriranih vezij s celokupnim izplenom 97%.

Ključne besede: Enkratno programiranje, Zener varovalka, Vezja po naročilu, Zajem podatkov, pulz za prežig, antivarovalka

* *Corresponding Author's e-mail: janez.trontelj-jr@fe.uni-lj.si*

1 Introduction

In modern industry there is a huge demand for high-precision, low-cost, fully integrated analog sensors. Over the years, several methods have been implemented to overcome the tolerances of the integrated circuit fabrication process. Although ratiometric design principles may be successfully adopted, there is still a need for finer methods to adjust critical parameters of the integrated sensors. Here various, one-time programming methods (OTP) take place - such as laser trimming, poly fuse burning and zener-zapping. By using these methods, we can significantly improve the production yield and fulfill the requirements for accuracy of high-precision integrated circuits. This is usually done on the wafer level at wafer sort, but sometimes it must be also implemented for packaged parts - to eliminate the so-called 'package effect'. It is evident that during dicing and packaging there may be a certain amount of stress applied to the sensitive sensor structures. So the overall accuracy of the sensor can be easily affected. This problem can be resolved even after packaging - by using automated measurements, handling, and fine-trimming of the packaged microelectronics systems.

This article describes a one-time programming technique that uses zener-zapping. This well- established method creates antifuse devices. The term 'antifuse' describes an element which initially represents an open circuit, but can be later irreversibly changed to approach a short circuit. Such an element can be implemented with a reverse biased zener diode. This is a small, subsurface lateral N+, P+ structure. When the zener diode programming current is increased, a temporary avalanche breakdown in a P-N junction is forced. This causes localized heating and subsequent migration of metallization across the junction (spiking). In other words, zener zapping is a short current pulse to the reverse biased zener diode. The resistance of the zapped diode is drastically changed after the OTP. This very interesting process is described in more detail in [1] and [2].

This article is not intended to describe zener zapping structures in detail. Such cells are now available as standard parts in design libraries for several technologies. Additional improvements of various OTP methods are constantly evolving. Examples for this are described in [3], [4] and [5]. The trend is in further increasing the reliability, while reducing the zapping current.

Unfortunately, very little information is available on implementing the zapping procedure. When we began to deal with this topic, we experienced quite a few difficulties in achieving a fast and consistent zener zapping. We noticed that other teams also had a lot of trouble with this, and that our assistance was welcome. So, the main focus of this article is to describe how to create low-cost, fast as possible and reliable communication hardware to implement a test, a statistical analysis, and an OTP solution. Moreover, all this was developed to test our, in the LMFE (Laboratory for Microelectronics from Faculty of Electrical Engineering) designed ASIC with a high-precision magnetic sensor. In this case, a widely available and proven OTP zener zap cells from the silicon foundry technology library were used.

Figure 1 presents an actual photograph of a small part of the zener zap array on our ASIC. A photograph of four zener zap structures was taken at 3000x magnification. To take this photo, some layers above the zener zap structures had to be removed. Unfortunately, the entire zener zap structure is not at the same level, so some parts of the photograph are a little bit out of focus.

The zener zapping method has numerous benefits. A zener diode is commonly available in all standard CMOS processes, and therefore represents no significant extra cost in fabrication. Each diode can be controlled by a single selection transistor. So, it is relatively easy to implement a mixed mode sequential system for selecting and programming each zener diode separately. This approach usually requires one additional pin on the circuit. Also quite important is the fact that no life-time reliability problems of properly trimmed zener zaps are expected. The reason for this is that during OTP, no damage is caused to the other layers or the passivation on the silicon wafer surface. So, all affected structures remain safely isolated from the harsh environmental influences, before device packaging takes place.

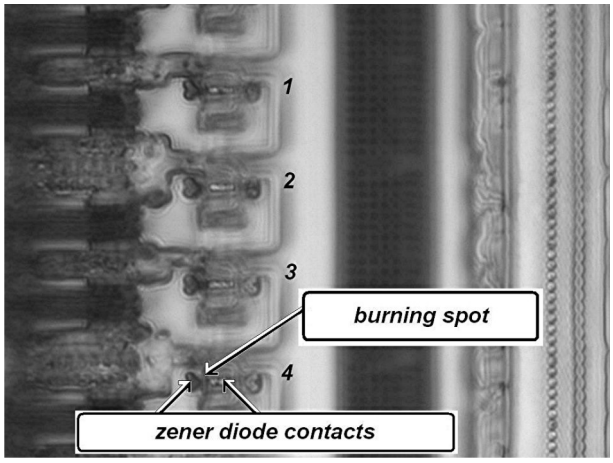


Figure 1: Zener zap structure photograph taken at 3000x magnification.

However, besides occupying some extra silicon, there are two major problem areas identified. One is in supplying the correct amount of current for effective burning, and the second one is about defining the optimal burn pulse duration and shape. The final resistance of the zapped diode is additionally depending on the amount of the supplied current after the initial modification of the P-N junction is done [2]. Last but not at least, for industrial production it is also quite essential to obtain as brief as possible programming and programming verification time.

In our case only one pin of the ASIC is reserved for OTP communication implementation. As the basis for the project, we decided to use a low-cost USB (or alternatively 'PC Card') data acquisition card (DAQ) [6] and some extra, in-house designed hardware. For improved reliability, a sort of adaptive OTP pulse was developed. It can be automatically readjusted for each wafer lot, or even during testing each wafer separately. The described solution was practically verified in burning several millions of zener zap devices. It is capable to do the OTP of 250 zener zaps on one ASIC in approximately a 4 millisecond time frame. Besides for communication purposes, the DAQ card may also be used for taking various measurements, and according to measurement results, actual trimming of the measured sensor on the ASIC can be performed.

2 OTP procedure description

In this section the OTP method is described that was proposed for our high-precision magnetic sensor ASIC. In this case, besides the required selective trimming of critical parameters, unique identification of each microelectronic system was also required. So each micro system is given a unique serial number. This enables us to easily compare the measured parameters on wafer sort with later measured parameters on packaged parts. In our particular example, 250 zener zap structures for various OTP features are necessary.
As we determined before, one pin of the ASIC is enough to implement the suggested OTP procedure. Basically, what we need is some sort of a pulse train, to access each zener element in a zener zap array. The train of pulses contains by default the information about the communication clock. When adopting different pulse levels, it can carry additional information. Figure 2 presents the proposed pulse train with different levels and their meaning.

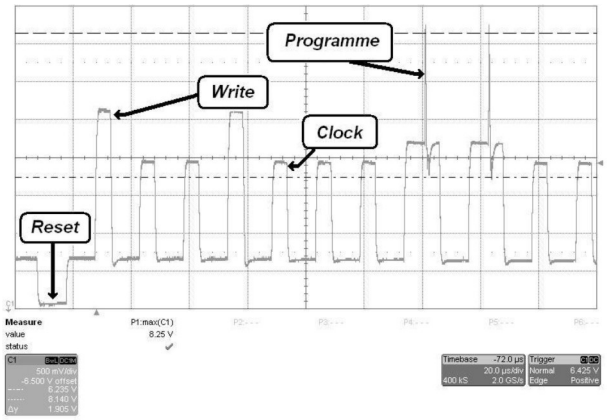


Figure 2: Pulse train with described meaning of different levels.

To prevent undesired false zapping during electrostatic discharge on the programming pin, there is a unique sequence of pulses in the beginning of the pulse train. This unlocks further recognition of the pulse train and enables eventual zener zapping. Figure 2 shows four different levels of pulses. The lowest level is the micro system reset. A normal level represents a clock with no programming action. This level only addresses the next zener diode. A higher level represents temporarily programming in shadow RAM (for a preview of the eventual OTP) on the currently selected zener zap. This state is active, until reset or the micro system power down takes place. This enables us to do evaluation and verification of the ASIC behavior before the final OTP is done. Furthermore, the highest level of the pulse represents an action of irreversible OTP, or with other words – zener zapping.

After the zener zapping is completed, it is possible to send another pulse train to the programming pin, now without using the zener zapping highest pulse level. By temporarily setting up and using one, additional output pin on the ASIC, resistance of each zapped and un-zapped antifuse can be measured and verified. This further enhances the reliability and control of the zener zapping process.

3 Implemented methodology

The standard method for zener zapping is to discharge a small capacitor over a reverse biased zener diode. This forces a quite well-defined and repeatable avalanche breakdown in a P-N junction. When properly selected, the desired pulse width from 1 µs to 3 µs [2] can be easily achieved. The problem is that this method needs additional time to sufficiently recharge the capacitor. A drawback is also evident, that during programming the charging current must be disconnected from the capacitor. This additionally slows down the effectiveness of this method.

Another approach is to use expensive dedicated equipment that is capable to drive and precisely control the current and shape for a relatively short burn pulse. We had a chance to compare the results from our low-cost solution with a similar solution on such relatively expensive equipment (approx. cost ratio 1:50), and our solution was superior.

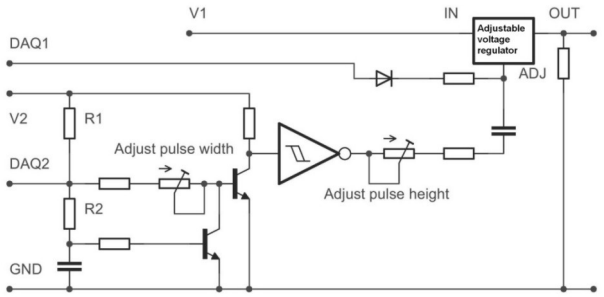


Figure 3: Simplified schematic for generation of variable OTP pulse.

Figure 3 describes the method proposed in this article. An adjustable voltage regulator is controlled by the analog output DAQ1 pin of the DAQ card to achieve different levels of the pulse train. The burn pulse is triggered by the DAQ2 digital signal and a simple delay circuit with a Schmitt trigger, and then added to the pulse train via small capacitor. Trimmers are used for fine adjusting the amplitude and pulse width. To achieve approx. 1 µs switch delay, a resistor R2 must be significantly larger than resistor R1. Voltage V1 must be a little bit higher than the maximum allowed program-

ming voltage. Voltage V2 should be set to 5 volts for proper Schmitt trigger operation.

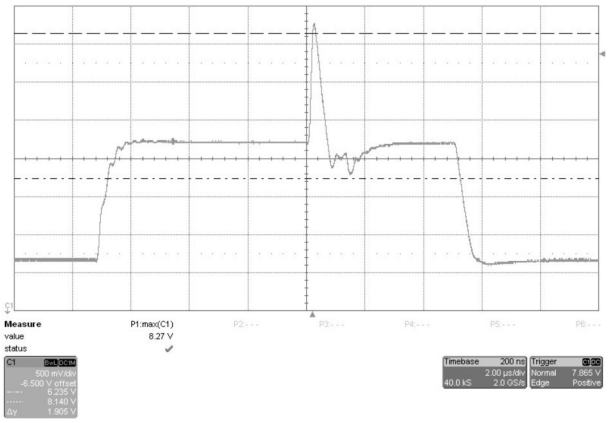


Figure 4: Detailed burn pulse with time base 2 µs/division.

A detailed example of such a pulse is represented in Figure 4. As we can see, the desired positive part of the triggered glitch is preserved, and undesired negative part is almost eliminated. This is a very important feature for stable communication. The best results were usually achieved at a pulse time a little bit below 1 µs, with a pulse peak level of 8.25 V, and at 6.75 V remaining after the glitch. The criterion for these three parameters is the statistical analysis of zapped fuse resistance uniformity. When the uniformity is high, we are close to the ideal zapping parameters.

An example for the entire pulse train to access all 250 zener zap elements is presented in Figure 5. This pulse train will zap at indexes 12, 15, 55, 100, 150, 200, 201, 202, 203, 204, and 205.

This method successfully eliminates the drawback of slow capacitor recharging, and burning can be repeated in the range of micro seconds. Another benefit is that the entire pulse train shape can be easily readjusted and adapted to a specific wafer or wafer lot automatically by the software itself.

Another problem to be solved here was the principle of controlling the pulse train with USB port. Sending each pulse separately through USB communication protocol would be to slow. Fortunately, there is quite a large selection of low-cost DAQ cards that have some storage capability. So it is possible to use only one USB write cycle to store an entire pulse train pattern in the DAQ card memory. Afterwards, a trigger must be generated to execute the stored pulse train sequence. This pulse train is then executed promptly, without any interrupts.

After all the selected zener zaps are burned, zener zap verification takes place. For this purpose, another pulse train with an added measuring sequence is stored into the DAQ card memory. In this case (besides a pulse train), a synchronous measurement procedure will also be triggered. This will store the measured voltages for each zener zap in-to the DAQ card's memory. When the measuring task is finished, one USB read cycle takes the measured data from the DAQ card into the computer memory, where data evaluation takes place. If any anomaly, such as too high antifuse resistance or an incorrect burned zener zap index is detected, the tested device is discarded and marked as a bad part on the wafer map.

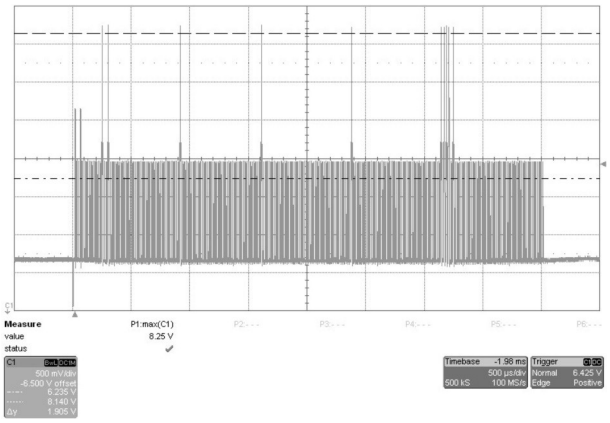


Figure 5: Complete pulse train for programming 250 zener zaps. Time base is 500 µs/div.

Similar functionality can also be achieved by using a suitable PC Card or ISA slot type DAQ card in a real-time operating system environment. This solution can be even faster, because it eliminates delay in USB communication. Such a system usually requires a little bit more time to implement, but for mass production, this extra time can be easily justified.

In this particular case, besides the basic functionality of the tested devices, the temperature coefficient also needs to be trimmed during the wafer sort. Therefore, all devices must be measured and evaluated at two different temperatures. First, we measure all the parameters for each sensor on the wafer at room temperature. This measurement data is stored and later compared to the measured parameters at high temperature. Besides determining the physical position of each part on the wafer, it is also quite essential, to identify each part correctly with a unique serial number. This additionally ensures error-free correlation between high and low temperature data and correct trimming of each sensor at high temperature.

For fast testing and temperature trimming of packaged sensors, we successfully developed and patented some special temperature coefficient measurement procedures that are described in detail in [7]. This was,

however, mainly used for the wafer sort procedure verification and some small experimental series.

4 Conclusion

Most mixed-mode integrated circuits are dominated by a digital part area. Failure of a small analog section to meet strict, predefined accuracy requirements can have poor yield economics issues. Efficient trimming of critical parameters is more than welcome - especially, when relatively large quantities of silicon are in question.

Next to yield, test time optimization is also very essential. With the described method, the trimming time of 250 zener zaps (without considering hardware dependent time for communication between DAQ and computer via USB port) takes app. 4 milliseconds. This time is actually determined by the reliability of the 'on chip' integrated communication protocol. The test system itself would be capable to accomplish the zapping task even faster.

Slightly more time is needed while doing the zener zapping verification. The reason for this is the required settling time for better zap resistance measuring accuracy. If we use 50 µs of time to settle the measurement for each zener zap, it takes app. 18 milliseconds to measure and verify the resistance of all 250 antifuses. Further test time optimization can be done by improving the speed of the utilized communication protocol on the integrated circuit.

Besides an as short as possible test time, it is also very important feature to provide a low-cost multiplication of the test system. Several test sites usually drastically reduce the turn out time. For this particular project, six functional test sites were configured. To maintain the equivalence between the test sites, automatic test parameter calibration procedures were implemented. They also comply with strict automotive VDA 6.3 standards. The entire wafer sort and the OTP process was actually checked by external process audit, according to automotive VDA 6.3 (chapters 3-7) with a 92% overall degree of conformity.

At the time, when this article was written, approximately ten million high sensitive integrated sensor circuits were trimmed and tested in our facilities. The test yield was more than 97%, while the yield difference between different test sites was negligible. The average number of OTP zener zaps per ASIC was approximately 36. This means that over the past few years (from 2009 to 2013) we have successfully burned and verified more than 360 million zener antifuses. Also, production was ongoing when this article was written.

To briefly summarize, the most important contribution described in this article is a unique method for variable burn pulse generation that enables a very fast, reliable, and highly adaptive zener zap burning and burn verification procedure for industrial application. This variability was also a key feature to do a rapid statistical analysis for fine tuning zener zapping parameters.

5 Acknowledgments

The author wishes to thank the staff of the Laboratory for Microelectronics at the University of Ljubljana for their help and support in this interesting project, which inspired him to write this article.

6 References

1. D. T. Comer, "Zener Zap Anti-Fuse Trim in VLSI Circuits," VLSI Design, Vol. 5, No. 1, pp. 89-100, 1996.
2. J. Teichmann, K. Burger, W. Hasche, J. Herrfurth, G. Täschner, "One-Time Programming (OTP) with Zener Diodes in CMOS Processes," 33rd European Solid-State Device Research Conference – ESSDERC 2003, IEEE Catalog Number: 03EX704C, ISBN:0-7803-8100-0, pp. 433-435, 2003.
3. M. Chen, C. E. Huang, Y. H. Tseng, Y. C. King, C. J. Lin, "A New Antifuse Cell With Programmable Contact for Advance CMOS Logic Circuits," Electron Device Letters, IEEE, Vol. 29, No. 5, pp. 522-524, 2008.
4. R. Barsatan, T. Y. Man, M. Chan, "A zero-mask one-time programmable memory array for RFID applications," 2006 IEEE International Symposium on Circuits and Systems, ISCAS 2006, pp. 975-978, 2006.
5. J. Roig, J. Lebon, S. Vandeweghe, S. Mouhoubi, F. Bauwens, "Improved Current Filament Control during Zener Diode Zapping," Special Issue 23rd European Symposium on the Reliability of Electron Devices, Failure Physics and Analysis, Cagliary, Italy, pp. 2368-2373, 2012.
6. National Instruments, "DAQ M series User Manual," 2008.
7. J. Trontelj Jr., J. Trontelj, B. Šmid, "Postopek in naprava za testiranje in uravnavanje temperaturnega koeficienta integriranih vezij," patent št. 24004, Urad Republike Slovenije za intelektualno lastnino, 2013.

Arrived: 20. 01. 2014
Accepted: 18. 03. 2014

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 44, No. 2 (2014), 109 – 118

Performance Analysis of a Memristor - Based Biquad Filter Using a Dynamic Model

Şuayb Çağrı Yener[1], Reşat Mutlu[2], H. Hakan Kuntman[3]

[1]Sakarya University, Engineering Faculty, Electrical and Electronics Engineering Department, Sakarya, Turkey
[2]Namık Kemal University, Çorlu Engineering Faculty, Electronics and Communication Engineering Department, Çorlu, Tekirdağ, Turkey
[3]Istanbul Technical University, Electrical – Electronics Faculty, Electronics and Communication Engineering Department, Maslak, Istanbul, Turkey

Abstract: New kinds of programmable amplifiers, adaptive filters, and programmable oscillators can be designed using a new fundamental circuit element memristor. Application of the memristor to analog filters can result in many new properties especially thanks to its variable memristance. In this paper, by using linear drift memristance model, a memristor-based biquad analog filter is examined. The filter is simulated using its dynamic model. The linear dopant drift model of TiO2 memristor is used in the simulations. Simulations have shown that the filter components such as gain and quality factor can be adjusted using the memristor in biquad filter. It has also been observed that memristor may go into saturation at very low frequencies and very low charge values. Considering the results of this study, the tunable memristance gives filters an adjustable characteristic which cannot be obtained by traditional resistors. Results presented in this study can also be considered when designing biquad filters with memristors to ensure their stability and high performance.

Keywords: Memristor, analog filters, memristor-based filter design, biquad filters

Analiza učinkovitosti bikvadrantnega filtra na osnovi memristorja z uporabo dinamičnega modela

Izvleček: Novi programabilni ojačevalniki, adaptivni filtri in programabilni oscilatorji so lahko načrtovani z uporabo novega elementa memristorja. Uporaba memristorja v analognih filtrih lahko vodi v nove lastnosti filtra predvsem zaradi spominske upornosti elementa. V članku je predstavljen bikvadrantni analogni filter na osnovi memristorja z uporabo linearnega modela spominske upornosti. Filter je simuliran z dinamičnim modelom. Simulacije so pokazale, da uporaba memristorja v bikvadrantnem filtru omogoča spreminjanje ojačenja in faktorja kvalitete. Opaženo je bilo tudi, da lahko memristor pride v stanje nasičenosti pri zelo nizkih frekvencah in vrednosti naboja. Na osnovi te rezultatov te raziskave je bilo ugotovljeno, da spremenljiva spominska upornost zagotavlja karakteristike filtra, ki jih s klasičnimi upori ni bilo mogoče doseči. Rezultati raziskave so uporabni tudi pri načrtovanju bikvadrantnih filtrov z visoko stabilnostjo in učinkovitostjo.

Ključne besede: Memristor, analogni filtri, memristor filtri, bikvadrantni filter

** Corresponding Author's e-mail: syener@sakarya.edu.tr*

1 Introduction

Memristor was declared as the missing circuit element in 1971 [1]. It can be thought as a nonlinear resistor whose resistance or memristance depends on electrical charge which have passed through it. Almost 40 years later than its prediction, a memristive system which behaves as a memristor has been announced as fabricated [2]. This solid state realization has resulted in a large-scale interest in memristor. However, no commercially and practically available memristor exists yet. Memristors can be used in analog circuits and may provide many new additional features. Various

SPICE macro-models, memristor emulators exhibiting memristor-like behavior and some analog and chaotic applications have already been presented in literature [3-10].

It is thought that application of the memristor to analog filters can result in many new properties especially because of its variable memristance. Some studies are already presented in the literature related to application of the memristor to analog filters such as band-pass adaptive filter based on vanadium dioxide (VO_2) memristor [11], a first-order filter for sensing resistive memory based on a memristor and a capacitor [12], low-pass and high-pass filter design using TaO_x based memristor [13], first-order and a second-order low-pass filters employing Cu/ZnO/Cu based memristive structures [14], analyzes of first-order low-pass and second-order band-pass memristor-based filters using PSpice based Boundary Condition Model (BCM) [15], a first-order memristor based low-pass filter using its dependent voltage source based PSPICE model [16].

Tow-Thomas biquad filter [17-19] is used in many analog signal processing applications. Current or voltage mode Tow-Thomas filters have been introduced and their quality factor and cut-off frequency are electronically tunable by adjusting some circuit components or the biasing current of CMOS active blocks etc [20-24]. In this study, a memristor-based Tow-Thomas Biquad filter is designed, it uses a resistance tuning circuit and does not need any active blocks to adjust the filter parameters. It has also an advantage: the memristor is a nonvolatile memory and, if the power source is turned off and back again, the memristor remembers the charge which passed through it and the filter starts operating with the last operating points set.

In this study, the feedback resistor of the first stage in the Tow-Thomas filter is replaced with a memristor and the memristor-based filter properties are inspected using simulations. Linear dopant drift model of TiO_2 (titanium-dioxide) memristor model is commonly used in literature [2,3] and it is also used in the simulations performed. For the first time in the literature to the best of our knowledge, we will demonstrate the effect of polarity of memristor on waveforms of memristor-based filters. Results of this study can be used for designing memristor-based filters when a memristor as a separate or integrated circuit component element becomes commercially available in the market.

Structure of the paper is as follows. The second section, which follows this introduction, summarizes linear drift modeling of a memristor. In the third section, the memristor based Tow-Thomas biquad filter is introduced. In the fourth section, dynamic model of the memristor-based biquad filter is given. In the fifth section, simulation results performed on Simulink™ toolbox of MATLAB™ are provided. Time domain waveforms of current, voltage, charge and memristance are analyzed. The effect of polarity is analyzed. Gain responses of the band-pass (BP) and low-pass (LP) biquad filters with respect to frequency and as a function of variable memristance are also inspected. Finally, in the last chapter, the performance and constraints of memristor based filters and also its new possibilities on analog filter design are discussed.

2 Linear drift TIO2 memristor model

A memristor is a nonlinear circuit element whose voltage to current ratio or its instantaneous resistance depends on electrical charge which have passed through it [1]. A memristor can also be modeled as flux dependent [1]. In this study, charge-controlled memristor model is used. The instantaneous resistance of a memristor is called memristance and memristance function of a charge-controlled memristor is given as

$$M(q) = \frac{d\varphi(q)}{dq} \tag{1}$$

where q is the memristor charge and φ is the memristor flux, which are equal to integration of current with respect to time and integration of voltage with respect to time, respectively. They are calculated as

$$q(t) = \int_{-\infty}^{t} i(\tau)\, d\tau \tag{2}$$

$$\varphi(t) = \int_{-\infty}^{t} v(\tau)\, d\tau \tag{3}$$

In this work, the charge dependent model of TiO2 memristor with linear dopant drift speed as given in [2] is used. Memristance function of TiO_2 memristor with linear dopant drift system is given as

$$M(q) = \frac{d\varphi}{dq} = R_{OFF}\left(1 - \frac{\mu_V R_{ON}}{D^2} q(t)\right) \tag{4}$$

Memristance function can also be simplified as

$$M(q) = M_0 - K_q q(t) \tag{5}$$

where M_0 is the maximum memristance of the memristor, and $M_0=R_{OFF}$. K_q is the charge coefficient of the memristor and q(t) is the instantaneous memristor charge.

The minimum memristor memristance is given as

$$M_{SAT} = M_0 - K_q q_{SAT} \tag{6}$$

where q_{SAT} is the maximum memristor charge. The terminal equation of a charge-controlled memristor is expressed as

$$v = M(q)\,i \tag{7}$$

3 Biquad filter

In this section, a Tow-Thomas biquad filter is first briefly explained and then the memristor-based biquad filter is introduced.

3.1 Tow-thomas biquad filter

A two-integrator loop biquad filter topology where all three op-amps are used in a single-ended configuration is shown in Figure 1 [17-19]. It is called as a Tow-Thomas biquad after its inventors. It has two integrator circuits and an inverting amplifier at the last stage. This configuration has a BP output, a LP output and one more LP output in reversed phase which are taken from nodes V_{BP}, V_{LP} and V_{LPI}, respectively. In this topology high-pass output is no longer available as it is the result of all op-amps being in the single-ended mode. [20,21].

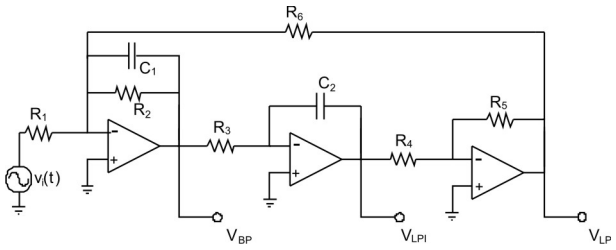


Figure 1: Traditional Tow-Thomas biquad filter.

Standard output form for a second-order BP filter:

$$H_{BP}(s) = \pm\frac{sH_0\dfrac{\omega_0}{Q}}{s^2 + s\dfrac{\omega_0}{Q} + \omega_0^2} \tag{8}$$

The transfer function for the BP filter given in Figure 1:

$$H_{BP}(s) = \frac{V_{BP}}{V_{IN}} = -\frac{s\dfrac{1}{C_1R_1}}{s^2 + s\dfrac{1}{C_1R_2} + \dfrac{R_5}{C_1C_2R_3R_4R_6}} \tag{9}$$

Therefore, some important parameters of the filter in Figure 1 can be expressed as follows.

The BP gain at the cut-off or resonant frequency:

$$H_{0(BP)} = \frac{R_2}{R_1} \tag{10}$$

The cut-off frequency:

$$\omega_0 = \sqrt{\frac{R_5/R_4}{C_1C_2R_3R_6}} \tag{11}$$

The filter quality factor:

$$Q = \sqrt{\frac{R_5}{R_4}\frac{C_1R_2^2}{C_2R_3R_6}} \tag{12}$$

For the simplicity, by taking R_4=R_5, the filter parameters become

$$H_{BP}(s) = \frac{V_{BP}}{V_{IN}} = -\frac{s\dfrac{1}{C_1R_1}}{s^2 + s\dfrac{1}{C_1R_2} + \dfrac{1}{C_1C_2R_3R_6}} \tag{13}$$

$$\omega_0 = \frac{1}{\sqrt{C_1C_2R_3R_6}} \tag{14}$$

And

$$Q = \sqrt{\frac{C_1R_2^2}{C_2R_3R_6}} \tag{15}$$

General output form for a second-order LP filter:

$$H_{LP}(s) = \pm\frac{H_0\omega_0^2}{s^2 + s\dfrac{\omega_0}{Q} + \omega_0^2} \tag{16}$$

The transfer function for the LP filter given is Figure 1 is:

$$H_{LP}(s) = \frac{V_{LP}}{V_{IN}} = -\frac{\dfrac{R_5}{C_1C_2R_1R_3R_4}}{s^2 + s\dfrac{1}{C_1R_2} + \dfrac{R_5}{C_1C_2R_3R_4R_6}} \tag{17}$$

By taking R_4=R_5:

$$H_{LP}(s) = \frac{V_{LP}}{V_{IN}} = -\frac{\dfrac{1}{C_1C_2R_1R_3}}{s^2 + s\dfrac{1}{C_1R_2} + \dfrac{1}{C_1C_2R_3R_6}} \tag{18}$$

Its gain at LP frequencies is given as

$$H_{0(LP)} = \frac{R_6}{R_1} \tag{19}$$

Both types of filter transfer functions have the same denominator. Thus they have the same cut-off frequencies and quality factors, which are given in and .

3.2 Memristor-based biquad filter

The memristor based Tow-Thomas biquad filter is obtained by replacing resistor R_2 with a memristor designated as M(q). Considering its polarity, a memristor can be placed into the filter in two ways as shown in Figure 2 and Figure 3.

In order to adjust the quality factor of the filters without affecting the cut-off frequency, a memristor will be used instead of resistor R_2. By replacing R_2 with the memristor, M(q), the gain of the band-pass filter at the resonant frequency also becomes adjustable with memristance. For the simplicity, by taking that R_4=R_5 and assuming that the memristor has almost constant memristance, i.e. a small memristance change, the resonant frequency gain of the BP and the quality factor of the both BP and LP memristor-based biquad filters can be expressed as follows:

$$H_{0(BP)} = \frac{M(q)}{R_1} \tag{20}$$

$$Q = \sqrt{\frac{C_1\left(M(q)\right)^2}{C_2 R_3 R_6}} \tag{21}$$

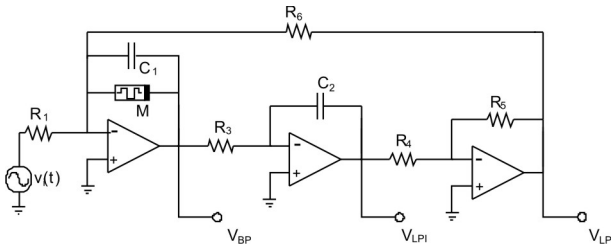


Figure 2: Tow-Thomas biquad filter with positive polarized memristor

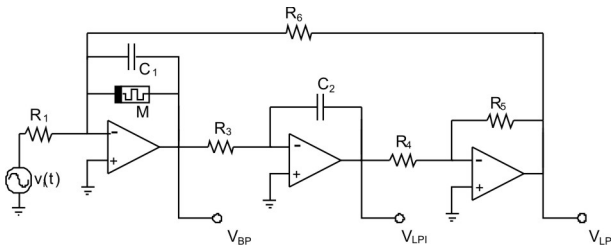
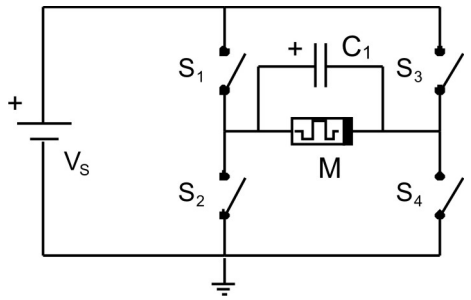
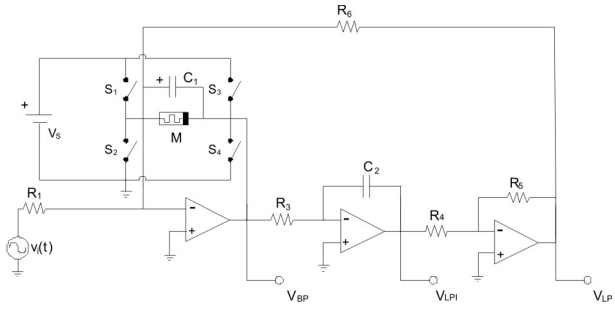


Figure 3: Tow-Thomas biquad filter with negative polarized memristor

Since some of the filter parameters can be adjusted with the memristor memristance, a tuning circuit is needed for this purpose. In Figure 4 (a) memristor value set circuit is shown and its combination with Tow-Thomas biquad filter with positive polarized memristor is given in Figure 4 (b).



(a)



(b)

Figure 4: (a) Memristance value set circuit. (b) Memristor based Tow-Thomas biquad filter with memristor set circuit

S_1 and S_4 are turned on to decrease memristance. S_2 and S_3 are turned on to increase memristance. For a simplified filter operation, it is preferred to make initial capacitor charge equal to zero. S_1 and S_3 can both be turned on to short-circuit the capacitor C_1 for this purpose during memristance tuning.

4 Dynamic system model of memristor based biquad filter

Assuming there is no saturation in the circuit, State-space representation of the memristor based Tow-Thomas biquad filter is given as

$$\frac{dv_{C_1}}{dt} = \frac{1}{C_1}\left(-\frac{v_{C1}}{M(q)} + \frac{R_5}{R_4 R_6} v_{C_2} + \frac{1}{R_1} v_{in}\right) \tag{22}$$

$$\frac{dv_{C_2}}{dt} = -\frac{v_{C1}}{R_3 C_2} \tag{23}$$

$$v_{BP} = -v_{C1} \tag{24}$$

The filter outputs are

$$v_{BP} = -v_{C1} \tag{25}$$

$$v_{LPI} = -v_{C2} \tag{26}$$

$$v_{LP} = \frac{R_5}{R_4} v_{C2} \tag{27}$$

When the memristor is added, due to its memristance, which is a nonlinear function, an analytical solution for the memristor-based biquad filter circuit output voltage in time or frequency domain cannot be obtained. That's why its dynamic model was designed and simulated with Simulink™ toolbox of MATLAB™. Simulink is commonly used to model, analyze and simulate dynamic systems and it has comprehensive block library which can be used to simulate linear, non–linear or discrete systems.

The block diagram of dynamic system and sub-block of linear drift memristor are shown in Figure 5 and Figure 6, respectively. Block diagram of the filter is constructed based on the dynamic model of the filter using a clock signal, a sinusoidal source, a constant, gains, integrators, mathematical operation blocks, and sinks from Simulink library. One of the integrators used is a saturable integrator used in the memristor sub-block diagram to limit memristor memristance between M_{SAT} and M_0.

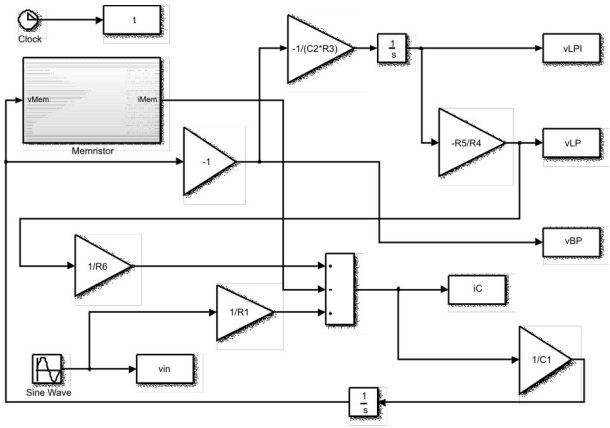


Figure 5: Simulink block diagram of Tow-Thomas biquad filter.

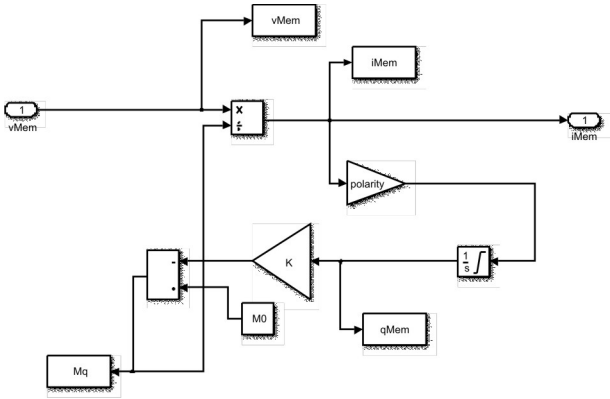


Figure 6: Simulink sub-block diagram of memristor

5 Simulation results

A sinusoidal input voltage of $v_i(t)=V_m \times \sin(\omega t)$ is applied to the input of the memristor-based biquad filter in all cases. Unless otherwise noted, the following circuit parameters are used in simulations: V_m=0.5V, R_1=5kΩ, R_3=5kΩ, R_4=5kΩ, R_5=5kΩ, R_6=5kΩ, C_1=300nF and C_2=300nF. And memristor parameters are taken as M_0=40kΩ, M_{SAT}=100Ω.

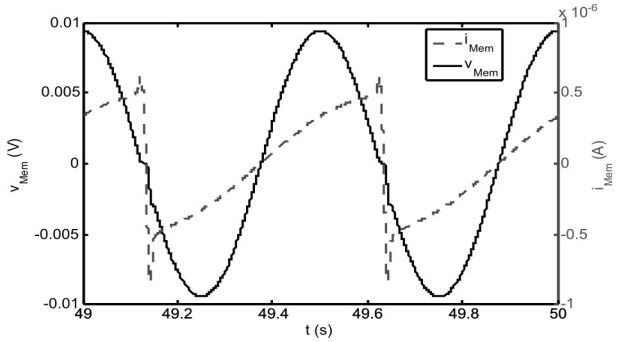
Current-voltage waveforms, memristor hysteresis loop, memristance and memristor charge characteristics are illustrated in time domain. Also the effect of memristor polarity is analyzed. Filter output voltages are simulated in time domain. Filter gain responses are obtained with respect to frequency taking M_{avg} or $M(q_0)$ as parameter where q_0 is the initial or the average charge of the memristor.

5.1 Memristor characteristics and the effect of polarity on filter waveforms

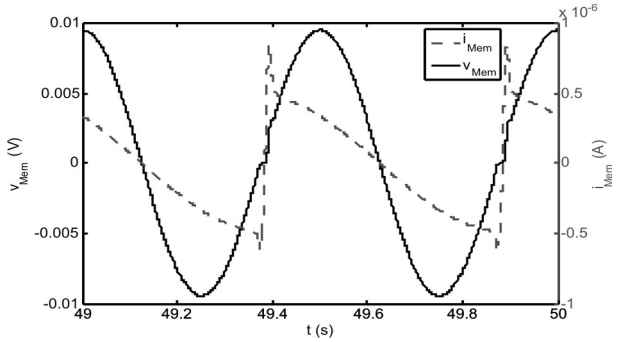
Memristor current-voltage, hysteresis loop, memristance-memristor charge waveforms are presented in Figure 7, Figure 10, Figure 13 for 2 Hz; Figure 8, Figure 11, Figure 14 for 100 Hz and Figure 9, Figure 12, Figure 15 for 1 kHz, respectively.

As it can be seen from Figure 7, Figure 10 and Figure 13 there is distortion in memristor waveforms at very low frequencies and low q_{SAT} values. Saturation of memristor, occurring at very low frequencies, is examined by taking q_{SAT}=0.075 μC. If the frequency is made somewhat higher or a memristor with a sufficiently higher q_{SAT} value is chosen, this distortion either is reduced or disappears.

The saturation occurs at low frequencies since the period is high enough to push current to saturate the memristor i.e. to make its charge equal to q_{SAT} for some interval(s) as seen in Figure 7, Figure 10 and Figure 13. During saturation, all the waveforms, the memristor current, voltage, charge and memristance, become distorted as seen in Figure 7, Figure 10 and Figure 13. The saturation disappears since at high frequencies a memristor behaves as a resistor or the period is not high enough to push current to saturate the memristor, i.e. is unable to make its charge equal to qsat for some interval(s) as seen in Figure 8, Figure 9, Figure 11, Figure 12, Figure 14 and Figure 15.

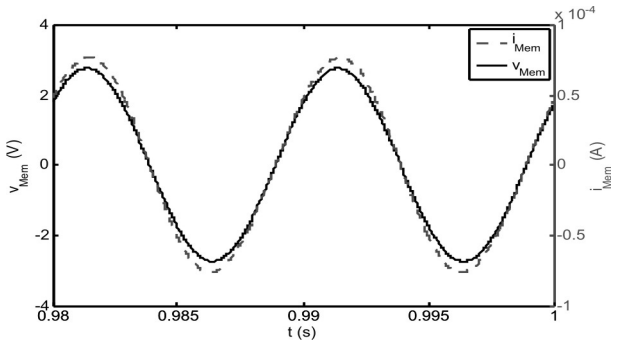


(a)

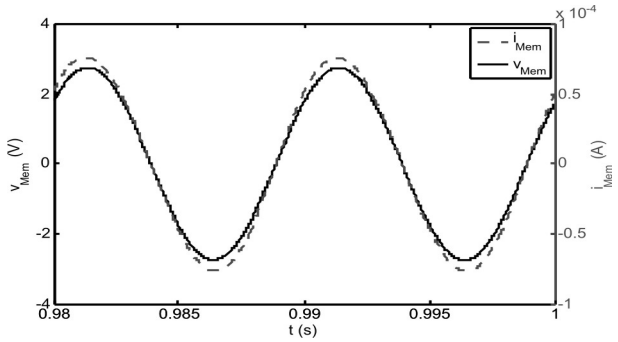


(b)

Figure 7: Memristor voltage and current with respect to time for q_{SAT}=0.075μC, q_0=0.1×q_{SAT} at f=2Hz, with (a) positive polarity (b) negative polarity

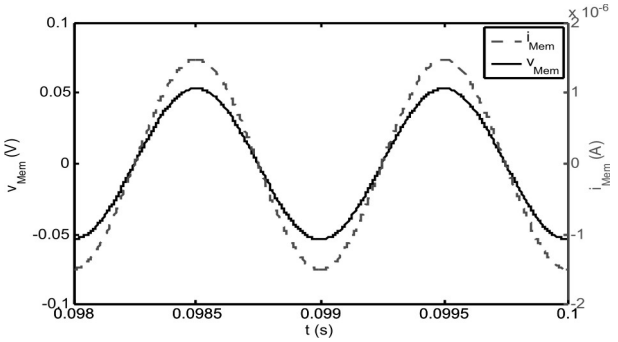


(a)

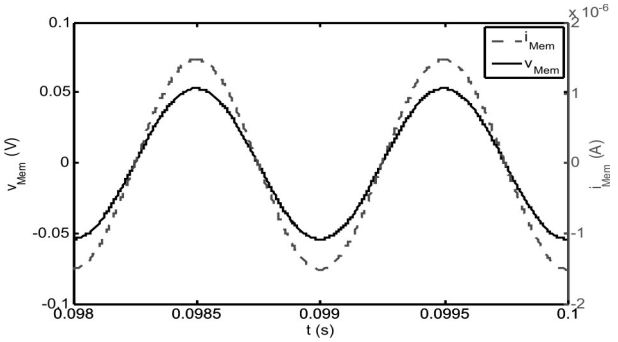


(b)

Figure 8: Memristor voltage and current with respect to time for q_{SAT}=2.5μC, q_0=0.1×q_{SAT} at f=100Hz, with (a) positive polarity (b) negative polarity

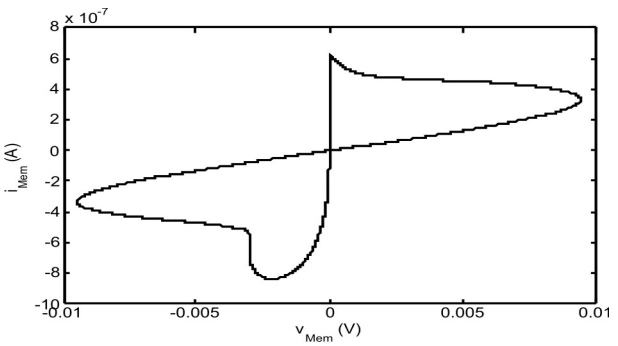


(a)

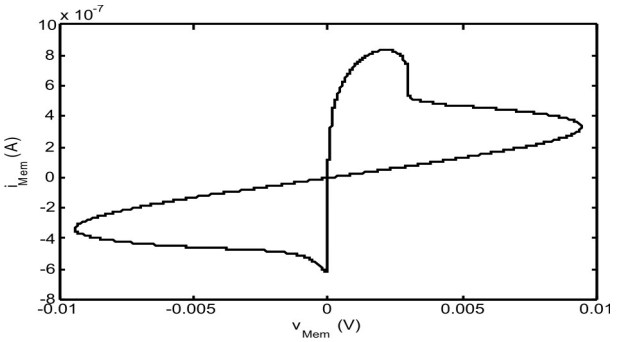


(b)

Figure 9: Memristor voltage and current with respect to time for q_{SAT}=2.5μC, q_0=0.1×q_{SAT} at f=1kHz, with (a) positive polarity (b) negative polarity



(a)



(b)

Figure 10: Memristor I-V characteristics for q_{SAT}=0.075μC, q_0=0.1×q_{SAT} at f=2Hz, with (a) positive polarity (b) negative polarity

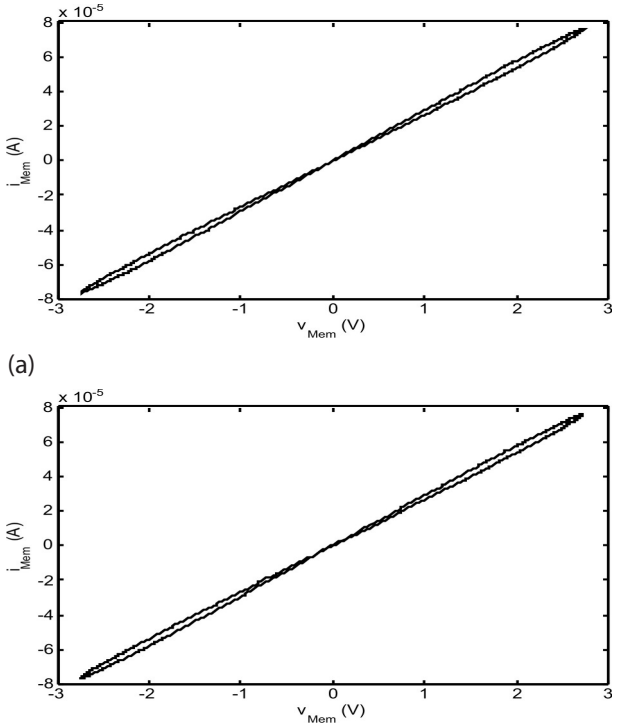


Figure 11: Memristor I-V characteristics for q_{SAT}=2.5μC, q_0=0.1×q_{SAT} at f=100Hz, with (a) positive polarity (b) negative polarity

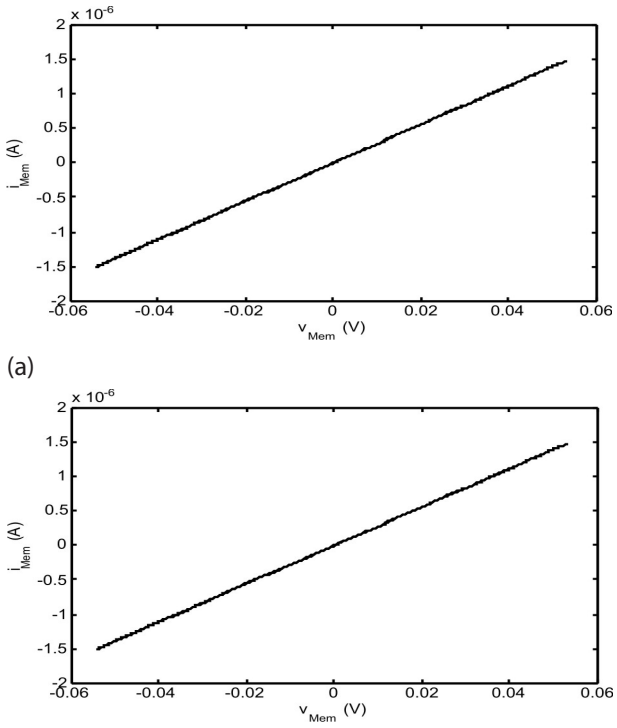


Figure 12: Memristor I-V characteristics for q_{SAT}=2.5μC, q_0=0.1×q_{SAT} at f=1kHz, with (a) positive polarity (b) negative polarity

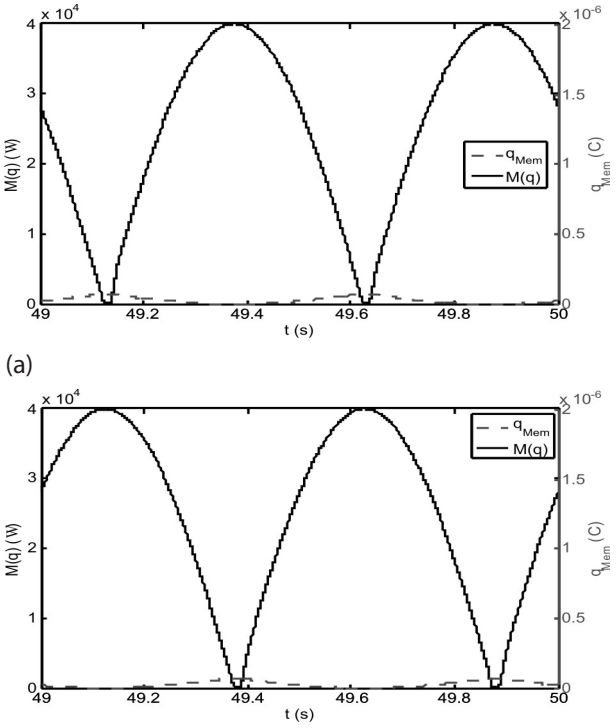


Figure 13: Memristance and memristor charge with respect to time for q_{SAT}=0.075μC, q_0=0.1×q_{SAT} at f=2Hz, with (a) positive polarity (b) negative polarity

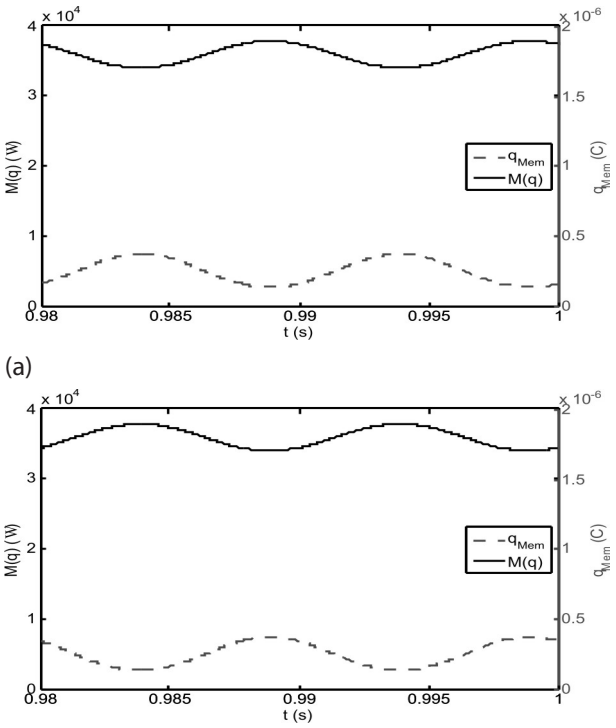


Figure 14: Memristance and memristor charge with respect to time for q_{SAT}=2.5μC, q_0=0.1×q_{SAT} at f=100Hz, with (a) positive polarity (b) negative polarity

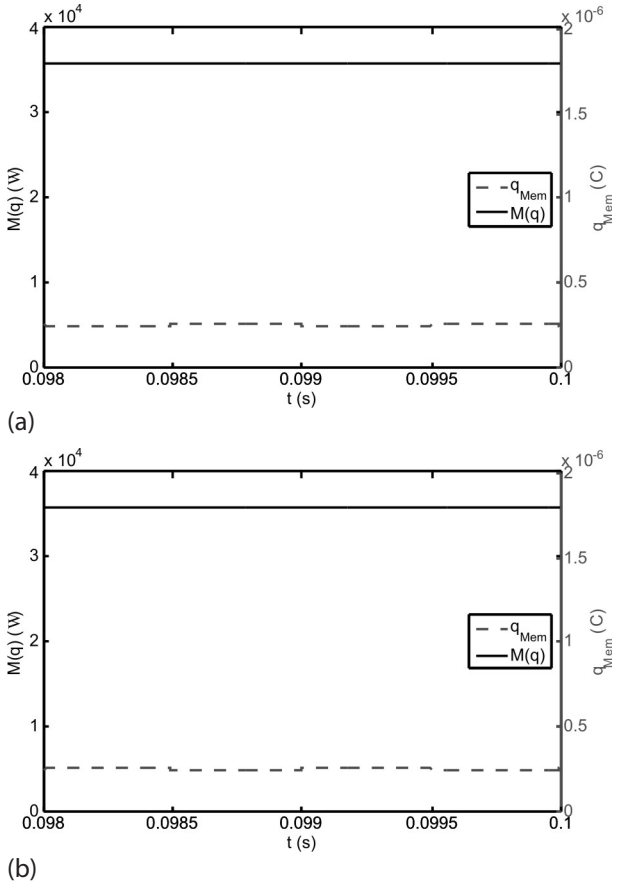


Figure 15: Memristance and memristor charge with respect to time for q_{SAT}=2.5μC, q_0=0.1×q_{SAT} at f=1kHz, with (a) positive polarity (b) negative polarity

The effects of the memristor polarity on the memristor waveforms are also analyzed and the corresponding curves are presented in Figure 7 - Figure 15 (b). If polarity of the memristor is switched as shown in Figure 3, the memristor currents for the reversed polarity are obtained by first 180° phase-shifting of the memristor current for the positive polarity and then flipping it with respect to horizontal-axis as shown in Figure 7 and Figure 8. At 1 kHz, since the frequency is sufficiently high, the memristor behaves as if it was a resistor, the polarity has no effect and the memristor voltages and currents for both polarities can be regarded as identical and sinusoidal as seen in Figure 9. For the reversed polarity, the memristor memristance and charge can be obtained by either phase-shifting of the memristor memristance and charge for the positive polarity by 180° or flipping them with respect to vertical axis as shown in Figure 13 and Figure 14. However, at 1 kHz, since the frequency is sufficiently high, the memristor behaves as a resistor, the polarity has no effect and the memristor memristance and charge can be regarded as constants as seen in Figure 15.

5.2 Filter output voltages with respect to time

Output voltages of memristor-based LP and BP filters are simulated. Corresponding time domain waveforms are provided in Figure 16 and Figure 17. As shown in Figure 16 and Figure 17, if the memristor has a low q_{SAT} value (q_{SAT}=0.075 μC here), it becomes saturated at very low frequencies as demonstrated in previous section and the output voltage has some distortion. The filter with either higher q_{SAT} value (q_{SAT}=2.5 μC here) or with the increasing of the frequency hasn't any distortion since it does not get saturated. That's why the memristor q_{SAT} value should be chosen high enough not to saturate the memristor over all the operating frequency range for a well-designed filter.

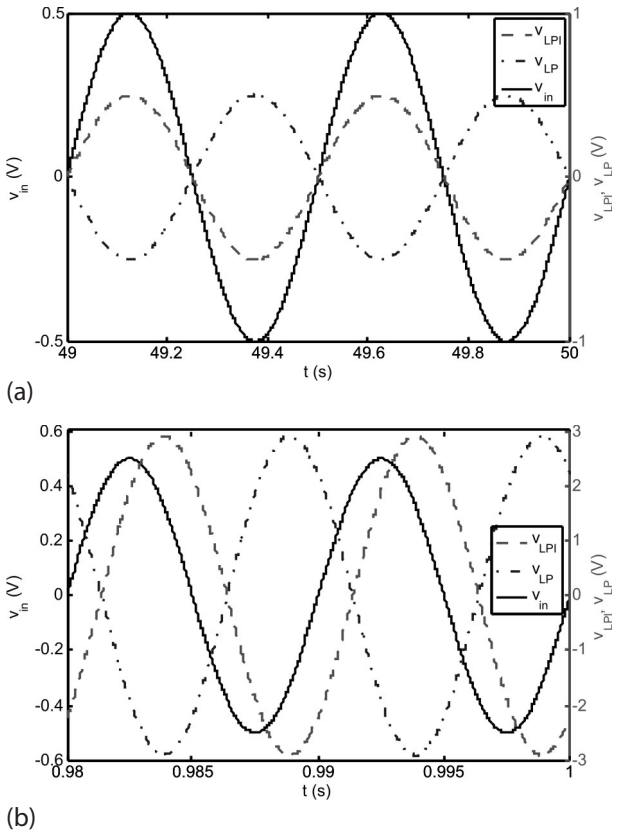


Figure 16: LP biquad filter input and output voltages as a function of time for q_0=0.1×q_{SAT} with positive polarity at a) f=2Hz, q_{SAT}=0.075μC (b) f=100Hz, q_{SAT}=2.5μC

5.3 Gain characteristics of filters

Gain characteristics of the biquad LP and BP filters with respect to frequency by taking M_{avg}, which is the average memristor memristance in steady-state, as parameter are shown in Figure 18. As it can be seen from the Figure 18 (a), (b) and (c), adjustable memristance in both BP and LP filters provides variable quality factor. Also an adjustable gain in BP biquad is obtained by inconstancy of the memristance as shown in Figure 18 (c).

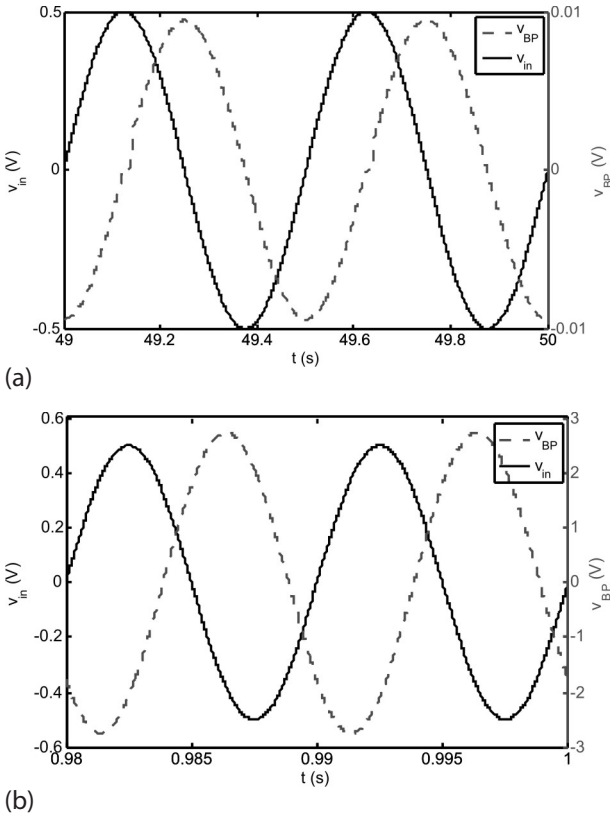


Figure 17: BP biquad filter input and output voltages as a function of time for $q_0=0.1\times q_{SAT}$ with positive polarity at a) f=2Hz, $q_{SAT}=0.075\mu C$ (b) f=100Hz, $q_{SAT}=2.5\mu C$

6 Conclusions

In this paper, a memristor-based biquad analog filter is examined by using a linear drift model of a memristor. Since an analytical solution was not available, the characteristics of the filter are observed by means of simulations.

Simulations have shown that the quality factor and BP filter gain at the resonant frequency can be adjusted by varying the average memristance of a memristor in a biquad filter. The effect of the memristor polarity on the biquad filter is also inspected. It has been found that, at low frequencies, the polarity also defines the shape of the memristor current, voltage and memristance waveforms but, at high frequencies, it has no effect, i.e. all waveforms have the same shape for both polarities since the memristor behaves as a resistor.

It has also been observed that the memristor, depending on its q_{SAT} value, may go into saturation at very low frequencies. Above the very low operation frequencies the biquad filter operates without saturation but with some distortion due to varying memristance. At high frequencies, the memristor behaves similar to a resistor and the filter operates well without distortion.

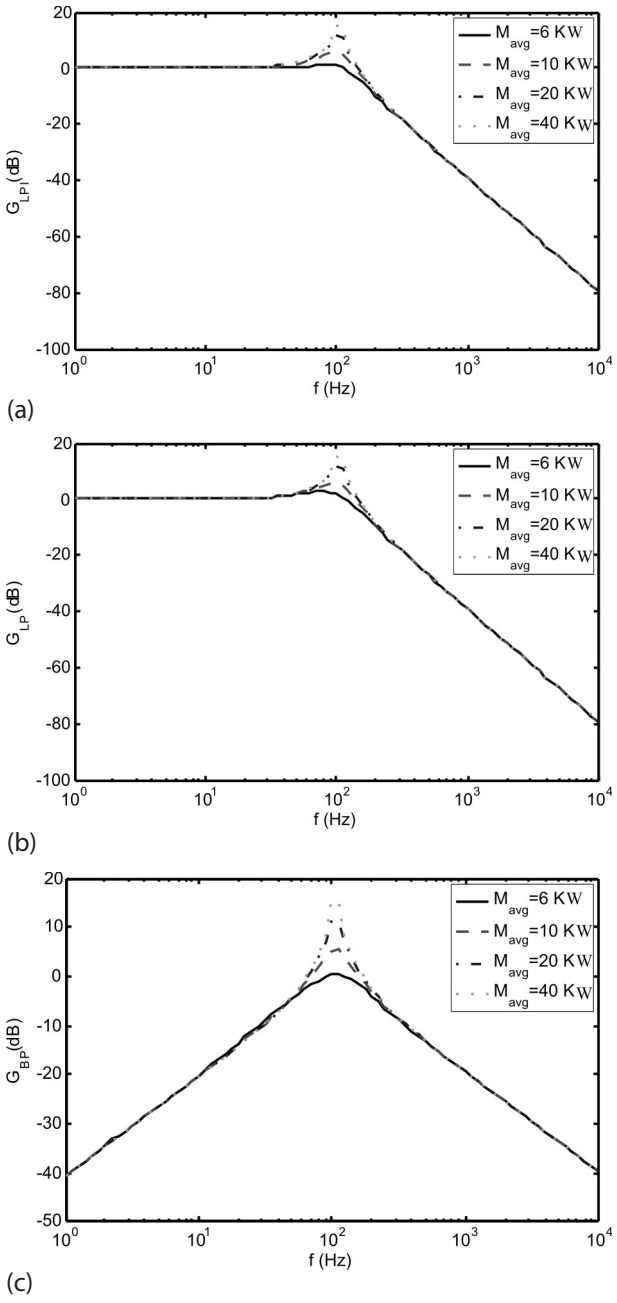


Figure 18: Filter gain characteristics with respect to frequency by taking M_{avg} is parameter, $q_{SAT}=2.5\mu C$ (a) LP (in-phase), (b) LP (c) BP filter

The undesired saturation or a big memristance perturbation in biquad filters results in distortion at output voltage waveforms. These issues for memristor-based biquad filters are considered for the first time in literature. That's why special precautions should be taken when designing memristor-based biquad analog filters regarding the input signal magnitudes and operation frequencies. The analysis of the filter can also be done using more complex models when they become available.

It is expected that the new circuit element, memristor, can contribute new properties to analog circuits. According to the results presented in this study, the variable memristance gives the memristor-based biquad filter adjustable characteristics, which cannot be mimicked with traditional resistors. The memristor-based biquad filter is able to tune the filter parameters, the gain at the resonant frequency, and the BP filter quality factor, i.e. the band-width. Results of this study can be used to design memristor-based biquad filters, fulfilling their performance and stability requirements.

7 References

1. Chua, L.O., "Memristor - the missing circuit element", IEEE Trans Circuit Theory, 18, pp. 507-519, 1971.
2. Strukov, D.B., Snider, G.S., Stewart, D.R., Williams, R.S., "The missing memristor found", Nature, 453, pp. 80-83, 2008.
3. Kavehei, O., Iqbal1, A., Kim, Y.S., Eshraghian, K., Al-Sarawi, S.F., Abbott, D., "The fourth element: characteristics, modelling and electromagnetic theory of the memristor", Proc. R. Soc. A, 2010.
4. Batas D., Fiedler H., "A memristor SPICE implementation and a new approach for magnetic flux-controlled memristor modeling". IEEE Transactions on Nanotechnology 2011; 10: 250-255.
5. Benderli S., Wey T.A. "On SPICE macromodelling of TiO2 memristors". Electron Letters 2009; 45: 377-379.
6. Yener Ş., Kuntman H. "A new CMOS based memristor implementation". In: International conference on Applied Electronics; 5 - 7 September 2012; University of West Bohemia, Pilsen, Czech Republic. pp. 345-348.
7. Pershin Y.V., Ventra D.M. "Practical approach to programmable analog circuits with memristors". IEEE Transactions on Circuits and Systems I: Regular Papers 2010; 57: 1857-1864.
8. Mutlu R. "Solution of TiO2 memristor-capacitor series circuit excited by a constant voltage source and its application to calculate operation frequency of a programmable TiO2 memristor-capacitor relaxation oscillator". Turk J Elec Eng & Comp Sci 2013; accepted, available online: DOI: 10.3906/elk-1108-38.
9. Shin S., Kim K., Kang S.M. "Memristor applications for programmable analog ICs". IEEE Transactions on Nanotechnology 2011; 10: 266-274.
10. Kim H., Sah M.P., Yang C., Cho S., Chua L.O. "Memristor emulator for memristor circuit applications". IEEE Transactions on Circuits and Systems I: Regular Papers 2012; 59: 2422-2431.
11. Driscoll, T., Quinn, J., Klein, S., Kim, H.T., Kim, B.J., Pershin, Y.V., Ventra, M.D., Bassov, D.N., "Memristive adaptive filters", Applied Physics Letters, 97, pp. 093502–1-093502–3, 2010.
12. Quereshi, M.S., Medeiros-Ribeiro, W.Y.G., Williams, R.S., "AC sense technique for memristor crossbar", Electronics Letters, 48, pp. 757-758, 2012.
13. Lee, T.W., Nickel, J.H., "Memristor resistance modulation for analog applications", IEEE Electron Device Letters, 33, pp. 1456-1458, 2012.
14. Chew, Z.J., Li, L., "Printed circuit board based memristor in adaptive lowpass filter", Electronics Letters, 48, pp. 1610-1611, 2012.
15. Ascoli, A., Tetzlaff, R., Corinto, F., Mirchev, M., Gilli, M., "Memristor-based filtering applications" In: 14th Latin American Test Workshop (LATW) 2013, 3-5 April 2013, Cordoba.
16. Mahvash, M., Parker, A.C., "A memristor SPICE model for designing memristor circuits", In: 2010 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 1-4 Aug, 2010, Seattle, WA.
17. Tow, J., "Active RC filters – a state space realization", Proceedings of the IEEE, 56, pp. 1137-1139, 1968.
18. Thomas, LC., "The biquad: part I - some practical design considerations", IEEE Transactions on Circuit Theory, 18, pp. 350-357, 1971.
19. Thomas, LC., "The biquad: part II - a multipurpose active filtering system", IEEE Transactions on Circuit Theory, 18, pp. 358-361, 1971.
20. Soliman A. M., "Voltage mode and current mode Tow Thomas bi-quadratic filters using inverting CCII", International Journal of Circuit Theory and Applications, Volume 35, Issue 4, pp. 463–467, 2007.
21. Tola, A.T., Arslanalp R., Yilmaz S.S., "Current Mode Tow-Thomas Biquadratic Differential Class AB Log Domain Filter" International Review of Electrical Engineering, Vol. 4 Issue 6, pp.1426-1432, 2009.
22. Ibrahim M.A., "Tunable Current-Mode Tow-Thomas Biquad Based on CDTAs", The Third International Conference on Digital Information Processing and Communications (ICDIPC2013) - United Arab Emirates, pp. 366-370, 2013.
23. Mita R., Palumbo G., Pennisi S., "Nonidealities of Tow–Thomas Biquads Using VOA- and CFOA-Based Miller Integrators", IEEE Transactions On Circuits And Systems—II: Express Briefs, Vol. 52, No. 1, 2005.
24. Meng X.R., Yu Z.H., "CFA based fully integrated Tow-Thomas biquad", Electronics Letters, Vol. 32, No. 8, 1996.
25. Sedra, A.L., Smith, K.C., "Microelectronic Circuits", 6th edn, Oxford University Press, 2004.
26. Van Valkenburg M.E.. "Analog Filter Design", CBC College Publishing, 1982. ¸

Arrived: 14. 12. 2014
Accepted: 29. 03. 2014

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 44, No. 2 (2014), 119 – 125

Impact of Downscaling on Analog/RF Performance of sub-100nm GS-DG MOSFET

P. K. Sahu, S. K. Mohapatra, K. P. Pradhan

Nano Electronics Laboratory, Department of Electrical Engineering, National Institute of Technology (NIT), Rourkela, Odisha, India

Abstract: This paper presents a systematic study to show the impact of channel length on the Analog/RF performances of gate stack (GS) silicon on insulator (SOI) architecture. The downscaling of channel length becomes the biggest challenge to maintain higher speed, low power and better electrostatic integrity for each generation. This investigation is done to find out the potential of the channel length in view of analog and RF performance measures of sub-100nm GS-double gate (DG) MOSFETs. The threshold voltage (V_{th}) is made constant by tuning the gate metal work function while downscale the channel length (L). The impact of channel length variation on subthreshold slope (SS), drain induced barrier lowering (DIBL), transconductance (g_m), output conductance (g_d), early voltage (V_{EA}), transconductance generation factor (TGF), intrinsic gain (A_V), cut-off frequency (f_T), transconductance frequency product (TFP), gain frequency product (GFP) and gain transconductance frequency product (GTFP) are rigorously examined. It is shown that gate stack design results in higher cut-off frequency along with a broader analog 'sweet spot' in nanoscale MOSFETs thus offering better possibilities for analog/RF scaling below 50nm. For shorter gate length devices (L=30nm), the design results in an impressive 69.10% improvement in f_T along with 36.31% enhancement in 'sweet spot' as compared to L=60 nm. The study generates an optimized channel length of L=40 nm for the designed device dimension in connection with the analog and RF performance for circuit design.

Keywords: Gate Stack (GS), DG-MOSFETs, Metal Gate Technology, Analog/RF FOMs, Sweet Spot

Vpliva pomanjševanja na analogne/RF lastnosti pod-100 nm GS-DG MOSFETa

Izvleček: V članku je predstavljana sistematična študija vpliva dolžine kanala na analogne RF lastnosti arhitekture večplastnih vrat (GS) silicija na izolatorju (SOI). Največji izziv pri krajšanju kanala je ohranjanje visoke hitrosti, nizke moči in boljše elektrostatične celote. Raziskava odkriva potenciale dolžine kanala pri analognih in RF lastnostih. MOSFET-ov z dvojnimi vrati. Konstantnost pragovne napetosti pri krajšanju kanala se je ohranjala s spreminjanjem delovne funkcije kovinskih vrat. Raziskan je vpliv krajšanja kanala na podpragovni naklon (SS), ponorno vzbujano nižanje bariere, transkonduktanco (g_m), izhodno prevodnost (g_d), zgodnjo napetost (V_{EA}), generacijski faktor transkonduktance (TGF), intrinsično ojačenje (A_V), frekvenco reza (f_T), produkt transconduktančne frekvence (TFP), produkt frekvence ojačenja (GFP) in produkt frekvenc ojačenja in transkonduktance (GTFP). Izkazalo se je, da večplastna vrata omogočajo višje frekvence reza skupaj s širšim območjem najboljšega delovanja v nanodimenzijskih MOSFET-ih, kar omogoča krčenje na 50 nm. Pri krajših dolžinah vrat (L=30nm) oblika izkazuje impresivno 69.10 % izboljšanje f_T in 36.31 % izboljšanje območja najboljšega izplena v primerjavi z L = 60 nm. Izkazalo se je, da je optimalna dolžina kanala 40 nm.

Ključne besede: večplastna vrata, DG-MOSFET, tehnologija kovinskih vrat, Analogni/RF FOM, območje najboljšega izplena

* *Corresponding Author's e-mail: kp2.etc@gmail.com*

1 Introduction

The use of low power and high frequency operated devices are having a high priority for future electronic applications. Silicon on Insulator (SOI) devices are excellent candidates as an alternative for the conventional bulk CMOS [1-2]. Advanced MOSFET structures such as ultra-thin body (UTB) SOI double gate (DG) MOSFET can be scaled more aggressively than bulk Si structure [3]. A double gate structure fabricated on SOI wafer has been utilized in CMOS technology due to their excellent scaling capability, outstanding Short Channel Effects (SCEs) immunity, high current drivability (I_{on}) and transconductance (g_m) and lower leakage current (I_{off}) as compared to the bulk MOSFETs [4-10]. Channel length scaling is limited by the ability to control off-

state leakage current due to quantum tunneling and thermionic emission between the source and drain.

The analog and RF circuits with a digital CMOS technology suffers from many challenges. More over the technology is optimized for digital design and the devices are characterized for current drive and gate delay. For System on Chip (SoC) and System in Package (SiP) applications, optimization of the devices becomes more challenging. SiP refers to a semiconductor device that incorporates multiple readily available chips into a single package; while SoC refers to a device that incorporates a system of differently functioning circuit blocks on a single silicon chip. So it is required to enhance the performance for digital and analog/RF circuit applications [11-18]. Major semiconductor companies such as IBM, RFMD, Honeywell, OKI, etc., have already produced several products for the telecommunication market based on SOI RF technologies.

In this work, a study has been made with designing different device cases by varying channel length (L) keeping all other process parameters constant for high-k/metal gate (HKMG) DG-MOSFETs. In our analysis, Analog/RF devices designed around the 'sweet spot' (compromise between power and speed performance, and linearity) signified by the peak of transconductance to current ratio (g_m/I_D) and cut-off frequency (f_T) product, typically characterized by a gate voltage of 0.35 V. The device performance is investigated keeping in view for analog and RF circuit application. For the analysis, the threshold voltage (V_{th}) is maintained at a constant value for all cases by tuning the gate metal work function between 4.6 eV to 4.7 eV. The V_{th} is achieved a constant value of 0.2V for all channel length device cases. Section 2 describes the device description that includes all the dimensions, materials and doping concentrations of HKMG DG-MOSFET. Section 3 analyses the physics of the device using device numerical simulations and models activated for simulation. In section 4, various performance metrics of the device including the short channel effects (SCEs) like SS, DIBL, and the important analog and RF FOMs such as g_m, g_d, TGF, V_{EA}, A_V, C_{gs}, C_{gd}, f_T, TFP, GFP, GTFP have been closely observed. Finally, the concluding remarks have been included in section 5.

2 Basic Structure

For the purpose of study a planar DG SOI n-channel transistor is considered. For the simulation a symmetric device structure model has been designed. Four different channel lengths (L= 60nm, 50nm, 40nm, and 30nm) are chosen for the device to analyze the device performance. The schematic simulated structure is shown in Fig. 1, where the silicon channel is surrounded above and below by two layer of oxide, SiO_2 and HfO_2. Metal gate technology is attractive because, it eliminates the poly-Si gate depletion effect and the associated degradation in transistor performance. To achieve a constant V_{th}, the work function of the metal gate is tuned in between 4.6 eV to 4.7 eV while varying the channel length of the device.The doping profile for channel (p-type 10^{16} cm^{-3}) and source, drain (n-type 10^{20} cm^{-3}) are set. For a better comparison of analog/RF FOMs, the V_{th} is maintained at a constant value 0.2 V while varying the metal gate work function at V_{DS}=0.1 V.

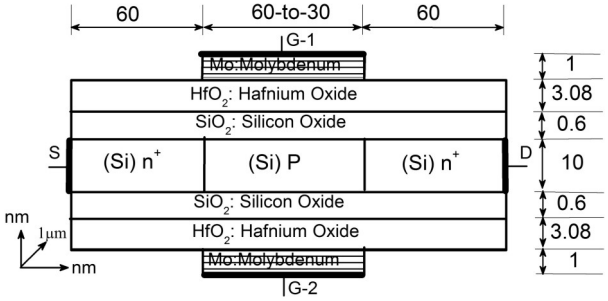


Figure 1: Schematic structure of Double Gate N-MOSFET

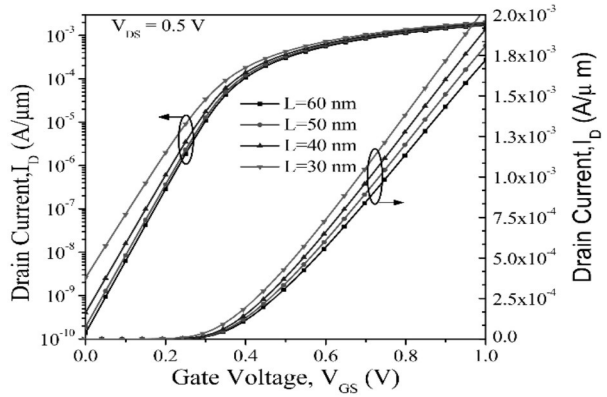
3 Device Simulation

The 2-D numerical device simulator ATLAS is employed to simulate the planner DG-MOSFET with high-k/metal gate. According to International Technology Roadmap for Semiconductors (ITRS), the drain bias has been fixed at V_{DD} = 1.0 V [19]. In order to study the analog performance, the simulation is performed with V_{DS} = 0.5 V (which is half of the supply voltage i.e., $V_{DD}/2$) [20-21] with variable V_{GS} = 0 V to 1.0 V. Threshold voltage (V_{th}) is extracted using constant current (I_D=10^{-6} A/μm) definition from the I_D-V_{GS} transfer characteristic at V_{DS}=0.1 V. The threshold voltage is used to find out the gate overdrive voltage (V_{GT}=V_{GS}-V_{th}). The gate over drive voltage is an important property of amplifier circuit as it decides the region of operation. The increment of V_{GT} increases drain current until saturation. Hence in our investigation all the analog and RF analysis has been done against V_{GT} [22- 23]. For more accuracy, it is essential to account for the mobility degradation inside the inversion layers. The degradation normally occurs as a result of higher surface scattering near the semiconductor to insulator interface. Hence, during simulation, the inversion-layer Lombardi constant voltage and temperature (CVT) mobility model has been considered. The Shockley–Read–Hall (SRH) generation and recombination parameters simulate the leakage currents existing due to thermal generation are incorporated in

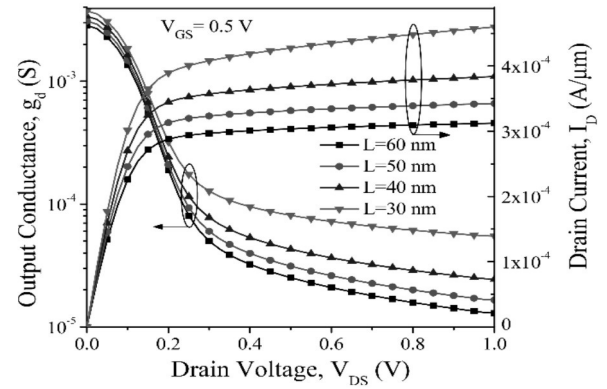
the simulation. At thermal equilibrium, a semiconductor lattice obeys Fermi-Dirac statistics. The use of Boltzmann statistics is normally justified in semiconductor device theory. However, Fermi-Dirac statistics are necessary to include for certain properties of very highly doped (degenerate) materials. The model Fermi-Dirac uses a Rational Chebyshev approximation that gives results close to the exact value. In the simulation all the junctions of the structure are considered to be of abrupt. Suitable empirical parameter β is selected to calibrate the drift diffusion transport model [20]. The biasing conditions are granted as per the room temperature T=25 °C. Furthermore, we have chosen two numerical techniques Gummel and Newton to obtain the solutions [24].

4 Results and Discussion

In order to analyze the impact of channel length of the device on the performance, simulation is done for four different channel lengths as 60 nm, 50 nm, 40 nm, and 30 nm.



(a)



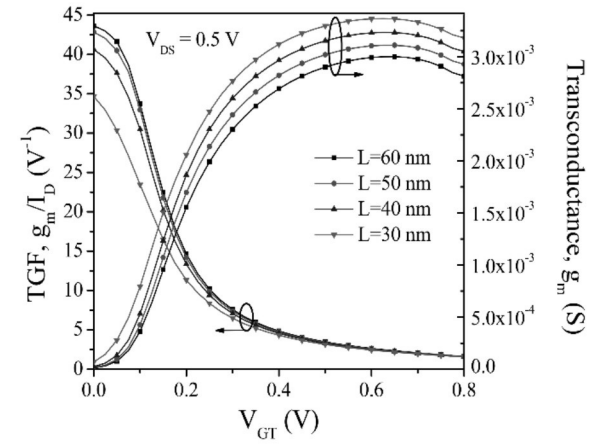
(b)

Figure 2: Drain current (I_D) in both linear and log scale as a function of gate to source voltage (V_{GS}) (b) Output conductance (g_d) and drain current (I_D) with respect to drain to source voltage (V_{DS}) for different channel lengths.

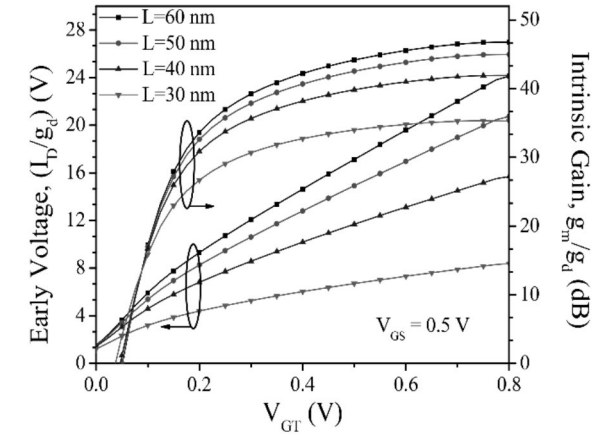
However, for analog and RF performance comparison among all the channel length cases, V_{th} kept constant (0.2 V) by adjusting the metal gate work function between 4.6 eV and 4.7 eV. The I_D-V_{GS} transfer characteristics both in linear and log scales have been shown in Fig. 2 (a) for different configurations at V_{DS}=0.5 V. The leakage current (I_{off}) is quit constant for three different channel length except L=30 nm. In the short channel device the I_{off} increases due to random motion of charge carriers. As channel length decreases, it gives rise to high drain current because of the relation $I_D \propto 1/L$. However, from the log scale, the leakage current is also prominent for lower channel lengths.Drain current (I_D) and output conductance (g_d) against drain to source voltage (V_{DS}) for different cases at V_{GS}=0.5 V are presented in Fig.2 (b). As per the Fig.2 (b), the drain current is increasing with decrease in channel length which in turn makes; the g_d high for lower L devices as $g_d=\partial I_D/\partial V_{DS}$. As we know from the literatures that gain and early voltage are inversely proportional to output conductance, so the device having lower L gives higher g_d which comprises lower gain and early voltage of the device.

Transconductance generation factor (TGF=g_m/I_D) and transconductance (g_m) as a function of gate over drive voltage ($V_{GT}=V_{GS}-V_{th}$) are presented in Fig.3 (a). From the figure, it is clear that as the channel length decreases the g_m value is increasing because of high drain current. The g_m/I_D ratio demonstrates how efficiently the current is used to achieve a certain value of transconductance. The advantage of high transconductance-to-drain ratio is the realization of circuits operating at low supply voltage. As shown in the figure, g_m/I_D is maximized towards the subthreshold region of device operation. From the Fig.3 (a), it is clear that the structure having channel length 60 nm shows higher g_m/I_D ratio as compare to others and it decreases as channel length decreases. Fig.3 (b) shows the variation of the early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for different channel lengths. For better analog performance the V_{EA} and A_V should be as high as possible. An enormous improvement is observed in V_{EA} for channel length L=60 nm as compared to others.

The intrinsic gain of the device, which is a ratio of transconductance and output conductance for various channel lengths is plotted against gate voltage (V_{GS}) for V_{DS}=0.5 V is shown in Fig.3 (b). The intrinsic gain ($A_V=g_m/g_d$) is a valuable figure of merit for operational transconductance amplifier. From the figure, the device having channel length 60 nm gives highest gain from others and it decreases as the channel length decreases. Both the extracted values of SS and calculated values of DIBL for different channel lengths are tabulated in Table 1.



(a)



(b)

Figure 3: (a) Transconductance generation factor (TGF) and transconductance (g_m) (b) Early voltage (V_{EA}) and intrinsic gain (A_V) as a function of gate over drive voltage (V_{GT}) for different channel lengths.

The DIBL calculation is performed for V_{th} at V_{DS}=0.1 V and V_{DS}=1.0 V. From the table, it is clear that the SS value increases as channel length decreases and it is high for channel length 30 nm. Similarly, the DIBL value also increases as channel length decreases and it gives a maximum value for channel length of 30 nm. These two parameters are very important for short channel effects, which should be minimized. The maximum values for g_m, g_d, V_{EA}, A_V, TGF are also tabulated in Table 1. I_D increases for lower channel length devices which consequently increases g_m values for devices having lower value of L. However, because of high g_d, the V_{EA}, and A_V becomes lower as L decreases. Coming from L=60 nm to 30 nm, the DIBL and SS values are more prominent for lower channel length devices and also the TGF and Gain are decreases as L decreases.

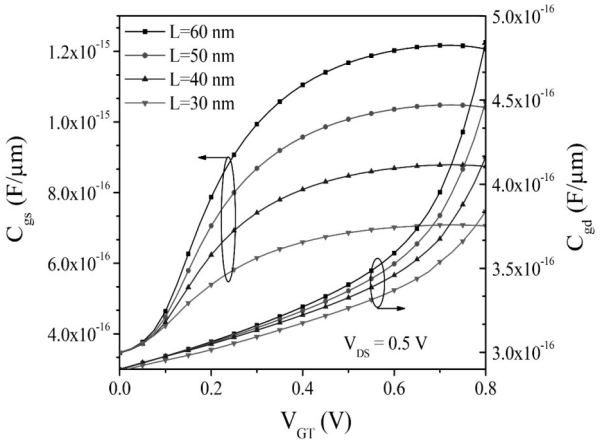


Figure 4: Gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) as a function of gate over drive voltage (V_{GT}) for different channel lengths.

Fig. 4 shows the intrinsic capacitances (C_{gs} & C_{gd}) as a function of V_{GT}. As shown in figure, the intrinsic capacitance parameters increase swiftly in the super threshold region. This is because of the increase in the fringing field lines emanating from the gate edges. The device having channel length 60nm shows higher values of intrinsic capacitances (both C_{gs} & C_{gd}) and it decreases as channel length decreases. From Fig.5 (a), the variations of cut off frequency ($f_T=g_m/2\pi(C_{gs}+C_{gd})$) and gain transconductance frequency product ($GTFP=A_V*TGF*f_T$) can be observed with respect to V_{GT} for different values of channel lengths. Here, the value of f_T obtained for the device having low channel length is higher and it gradually decreases as the channel length decreases. f_T is inversely proportional to the intrinsic capacitances (C_{gs} & C_{gd}). So, f_T value is low due to high capacitance values for higher channel length devices. It is interesting to see that the device having

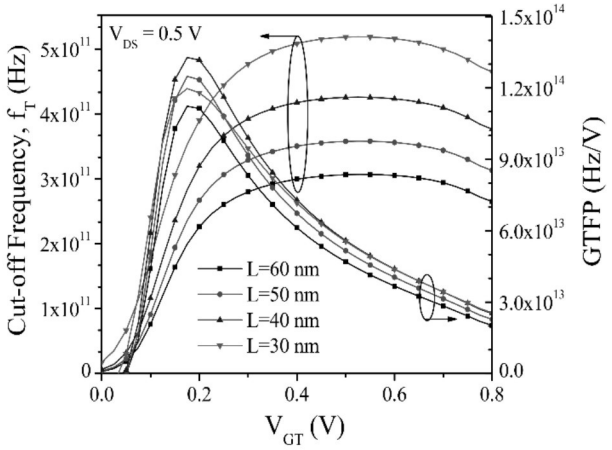
Table 1: Electrostatic & Analog performances for different values of channel lengths

Channel Length (nm)	DIBL (mV/V)	SS (mV/decade)	Transconductance, g_m (mS)	Output Conductance, g_d (μS)	Early Voltage, V_{EA} (V)	Gain, A_V (dB)	TGF (V^{-1})
		V_{DS}=0.5V					
L=60	20.71	62.31	2.81	12.94	24.130	46.742	43.637
L=50	21.12	63.12	2.93	16.57	20.737	44.969	42.840
L=40	37.24	65.95	3.05	24.53	15.787	41.921	40.639
L=30	49.88	68.35	3.18	54.84	8.499	35.458	34.669

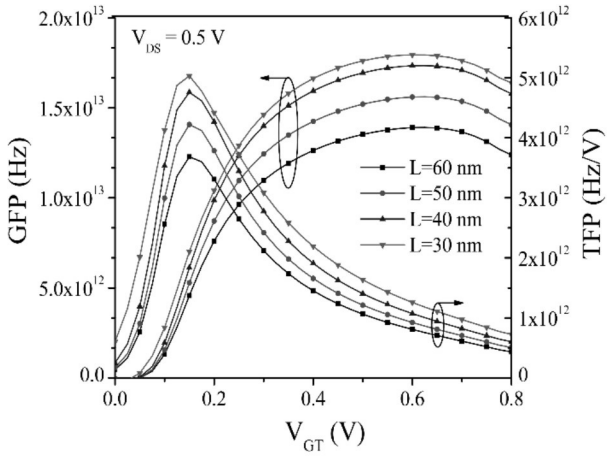
Table 2: RF performances for different values of channel lengths

Channel Length (nm)	C_{gs} (fF)	C_{gd} (fF)	f_t (GHz)	GFP (GHz)	TFP(GHz/V)	GTFP (GHz/V)
L=60	1.207	0.484	306.78	4.57*103	3.69*103	1.12*105
L=50	1.041	0.449	358.00	5.27*103	4.22*103	1.25*105
L=40	0.874	0.416	425.80	6.12*103	4.76*103	1.33*105
L=30	0.706	0.384	518.79	7.02*103	5.03*103	1.20*105

channel length L=40 nm shows a higher GTFP value as comparison to others. This is due to the reduction in peak electric field, lower output conductance of the device having channel length 40nm. The GTFP value is very low for L=30nm.



(a)



(b)

Figure 5: (a) Cut off frequency (f_T) and gain transconductance frequency product (GTFP) (b) Gain frequency product (GFP) and transconductance frequency product (TFP) as a function of gate over drive voltage (V_{GT}) for different channel lengths.

The product of g_m/I_D and f_T represents a trade-off between power and bandwidth and is utilized in moderate to high speed designs. Fig.5 (b) gives the gain frequency product ($GFP=A_V*f_T$) and TFP against gate over drive voltage (V_{GT}) for different values of channel lengths. From the figure, the value of GFP increases as channel length decreases and reaches utmost for the device having channel length 30nm. The same figure also shows transconductance frequency product (TFP) as a function of V_{GT} for different values of channel lengths. Where the bandwidth is flexible and part of the overall optimization process, it is important to consider the product of g_m/I_D and f_T as shown in Fig. 5 (b). This figure of merit exhibits a 'sweet spot' i.e., peak value for all device cases. Peak values for the product (TFP) increases from $3.69*10^3$ $GHzV^{-1}$ to $4.76*10^3$ $GHzV^{-1}$ when gate length (L) is reduced from 60nm to 30nm. The maximum values for TFP i.e., 'sweet point' is achieved at a gate voltage of 0.35 V which is 0.15 V more than from the threshold voltage. From the figure it is clear that the device having channel lengths 40nm and 30nm gives higher TFP values as comparison to others.

All the extracted values for analog/RF FOMs are plotted in Table 2 for different values of channel lengths. It is clear from the Table that, while the gate length is reduced the RF FOMs like f_T, GFP and TFP are also increased because of high drain current which results in higher g_m values for shorter gate length devices. However, the improvement in GTFP, which is a unique and major FOM, with L downscaling reduces below 40 nm due to short channel effects. From Table 1, the A_V values are obtained around 41.921 dB and 35.458 dB for 40nm and 30nm respectively whereas the g_m/I_D shifts lower to 34.669 V^{-1} for 30nm technology from 40.639 V^{-1} for 40nm technology. The GTFP is nothing but the product of three parameters i.e., TGF, gain and frequency, so the peak values are more for 40 nm technology as compare to 30 nm technology.

5 Conclusion

A detailed study on the analog/RF performance measure of GS-DG MOSFETs has been presented. It has been demonstrated that analog/RF performance metrics can be significantly enhanced by down scaling the channel length in terms of (a) analog 'sweet spot' and (b) compromise between gain and cut-off frequency i.e., GFP. However, the improvement in GTFP with L down scaling continues up till 40nm where a peak value of $1.33*10^5$ $GHzV^{-1}$ is attained. Beyond 40 nm, peak GTFP

value reduces to 1.20*10^5 $GHzV^{-1}$ in 30 nm GS-DG MOSFET due to short channel effects (peak g_m/I_D~34.669 V^{-1} and gain~35.458 dB, Table 1). So, from the results it is clear that all studied parameters are more sensitive to the channel length (L) of the device. The calculated and simulated results demonstrate that the optimized value of "L" will be 40 nm for the chosen device dimension. The values of the parameters like DIBL=37.24 mV/V, SS=65.95 mV/decade, I_{on}=1.912 mA, A_V=41.92 dB, f_T=425.80 GHz, GTFP=1.33*10^5 GHz/V are achieved for L=40 nm. The other device parameters could also be properly chosen for further downscaling of the transistor.

Due to lack of fabrication facilities, we can't validate our simulation results with the experimental results in literature. However, as our simulation is calibrated with experimental results, so we can give a formal assurance that degradation of studied parameters may not be expected when implementing MOSFETs in a real chip/ SoC.

6 References

1. D.J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, H. Wong, "Device scaling limits of Si MOSFETs and their application dependencies", *Proc. IEEE*, Vol. 89 , No.3, pp. 259–288, Mar., 2001.
2. Leland Chang, Y-K Choi, D Ha, P Ranade, S Xiong, J Bokor, C Hu, And T-J King, "Extremely Scaled Silicon Nano-CMOS Devices", *Proceedings of The IEEE*, vol. 91, no. 11, pp. 1860 – 1873, Nov., 2003.
3. Isabelle Ferain, Cynthia A. Colinge, Jean-Pierre Colinge, " Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors", *Nature*, vol.-479, pp.310-316, Nov., 2011.
4. K. Suzuki, Y. Tosaka, T. Tanaka, H. Horie, Y. Arimoto, "Scaling theory of double-gate SOI MOSFET's", *IEEE Transactions on Electron Devices*, Vol. 40, No.12, pp.2326–2329, Dec., 1993.
5. Scott Thompson, Paul Packan, Mark Bohr, "MOS Scaling: Transistor Challenges for the 21st Century" *Intel Technology Journal*, vol. 2, issue 3, 1998.
6. Colinge J.P. "Multiple-gate SOI MOSFETs" *Solid State Electron*ics, Vol. 48, No.6, pp.897–905, June, 2004.
7. C. Wann, K. Noda, T. Tanaka, M. Yoshida, and C. Hu, "A Comparative study of advanced MOSFET concepts", *IEEE Transactions onElectron Devices*, Vol. 43, pp. 1742, Oct. 1996.
8. H.-S. P. Wong "Beyond the conventional transistor" *IBM J. Res. & Dev.*, Vol. 46, No. 2/3, Mar./May, 2002.
9. G. K. Cellera, Sorin Cristoloveanu, "Frontiers of silicon-on-insulator", *Journal of Applied Physics*, Vol., No.-9, pp.4955-4978, May, 2003.
10. Chaudhry, M.J. Kumar, "Controlling short-channel effects in deep submicron SOI MOSFETS for improved reliability: a review", *IEEE Transaction on Device Material Reliability* , Vol. 4, No.3, pp. 99–109, Mar, 2004.
11. Jean-Pierre Colinge, "Fully-Depleted SOI CMOS for Analog Application", *IEEE Transaction on Electron Devices*, Vol.-45, No.-5, pp.-1010-1016, May, 1998.
12. Behzad Razavi, "CMOS Technology Characterizationfor Analog and RF Design", *IEEE Journal Of Solid-State Circuits*, Vol.-34, No.-3, pp.-268-276, Mar., 1999.
13. Valeriya Kilchytska, A Nève, L Vancaillie, D Levacq, S Adriaensen, H V Meer, K De Meyer, C Raynaud, M Dehan, J P Raskin, D Flandre, "Influence of Device Engineering on the Analog and RF Performances of SOI MOSFETs", *IEEE Transactions on Electron Devices*, Vol. 50, No.3, pp. 577–588, Mar., 2003.
14. Lazaro, B. Iniguez, "RF and noise performance of double gate and single gate SOI",*Solid-State Electronics*, Vol. 50, Issue 5, pp. 826–842, May, 2006.
15. Jean-Pierre Raskin, Tsung Ming Chung, Valeria Kilchytska, Dimitri Lederer, Denis Flandre,"Analog/ RF Performance of Multiple Gate SOIDevices: Wideband Simulations and Characterization",*IEEE Transactions on Electron Devices*, Vol. 53, No.5, pp. 1088–1095, May, 2006.
16. N. Mohankumar, B Syamal, C K Sarkar, "Influence of Channel and Gate Engineering on the Analog and RF Performance of DG MOSFETs", *IEEE Transactions on Electron Devices* , Vol. 57, No. 4, pp. 820–826, Apr., 2010.
17. Angsuman Sarkar, Alok Kumar Das, Swapnadip De, Chandan Kumar Sarkar, "Effect of gate engineering in double gate MOSFETs for analog/RF applications", *Microelectronics Journal*, Vol. 43, pp.-873-882, July, 2012.
18. Rupendra Kumar Sharma, Matthias Bucher, "Device Design Engineering for Optimum Analog/ RF Performance of Nanoscale DG MOSFETs", *IEEE Transactions on Nanotechnology*, Vol.-11, no.-5, pp.-992-998, Sept., 2012.
19. The International Technology Roadmap for Semiconductors [Online]. Available: http://public.itrs.net/ reports.html.
20. K. P. Pradhan, S. K. Mohapatra, P. K. Sahu, D. K. Behera, "Impact of High-k Gate Dielectric on Analog & RF Performance of Nanoscale DG-MOSFET", *Microelectronics Journal* , vol. 45, Issue 2, pp.-144-151, Feb., 2014.
21. Abhijit Mallik; Chattopadhyay, A., "Tunnel Field-Effect Transistors for Analog/Mixed-Signal System-on-Chip Applications," *IEEE Transactions on Electron Devices*, vol.59, no.4, pp.888,894, April, 2012.

22. N. Mohankumar, Binit Syamal, C.K. Sarkar, "Investigation of novel attributes of single halodual-material double gate MOSFETs for analog/RF applications", *Microelectronics Reliability*,vol. 49, Issue 12,pp.-1491-1497, Dec., 2009.
23. Saurav Chakraborty, Abhijit Mallik, Chandan Kumar Sarkar, "Subthreshold Performance of Dual-Material Gate CMOS Devices and Circuits for Ultralow Power Analog/Mixed-Signal Applications", *IEEE Transactions on Electron Devices* , Vol. 55, No.3, pp. 827–832, Mar. 2008.
24. ATLAS manual: SILVACO Int. Santa Clara, 2008.

Arrived: 18. 12. 2013
Accepted: 25. 03. 2014

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 44, No. 2 (2014), 126 – 136

Micropreconcentrators In Silicon-Glass Technology for the Detection of Diabetes Biomarkers

Artur Rydosz

AGH University of Science and Technology, Krakow, Poland

Abstract: In the present study concentration factors (CF) obtained for diabetes biomarkers such as acetone, propane, ethanol and ethylbenzene in a micropreconcentrator structure are presented. The concentration factor is defined as the ratio of gas preconcentration after and before preconcentration process. It was calculated from GC measurements as the ratio of peak area before and after desorption. The micropreconcentrator was manufactured using silicon-glass technology. The structure is 1.68 mm thick and has lateral dimensions 2 cm by 2 cm. It contains a 12 cm-long channel etched in an Si wafer. The micropreconcentrator is based on thermal desorption, and therefore the Pt heater was positioned at the bottom of the structure. The paper presents the technology behind the micropreconcentrator, and the thermal and preconcentration measurements of the manufactured structures. The Carboxen-1018 adsorbent material used in the experiments has also been studied. It is recommended by Sigma-Aldrich as a promising material for measuring concentrations of volatile organic compounds present in human breath. The lowest concentration factor value is around 30 for a mixture of diabetes biomarkers and the highest around 2800 for a single biomarker, i.e. acetone. The gas mixture has been prepared from certified gases using mass flow controllers (MFC) and a GC/MS setup.

Keywords: Breath analysis, gas detectors, silicon-glass technology, micropreconcentrators

Mikro predkoncentratorji tehnologije silicij-steklo za določevanje biomarkerjev diabetesa

Izvleček: Raziskava predstavlja koncentracijske faktorje (CF) biomarkerjev diabetesa, kot so aceton, propan, etanol in etilbenzen, v mikro predkoncentratorski strukturi. Faktor koncentracije je določen kot razmerje predkoncentracije plina pred in po predkoncentracijskim procesom. Računan je iz GC meritev vršnih površin pred in po desorpciji. Mikro predkoncentrator je razvit v tehnologiji silicij-steklo. Struktura je 1velika 2 x 2 cm^2 in 1.68 mm debela. Vsebuje 12 cm, v silicijevo rezino jedkan, kanal. Ker mikro predkoncentrator deluje na osnovi termične desorpcije, je Pt grelec nameščen na dno strukture. Članek predstavlja tehnologijo mikro predkoncentratorja ter termične in predkoncentratorske meritve izdelanih struktur. V raziskavah je bil, kot absorpcijski material, uporabljen Carboxen-1018, ki ga podjetje Sigma-Aldrich promovira za meritev hlapnih organskih deležev v izdihanem zraku. faktor koncentracije za mešanico biomarkerjev diabetesa je 30, najvišji faktor koncentracije za posamezen biomarker pa 2800. Plinska mešanica je bila pripravljena iz certificiranih plinov s pomočjo kontrolerjev masnega pretoka in GC/MS merilnega mesta.

Ključne besede: analiza dihanja, detektorji plina, tehnologija silicij-steklo, mikro predkoncentratorji

** Corresponding Author's e-mail: artur.rydosz@agh.edu.pl*

1 Introduction

According to data provided by the World Health Organization (WHO), 347 million people worldwide have diabetes. WHO projects that diabetes will be the seventh leading cause of death in 2030 [1]. Current management of diabetes is mainly based on repeated testing of blood glucose. Other key metabolic variables such as insulin and lipids are less frequently controlled [2]. Blood glucose measurement is an invasive method, with a risk of serious consequences for the patient in case of infection. Frequent blood testing is especially necessary for patients receiving insulin treatment. The global recommendation is for patients to monitor their blood glucose concentration at least 3 times daily [3]. However, this is expensive, impractical and can be painful. New approaches for diabetes monitoring have been under consideration for many years. One alternative non-invasive method is breath analysis [4 -

8]. The human breath contains almost 3500 different volatile organic compounds (VOCs) [9]. Some of them are biomarkers, since their presence in breath indicates disease. The total number of diseases that can be detected by breath analysis is still unknown. However, results of breath analysis are presented in many papers, including research on lung cancer [10 - 13], chronic obstructive pulmonary disease [14], metabolic disorders [15], oxidative stress [16], asthma [17], helicobacter pylori infection [18], diabetes [19, 20] and others. An average breath sample contains around 200 VOCs [9]. The concentrations of biomarkers in human breath are typically in the range of several ppt (parts per trillion) to several hundred ppb (parts per billion). Due to this, the portable devices for breath analysis have to detect biomarkers in such concentration range. Commercially-available gas sensors are under development for measuring samples at several tens parts per million (ppm). Furthermore, they have a lower selectivity for compositions of a few VOCs in a gas sample. A cheap and very effective method of decreasing the limit of detection and improving selectivity is the utilization of gas preconcentrators. Conventional preconcentrators are usually glass or stainless steel tubes filled with an adsorbent material. Similar solutions are also used in breath analysis [21, 22]. However, these structures have large lateral dimensions and they consume too much power to be used in portable devices.

The paper describes micropreconcentrator structures as a solution that overcomes these limitations. The micropreconcentrator designed by the author uses silicon micromachining technology and silicon as a base material. The channel is embedded inside the structure. The channel width of the micropreconcentrator is 300 and 350 μm. The Pt heater was positioned at the bottom of the structure and covered by a dielectric layer with the exception of the pads. In order to seal the channel from the top, glass anodic bonding is used. The main advantage of this is that it provides full control over the process of filling the spiral-shaped channel with adsorbent grains. Micropreconcentrators are well known in silicon-glass technology [23-28]. Bassam *et al* presented a MEMS-based multi-inlet/outlet preconcentrator coated with polymer adsorbents using inkjet printing [29]. The concentrator factor (CF) was in the 15 - 32 range for a single inlet/outlet port and around 1000 for multi-port design for pure nonane. Camara *et al* presented a micro gas preconcentrator with improved performance for pollution monitoring and detection of explosives. The authors used Tenax-TA as the adsorbent material, and they obtained a CF of around 23 (at exposure time of 45 min) for nitrobenzene (initial concentration of 1 ppm) [30]. Later, the same group presented a micro gas preconcentrator in porous silicon for benzene preconcentration [31]. The "practical" concentration factor was around 55 for pure benzene, and it was largely dependent on the preconcentrator's external parameters such as the detection system (at 5 min adsorption time and 250 ppb initial concentration). Ivanov *et al* presented a silicon micropreconcentrator for detecting benzene [32]. The obtained concentration factors were between 5.28 and 40.25 for different flows and exposure times to benzene.

A literature review highlighted the efforts to develop miniaturized preconcentrators for assessing lower detection levels for a single gas, mainly for benzene. There are very few papers presenting full investigation results on preconcentration levels of diabetes biomarkers. This paper presents the obtained concentration factor for a single gas (acetone, propane, ethanol or ethylbenzene), as well as for a mixture of diabetes biomarkers.

1.1 Diabetes biomarkers in exhaled breath

Previously, the author has focused on acetone [33], since patients with diabetes tend to have higher acetone levels in their breath than healthy people. Exhaled acetone levels are usually around 300-900 ppb for healthy subjects and over 3000 ppb for patients with diabetes [34]. Analysis of acetone in breath has been used as a supplementary diagnostic tool for diabetes. However, analysis of the exhaled acetone is insufficient to control glucose levels in diabetes. Galasetti *et al* reported results of their studies into plasma glucose [35]. Eight patients with type 1 diabetes (T1DM) and 17 healthy control patients were investigated. Two groups of four gases (cluster A: acetone, methyl nitrate, ethanol, ethylbenzene; cluster B: 2-pentyl nitrate, propane, methanol, acetone) were used as covariance to their models. The exhaled ethanol levels were between 9.6 and 45.0 ppb, acetone 280 - 364 ppb, methyl nitrate 5 - 216 ppb, and ethylbenzene 46 - 434 ppt. This 4-gas model works as a method of breath-based glucose detection with a mean correlation coefficient of 0.91 (R = 0.70 - 0.98) compared to standard glucose measurements [35].

Blood ethanol measurements are very common. "Haziness" (blurred vision) is defined when blood ethanol falls in the 0.5-1.0 g/l range, which corresponds to 130-260 ppm in breath. In higher doses ("inebriation"), the effects of alcohol on the brain contribute to the loss of balance and coordination, loss of the ability to judge distance and height as well as dizziness. For "slight inebriation" (1.0-1.5 g/l) and "inebriation" (1.5-2.5 g/l), breath equivalents are 260-390 ppm and 390-650 ppm, respectively [36].

The presence of propane in breath is not fully explained. M. Barker *et al* measured exhaled VOCs and

ambient air from patients who suffer from cystic fibrosis and controls. Results show that the exhaled propane concentration is the same for both groups (1.95 ppb), when background propane concentration was approx. 1.38 ppb [37]. Rudnicka *et al* investigated patients with lung cancer. The exhaled propane was between 3.45 ppb and 5.96 ppb for healthy subjects and 3.19 ppb - 9.74 ppb for patients with lung cancer [12].

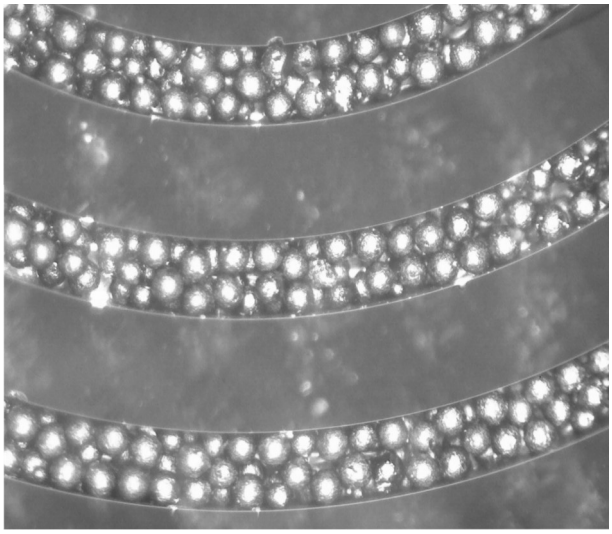
In [38], the authors report that 80% of ethylbenzene and xylenes are metabolized by hepatic enzymes in the human body. In this case, the exhaled ethylbenzene concentrations are lower than in inhaled air. On the other hand, some metabolic changes can modify the inhaled/exhaled ratio [2]. In [39], the authors measured exhaled ethylbenzene in the 46 ppt - 434 ppt range and methyl nitrate in the 5 ppt - 216 ppt range for hyperglycaemia. Achieving such low concentrations of VOCs is one of the most difficult stages of the preconcentration measurements.

2 Experimental

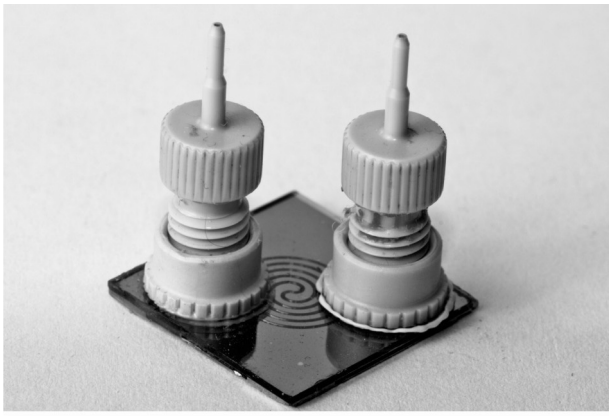
2.1 Basic limitations in micropreconcentrator fabrication

The microchannel shape and surface roughness are critical parameters for micropreconcentrators filled with adsorbent material. Due to this fact the fabrication process of micropreconcentrators was based on deep reactive ion etching (DRIE) of silicon substrate and the anodic bonding process. The microchannels were etched using the Bosch process, with an SiO_2 layer used as a masking material for the process. The manufacturing details was reported in [33]. The micropreconcentrators were fabricated with two microchannel dimensions: 300 µm x 300 µm x 120 mm, and 350 µm x 350 µm x 120 mm. The microchannel volumes are 1.08 μm^3 and 1.47 μm^3, respectively. The approximate adsorbent weight in the micropreconcentrator is 2.59 µg ± 0.8 µg. The channel width and depth were selected to prevent clogging of the adsorbent material inside the channel (Fig.1a.) However, some defects appeared during the fabrication process. For this reason, a few structures had a channel that could not be filled. Before filling the micropreconcentrator with the adsorbent material, the channel was examined using an optical microscope.

In recently reported structures, the gas inlet/outlet ports were placed on the edge of the structures. In the proposed solution, the gas ports are made with a glass cover. The author has investigated gas ports with a differently sized diameter. A filled micropreconcentrator with a NanoPort (NanoPort N-131, IDEX, Health & Science LCC, WA, USA) is presented in Fig.1b.



a) Optical image of the channel filled with Carboxen-1018

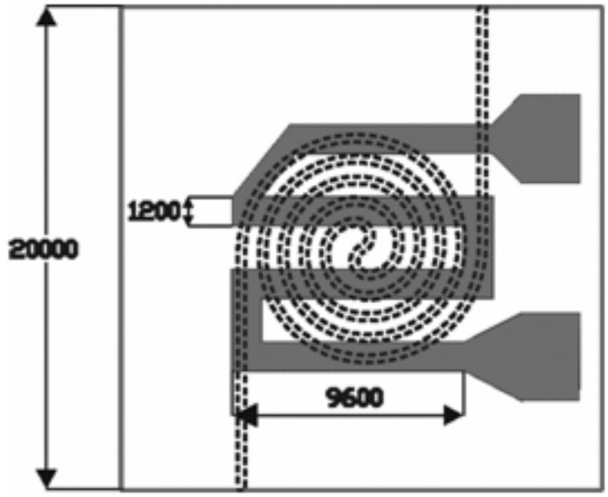


b) micropreconcentrator with assembled NanoPorts

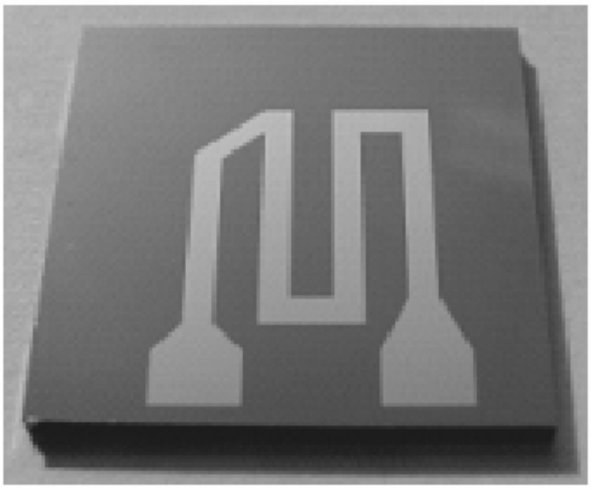
Figure 1: The micropreconcentrator filled with Carboxen-1018 and gas inlet/outlet ports.

2.2 Thermal and Electrical Measurements

As already mentioned, the micropreconcentrator is based on thermal desorption. Desorption temperature is dependent on the type of adsorbent material. The main goal is to achieve this temperature as fast as possible and then to stabilize it during the desorption process. Moreover, temperature distribution inside the channel needs to be uniform. The microheater was deposited to cover the entire working area of the microchannel (Fig.2). The nominal resistance was 40Ω ± 2Ω. The desorption temperature was set to 220°C; this was achieved after approx. 35 s (with a 10 W power supply) when gas was flowing through the microchannel (25 ml/min). For the purpose of controlling the micropreconcentrator temperature a Temperature Resistance Coefficient (TCR) of the Pt heater paste was measured. The value of TCR is 2026 ppm/°C.



(a)



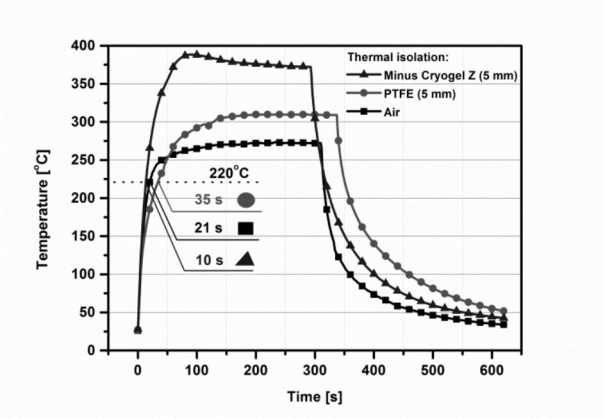
(b)

Figure 2: a) heater topology with dimensions, b) the micropreconcentrator - view of the heater side.

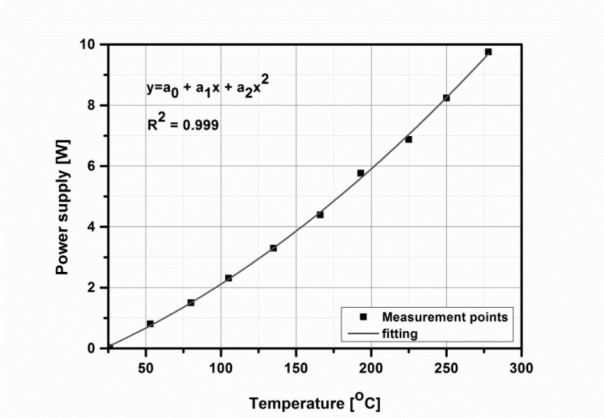
The desorption can be improved if the micropreconcentrator is placed in isolation. Using the Minus Cryogel Z material (Aerogels Poland Nanotechnology) with a very low thermal conductivity (0.0014 W/mK), the desorption temperature is achieved after approx. 10 s with a 7 W power supply (Fig.3a). To reduce power consumption the lateral dimensions have to be reduced. New micropreconcentrator concept is still under investigation. The power consumption vs. temperature was presented on Fig. 3b.

2.3 Preconcentration Process

Before taking the measurements, the micropreconcentrators are conditioned under specific parameters. The author used a typical time - temperature profile for adsorbent made with CMS (Carbon Molecular Sieve). To start with, the temperature was around 100°C for at least 30 minutes. Then, it was increased to 200°C and



(a)



(b)

Figure 3: a) temperature changes over time for different thermal isolation, b) power supply vs. temperature for micropreconcentrator with Minus Cryogel Z isolation

300°C for 1h, respectively. At the end, the temperature was set to 350°C for around 30 minutes. The author used nitrogen (6N) as the carrier gas. The author previously investigated adsorbent materials from the Carbon Adsorbent Sampler Kit (Sigma-Aldrich, St. Louis, MO 63178, USA) which contains eight different adsorbents. On the basis of the obtained results and data provided by the company, Carboxen-1018 was selected as a promising material for breath analysis. During the experiment, the author used four gases with certified concentrations: acetone (80 ppm and 800 ppb), ethanol (500 ppm), propane (1000 ppm), and ethylbenzene (100 ppb). A schematic view of the measurement system is presented in Fig 4. The measurement system was built using a Drechsler gas washing bottle and a 6-port electrically-actuated microvalve. Five gas lines were connected to the bottle. Mass flow controllers (MKS Instruments, MA, USA) were used to control the flow rate, while synthetic air was used to obtain lower concentrations of the investigated biomarkers. The gas mixture flow rate was set to 25 ml/min (same as the car-

rier gas). The maximum obtained value was around 28 ml/min. This was due to several factors, such as the microchannel being completely filled with adsorbent material (Fig.1a), and the hole diameter in the glass cover being too small (100 μm).

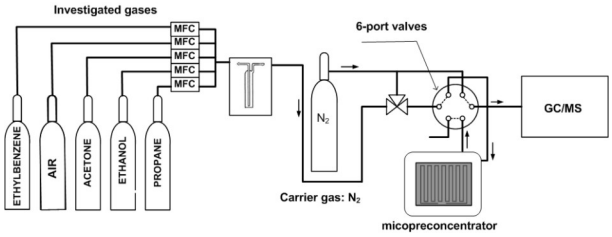


Figure 4: Gas preconcentration measurement system

Micropreconcentrator efficiency is measured using concentrator factors. The concentration factor is determined by (1):

$$CF = \frac{V_{sample}}{V_{desorbed}} = \frac{V_{sample}}{W_h \times u} \quad (1)$$

where: V_{sample} - sampled volume, $V_{desorbed}$ - desorbed volume, W_h - width of injection band (min), u - desorption flow rate (ml/min) [40]. According to Poiseuille's equation flow rate in preconcentrator could be determined by:

$$u = \frac{dV}{dt} = v\pi r^4 = \frac{\pi r^4 \Delta P}{8\eta L} \quad (2)$$

where: u - volumetric flow rate, V - volume (m^3), t - time (s) , v is mean fluid/gas velocity along the length of the tube (m/s), r is the internal radius of the tube (m), ΔP is the pressure difference between the two ends (Pa), η is the dynamic fluid/gas viscosity (Pa·s), L is the total length of the tube in the x direction (m). The Poiseuille's law corresponds to Ohm's law for electrical circuits, where volumetric flow rate is analogous to the current and pressure drop is analogous to the voltage. In this case resistance is:

$$R = \frac{8\eta L}{\pi r^4} \quad (3)$$

Equation (3) describes resistance in the tube, where resistance is inversely proportional to the fourth power of the radius. Referring to equations (1), (2) and (3) we can pre-calculate concentration factor in designed preconcentrator structures. Unfortunately theoretical calculations usually are different than experimental results. The difference is correlated with compressible nature of some gases and with non-laminar flow through the preconcentrator channel. Theoretical calculations should be performed before the experiment in order to predict what could be expected.

The experiments have four stages: pre-purge, adsorption, purge, and desorption; each takes a specific length of time. The pre-purge stage was performed for at least 10 minutes under carrier gas to clean gas line connections and stabilize the pressure in the reference analyzing setup (GC/MS). The author used an SRI-310 GC with an AB-Plot Q capillary column and a MS Hiden HPR-20 system with high sensitivity (5 ppb for mass up to 510 amu).

The adsorption time was adjusted during the measurements to calculate the CF vs. adsorption time. After adsorption, the second purge step was set to 1 minute and desorption for at least 3 minutes. After 3 minutes, the investigated gases were fully desorbed (Fig. 5.)

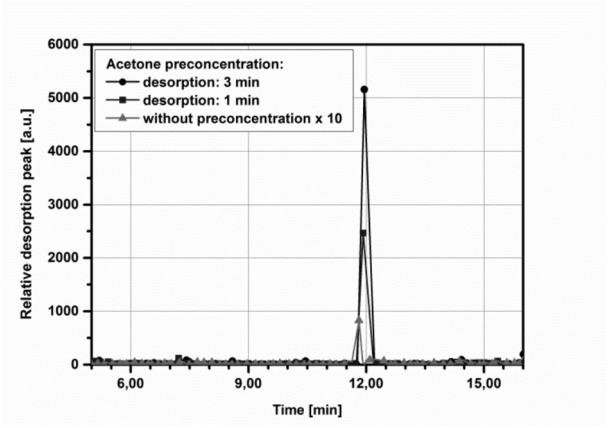


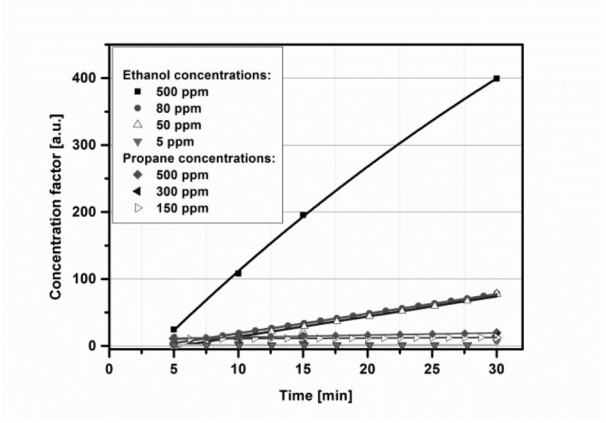
Figure 5: Desorption peak for different desorption time at constant flow rate set to 25 ml/min

The concentration factor was obtained for gas mixtures with various VOCs concentrations. Taking into account all the literature reports, the author measured the concentration factor for a single biomarkers, as well as for a mixture of diabetes biomarkers. Before conducting clinical studied, it is necessary to perform a number of basic investigations in the laboratory. It is essential to achieve repeatable measurement results for a wide range of concentrations.

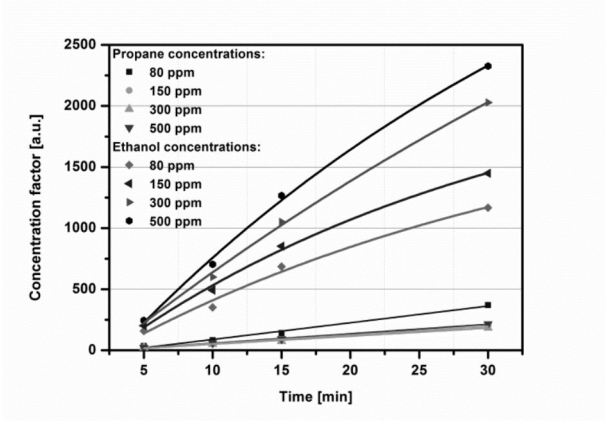
3 Results

To start with, the author measured concentration factors for different concentrations of ethanol and propane separately. The results are presented in Fig. 6a. The maximum value of CF (400) was obtained for an initial concentration of ethanol of 500 ppm and 30 min adsorption time. The CF for 500 ppm, 50 ppm and 5 ppm of ethanol was 400, 77.8 and 6.5, respectively. The maximum CF for propane was 19.5 at an initial concentration of 500 ppm and 30 min adsorption time. Carboxen-1018 is useful for adsorption/desorption of

small analytes, such as C_2 - C_3 hydrocarbons. However, it is less well suited to propane (C_3H_8) and ethylbenzene (C_8H_{10}), even at initial concentrations in the ppm range. In the next measurements, concentration factors were obtained for a mixture of acetone (80 ppm) with ethanol and propane at different concentrations. The results are presented in Fig.6b. The highest CF value was obtained when acetone was mixed with 500 ppm ethanol, reaching approx. 2325 for 30 min adsorption time. The CF for acetone with propane at 500 ppm was approx. 215 at the same conditions.



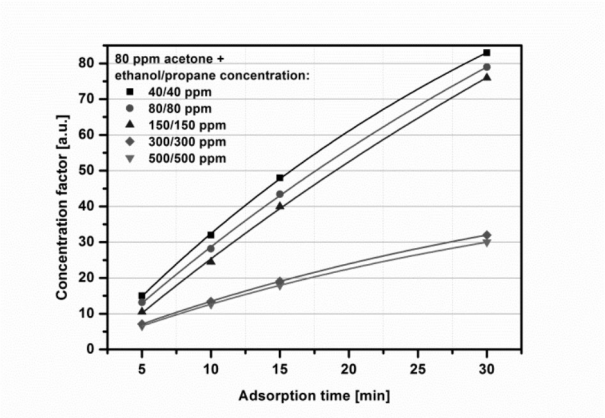
(a)



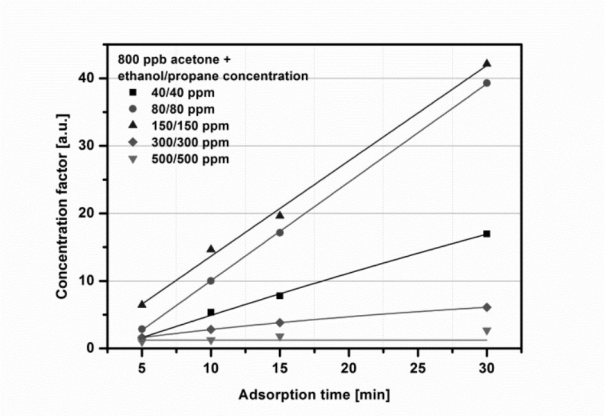
(b)

Figure 6: Concentration factor vs. adsorption time for the channel filled with Carboxen-1018 and different concentrations of: a) propane and ethanol, b) propane and acetone, ethanol and acetone

The next step in the laboratory experiments was measuring CF for a range of mixtures of acetone, ethanol and propane. The acetone concentration was set to 80 ppm and 800 ppb, and the ethanol/propane concentration was varied during the experiments. Concentration factors for such mixtures of gases vs. adsorption time are presented in Fig.7a. and Fig.7b, respectively.



(a)



(b)

Figure7: Concentration factor vs. adsorption time for the channel filled with Carboxen-1018 and: a) 80 ppm acetone, b) 800 ppb acetone with different ethanol/propane concentrations,

The CF_{MAX} for different combinations of acetone and other diabetes biomarkers (at 5 and 30 min adsorption time) are presented in table 1.

Table 1: Maximum Concentration Factors obtained for various compositions of diabetes biomarkers

Diabetes biomarker name	Initial concentration of VOCs	Adsorption time [min]	CFMAX
Propane	500 ppm	5	11.70
		30	19.50
Acetone	800 ppb	5	3.77
		30	19.53
	80 ppm	5	360.00
		30	2831.00
Ethanol	500 ppm	5	24.60
		30	400.00
Ethylbenzene	100 ppb	5	1.00
		30	1.00

Ethanol + Acetone	500ppm + 80 ppm	5	244.45
		30	2324.38
	500 ppm + 800 ppb	5	1.30
		30	2.00
Propane + Acetone	80 ppm + 80 ppm	5	35.55
		30	376.63
	80 ppm + 800 ppb	5	20.00
		30	66.00
Ethanol + Propane + Acetone	40 ppm + 40 ppm + 80 ppm	5	15.00
		30	83.02
	150 ppm + 150 ppm + 800 ppb	5	6.42
		30	42.14
Ethylbenzene + Ethanol	100 ppb + 500 ppm	5	1.70
		30	1.95
Ethylbenzene + Propane	100 ppb + 500 ppm	5	1
		30	1.08
Ethylbenzene + Acetone	100 ppb + 80 ppm	5	18.30
		30	53.5
	100 ppb + 800 ppb	5	1
		30	1.12
Ethylbenzene + Acetone + Ethanol	100 ppb + 80 ppm + 5 ppm	5	12.25
		30	30.53
	100 ppb + 800 ppb + 5 ppm	5	1
		30	1.05
Ethylbenzene + Acetone + Ethanol + Propane	100 ppb + 80 ppm + 10 ppm	5	7.30
		30	25.12
	100 ppb + 800 ppb + 10 ppm	5	1.05
		30	2.00
Ethylbenzene + Acetone + Ethanol + Propane	100 ppb + 80 ppm + 5 ppm + 5 ppm	5	11.32
		30	30.00
	100 ppb + 800 ppb + 5 ppm + 5 ppm	5	1.50
		30	1.75

The final composition of gases consists of ethylbenzene, acetone, ethanol and propane. The ethanol concentration was changed, and acetone, ethylbenzene and propane concentrations were set to values that had previously been calibrated and certificated. The concentration factor results for this experiment are presented in Fig.8.

As it is shown in Fig.8. there is a linear correlation between concentration factor for the acetone and ethanol concentration in the composition of acetone (80 ppm), ethylbenzene (100 ppb), propane (5 ppm) and ethanol (5 - 500 ppm). The highest concentration factor for acetone is obtained for lower ethanol concentration. The measurements results confirmed, that there is evidently a significant lower adsorption capacity of

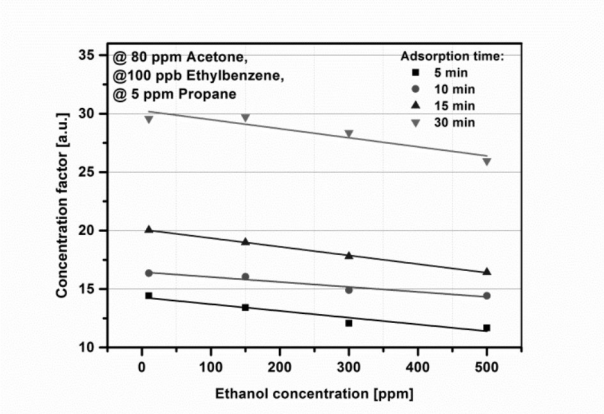


Figure 8: Concentration factor vs. ethanol concentration for the channel filled with Carboxen-1018 and 80 ppm acetone, 5 ppm propane and 100 ppb ethylbenzene.

the acetone in the present of interfering gases such as: propane and ethylbenzene. Due to fact, that Carboxen-1018 possess a large percentage of narrow (60-70 nm) micropores, is useful for the adsorption/desorption of small analytes, such as: C_2-C_3 hydrocarbons. The obtained concentration factor for acetone (30 min adsorption) was in the range 25-30 for different ethanol concentrations. To compare, the concentration factor was approx. 2831, 2324, 376, 53 for pure acetone, acetone with ethanol, acetone with propane and acetone with ethylbenzene, respectively (Table 1).

4 Prospectives

In the experiments, the GC/MS analysis setup was used only as the reference analyzer. In table 1 the concentration factors for different diabetes biomarkers concentration and adsorption time were presented. The micropreconcentrator with CFs >10 is suitable to use it with metal oxide (MOX) sensor array. A gas sensor array will be used in the final application. The author is currently developing arrays based on MOX sensors with a higher sensitivity and selectivity for diabetes biomarkers [41, 42]. MOX sensors are commonly used in many industrial and medical applications, including breath analysis [43]. However, the market still lacks sensors for the detection of diabetes biomarkers. Promising results were obtained by M. Righettoni *et al.* They proposed an acetone detector based on Si-doped WO_3 nanoparticles made in the gas phase. The acetone sensor responded to the 3 ppm acetone concentration [44]. Due to this, the preconcentration remains a useful method of detecting exhaled acetone and other diabetes biomarkers. The concentration factors can be improved further by choosing preconcentration of two or three steps. Each step should to be dedicated

to concentrating different VOCs. Before commercialization the breakthrough time has to be determined. It can be done using the Wheeler-Jonas equation (4). It is the most widely used to estimate the breakthrough time of organic compounds on activated carbon:

$$t_b = \frac{W_e W_B}{C_0 Q} - \frac{\rho_B W_e}{k_v C_0} \ln\left(\frac{C_0 - C_x}{C_x}\right) \quad (4)$$

where: t_b is breakthrough time (min), W_e the equilibrium adsorption capacity (g/g), W_B is the bed mass (g), C_0 is the challenged concentration (g/l), C_x is the fraction of C_0 where breakthrough is measured (g/l), k_v is kinetic rate coefficient (1/min), ρ_B - density (g/cm^3), Q - gas flow rate (ml/min).

To apply this equation the two parameters, W_e and k_v, must be determined. Only W_e can be determined independently using some analytics method, i.e. gas chromatography or mass spectrometry. The k_v must be determined empirically. However, the W_e in most cases is determined from a series of breakthrough experiments [45]. Even a slight deviation between the calculated equilibrium adsorption capacity and the effective adsorption capacity required for (4) may cause a significant error into the estimated breakthrough time. The effect of such error is discussed in [46]. Due to this limitation the t_b is somewhat difficult to predict. First, k_v cannot be measured directly experimentally. It has to be calculated either from the breakthrough time or from breakthrough curves. Second, there are different concept regarding how it should be calculated from (4). Some concepts are summarized in a review in paper [47]. So far, the three models for predicting adsorption rate coefficient have been developed. A model proposed by Jonas [48], an alternative model suggested by Wood [49]. Third model has been proposed by Lodewyckx and Vasant [50]. The major limitation of cited models is that they are not based on a systematic investigation of the parameters that might influence on adsorption rate coefficient, such as: velocity, inlet concentration, adsorbent material properties (carbon properties) and volatile organic compounds properties.

In this work the author presents the results of systematic investigation on concentration factor obtained in micropreconcentrator filled with Carboxen-1018 and for various concentration of the diabetes biomarkers. Such experiments are necessary for better understanding the fundamental behavior of adsorbent material under selected VOCs exposure. In the presented results, the following fitting equation was used (5):

$$y = A_1 - A_2 \cdot \exp(-kt) \quad (5)$$

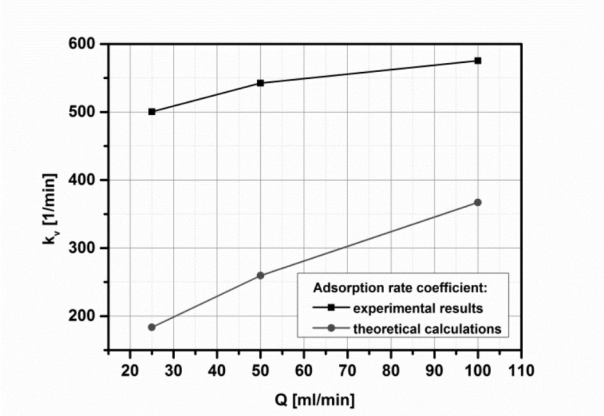
where: A_1, A_2, k - constant, t - adsorption time.

The experimental coefficient can be easily calculated from the fitting equation (5). Referring to equations (4) and (5) as well as data provided by the company we can pre-calculate adsorption rate coefficient in designed preconcentrator structures (6):

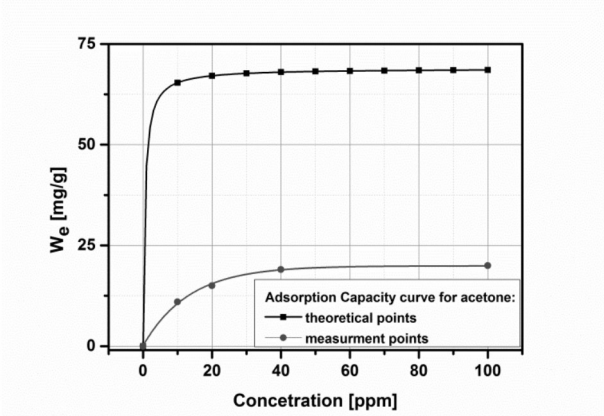
$$k_v = -\frac{\rho_B \cdot Q \cdot \ln(A_2)}{W_B} \quad (6)$$

where: W_B is the bed mass (g), ρ_B - density (g/cm^3), Q - gas flow rate (ml/min).

Fig.9a. shows the adsorption rate coefficient obtained from model proposed by Jonas [48] and from experimental results. Due to the fact that, k_v is a function of



(a)



(b)

Figure 9: a) Adsorption rate coefficient vs. gas flow rate calculated based on experimental results for micropreconcentrator filled with Carboxen-1018 and upon exposure to acetone as well as theoretical calculations from Jonas model, b) equilibrium adsorption capacity vs. concentration for acetone obtained from experimental results for micropreconcentrator filled with Carboxen-1018 and from theoretical calculations.

superficial velocity, microchannel geometry and particle shape/size, there are limits of the applicability of the estimated parameters. Thus, the k_v obtained from experimental results and mathematical calculations are not of the same order of magnitude. It is generally necessary to determine k_v and W_e empirically. The equilibrium adsorption capacity obtained from experimental results and theoretical calculations for acetone for micropreconcentrator filled with Carboxen-1018 are presented in Fig.9b. As it can be seen, for concentrations higher than 100 ppm the W_e for micropreconcentrator filled with Carboxen-1018 achieved a constant value.

The resulting data can then be used directly to estimate the breakthrough time as well as adsorbent mass, which would be required to efficiently preconcentrate acetone. However, the main aim is to estimated the breakthrough time for all of the examined vapors as well as to compare with those measured with humid air, which is still under investigations. The investigation results would be used to manufacture the micropreconcentrators with suitable geometrical dimensions. In other words, such results help to determine the microchannel geometry which provide suitable concentration factor for acetone and it can be used to preconcentrate acetone in breath.

5 Conclusions

Based on results reported by scientists, it can be assumed that a typical concentration of diabetes biomarkers in breath is a few hundred ppb. To analyze such concentrations using portable devices, it is necessary to use preconcentration methods. Exhaled breath contains many VOCs, although some would have been inhaled from ambient air. It needs to be analyzed before the experiment. In this paper the results obtained for the micropreconcentrator using silicon-glass technology filled with Carboxen-1018 are presented. The obtained concentration factor was approx. 2831 for 30 min adsorption time. Blanco *et al* [51] present the preconcentrator for benzene vapours. The obtained concentration factor was less than 400 for different adsorbent materials and different flow rates at 30 min adsorption time. Dow and Lang [52] present a micromachined preconcentrator for ethylene monitoring system. The obtained concentration factor was in the range of 40 - 120 for different adsorption time and desorption flow rate. Tian *et al* [53] present a novel micropreconcentrator employing a laminar flow patterned heater for micro gas chromatography. The obtained concentration factor was approx. 118 for acetone after 30 min adsorption time. However, the concentration factor obtained for xylene was approx. 2015. The CF is highly dependent on adsorption time, gas flow and desorption temperature. The obtained CFs are sufficiently high to use fabricated devices in diabetes biomarker analysis. The micropreconcentrator with concentration factors higher than 10 can be used as a part of portable microsystem. The obtained CFs for a single diabetes biomarkers as well as for a mixture of diabetes biomarkers are quite good in comparison with other results presented in the Introduction part. A microsystem with three-step preconcentration and gas sensor array is currently under investigation. High humidity of breath also needs to be taken into account, as does the humidity of ambient air.

6 Acknowledgments

This work was supported by the NCN Preludium Grant UMO-2013/09/N/ST7/01232

7 References

1. Definition and diagnosis of diabetes mellitus and intermediate hyperglycaemia. (2006). *Report of a WHO/IDF consultation*, 1-50.
2. T. Minh, D. Blake, P. R. Galassetii. (2012). The clinical potential of exhaled breath analysis for diabetes mellitus. *Diabetes Research and Clinical Practice* 97, 195-205.
3. Standards of Medical Care in Diabetes - 2011. (2011). *Diabetes Care* 34, 11–61.
4. C. Tassopoulos, D. Barnett, and T.R. Fraser. (1969). Breath-Acetone and Blood-Sugar Measurements in Diabetes. *The Lancet*, 293(7609), 1282-1286.
5. Q. Zhang, P. Wang, J. Li, and X. Gao. (2000). Diagnosis of diabetes by image detection of breath using gas sensitive laps. *Biosensors and Bioelectronics*, 15(5-6), 249-256.
6. M. Philips, R. Cataneo, T. Cheema, J. Greenberg. (2004). Increased breath biomarkers of oxidative stress in diabetes mellitus. *Clinica Chimica Acta*, 344(1-2), 189-194.
7. A. Mashir, and R.A. Dweik, Exhaled breath analysis: The new interface between medicine and engineering. (2009). *Advanced Powder Technology* 20, 420-425.
8. D. Guo, D. Zhang, L. Zhang, and G. Lu. (2012). Non-invasive blood glucose monitoring for diabetes by means of breath signal analysis. *Sensors and Actuators B*, 173, 106-113.
9. M. Phillips, J. Herrera, S. Krishnan, M. Zain, J. Greenberg, and R. N. Cataneo. (1999). Variation in volatile organic compounds in the breath of nor-

mal humans. *Journal of Chromatography B*, 729, 75-88.
10. M. Phillips, K. Gleeson, J. M. B. Hughes, J. Greenberg, R. N. Cataneo, L. Baker, and W. P. McVay. (1999). Volatile organic compounds in breath as markers of lung cancer: a cross-sectional study. *The Lancet*, 353, 1930-1933.
11. D. Poli, et al. (2010). Determinaation of aldehydes in exhaled breath of patients with lung cancer by means of on-fiber-derivatisation SPME-GC/MS. *Journal of Chromatography B* 878, 2643-2654.
12. J. Rudnicka, T. Kowalkowski, T. Ligor, and B. Buszewski. (2011). Determination of volatile organic compounds as biomarkers of lung cancer by SPME-GC-TOF/MS and chemometrics. *Journal of Chromatography B*, 879, 3360-3366.
13. P. J. Mazzone. (2012). Exhaled breath volatile organic compound biomarkers in lung cancer. *Journal Breath Res*. 6, 027106-027114.
14. V. Bessa, et al. (2011). Detection of volatile organic compounds (VOCs) in exhaled breath of patients with chronic obstructive pulmonary disease (COPD) by ion mobility spectrometry. *Int. J. Ion. Mob. Spec.*, 14, 7-13.
15. F. Di Francesco, R. Fuoco, M.G. Trivella, A. Ceccarini. (2005). Breath analysis: trends in techniques and clinical applications. *Microchemical Journal* 79, 405-410.
16. T. H. Risby, S. S. Sehnert. (1999). Clinical Application of Breath Biomarkers of Oxidative Stress Status, *Free Radical Biology & Medicine*, 27, 1182-1192.
17. K. Kostikas, A. Papaioannou, K. Tanou, P. Giouleka, A. Koutsokera, M. Minas, S. Papiris, K. Gourgoulianis, D.Taylor, S.Loukides. (2011). Exhaled NO and exhaled breath condensate pH in the evaluation of asthma control. *Respiratory Medicine,*105, 526-532.
18. F. Gomollón, J.A. Ducons, S. Santolaria, I. L. Omiste, R. Guirao, M. Ferrero M. Montoro. (2003). Breath test is very reliable for diagnosis of Helicobacter pylori infection in real clinical practice. *Digestive and Liver Disease*, 35, 612-618.
19. Ch. Wang, A. Mbi, M. Shepherd. (2010). A Study on Breath Acetone in Diabetic Patients Using a Cavity Ringdown Breath Analyzers: Exploring Correlations of Breath Acetone With Blood Glucose and Glycohemoglobin A1C. *IEEE Sensors Journal*, 10, 54-63.
20. C. Turner, Ch. Walton, S. Hoashi, M. Evans. (2009). Breath acetone concentration decreases with blood glucose concentration in type I diabetes mellitus patients during hypoglycaemic clamps. *Journal Breath Res.,* 3, 0466004-0466010.
21. T. Nakamoto, E. Sumitimo. (2003). Study of robust odor sensing system with auto-sensitivity control. *Sensors and Actuators B,* 89, 285-291.
22. K. Song, S.-K. Lee. (2007). Development of a compact sample pre-concentration system for the detection of a trace amount of volatile organic compounds (VOCs). *Sensors and Actuators B*, 125, 173-179.
23. G. Serrano, T. Sukaew, E.T. Zellers. (2013). Hybrid preconcentrator/focuser module for determinations of explosive marker compounds with a micro-scale gas chromatograph. *Journal of Chromatography A,* 1279, 76-85.
24. W. Groves, E. Zellers, G. Frye. (1998). Analyzing organic vapors in exhaled breath using a surface acoustic wave sensor array with preconcentration: Selection and characterization of the preconcentrator adsorbent. *Analytica Chimica Acta* 371, 131-143.
25. S. Cho, Y. Kim, G. Heo, S.-M. Shin. (2006). Two-step preconcentration for analysis of exhaled gas of human breath with electronic nose. *Sensors and Actuators B*, 117, 50-57.
26. A. Dow, W. Lang. (2012). Design and fabrication of a micropreconcentrator focuser for sensitivity enhancement of chemical sensing systems. *IEEE Sensors Journal*, 12, 2528–2534.
27. M. Martin, et al. (2010). Performance of stacked, flow-through micropreconcentrators for portable trace detection. *International Journal for Ion Mobility Spectrometry,* 13, 109–119.
28. M. Kim, S. Mitra. (2003). A microfabricated micropreconcentrator for sensors and gas chromatography. *Journal of Chromatography A*, 996, 1–11.
29. A. Bassam, et al. (2008). MEMS-based multi-inlet/outlet preconcentrator coated by inkjet printing of polymer adsorbents. *Sensors and Actuators B,* 133, 24-42.
30. E. Camara, et al. (2011). A micro gas preconcentrator with improved performance for pollution monitoring and explosive detection. *Analytica Chimica Acta,* 688, 175-182.
31. E. Camara, et al. (2010). Micro gas preconcentrator in porous silicon filled with a carbon adsrobent. *Sensors and Actuators B,* 148, 610-619.
32. P. Ivanov, et al. (2007). Improvement of the gas sensor response via silicon μ-preconcentrator. *Sensors and Actuators B*,127, 288-294.
33. A. Rydosz, W. Maziarz, T. Pisarkiewicz, K. Domański, P. Grabiec. (2012). A gas micropreconcentrator for low level acetone measurements. *Microelectronics Reliability,* 52, 2640-2646.
34. N. Teshima, J Li., K. Toda, P. Dasgupta. (2005). Determination of acetone in b reath. *Analytica Chemica Acta,* 545,189-99.
35. J. Lee, et al. (2009). Improved predictive models for plasma glucose estimation from multi-linear regression analysis of exhaled volatile organic

compounds. *Journal of Applied Physiology*, 107(1), 155-160.
36. K. Mitsubayashi, et al. (2005). Bio-sniffer stics for breath analysis after drinking. *Sensors and Actuators B*, 108, 660-664.
37. M. Barker, et al. (2006). Volatile organic compounds in the exhaled breath of young patients with cystic fibrosis. *European Respiratory Journal*, 27(5), 929-936.
38. I. Astrand, J. Engstroem, P. Ovrum. (1978). Exposure to xylene and ethylbenzene. I. Uptake, distribution and elimination in man, *Scandinavian Journal of Work, Environment & Health*, 4(3), 185-194.
39. J. Lee et al. (2009). Improved predictive models for plasma glucose estimation from multi-linear regression analysis of exhaled volatile organic compounds. *Journal of Applied Physiology,* 170, 155-160.
40. J. Namiesnik. (1988). Methods of preconcentration of vapours of organic polutants from atmosphere. *Talanta,* 35(7), 567-587.
41. T. Pisarkiewicz, T. Kenig, A. Rydosz, W. Maziarz. (2011). Solution growth of ZnO sub-micro rods enhanced by electric field. *Bulletin of the Polish Academy of Sciences - Technical Sciences,* 59, 425-428.
42. W. Maziarz, A. Rydosz, T. Pisarkiewicz, K. Domański, P. Grabiec. (2012). Gas-sensitive properties of ZnO nanorods/nanowires obtained by electrodeposition and electrospinning methods. *Procedia Engineering,* 47, 841-844.
43. J. Gardner, E. Hines, F. Molinier, P. Barlett, T. Mottram. (1999). Prediction of health of dairy cattle from breath samples using neural network with parametric model of dynamic response of array of semiconducting gas sensors, *IEE Proc.-Sci. Meas. Technol*., 146(2), 102-106.
44. M. Righettoni, A. Tricoli, S.E. Pratsinis. (2010). Si:WO_3 Sensors for Highly Selective Detection of Acetone for Easy Diagnosis of Diabetes by Breath Analysis. *Analytical Chemistry*, 82(9), 3581-3587.
45. P. Lodewyckx, G.O. Wood, S.K. Ryu. (2004). The Wheeler–Jonas equation: a versatile tool for the prediction of carbon bed breakthrough times. *Carbon* 42, 1351-355.
46. J. Wu. (2004). Modeling adsorption of organic compounds on activated carbon, Ph.D. dissertation, Umea Universitet, Sweden.
47. G.O. Wood. (2002). A review of the effects of covapors on adsorption rate coefficient of organic vapors adsorbed onto activated carbon from flowing gases. *Carbon* 40, 685-694.
48. L. Jonas, J. Rehrmann. (1974). The rate of gas adsorption by activated carbon. *Carbon* 12, 95-101.
49. G. Wood, J. Stampfer. (1993). Adsorption rate coefficient for gases and vapors on activated carbons, *Carbon* 31, 195-200.
50. P. Lodewyckx, E. Vansant. (2000). Estimating the overall mass transfer coefficient k_v of the Wheeler-Jonas equation: a new and simple model. *American Industrial Hygiene Association Journal,* 61, 501-505.
51. F. Blanco, X. Vilanova, V. Fierro, A. Celzard. P. Ivanov, E. Llobet, N. Canellas, J. L. Ramirez, X. Correig. (2008). Fabrication and characterisation of microporous activated carbon-based pre-concentrators for benzene vapours. *Sensors and Actuators B,* 132, 90-98.
52. A. B. A. Dow, W. Lang. (2010). A micromachined preconcentrator for ethylene monitoring system. *Sensors and Actuators B*, 151, 304-307.
53. W.-C. Tian, T.H. Wu, C.-J. Lu, W.R. Chen, H. J. Sheen. (2012). A novel micropreconcentrator employing a laminar flow patterned heater for micro gas chromatogrpahy. *Journal of Micromechanical Microengineering,* 22, 065014-065022

Arrived: 20. 12. 2013
Accepted: 18. 03. 2014

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 44, No. 2 (2014), 137 – 141

A 4th Order Differential G_m-C Band-Pass Filter Using Improved Floating Current Source

Fırat Kaçar[1], Arsen A.M. Shakir[2], Yasin Özçelep[1]

[1]Dept. of Electrical and Electronics Engineering, University of Istanbul, Istanbul, Turkey
[2]Dept. of Mechanical Engineering, Kirkuk University, Kirkuk, Iraq

Abstract: Gm-C filters are the most popular technique used in implementing integrated continuous-time filters. In the study, we proposed a 4th order differential Gm-C band-pass filter using improved floating current sources. The improved current source structure is simple and includes fewer transistors. This provides an effective use of the chip area and brings simplicity to the design of circuits. Thus it reduces the investment cost. The proposed filter structure does not contain the resistor which is very important for integration. All capacitors in proposed filter are grounded which reduces the parasitic effects. The proposed filter is simulated using CMOS TSMC 0.18µm technology. Simulation results are given to confirm the theoretical analysis.

Keywords: Analogue filter, analogue signal processing, floating current source, MOS integrated circuits

Diferencialen G_m-C pasovno prehoden filter četrtega reda z uporabo izboljšanega plavajočega tokovnega vira

Izvleček: Pri uporabi integriranih časovno neomejenih filtrov se najbolj uporablja tehnika Gm-C filtrov. V članku predlagamo diferencialen Gm-C pasovno prehoden filter četrtega reda z uporabo izboljšanega plavajočega tokovnega vira. Struktura izboljšanega tokovnega vira je enostavna in uporablja manj tranzistorjev, kar prinaša efektivno izrabo prostora in enostavnost vezja. Istočasno tudi znižuje stroške. Predlagani filter ne vsebuje upora, ki je potreben za integracijo. Vsi kondenzatorji so ozemljeni, kar zmanjšuje parazitne vplive. Filter je simuliran v CMOS TSMC 0.18 µm tehnologiji. Podani so simulacijski rezultati, ki potrjujejo teorijo.

Ključne besede: analogni filter, analogna obdelava signalov, plavajoči tokovni vir, MOS integrirana vezja

** Corresponding Author's e-mail: ycelep@istanbul.edu.tr*

1 Introduction

A continuous time filter has been widely applied in video signal processing, hard disk drive, communication integrated circuit, CDMA, ultra-wideband wireless access technology, and etc. [1]. G_m-C filters are the most popular technique used in implementing integrated continuous-time filters [2]. Research and development in the microelectronic technology enable possibility to design filters with less number of active and passive components. It also brings versatility and simplicity to the design of circuits and systems while reducing the investment cost[3].

Mostly the desired radio frequency signal is narrowband and therefore most of the intermediate frequencies in a superheterodyne (superhet) receiver designed for applications are also narrowband. As a result of this important fact, band pass filters are very important building blocks in modern RF communication systems. Figure 1 shows the block diagram of a typical multistep superhet receiver with a digital back-end [4]. As the figure shows, a sequence of filter operations is used to convert the desired signal from radio frequency (RF), typically in the VHF (30 MHz to 300 MHz) range, down to one or more intermediate frequencies (IFs) and finally down to baseband, where the signal is digitized by an ADC [4].

The studies about the 4th order filters have been reported in the literature [1-2,5-9]. The comparison of 4th order filter circuits in terms of including active devices and passive components are shown in Table 1.

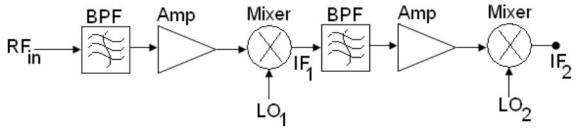


Figure 1: A typical superheterodyne receiver [4]

This paper proposes 4th order differential G_m-C band-pass filter using improved floating current sources. Improved floating current sources performance is better than the floating current sources at low frequencies, because of high output resistance. Compared with the studies that are shown in Table 1, the improved current source structure is simple and includes fewer transistors. Thus, we can use the chip area more effective and this brings simplicity to the design of circuits and reduces investment costs.

Table 1: The 4th order filter structures reported in literature

Active Device	Active Device Number	Passive Component Number	Reference
DVCC	4	8	[5]
OTA	6,8,8	4,4,8	[6-8]
OPAMP	2	20	[9]
Current Mirror	4	4	[1]
G_m cells	8	4	[2]

2 Proposed 4th order band-pass filter structure

The improved floating current source has very simple structure as shown in Figure 2. Having two different G_m and its frequent use in recent studies make the floating current source useful. Its G_m is electronically adjustable using bias current as OTA structures. Floating current source operation is similar to OTA. But, there is only one G_m for OTA and two different G_ms in floating current source. The output resistance of the improved floating current source is higher than the floating current source which is proposed by Arbel and Goldminz [10]. M5, M6, M7 and M8 transistors are added to the conventional floating current source to get high output resistance values as shown in Figure 2. The high output resistance is a necessity in current-mode structures and therefore the improved floating current source is preferred according to conventional improved floating current source. High output resistance provides better results at low frequency region. Output current of the improved floating current source is calculated by multiplying the voltage difference between P and N terminals with G_m. The G_m for P terminal is $(g_3/g_4)/2$ and the G_m of the n terminal is $-(g_1+g_2)/2$. The capacitors are connected to the structure without using resistance and this connection provides the desired transfer function in filter and oscillator applications [11-12]. In this study, we proposed G_m-C filter application.

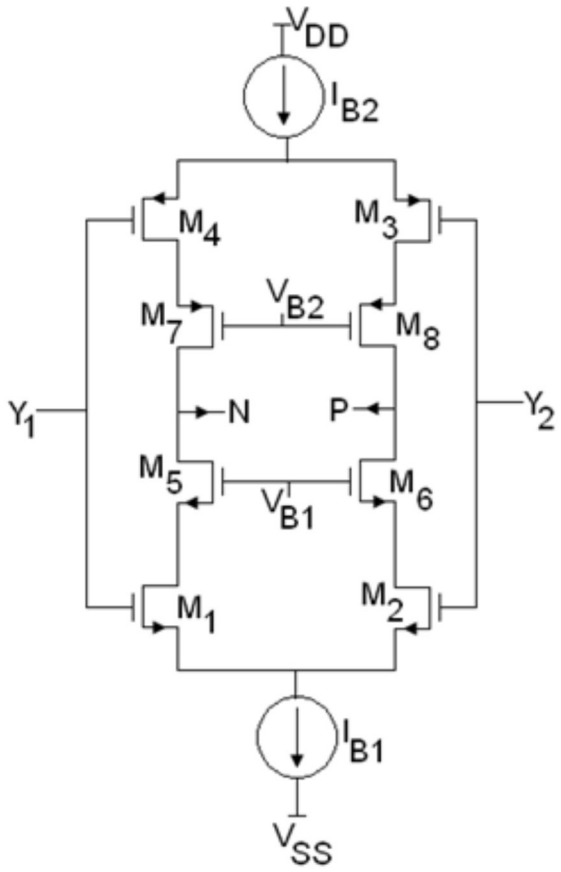


Figure 2: Schematic representation of improved floating current source [12]

W/L of transistors and DC values of the circuit are reported in Table 2 and Table 3, respectively. The functionality of the proposed circuit is demonstrated on a 4th order band pass ladder filter design which is illustrated in Figure 3 and the ladder filter component values are given in Table 4.

Table 2: Transistor dimensions

Transistors	W(μm)	L(μm)
M_1, M_2	18	0.18
M_3, M_4	72	0.18
M_5, M_6	27	0.18
M_7, M_8	90	0.18

Table 3: DC values of improved floating current source

Parameters	Value
V_{DD}, V_{SS}	±0.9V
I_{B1}, I_{B2}	300µA
V_{B1},V_{B2}	0.3V

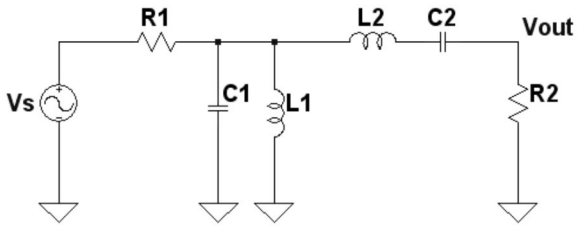


Figure 3: The LC Butterworth ladder filter

Table 4: Ladder filter component values

Component	Value
R1, R2	100Ω, 100Ω
C1, C2	225pF, 12.5pF
L1, L2	125nH, 2.251µH

The block diagram of the proposed 4th order G_m-C band-pass filter is presented in Figure 4. The proposed filter block diagram is the equivalent filter of the ladder filter in Figure 3 which consists of passive components. G_m-C filter component values and performance parameters are given in Table 5.

Table 5: G_m-c filter component values and performance parameters

Component	Value
$C_1=C_1'$, $C_2==C_2'$	225pF, 12.5pF
$C_{L1}=C_{L1}'=L_1.(G_m)^2$	0,87pF
$C_{L2}=C_{L2}'=L_2.(G_m)^2$	15,71 pF
Parameter	
$G_{m1}= G_{m3}= G_{m4}= G_{m5}= G_{m6}= G_{m7}= G_{m8}$	2.642mA/V
$G_{m2}= G_{m9}$	0.99mA/V

Transfer function of the filter is given in Equation (1).

$$H(s)=\frac{s\frac{G_{m1}}{C_1}}{s^2+sC_{L1}\frac{G_{m2}}{C_1}+\frac{G_{m3}\cdot G_{m4}}{C_1\cdot C_{L1}}}\cdot\frac{s\frac{G_{m6}}{C_2}}{s^2+sC_{L2}\frac{G_{m9}}{C_2}+\frac{G_{m7}\cdot G_{m8}}{C_2\cdot C_{L2}}} \quad (1)$$

Center frequency of the band pass filter is given in Equation (2).

$$\omega_0=\sqrt{\sqrt{\frac{G_{m3}\cdot G_{m4}}{C_1\cdot C_{L1}}\cdot\frac{G_{m7}\cdot G_{m8}}{C_2\cdot C_{L2}}}} \quad (2)$$

3 Simulations

We perform the simulations by using LTSPICE program with TSMC CMOS 0.18 µm process parameters. The performance parameters of improved floating current source used in simulations are presented in Table 6.

Table 6: Performance parameters of IFCS G_m structure

Parameter	Value
V_{DD}, V_{SS}	±0.9V
I_{B1}, I_{B2}	300µA
V_{B1},V_{B2}	0.3V
$G_{m1}= G_{m1}$	2.445mA/V
Parasitic capacitances at p, n terminals	0.3pF, 15.6fF
Input offset voltage	0
Power dissipation	0.54mW

The output currents at n and p terminals of improved floating current source against input voltage (V_{Y1}-V_{Y2}) are shown in Figure 5. The output currents changes between ±300µA.

Figure 6 clearly shows that the G_m of improved floating current source operates well at frequencies close to 100MHz.

The ladder circuit in Figure 3 and the proposed circuit in Figure 4 are simulated with using the component values in Table 4 and Table 5. Figure 7 illustrates

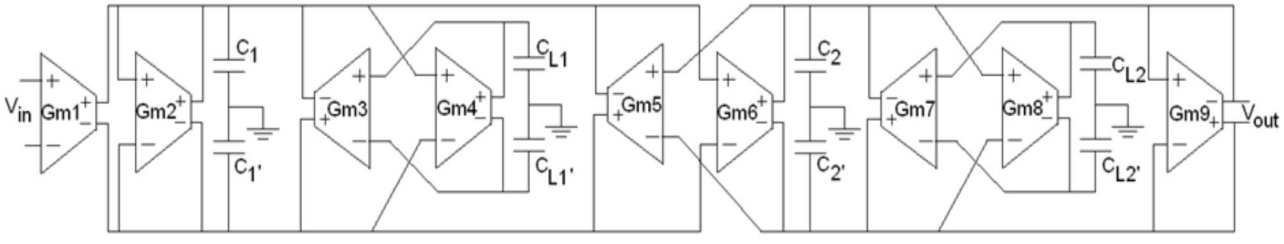


Figure 4: Block diagram of 4th order differential G_m-C band-pass filter

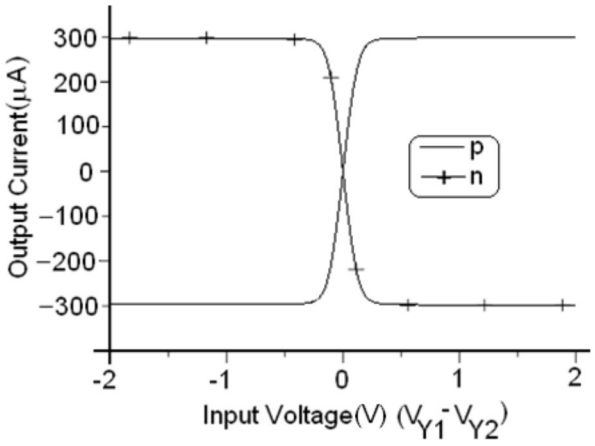


Figure 5: The DC transfer characteristic of improved floating current source

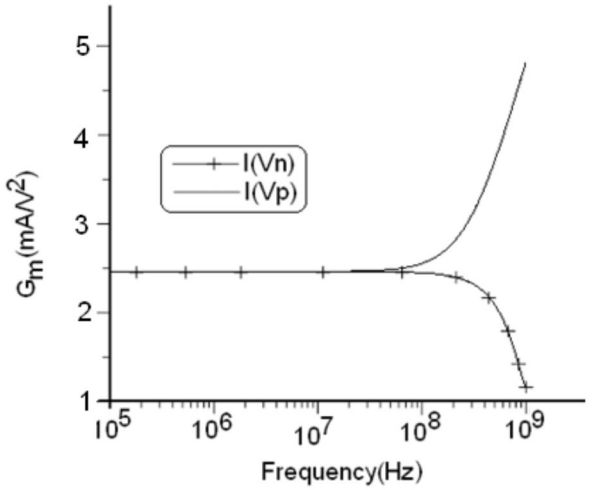


Figure 6: The AC transfer characteristic of improved floating current source G_m

the simulation results of ideal and proposed 4th order differential Gm-C band-pass filter. Center frequency is 30,11 MHz in LTSPICE simulation results of the filter responses. We calculated theoretical centre frequency using Equation 2 as $\omega_0=2\pi x30{,}05$ MHz using the values in Table 5. Simulations results obtained from our experiments show good match with the theoretical results.

Figure 7 shows that, the proposed filter can be used in modern RF communication circuits as the proposed filter operates intermediate frequencies in a superheterodyne (superhet) receiver. The large signal behavior of the proposed circuit band-pass filter was tested by applying a 10 MHz sinusoidal signal with different amplitudes to the input. The dependence of the output harmonic distortion of band-pass filter on input voltage amplitude is illustrated in Figure 8. The total harmonic distortion slowly increases (past tense olabilir bence) depending input voltage which is lower than 400mVp-

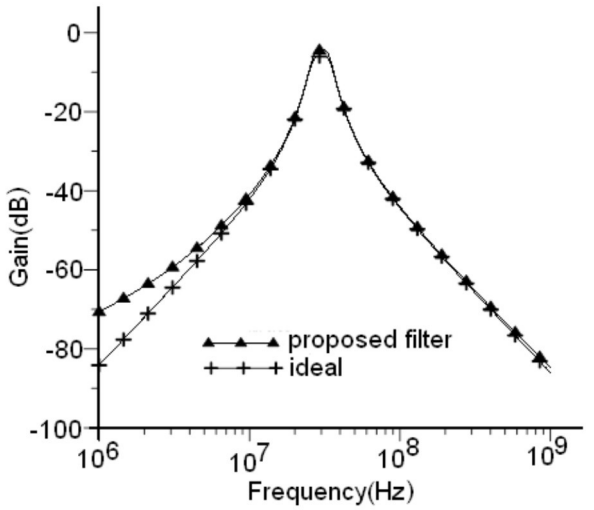


Figure 7: Ideal and simulation frequency responses of 4th order differential G_m-C band-pass filter

p. The THD remains in acceptable limits i.e. 3 %. Thus it confirming the practical utility of the proposed circuit shown in Figure 8.

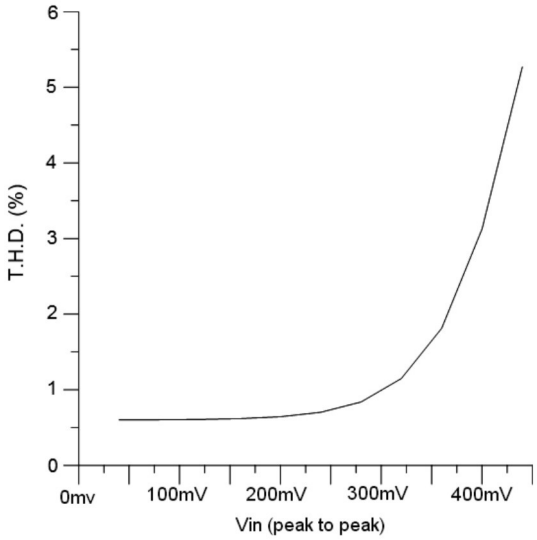


Figure 8: Total harmonic distortion (THD) values of band-pass filter for different frequency values terminals

4 Conclusion

In the study; a fourth order differential G_m-C band-pass filter using improved floating current sources is presented. Floating current source operation is similar to OTA. But, floating current source is superior to the OTA as it contains two different G_ms while there is only one in OTA. The improved floating current source has very simple structure. Its G_m is electronically adjustable using bias current. The filter centre frequency is about 30MHz. Simulations results show good match with the

theoretical results. The proposed filter operates intermediate frequencies and can be used in modern RF communication circuits. The simulations obtained by LTSPICE indicate good functionality of the circuit, low total harmonic distortion. The improved current source structure is simple and includes fewer transistors. Thus, we can use the chip area effectively and also bring simplicity to the design of circuits and reduces the investment cost. The filter does not contain resistor and all capacitors are grounded. Therefore, it is suitable for integration and less effected from parasitic.

5 Acknowledgements

The authors would like to thank Istanbul University Research Fund for this financial support. This work was partially supported by Istanbul University Research Fund with the project code 16402.

6 References

1. FENG, J., WANG, C., ZANG, M., REN, Y. Realization of Current-Mode General Nth-Order Filter Based on Current Mirrors. *3rd International Conference on Advanced Computer Control (ICACC 2011)*, 2011, p. 367-370.
2. BOZOMITU, R.G., CEHAN, V. A VLSI Implementation of a New Low Voltage 4th Order Differential G_m-C Band-Pass Filters For Different Approximation In CMOS Technology. *Acta Technica Napocensis , Electronics and Telecommunications*, 2009, vol.50, p. 5-12.
3. RANJAN, A., PAUL, S.K. Voltage Mode Universal Biquad Using CCCII. *Active and Passive Electronic Components*, 2011, doi:10.1155/2011/439052.
4. KAÇAR, F. A New Tunable Floating CMOS FDNR and Elliptic Filter Applications. *Journal of Circuits, Systems, and Computers*, 2010, vol. 19, n.8 p. 1641-1650.
5. ČAJKA, J., DOSTÁL, T., VRBA, K. High-Order Lowpass Filters Using DVCC Element. *Radioengineering*, 2002, vol. 11, p. 14-17.
6. MEHRMANESH, S., ASLANZADEH, H.A., VAHIDFAR, M.B., ATARODI, M. A 1.8v High Dynamic Range CMOS G_m-C Filter For Portable Video Systems. *IEEE 14th International Conference on Microelectronics ICM-2002*, 2002, p. 38-41.
7. LIN, J.Y., CHANG, W.H., HUNG, C.C. 15mhz Wide Tuning-Range OTA With –69db Hd3 And Its Application To G_m-C Filter. *IEEE International Symposium on VLSI Design, Automation and Test*, 2011, p. 108-111.
8. STEHR, U., HENKEL, F., DALLÜGE, L., WALDOW, P. A Fully Differential CMOS Integrated 4th Order Reconfigurable G_m-C Lowpass Filter For Mobile Communication. *ICECS 2003*, 2003, p. 1-4.
9. D'AMICO, S., GIANNINI, V., BASCHIROTTO, A. A 4th-Order Active-G_m-RC Reconfigurable (UMTS/WLAN) Filter. *IEEE Journal Of Solid-State Circuits*, 2006, vol. 41, p. 1630- 1637.
10. ARBEL, A.F., GOLDMINZ, L. Output Stage for Current-Mode Feedback Amplifiers, Theory And Applications. Analog Integrated Circuits Signal Process, 1992, vol.2, p. 243-255.
11. SOBHY, E. A., SOLIMAN, A.M. Novel CMOS realizations of the inverting second-generation current conveyor and applications, Analog Integrated Circuits Signal Process, 2007, vol.52, p. 57-64.
12. ALTUN, M., KUNTMAN, H. Design of a Fully Differential Current Mode Operational Amplifier with Improved Input-Output Impedances and Its Filter Applications. *AEU: International Journal of Electronics and Communications*, 2008, vol. 62, p. 239-244.

Arrived: 10. 02. 2014
Accepted: 31. 03. 2014

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 44, No. 2 (2014), 142 – 151

MOSFET Spice parameter extraction by modified genetic algorithm

Muhammed Emin Başak[1], Ayten Kuntman[2], Hulusi Hakan Kuntman[3]

[1,2]Istanbul University, Faculty of Engineering, Department of Electrical & Electronics Engineering, Avcılar, Istanbul, Turkey
[3]Istanbul Technical University, Faculty of Electrical &Electronics Engineering, Maslak, Istanbul, Turkey

Abstract: This paper presents a modified genetic algorithm to extract MOSFET BSIM3V3 model parameters. There are several techniques for solving nonlinear optimization problems. Model equations are all non-linear functions and these functions are difficult to be employed in order to extract parameters using deterministic methods.

In this study, modified genetic algorithm is applied to extraction of MOSFET BSIM3V3 model parameters. The results of experimental studies of both 0.35µm fabricated by C35 process and 0.7µm test transistors fabricated by TUBITAK Laboratories have been used for parameter extraction. Threshold voltage and mobility related to model parameters have been found for BSIM3V3. I-V characteristics have been obtained by using both genetic and modified genetic algorithm and then the results were compared with the measurement data. The simulation results show that the modified genetic algorithm implemented for parameter extraction is much more effective and accurate compared to the genetic algorithm.

Keywords: MOSFET, parameter extraction, genetic algorithm, modified genetic algorithm

Določitev Spice parameterov MOSFET s pomočjo spremenjenega generičnega algoritma

Izvleček: Članek predstavlja spremenjen generičen algoritem za določitev modelnih parametrov MOSFET BSIM3V3. Obstajajo številni algoritmi reševanja nelinearnih optimizacijskih problemov. Vse enačbe so nelinearne, kar otežuje določitev parametrov sz determisnističnimi metodami.

Ta določitev parametrov so bili uporabljeni eksperimentalni rezultati tranzistorjev TUBILAK Laboratories v 0.35 µm in 0.70 µm tehologiji. Pragovna napetost in mobilnost je bila določena za BSIM3V3. Za generičen in spremenjen generičen algoritem so bile določene I-U karakteristike. Rezultati kažejo, da so parametri pridobjeni s spremenjenim modelom precej boljši od parametrov pridobljenih z generičnim modelom

Ključne besede: MOSFET, določitev parametrov, keneričen algoritem, spremenjen generičen algoritem

** Corresponding Author's e-mail: mebasak@istanbul.edu.tr*

1 Introduction

The BSIM models derived for MOS transistors use a very large number of parameters. These parameters are extracted for particular operating conditions. Finding a set of parameters is an optimization problem and hence genetic algorithms are good candidates for this task. Optimum parameter extraction exhibits great significance in modern technology [1-2]. Because of the local optimum in the solution space with traditional methods of parameter extraction, this type of extraction processes can produce results far from optimal solutions [3]. In this study, the abilities of genetic algorithm such as easiness, suitability for simple operation, effectiveness, and converging to global optimum are reflected to extraction of MOSFET model parameters. Generally, model parameters are extracted by using commercial software such as ICCAP, UTMOST, BSIMPro [1-3]; since model equations are all non-linear func-

tions, the combination of least squares and Newton Raphson iteration is often adopted. Other nonlinear fitting methods require simplification of the model equations and complex computation such as gradient and inverse Hessian matrix [1-3]. There are also analytical methods [4-5] to extract only a few parameters so that they are not practical for extraction of a complex model such a BSIM3V3. Although SaPOSM [1] and Fast Diffusion [6] methods are global optimization methods, the extraction process in these methods is slow and difficult because they use derivatives in the calculation. Genetic algorithm (GA) method doesn't need complex computation. Consequently, this method is more practical than conventional and analytical methods. One of the other known simple models, called α-power model [7], ignores the channel–length modulation effect and is also unable to predict an accurate value for the drain current in the saturation region. The n-th power model [8] considers the channel–length modulation but the accuracy of this method may not be satisfactory for some applications. A computational intelligence technique is used to extract and simulate the stationary and high-frequency properties of bipolar junction transistors in [9]. Genetic algorithm and simulated annealing are performed in determining the model parameters in [10, 11], but only nine parameters are used for the accuracy and the error prediction is found as 1.3% in these methods. The performance of the particle swarm optimizations (PSO) is better than the genetic algorithm in terms of accuracy and consistency shown in [12]. However, the root mean square (RMS) error between measurement data and model results is within 3-7% for various characteristics in PSO method. PSO and GA have been used to extract parameters for NMOS device in [13]. The calculated average errors have been found as 4.84% and 7.15% for PSO and GA, respectively. In a recent work, an application of differential evolution to extract 16 small signal model parameters of GaAs MESFET (metal extended semiconductor field effect transistor) has been presented [14]. The MOS 9 Model is optimized using the simplified model instead of direct optimization by using GA in [15]. In essence, most of the research on GA has been done on electrical parameter extraction [15-21].

Before the actual fabrication of a designed circuit, the circuit performance should be predicted and evaluated. A better modeling is needed to predict and evaluate the behavior of the circuit. These models, designed mathematically, get the great benefit of improving and predicting the real time behaviour of the transistors. In this context, there are several works performed to realize accurate MOS transistor modeling [22-27].

Genetic Algorithm is an intelligence optimization algorithm that simulates the evolution of natural biology [28-29]. It originates from a population that represents a gather of probable results. GA is well suited for finding near optimal results in irregular parameter spaces. A population is composed of a certain quantity of individuals. These individuals are obtained by gene coding. After the generation of the initial population, the solution becomes more adequate with the population evolution according to the principle of natural selection. In every generation, individuals are selected according to their fitness. A new population that represents the new gather of new solutions is produced through crossover and mutation by using genetic operators [30]. The latter population is more suitable than former population. The most excellent individual of the last population is output as the approximately most suitable solution. Z. Michalewicz and et al. [31] proposed a modification of GA which uses the floating point representation and some specialized operators. In addition to applying the enhancements of GA, we proposed some extra contributions in MGA. In our study, the main structure of the flowchart, the order of the operators, ending condition, and using the method of the crossover and mutation operators are the main differences between GA and MGA. The aim of this paper is to show how the genetic algorithm can be modified and used.

In this study, Spice BSIM3V3 MOS model parameters have been extracted and optimized with both genetic algorithm and modified genetic algorithm, separately. Both threshold voltage and mobility related model parameters have been found for BSIM3V3.3. I-V characteristics have been extracted by using both genetic algorithm and modified genetic algorithm. I-V characteristics of extracting parameters data results have been compared with measurement results. The simulation results show that a modified genetic algorithm extracts accurately and effectively all 26 model parameters of the MOSFET. This study not only extracts the BSIM3V3.3 MOSFET model parameters, but also enhances the genetic algorithm. Although the work has been performed using old technology, the proposed extraction strategy has been verified for the current technology devices. In this work, Section 2 gives an overview of genetic algorithm and modifications of the standard GA design. Section 3 describes basic points, including the necessary steps on parameter extraction using GA and MGA. Section 4 reflects the results and discussion, including the evaluation of measurements and the model parameters obtained, finally followed by Section 5 to conclude the work.

2 The genetic algorithm

The genetic algorithm is an inspiration from the genetic process of nature. It offers acceptable solutions for

hard problems in reasonable computation times. GA tries to optimize the solution set for a number of iterations and picks up the most optimized solution available to a problem at the end. Initial population creation, fitness evaluation, selection, crossover, and mutation are the five basic functions of the algorithm.

Creation of the initial population is the first step of the genetic algorithm. A population is a set of individuals used as parameters. Each individual has its own genetic content, called chromosomes. In the initial population creation process, chromosomes are produced randomly in order to assume diversity in the initial population. In our program, each chromosome is coded as floating point numbers in order to generate the solution vector. The lower and upper bound of the parameters representing the solution of the problem are given in Table 1. The population size is chosen as 500 in this study. After creating the initial population of parameters, the fitness value of parameters is evaluated. The fitness function which is used in both GA and MGA is presented in Equation 1.

$$f = \sqrt{\sum \left(\frac{I_{d,lab} - I_{d,\mathrm{mod}el}}{I_{d,lab}} \right)^2} \tag{1}$$

where f is the fitness function, $I_{d,lab}$ and $I_{d,model}$ corresponds to the measured and extracted values of I_{ds} of the MOSFET, respectively.

If all chromosomes in fitness function are becoming nearly same, the program is terminated. Otherwise, either two parameters are randomly picked from the mating pool generated by the selection operator as the potential parents or they may be copied into the next generation directly. In each case, they have the ability to carry their superior properties to the next generation. The exchange of genetic material occurs between the parameters with a probability of β. New chromosomes (p_{new}) are obtained by using the following equation.

$$p_{new} = \beta p_{mn} + (1 - \beta) p_{dn} \tag{2}$$

Here, β is the random number on the interval [0, 1]; p_{mn} is the n-th variable in the mother chromosome and p_{dn} is the n-th variable in the father chromosome. Crossover plays a primary role with the reproduction operator in GA. After reproduction emphasizes the highly fit strings, crossover recombines these selected strings to produce better individuals. After crossover, some randomly selected members are mutated according to some parameters in order to produce different genes that are not existed in the population.

The number of mutations (M_{num}) is determined in Equation 3 by multiplying the number of chromosomes (N_{chr}) chosen as 26, the number of genes (N_{gen}) chosen as 500, and mutation rate (Mrate) chosen as 0,02. New mutated chromosomes (p_{newmut}) are obtained by using Equation 4.

$$M_{num} = N_{chr} \times N_{gen} \times M_{rate} \tag{3}$$

$$p_{new_{mut}} = p_n + \sigma \mathrm{N}_n(0,1) \tag{4}$$

Where σ is a standard deviation of the normal distribution and $\sim N_n(0,1)$ is a random number whose average and deviation are zero and one, respectively. The iterations continue for a predefined number of times, called generation, to reveal the most optimal solution. Classical genetic algorithm main program flowchart is given in Figure 1. In our program, number of generations are chosen as 100.

Table 1: The upper and lower bound of MOSFET BSIM3V3 model parameters extracted by both GA and MGA

No	Parameters	Lower Bound	Upper Bound
1	VTHO	1×10^{-2}	1
2	K1	1×10^{-10}	1
3	K2	-1×10^{-10}	1×10^{-10}
4	U0	1	1×10^{5}
5	UA	-1×10^{-20}	1×10^{-20}
6	UB	1×10^{-20}	1
7	UC	1×10^{-20}	1
8	NLX	1×10^{-10}	1
9	DVT0	-100	100
10	DVT1	-100	100
11	DVT2	-1×10^{-10}	1×10^{-10}
12	RDSW	1	1×10^{5}
13	PRWG	1×10^{-20}	1
14	PRWB	-1×10^{-20}	1
15	WR	1	2
16	W0	1×10^{-20}	1
17	K3	-10	10
18	K3B	-10	10
19	A0	-10	10
20	AGS	-1	1
21	B0	1×10^{-20}	1
22	B1	1×10^{-20}	1
23	KETA	1×10^{-20}	1
24	DVT0W	1×10^{-20}	1
25	DVT1W	1	1×10^{10}
26	DVT2W	-1×10^{-20}	1

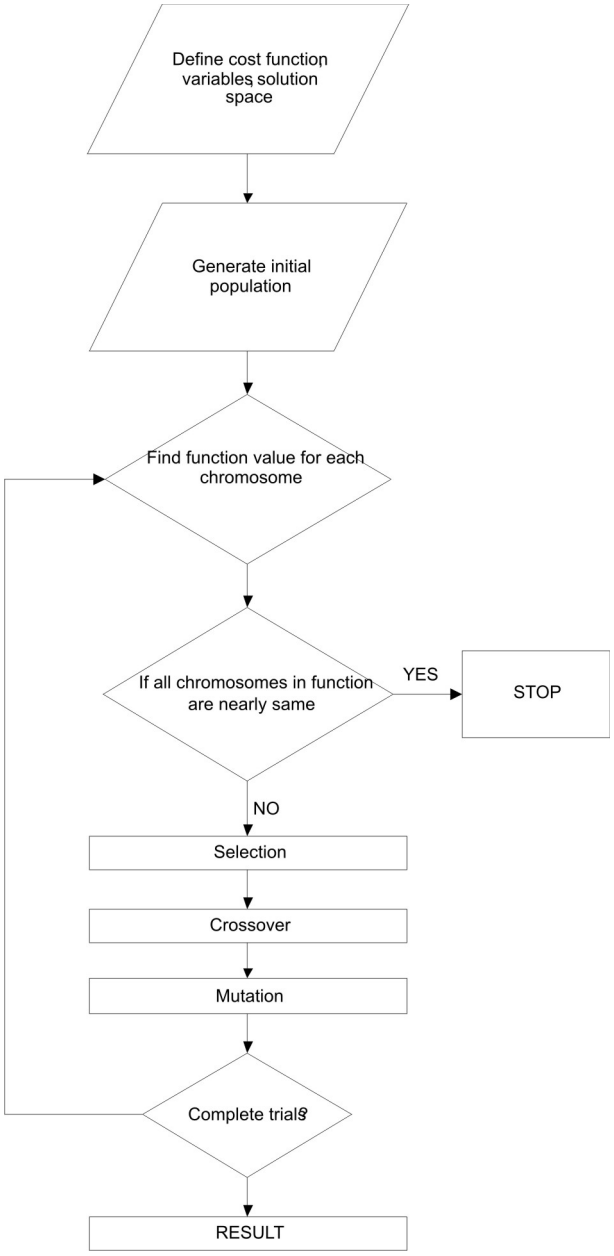


Figure 1: Main program flowchart of genetic algorithm

2.1 A modified genetic algorithm

Creation of the initial population is the first step of the modified genetic algorithm same as genetic algorithm. A population is a set of individuals used as parameters. Each individual has its own genetic content, called chromosomes. The modified genetic algorithm uses the floating point representation, where lower and upper bound for the parameters are used as the same as genetic algorithm. The population size is also chosen as same as genetic algorithm.

The main differences between GA and MGA are listed below.

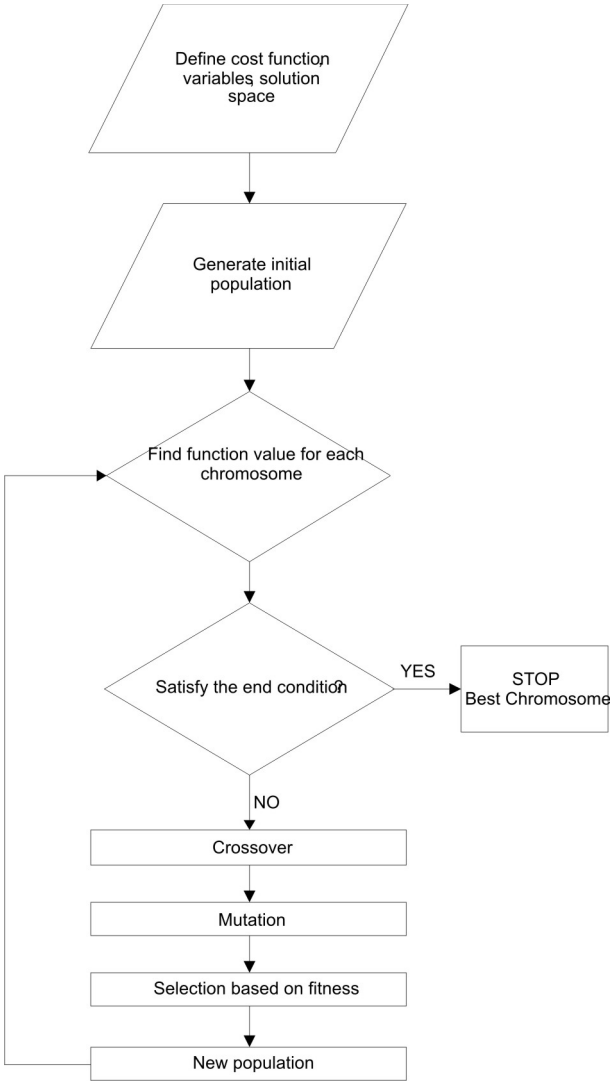


Figure 2: Main program flowchart of modified genetic algorithm

1. The main flowchart of MGA shown in Figure 2 is different from the standard GA shown in Figure 1.
2. Using a selection operator is one of the main differences between the GA and MGA. Selection operator is used after the crossover and mutation operators are applied to all the population in the GA. Unlikely, the selection operator is used after the each individual of the population is applied to mutation and crossover operator in the MGA.
3. Crossover and mutation operators simultaneously apply to all populations in GA, but chromosomes are taken one by one and new parameter is obtained by randomly selected another three or five chromosomes in MGA. The suitability of existing chromosomes is compared with the suitability of the new chromosomes and then whichever is better is transferred into the next population.

4. The condition that terminates the GA is satisfied when either the values of all chromosomes are nearly same in the function or determined trials are completed. However, the end condition of MGA is satisfied either in the minimum value of the fitness function or when determined trial number is completed.

3 Parameter extraction

Measurement of I-V characteristics of MOSFET was carried out using a parametric analyzer and wafer prober. After performing measurements using a wafer probe and parametric analyzer, the results of the I-V measurement were applied to GA and MGA. MOSFET model parameters determined by using five different steps applied to both genetic algorithm and modified genetic algorithm. These steps are defined below and summarized in Table 2. GA and the MGA program were written in MATLAB file. The operating temperature was settled at 294K.

Different combinations of GA and MGA parameters were used to find the best fitness chromosome. The default generation count was taken as 100. If the result of the first run after 100 generations was not satisfactory and had an error greater than 10%, then a second run with a different random seed number was executed. Moreover, both of the algorithms were applied to the population during the simulation as the number of parameters was chosen as 500.

Before extracting model parameters, some process parameters are required to be known. These process parameters are the gate oxide thickness (Tox), doping concentration in the channel (Nch), the temperature at which the data are taken (T), mask level channel length (Ldrawn), mask level channel width (Wdrawn) and junction depth (Xj). The values of the process parameters are shown in Table 3.

Table 3: Some process parameters are used in extraction

Process Parameters	Value
Tox	7.575×10^{-9} m
Nch	2.611×10^{17} 1/cm3
T	294 K
Ldrawn	0.45 µm
Wdrawn	0.538 µm
Xj	3.0×10^{-7} m

One large sized device and two sets of small-sized devices are required to extract the transistor parameters. Geometric features of transistors used in the extraction of parameters are shown in Figure 3. Equations of the extracted parameters are taken from BSIM3V3.3 User's Manual [2] for the extraction process.

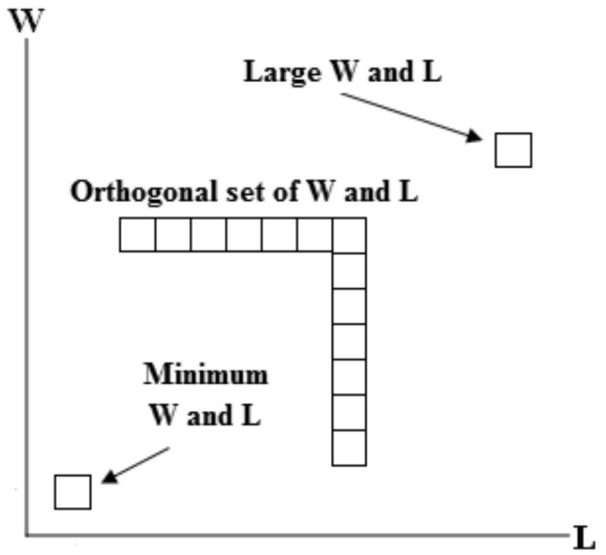


Figure 3: Geometric features of transistors used in the extraction of parameters

Table 2: MOSFET model parameters extraction steps

Step	Parameters	Dimensions of Transistors	Measurement
Step 1	VTH0, K1, K2, µ0, UA, UB, UC	Wide channel width and long channel length transistors	I_d vs V_{gs} data at V_{ds} equals low voltage with different V_{bs} values
Step 2	K3, W0, K3B	Narrow channel width and long channel length transistors	I_d vs V_{gs} data at V_{ds} equals low voltage with different V_{bs} values
Step 3	RDSW, DVT0, DVT1, DVT2, NLX, WR, PRWG, PRWB	Wide channel width and short channel length transistors	I_{ds}-V_{gs} at V_{ds}=0.05V, V_{bs} is Parameter
Step 4	A0, AGS, B0, B1, KETA	Short channel length and narrow channel width transistors	I_d - V_{ds} curves obtained from different values of V_{gs} and V_{ds} with the condition of zero.
Step 5	DVT0W, DVT1W, DVT2W	Short channel length and narrow channel width transistors	I_d – V_{gs} curves obtained from different values of V_{bs} and V_{ds} equals low voltage

The first step is applied to the wide and long transistor and the target parameters are **VTH0, K1, K2, µ0, UA, UB,** and **UC.** It requires I_d - V_{gs} curves at low voltage of V_{ds} with different V_{bs} values [2-3].

$$V_{th} = V_{TH0} + K_1\left(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}\right) - K_2 V_{bs} \tag{5}$$

$$\mu_{eff} = \frac{\mu_0}{1 + \left(U_a + U_c V_{bs}\right)\left(\frac{V_{gst} + 2V_{th}}{Tox}\right) + U_b\left(\frac{V_{gst} + 2V_{th}}{Tox}\right)^2} \tag{6}$$

The second step is applied to the narrow W and long L transistor and the target parameters are **K3, W0** and **K3B.** It requires I_d - V_{gs} curves at low voltage of V_{ds} with different V_{bs} values [2-3].

$$\begin{aligned} V_{th} &= V_{TH0} + K_1\left(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s}\right) - K_2 V_{bseff} \\ &+ K_1\left(\sqrt{1 + \frac{N_{LX}}{L_{eff}}} - 1\right)\sqrt{\phi_s} + \left(K_3 + K_{3B} V_{bseff}\right)\frac{T_{OX}}{W'_{eff} + W_0}\phi_s \\ &- D_{VT0}\left(\exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right) + 2\exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right)\left(V_{bi} - \phi_s\right) \\ &- \left(\exp\left(-D_{SUB}\frac{L_{eff}}{2l_{to}}\right) + 2\exp\left(-D_{SUB}\frac{L_{eff}}{l_{to}}\right)\right)\left(E_{TA0} + E_{TAB} V_{bseff}\right)V_{ds} \end{aligned} \tag{7}$$

The third step is applied to the wide W and short L device and the target parameters are **RDSW, DVT0, DVT1, DVT2, NLX, WR, PRWG,** and **PRWB** [2-3].

$$\begin{aligned} V_{th} &= V_{TH0} + K_1\left(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s}\right) - K_2 V_{bseff} \\ &+ K_1\left(\sqrt{1 + \frac{N_{LX}}{L_{eff}}} - 1\right)\sqrt{\phi_s} + \left(K_3 + K_{3B} V_{bseff}\right)\frac{T_{OX}}{W'_{eff} + W_0}\phi_s \\ &- D_{VT0}\left(\exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right) + 2\exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right)\left(V_{bi} - \phi_s\right) \\ &- \left(\exp\left(-D_{SUB}\frac{L_{eff}}{2l_{to}}\right) + 2\exp\left(-D_{SUB}\frac{L_{eff}}{l_{to}}\right)\right)\left(E_{TA0} + E_{TAB} V_{bseff}\right)V_{ds} \end{aligned} \tag{8}$$

$$R_{ds} = \frac{R_{DSW}\left(1 + P_{RWG} V_{gsteff} + P_{RWB}\left(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s}\right)\right)}{\left(10^6 W_{eff}'\right)^{W_r}} \tag{9}$$

The fourth step is applied to only small sized device (short channel and narrow width). In this step, the large sized transistor with the fixed channel width and short-channel length was used for extraction of **A0** and **AGS** parameters. Also fixed channel length with a large channel width of transistors and other small sized transistors were used for determining **B0, B1,** and **KETA** parameters. I_d - V_{ds} curves were obtained from different values of V_{gs} and V_{bs} with the condition of zero [2-3].

$$A_{bulk} = \left(1 + \frac{K_{1ox}}{2\sqrt{\phi_s - V_{bseff}}}\left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}}\left(1 - A_{gs} V_{gsteff}\left(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}}\right)^2\right) + \frac{B_0}{W'_{eff} + B_1}\right)\right) \cdot \frac{1}{1 + KetaV_{bseff}} \tag{10}$$

The fifth step is applied to small sized transistors. **DVT0W, DVT1W,** and **DVT2W** parameters were determined by using a small-sized transistor with the short channel length and narrow channel width. I_d – V_{gs} curves were obtained from different values of V_{bs} [2-3].

$$\begin{aligned} V_{th} &= V_{TH0} + K_1\left(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s}\right) - K_2 V_{bseff} \\ &+ K_1\left(\sqrt{1 + \frac{N_{LX}}{L_{eff}}} - 1\right)\sqrt{\phi_s} + \left(K_3 + K_{3B} V_{bseff}\right)\frac{T_{OX}}{W'_{eff} + W_0}\phi_s \\ &- D_{VT0}\left(\exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right) + 2\exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right)\left(V_{bi} - \phi_s\right) \\ &- \left(\exp\left(-D_{SUB}\frac{L_{eff}}{2l_{to}}\right) + 2\exp\left(-D_{SUB}\frac{L_{eff}}{l_{to}}\right)\right)\left(E_{TA0} + E_{TAB} V_{bseff}\right)V_{ds} \\ &- D_{VT0W}\left(\exp\left(-D_{VT1W}\frac{W'_{eff} L_{eff}}{2l_{tw}}\right) + 2\exp\left(-D_{VT1W}\frac{W'_{eff} L_{eff}}{l_{tw}}\right)\right)\left(V_{bi} - \phi_s\right) \end{aligned} \tag{11}$$

GA and the MGA program were written in MATLAB file. The main program flowcharts of a genetic algorithm and modified genetic algorithm are given in Figure 2 and Figure 3, respectively.

4 Results and discussion

The values of MOSFET BSIM3V3 model parameters extracted by GA and MGA for 0.7µm test transistors fabricated by TUBITAK Laboratories are shown in Table 4. The results of the fitted drain current using BSIM3V3 model with different bias gate are shown in Figure 4 - 5. In these figures, solid lines, squared lines, and dashed lines represent the I – V data measured, parameters extracted by using GA, and parameters extracted by using MGA, respectively. Model generated data with extracted values of parameters has shown excellent agreement with measurement data for all types of characteristics.

Table 4: GA and MGA extracted MOSFET BSIM3V3 model parameters for 0.7 µm test transistors fabricated by TUBITAK

Parameters	Extracted by GA	Extracted by MGA
VTHO	6.518×10^{-1}	6.438×10^{-01}
K1	7.935×10^{-01}	7.7351×10^{-01}
K2	-7.3912×10^{-02}	-8.4912×10^{-02}
U0	$4.491\times10^{+02}$	$4.511\times10^{+02}$
UA	$-3.1652\cdot10^{-10}$	$-3.055\cdot10^{-11}$
UB	2.565×10^{-18}	2.7711×10^{-18}
UC	2.3660×10^{-11}	3.1660×10^{-14}
NLX	4.23×10^{-7}	4.1617×10^{-7}
DVT0	3.05	3.013
DVT1	3.59	3.292
DVT2	-7.3916×10^{-2}	-7.5516×10^{-2}

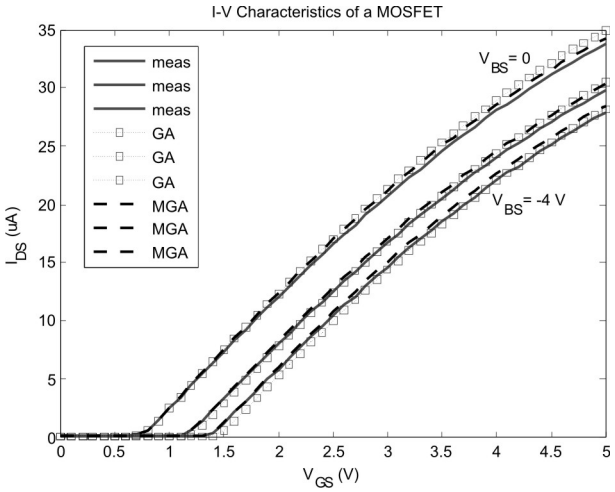


Figure 4: The results of the fitted drain currents where V_{BS} varies from 0 to -4.0 V with the step of 2 V. (The dimensions of transistor are W = 27 µm and L = 27 µm.)

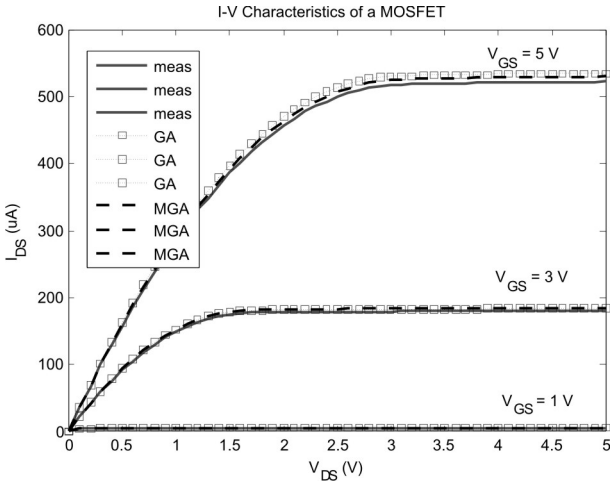


Figure 5: The results of the fitted drain currents where V_{GS} varies from 1 to 5.0 V with the step of 2 V and bulk bias V_{BS} is 0 V. (The dimensions of transistor are W = 27 µm and L = 27 µm.)

The values of MOSFET BSIM3V3 model parameters extracted by GA and MGA for 0.35µm test transistors fabricated by C35 process are shown in Table 5. The result of the fitted drain current using BSIM3V3 model with different bias gate is shown in Figure 6 - 10. In these figures, solid lines, dotted lines, and dashed lines represent the I – V data measured, parameters extracted by using GA, and parameters extracted by using MGA, respectively. Model generated data with extracted values of parameters has shown excellent agreement with measurement data for all types of characteristics.

Table 5: GA and MGA extracted MOSFET BSIM3V3 model parameters for 0.35 µm transistors fabricated by C35 process

No	Parameters	Extracted by GA	Extracted by MGA
1	VTHO	4.999×10^{-1}	5.013×10^{-01}
2	K1	4.96296×10^{-01}	5.0302×10^{-01}
3	K2	3.3385×10^{-02}	3.41×10^{-02}
4	U0	$4.788\times10^{+02}$	$4.7905\times10^{+02}$
5	UA	4.605×10^{-12}	4.396×10^{-12}
6	UB	2.039×10^{-18}	2.112×10^{-18}
7	UC	7.785×10^{-20}	2.914×10^{-17}
8	NLX	2.048×10^{-7}	1.856×10^{-7}
9	DVT0	4.9101×10^{1}	4.9513×10^{1}
10	DVT1	1.04	1.091
11	DVT2	-8.975×10^{-3}	-8.416×10^{-2}
12	RDSW	3.603×10^{2}	3.317×10^{2}
13	PRWG	7.433×10^{-19}	1.901×10^{-17}
14	PRWB	-2.016×10^{-1}	-2.518×10^{-1}
15	WR	1.0091	1.0012
16	W0	3.173×10^{-7}	2.731×10^{-7}
17	K3	-1.536	-1.151
18	K3B	-4.409×10^{-1}	-0.4361
19	A0	2.164	2.704
20	AGS	1.848×10^{-1}	2.598×10^{-1}
21	B0	7.0391×10^{-9}	5.359×10^{-9}
22	B1	1.98×10^{-18}	9.194×10^{-17}
23	KETA	4.102×10^{-2}	2.420×10^{-2}
24	DVT0W	1.129×10^{-10}	9.919×10^{-11}
25	DVT1W	5.981×10^{4}	6.1702×10^{4}
26	DVT2W	-2.332×10^{-2}	-2.0141×10^{-3}

Root Mean Squared (RMS) percentage errors of 0.35µm transistors fabricated by C35 process for both GA and

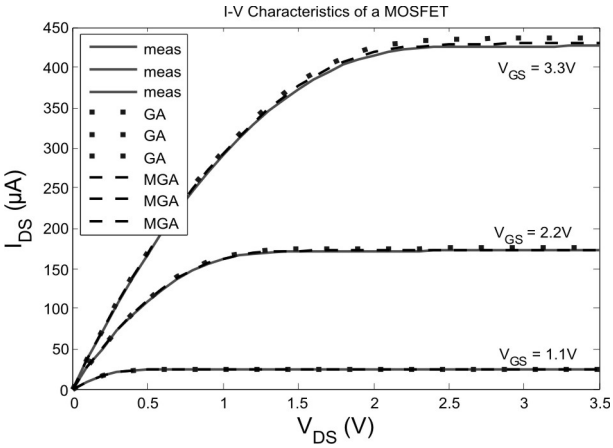


Figure 6: The results of the fitted drain currents where V_{GS} varies from 1.1 to 3.3 V with the step of 1.1 V and bulk bias V_{BS} is 0 V. (The dimensions of transistors are W = 10 µm and L = 10 µm).

MGA were calculated. The results showed that MGA implemented parameter extraction is more successful than GA implemented parameter extraction. The RMS error between measurement data and extracted data was shown in Table 6. It was observed that this error occurs between 0.75% and 2% for various characteristics of 0.35µm device. MGA results agree very well with the measurements.

Table 6: Root Mean Squared (RMS) percentage errors of 0.35 µm transistors fabricated by C35 process

Root Mean Squared Percentage Error (%) for GA				Root Mean Squared Percentage Error (%) for MGA	
	Id-Vds		Id-Vgs	Id-Vds	Id-Vgs
W=10µm L=10µm	Vds=0.05V	2.44	2.09	1.19	1.61
	Vds=3.3V	1.11	1.67	0.75	1.13
W=10µm L=0.35µm	Vds=0.05V	1.09	1.66	0.76	0.81
	Vds=3.3V	2.45	2.03	1.11	1.23
W=0.35µm L=10µm	Vds=0.05V	2.25	2.11	1.08	1.06
	Vds=3.3V	2.71	2.50	1.21	1.04
W=0.35µm L=0.35µm	Vds=0.05V	3.01	3.58	1.93	1.63
	Vds=3.3V	2.62	2.29	0.99	1.28

5 Conclusion

In this research, based on a global optimization algorithm, modified genetic algorithm is employed to specify the MOSFET model parameter values. For this extraction experiment, the industrial Standard BSIM3V3.3 SPICE model is adopted. The results show that this technique reduces the engineering effort required to

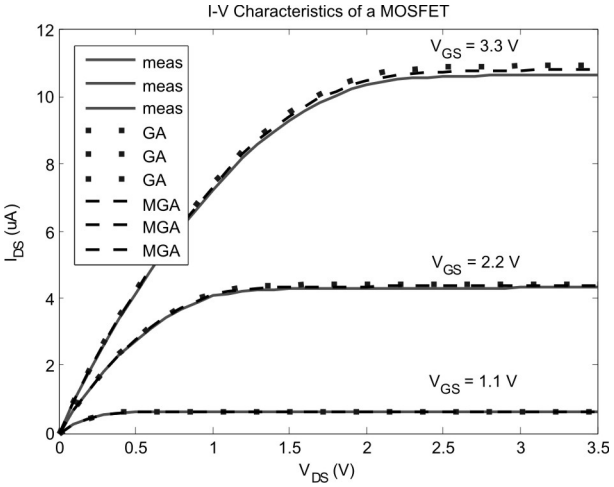


Figure 7: The results of the fitted drain currents where V_{GS} varies from 1.1 to 3.3 V with the step of 1.1 V and bulk bias V_{BS} is 0 V. (The dimensions of transistors are W = 0.35 µm and L = 10 µm).

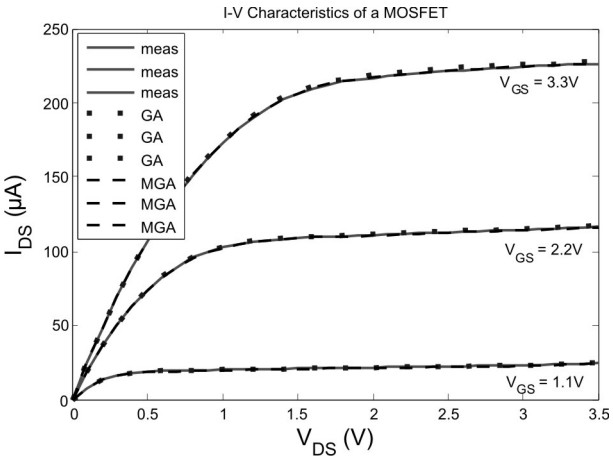


Figure 8: The results of the fitted drain currents where V_{GS} varies from 1.1 to 3.3 V with the step of 1.1 V and bulk bias V_{BS} is 0 V. (The dimensions of transistors are W = 0.35 µm and L = 0.35 µm).

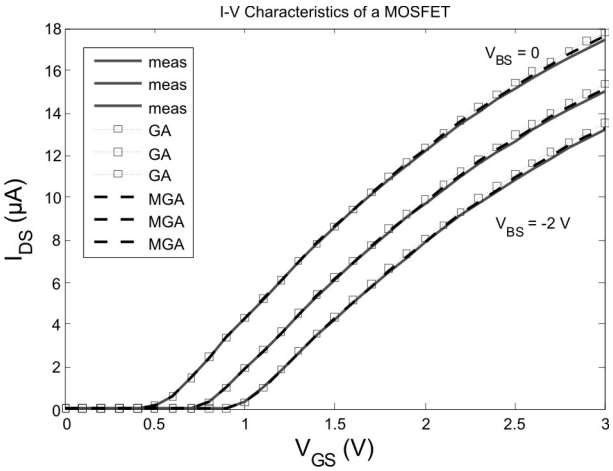


Figure 9: The results of the fitted drain currents where V_{BS} varies from 0 to -2.0 V with the step of 1 V. (The dimensions of transistors are W = 10 µm and L = 10 µm.)

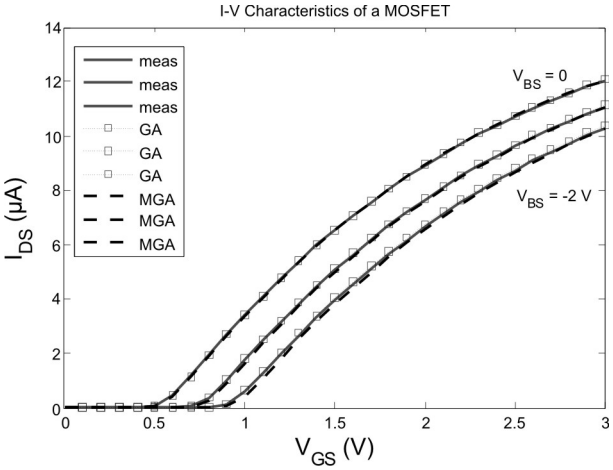


Figure 10: The results of the fitted drain currents where V_{BS} varies from 0 to -2.0 V with the step of 1 V. (The dimensions of transistors are W = 0.35 µm and L = 0.35 µm.)

produce a model while improving overall model quality. The modified genetic algorithm is empirically shown as a robust, general purpose optimizer, and suitable for optimizing multimodal and high dimensional objective functions. Furthermore, MGA is used as powerful genetic operators to concurrently guide its research throughout the solution space by considering a set of parameter at a time. The parameters are extracted step-by-step depending upon the characteristics where they play a major role.

We have used a genetic algorithm and modified genetic algorithm to extract parameters for NMOS device. MGA is deemed highly effective in order to solve the non-linear and the transient problems. The results of the extracted parameters and measurement curves are obtained close to each other due to the fact that the same determined parameters of the mathematical models are used in the both algorithms. Values obtained in determining working conditions for especially small sized transistor parameters are found to be in high accuracy. This can be considered as the success of this work because small-sized problems on behalf of the designer is crucial for troubleshooting. This study not only extracts the BSIM3V3.3 MOSFET model parameters, but also enhances the genetic algorithm. It was observed that MGA exhibits much better performance compared to GA in terms of accuracy and consistency. The simulations showed that MGA accurately extracts all 26 model parameters of MOSFET in an effective way.

6 Acknowledgement

This study supported by the Research Fund of the Istanbul University. Project number T-36/15122006.

7 References

1. Y. H. Hu, S. W. Pan, "SaPOSM: An Optimization Method Applied to Parameter Extraction of MOSFET Models", IEEE Trans on CAD, Vol 12, pp. 1481-1487, 1993.
2. W. Liu, X. Jin, X. Xi, J. Chen, M. Jeng, Z. Liu, Y. Cheng, K. Chen, M. Chan, K. Hui, J. Huang, R. Tu, K. Ping Ko, C. Hu, BSIM3V3.3 User's Manual. Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, 2005.
3. W. Liu, MOSFET Models for SPICE Simulation Including BSIM3v3 and BSIM4, Wiley Interscience. ISBN-10: 0471396974, 2001.
4. A. Ortiz-Conde, A. Cerdeira, M. Estrada, D. Flandre, J.J. Liou, "A method to extract mobility degradation and total series resistance of fully-depleted SOI MOSFETs", IEEE Transactions on Electron Devices, Vol 49, pp. 82-88, 2002.
5. C. L. Lou, W. K. Chim, D. S. H. Chan, T. Pan, "A novel single-device DC method for extraction of the effective mobility and source-drain resistance of fresh and hot-carrier degraded drain-engineered MOSFET's", IEEE Transactions on Electron devices, Vol 45, pp. 1317-1323, 1998.
6. T. Sakurai, B. Lin, R. Newton, "Fast Simulated Diffusion: An optimization Algorithm for Multiminimum Problems and Its Application to MOSFET Model Parameter Extraction.", IEEE Trans on CAD, Vol 11, pp. 228-234, 1992.
7. T. Sakurai, R. Newton, "Alpha-power low MOSFET model and its application to CMOS inverter delay and other formulas", IEEE Journal of Sold State Circuits, Vol 25, pp. 584-594, 1990.
8. T. Sakurai, R. Newton, "A Simple MOSFET model for circuit analysis", IEEE Trans Electron Device, Vol 38, pp. 887-894, 1991.
9. Y. Li, Y. Y. Cho, C. S. Wang, K. Y. Huang, "A genetic algorithm approach to InGaP/GaAs HBT parameters extraction and RF characterization", Japanese Journal of Applied Physics, Vol 42, pp. 2371–2374, 2003.
10. M. Taherzadeh-Sani, A. Abbasian, B. Amelifard, A. Afzali-Kusha, "MOS Compact I-V Modeling with Variable Accuracy Based on Genetic Algorithm and Simulated Annealing", Microelectronics, ICM 2004 Proceedings, The 16th International Conference, pp. 364 – 367, 6-8 Dec 2004
11. A. Abbasian, M. Taherzadeh-Sani, B. Amelifard, A. Afzali-Kusha, "Modeling of MOS Transistors Based on Genetic Algorithm and Simulated Annealing", Circuits and Systems, ISCAS 2005, IEEE International Symposium, 23-26 May 2005
12. R. A. Thakker, N. Gandhi, M. B. Patil, K. G. Anil, "Parameter Extraction for PSP MOSFET Model using Particle Swarm Optimization", Physics of Semiconductor Devices, IWPSD 2007, International Workshop, 2007
13. A. M. Chopde, S. Khandelwal, R. A. Thakker, M. B. Patil, K. G. Anil, "Parameter Extraction for MOS Model 11 using Particle Swarm Optimization", Physics of Semiconductor Devices, IWPSD 2007, International Workshop, 2007.
14. L. S. Samrat, K. U. Siba, "Differential Evolution Algorithm for MESFET Small Signal Model Parameter Extraction", Electronic System Design (ISED), 2010 International Symposium, 2010.
15. D. Isa, L. Mei Fong, L. Leong, L. Y. Kuan, "GA optimized Power MOSFET model", Electronics Manufacturing and Technology, 31st International Conference, 8-10 Nov 2007.
16. M. E. Başak, A. Kuntman, H. Kuntman, "Extraction of BSIM3V3 Threshold Voltage and Mobility Effect

Parameters with Genetic Algorithm", 5 - 9 December 2007, ELECO 2007: The 5th International Conference on Electrical and Electronics, (Electronics), pp. 75-79, 2007.
17. CK. Chen, "A Genetic Algorithm For Deep-Submicron Mosfet Parameters Extraction And Simulation", Masters' thesis, 2002.
18. M. E. Basak, "Genetik Algoritma ile MOS Parametrelerinin Belirlenmesi ve Optimizasyonu", Fen Bilimleri Enstitüsü, Elektrik –Elektronik Müh Anabilim Dalı Yüksek Lisans Tezi, 2008.
19. M. E. Başak, A. Kuntman, H. Kuntman, "MOS parameter extraction and optimization with genetic algorithm", Journal of Electrical & Electronics Engineering, Engineering Faculty, Istanbul University, Vol 9, pp. 1101-1107, 2009.
20. Y. Li, "An automatic parameter extraction technique for advanced CMOS device modeling using genetic algorithm", Micro. Eng., Vol 84, pp. 260-272, 2007.
21. M. Keser, K. Joardar, "Genetic algorithm based MOSFET model parameter extraction," Proc. of Int. Conf. on Modeling and Simulation of Micro., pp. 341-344, 2000.
22. K. Doganis, D. L. Scharfetter, "General Optimization and Extraction of IC Device Model Parameters", IEEE Transactions on Electron devices, Vol 30, pp. 1219-1228, 1983.
23. H. Abebe, V. C. Tyree, BSIM3V3.1 Model Parameters Extraction and Optimization, USC-ISI, The MOSIS Service, 2000.
24. P. R. Karlsson, K. O. Jeppson, "A direct extraction algorithm for a submicron MOS transistor model", Pro-ceedings of the 1993 International Conference on Microelectronic Test Structures, pp. 157–162, 1993.
25. P. R. Karlsson, K. O. Jeppson, "A direct method to extract effective geometries and series resistances of MOS transistors", Proceedings of the 1994 International Conference on Microelectronic Test Structures, pp. 184–189, 1994.
26. H. Kunii, Y. Kinouchi, "Parameter estimation of lumped element circuit for tissue impedance", Proceedings of the 20th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, Vol 20, pp. 3108–3111, 1998.
27. S. P. Antognetti, G. Massobrio, Semiconductor Device Modeling With SPICE, McGraw-Hill Book Comp. ISBN: 007 0.024.693, 1993.
28. D. E. Goldberg, Genetic Algoritms in Search, Optimization, and Machine Learning. Addison-Wesley, Reading, pp. 1-432, 1989.
29. Z. Michalewicz, Genetic algorithms + data structures = evolution programs, Springer-Verlag, Berlin, Heidelberg, New York, ISBN 3-540-60676-9, 1995.
30. S. E. Haupt, R. L. Haupt, Practical Genetic Algorithms, A Wiley-Interscience publication, ISBN 0-471-45565-2, 2004.
31. Z. Michalewicz, C. Z. Janikow, J. B. Krawczyk, "A Modified Genetic Algorithm For Optimal Control Problems", Computers & Mathematics With Applications, vol. 23, Issue 12, Pages 83–94, 1992.

Arrived: 17. 12. 2013
Accepted: 04. 04. 2014

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 44, No. 2 (2014), 152 – 158

Design of an intelligent electronic system for dump truck tip-over prevention

Chin Leei Cham, Wooi Haw Tan

Faculty of Engineering, Multimedia University, Malaysia

Abstract: This paper presents the basic idea behind the implementation of an intelligent electronic tip-over prevention system for a 30-tonne dump truck using a microcontroller. The objective is to design an intelligent control system to manage the stability of the truck during the dumping process. The three factors that contribute to the stability of the dump truck during the lifting process are the horizontal chassis position of the vehicle, the tilting angle of the dump bed, and the lifting speed. An intelligent tip-over prevention system has been designed and successfully tested by recording and analyzing the real-time data collected from multiple accelerometers and gyro sensors fixed on the dump bed and chassis of the truck with a feedback control for the dynamic lifting system.

Keywords: Truck stability, Truck tip-over prevention systems

Načrtovanje inteligentnega elektronskega sistema za preprečevanje prevrnite smetarskega tovornjaka

Izvleček: Članek predstavlja osnovno idejo uporabe inteligentnega elektronskega sistema z mikrokontrolerjem za prevprečevanje prevrnitve 30 tonskega smetarskega tovornjaka. Namen Sistema je zagotavljanje stabilnosti tovornjaka med odlaganjem smeti. Trije parametric, ki vplivajo na stabilnost vozila med dvigovanjem kesona so vodorovna lega vozila, naklonski kot kesona in hitrost dvigovanja kesona. Inteligenten system preprečevanja prevrnitve je bil razvit in uspešno testiran na osnovi posnetih in analiziranih podatkov večih akcelerometrov in žiroskopov na kesonu in šasiji vozila. Sistem nudi povratne informacije dinamičnemu dvižnemu mehanizmu.

Ključne besede: MOSFET; stabilnost vozila, system preprečevanja prevrnitve vozila

** Corresponding Author's e-mail: clcham@mmu.edu.my*

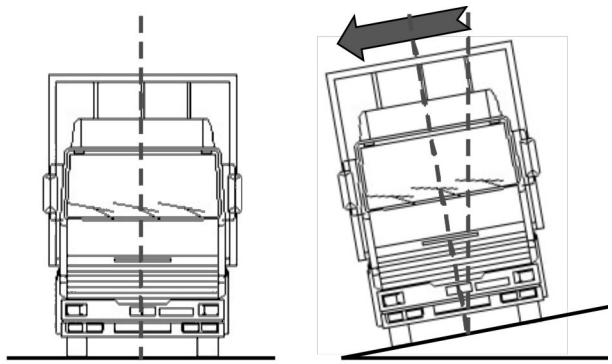
1 Introduction

In developing construction areas, nonlinear soil-structure foundation is a great concern and significantly affects ground stability [1, 2, 5]. The unsaturated soil structure becomes unpredictable, especially during the rainy season. In an earth fill process, lifting a dump bed can cause the weight of a dump truck to shift to the back or tilt to either side of the truck. For instance, if one of the wheels of the truck sinks into the loosely compacted soil structure, the truck chassis will tilt to one side, causing the center of gravity of the rising dump bed to exceed the stability baseline range of the dump truck [9]. This phenomenon causes the dump truck to tip over to the side where the dump bed tilts.

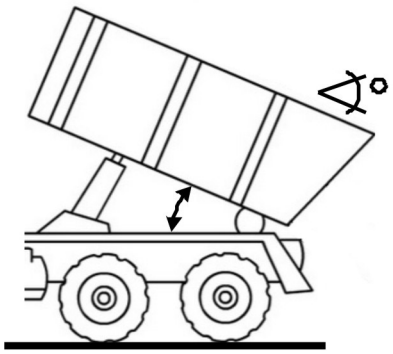
Dump truck tip-over generally happens too fast for the operator to react and unlift the dump bed to a safe range. A tip-over can reach the "point of no return" in approximately 0.5 to 0.75 second and cause the dump truck to flip completely in 1.5 seconds [3,8]. An operator may take 0.5 second to realize that the truck is overturning and another 0.5 second to react to the situation. In other words, the operator takes a whopping 1 second to recognize the hazard and react to it. Given this slow reaction, the 1-second delay makes the disaster unpreventable, which poses a great danger and compromises the safety of any operator of such a machine. Therefore, to enhance the safety scheme and improve the reaction response, an intelligent detection

system is necessary, which could accurately analyze the chassis horizontal position, dump bed tilt angle, and lifting speed so that an immediate response can be taken in motion planning of the lifting mechanism.

To address the aforementioned concern, various studies on dump truck stability have been conducted with the goal of creating a safety scheme during task execution [4, 6, 7]. These schemes provide the operator with a table specifying the maximum angles they can lift the dump bed for a particular chassis tilt angle. The operator refers to the table and estimates the angle independently. These techniques require a manual control system used by skillful operators. Given the hazardous situation in a real construction site, operators may have difficulty in maintaining a standard and consistent performance [10]; thus, research on electronic monitoring and detection systems is essential. In the proposed system, the accelerometer and gyro sensor technology was used to perform chassis lateral position tracking, dump bed tilt angle sensing, and dump bed lifting speed recognition, as shown in Fig. 1.



(a)



(b)

Figure 1: a) Chassis position tracking, b) Dump bed tilt angle sensing.

In this study, the proposed intelligent stability control system consists of four sub-systems: 1, 2, 3, and 4, as shown in Fig. 2. Sub-systems 1 and 2 are the truck chassis lateral position tracking and the dump bed tilt angle measurement systems, respectively. The data collected from sub-systems 1 and 2 are processed by sub-system 3, which is the microcontroller-based data processing system. Sub-system 4 is the dump bed hydraulic shaft controlling system.

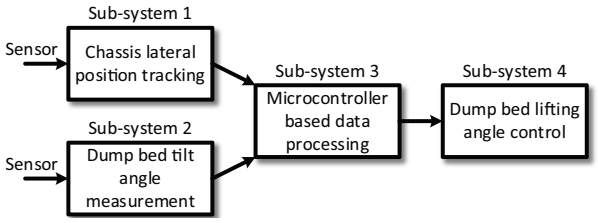


Figure 2: Sub-systems.

Both the truck chassis and dump bed measurement sub-systems are equipped with an accelerometer, gyro sensor, and microcontroller. Every sub-system works independently and performs data sampling, analog-to-digital conversion, and noise filtering. Data collected from sub-systems 1 and 2 are sent to sub-system 3 for processing. After processing, the control signal is fed back to sub-system 4 to control and adjust the speed and direction of the dump bed lifting actuator of the truck accordingly.

2 Measurement of chassis horizontal position, dump bed tilt angle, and lifting speed

The positioning systems examined in this study are as follows:

1. Dump truck chassis positioning – Dump truck chassis position is measured with reference to the initial orientation of the gyro sensor that has been set on flat ground.
2. Dump bed tilting measurement – Relative positioning and incremental positioning. This type of sensing can provide accurate positioning of the dump bed relative to the truck chassis.
3. Lifting speed measurement - Relative positioning

The horizontal position of the truck chassis is determined using a gyro sensor, such that a signal from the gyro sensor is read and compared relative to the ground. Initially, the horizontal position of the chassis should be at planar or near planar condition; then, a set of vector parameters is defined to determine the horizontal position. The lateral position of the chassis is checked before the dump bed is lifted to ensure that it is at the same height and that no tilt occurs. When the dump bed starts to tilt, the center of gravity of the region shifts accordingly; thus, the values of the current

tracking position is compared with the previous tracking values to determine the next tracking position. The forces for each axis component from the accelerometer are given by

$$R_x = \left(\frac{AdcR_x \times \frac{V_{ref}}{value_{\max} - V_{zeroG}}}{sensitivity} \right)$$

$$R_y = \left(\frac{AdcR_y \times \frac{V_{ref}}{value_{\max} - V_{zeroG}}}{sensitivity} \right)$$

$$R_z = \left(\frac{AdcR_z \times \frac{V_{ref}}{value_{\max} - V_{zeroG}}}{sensitivity} \right)$$

where $R_{x,Ry,}$ and R_z are the force vectors in the x, y, and z axes, respectively; *Adc* is the analog-to-digital conversion scheme; *Vref* is the reference voltage; *valuemax* is the maximum value for a particular AD converter; and V_{zeroG} is the reference voltage at zero gravity. The integrations of the gyro sensor and accelerometer are used to improve the dynamic tilt angle detection efficiency. The positioning of the truck chassis and dump bed angle are captured by examining the three-dimensional position of the tracking targets. A high-speed microcontroller is used to calculate the complexity of the dynamic data.

Only the dump bed is supposed to tilt throughout the dump bed lifting process. The horizontal position of the truck chassis should remain unchanged, and the value of the gyro sensor should be maintained at horizontal planar value because no tilting of the truck chassis is allowed. The microcontroller immediately recalculates the chassis angle when the value of the accelerometer varies. The angle can be calculated as follows:

$$A_{xr} = \arccos\left(\frac{R_x}{R}\right) \quad A_{yr} = \arccos\left(\frac{R_y}{R}\right) \quad A_{zr} = \arccos\left(\frac{R_z}{R}\right)$$

where A_{xr}, A_{yr}, and A_{zr} are the angles between the force vector R and the x, y, and z axes. After the movement of the truck chassis is detected and the tilt angle is calculated, sub-system 3 analyzes the situation. The data are then compared with the lifting speed of the dump bed. The dump bed tilting angle and lifting speed can be measured as follows:

$$Rate\ A_{xz} = \frac{\left(Adc\ Gyro_{xz} \times \frac{V_{ref}}{value_{\max} - V_{zero\ rate}} \right)}{sensitivity}$$

$$Rate\ A_{yz} = \frac{\left(Adc\ Gyro_{yz} \times \frac{V_{ref}}{value_{\max} - V_{zero\ rate}} \right)}{sensitivity}$$

where *Rate* A_{xz} and *Rate* A_{yz} are the rotation of projections of the R vector in the XZ and the YZ planes, and $value_{max}$ is the maximum value for a particular AD converter. A control signal is issued to slow down the lifting speed when the tilting of the chassis does not exceed the safety range from the center of gravity. However, when the value touches the boundary of the overturn range, the lifting process must be halted immediately and the delifting process must take over.

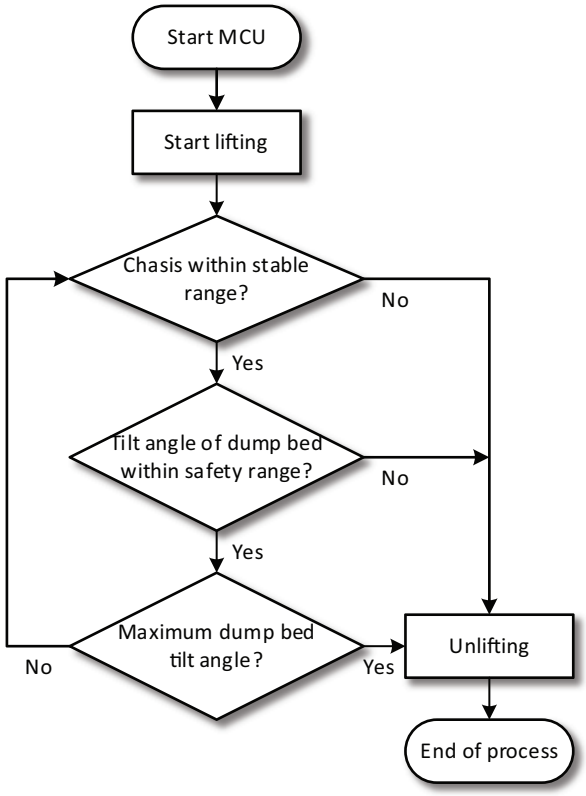


Figure 3: Process flow diagram.

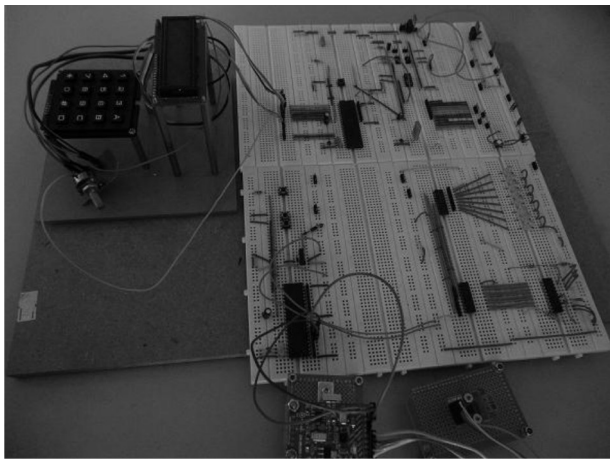


Figure 4: Proof-of-concept implementation.

Figure 4 shows the detailed hardware setup. Reference points are compared with the preset schemes. Based

on the feature error of comparison, the microcontroller generates an error signal and sends the control command to the USB I/O card for interfacing with the hydraulic pump control system. In this theory, several assumptions are made as follows:

1. The hydraulic pump stops instantaneously when the stop command is sent to the hydraulic controller.
2. The vibration of the dump truck is in a known range.
3. The microcontroller response is significantly faster than the gyro sensor response.

3 Tip-over range detection algorithm

Sensor systems must have fault-tolerant and real-time capabilities. A tip-over safety range is derived and shown in Figure 5. The reference load is an 18-tonne weight carried on an 11.9-tonne truck chassis. The stability range is divided into three regions: safety, quasi-safe, and dangerous. The quasi-safe region is where the combination of truck chassis tilt angle and dump bed tilt angle causes the center of gravity to be extremely near to the boundary of the stability baseline of the dump truck. The microcontroller from sub-system 3 analyzes the readings from sub-systems 1 and 2 to determine the stability region of the overall truck position.

According to the proposed scheme, the truck lifting is at its maximum speed, which is 4°/sec, when the truck is in the safe region. When the truck reaches the quasi-safe region, the lifting process is slowed down to 1°/sec. The lifting process is stopped immediately and the delifting process takes over when the truck touches the dangerous cross over line.

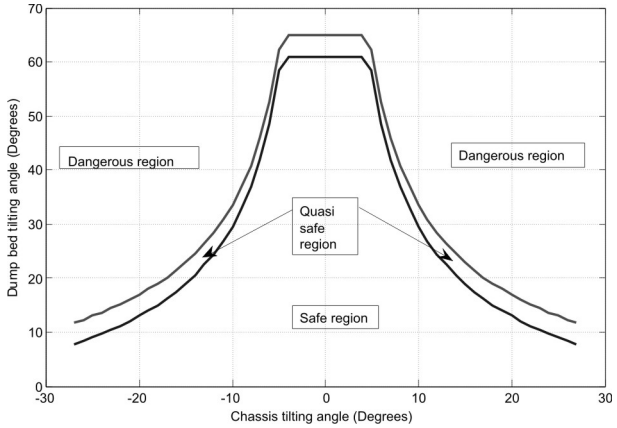


Figure 5: Safe, quasi-safe, and dangerous regions.

4 Implementation of real dump truck system

The lack of commercially available dump truck tip-over electronic sensing and control system motivated this study. Given that operating the dump truck usually involves hazardous conditions, the tip-over prevention system must be able to process real-time input and output data with minimum latency. The data are collected from sub-systems 1 and 2 where the influence of noise is addressed. Sub-system 3 should possess high computational data throughput. The system should be robust and compact enough, as well as efficient, so that it can be attached to the available onboard truck system.

4.1 Electronic circuit design

A low noise gyro sensor with Kalman filtering is selected for the axes sensing part. The model used in our system is the MPU3300-gyroscope from InvenSense, which is equipped with a 16-bit analog-to-digital converter for digitizing the gyroscope outputs. The I^2C protocol is used as the communication protocol among the sensors and microcontroller sub-systems. The following features are embedded in the intelligent detector system for robust control:

- Automatic connection and disconnection
- Estimation of system positions
- Presentation of graphic image on LCD

The output from the detection system is connected to the hydraulic lifting system. To ensure safety, the dump bed lifting process rechecks every sensor when the operator starts the lifting process. If any sensor has malfunctioned, the system triggers an alarm and automatically informs the operator and switches to manual mode.

4.2 Communication protocol among sensors and microcontrollers

A synchronization approach must be applied for designing applications that collect data from the gyro sensors and accelerometers. The combination of such a system allows applications to request data synchronously. A microcontroller management system functions as a master process on the host that connects the sensing sub-systems and a lifting control system together. During the communication, the master and slave can be the receiver and transmitter, and the data transfer can be bi-directional (full duplex). The system clock is independent because each of the sub-systems are self-clocked and synchronized by the falling edge of the master controller. The details of the manager will

be described in another paper; thus, the capabilities of the manager are only listed in this paper as follows:

- Microcontroller node sharing among multiple subcontrollers
- Programming interfaces to access the submicrocontroller systems
- Dynamic network configurations without stopping any application

Figure 6: Implementation on truck.

5 System analysis and performance evaluation

A test area was constructed to evaluate the response of the tip-over prevention system of the truck. In this experiment, the truck chassis is initially set to a certain tilt angle; then, the fully loaded dump bed is lifted and measurements are conducted to observe the maximum angle of the tilting dump bed before the unlifting process. An excavator is used to pile up a slope with a certain tilt angle that mimics the real construction site, and the truck is driven onto the slope. During the testing stage, the entire system performs in automatic mode after the lifting button is pressed by the operator. The operator then leaves the truck to avoid any accident.

The experimental slope is rebuilt for every particular angle. A total of 55 experiments have been conducted. The angles are from –27 degrees to 0 degree and from 0 degree to +27 degrees. The negative degrees indicate that the truck is tilting to the left, whereas the positive degrees indicate that the truck is tilting to the right. The truck chassis tilt angle is increased by 1 degree for each of the subsequent experiments.

The experiment established demonstrates how closely the reaction of the tilt angle of the dump bed correlates to the dump truck chassis position in space. All of the components are integrated into a circuit board and constructed in an onboard embedded system. Two experiments have been conducted to evaluate the system. The first experiment tests the angle at which the dump bed tilting speed slows down upon entering the quasi-safe region. The dump bed lifting speed is initially set to its maximum lifting speed, which is 4°/sec. The dump bed rising speed and angle are monitored and recorded. The output response graph in Figure 7 shows the angle of the dump bed at the point where the lifting speed slows down to 1°/sec. The second experiment is executed in the quasi-safe region, where the dump bed lifting speed is 1°/sec. The second experiment tests the angle at which the dump bed lifting speed changes from 1°/sec to 0°/sec.

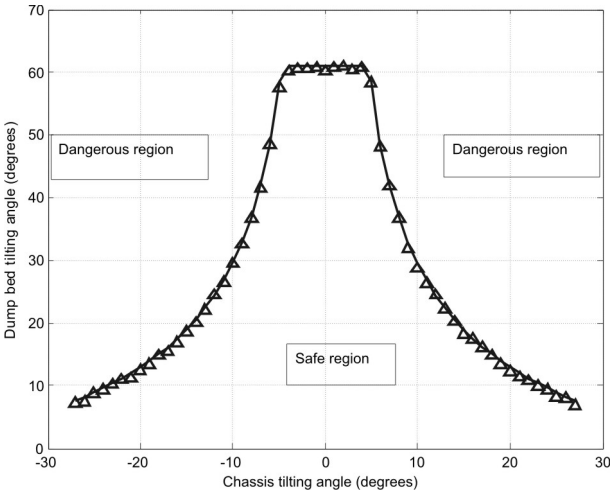


Figure 7: Points at which the rising speed of the dump bed slows down.

The output response graph shows that the real experimental results obtained from the control system of the decrease of dump bed lifting speed match the simulated data from the proposed scheme. This finding indicates that the dump bed lifting mechanism can have a smooth transition from the safe region to the quasi-safe region, which is proven in Figure 8 where the error between the real experimental result and the simulated data is less than 1 degree.

The output response graph shown in Figure 9 indicates that the real experimental results obtained from the dump bed stopping angle are extremely close to the crossing line of the dangerous region from the simulated data. This result shows that the dump bed lifting mechanism can stop efficiently upon reaching the dangerous region as indicated in Figure 10 where the error between the real experimental result and the simulated data is less than 1 degree. Finally, Figure 11 shows both the combination of real experimental results and simulated data.

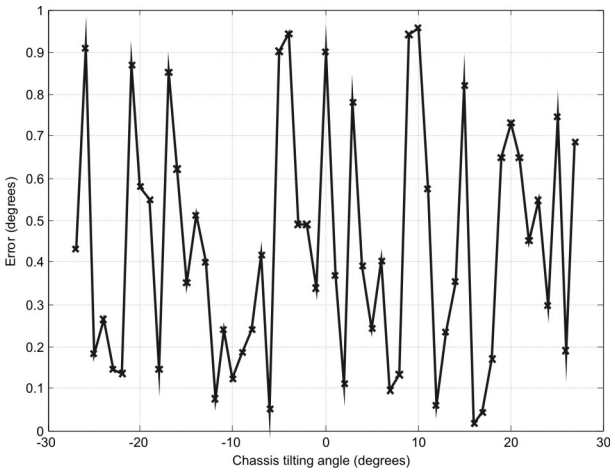


Figure 8: Errors between the experimental and simulated data for rising speed slow-down region of the dump bed.

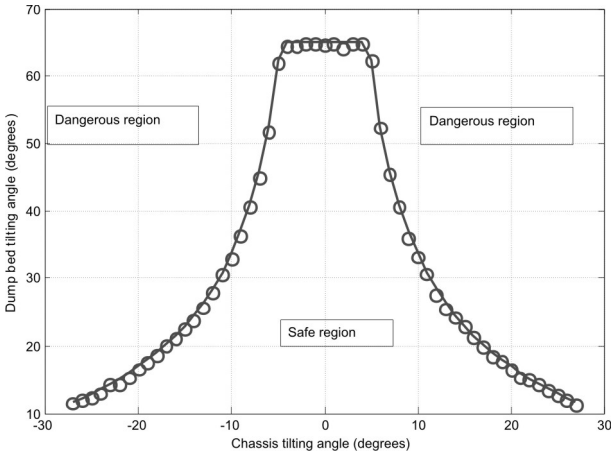


Figure 9: Points at which the dump bed stops rising.

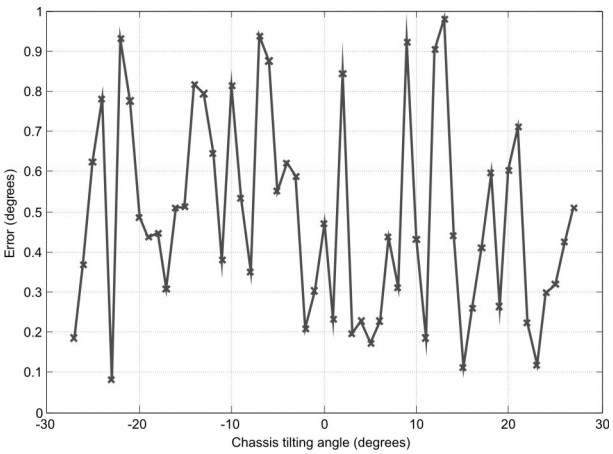


Figure 10: Error between the experimental and simulated data for region where the dump bed stops rising.

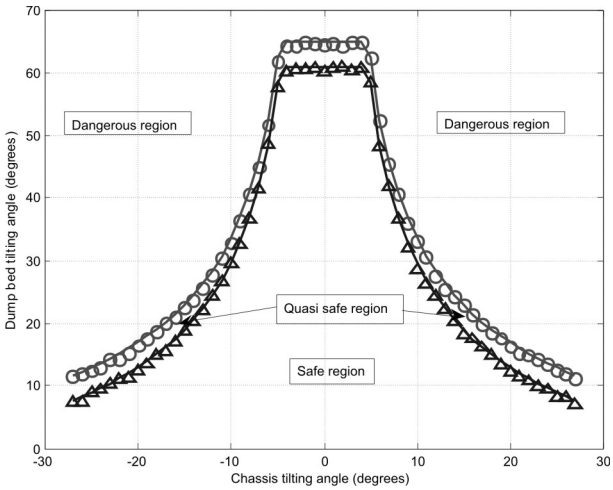


Figure 11: Final response plot for both simulated and experimental data for the region where the speed of the dump bed slows and the dump bed stops rising.

6 Conclusion

An intelligent dump truck tilt-over prevention system is proposed and successfully tested in this study. The system measures the tilt angle of the truck chassis and dump bed. The data are analyzed and used to control the speed of the lifting dump bed and the stopping angle so that the dump bed lifting range is within the safe region. The complete system developed in this project would have a significant effect on the safety of dump truck operators.

7 References:

1. T. P. Yan, "Design of 3201Z-type dump truck's lifting mechanism", Proceedings of Second International Conference on Mechanic Automation and Control Engineering (MACE), Hohhot, Mongolia,pp.1165-1168, 15-17 July 2011.
2. S. Sarata, "Model-based task planning for loading operation in mining", Proceedings of IEEE/RSJ International Conference on Intelligent Robots and systems,Maui, Hawaii, USA, Vol.1, pp. 439-445, 29 Oct-03 Nov 2001.
3. T. P. Yan, "Analysis and design on air controlled hydraulic system about dump truck lifting mechanisms", Proceedings of 2nd International Conference on Artificial Intelligence, Management Science and Electronic Commerce (AIMSEC), Zhengzhou, China, pp. 5405-5408, 8-10 August 2011.
4. J. C. Schroeder and F. W. Fuchs, "Design of a power management for a battery buffer system in an electric lift truck by means of fuzzy control and genetic algorithm," Proceedings of 14th European Conference on Power Electronics and Applications (EPE 2011), Birmingham, UK, pp.1-10, 30 August-1 Sept. 2011.

5. P. Lianggui, "Mechanical design",The seventh edition Beijing Management Institute of Beijing University Press, 2009.
6. Chen, T. Wang, Z. Zhao, J. Shen, D. Zhen, and F. Gu, "The lightweight design of a dump truck frame based on dynamic responses", Proceedings of 18th International Conference on Automation and Computing (ICAC), Loughborough, UK, pp.1-5, 7-8 Sept. 2012.
7. Saito, H. Sugiura, and S. Yuta, "Development of autonomous dump trucks system (HIVACS) in heavy construction sites", Proceedings of International Conference on Robotics and Automation, Nagoya, Japan, Vol.3,pp.2524-2529, 21-27 May 1995.
8. C. Li, H. Chen, Y. Li, and G. Zheng, "Automatic transmission test data acquisition system development based on virtual instrument", Proceedings of 9th International Conference on Electronics Measurement & Instruments (ICEMI), Beijing, China, pp.3-205-3-209, 16-19 Aug. 2009.
9. N. Koyachi and S. Sarata, "Unmanned loading operation by autonomous wheel loader",Proceedings of International Joint Conference on ICCAS-SICE, Fukuoka, Japan, pp.2221-2225, 18-21 Aug. 2009.
10. T. Kitamura and K. Okamoto, "Automated route planning for milk-run transport logistics using model checking", Proceedings of 3rd International Conference on Networking and Computing (ICNC), Okinawa, Japan, pp.240-246, 5-7 Dec 2012.

Arrived: 4.1.2014
Accepted: 10.4.2014

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 44, No. 2 (2014), 159 – 167

Voltage summing current conveyor (VSCC) for oscillator and summing amplifier applications

Sezai Alper Tekin

Department of Industrial Design Engineering, Erciyes University, Kayseri, Turkey

Abstract: In this paper, a voltage summing current conveyor (VSCC) as an active building block for realizing the controlled oscillator and the summing amplifier applications has been presented. The VSCC required low supply voltage as ± 0.5 V consumes low power and has a simple structure. The controlled oscillator has three passive components. The VSCC based oscillator offers using of the grounded capacitors which are suitable for IC implementation, using the less passive components, very good frequency stability and the low voltage operation. In addition, the summing amplifier has been realized using only one VSCC and a grounded passive resistor. The amplifier provides some advantages such as high accuracy and very high input impedance. The performance of the proposed circuit is simulated with SPICE to confirm the presented theory.

Keywords: Current conveyor, oscillator, voltage summing circuit, low-voltage, floating gate MOS

Krmiljen tokovni ojačevalnik za realizacijo oscilatorjev in napetostnih seštevalnikov

Izvleček: V članku je, kot aktivni gradnik, predstavljen krmiljen tokovni ojačevalnik (VSCC) za realizacijo oscilatorjev in napetostnih seštevalnikov. Zahtevana nizka napajalna napetost ± 0.5 V zagotavlja nizko porabo in enostavno zgradbo. Krmiljen oscilator ima tri pasivne elemente. Oscilator na osnov VSCC nudi, ob uporabi ozemljenih kondenzatorjev in manj pasivnih elementov, dobro frekvenčno stabilnost in nizkonapetostno delovanje. Seštevalni ojačevalnik je realiziran le z enim VSCC in ozemljenim pasivnim uporom. Ojačevalnik nudi visoko natančnost in zelo visoko vhodno impedanco. Predlagano vezje je simulirano v SPICE okolju.

Ključne besede: tokovni ojačevalnik, oscilator, napetostni seštevalnik, nizkonapetostno vezje, MOS s plavajočimi vrati

* *Corresponding Author's e-mail: satekin@erciyes.edu.tr*

1 Introduction

In recent years, differential difference current conveyor (DDCC) has been reported [1]. In [2], this circuit has been improved to the differential difference complementary current conveyor (DDCCC) [3]. The differential voltage current conveyor (DVCC) was proposed in [4], which could be realized using a DDCCC (grounding terminal Y_3 of a DDCCC results in a DVCC). Numerous applications employing DVCC and DDCC have been proposed earlier [5-9]. Although there are various circuit topologies using voltage summer [10-13], it has not been shown in any active block using current conveyor implementing only voltage summing. Also, the voltage summing current conveyor can be realized with using DDCC. A current conveyor providing arithmetic operations has already been presented by Kuntman [9]. The linearity range of the circuit has been increased due to the properties of the FGMOS differential pair. However, such a complex circuitry structure has not been required for voltage summing function and also, the circuit has no tunability.

The sinusoidal waveform is an important function in electronics systems. The sinusoidal oscillators are commonly utilized in signal processing circuits, communication, control and measurement systems, etc. Therefore, several sinusoidal oscillators using operational amplifier (Op-Amp) have been introduced in the literature [14, 15]. On the other hand, the op-Amp allows the limited gain-bandwidth product. Thus situated, both the condition of the oscillation (CO) and the oscillation frequency of the oscillators designed using op-Amp are negatively affected. For this reason, these oscillators are not suitable for operating at higher frequencies [16]. Lately, current-mode circuits have been attracted

attention due to having advantages such as wide bandwidth, simple circuit structure, wider dynamic range and low power dissipation [17]. In this context, there are many controllable oscillators with two or more active elements or employing only one active element such as current conveyor (CC), transconductance amplifier (OTA), current differencing transconductance amplifier (CDTA) and differential voltage current conveyor transconductance amplifier (DVCCTA) in the literature [18-22]. It can be seen that the above mentioned performance parameters of the current-mode circuits, especially total power dissipation, have been gone the worse when the more active elements have been used in the designing circuit. Although one active element has been used in design, the circuit structure using as an active element can be included a lot of components. Thus, both using less components and designing at low-voltage have been aimed recently [5, 23].

The summing amplifiers and the difference amplifiers using generally Op-Amp and the current conveyor have been presented in the previous studies [12, 24]. The circuit proposed in 2003 uses only three CCCIIs to realize the functions which are current variable by the bias currents of the conveyors [11]. It is shown that the dynamic range and the linearity of the circuit are not sufficient. Also, it has utilized a high supply voltage as ± 2.5 V. The designed circuits using Op-Amp usually suffers from having lots of passive components and restricted frequency performance of the circuit [16].

In this study, a voltage summing current conveyor (VSCC) for realizing the controlled oscillator and the summing amplifier applications has been presented. Therefore, the purpose of this paper is to introduce a proposed VSCC as a new approach and to show the usability of its applications as a controlled oscillator and a summing amplifier. The VSCC has a simple structure and a good frequency performance. Besides, this circuit required low supply voltage as ± 0.5 V consumes low power. The controlled oscillator has three passive components (one grounded resistor and two grounded capacitors). This oscillator offers using of grounded capacitors which are adorable for IC implementation in a long side eliminating parasitic capacitances, using the less passive components, very good frequency stability and the low voltage operation. Additionally, the summing amplifier has been implemented using merely one VSCC and a grounded passive resistor. The amplifier exhibits high accuracy and very high input impedance. Finally, the functionality of the proposed circuit has been confirmed by the SPICE simulations.

2 Proposed Voltage Summing Current Conveyor

The VSCC is designed by employing floating gate MOS transistors (FGMOS). The symbol and the equivalent circuit of an n-type FGMOS transistor with three inputs are shown in Fig. 1. There are several models to simulate the FGMOS transistors in [25]. The model of the FGMOS used in proposed circuit is based on connecting capacitors in parallel with the resistors as given in [26].

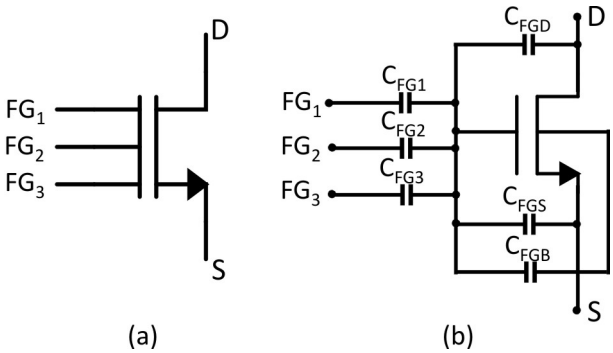


Figure 1: The n-type FGMOS transistor with three inputs a) symbol, b) equivalent circuit

FG_1, FG_2 and FG_3 are the input gate terminals of the FGMOS transistor as displayed in Fig. 1. The input capacitances are C_{FG1}, C_{FG2} and C_{FG3} and the input gates are coupled to floating gate of the FGMOS. C_{FGD}, C_{FGS} and C_{FGB} are the parasitic capacitances between the drain, source, bulk and gate, respectively. Input gate voltages and drain, source and bulk voltages affect an effective floating gate voltage in proportion to value of the coupling capacitances. C_T, sum of all the capacitances between the floating gate and the other terminals can be written as

$$C_T = C_{FGD} + C_{FGS} + C_{FGB} + C_{FG1} + C_{FG2} + C_{FG3} \quad (1)$$

Assumed that the relation shown in Eq.1 is $C_{FGD} + C_{FGS} + C_{FGB} << C_{FG1} + C_{FG2} + C_{FG3}$, then the total capacitance is approximately equal to $C_{FG1} + C_{FG2} + C_{FG3}$. Here, V_{FG} is the effective floating gate voltage and it can be defined as

$$V_{FG} = \frac{C_{FG1}V_{FG1} + C_{FG2}V_{FG2} + C_{FG3}V_{FG3}}{C_T} \quad (2)$$

The drain current I_{DS} of the FGMOS transistor in saturation region is expressed as

$$I_{DS} = \frac{k_n}{2}\left[V_{FG} - V_S - V_{TH}\right]^2 \quad (3)$$

where V_{FG} is the effective floating gate voltage, V_S is the source voltage, I_{DS} is the drain current and V_{TH} is the threshold voltage of the FGMOS transistor. In addition,

kn known as transconductance parameter is $\mu_n .C_{ox}$. (W/L) where μ_n is the electron mobility, C_{ox} is the gate-oxide capacitance per unit area, W/L is the aspect ratio of the FGMOS transistor.

The block diagram of the voltage summing current conveyor as a new approach is demonstrated in Fig. 2.

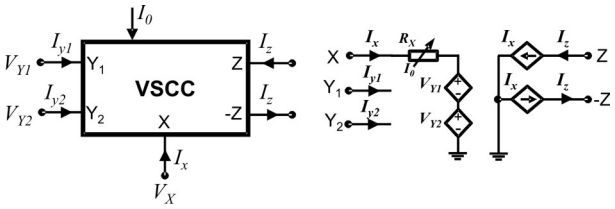


Figure 2: The block diagram and the equivalent circuit of the VSCC.

For the VSCC, Y terminals have high input impedances. The input impedance of the port X is a parasitic resistance and the resistance value can be easily adjusted by bias current I_0 of the VSCC. The Z terminals have high output impedances. The matrix equations of the VSCC are defined as follow:

$$\begin{bmatrix} V_X \\ I_{y1} \\ I_{y2} \\ I_z \end{bmatrix} = \begin{bmatrix} R_X & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \pm 1 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_x \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{bmatrix} \tag{4}$$

The circuit structure of the active block as introduced the FGMOS transistor based VSCC is shown in Fig. 3.

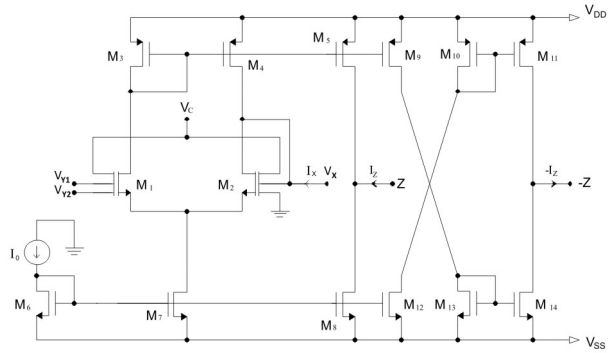


Figure 3: The circuit structure of the VSCC.

In Fig. 3, V_{FGS1} and V_{FGS2} are the floating gate-source voltages terminal for M_1 and M_2 transistors, respectively. The effective floating gate voltages of M_1 and M_2 transistors are V_{FG1} and V_{FG2}. A loop equation written from floating gate of M_2 to floating gate of M_1 transistor can be expressed as

$$V_{FG2} - V_{FGS2} + V_{FGS1} - V_{FG1} = 0 \tag{5}$$

If it is assumed that $C_{FG1} = C_{FG2} = C_{FG3} = C_{FG}$, C_T can be obtained as $3C_{FG}$ shown in Eq. 6. The gate-source voltages in (5) are given as

$$V_{FG1} = \frac{1}{3}\left(V_{Y1} + V_{Y2} + V_C\right)$$
$$V_{FG2} = \frac{1}{3}\left(V_X + V_C\right) \tag{6}$$

where V_C is used for operating the FGMOS transistors at lower voltages. If Eq. 5 is arranged, it can be written as below.

$$V_{FGS2} - V_{FGS1} = \frac{1}{3}\left(V_X - V_{Y1} - V_{Y2}\right) \tag{7}$$

The drain currents of transistors M_1 and M_2 can be written as,

$$I_{D1} = \frac{1}{2}k_n\left(\frac{W}{L}\right)\left(\frac{1}{3}\left(V_{Y1} + V_{Y2} + V_C\right) - V_{TH}\right)^2 \tag{8.a}$$

$$I_{D2} = \frac{1}{2}k_n\left(\frac{W}{L}\right)\left(\frac{1}{3}\left(V_X + V_C\right) - V_{TH}\right)^2 \tag{8.b}$$

I_{D1} and I_{D2} are the drain currents of transistors M_1 and M_2, respectively. $V_X - (V_{Y1}+V_{Y2}) = V_{XY}$. The relationship between input voltages can be calculated as

$$V_{XY} = 3 \cdot \left[\sqrt{\frac{I_0 + I_X}{k_n\left(W/L\right)}} - \sqrt{\frac{I_0 - I_X}{k_n\left(W/L\right)}}\right] \tag{9}$$

where I_0 is the biasing current of the differential pair. From equation (9), current I_X shown in figure 3 can be written as

$$I_X = \frac{1}{3}V_{XY}\sqrt{k_n(W/L)}\sqrt{2I_0 - \frac{1}{2}k_n(W/L)(V_{XY})^2} \tag{10}$$

In equation (10), it is assumed that $2I_0 >> k_n(W/L)(V_{YX})/2$ for a small input voltage. Using this approximation, the output current I_X of the differential pair is obtained as

$$I_X \cong \frac{1}{3}V_{XY}\sqrt{\frac{1}{2}k_n(W/L)}\sqrt{2I_0} \tag{11}$$

From Equation (11), parasitic resistance of the circuit will be expressed as

$$R_x \cong \frac{V_{XY}}{I_X} = \frac{3}{\sqrt{I_0 k_n\left(W/L\right)}} \tag{12}$$

The parasitic resistance is easily controlled by biasing current. It is clear that the electronic tunability of the resistance is presented by this circuit.

3 Simulation results

The proposed VSCC was simulated by SPICE to confirm the theoretical approaches. The SPICE model 0.13 μm TSMC CMOS technology parameter is used for the NMOS and the PMOS transistors. The aspect ratios of the MOS transistors, occurred in the VSCC implementation, are illustrated in Table I. The supply voltage is ±0.5 V. The value of the capacitances shown in Fig. 1 (b) as C_{FG1}, C_{FG2} and C_{FG3} can be taken as 0.07 pF.

Table 1: The aspect ratio of the MOS transistors.

Transistor	W (μm)	L(μm)
M_1, M_2	0.78	0.26
M_3,M_4,M_6,M_7,M_8,M_{10},M_{11},M_{12}	2.6	0.26
M_5,M_9,M_{13},M_{14}	6.24	0.26

Figure 4 displays the changing of the input voltage V_{Y1} versus voltage V_X for the proposed VSCC.

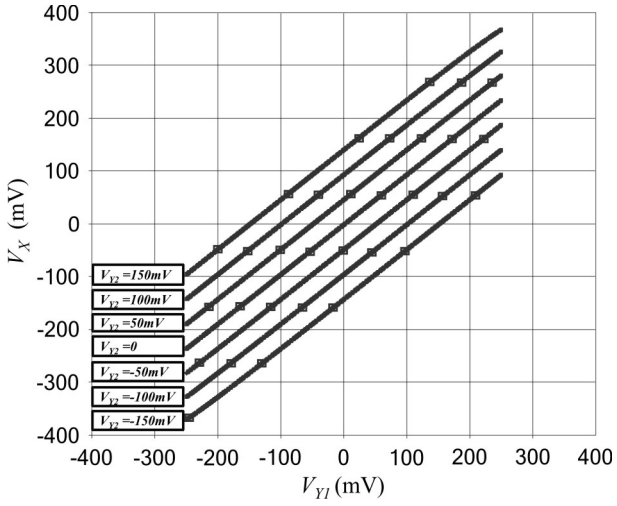


Figure 4: The voltage transfer curve for the VSCC.

The graph has been obtained for the different values of the voltage V_{Y2} as shown in Fig. 4. The curve which has highly linear characterization shows that the voltage transfer gain of the VSCC ($V_X/(V_{Y1}+V_{Y2})$) is equal to 0.99. This value is more satisfactory according to the some designs presented in early studies [27-29]. The changing of the input current I_x versus current I_z for the VSCC is depicted in Fig. 5.

The current gain between terminal X and terminal Z is 0.98. The current transfer curve of the VSCC has almost unity current gain (I_z / I_x). Also, the transfer of current is linear from X to Z node. Figure 6 displays the frequency response for the voltage transfer gain (V_X / V_{Y1}).

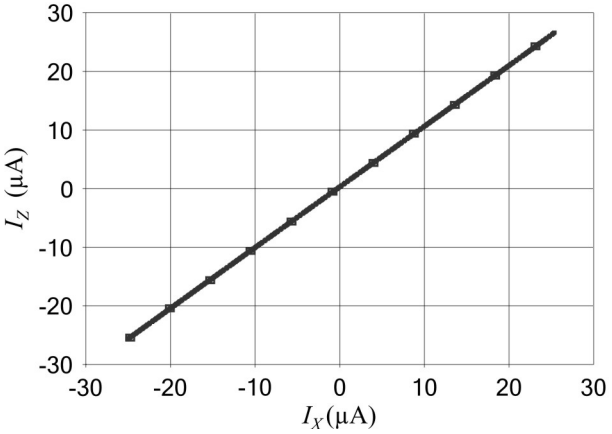


Figure 5: The current transfer curve for the VSCC.

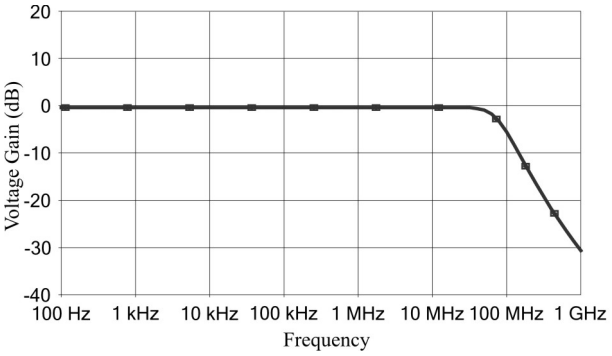


Figure 6: The frequency response of the voltage transfer gain for the proposed circuit.

The frequency response of the VSCC is shown in figure 6 giving bandwidth of 80.1 MHz. The frequency response of the current transfer gain for the VSCC is shown in figure 7. This figure is valid for the all Y terminals having same inputs capacitance values.

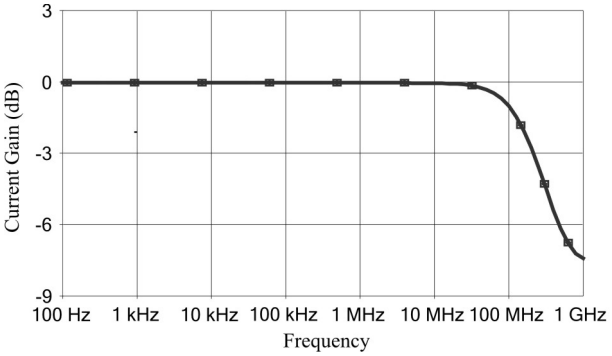


Figure 7: The frequency response of the current transfer gain for the proposed circuit.

The cut-off frequency (-3 dB) is about 211.6 MHz as shown in figure 7. The performance parameters of the VSCC is shown in Table II.

Table 2: The parametric characteristics of the VSCC.

Parameters	Values
Supply voltage	±0.5V
Input voltage range	±300 mV
Output current range	±35µA
Voltage transfer gain ($V_X/(V_{Y1}+V_{Y2})$)	0.99
Current transfer gain (I_Z/I_X)	0.98
3 dB bandwidth I_Z/I_X	211.6 MHz
3 dB bandwidth V_X/V_{Y1}, V_X/V_{Y2}	80.1 MHz
R_X adjustable range (I_0 = 1 µA – 35 µA)	14kΩ-2.1MΩ
Y_1 and Y_2 input resistance	10 GΩ
Z Output resistance	40 MΩ
Power dissipation (I_0 = 25 µA)	61 µW

The parameters of the proposed circuit according to the Table II are reasonable values. The proposed circuit offers some advantages such as described in below.

1. Low-voltage supply requirements about ±500 mV.
2. Low power consumption 61 mW.
3. Acceptable current and voltage gain bandwidth product close to 211.6 MHz and 80.1 MHz, respectively.
4. Electronically tunable intrinsic resistance having wide range.
5. Very high Z-output resistance.
6. Simple circuit design.
7. A new approach which has some advantages.

4 Controlled oscillator based on VSCC

A controlled oscillator based on VSCC shown on Figure 8 is introduced to demonstrate the usability of the proposed VSCC.

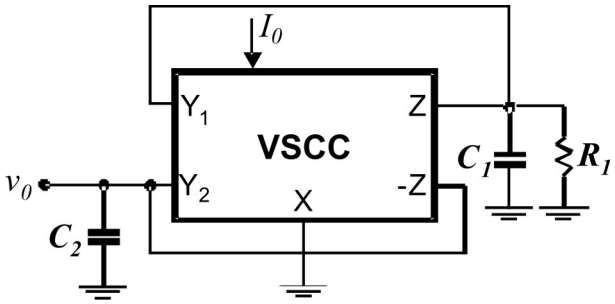


Figure 8: A controlled oscillator based on VSCC.

The circuit consists of single VSCC, one passive resistor and two grounded capacitors. The characteristic equation of the proposed circuit is formulated as below

$$s^2 + s\left(\frac{R_X C_2 + R_1 C_1 - R_1 C_2}{R_X R_1 C_1 C_2}\right) + \frac{1}{R_X R_1 C_1 C_2} = 0 \quad (13)$$

where R_x is the intrinsic resistance of all the current conveyors. From figure 15, input current Iin is equal to current I_2. From equation (11) the oscillation frequency of the oscillator and the condition of oscillation (CO) can be obtained as

$$f_0 = \frac{1}{2\pi\sqrt{R_X R_1 C_1 C_2}} \quad (14)$$

$$CO: \frac{R_1 C_1 + R_X C_2}{R_1 C_2} \leq 1 \quad (15)$$

Taking into consideration both the voltage and the current tracking errors of the current conveyors, $\beta=1-\varepsilon_V$ denotes voltage tracking error from X to the Y terminals; $\alpha=1-\varepsilon_I$ denotes current tracking error from X to the Z terminal where β and α are the voltage and the current transfer gains, respectively and ε_V and ε_I are the voltage and the current transfer errors of the VSCC, respectively. In this situation, the frequency of oscillation can be calculated as

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{\beta\alpha}{R_X R_1 C_1 C_2}} \quad (16)$$

Figure 9 represents the voltage output of the oscillator.

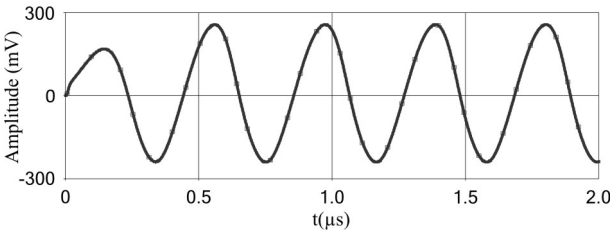


Figure 9: Oscillator output

Controlled oscillator based on VSCC shown in Figure 8 was simulated with the following values for the passive components C_1, C_2 and R_1 are equal to 1 pF, 5 pF and 40 KΩ, respectively, using the value: 25 µA for I_0. Thus, the simulated oscillation frequency value is 2.757 MHz. When this value is theoretically calculated from Eq. 14, the oscillation frequency is obtained as the value of 2.8 MHz. This small difference results from the voltage and the current transfer errors of the VSCC. Figure 10 shows the variation of the oscillation frequency for different biasing currents.

The curves have been obtained both theoretically and simulated using the values: 10, 15, 20, 25, 30 and 35 µA for I_0. The curves shown in Figure 10 exhibit a good coherence with each other. Also, the oscillation frequency between 1.89 MHz and 3.28 MHz is easily controlled by biasing current, and further, total harmonic distortion (THD) of the proposed circuit is less than 2 %.

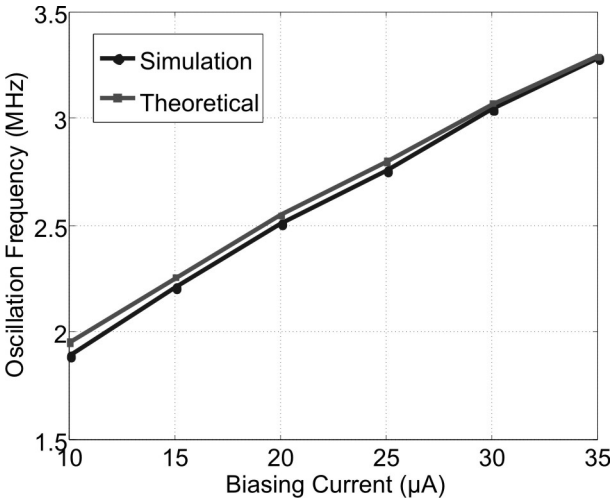


Figure 10: Oscillator frequency versus biasing current.

5 Summing Amplifier

The proposed summing amplifier circuit is shown in Fig. 11. As it is seen from Fig. 2, the circuit whose Port X and Port –Z are connected to each other contains one passive resistor.

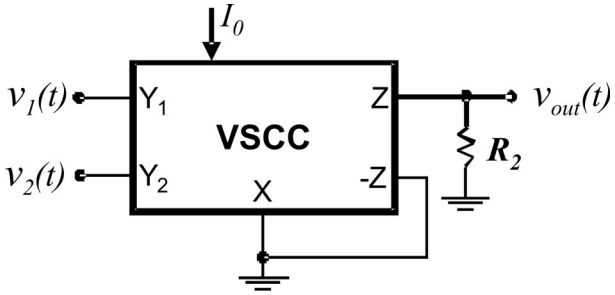


Figure 11: The summing amplifier with two inputs.

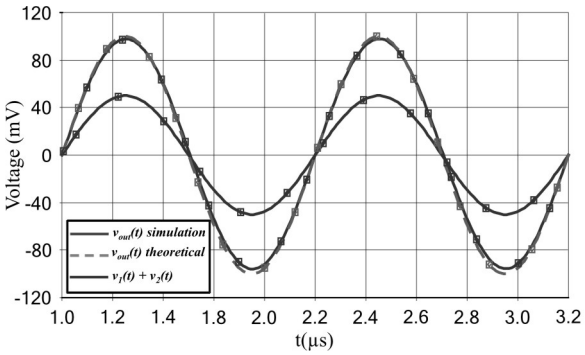


Figure 12: Sinusoidal voltage waveforms for the amplifier.

The transfer function of the summing amplifier shown in Figure 10 is written as,

$$A_V = \frac{v_{out}(t)}{v_1(t)+v_2(t)} = \frac{R_2}{R_x} \quad (17)$$

The simulation of the summing amplifier using VSCC shown in Fig. 10 has been done. Besides, voltage waveforms of the circuit is shown both simulation and theoretical in Fig. 12. The value of the passive resistor is 31 KΩ and the intrinsic resistance R_x is taken as 15.5 KΩ. As shown in Figure 12, voltage $v_1(t)$ and voltage $v_2(t)$ are chosen at 1 MHz 30 mV and 20 mV, respectively.

Sum of the voltages is named $v_{out}(t)$ as shown in Figure 12. On the other hand, the voltage gain of the amplifier can be obtained as 2. The simulation results almost correspond with theoretical results. Maximum error of the gain is about 1 % for $V_{out} = \pm 300$ mV. However, the error of the gain is 0.1 % for -100 mV ≤ V_{out} ≤ +100 mV. Additionally, DC output offset voltage and total power dissipation of the amplifier are 329 μV and 79.8 μW, respectively. The frequency responses of the amplifier for

Table 3: The comparison between this study and the others.

Parameters	This study	[30]	[31]	[32]	[33]
Supply voltage	± 0.5 V	± 1.35 V	± 2.5 V	± 15 V	5 V
Input voltage range	± 250 mV	-2.5 V, + 5.5 V for $V_S^* = +5$ V	NA	± 10 V	NA
Output voltage range	± 300 mV	(+V_S) - 0.35 V (-V_S) + 0.3 V	± 280 mV	± 10 V	NA
DC offset voltage	329 μV	250 μV	25 mV	100 μV	150 mV
Total voltage noise	13.89 nV/√Hz	87 nV/√Hz	NA	60 nV/√Hz	212 nV/√Hz
Power dissipation	79.8 μW	NA	40 mW	NA	1068 mW
Bandwidth	61.3 MHz	800 kHz	NA	1 MHz	20 kHz
Gain Error	1 %	0.1 %	NA	NA	NA
Input impedance	10 GΩ	80 kΩ	NA	1 MΩ	NA
Electronically Tunability	Yes	No	No	No	No

*V_S : Supply voltage

different biasing current are displayed in Figure 13. The biasing current is changed from 20 µA to 30 µA step by step with 5 µA. The cut-off frequencies of the considered amplifier have been obtained as 54.5 MHz, 61.3 MHz and 66.4 MHz for 20 µA, 25 µA and 30 µA, respectively.

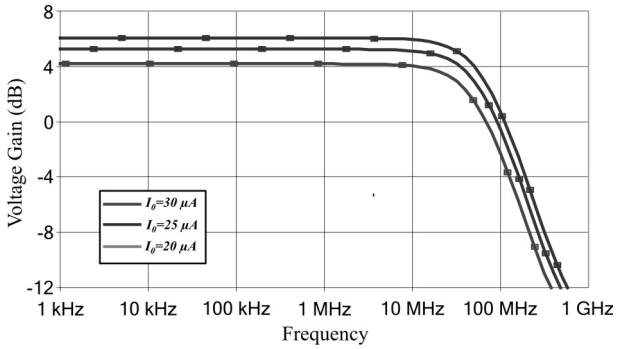


Figure 13: Frequency responses of the amplifier for different biasing current ($V_z/V_{y1}+V_{y2}$).

A noise analysis of the summing amplifier was performed in SPICE. Therefore, with respect to SPICE results, the noise curve belonging to the total output voltage of the amplifier is given in Fig. 14. Total voltage noise of the proposed circuit can be obtained as 13.89 nV/√Hz for I_0=30 µA.

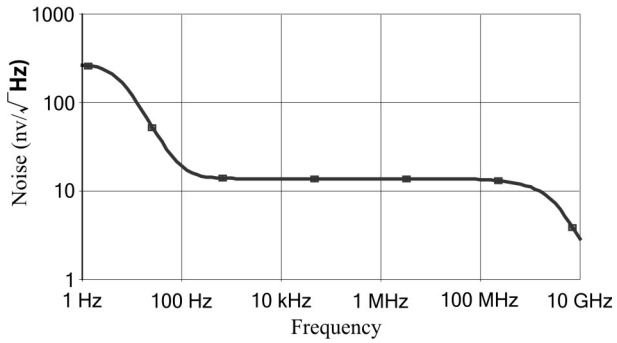


Figure 14: The total output voltage noise versus frequency.

When the literature is investigated, it has been seen that there are a lot of Op-Amp based summing amplifier as an IC structure. Their summing amplifier IC products and proposed amplifier displayed in Table III are compared with each other.

The frequency performance of the presented circuits is restricted as shown in Table III. The circuits have no electronically tunability. Also, these circuits have low input impedance of about KΩs. On the other hand, the proposed amplifier has high input resistance. The obvious advantage is the high input resistance of the proposed circuit reducing the loading on the input signal sources, and therefore affords better signal accuracy and linearity. When the low value input resistors are used, the input leakage currents to the amplifiers significantly are higher than the lowest input signal currents available such that the accuracy of the summing amplifier is not preserved. The multi-input summing amplifier which has four inputs shown in Figure 15 can be given as an example.

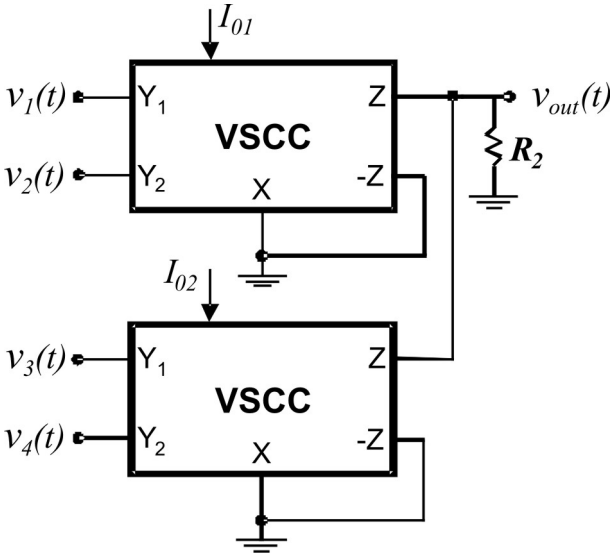


Figure 15: The multi-input summing amplifier.

The voltage output of the circuit can be calculated as below.

$$v_{out}(t) = \frac{R_2}{R_x}\left[v_1(t) + v_2(t) + v_3(t) + v_4(t)\right] \quad (18)$$

The voltage gain of the circuit can be controlled by intrinsic resistance R_x shown in Equation 18. This situation is an important advantage in the electronic circuit design.

6 Conclusion

In this paper, a new approach called voltage summing current conveyor for realizing controlled oscillator and summing amplifier applications has been presented. Simulation results done by SPICE confirm the validity of the theory and demonstrate the use of the VSCC in the controlled oscillator and the summing amplifier applications. FGMOS based the proposed circuit which has highly linear characterization shows that voltage transfer gain and current transfer gain are equal to 0.99 and 0.98, respectively. These values are admirable. Moreover, the frequency responses of the VSCC are acceptable levels. This VSCC is designed in 0.13 µm CMOS process and has ± 0.5 V supply voltage. The linear electronically tunable intrinsic resistance can be tuned for the resistive value from 14 kΩ to 2.1 MΩ. The simulation

results show that this design is powerful sufficient to be utilized in the proposed circuit to achieve low-voltage and low-power. The controlled oscillator used as an application has a stable sinusoidal output. Furthermore, the oscillation frequency value can be controlled by the biasing current. As another application, the summing amplifier having high input resistance and controllable gain has been introduced.

Finally, such an active element is rather proper for low-voltage and low-power IC realizations of which results in decreasing of power consumption. That's why it is clearly shown that the proposed circuit can be used in general electronic circuit design as an active element which has different features such as voltage summing operation.

7 References

1. W. Chiu, S.-I. Liu, H.-W. Tsao and J.-J. Chen, "CMOS differential difference current conveyors and their applications," IEE Proceedings Circuits, Devices and Systems, vol. 143, no. 2, pp. 91–96, 1996.
2. S. S. Gupta, R." Senani, Comments on CMOS differential difference current conveyors and their applications, " IEE Proceedings Circuits, Devices and Systems, vol. 148 no. 6, pp. 335–336, 2001.
3. H. O. Elvan and A. M. Soliman, "Novel CMOS differential voltage current conveyor and its applications," IEE Proceedings Circuits, Devices and Systems, vol. 144, no. 2, pp. 195–200, 1997.
4. S. S. Gupta, R. Senani, "Grounded capacitor currentmode SRCO: Novel application of D V C C C , " IEE Electronics Letters, vol. 36, no. 3, pp. 195–196, 2000.
5. V. Stornelli, G.A. Ferri, "0.18µm CMOS DDCCII for Portable LV-LP Filters," Radioengineering, vol. 22, no. 2, pp. 434 – 439, 2013.
6. M. Kumngern, F. Khateb, K. Dejhan, P. Phasukkit and S. Tungjitkusolmun, "Voltage-Mode Multifunction Biquadratic Filters Using New Ultra-Low-Power Differential Difference Current Conveyors," Radioengineering, vol. 22, no. 2, pp. 448 – 457, 2013.
7. M. S. Ansari and S.A. Rahman, "DVCC-Based Nonlinear Feedback Neural Circuit for Solving System of Linear Equations," Circuits Systems and Signal Processing, vol. 30, no. 5, pp. 1029–1045, 2011.
8. H.-C. Chien, Design and implementation of relaxation generators: new application circuits of the DVCC," International Journal of Electronics, vol. 100, no. 2, pp. 227–244, 2013.
9. S. Keleş and H. H. Kuntman, "A new floating gate MOS universal current conveyor," National Conference on Electrical, Electronics and Computer Engineering, ELECO 2010, Bursa, Turkey, pp. 643–647, 2010.
10. S.I. Liu, "Square-rooting and vector summation circuits using current conveyors," IEE Proc.- Circuits Devices Syst., vol. 142, no. 4, pp. 223–226, 1995.
11. G. Han and E. S´anchez-Sinencio, "CMOS Transconductance Multipliers: A Tutorial," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, vol. 45, no. 12, pp. 1550–1563, 1998.
12. S. Maheshwari, "Active-Only Current Controlled Summing-Difference Amplifiers Using CCCIIs," Active and Passive Electronic Components, vol. 26, no. 4, pp. 231–234, 2003.
13. C. Winstead, N. Nguyen, V.C. Gaudet and C. Schlegel, "Low-Voltage CMOS Circuits for Analog Iterative Decoders," IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 53, no. 4, pp. 829–841, 2006.
14. R. Senani, "On Equivalent Forms of Single Op-Amp Sinusoidal RC Oscillators," IEEE Transactions on Circuits and Systems-I, vol. 41, no.10 , pp. 617–624, 1994.
15. M. T. Darkani and B. B. Bhattacharya, "Generation and Design of Canonic Grounded Capacitor Variable-Frequency RC-Active Oscillators," IEE Proceedings Circuits, Devices and Systems, vol. 132, no. 4, pp. 153–160, 1985.
16. A. Budak, "Passive and Active Network Analysis and Synthesis," Boston, USA: Houghton Mifflin, 1974.
17. C. Toumazou, F. J. Lidjey and D. Haigh, "Analog IC Design: The Current-Mode Approach," UK: Peter Peregrinus, 1990.
18. B. Linares-Barranco,A. Rodriguez-Vazquez,E. Sanchez-Sinencio and J.L. Huertas, "10 MHz CMOS OTA–C Voltage-Controlled Quadrature Oscillator," Electronics Letters, vol.25, no. 12, pp. 198–211, 1989.
19. M. Kumngern, S. Junnapiya, "A Sinusoidal Oscillator Using Translinear Current Conveyors," in Proc. of Asia Pacific Conference On Circuits and Systems, APPCAS2010, Kuala Lumpur, pp. 740–743, 2010.
20. R. Sotner, Z. Hrubos, B. Sevcik, J. Slezak, J. Petrzela and T. Dostal, "An Example of Easy Synthesis of Active Filter and Oscillator Using Signal Flow Graph Modification and Controllable Current Conveyors," Journal of Electrical Engineering, vol. 62, no. 5, pp. 258–266, 2011.
21. W. Tangsrirat and W. Tanjaroen, "Current-Mode Multiphase Sinusoidal Oscillator Using Current Differencing Transconductance Amplifiers," Cir-

cuits Systems & Signal Processing, vol. 27, no.1, pp. 81–93, 2008.
22. A. Lahiri, W. Jaikla and M. Siripruchyanun, "Voltage–Mode Quadrature Sinusoidal Oscillator with Current Tunable Properties," Analog Integrated Circuits and Signal Processing, vol. 65, no. 2, pp. 321– 325, 2010.
23. S.A. Tekin, H. Ercan and M. Alçı, "Novel Low Voltage CMOS Current Controlled Floating Resistor Using Differential Pair," Radioengineering, vol. 22 no. 2, pp. 428 – 433, 2013.
24. D. L. Terrell, "Op Amps: Design, Applications, and Troubleshooting," Elsevier Science, USA, 1996.
25. E. Rodriguez-Villegas, "Low Power and Low Voltage Circuit Design with the FGMOS Transistor," IET Circuits, Devices and Systems Series 20, 2006.
26. L. Yin, S.H.K. Embabi and E. Sa´nchez-Sinencio, "A Floating-Gate MOSFET D/A Converter," Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 409–412, 1997.
27. F. Khateb, N. Khatib and J. Koton, "Novel low voltage ultra-low-power DVCC based on floating gate folded cascade OTA," Microelectronics Journal, vol. 42, no.8, pp. 1010-1017, 2011.
28. H. Ercan and M. Alçı, "A New Design for A BiCMOS Controlled Current Conveyor," Elektronika Ir Elektrotechnika (Journal Electronics and Electrical Engineering), vol.19, no.1, pp.56-60, 2013.
29. B.Calvo, S.Celma, P.A. Martı´nez and M.T. Sanz, "High-speed high-precision CMOS current conveyor," Analog Integrated Circuits and Signal Processing, vol. 36, no.3, pp. 235–238, 2003.
30. INA152 – Single Supply Difference Amplifier, Texas Instruments, http://www.ti.com/lit/ds/sbos184/sbos184.pdf.
31. CXA1821M – RF Amplifier for CD Players, Sony, http://www.sony.net/Products/SC-HP/datasheet/02/data/E94932B36.pdf.
32. SIM980 – 1 MHz Analog Summing Amplifier, Stanford Research Systems (SRS), http://www.thinksrs.com/products/SIM980.htm
33. SA575 – Low Voltage Compandor, ON Semiconductor, http://www.onsemi.com/pub_link/Collateral/SA575-D.PDF.

Arrived: 13. 11. 2013
Accepted: 11. 02. 2014

Professional paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 44, No. 2 (2014), 168 – 173

FPGA-based EtherCAT Microcontroller circuit design of SPI communication for real-time systems

Mingxin Hou[1], Li Jiang[1], Fenglei Ni[1], Minghe Jin[1], Hong Liu[1], Zhaopeng Chen[2]

[1]School of Technology State Key Laboratory of Robotics and System, Harbin Institute of Technology, Harbin, China
[2]Institute of Robotics and Mechatronics, German Aerospace Center, Munich, Germany

Abstract: In this study a novel Microcontroller unit (MCU) circuit based on FPGA for EtherCAT system is presented. The resource utilization statistics of the MCU circuit are provided and the performance of the MCU circuit is analyzed. The first objective is to understand the feasibility of the approach, i.e., whether it is possible for the MCU to drive the EtherCAT slave interface, be reasonable for real-time performance and be stable at different communication SPI frequencies. The second objective is to give the MCU circuit developers some valuable guidelines. Furthermore, it is verified that the proposed MCU circuit based on FPGA is stable, reliable and real-time tested using the online debugging tool SignalTap II.

Keywords: MCU circuit, EtherCAT, SPI, FPGA, online real-time system

FPGA EtherCAT mikrokontroler SPI komunikacij za isteme v realnem času

Izvleček: V študiji je predstavljen novo vezje mikrokontrolne eneote (MCU) na osnovi FPGA za EtherCAT sisteme. Predstavljena je statistika koriščenja MCU vezij ter analiza učinkovitosti MCU vezij. Prva naloga je razumevanje zmožnosti pristopa, npr. ali lahko MCU krmili podrejen EtherCAT vmesnik, je sprejemljiv za sisteme v realnem času, ali je stabilen za različne frekvence SPI komunikacije. Druga namen je ponuditi razvijalcem MCU vezij pomembna vodila. Dokazano je, da je predlagan FPGA mikrokontroler stabilen, zanesljiv in testiran v realnem času z online SignalTap II razhroščevalnim orodjem.

Ključne besede: MCU vezhe, EtherCAT, SPI, FPGA, online sistem v realnem času

** Corresponding Author's e-mail: jiangli01@hit.edu.cn*

1 Introduction

Ethernet for Control Automation Technology (EtherCAT) is an open real-time Ethernet network, which is typical for a transfer of 125 byte over 100 Mbit/s Ethernet [1]. The EtherCAT has many practical applications, which includes industrial robots [2], precision motion control [3-5], real-time networks communication [6-9], etc. As pointed out in [10], the EtherCAT circuit coupler accuracy is 23 ns. This may be associated to the concept of MCU slave circuit delay defined by M. Sung [11], where to be essentially used for the design of EtherCAT communication-based circuit are crucial [12-14].

However, presently most of the research has focused only on the EtherCAT master or slave applications in networks [15, 16]. Much remains to be done to understand and exploit the EtherCAT system design using MCU. For instance, to enable the compliance with real-time requirements as well as to provide data transparent security, the actual communication delay is being considered as a practical problem. If there is no estimated precisely the circuit power consumption, then the suitable power supply for the EtherCAT MCU circuit will be unacceptable in a real situation.

To present the performance and power optimization of the SPI communication used for EtherCAT system, as shown in Fig.1, the EtherCAT system structure is firstly analyzed. The typical process of establishing a communication is initiated by the EtherCAT master by sending a broadcast to the EtherCAT slave, which relies on Ethernet wire. The SPI master block and SPI slave block, which are integrated into the MCU circuit and EtherCAT Slave, take care of the communication as a crucial interface between the field bus(MCU users apply) and the EtherCAT slave application. Furthermore, the power consumption of the EtherCAT user circuit design will be determined by the SPI_CLOCK signal. Therefore, the optimization of the SPI communication will play a critical role in the whole real-time EtherCAT system.

The Field Programmable Gate Array (FPGA) is a programmable digital logic device by software, which has advantages include the ability to re-program in the field to fix bugs, and may include a shorter time to market and lower non-recurring engineering costs [17-20]. To design and evaluate the EtherCAT slave MCU circuit effectively, we choose Altera FPGA (EP3C25F256) as a develop platform, for it is especially useful for complex EtherCAT protocol algorithm [21-24]. High-precision and real-time synchronous operation is important for EtherCAT MCU circuit design. With an EtherCAT-based real-time system, the development of such synchronized operations relies on enough Static Random Access Memory (SRAM). Currently there are various types of SRAM-based schemes in practice [25-27]. We chose SRAM CY7C1380D for the MCU circuit design because it has desirable features for realizing enough memory cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation.

The objective of this research is to provide a novel MCU structure circuit based on FPGA and give some guidelines to the developers who are actively engaged in designing the EtherCAT circuit. This paper will be arranged as follows: Section 2 describes the architecture of the MCU design, and section 3 evaluates the MCU performance. Section 4 presents the real-time characteristics through online experiments. Finally, a conclusion of this paper is addressed in section 5.

2 MCU circuit for EtherCAT

The real-time EtherCAT system is composed of three basic blocks: EtherCAT master block, EtherCAT slave block and MCU circuit [28] (see Fig.1). Moreover, two basic design principles of the MCU circuit are how to communicate with the EtherCAT slave by SPI blocks and what's the MCU circuit Electrical characteristic. Fig. 2 (a) shows a MCU circuit architecture that achieves

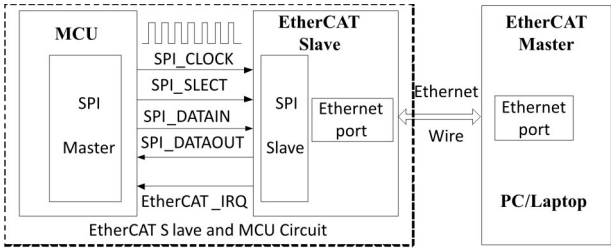


Figure 1: EtherCAT system structure

real-time communication of a cable-driven EtherCAT when opens and runs. The MCU block will be signaled by the EtherCAT AL Event Register using the Process Data Interface (PDI) Interrupt Request signal (SPI_IRQ). For IRQ generation, the AL Event Request register (0x0220:0x0223) is combined with the AL Event Mask register (0x0204:0x0207) using a logical AND operation, then all resulting bits are combined (logical OR) into one interrupt signal. The FPGA PIO core is configured to input ports for capturing the IRQ signal from the EtherCAT slave interface. Whenever the MCU synchronously detects a falling-edge from the IRQ signal, an internal MCU interrupt request should be generated. The SPI logic block of the MCU is synchronous to the clock input provided by SOPC PLL. Meanwhile, the Nios II CPU also shares the same clock with the SPI core. Because the MCU has been configured as a SPI master, the Avalon-MM clock is divided to generate the SPI_Clock. The JTAG UART circuitry is built into the MCU. Therefore, the hosts PC can connect to the MCU using a JTAG download cable by a USB-Blaster. A Tristate Bridge and CY7C1380D SRAM are created into the MCU circuit for large external volatile memory. The CY7C1380D SRAM integrates 524,288 × 36 and 1,048,576 × 18 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for the internal burst operation. 2 M physical memory sizes will make sure that the MCU has enough memory to run the EtherCAT protocol program adequately, reliably and efficiently. The MCU based on Nios II system can use the EPCS device controller to store program code, keep non-volatile program data and manage the MCU configuration data.

To simultaneously achieve good speed and circuit performances, we connect 5 signals to the EtherCAT slave interface: the SPI_Clock, SPI_Slect, SPI_Data_In, SPI_Data_OUT and Interrupt Signal for IRQ generated. From a signal integrity perspective, to ensure the consistency and stability of the SPI data transmission, all the five signal lines should have the same length when laying out the PCB as shown in Fig.2 (b). The architecture of the MCU based on Altera Cyclone III is shown in Fig.2(c), and offers an unprecedented combination of low power, high functionality, and low cost. The architecture consists of up to 120 K vertically arranged logic elements (LEs) and 200 18x18 embedded multipliers.

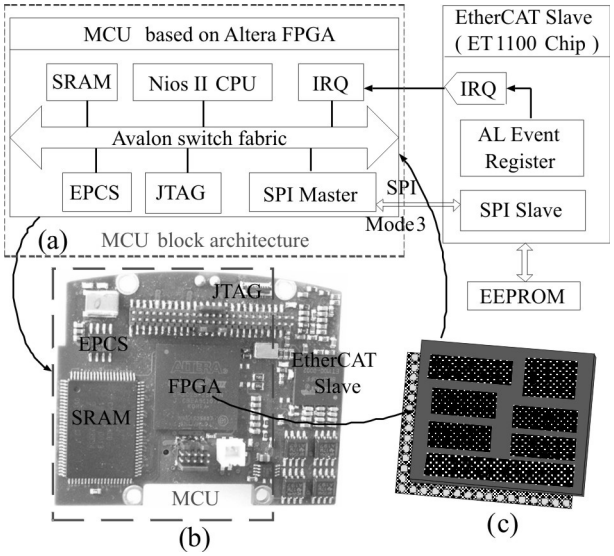


Figure 2: MCU circuit Block Diagram

3 Flow summary and timing specifications

3.1 Flow summary

The MCU circuit based on the Altera Cyclone® III FPGA has been compiled by the Quartus II software platform and these characteristic are reported in Table 1.

Table 1: Accurate MCU based on FPGA compilation resource report

SPI Clock	TR	TMB	DLR	TCF	TLE
1 MHz	2,389	57,600	2,264	2,954	3,542
5 MHz	2,387	57,600	2,262	2,954	3,541
10 MHz	2,386	57,600	2,261	2,958	3,547
15 MHz	2,385	57,600	2,260	2.959	3,548
20 MHz	2,385	57,600	2,260	2,954	3,530
25 MHz	2,384	57,600	2,259	2,939	3,524
30 MHz	2,384	57,600	2,259	2,943	3,535

First, we chose a 1 MHz SPI clock driven by the MCU master to the EtherCAT slave, used it to synchronize the data bit. Total registers (TR) shows a total of 2,389 registers were used. Total memory bits (TMB) illustrate that a total of 57,600 memory bits were used. Total logic elements (TLE) show that a total of 3,542 logic elements were used. Dedicated Logic Registers (DLR) and Total Combinational Functions (TCF) indicated that 2,264 dedicated logic registers and a total of 2,954 combinational functions were used, respectively. Similarly, we get the other SPI clock information which has also been compiled by Quartus II under different rates of frequencies.

Secondly, Table I shows the measured throughput comparison. At 1 MHz the communication between the MCU and EtherCAT slave, the Total Registers column decrease slowly from 2,389 to 2,384 registers. The Dedicated Logic Registers column shows that the data gradually reduces as the SPI clock frequency increases. By contrast, there are no evident consistent tendencies in the columns of the Total Combinational Functions and Total Logic Elements. It is interesting to note that there is no change in the Total Memory Bits no matter the difference in the SPI clock.

3.2 Timing specifications

The MCU circuit is consisted mainly of SPI block, Nios CPU block, external memory block (SRAM), flash block (EPCS), etc (see Fig.2). In order to realize the data communication between the MCU circuit and the EtherCAT Slave chip (ET1100), a reasonable SPI connection mode must be selected synchronously and consistently between the master and the slave side. So, links are established in this case and EtherCAT data communication begins from the master side (MCU circuit) access to the EtherCAT slave registers (EtherCAT slave chip ET1100) by SPI protocol mode 3.

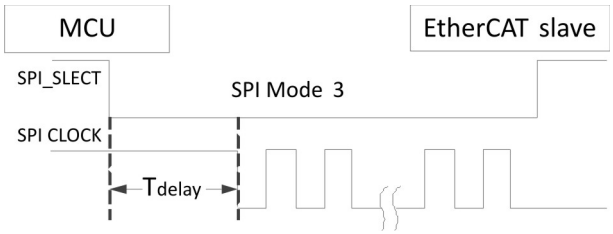


Figure 3: MCU communication time delay

However, the problem of the real-time performance of the MCU circuit is affected by SPI time delay in the case of Fig.3, it is T_{delay}. The rectangles of the MCU and the EtherCAT slave in Fig.3 also correspond to MCU block and EtherCAT slave block in Fig.1. The MCU delay generation logic uses a granularity of half the period of the SPI clock. And the actual delay achieved does not take place during the same time. Instead, it is actually rounded up to the nearest multiple of the falling edge clock, as shown in equation (1) and equation (2).

$$T_{delay} \geq \frac{1}{2}(\text{Period of SPI clock}) \quad (1)$$

$$T_{delay} \leq (\text{Period of SPI clock}) \quad (2)$$

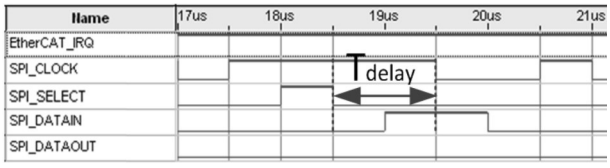
For the SPI master/slave pair must use the same mode to communicate and SPI Mode 3 is selected as the communication between the MCU and the EtherCAT.

Therefore, we setup the Clock Polarity equal to 1, and the Clock Phase equal to 1.

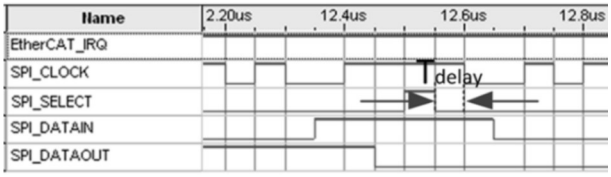
4 MCU circuit for EtherCAT

4.1 Online real-time waveforms

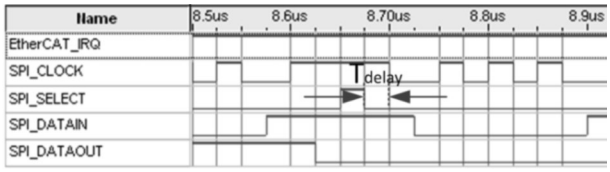
The MCU with online signals generated by a system-on-a-programmable-chip (SOPC) Builder, which is monitored by a SignalTap II, have been shown in Fig.4. By using a SignalTap II Embedded Logic Analyzer (ELA) in the MCU circuit system, we can observe the online behavior of this hardware circuit in real-time operating waveforms more practical than the Quartus II or ModelSim simulation.



(a) 1 MHz MCU circuit SPI clock



(b) 10 MHz MCU circuit SPI clock



(c) 20 MHz MCU circuit SPI clock

Figure 4: MCU circuit online real-time signals by SignalTap II

The MCU transmission clock directly influences the MCU circuit communication speed. Three different frequencies of the SPI clock are observed at 1 MHz, 10 MHz and 20 MHz, respectively, where the five signals are connected to the EtherCAT slave interface: EtherCAT_IRQ, SPI_CLOCK, SPI_SELECT, SPI_DATAIN, and SPI_DATAOUT. The interrupt signal EtherCAT_IRQ is generated by the EtherCAT AL Event register dedicated to the MCU circuit, and typically has low signal polarity. The MCU can synchronously capture the falling edge while an internal interrupt requirement will be generated. The MCU master circuit starts the EtherCAT SPI access by asserting the SPI_SELECT signal and terminates it by taking back the SPI_SELECT, and generally has low signal polarity.

During the communication we tested its online performance. Because the EtherCAT SPI slave device needs additional time for initialization in real situations, the actually maximum time delay (T_{delay}) is about 1 clock cycle. By contrast, the minimum T_{delay} is about half of the clock period. This has been analyzed in section 3.2 and the actual results are exactly the same.

4.2 Electrical characteristics

To maintain the highest possible performance and reliability of the MCU circuit, we must consider the power consumption in a real situation. As depicted in Fig.5, the power consumption of the MCU (µController) circuit grows sharply from 610 mA to 637 mA with the communication SPI clock increases from 1 MHz to 20MHz. It is worth noting that the changing MCU current value is independent of power supply (3.3 V provided). Even so, it only depends on the communication frequency, which is determined by the SPI clock.

Therefore, when starting a new MCU circuit design, the developer could try to follow the two guidelines:

- Choose a suitable DC to DC voltage converter chip, for the absolute maximum output current must be provided.
- Select a satisfactory battery supply, for the power consumption of the MCU circuit clearly rises as the communication clock increase, as shown in Fig.5.

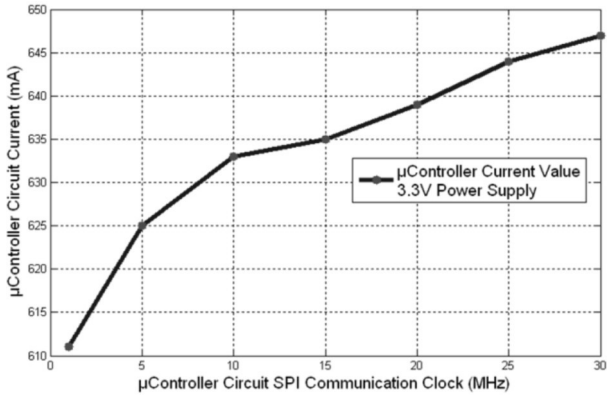


Figure 5: Electricity consumption

5 Conclusions

In this study, our primary objective is to propose the architecture of the MCU circuit block based on FPGA for EtherCAT that are applied in a real-time system. The proposed MCU circuit integrates CPU, SRAM and Flash into the structure in order to investigate its whole behavior under different communication frequencies (1

MHz, 10 MHz and 20 MHz). In particular, the power consumption of the MCU circuit has been tested, which revealed the maximum output current and the tendency for MCU current under corresponding communication frequencies. Furthermore, the technical benefits and practical operation are as follows:

1) MCU circuit block: The EtherCAT MCU circuit can be described as several system blocks, which could be easily found by researchers,
2) Transmission speed: The MCU interface communication speed will be determined by SPI block frequencies. So, the developers could choose the proper SPI clock to satisfy their requirements. However, the maximum communication speed for the EtherCAT MCU is 20 M/S,
3) Power consumption: The procedure allows designers to choose suitable power supply chips conveniently and estimate the battery supply time easily.

The online real-time signals have been captured and displayed by SignalTap II. Meanwhile, the performance of the MCU circuit has been discussed. Furthermore, it was verified that the merits of the MCU circuit performs in real-time and is stabile for EtherCAT technology by online observed experiments under different communication frequencies.

6 Acknowledgments

This work is supported by National Program on Key Basic Research Project of China (973 Program). No.2011CB013306

The authors would thank the reviewers and the editors for their careful review and very helpful comments.

7 References

1. Marco Cereia, Ivan Cibrario Bertolotti, Stefano Scanzio, "Performance of a Real-Time EtherCAT Master Under Linux", IEEE Transactions on Industrial Informatics, vol.7, no. 4, pp. 679-687, 2011.
2. You Wei, Kong Minxiu, Sun Lining, Diao Yanbin, "Control system design for heavy duty industrial robot", Industrial Robot-An International Journal, vol.39, no.4, pp. 365-380, 2012.
3. Kim Kanghee, Sung Minyoung, Jin Hyun-Wook, "Design and Implementation of a Delay-Guaranteed Motor Drive for Precision Motion Control", IEEE Transactions on Industrial Informatics, vol.8, no. 2, pp.351-365, 2012.
4. Vitturi Stefano, Peretti Luca, Seno Lucia, Zigliotto Mauro and Zunino Claudio, "Real-time Ethernet networks for motion control", Computer Standard and Interfaces, vol.33, no.5, pp.465-476, 2011.
5. Kim Jung-Hoon, Lim Sun, Jung Il-Kyun, "EtherCAT based parallel robot control system",Advances in Intelligent Systems and Computing, vol.208, pp.375-382, 2013.
6. Brugger Florian, Kreiner Christian, Thurner Thomas, "Runtime Reconfigurable Communication Concept for Real-Time Measurement and Control", Instrumentation and Measurement Technology Conference, 2012 IEEE International , pp. 2351- 2356, 2012.
7. Toh Chuen Ling, Norum Lars, "A Performance Analysis of Three Potential Control Network for Monitoring and Control in Power Electronics Converter", 2012 IEEE INTERNATIONAL CONFERENCE ON INDUSTRIAL TECHNOLOGY,pp.224-229, 2012.
8. Ju Kyung Leel, Young Hun Song, Suk Lee, Kyung Chang Lee and Young Jin Lee, "Implementation of Multi-axis Smart Driver System via EtherCAT Network based on IEC61800 standard", 2011 11TH INTERNATIONAL CONFERENCE ON CONTROL, AUTOMATION AND SYSTEMS, pp. 1871-1874, 2011.
9. Jansen Dirk, Buttner Holger, "Real-time Ethernet - The EtherCAT solution", COMPUTING AND CONTROL ENGINEERING JOURNAL, 16-21, 2004.
10. Gianluca Cena, Ivan Cibrario Bertolotti, Stefano Scanzio, Adriano Valenzano, Claudio Zunino, "Evaluation of EtherCAT Distributed Clock Performance", IEEE Transactions on Industrial Informatics, vol.8, no.1, pp.20-29. 2012.
11. Minyoung Sung, Ikhwan Kim, Taehyoun Kim, "Toward a Holistic Delay Analysis of EtherCAT Synchronized Control Processes", International Journal of Computers Communications and Control, vol.8, no.4, pp.608-621, 2013.
12. Liu Xiaosheng, Ren Huifen, Zhao Zhenfeng, Zhang Pengyu, "EtherCAT technology for the network of smart substation", 2012 IEEE 7th International Power Electronics and Motion Control Conference, pp.2300-2304, 2012.
13. Park Jee Hun, Lee Suk, Lee Kyung Chang, Lee Yong Jin, "Implementation of IEC61800 based EtherCAT slave module for real-time multi-axis smart driver system", ICCAS 2010 International Conference on Control, Automation and Systems, pp.682-685, 2010.
14. Liu Yanqiang, Song Yongli, "EtherCAT based functional safety integrated communication", International Conference on Automatic Control and Artificial Intelligence, pp. 1005-1008, 2012.
15. Jiang Li, Hou Mingxin, Wei Fanshao, Jin Minghe, Liu Hong, Chen Zhaopeng, "Evaluation of the MCU networks communication for EtherCAT pro-

cess data interface", WSEAS Transactions on Communications, vol.12, no.10, pp. 509-518, 2013.
16. Qi Junyan，Zhao Jianggui, Wang Lei, "Response times evaluation for embedded EtherCAT networks", International Journal of Advancements in Computing Technology, vol. 4, no. 17, pp. 435-442, 2012.
17. Rok Tavčar, Jože Dedič, Drago Bokal, Andrej Žemva, "Transforming the LSTM training algorithm for efficient FPGA-based adaptive control of nonlinear dynamic systems", Informacije MIDEM, Journal of Microelectronics, Electronic Components and Materials, vol.43, no.2, pp.131-138, 2013.
18. Uroš Legat, "On-line Testing and Recovery of Systems on SRAM-based FPGA", Informacije MIDEM, Journal of Microelectronics, Electronic Components and Materials, vol.42, no.3, pp. 144-151, 2012.
19. Thao Tran Phuong, Ohishi Kiyoshi, Yokokura Yuki, et al, "FPGA-Based High-Performance Force Control System With Friction-Free and Noise-Free Force Observation", IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, vol.61, no.2, pp. 994-1008, 2014.
20. Bahri Imen, Idkhajine Lahoucine, Monmasson Eric, et al, "Hardware Software Codesign Guidelines for System on Chip FPGA-Based Sensorless AC Drive Applications", IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS, vol.9, no.4, pp. 2165-2176, 2013.
21. Ristovic Milica, Lubura Slobodan, Jokic Dejan, "Implementation of CORDIC Algorithm on FPGA Altera Cyclone", 2012 20TH TELECOMMUNICATIONS FORUM, pp. 875-878, 2012.
22. Koyuncu Ismail, Ozcerit Ahmet Turan, Pehlivan Ihsan, "An analog circuit design and FPGA-based implementation of the Burke-Shaw chaotic system", OPTOELECTRONICS AND ADVANCED MATERIALS-RAPID COMMUNICATIONS, vol. 7, no. 9, pp. 635-638, 2013.
23. Hace Ales, Franc Marko, "FPGA Implementation of Sliding-Mode-Control Algorithm for Scaled Bilateral Teleoperation", IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS, vol. 9, no. 3, pp. 1291-1300, 2013.
24. Das Joydip, Wilton Steven, "Towards Development of an Analytical Model Relating FPGA Architecture Parameters to Routability",ACM TRANSACTIONS ON RECONFIGURABLE TECHNOLOGY AND SYSTEMS, vol.6, no.2, 2013.
25. Kretzschmar Uli, Astarloa Armando, Jimenez Jaime, et al, "Compact and Fast Fault Injection System for Robustness Measurements on SRAM-Based FPGAs",IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, vol.61, no.5, pp. 2493-2503, 2014.
26. Agrawal Nidhi, Kimura Yoshie, Arghavani Reza, et al, "Impact of Transistor Architecture (Bulk Planar, Trigate on Bulk, Ultrathin-Body Planar SOI) and Material (Silicon or III-V Semiconductor) on Variation for Logic and SRAM Applications", IEEE TRANSACTIONS ON ELECTRON DEVICES, vol.60, no.10, pp.3298-3304, 2013.
27. Okumura Shunsuke, Kagiyama Yuki, Nakata Yohei, et al, "7T SRAM Enabling Low-Energy Instantaneous Block Copy and Its Application to Transactional Memory", IEICE TRANSACTIONS ON FUNDAMENTALS OF ELECTRONICS COMMUNICATIONS AND COMPUTER SCIENCES, vol.E94A, no.12, pp. 2693-2700, 2011.
28. Il-Kyun Jung, Sun Lim, "An EtherCAT based Real-time Centralized Soft Robot Motion Controller", 2012 International Symposium on Instrumentation and Measurement, Sensor Network and Automation, vol.1, pp. 117-120,2012.

Arrived: 05. 12. 2013
Accepted: 09. 02. 2014

Boards of MIDEM *Society* | *Organi društva* MIDEM

MIDEM *Executive Board* | *Izvršilni odbor* MIDEM

President of the MIDEM Society | Predsednik društva MIDEM
Prof. Dr. Marko Topič, University of Ljubljana, Faculty of Electrical Engineering, Slovenia

Vice-presidents | Podpredsednika
Prof. Dr. Barbara Malič, Jožef Stefan Institute, Ljubljana, Slovenia
Dr. Iztok Šorli, MIKROIKS, d. o. o., Ljubljana, Slovenija

Secretary | Tajnik
Olga Zakrajšek, UL, Faculty of Electrical Engineering, Ljubljana, Slovenija

MIDEM Executive Board Members | Člani izvršilnega odbora MIDEM
Prof. Dr. Slavko Amon, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Darko Belavič, In.Medica, d.o.o., Šentjernej, Slovenia
Prof. Dr. Bruno Cvikl, UM, Faculty of Civil Engineering, Maribor, Slovenia
Prof. DDr. Denis Đonlagič, UM, Faculty of Electrical Engineering and Computer Science, Maribor, Slovenia
Prof. Dr. Leszek J. Golonka, Technical University Wroclaw, Poland
Leopold Knez, Iskra TELA d.d., Ljubljana, Slovenia
Dr. Miloš Komac, UL, Faculty of Chemistry and Chemical Technology, Ljubljana, Slovenia
Prof. Dr. Miran Mozetič, Jožef Stefan Institute, Ljubljana, Slovenia
Jožef Perne, Zavod TC SEMTO, Ljubljana, Slovenia
Prof. Dr. Giorgio Pignatel, University of Perugia, Italia
Prof. Dr. Janez Trontelj, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia

Supervisory Board | Nadzorni odbor

Prof. Dr. Franc Smole, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Mag. Andrej Pirih, Iskra-Zaščite, d. o. o. , Ljubljana, Slovenia
Dr. Slavko Bernik, Jožef Stefan Institute, Ljubljana, Slovenia

Court of honour | Častno razsodišče

Emer. Prof. Dr. Jože Furlan, UL, Faculty of Electrical Engineering, Slovenia
Prof. Dr. Radko Osredkar, UL, Faculty of Computer and Information Science, Slovenia
Franc Jan, Kranj, Slovenia

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
ISSN 0352-9045

Publisher / Založnik:
MIDEM Society / Društvo MIDEM
Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia
Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, Ljubljana, Slovenija

www.midem-drustvo.si