NEW INTERPOLATION TECHNIQUE FOR HIGHLY LINEAR CMOS ADC

Shazia Seemi, Mohd Shahiman Sulaiman, Arshad Suhail Farooqui, M.B.I. Reaz

Faculty of Engineering, Multimedia University, Cyberjaya, Malaysia

Key words: CMOS ADC, flash, interpolation, high-speed ADC, data converter

Abstract: A new interpolation technique for high speed ADCs is described. Simple summing differential amplifiers operating in continuous time are used as the interpolator. Incorporated in a 1.3Gsample/s 6-bit CMOS Flash with Interpolation Analog-to-Digital Converter and prototyped on CMOS 0.18-um process, measured results indicated a significant improvement in converter linearity compared to other interpolation techniques.

Nova interpolacijska tehnika za zelo linearne CMOS ADC pretvornike

Kjučne besede: CMOS ADC, flash, interpolacija, hitri ADC, podatkovni pretvornik

Izvleček: V prispevku opišemo novo interpolacijsko tehniko za zelo hitre ADC pretvornike. Kot interpolator uporabimo enostavne diferencijalne operacijske ojačevalnike v realnem času. Vgrajen v 6-bitni CMOS Flash z 1.3Gvzorcev/s in skupaj z ADC pretvornikom izdelan v 0.18um CMOS tehnologiji; meritve pretvornika kažejo bistvene izboljšave v njegovi linearnosti v primerjavi z drugimi interpolacisjkimi tehnikami.

1 Introduction

High speed requirements for ADCs (Analog to Digital Converters) in the fields of data storage and digital communication has led to finding new ways to accomplish high speed without sacrifying dynamic and static performance /1/-/2/. Although Flash Architecture is a good choice for high speed ADCs, it has a large number of input amplifiers. This results in a large input capacitance and high power consumption /3/-/5/. An alternative approach is to use Interpolating architecture that has fewer amplifiers at the input stage /3/. Interpolation can be of two types, current mode or voltage mode. Current mode interpolation is based on the summation of currents reflected through current mirrors with different ratios. It is fast but power hungry and is not very precise due to non-idealities in current mirrors /6/-/7/. Voltage interpolation requires less number of amplifiers, hence, consumes less power. One of the major drawbacks of voltage interpolation is the skew related to the delay from amplifier output to each comparator, i.e. delay from amplifier output to each comparator may not be the same. This delay is primarily due to the series resistance and input capacitance of the comparator. It can be reduced by adding series resistance at the input of the comparator but there could be phase errors when a sinusoidal input is applied. The phase errors degrade comparator's dynamic performance /8/. The interpolation circuit presented in this paper solved the issues faced by voltage-mode interpolation by significantly reducing the delay mismatches and the phase errors and consuming power less than that of a current-mode interpolation circuit. When implemented in a data converter, the circuit demonstrates that the new active/voltage-mode interpolation circuit is capable of working at the frequency before this only achievable by current-mode interpolator and with better linearity performance, compared to the work by /6/,/9/,/11/ and /13/. This circuit would allow more active interpolator to be used in the future to achieve low power consumption and high linearity.

2. Interpolator Cell Architecture

Active interpolation circuit is performed by summing the output currents of two differential pairs into resistive loads.

Figure 1 depicts the circuit diagram of the basic interpolator cell. The two identical differential pairs (M1, M2, M5 and M3, M4, M6) share the same resistive loads R_{L1} and R_{L2}. The small signal current through R_{L1} is equal to the sum of currents flowing through M1 and M3, and the current through R_{L2} is equal to the sum of currents flowing through M2 and M4. The differential output $(Voutp - Voutn)$ is proportional to the sum of differential input voltages

$$(Voutp - Voutn) \propto (Vinp1 - Vinn1) + (Vinp2 - Vinn2)$$

Hence, it is proportional to the average of the input voltages. From small-signal analysis, the interpolator output is given as

$$Voutp - Voutn = \frac{g_m r_o R_l [(Vinp1 - Vinn1) + (Vinp2 - Vinn2)]}{2R_l + r_o + sC_l R_l r_o} \quad (1)$$

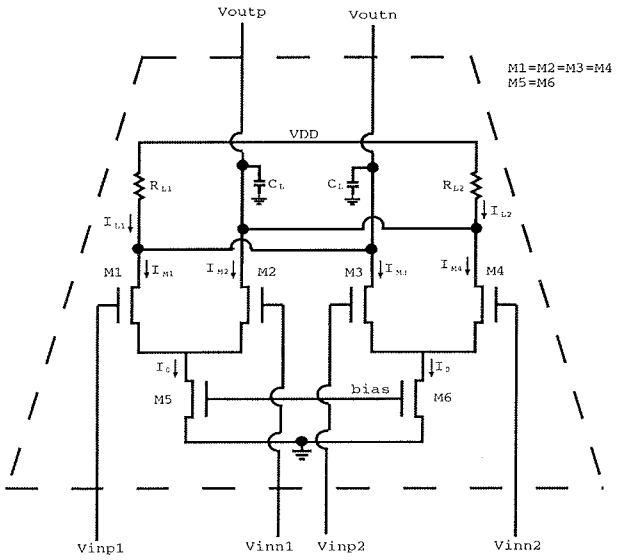

Figure 1: Interpolator Cell

The new interpolation technique is performed by arranging the interpolator cells as illustrated in Figure 2. The signals to be interpolated (IN_{n-1}, IN_n and IN_{n+1}) are fed into the differential inputs of $IAMP_{n-2}$ through $IAMP_{n+2}$. Interpolated outputs are received as OUT_{n-2} through OUT_{n+2}. The input pairs of $IAMP_{n-2}$, $IAMP_n$ and $IAMP_{n+2}$ are connected together. This is done in order to maintain the same common mode at all interpolator cell outputs and to equalize the path delays of interpolated and non-interpolated signals. Averaging resistors (Ravg) are used to reduce the effects of device mismatches, as demonstrated by /9/. Besides that, advanced circuit layout techniques such as gate-aligned and common-centroid are used to ensure device symmetry. The combination of active interpolation based on the new interpolator cell, resistive averaging and symmetrical layout techniques results in uniform path delays and fairly low nonlinearities, hence solving problems commonly faced by voltage interpolator.

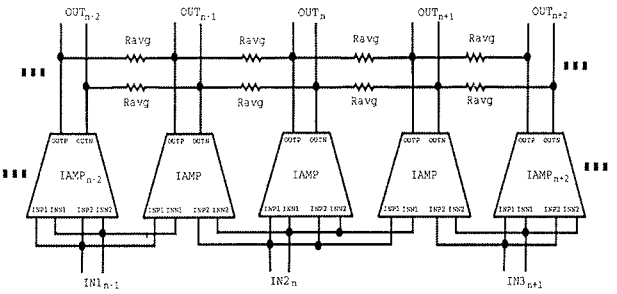

Figure 2: Delay equalization using interpolator cell

3. A 6-bit Interpolating ADC

The proposed interpolation scheme is verified by designing a 1.3Gsample/s 6-bit Interpolation with Flash ADC and prototyped on a CMOS 0.18-um CMOS process. Interpolation is performed by a two-stage 16-to-64 interpolator with resistive terminated averaging. Figure **3** depicts the top segment of the interpolator. Figure 5 shows the ADC block diagram. The averaging and termination resistor values are calculated based on the following formulas

$$R_{avg} = \frac{8}{7} R_L$$

$$R_{trm} = R_{avg} - R_L$$

where

R_L is the load resistor of interpolator cell.

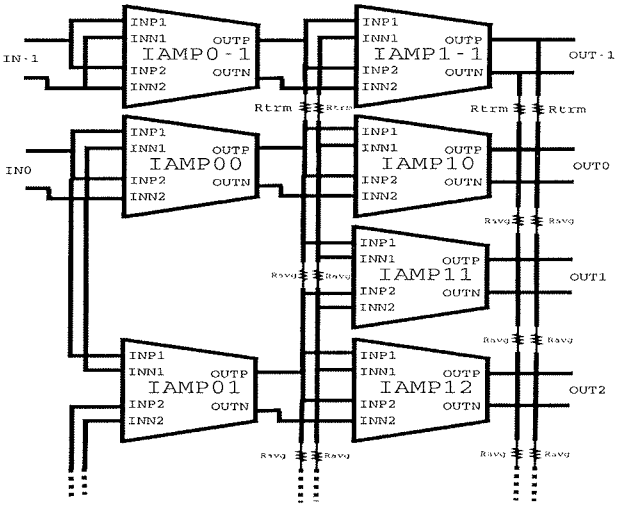

Figure 3: 16-to-64 Interpolator

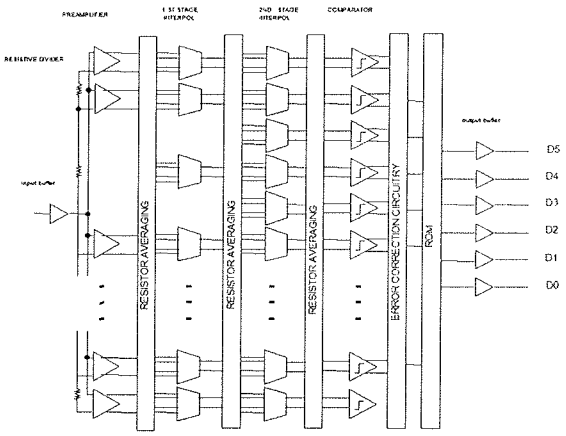

Figure 5: ADC Block Diagram

4. Results and Discussion

The whole ADC was prototyped on CMOS 0.18-um 6-metal 1-poly process, mounted on a 40-pin ceramic package.

The proposed interpolation technique achieves a phase difference of only 0.05° between the interpolated and non-interpolated outputs. This phase difference is significantly lower than 0.45° obtained using resistive interpolation /8/ and other voltage-mode interpolation techniques. The value of INL is ±0.35 LSB at 1.3GSps, which is lower than

other interpolation based designs /6/,/11/. Figure 6 shows a plot of the measured DNL, which varies from +0.15LSB to -0.15LSB. This is the lowest DNL achieved in a CMOS-based high speed ADC (/9/,/12/,/13/) and is certainly the best DNL figure for voltage-mode interpolator. Table 1 compares various types of interpolation with the new technique proposed in this paper. It can be seen that the new technique offers an enormous decrease in pertinent phase delay problem of voltage interpolation. It can also be seen from the table that, the new technique has a better static performance as compared to current interpolation technique.

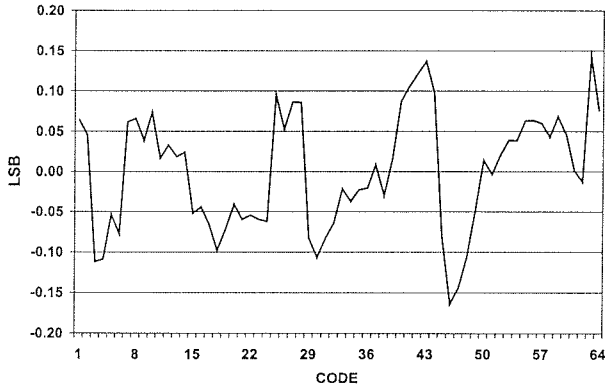

Figure 6: Measured DNL for ADC based on the new Active Interpolation Technique

Table 1 : Comparisons with other Interpolating ADCs

	Voltage	Current	This work
Phase	>=0.45°	<=0.05°	<=0.05°
Delay	>±0.5 LSB	>=±0.4 LSB	±0.15 LSB
DNL	>=±0.5 LSB	>=±1 LSB	±0.35 LSB
INL	Low	High	Low

The whole interpolator for the ADC has a bandwidth of 750 MHz, occupies an active area of 0.13mm^2 and consumes 122-mA current from a 1.8-V power supply. A parametric comparison between this design (ADC using Active Interpolation) and other works is summarized in Table 2.

Table 2 : Performance Comparison of ADCs based on various interpolator circuit

	DNL (LSB)	INL (LSB)	Power (mW)	Process (µm)	Voltage Supply (V)
ADC1300 (This work) 6-bit, 1.3Gsample/s	0.15	0.35	612	0.18	1.8
6-bit 1.3Gsamples/s (Uyttenhove, Steyaert, 2003)	0.42	0.8	600	0.25	1.8 V(A) / 2.5 V(D)
6-bit 1.6Gsamples/s (Scholtens, Vertregt, 2002)	Approx. 0.25	0.42	340	0.18	1.95(A) / 2.35(D)
10-bit, 300Mhz (Kimura, Matsuzawa, 1993)	0.4	1	400	1,bipolar	5.2

5. Conclusion

The new interpolation technique offers extremely low phase delay between the interpolated and the non-interpolated signal, which improves its dynamic performance. At the same time, combination with resistive-averaging network when implemented in an ADC improves the static performance. The ADC's ability to achieve high sampling rate of 1.3Gsample/s while maintaining very low static and dynamic errors makes this interpolation technique suitable for implementation in high speed ADCs.

References

/1/ Sanroku Tsukamoto, William G. Schofield, And Toshiaki Endo, "A CMOS 6-b, 400-MSample/s ADC With Error Correction", IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, December 1998.

/2/ Lauri Sumanen, Mikko Waltari, And Kari A. I. Halonen, "A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter", IEEE Journal of Solid-State Circuits, Vol. 36, No. 7, July 2001.

/3/ Myung-Jun Choe, Bang-Sup Song, And Kantilal Bacrania, "An 8-b 100-Msample/s CMOS Pipelined Folding ADC", IEEE Journal of Solid-State Circuits, Vol. 36, No. 2, February 2001.

/4/ Yunchu Li, And Edgar Sánchez-Sinencio, "A Wide Input Bandwidth 7-bit 300-Msample/s Folding And Current-Mode Interpolating ADC", IEEE Journal of Solid-State Circuits, Vol. 38, No. 8, August 2003.

/5/ Michael P. Flynn, And Ben Sheahan, "A 400-Msample/s, 6-b CMOS Folding And Interpolating ADC", IEEE Journal Of Solid-State Circuits, Vol. 33, No. 12, December 1998.

/6/ M. P. Flynn And D. J. Allstot, "CMOS Folding ADC's With Current Mode Interpolation", ISSCC Dig. Tech. Papers, San Francisco, pp. 274-275, Feb. 1995.

/7/ Ovidiu Carnu, Adrian Leuciuc - "Design Issues For Low-Voltage, High Speed Folding And Interpolating A/D Converters", Proceedings Of MWSCAS 2002, Tulsa, OK, Vol. I, pp. 575-578, 2002.

/8/ Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition, Oxford University Press, 2002.

/9/ Peter Scholtens, Maarten Vertregt, Philips Research Laboratories, Eindhoven, The Netherlands "A 6 Bit 1.6GS/s Flash ADC in 0.18-?m CMOS Using Averaging Termination", IEEE Journal of Solid-State Circuits, Vol. 31, No. 9, September 1996.

/10/ Michael P.Flyn, And David J. Allstot, "CMOS Folding A/D Converters With Current-Mode Interpolation", IEEE Journal of Solid-State Circuits, Vol. 31, No. 9, September 1996.

/11/ Hiroshi Kimura, Akira Matsuzawa, Takashi Nakamura, And Shigeki, Sawada, "A 10-b 300-Mhz Interpolated-Parallel A/D Converter", IEEE Journal Of Solid-State Circuits, Vol. 28, No. 4, pp. 438, April 1993.

/12/ M. Choi And A. Abidi, "A 6-bit 1.3GSamples/s Flash ADC In 0.35ěm CMOS", IEEE Journal Of Solid-State Circuits, Vol. 36, Pp. 1847-1858, Dec. 2001.

/13/ Koen Uyttenhove And Michiel S. J. Steyaert, "A 1.8-V 6-Bit 1.3-GHz Flash ADC in 0.25-µm CMOS", IEEE Journal Of Solid-State Circuits, Vol. 38, Pp. 1115-1118, July 2003.

Shazia Seemi, Mohd Shahiman Sulaiman,
Arshad Suhail Farooqui, M.B.I. Reaz
Faculty of Engineering, Multimedia University,
63100 Cyberjaya, Malaysia

Prispelo (Arrived): 30. 01. 2006; Sprejeto (Accepted): 08. 09. 2006