Professional paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 44, No. 1 (2014), 69 – 74

Delaying analogue quadrature signals in Sin/Cos encoders

Tomaž Dogša, Mitja Solar, Bojan Jarc

University of Maribor, Faculty of Electrical Engineering and Computer Science, Slovenia

Abstract: Various measurement and control systems use magnetic or optical encoders that transform linear displacement and other physical quantities to an analogue quadrature signal. In this paper, we study the problem of, how to accurately delay the analogue quadrature signals in the Sin/Cos encoders within the range of ±10° with the circuit that is potentially integrable on a single chip. Such precision is needed for the efficient phase shift compensation. The typical analogue delay circuit comprises a summing amplifier and a digitally controlled variable resistor that is used to set a delay. We propose a new circuit based on the voltage divider with better linearity and a completely symmetrical range. The design procedure for the delay circuit is also presented.

Keywords: quadrature encoder signals, phase delay, error analysis, delay circuit, analogue quadrature signals.

Zakasnjevanje analognih kvadraturnih signalov v Sin/Cos enkoderjih

Izvleček: Razni krmilni in merilni sistemi uporabljajo optične in magnetne enkoderje, ki pretvarjajo linearni pomik in tudi druge fizične veličine v analogni kvadraturni signal. V tem prispevku objavljamo rezultate raziskave, v kateri smo proučevali problem natančnega zakasnjevanja enega izmed kvadraturnih signalov, ki jih generirajo Sin/Cos enkoderji. Natančnost zakasnitve je pomembna za učinkovito korekcijo faze. Rešitev za zakasnjevanje v območju ±10° smo iskali v obliki vezja, ki je integrabilno. Tipično analogno vezje, ki se uporablja za zakasnjevanje, temelji na seštevalniku, ki vsebuje digitalno krmiljen potenciometer. Z novo strukturo zakasnilnega vezja, ki temelji na napetostnem delilniku, smo dosegli boljšo linearnost in popolnoma simetrično območje. Prikazan je tudi načrtovalski postopek.

Ključne besede: kvadraturni signali, fazna zakasnitev, analiza pogreška, zakasnilno vezje, enkoder.

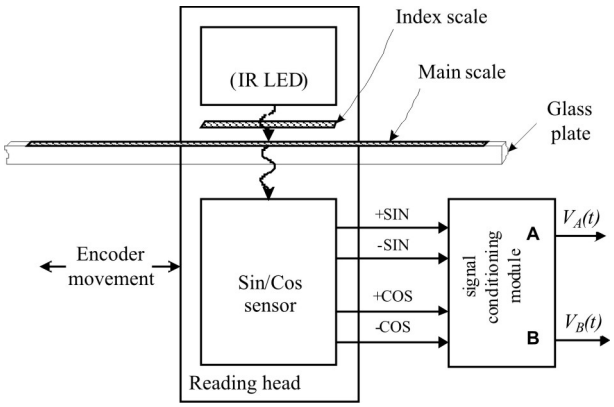
* *Corresponding Author's e-mail: tdogsa@uni-mb.si*

1 Introduction

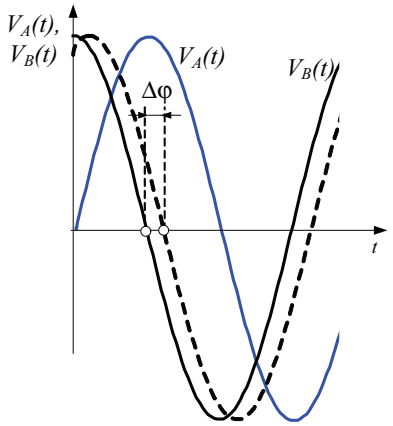
Various measurement and control systems use magnetic or optical encoders that transform linear displacement, the angular position, velocity, and other physical quantities to an analogue quadrature signal. The precision of the system is further improved with the interpolator. The ideal quadrature signals consist of two periodic signals with equal amplitudes and a relative phase shift of 90°. The signals are usually denoted as signal A and signal B or SIN and COS signal (Fig. 1).

Imperfections of encoders and quadrature signals are the major cause of the interpolation error. A method for estimating the accuracy of quadrature output sensors is proposed in [1-2]. The reduction of the imperfections can be performed either in software or implemented with the conditional circuit which is inserted between the output sensors and the interpolator [3]. Authors [4-8] proposed various interpolation algorithms that reduce the imperfections of the signals. These approaches generally require high-precision ADCs and a high-speed DSP to compute the angle to the required resolution. A harmonic distortion reduction achieved by adequate design of a reading-plate is also reported in [9].

All proposed methods are aimed toward the compensation of the imperfections. In this paper, we focus on the problem of how to precisely set the small delay $\Delta\varphi$ of the analogue quadrature signal within the interval (-10°, 10°). Such precision is needed for the efficient phase shift compensation. The most straightforward way to delay an analogue harmonic signal is to use a circuit with at least one reactance as in the analogue



a.



b.

Figure 1: a. Sin/Cos sensor and **b.** the quadrature signals

phase shifter. Yet these solutions are frequency dependent. The second method is based on a trigonometric identity: adding a fraction of signal A to signal B delays a cosine signal. The typical analog delay circuit, based on this idea, comprises a controlled resistor and a summing amplifier [3, 9, 10] In this paper we propose a new circuit that has better linearity and is based on the voltage divider.

This paper is organized as follows. In Section 2, we briefly describe the theoretical aspect of the delaying an analogue orthogonal signal and the structure of the proposed circuit. Example of the design procedure is in Section 3. The experimental version of the proposed circuit was built and the measurements were carried out (Section 4). Finally, the results are summarized in the Conclusion section.

2 Delaying the orthogonal signals

The ideal quadrature signals consist of two periodic signals with equal amplitudes and with a relative phase shift of 90°. The actual signals are harmonically distorted, have unequal amplitudes ($Vs \neq Vc$), have DC offset (V_0) and a phase shift offset ($\Delta\varphi_0$). If the harmonic distortion is neglected then signals can be expressed as

$$V_A(t) = V_s \sin(\omega t) + V_{os} \quad \text{and}$$
$$V_B(t) = V_c \cos(\omega t + \Delta\varphi_0) + V_{oc} \tag{1}$$

It will be assumed that signal B has to be delayed, and the total shift is smaller than 10°

$$|\Delta\varphi_0 + \Delta\varphi| \le \Delta\varphi_{\max}, \quad \Delta\varphi_{\max} = 10^\circ \tag{2}$$

Given is the required phase shift step k_φ and delay interval ($\pm\Delta\varphi_{max}$). Let b denote the control signal. Then the characteristic of an ideal delay circuit is specified by

$$\Delta\varphi(b) = \pm k_\varphi b, \; b = 0, 1, 2 \ldots b_{max} \tag{3}$$

The most straightforward way to delay an analogue harmonic signal is to use a circuit with at least one reactance as in the analogue phase shifter. Yet these solutions are frequency dependent. The second method is based on a trigonometric identity: adding a fraction of signal A to signal B (see Fig. 2) delays a cosine signal.

$$V_{c\_out} \cos(\omega t + \Delta\varphi) = V_c \cos(\omega t) + kV_s \sin(\omega t) \tag{4}$$

where $-1 < k < 1$. Let k_A denote the amplitude imbalance of the signals A and B

$$k_A = \frac{V_s}{V_c} \tag{5}$$

Note that value of the actual amplitude imbalance k_A is not known precisely and may vary within known ranges.

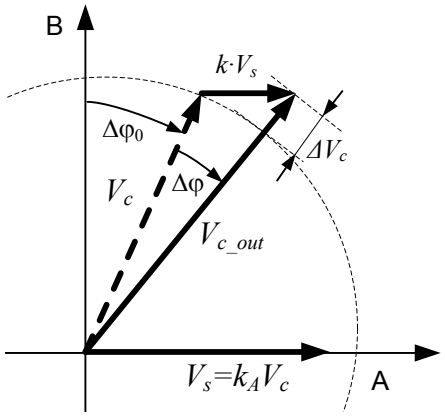


Figure 2: Positive Δφ increases the amplitude of signal B. Note, that amplitudes of real signals are not equal

By applying the trigonometric formulas and considering (5), the resulting delay is given by

$$\Delta\varphi(k,\Delta\varphi_0)=45^\circ-\frac{\Delta\varphi_0}{2}+arctg\left(\frac{(k_Ak-1)}{(k_Ak+1)}\cdot\frac{\cos\Delta\varphi_0}{1+\sin\Delta\varphi_0}\right) \quad (6)$$

Note, that delay does not depend solely on *k*, but also on the phase shift offset $\Delta\varphi_0$ and amplitude imbalance k_A as well. Furthermore, adding the signal B also increases/decreases the amplitude of signal A for ΔV_c (see Fig. 2)

$$V_{c\_out}=\sqrt{(kV_s)^2+(V_c)^2-2kV_sV_c\sin\Delta\varphi_0}=V_c+\Delta V_c \quad (7)$$

If there is no initial phase shift offset ($\Delta\varphi_0$=0°) the equations (7) reduces to

$$V_{c\_out}=V_c/\cos\Delta\varphi\,;\ \Delta\varphi>0 \quad (8)$$

$$V_{c\_out}=V_c\cos\Delta\varphi\,;\ \Delta\varphi<0$$

To set a required delay digitally, *k* in (6) has to be controlled by the digital signal *b*. If $\Delta\varphi_0$ = 0°, the equation (6) simplifies to

$$\Delta\varphi(b)=arctg(k_Ak(b)),\ \ b=0,1,2\ldots b_{max} \quad (9)$$

The relation (9) is approximately linear[1], if *k* is small

$$\Delta\varphi(k)\approx\frac{180}{\pi}k_Ak \quad (10)$$

The required range of *k* is

$$k\approx\pm\frac{\Delta\varphi_{\max}\pi}{180} \quad (11)$$

If $\Delta\varphi_{max}=\pm10°$ is chosen, then the required range of *k* is ±0.1745. The biggest change of the amplitude within this range is ±1.5 %.

Fig. 3 (a) shows typical implementations of the equation (4) [3, 9, 10]. A small amount of signal A is added to signal B using a summing amplifier. A desired fraction of signal A is set by the value of R_d, whereas R_{bs} is needed for setting the step of the delay. The influence of the wiper's resistance[2] R_w (see Fig. 4) and the week linearity are the main disadvantages of this variant. We propose a new circuit based on the voltage divider with better linearity and a completely symmetrical range (Fig. 3(b)). For these reasons we decided to study variant based on the voltage divider.

2.1 Delay circuit

A scheme of the implemented circuit shown in Fig. 3(b) is presented in Fig. 5. A delay is set by digital potentiometer RD. The unity gain amplifier A_5 eliminates the

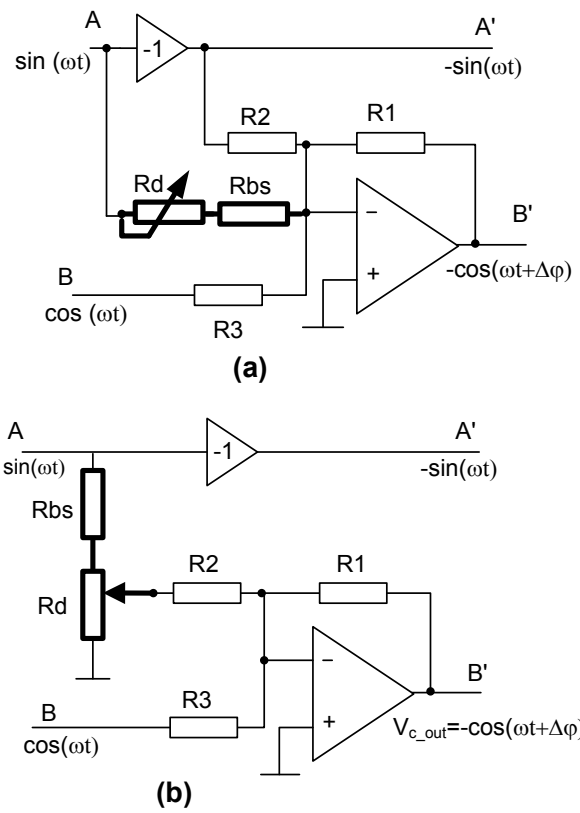


Figure 3: Two possible configurations of the delay circuits

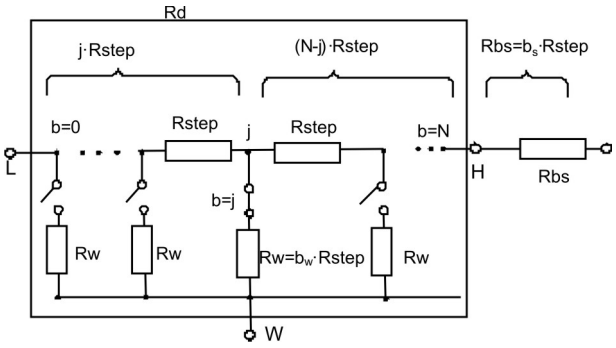


Figure 4: Simplified model of a digital potentiometer R_d with N segments and the additional resistor R_{bs}. R_w is a resistance of the CMOS switch.

influence of the wiper's resistance R_w. All control signals for the digital potentiometers are generated with FPGA module. The fraction of the signal A is added to a signal B by a specially designed summing amplifier A_2. Unity gain amplifiers (A_7, A_6) may be neglected if the output resistance of the sensors is low. Out of the many imperfections only the amplitude imbalance k_A will be considered in the analysis that follows. Since DC offset affects phase shift, all opams should have low offset voltage.

1 $arctg(x)=\left(x-x^3/3+x^5/5-\ldots\right)$

2 *For the 128-tap, 100kW digital potentiometer MAX5439 is Rw = 0.9 ... 2kW*

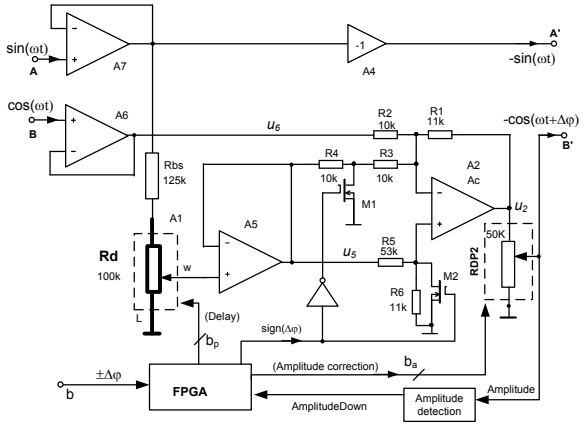


Figure 5: An implemented delay circuit with simple amplitude correction circuit

First, we rewrite the equation (9) into the form

$$\Delta\varphi(b) = arctg\left(k_A A_1(b) A_2\right) \tag{12}$$

where A_2 is a gain of the summing amplifier and $A_1(b)$ is the attenuation of the voltage divider. By applying a model of N-bit digital potentiometer (see Fig. 4), we obtain

$$A_1(b) = \frac{b}{N + b_s} \tag{13}$$

Note that b is in the numerator, which means that A_1 is linearly dependent on b. Let Ac denote the gain u_2/u_6 and A_2 the gain u_2/u_5

$$A_c = u_2 / u_6 = -R1 / R2 \tag{14}$$

The analysis of the circuit gives

$$\begin{aligned} u_2 &= A_c V_c \cos\omega t + A_c k_A A_1(b) V_c \sin\omega t = \\ &= A_c V_c \left(\cos\omega t + k_A A_1(b) \sin\omega t\right) \end{aligned} \tag{15}$$

This proves the correct implementation of the theoretical model (4). Note, that A_c does not affect the phase shift but the amplitude of the delayed signal.

The sign of the delay is controlled by MOS switches M1 and M2. For $\Delta\varphi<0$ is M1 OFF and M2 is ON. If the change of amplitude (8) cannot be tolerated, then the amplitude correction is needed. If the amplification of cos signal, that is defined by ratio R1/R2, is greater that one, then oversized output amplitude can be adjusted with a divider RDP2 that is controlled by the amplitude detection circuit. By choosing R2=R3=R4, we obtain

$$A_2 = \frac{u_2}{u_5} = -\left(\frac{R1}{R3 + R4}\right) = -\frac{A_c}{2} \tag{16}$$

To achieve positive delay the summing amplifier is transformed by the switches M1=ON, M2=OFF to the non-inverting type with the same inverted gain.

$$A_2 = \frac{u_2}{u_5} = +\left(\frac{R6}{R5 + R6}\right)\left(1 + \frac{R1(R2 + R3)}{R2R3}\right) = +\frac{A_c}{2} \tag{17}$$

The equal gain (11) is obtained by the appropriate ratio R6/R5:

$$\frac{R5}{R6} = \frac{2}{A_c} + 3 \tag{18}$$

Note that gains A_1, A_2 and Ac are well defined since they depend on the ratio of resistors. A_c has to be greater than one to ensure that the amplitude of u_2 will always be greater than Vc. This oversized output amplitude of cos signal is reduced to Vc with a divider RDP2 that is controlled by the amplitude detection circuit.

The equation (12) can be rewritten now

$$\Delta\varphi(b) = arctg\left(\frac{k_A}{2}\frac{b}{(N + b_s)}\right) \tag{19}$$

If the amplitude imbalance k_A is unknown then k_A has to be considered as a random variable. In order to reduce the phase error, amplitudes has to be equalized by a special circuit. For small delays is (19) approximately linear

$$\Delta\varphi(b) \approx \frac{180}{\pi}\frac{k_A}{2} \cdot \frac{b}{(N + b_s)} = \Delta\varphi_{step} b \tag{20}$$

By rearranging (18) and setting $\Delta\varphi_{step} \approx k_\varphi$ we can derive a designing rule for R_{bs}

$$R_{bs} = b_s R_{step} = \left(\frac{90 k_A}{\pi k_\varphi} - N\right) R_{step} \tag{21}$$

2.2 Reducing the systematic error due to the nonlinearity

Let $\Delta\varphi_{err\_s}$ denote the systematic error, which is the difference between a measured $\Delta\varphi(b)$ and the target value

$$\Delta\varphi_{err\_s}(b) = \Delta\varphi(b) - k_\varphi b \tag{22}$$

One reason for the $\Delta\varphi_{err\_s}$ is a nonlinear function arctg in (12). If the argument of the arctg follows tg function, then the nonlinearity is eliminated:

$$\begin{aligned} \Delta\varphi(b) &= arctg\left(k_A A_1(b) A_2\right) = \\ &= arctg\left(tg\left(k_A A_1(b) A_2\right)\right) = k_A A_1(b) A_2 \end{aligned} \tag{23}$$

The simplest way to implement this idea is to adequately change the value of the signal b. Let b_p denote modified control signal

$$b_p = b + \Delta b \tag{24}$$

From (23) we can derive a modification rule $b \rightarrow b_p$:

$$b_p = floor\left(0.5 + \frac{2(N+b_s)}{k_A} tg\left(\frac{k_A}{2}\frac{b}{(N+b_s)}\right)\right) \tag{25}$$

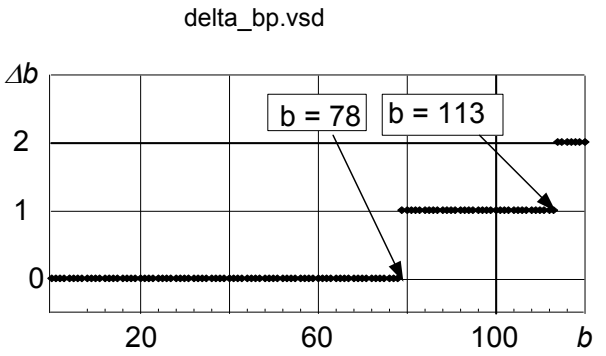


Figure 6: The solution of (25) and (24)

From the solution of (24) and (25) a simple modification rule can be constructed (see Fig. 6). If the range of the control signal is b=1…127, then the rule is

if (b≤78) then $b_p = b$
if (78<b<113) then $b_p = b+1$
if (b≥113) then $b_p = b+2$

Note that the modification rule reduces the range

$$b_{\max} = N - \Delta b_{\max} \tag{26}$$

For example, If $k_\varphi = 0.1°$ and $N = 127$, then the biggest error is $\Delta\varphi_{err\_s} = -0.15°$ (Fig. 7(b)). By using the correction of the signal b, the error is not completely eliminated yet substantially reduced: $-0.06° < \Delta\varphi_{err\_s} < +0.06°$ (see (Fig. 7(a))).

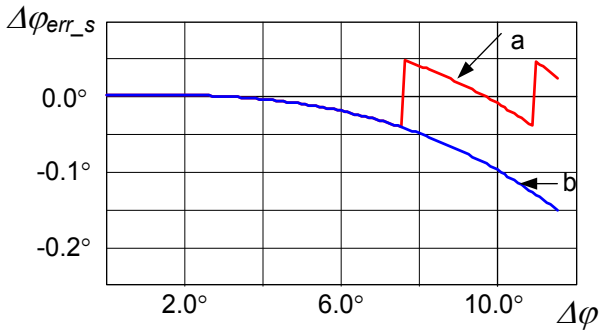


Figure 7: Systematic (linearity) error $\Delta\varphi_{err\_s}$ (Eq. 11, 23 and 25) for $k_\varphi = 0.1°$ and $N = 127$. Amplitudes are equal ($k_A \approx 1$). **a** with linearity correction, **b** without correction

3 Example of the design procedure

Given are: $k_\varphi = 0.1°$, $\Delta\varphi_{max} \leq 10°$, $\Delta\varphi_{min} \geq -10°$, $k_A \approx 1$

128-tap, 100kΩ digital potentiometer MAX5439 was selected for a prototype with discrete components. This means: R_d = 100 kΩ, N=127 and R_{step}=787Ω. If the integrated version were planned then N would be 101. Equation (21) gives b_s = 159 and R_{bs}=125kΩ. A_c was chosen 11/10 and R2=R3=R4=10kΩ. Equations (14) and (18) determine the value of R1=11kΩ and R5/R6=53kΩ/11kΩ. The resulting theoretical characteristics (19) of the delay circuit are:

$$\Delta\varphi(b) = -arctg\left(\frac{b}{572}\right);\ b = 0, 1, 2, \ldots 125$$

$\Delta\varphi_{max}$ = 12.52° , $\Delta\varphi_{min}$ = -12.52° , $|\Delta\varphi_{err\_s}| < 0.06°$, $|\Delta\varphi_{step}| = 0.10°$

4 Measurement results

To estimate a worst-case a SPICE simulator was applied. OPA27 amplifiers and two digital potentiometers (128-Tap MAX5437 and MAX5439) were used in the prototype circuit. The magnetic encoder sensor was replaced by the signal generator that generates almost perfect signals. Each delay was measured 100 times with digital oscilloscope LeCroy LT344. Data for the positive delay[3] are shown in Fig. 8. The signal generator had an offset delay ($\Delta\varphi_{err}(b = 0)$) which was removed in the analysis. The biggest total error $\Delta\varphi_{err}$ = 0.39° was at 10°. Best results were in the range from 0° to 5° where total error was below 0.2°.

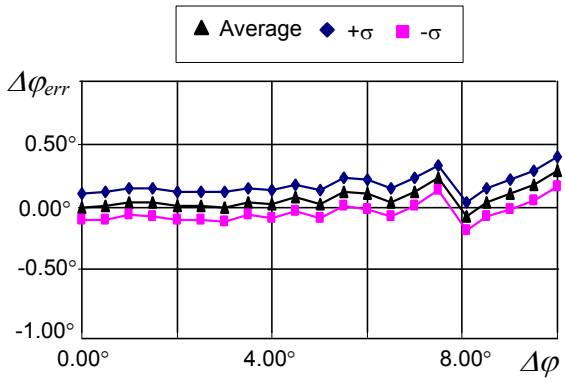


Figure 8: Simulation and actual measurement results (f = 1 kHz)

3 *The negative delay had even better results*

5 Conclusions

In order to achieve a precise delay, low-offset voltage opamps are required and the circuit has to be designed in such a way, that the delay depends only on the ratio of the resistors. The design procedure for the delay circuit was developed: two out of four parameters (N, A_c, k_φ, $\Delta\varphi_{max}$) can be chosen, the other two are calculated. If the signals are perfect and frequency is low, then the precision of the delay is limited only by the systematic error $\Delta\varphi_{err-s}$ and the resistors ratio. In the ideal case the phase step defined by $\Delta\varphi_{step} = \Delta\varphi_{max}/N = 10°/128 = 0.08°$. The actual usable $\Delta\varphi_{step}$ depends on the quality of the signal and on the tolerances as well. To verify the theoretical results the SPICE simulation was applied and a discrete prototype of the delay circuit was built. The prototype shows that with the discrete elements it is possible to obtain the total error below 0.2° in the range from 0° to 5°, if signals are of good quality. To obtain more reliable yield estimation the additional tolerance analysis is needed.

6 References

1. Lin, Q., Li, T., Zhou, Z. (2011). Error Analysis and Compensation of the Orthogonal Magnetic Encoder. *2011 International Conference on Instrumentation, Measurement, Computer, Communication and Control*. doi: 10.1109/IMCCC.2011.12.
2. Denk, D. E. (2008). A method for estimating the accuracy of quadrature output sensors. ISSN 8756-6990, *Optoelectronics, Instrumentation and Data Processing, 44*(2), 105–110.
3. Pleteršek, A. (2001). Integrated optical position microsystem with programmable resolution. *Inf. MIDEM, 31*(4), 281-286.
4. Hieu Tue Le; Hung Van Hoang; Jae Wook Jeon. (2008). Efficient method for correction and interpolation signal of magnetic encoders. *Industrial Informatics, 6th IEEE International Conference on*. Daejeon, 1383-1388.
5. Tan, K. K., Zhou, H. X., Lee, T. H. (2002). New interpolation method for quadrature encoder signals. *IEEE Trans. On Instrument and Measurement*, *51*(5), 1073-1079.
6. Balemi, S. (2005). Automatic Calibration of Sinusoidal Encoder Signals. *Proceedings of IFAC World Congress*, Prague.
7. Hoang, H. V., Jeon, J. W. (2007). Signal Compensation and extraction of High Resolution Position for Sinusoidal Magnetic Encoders. *International Conference on Control, Automation and System*, 1368-1373.
8. Emura, T., Wang, L. (2000). A high-resolution interpolator for incremental encoders based on the quadrature PLL method. *IEEE Trans. Industrial Electronics*, *47* (1), 84 - 90.
9. Rozman, J., Pleteršek, A. (2010). Linear optical encoder system with sinusoidal signal distortion below -60 dB. *IEEE trans. instrum. meas.*, *59* (6), 1544-1549.
10. Yang, C.-J., Kao, C.-F., Chen, Y.-Y., Lin, C.-F., Chen, T.-L. & Ker, M.-D. (2003). ASIC with interpolator for incremental optical encoders. *Proc. 7th Int. Conf. Mechatronics Technology*.
11. Jung, W. G. (2005). *Op Amp Applications Handbook*, Elsevier/Newnes, ISBN 0-7506-7844-5.

Arrived: 03. 10. 2013
Accepted: 08. 01. 2014