MATERIALS FOR DIFFUSION-PATTERNING; THICK-FILM INTERCONNECTIONS TECHNOLOGY

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INVITED PAPER
MIDEM 2002 CONFERENCE
09.10.02 - 11.10.02, Hotel Klub, Lipica

Key words: thick film, materials, diffusion patterning, multilayers, resistors

Abstract: Diffusion patterning is a dielectric patterning technology, which is used in the screen-printed thick-film technology for higher density multilayer circuits. This technology is suitable for producing lower cost multichip modules and requires a low additional investment in conventional thick-film technology production lines. Comparisons of via resolution capability of diffusion patterning versus conventional thick-film technology are described and discussed. Preliminary experimental results obtained with a test circuit showed that 200 µm lines and 200 µm vias could be achieved with acceptable yield and with minimal modification to standard production lines. A few results of an investigation of some thick-film materials, which comprise the "set" of pastes for diffusion patterning technology, are presented. The electronic circuit for the pressure sensor was designed with the advantages of semi-custom ASIC and realised with the verified technology as a low-cost ceramic multichip module.

Materiali za difuzijsko oblikovanje; tehnologija za debeloplastne povezave

Ključne besede: debeloplastna tehnologija, materiali, difuzijsko oblikovanje, večplastna vezja, upori

Izvleček: Difuzijsko oblikovanje je debeloplastna tehnologija, ki z običajno tehniko tiskanja in žganja omogoča izdelavo večplastnih vezij z večjo gostoto komponent. Ta tehnologija je primerna za izdelavo cenejših keramičnih modulov z golimi silicijevimi tabletkami (MCM-multi-chip modules), ker zahteva samo minimalne dodatne investicije k obstoječim linijam za proizvodnjo debeloplastnih hibridnih vezij. V članku primerjamo in ocenimo "sposobnost" resolucije odprtin v dielektriku v večplastnih vezjih v primerjavi s "klasično" debeloplastno tehnologijo. Eksperimentalni rezultati so pokazali, da lahko ponovljivo izdelamo 200 um linije in 200 um odprtine z minimalnimi spremembami obstoječe tehnologije. Predstavljeni so izbrani rezultati testiranja materialov za difuzijsko oblikovanje. Elektronsko vezje za senzor pritiska, ki je bilo izdelano s to tehnologijo, je prikazano kot primer uporabe difuzijskega oblikovanja.

1. Introduction

The density of electronic packaging is increasing due to the requirements for higher performance and smaller size in electronic systems. Since smaller size and lighter weight with lower cost are basic requirements, multi-chip module (MCM) technology is an essential technology to meet these demands. Typical MCMs are realised by using bare dies or dies in chip-scale packaging, because the absence of additional leads provides a shorter interconnection length and higher density. Multilayer interconnections contribute significantly to the reduction of overall dimensions. There are several technologies and materials which enable the realisation of interconnections for multichip modules. The general types of MCM are: high-density glass-epoxy laminated printed-circuit board (MCM-L), thick-film on ceramic substrate (MCM-C), and thin film on ceramic or silicon substrate (MCM-D). Each combination of these technologies and materials offers a different level of performance/cost ratio /1-7/. A ceramic MCM-C can be realised using LTCC

(low-temperature co-fired ceramic), HTCC (high-temperature co-fired ceramic) and thick-film technology, including also photo-patternable and diffusion-patternable technology. An additional contribution to the smaller size and higher density of MCM-C is the ability to integrate screen-printed resistors or sometimes capacitors and inductors. These screen-printed components can be placed either beneath the discrete components on the surface of the multilayer dielectric or be buried (sandwiched) within the multilayer structure /8-11/.

2. Feasibility study

The market for pressure sensors is one of the largest of all sensor technologies, as a consequence the technology and applications of pressure sensors have developed rapidly. The market niche for small and medium enterprises (SMEs) is to develop and produce application-specific sensors integrated in miniature electronic (sensor) modules.

The technology foresight of the HIPOT-HYB Company (which is an SME) is based on a strategic orientation to research, design, develop and produce pressure sensors and hybrid circuits. The competitive advantage of the HIPOT-HYB Company is the use of thick-film technology in sensor applications. This technology is used in two ways, to produce the sensor elements themselves and/or the electronic circuits for signal processing. However, these days the design of new pressure sensors is faced with strict requirements: device size is reducing, functions and performances are expanding; while at the same time the cost of the sensor is restricted. In this respect the developments in sensor technology for small- and medium-volume production have two directions. The first direction is to integrate all or most of the electronic functions into an application-specific integrated circuit (ASIC), the second is to use one of the lower cost high-density interconnection technologies to integrate the sensing element, ASICs and passive components in a sensor module. A multichip module (MCM) is an essential technology to meet these demands.

The special requirements for the mechanical (pressure) sensor application which must be considered:

- Analog and mixed analog-digital functions;
- A low-frequency range from DC up to 10MHz clock in digital applications;
- Low power consumption;
- A small number of electronic components;
- The maximum number of conductive layers is 3 or in some cases 4;
- Restricted external dimensions;
- Mechanical and thermo-mechanical properties suitable for use in mechanical sensor applications;
- Electomagnetic compatibility (EMC) aspect;
- Ecological aspects.

Due to above-listed requirements, and in particular the mechanical and thermo-mechanical properties, the ceramic multichip module (MCM-C) is an essential or at least a "good" technology to meet these demands /12-14/. A ceramic is probably the most common substrate material for pressure sensors, with a silicon die as the sensor element. The reason lies in its physical properties, which include: high compressive strength and hardness; thermal expansion similar to the silicon die and dimensional stability. In some applications high resistance to chemical attack is also important.

The interconnection performance (number of layers, via size and line pitch) of ceramic multichip module technologies for photo-patternable, screen-printed, diffusion-patternable and LTCC technologies is shown in Fig 1 /15/.

3. Diffusion-patterning technology

Thick-film multilayers are made by printing and firing alternate layers of conductors and dielectrics. The dielectric

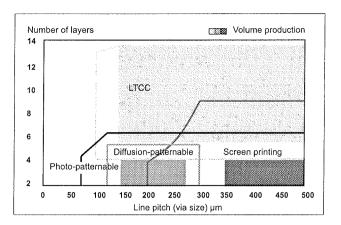


Fig. 1: Interconnection performance of ceramic multichip module technologies /14/.

layer covers the whole area of the substrate. Conductor layers are connected through openings - vias - in the dielectric film. Thick-film pastes are tixotropic; this means that the paste should flow easily when the squeegee pushes it through the screen mesh during screen printing and then "freeze up" in the desired shape on the substrate. However, in the case of multilayer dielectrics, which cover large areas, some compromises are needed. If the multilayer dielectric paste is "stiff", small and well-defined vias can be made. However, small undesirable pinholes could also appear in the layer resulting in short circuits between upper and lower conductor. Therefore the viscosity of the paste should be low enough so that it flows a little after screen printing to "heal", i.e. close up any pinholes. However, this means that vias should be large enough so that they will stay open. This is shown schematically on the left side of Fig. 2. In hybrid circuits production, this limits the dimensions of vias to something like 400x400 um².

Diffusion patterning (Diffusion Patterning is a trademark of the Du Pont company) is a technology, which enables the production of smaller vias with standard thick-film technology /16,17/. For diffusion patterning, a layer of dielectric paste Q-42-DP (DP-diffusion patterning) is screen printed over the whole circuit without vias for connecting lower and upper conductor layers. The relatively low viscosity of the dielectric paste, partly due to a lower inorganic content, results in a smooth film with few or no pinholes. After drying of the dielectric layer, the droplets of diffusing (or image) paste are screen printed on to the dielectric layer. Image paste consists of an organic material and an inert alumina filler. At elevated temperatures this organic material diffuses down into the dried and polymerised organic vehicle of the dielectric. Diffused parts are then washed out with warm water (around 80°C) enabling the "creation" of small round vias. This is shown schematically on the right side of Fig. 2. All further production steps are the same as with standard thick-film materials. Unlike standard vias construction with screen-printing, diffusion patterning vias do not need any extra substrate space. The dimensions of vias are similar to the width of the conductor. It is estimated that complex hybrids can therefore be built on 20% to 40% smaller substrates.

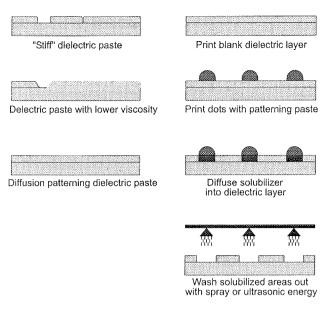


Fig. 2: Vias, realised with standard multilayer dielectric (on the left) and with dielectric for diffusion patterning (on the right) – schematically

The main difference between conventional thick-film multilayer technology and diffusion patterning is an organic part of the multilayer dielectric paste. It is based on a hydrogen bonded acidic acrylic polymer. The active phase in the image paste, which is coloured black for better screen-printed resolution, contains an alkaline organic. During diffusion base and acid materials react and break hydrogen bonds in the acrylic polymer. This results in a reduced green strength of the dielectric layer and enables washing out of the weakened material. The schematics of the diffusion mechanism are shown in Fig. 3 (after Needes et al. /18/).

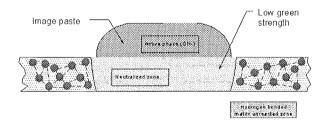


Fig. 3: The schematics of the diffusion mechanism /18/

The diffusion patterning technology is based on high-quality multilayer dielectric material compatible with silver conductors and resistor materials for printing and firing on or under dielectrics. Inorganic material in the Q 42 DP dielectric is the same as in the multilayer dielectric QM42 and is based on the mixture of crystallizable glass and ceramic filler /19/. The silver conductors are used for the inner conductor layers and the Ag/Pd and/or Au are used for the top conductor layer only. Discrete components are added by chip-and-wiring technology and/or with one of the SMT technologies (SMD, Flip-chip,...). Thick-film materials include two resistor series, QM 80 and QM 90, for making resistors on the top of the dielectric layer. Resistors from the QM 80 series are designed for Pd/Ag termi-

nation, while those from the QM 90 series are terminated with silver. /20,21/.

Some features of the diffusion patterning process are:

- Substrate: 96% Al₂O₃
- Multilayer dielectric for diffusion pattering Q42DP
- Image paste Q95IP
- Conductors: Ag (Au, Ag/Pd, Ag/Pt)
- Resistors: 1 ÷ 10 Mohm, on dielectric
- Minimum tracks width: 200 μm (150 μm)
- Minimum tracks separation: 200 μm (150 μm)
- Minimum via diameter: 200 μm (150 μm)
- Minimum crossover area/pitch: 400 μm (300 μm)
- Number of conductor layers: 4
- Size reduction factor (compared to the standard multilayer process): 0.6 ÷ 0.8

4. Diffusion-patterning - materials

In this part of the paper the results of an investigation of some thick-film materials which comprise the "set" of pastes for diffusion-patterning technology will be presented. For microstructural investigation the thick-film materials, printed and fired on alumina ceramics, were mounted in epoxy in cross-sectional orientation and then cut and polished using standard metallographic techniques. A JEOL JSM 5800 scanning electron microscope (SEM) equipped with an energy dispersive X-ray analyser (EDS) was used for overall microstructural and compositional analysis. Prior to analysis in the SEM, the samples were coated with carbon to provide electrical conductivity and to avoid charging effects. The conductive phase in the resistors and the "nature" of ceramic filler in the Q42-DP multilayer dielectric were determined by X-ray powder diffraction analysis (XRD) with a Philips PW 1710 X-ray diffractometer using Cu Kα radiation. X-ray spectra were measured from $2 \Theta = 20^{\circ}$ to $2 \Theta = 70^{\circ}$ in steps of 0.04°.

4.1. Silver-based conductors

QM 14 is a silver conductor for inner-layer interconnections and QM 34 is a via-fill conductor for buried vias and connections to Ag or Pd/Ag upper conducting layers in a multilayer structure. In Figs. 4.a and 4.b microstructures of QM-14 and QM-34 conductors are shown, respectively. Both materials were fired at 850°C. EDS microanalysis showed that both conductors are based on pure silver. The microstructrure of the QM 14 conductor is densely sintered. The diameter of the grains is from a few micrometers to more than ten micrometers. Exaggerated grain growth is due to the firing temperature, which is close to the melting point of silver at 960°C. On the other hand, the microstructure of QM 34 is porous with small grains of approximately one micron in diameter. On the boundaries of the silver grains small particles of secondary phase with

sub-micrometer dimensions are seen. In Fig. 4.b the particles are denoted with arrows. EDS semiquantitative analysis showed the presence of aluminium, silicon and oxygen. This alumosilicate secondary phase is added to inhibit the grain growth and densification during firing. For the via-fill paste it is important that the volume of dried and fired material is similar. In that way the vias stay filled with the conductor "cylinder" and no cracks, due to shrinkage, appear either between the via-fill conductor and the dielectric or the via-fill conductor and the upper and lower conducting layers.

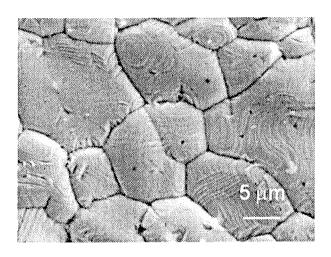


Fig. 4.a: The microstructure of silver-based conductor QM-14, fired 10 min. at 850°C.

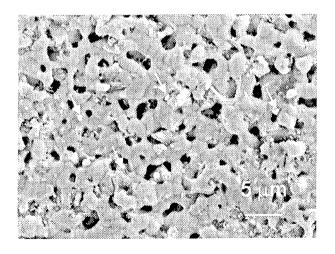


Fig. 4.b: The microstructure of silver-based via-fill conductor QM-34, fired 10 min. at 850°C.

4.2. QM-42 DP dielectric

The inorganic material in the Q 42 DP dielectric is based on a mixture of crystalizable glass and ceramic filler /19/. Fig. 5 shows the cross-section of a thick-film resistor (QM-93), fired on the top of the prefired dielectric layer. The microstructure of the dielectric is dense, with a few small, closed pores. The dielectric is densely sintered. The main elements, detected by EDS microanalysis in the dielec-

tric, are Si, Al, Zn, Ba and Zr. A small amount of cobalt, presumably added for blue colouring, was also detected. The black grains imbedded in the dielectric matrix are alumina particles, added as the ceramic filler.

XRD analysis confirmed that the ceramic filler in the Q42-DP dielectric is alumina. The X-ray spectrum of Q42-DP is shown in Fig. 6. Al₂O₃ peaks are denoted "A". Peaks of another crystalline phase, presumably SiZrO₄ (JCPDS file 83-1383), are denoted by an asterisk.

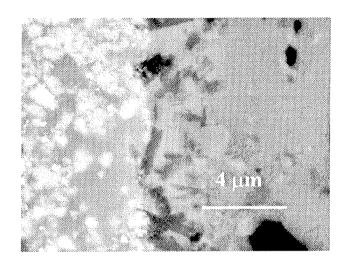


Fig.5: The microstructure of the interface between the resistor QM-93 and the Q42-DP dielectric. The dielectric is on the right.

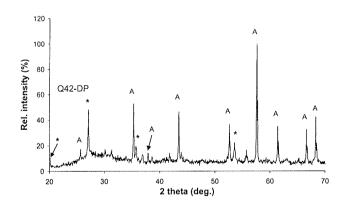


Fig. 6: X-ray spectrum of Q42-DP dielectric. Al₂O₃ and (presumably) SiZrO₄ peaks are denoted by "A" and by asterisk, respectively.

4.3. QM-80 and QM-90 resistors

As mentioned before, the Du Pont resistor series QM-80 and QM-90 are designed for firing on a prefired multilayer dielectric layer instead of on the surface of alumina substrates /19,21/. The resistors, made with QM 80 and QM 90 series, are intended for termination with palladium-silver and silver conductors, respectively. X-ray spectra of 1 and 10 kohm/sq. members of both series, fired at 850°C, are shown in Fig. 7.a (QM-83 and QM-93) and Fig. 7.b

(QM-84 and QM-94), respectively. The conductive phase in both 1 kohm/sq. resistors is a mixture of RuO₂ and ruthenate. For resistors with higher sheet resistivities, from 10 kohm/sq. up, only ruthenate was detected by X-ray analysis. Energy-dispersive X-ray quantitative analysis (EDX) indicated the presence of bismuth together with ruthenium. Therefore it is presumed that the ruthenate phase is Bi₂Ru₂O₇ or (Bi_{1-x}Pb_x)RuO_{7-y}.

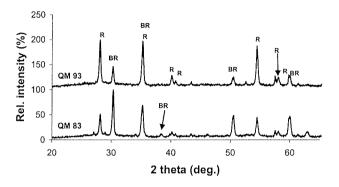


Fig. 7.a: X-ray spectra of 1 kohm/ sq. QM 83 and QM 93 resistors. RuO₂ is denoted R and ruthenate phase is denoted BR.

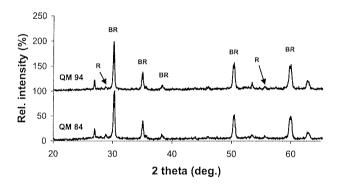


Fig. 7.b: X-ray spectra of 10 kohm/ sq. QM 83 and QM 93 resistors. Ruthenate phase is denoted BR.

Some of the measured electrical characteristics of QM-90 and QM-90 series resistors will be presented. A more complete evaluation of QM-90 resistors, fired also under a dielectric as buried resistive components within a multilayer structure, is reported in /23/.

Resistors were printed and fired on prefired QM-42 DP dielectric. QM-80 and QM-90 resistors were terminated with Pd/Ag-based QM-21 and Ag-based QM-14 conductors, respectively. Sheet resistivities as a function of temperature were measured. Cold (from -25°C to 25°C) and hot (from 25°C to 125°C) TCRs (temperature coefficient of resistivity) were calculated from resistivity measurements at -25°C, 25°C and 125°C. Current noise was measured in dB on 100 mW loaded resistors by the Quan Tech method (Quan Tech Model 315-C). Gauge factors (GF) (the ratio of the relative change in resistance and the strain) were measured by the changes in resistivity as a function of substrate deformation with the simple device described in

/24/. The results are presented un Table 1. TCRs of resistors, fired on the Q42 –DP dielectric, are, as stated by Du Pont, under 100x10⁻⁶/K. Noise indices and GFs increase with increasing sheet resistivity.

Table 1: Nominal sheet resistivities, cold (-25°C to 25°C) and hot (25°C to 125°C) TCRs, noise indices and gauge factors of the resistors

Resistor	Nominal sheet resistivity (ohm/sq.)		Hot TCR (x10 ⁻⁶ /K)	Noise (dB)	GF
QM-83	1 k	30	70	-18,3	4,5
QM-93	1 k	-55	-5	-21,2	4,0
QM-84	10 k	-5	50	-15,8	11,0
QM-94	10 k	20	75	-17,3	10,0
QM-85	100 k	30	75	-3,4	13,5
QM-95	100 k	35	75	-4,2	13,0

5. Diffusion patterning - experimental results

Based on the technical study and preliminary research /25/ the experimental work was designed to establish the necessary technological knowledge for the successful design and manufacture of multichip modules using diffusion-patterning technology. Two test patterns for the evaluation of diffusion-patterning materials and technology, presented in Figs. 8.a and 8.b, were designed. The first test pattern /26/ was intended for estimating the technological window (the dependence of vias and conductor lines' dimensions on, for example, drying temperature, washing out of the image paste, firing cycle etc.). The second test pattern /27/ was designed to evaluate the possibility of making differently shaped structures as well as specially designed thick-film resistors in a multilayer structure.

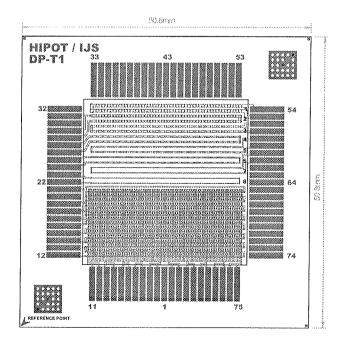


Fig. 8.a: Test pattern for estimation of the technological window of diffusion-patterning technology

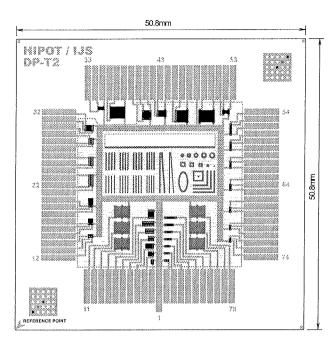


Fig. 8.b: Test pattern for evaluation of the possibility of making differently shaped structures and thick-film resistors in a multilayer structure

Visual and electrical inspection showed that the conductor lines going through vias with a diameter 150 μm or larger were continuous, while for smaller dimensions, conductors on part of the samples were open. Results obtained with the test circuit therefore showed that vias with 150 μm diameter or larger can be made while some of the 100 μm vias and nearly half of the 50 μm vias were closed. However, for high-volume production 200 μm is probably the lower limit. The vias with 50 μm , 100 μm and 150 μm diameter are shown in Fig. 9.

Via-dimension measuring shows that the diameter of the vias in the dielectric is in some cases up to 30% larger than the designed diameter. This can be attributed to the fact that the image paste diffuses not only vertically into the dielectric but also to some extent horizontally. The widening of the designed via dimensions should be taken into account when the multilayer circuit is designed. The results are summarised in Table 2. The ratio between the measered via diameters after firing and via diameters on photo mask are denoted in the Table 1 as the "D/PM increase".

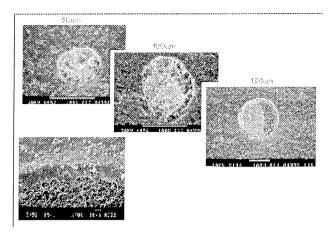


Fig. 9: Diffusion-patterning vias in the dielectric layer.
The edge of a 200 μm via is shown in lower left corner.

Standard diffusing time is 10 min at 85°C. To estimate the influence of the time of diffusion at this temperature on the dimensions of vias and lines, the diffusion time was varied for some samples from 5 to 20 minutes. Visual inspection showed that the diameter of the vias, which were already open after 5 minutes, is practically independent of the diffusion time. The width of lines increased with increasing time of diffusion by nearly 50% after 20 minutes. This effect was more pronounced for wider lines.

6. Diffusion patterning - A pressure sensor

In the case of a typical pressure sensor construction before miniaturisation the sensor element (gauge silicon piezoresistive pressure sensor) is integrated on a thick-film substrate with conditioning electronics on the periphery. Electronic conditioning circuit with conventional electronic components is shown in Fig. 10.a. The sensor in is designed for measuring absolute pressure in the range of 1 bar and has 0,5V to 4,5V output voltage with 5V supply voltage.

The common electronic conditioning circuit for pressure sensor applications needs an excitation voltage or current, instrumentation amplifier, voltage reference and an output stage. Before miniaturisation the conditioning electronics

Table 2: Dimension of vias from design to realisation

Via diameter (μm)										
Layout	500	400	300	250	200	150	100	50		
Photo-Mask	540	440	340	290	240	190	140	90		
Screen-Mask	550	450	350	300	250	210	150	100		
Dielectric	620	550	430	380	300	250	150			
D/PM increase	115%	125%	126%	131%	125%	132%	107%	/		

were realised with conventional electronic components in SMD form. To attain the object of miniaturisation a semicustom ASIC for signal processing AM401 (Analog Microelectronics) was used as an equivalent electronic conditioning circuit. The AM401 is a low-cost monolithic voltage transmitter, designed for flexible bridge input signal conditioning. It contains a high-accuracy instrumentation amplifier for differential input signals, an operational amplifier output stage, and an adjustable voltage reference (5V or 10V). In addition to these functional elements an auxiliary operational amplifier can be used as a current or voltage source. Output range and gain are adjustable over a wide range by external resistors.

Electronic design with ASIC AM401 completely replaces conventional electronics, except for a few passive components. These resistors and capacitors are still needed for temperature compensation of the silicon sensor element, calibration (offset voltage, output range, gain) of the complete sensor and stabilisation of the reference voltage and the first-stage voltage. This means that the passive sensor part is the same, only the amplifier is simplified. The important factor for miniaturisation and lower price is the use of active trimming of thick-film resistors to avoid the discrete trimmer potentiometers for all functional adjustments. Fewer electronic components mean less area required for the complete circuit and proportionally a lower price. The circuit with AM401 has some disadvantages too. For example, the supply voltage should be at least 5V above the maximum output voltage. This means that when using AM401, sensors lose their advantage of low supply voltage.

The new, miniaturised pressure sensor was designed for measuring relative pressure in the range of 1 bar and has 0,5V to 4,5V output voltage with a 12V supply. The pressure sensor was realised with a semi-custom ASIC AM401 for signal processing, silicon piezoresistive pressure sensor SM-21 as a sensing element, and 11 passive components for parameter adjustment and ASIC periphery. The electronic circuit schematic diagram is shown in Figure 10.b.

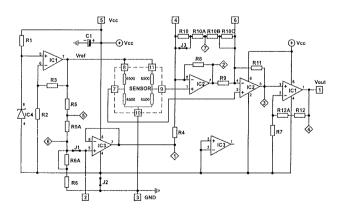


Fig. 10.a: Electronic conditioning circuit with conventional electronic components

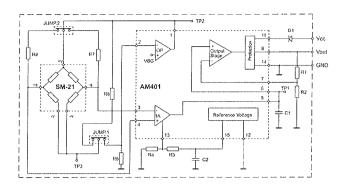


Fig. 10.b: Electronic conditioning circuit with analog ASIC

A thick-film multilayer MCM-C with four conductive layers was designed and produced with diffusion patterning technology. The substrate for the pressure sensor is Al₂O₃ ceramic with dimensions 3.5 mm × 18.0 mm × 0.64 mm. In the ceramic there are four holes, one 1.4 mm square hole for applying the measuring pressure, and three holes (0.2 mm diameter) for electrical interconnection with a throughhole printing technology. The thick-film multilayer interconnection consists of four conductive layers (one on the rear side), two dielectric layers, 38 interconnections between conductive layers, and two overglaze layers. The top conductive layer integrates also 19 gold bonding pads, eight laser trimmed thick-film resistors, three bare dies bonded with aluminium wires, two jumpers, and three terminal pads. On the rear side two multilayer chip capacitors are soldered. The layout and cross-section of pressure sensor are shown in Figure 11. The volume reduction from the conventional thick-film pressure-sensor module to the same module, realised as a MCM-C, is around 20x.

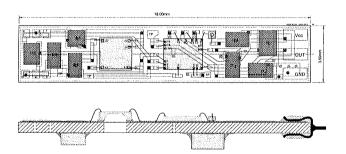


Fig. 11: The layout and cross-section of pressure sensor realised in diffusion patterning technology

Aknowledgement

The authors wish to thank Mr. Mitja Jerlah (HIPOT) for printing and firing the test circuits and the MCM-C module and Mr. Zoran Samardžija, dipl.ing. (Jožef Stefan Institute) for SEM and EDS analysis. The financial support of the Ministry of Education, Science and Sport of the Republic of Slovenia is gratefully acknowledged.

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Prispelo (Arrived): 09.10.2002 Sprejeto (Accepted): 20.11.2002