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A linear current-controlled floating negative resistor

Hamdi Ercan

Department of Avionics, Erciyes University, Kayseri, Turkey

Abstract: In this article, a low voltage CMOS current controlled floating negative resistor which is convenient for integrated circuit implementation is designed by using a self-cascode composite transistor. The proposed circuit only required ± 0.75 V as a power supply has a simple circuit structure and a low power consumption of which value is only 65 µW. The basic advantages of this circuit are a wide tuning range of the resistance value, an acceptable frequency performance and a wide dynamic range. The performances of the proposed circuit are simulated with SPICE to confirm the presented theory.

Keywords: Negative resistance, CMOS active resistor, current-controlled circuits, Current-mode, Integrated circuits

Linearen tokovno kontroliran plavajoči negativni upor

Izvleček: V članku je predstavljen nizko napetostni CMOS tokovno kontrolirani negativen upor, ki je uporaben v integriranih vezjih. Upor uporablja samo kaskaden kompozitni tranzistor. Predlagano vezje z napajalno napetostjo ± 0.75 V izkazuje nizko porabo okoli 65 µW. Glavne prednosti vezja so široko uporovno območje, sprejemljive frekvenčne lastnosti in široka dinamično območje. Teoretični rezultati so preverjeni s pomočjo SPICE simulacij.

Ključne besede: negativna uporost, CMOS aktiven upor, tokovno kontrolirano vezje, tokovni način, integrirana vezja

* *Corresponding Author's e-mail: hamdiercan@erciyes.edu.tr*

1 Introduction

In recent years, the disposition of the analog circuit design with low-voltage operation capability has been raised owing to the fact that it is aimed to consume as little power as possible. The low power dissipation is an important factor for the weight and life of a battery. Thus, the design techniques and device technology for low-voltage low-power operation of the analogue circuits are required [1].

Large areas of the chip are required to obtain resistors which can be implemented by using diffusion areas in an integrated circuit. Also, these resistors cannot be easily adjusted to demanded values. To overcome these drawbacks, MOS and bipolar based active resistors topology have been reported in the previous studies [2-5].

Bipolar-based floating resistor was presented in the literature [4, 6]. Though these resistors have a good frequency performance, they have not only narrow dynamic range but also consume more power than the MOS-based active resistors. But at the same time, MOS resistors are limited with regard to frequency response and electronically tunability.

The voltage-controlled resistors have been used as an application in the analog circuit design area [7, 8]. The tunable resistance value of these circuits has been restricted by supply voltage. However, they have a wide dynamic range. The current-controlled resistors can be independently tuned over a wide range by biasing current. Also, they have a good frequency performance. Recently, active resistors have been used as not only positive but also negative resistor in some applications. Active positive/negative resistors have been used in a lot of implementations such as oscillators, amplifiers and filters [4, 9, 10,11].

In this paper, a linear current-controlled negative resistor based on self-cascode composite transistor has been introduced. The proposed circuit offers the advantages of a good linearity, a high dynamic range

and low power consumption. This circuit only operates at low voltage as ± 0.75 V. Until now, it has not been shown that low-voltage negative resistor structures are designed in somewhere else. The main contribution of this design to the literature leads to use the low voltage and low power applications. Having a simple structure, the resistance value of the resistor is obtained as the positive and negative.

2 Floating negative resistor

Self-cascode composite transistor structure is shown in Fig. 1. In practical cases, for optimal operation the W/L ratio of the M_A should be larger than the W/L ratio of the M_B, that is, a > 1. Moreover, the transistor M_B must be in triode region. Depending on the drain voltage, transistor M_A can work in saturation region or triode region. The aspect ratio (W/L) of the equivalent MOS transistor shown in Fig. 1 is decreased. This circuit structure takes an advantage in terms of linearity, dynamic range and electronically controllable resistance range.

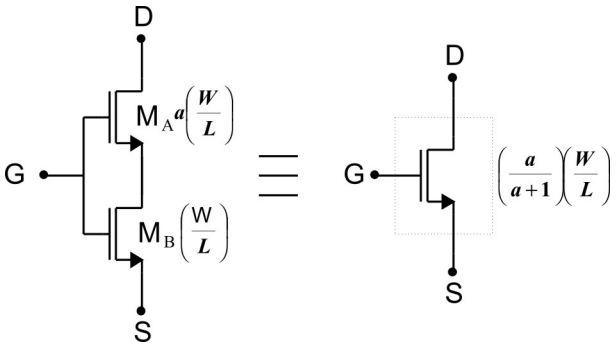

Figure 1: The self-cascode composite transistor.

Fig. 2 indicates the proposed linear current-controlled floating negative resistor.

The drain currents of transistors M_1 and M_4 can be written as,

$$I_{D1} = \frac{1}{2}k_n\left(\frac{a}{a+1}\right)\left(\frac{W}{L}\right)\left(V_1 - V_{S5} - V_{TH}\right)^2 . \quad (1)$$

$$I_{D4} = \frac{1}{2}k_n\left(\frac{a}{a+1}\right)\left(\frac{W}{L}\right)\left(V_2 - V_{S8} - V_{TH}\right)^2 . \quad (2)$$

I_{D1} and I_{D4} are the drain currents of transistors M_1 and M_4, respectively. In addition, V_{S5} and V_{S8} are the source voltages of transistors M_5 and M_8, respectively. From Eqs. (1) and (2), the relationship between V_1 and V_2 shown in Fig. 2 can be expressed as

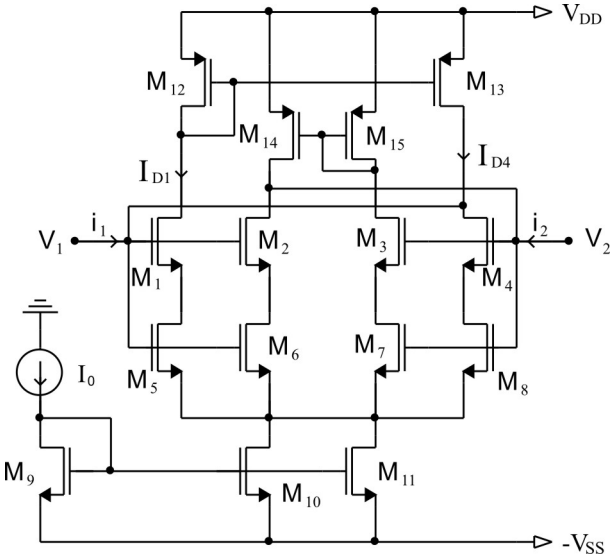

Figure 2: The current-controlled floating negative resistor.

$$V_1 - V_2 = \sqrt{\frac{I_0 - i_1}{k_n\left(\frac{a}{a+1}\right)\left(\frac{W}{L}\right)}} - \sqrt{\frac{I_0 + i_1}{k_n\left(\frac{a}{a+1}\right)\left(\frac{W}{L}\right)}} . \quad (3)$$

Current i_1 shown in Fig. 2 is given as:

$$i_1 \cong -\left(V_1 - V_2\right)\left[\frac{1}{2}k_n\left(\frac{a}{a+1}\right)\frac{W}{L}\right]^{1/2} \times$$

$$\times\left[2I_0 - \frac{1}{2}k_n\left(\frac{a}{a+1}\right)\frac{W}{L}\left(V_1 - V_2\right)^2\right]^{1/2} . \quad (4)$$

where $k_n = \mu_n C_{ox}$ is the transconductance parameter of the NMOS transistor. μn is the electron mobility and *Cox* is the oxide capacitance per unit area. I_0 is the biasing current. For a very small difference voltage which gives $2I_0 >> (1/2)k_n(a/a+1)(W/L)(V_1-V_2)^2$, the current i_1 exhibits a quite linear behavior. As shown in Eq. (4), linearity of the resistance highly depends on the aspect ratio (W/L) of the equivalent self-cascode composite MOS transistors and the difference voltage. Therefore, i_1 can be further reduced to:

$$i_1 \cong -\left(V_1 - V_2\right)\left[k_n\left(\frac{a}{a+1}\right)\frac{W}{L}I_0\right]^{1/2} . \quad (5)$$

In this instance, it is clear that $i_2 = -i_1$. The resistance of the proposed circuit can be written as

$$R_{12} \cong -\left[k_n\left(\frac{a}{a+1}\right)\frac{W}{L}I_0\right]^{-1/2} . \quad (6)$$

The resistance value can be easily controlled by biasing current as shown in Eq. (6). The proposed negative resistor shown in Fig. 2 can be easily converted to the positive resistor. A connection is made between the gates of transistor M_1, M_2 and drain of M_2 instead of M_4's drain. Additively, the gates of M_3 and M_4 are connected to the drain of M_4 instead of M_2's drain. In this case, it is clear that $i_1 = -i_2$. So, the definition of the positive resistance may be as follow:

$$R_{12} \cong \left[k_n \left(\frac{a}{a+1} \right) \frac{W}{L} I_0 \right]^{-1/2} . \quad (7)$$

The positive resistance of the resistor is able to be easily tuned by biasing current, too. Also, building two different kinds of in a single circuit is one of the important features of the proposed circuit. These features take essential advantages for the analog circuit applications.

For operating at low-voltage, this circuit requires to ensure the below-mentioned condition.

$$V_{DD} - \left(-V_{SS} \right) \geq V_{THP} + 4V_{DSsat} . \quad (8)$$

where V_{DD} and $-V_{SS}$ are the supply voltages of the circuit. V_{THP} is the threshold voltage of the PMOS and V_{DSsat} is the drain-source saturation voltage of the transistors. The value of the V_{THP} is approximately 0.4 V for 0.13 µm technology [12]. The lower drain currents have values, the more drain-source saturation voltage is reduced. Thus, the proposed circuit can be operated at low-voltage. Additionally, the estimation of the proposed circuit's dynamic-range is calculated as

$$\left| V_1 - V_2 \right| \leq \left[\left(\frac{a+1}{a} \right) \left(\frac{I_0}{\frac{1}{2} k_n \frac{W}{L}} \right) \right]^{1/2} . \quad (9)$$

The dynamic range highly depends on the biasing current as shown in Eq. (9). Thus, the dynamic range will be expanded for the high values of the biasing current.

3 Simulation results

The proposed linear current-controlled floating negative resistor was simulated by SPICE owing to approve the theoretical approaches. The SPICE model 0.13 µm CMOS parameter for the transistors are used in [12]. The supply voltage is ± 0.75 V and the aspect ratio of the transistors is presented in the Table I.

Table 1: Aspect ratio of the transistors.

Transistor	$M_1 - M_4$	$M_5 - M_8$	$M_9 - M_{15}$
W/L	5/1	1/2	30/0.26

I / V characteristics of the proposed resistor are shown in Fig. 3.

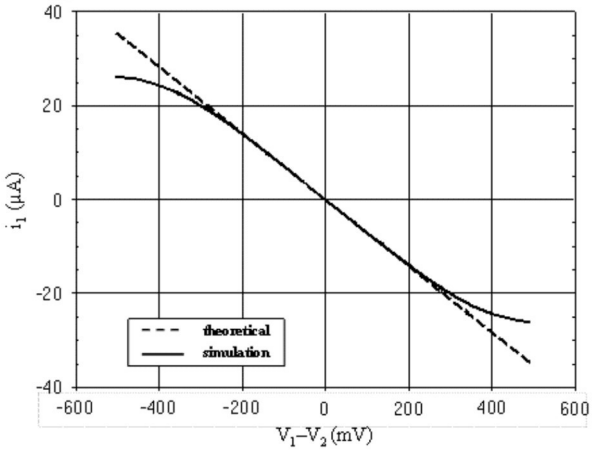

Figure 3: I / V characteristics of the proposed resistor.

Both theoretical and simulation results of the proposed resistor have been given in Fig. 3. It is shown that behaviour of the proposed resistor is highly linear from -250 mV to +250 mV. Fig. 4 shows the input voltage versus the input current of the simulated resistor.

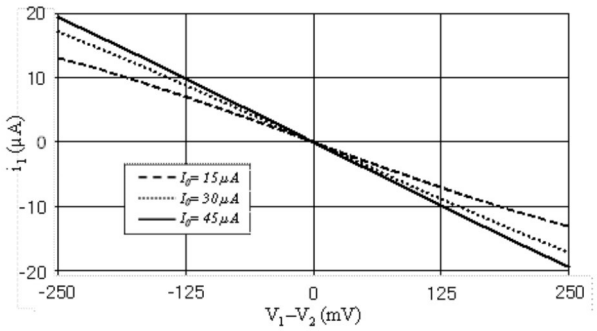

Figure 4: I / V characteristics for the different biasing current.

The biasing current of the resistor is varied from 15 µA to 45 µA step by step. The resistance value of the resistor can be easily adjusted by biasing current I_0 as shown in Fig. 4. The frequency response of the proposed resistor is illustrated in Fig. 5.

When the frequencies are increased, it is found that the proposed resistor can be operated with the –3dB bandwidth of about 148.3 MHz, 195.4 MHz and 222.1 MHz for 15 µA, 30 µA and 45 µA of the biasing current, respectively. Taking into consideration these results,

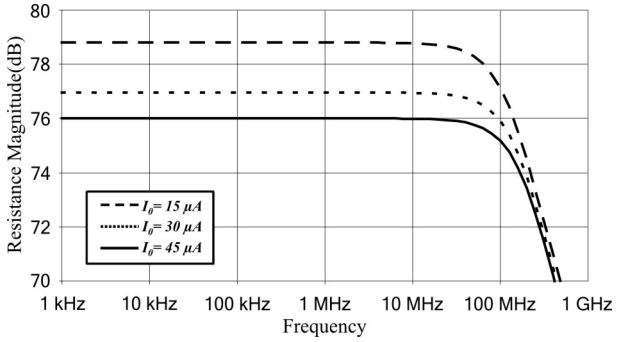

Figure 5: The frequency response of the proposed resistor.

the proposed circuit exhibits a good frequency performance.

The variation of the total harmonic distortion with peak to peak input voltage for I_0 = 15 μA and R_{12} = 8.7 kΩ is displayed in Fig. 6.

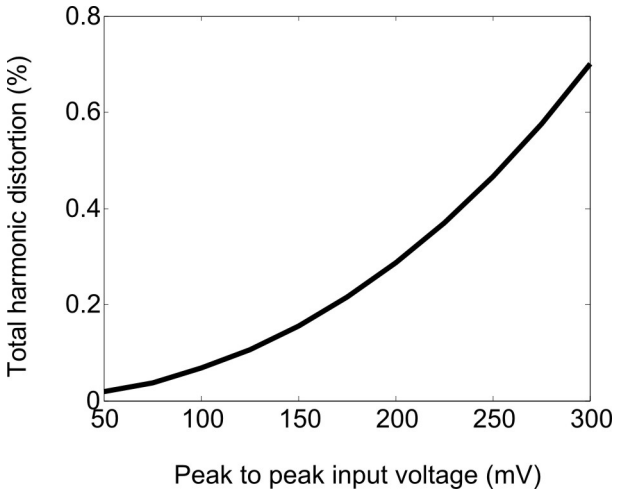

Figure 6: THD % versus input voltage.

The variation of the THD with input signal amplitude for a biasing current of 15 μA as shown in Fig. 6 is illustrated. We can evidently see that the THD value is 0.465 % at 250 mV_{p-p}. It is depicted that the THD values obtained according to different peak to peak input voltages are acceptable values. Also, the total power consumption of the proposed circuit is obtained as low value as 65 μW. The resistance of the proposed circuit has been calculated as both theoretical and simulation. The negative resistance of the proposed resistor for different bias currents is shown in Fig. 7.

The negative resistance is able to be tuned from 5.9 kΩ to 243 kΩ when the biasing current is adjusted between 0.1 μA and 60 μA. Note that, this circuit has a wide range negative resistance (R_{12}).

Noise is a main contributor to the inaccuracy of the analog circuits. The main source of the noise in a MOS

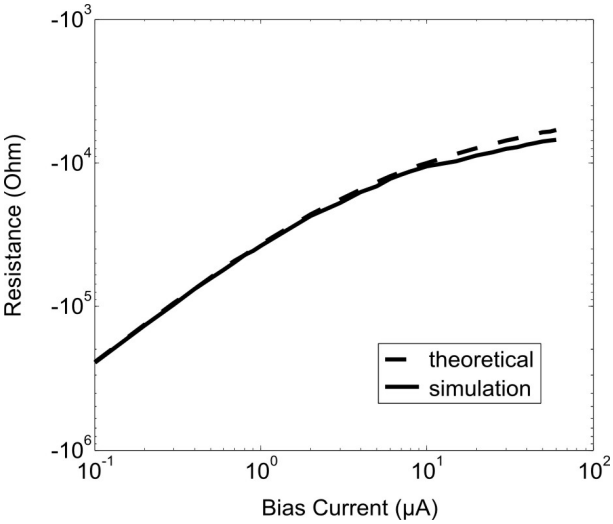

Figure 7: The negative resistance versus bias current.

transistor is the thermal noise owing to the thermal effect of the electrons in the resistive channel. The voltage noise of a MOS transistor is given in Eq. (10).

$$\overline{V^2} = \frac{8}{3} kTg_m r_0^2 \frac{V^2}{Hz} \tag{10}$$

where k is Boltzmann's constant and T is the temperature. g_m and r_0 are the transconductance and output resistance of the MOS transistor, respectively. Due to the fact that gm can be changed by the drain current of the transistor, the noise of the proposed circuit indicated in Fig. 2 depends on the biasing current.

A noise analysis of the negative resistor was performed in SPICE. Therefore, in accordance with SPICE results, the noise contributions of each transistor to the total output voltage noise are given in Table II.

Table 2: Noise sources of the proposed negative resistor.

Transistors	The voltage noise (V^2/Hz)	Transistors	The voltage noise (V^2/Hz)
M_1	$6.72x10^{-18}$	M_9	$2.60x10^{-15}$
M_2	$2.24x10^{-18}$	M_{10}	$6.80x10^{-16}$
M_3	$1.08x10^{-19}$	M_{11}	$6.80x10^{-16}$
M_4	$0.67x10^{-19}$	M_{12}	$19.77x10^{-20}$
M_5	$62.83x10^{-18}$	M_{13}	$7.03x10^{-21}$
M_6	$71.17x10^{-18}$	M_{14}	$1.70x10^{-18}$
M_7	$21.38x10^{-21}$	M_{15}	$1.00x10^{-30}$
M_8	$21.38x10^{-21}$		
Total voltage noise		64.07 nV/√Hz	

The resistance value of the proposed circuit is -6.31 kΩ for I_0=45 µA. The total voltage noise for the proposed circuit which has -6.31 kΩ resistance value is 64.07 nV/√Hz. The main contributors to the total noise are the three transistors M_9, M_{10} and M_{11}. Total voltage noises can be obtained as 57.544 nV/√Hz, 63.003 nV/√Hz and 64.070 nV/√Hz for I_0=15 µA, I_0=30 µA and I_0=45 µA, respectively. In other words, the total voltage noise is strongly depends on transconductance as shown in Eq. (10).

The negative resistance having a wide tuning range is an important advantage for the analog circuit applications. The comparison of the performance parameters belongs to some resistors and the proposed negative resistor is displayed in Table III.

If the circuits are compared in terms of supply voltage, the proposed negative resistor requires a small supply voltage. As shown in Table III, the total harmonic distortion of the proposed circuit is lower than the others. Moreover, this circuit consumes low power of which has only 65 µW value. The total voltage noise has not been studied in other cited paper. However, the total voltage noise of the proposed circuit can be obtained as 64.07 nV/√Hz.

4 Conclusion

In this study, the self-cascode composite transistor based a linear current-controlled floating negative resistor has been presented. The circuit required low supply voltage as well as ±0.75 V consumes low power about 65 µW. In addition, the circuit has highly basic circuit structure. The behaviour of the proposed resistor is highly linear from -250 mV to +250 mV. The value of the proposed resistance can also be adjusted from 5.9 kΩ to 243 kΩ with perfect correspondence between the theoretical and simulation results by changing the value of the bias current. The total voltage noise and THD values of the proposed circuit have been calculated as 0.465 % and 64.07 nV/√Hz, respectively. Finally, we expect that such a tunable behaviour of the proposed negative resistor could highly be appropriate for the low voltage integrated circuit realizations, considering into the perfect resemblance between all the simulated and theoretical performances.

References

1. S. S. Rajput and S. S. Jamuar, "Low voltage analog circuit design techniques," Circuits and Systems Magazine IEEE, vol. 2, no.1, pp. 24-42, 2002.
2. R. Senani, A. Singh, and V. K. Singh, "A new floating current-controlled positive resistance using mixed translinear cells," IEEE Transactions on Circuits and Systems II, vol. 51, no. 7, pp. 374-377, July 2004.
3. A. Manolescu and C. Popa, "Low-Voltage low-power improved linearity CMOS active resistor circuits," Analog Integrated Circuits and Signal Processing, vol. 62, no.3, pp. 373-387, 2010.
4. S. A. Tekin and M. Alçı, "Design and applications of electronically tunable floating resistor using differential amplifier," Elektronika Ir Elektrotechnika (Journal Electronics and Electrical Engineering), vol. 19, no.4, pp. 41-46, 2013.
5. P. Pawarangkoon and W. Kiranon, "Electronically tunable floating resistor," International Journal of Electronics, vol. 91, no. 11, pp. 665-673, November 2004.
6. A. Khan and M. T. Ahmed, "Realisation of tunable floating resistors," Electronics Letters, vol. 22, no. 15, pp. 799-800, July 1986.
7. M. Kumngern, U. Torteanchai, and K. Dejhan, "Voltage-controlled floating resistor using DDCC,"

Table 3: Comparison between this study and the others.

Parameters	This study	[3]	[13]	[4]	[5]
Supply voltage	± 0.75 V	± 3 V	± 1.5 V	± 1.5 V	± 2.5 V
Input range	± 250 mV	± 1 V	± 200 mV	± 30 mV	± 30 mV
Tuning range	5.9 kΩ - 243 kΩ	800 kΩ - 4 MΩ	60 kΩ - ∞	43Ω - 516kΩ	132 Ω-1.25 kΩ
Total harmonic distortion (THD)	0.465 % (at 1 MHz)	0.5 % (NA)	NA	0.747 % (at 1 MHz)	> 1 % (at 1 kHz)
Total voltage noise	64.07 nV/√Hz	NA	NA	NA	NA
Power dissipation	65 µW	NA	NA	0.9 mW	NA
Bandwidth	222.1 MHz	NA	NA	70.2 MHz	NA
Technology	CMOS (0.13 µm)	CMOS (0.35 µm)	CMOS	Bipolar	Bipolar
Positive resistance	Yes	Yes	Yes	Yes	Yes
Floating	Yes	Yes	Yes	Yes	Yes

Radioengineering Journal, vol. 20, no. 1, pp. 327-333 April 2011.
8. M., Gupta and R. Pandey, "FGMOS based voltage-controlled resistor and its applications," Microelectronics Journal, vol. 41, no. 6, pp. 25-32, 2010.
9. W. Surakamponton, "CMOS floating voltage-controlled negative resistor," Electronics Letters, vol. 28, no. 15, pp. 1457-1459, July 1992.
10. A. Sunca, O. Cicekoglu, and G. Dundar, "MOS only simulated grounded negative resistors," 34th International Conference on Telecommunications and Signal Processing (TSP), Budapest, Hungary, doi: 10.1109/TSP.2011.6043715, pp. 328-331, August 2011.
11. H. Ercan, S. A. Tekin, and M. Alçı, "Voltage- and current-controlled high CMRR instrumentation amplifier using CMOS current conveyors," Turkish Journal of Electrical Engineering & Computer Sciences, vol. 20, no. 4, pp. 547-556, July 2012.
12. E. Yuce and S. Minaei, "New CCII-based versatile structure for realizing PID controller and instrumentation amplifier," Microelectronics Journal, vol. 41, no. 5, pp. 311-316, May 2010.
13. S. Tantry, Y. Hiraku, T. Oura, T. Yoneyama and H. Asai, "A low voltage floating resistor circuit having both positive and negative resistance values," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, vol. E86-A, no. 2, pp. 335-341, February 2003.

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