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Za vse to skrbijo štirje stalno zaposleni. Lansko leto je društvo praznovalo svojo tridesetletnico. Za svoj začetek namreč štejejo ustanovitev ISHM (International Society for Hybrid Microelectronics), sedanji IMAPS pa je nastal prav lansko leto z združitvijo ISHM in IEPS (International Electronic Packaging Society).

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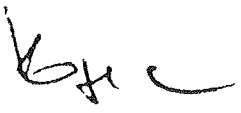

Dr. Marija Kosec

MICROSTRUCTURE AND PHYSICAL PROPERTIES OF MnZn FERRITES FOR THE HIGH FREQUENCY POWER SUPPLIES

M. Drofenik
Jožef Stefan Institute, Ljubljana, Slovenia

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Devices and Materials, MIDEM´97
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Keywords: MnZn ferrites, microstructure properties, physical properties, power suplies, high frequency power supplies, grain sizes, grain boundary properties, power losses, magnetic losses, high electrical resistance, aliovalent ions, ion doping, oxygen concentration, SMPS, switch-mode power supplies, eddy current

Abstract: The power loss of MnZn ferrites and its relation to the average grain size and grain boundary properties was studied. It was found that the power loss depend on the average grain size and on the highly electrically resistive grain boundaries which are formed by introduction of aliovalent ions in the intrinsic grain boundary of MnZn ferrite grains. A lower concentration of oxygen during sintering decreases the average grain size and improves the magnetic loss.

Mikrostrukturne in fizikalne lastnosti MnZn feritov za uporabo v visokofrekvenčnih napajalnikih

Ključne besede: MnZn-feriti, lastnosti mikrostrukturne, lastnosti fizikalne, napajalniki energetski, napajalniki energetski visokofrekvenčni, velikost zrn, lastnosti zrn mejne, izgube močnostne, izgube magnetne, upornost električna visoka, ioni aliovalentni, dopiranje ionov, koncentracija kisika, SMPS napajalniki komutacijski, tok vrtinčni

Povzetek: Preučevali smo močnostne izgube MnZn feritov in odvisnost izgub od povprečne velikosti zrn in lastnosti meja med zrni. Ugotovili smo, da je izguba odvisna tako od povprečne velikosti zrn, kakor tudi od mej med zrni z izredno visoko električno upornostjo, ki jih ustvarimo z vgradnjo večvalentnih ionov v zrna MnZn ferita. Nižja koncentracija kisika med sintranjem zmanjša povprečno velikost zrn in izboljša magnetne izgube.

1. INTRODUCTION

The application of MnZn ferrites in power electronics is constantly increasing. Particularly the growth of the commercial market for Switch Mode Power Supplies (SMPS) places demands on the ferrite industry to produce high performance ferrite cores capable of operating at increasingly higher frequencies /1/. In SMPS the switching frequency is related to the power output, making it possible for smaller core volumes to transform the same amount of power as a larger core would at lower frequencies. This is a direct challenge for the miniaturization of SMPS and related power devices /2/.

The main core characteristics are core losses which contribute the major part of the total electrical loss. In general the core loss can be divided into a residual loss, a hysteresis loss and an eddy current loss. The residual loss is important only at low induction levels and can be ignored in the power application of MnZn ferrites. The hysteresis loss $P_H = W_h f$, where $W_H = \int HdB$ is the energy represented by the area of the hysteresis loop measured under the maximum flux density, depends on many parameters; however, hindrance to domain wall displacements /3/, which takes place at high induction levels /4/, plays the major role.

The factors governing the hysteresis loss are the magnetocrystalline anisotropy K_1 magnetostriction λ, stress σ, porosity p, and saturation magnetization M_S. For low hysteresis loss K_1, λ, σ, and p should be low. These parameters can be controlled by the chemical composition; however, the porosity (p) and mechanical stress (σ) are controlled mostly by the microstructure and impurities. The ferrous content, which is essential in MnZn ferrites for achieving low magnetisation anisotropy and magnetostriction and thus low hysteresis loss, gives rise to a high electrical conductivity due to the thermally activated hopping mechanism between Fe^{2+} and Fe^{3+} in spinel ferrites. The relatively low electrical resistivity, ρ_{bulk}, influences the eddy current loss, $P_E = AB_m^2 f^2 / \rho_{bulk}$, where A is the core cross section, Bm is the maximal flux density, and f is the frequency. The most effective way to suppress electron hopping and thus the electrical conductivity inside the ferrite grains, is by the substitution of Ti^{4+}, which occupies the B site /5/ adjacent to Fe^{2+}.

At higher operating frequencies the contribution of the eddy current loss to the total loss strongly increases and above 500 kHz it dominates all other losses. Therefore in order to increase the performance of MnZn ferrites for powder applications at higher frequencies, the eddy current losses must be suppressed to the greatest possible extent.

2. CORRELATION BETWEEN MICROSTRUCTURE PARAMETERS AND POWER LOSS

In MnZn ferrites the grain boundary shows different chemical and physical properties from the ferrite grains. The segregation of impurities and partial reoxidation of Fe^{2+} on the grain boundaries during cooling makes the MnZn ferrite grain boundaries highly insulating in comparison to the grain interior. These insulating layers are in practice very thin and therefore exhibit a relatively high electrical capacity.

For such a ferrite core the equivalent electrical circuit of the semiconducting grains and the insulating grain boundaries form a resistance and capacitance connected in parallel whose impedance causes a dispersion with respect to the frequency /6/.

The impedance of parallel R;C; elements, which usually represent the equivalent circuit of a MnZn ferrite, is

$Z = Z' - jZ''$ where

$$Z' = \sum \frac{R_i}{1+(\omega R_i C_i)^2} \quad \text{and} \quad Z'' = \sum R_i \frac{\omega R_i C_i}{1+(\omega R_i C_i)^2}.$$

The impedance

$$Z = \sqrt{(Z')^2 + (Z'')^2}$$

for $\omega RC << 1$ where $\omega = 2\pi f$ will be close to the pure ohmic resistance $Z \rightarrow R$. However, in the case when $\omega RC >> 1$ and consequently $Z \rightarrow 1/\omega C$ the grain boundary capacitance will play the dominant role in the MnZn ferrite. Thus, depending on the operating frequency, two extreme cases govern the impedance of the MnZn ferrite and its power losses.

In order to elucidate the dependence of power loss P on the average grain size D and the grain boundary thickness δ_{gr} and its resistance R_{gr} which are the essential microstructure element, we will divide the ferrite material into small cubes, i.e. the brick wall model, Fig. 1. In this hypothetical model the grain boundaries with a thickness $\delta_{g.b.}$ will lie in directions perpendicular and parallel to the principal axis, i.e. to the electric field direction. The grain boundaries which are parallel to the principal axis will be electrically bypassed by the bulk material. Therefore the small cubes can be approximated by bulk material separated by high ohmic layers - the grain boundaries which are perpendicular to the principal axis. Each layer can be represented by a resistance-capacitance (R - C) lumped circuit of high ohmic layers. When the resistivity of the bulk is much lower than the grain boundary layers, the equivalent circuit of the ferrite can be represented by a series of lumped R - C circuits of the grain boundary layers.

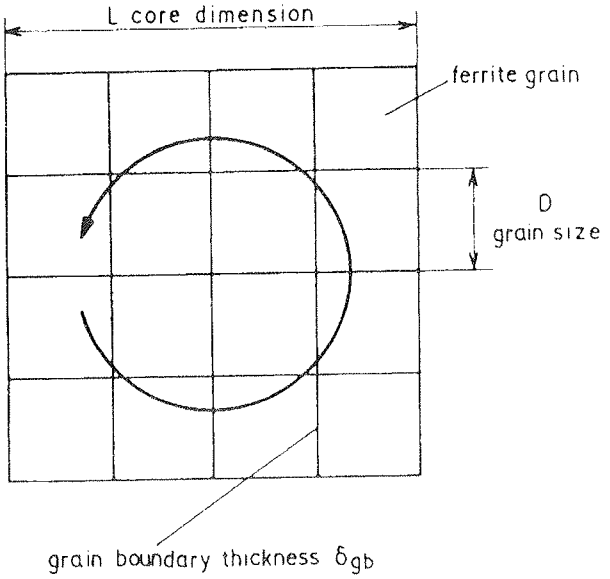

Fig.1: Brick wall microstructure model: a sketch of an ideal microstructure of a material - MnZn ferrite - with grain boundaries permeable to the eddy current

In a real material, the grains have the shapes of irregular polyhedra. In this case only the components of the grain boundaries which are perpendicular to the principal axis can effectively block the electric current.

By applying this model /7/ the macroscopic resistance, which can be obtained from the impedance spectra, can be expressed as

$$R_{g.b.}^{(mac.)} = R_{g.b.}^{(mic.)} \cdot \frac{L}{D+\delta_{g.b.}} \quad \text{where} \quad \frac{L}{D+\delta_{g.b.}} \approx \frac{L}{D}$$

is the number of grain boundaries perpendicular to the electric field, $\delta_{g.b.}$ is thickness of the grain boundary,

$$R_{g.b.}^{(mac.)} = \rho_{g.b.}^{(mic.)} \cdot \frac{L}{A}$$

is the macroscopic resistance obtained from complex impedance plots and L/A is length-area ratio of the samples. Further, by combination of the above Eqs. it follows that

$$\rho_{g.b.}^{(mac.)} = R_{g.b.}^{(mic.)} \cdot \frac{A}{D} = \rho_{g.b.}^{(mic.)} \frac{\delta_{g.b.}}{D}.$$

When we combine this expression with that of the eddy current loss, we finally obtain

$$P_e = cB_m^2 f^2 \cdot \frac{D}{R_{g.b.}^{(mic)}} \qquad (1)$$

Thus, at lower frequencies $\omega RC << 1$, the eddy current is proportional to the average grain size and inversely to the resistance of a grain boundary $R_{g.b.}^{(mic)}$. On the other hand, at higher frequencies where $\omega RC >> 1$ when again applying the brick-wall model, where for each grain boundary intersection perpendicular to the electric field

$$C^{(mic)} = \varepsilon_o \cdot \varepsilon_{g.b.} \frac{A}{\delta_{g.b.}}$$

and considering the number of grain boundaries $\approx L/D$, then it follows that

$$\frac{1}{C^{(mac)}} = \frac{L}{D}\frac{1}{C^{(mic)}} \quad \text{and finally} \quad C^{(mac)} = \varepsilon_o \cdot \varepsilon_{g.b.} \frac{D}{\delta_{g.b.}}\frac{A}{L}$$

By inserting the impedance in the relation for the eddy current power loss we obtain

$$P_E \approx cAB_m^2 f^2 \times \omega C^{(mac)} \propto \varepsilon_{g.b.} \frac{D}{\delta_{g.b.}} \qquad (2)$$

We can see that when $\omega RC >> 1$ the eddy current loss is determined by the average grain size, the thickness of the grain boundary and its permittivity. Therefore from the above considerations it can be seen that the average grain size is to a great extent the dominant microstructural parameter in the whole frequency range and determines the eddy current loss. Further, we can see that up to the operating frequencies where the grain boundaries are not short circuited by a high displacement current, the power loss of MnZn ferrites can be effectively suppressed by a decrease in average grain size $\overline{D}$, by increasing the grain boundary resistance $R_{g.b.}^{(mic)}$, by increasing the grain boundary width $\delta_{g.b.}$ and/or bydecreasing its permittivity $\varepsilon_{g.b.}$

3. TAILORING OF MICROSTRUCTURE PARAMETERS AND POWER LOSSES

The average grain size of a MnZn ferrite can be effectively decreased by sintering it at a lower oxygen partial pressure /8/, while the grain boundary resistivity can be increased by the addition of aliovalent ions to the ferrite /9/.

In order to engineer the MnZn ferrite parameters, i.e. to decrease average grain size (D) and/or to increase the intrinsic grain boundary resistance, the concentration of oxygen during sintering may be varied from 21 vol. % to 1 vol. % and the ferrite should be doped with aliovalent ions which segregate to the grain boundary during sintering.

It is well established that a higher amount of oxygen 21 vol. % increases the pore mobility and induces exaggerated pore growth, while a lower concentration of oxygen increases the concentration of the slowest moving species, i.e. oxygen vacancies, and promotes volume diffusion and hence grain boundary mobility /10/. On the other hand, the pore - grain boundary interaction during sintering has a decisive influence on the microstructure /11/. Depending on the pore size/grain size ratio, the grain growth is largely determined by the attachment or separation of the pores from the grain boundary. When this ratio is small the pores will be left behind and the conditions for the formation of grains with exaggerated grain size and trapped pores will be present. So, if one would like to engineer effectively the MnZn ferrites microstructure, exaggerated pores must first be developed by using a high partial pressure of oxygen during sintering. If these pores are large enough they can effectively pin the grain boundaries /12/ and impede grain growth at lower $P(O_2)$ (if applied) which promotes densification and grain boundary mobility.

Fig. 2 shows a typical power loss dependence vs. the temperature of MnZn ferrites sintered at different partial pressures of oxygen /8/ (sample 1 sintered at 21 vol% of oxygen, sample 2 at 10 vol % of oxygen, sample 3 at 5 vol % and the sample 4 at 1 vol % of oxygen). The essential microstructural parameters of the samples are shown in Table I.

Table I: The key microstructural parameters of the sintered samples; density (ρ), percentage of theoretical density (TD), average grain size ($\overline{D}$), average grain size without giant grains ($\overline{D}'$), and percentage of giant grains (A).

Sample code	ρ [g/cm^3]	TD Š%]	$\overline{D}$ [μm]	$\overline{D}'$ [μm]	A* [%]
1	4.88	95	10.87	-	-
2	4.90	96	9.95	9.87	8
3	4.93	97	9.36	9.19	6
4	4.94	97	9.54	9.20	14

* grains with more than two trapped pores

The density of the samples is more or less the same, with the exception of sample 1 which has a lower density. On the other hand, the average grain size and the percentage of grains with exaggerated grain size and intragranular porosity is different. The nominal composition of the samples studied is the same and can be excluded from further consideration. The outstanding properties of samples 2 and 3 can therefore be assigned exclusively to the influence of sample microstructure and their stoichiometry.

In the case that the operating frequency is lower than the relaxation frequency of the wall displacement, hysteresis and eddy current losses prevail. The equation which relates the static permeability (μ_s), relaxation frequency (f_r) and microstructural parameter (D) is $f_r(\mu_s - 1) = 3/4\ (4\pi Ms)2/\pi zD$, where Ms is the saturation magnetisation /13/. In Fig. 3 the permeability spectra of the high frequency power ferrites are shown.

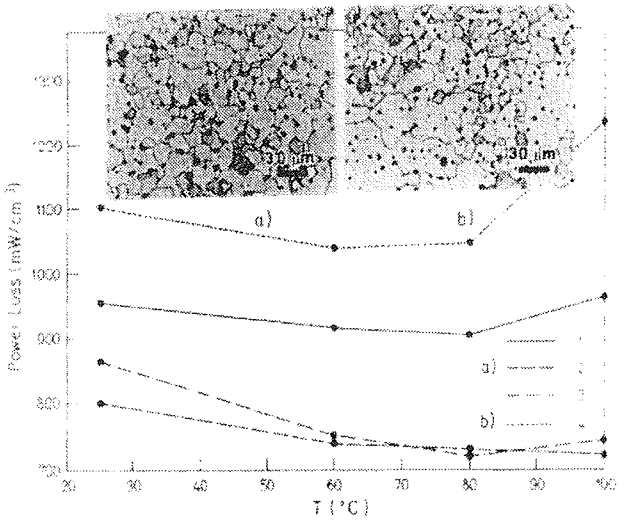

Fig. 2: Temperature dependence of core loss at 700 kHz (50 mT) for samples sintered at 1280°C and 21 vol % oxygen (sample 1),10 vol % (sample 2), 5% (sample 3) and 1 vol % of oxygen for sample 1 respectively and typical microstructures; a) sample 2 and b) sample 4.

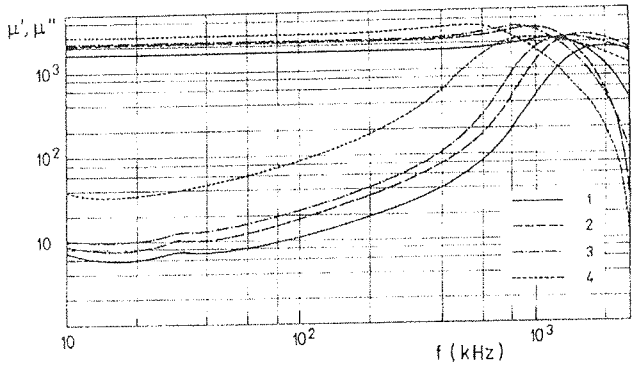

Fig. 3: Permeability spectra of high frequency MnZn-power ferrites for samples 1, 2, 3, and 4.

Table II: Permeability spectra of samples studied; relaxation frequency (f_r), static permeability (μ_s), the product ($f_r \cdot \mu_s$), the product, ($f_r \cdot \mu_s \cdot D$), and the amount of FeO present in the samples

Sample code	f_r [MHz]	μ_s -	$f_r \cdot \mu_s$ [GHz]	$f_r \cdot \mu_s \cdot D$ [KHzm]	[FeO] [%]
1	2.0	1800	3.6	39.6	2.15
2	1.8	2400	4.3	40.3	2.41
3	1.4	2500	3.5	32.76	2.48
4	1.0	3000	3.0	28.62	2.68

The values of the products $fr\ \mu s\ \overline{D} \equiv A$ in Table I, which is proportional to $M_s^2/ß$, gradually decrease indicating that the dumping ability of samples increases with the concentration of Fe^{2+} ions. All samples contain an equal amount of the four-valent ions Ti^{4+} and Sn^{4+} which when dissolved in the ferrite grains produce about 0.74 wt. % FeO. The rest is formed during the sintering at equilibrium conditions due to dissolution of the excess iron oxide in the spinel lattice and is $P(O_2)$ dependent. This part of the FeO and/or Fe^{2+} is not localised in Fe^{2+}-$Ti^{4+}(Sn^{4+})$ pairs and contributes to the damping mechanism, and thus decreases the relaxation frequency. In Fig. 4 the relationship between core loss per cycle (P/f) and the frequency is shown. A linear relationship was clearly found for all samples in accordance with the general expression for power loss

$$P/f = A + Cf \quad \text{where} \quad A = \int HdB, C = aB_m^2/\rho_{bulk} \propto D/\delta_{gr}$$

The eddy current loss of the samples, the grain resistivity and the grain boundary resistivity are given in Table III.

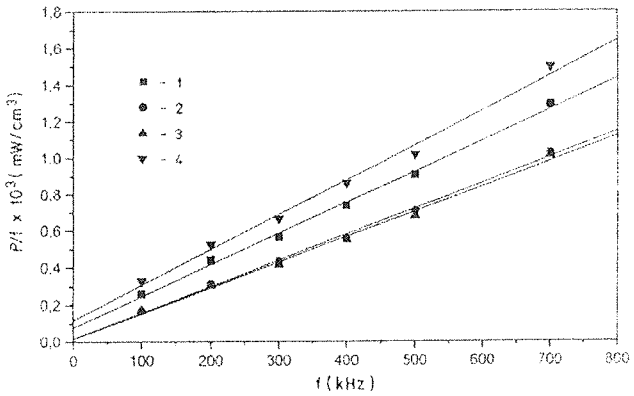

Fig. 4: Power loss per frequency vs. frequency for samples 1, 2, 3, and 4

Table III: Grain resistivity, grain boundary resistivity and eddy current losses at 80°C measured at 700 kHz (50 mT).

Sample code	Grain resistivity [Ω cm]	Grain bound. resistivity [Ω cm]	$P_E^{80°C}$ [mW/cm³]
1	7	63	833
2	8	64	686
3	7	66	686
4	7	22	931

Samples 1 and 4 show larger eddy current losses compared to the other two samples.

The eddy current loss depends mainly on the bulk electrical resistivity of the samples. The resistivity of a polycrystalline ferrite can be increased by increasing its grain boundary resistivity and/or reducing the grain size. At constant grain boundary resistance, the bulk resistance can be increased by reducing the average grain size and/or by increasing the number of grain boundaries $R_{bulk} = R_g + R_{g.b.}$. Samples 2, 3 and 4 exhibit smaller average grain size in comparison to sample 1 and therefore lower P_E losses. Sample 4 is an exception where the fraction of giant grains is relatively high. A higher fraction of these grains can substantially decrease the number of grain boundaries per eddy current path. On the other hand, in sample 1 neither are giant grains developed, nor is the grain boundary resistivity significantly lower. Besides, sample 1 has a higher total porosity which can create a demagnetisation field, a lower μ, and a substantial increase of the magnetic flux density and lead to an increase of the total loss. When considering grain boundary properties in electrical ceramics, AC impedance methods are widely used for their characterisation. When the experimental data are analysed and interpreted it is essential to have a model equivalent circuit that provides an acceptable representation of the electrical properties. In the MnZn ferrite ceramics considered it is well known that both inter- and intragranular impedances are present.

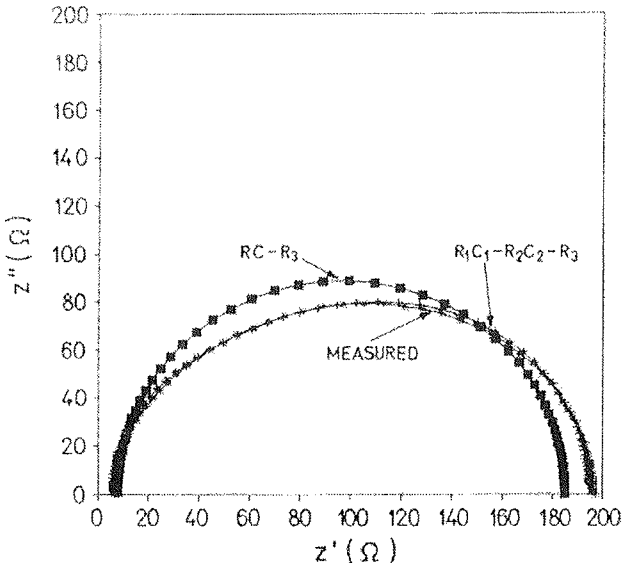

Fig. 5: Measured complex impedance spectra of doped MnZn ferrite sample doped with 0.2 wt% Ta_2O_3 sample with a fitted spectra with single RC value for the grain boundary and a fitted spectra in which the distinction is made between the extrinsic and intrinsic grain boundary.

In Fig. 5 a typical complex impedance spectrum is shown for the doped ferrite samples and a corresponding simulated spectrum when the distinction is made between an extrinsic and an intrinsic grain boundary, i.e. R_1C_1-R_2C_2-R_3. In addition, a simulated impedance spectrum where a single R and C value, i.e. RC-R_3 was used to fit the spectrum is also shown. Fig. 5 indicates that a simulated impedance spectrum where the grain boundary is separated fits the experimental measurements much better than those where a single RC element is used. This confirms that the separation of the grain boundary into an intrinsic and extrinsic part seems to be justified.

The electrical properties are determined in general by a series combination of such impedances which can be represented by a parallel RC element. From the complex impedance spectra of doped and undoped samples and the corresponding simulated impedance spectra, parallel R_1C_1-R_2C_2-R_3 elements were obtained. Once the equivalent circuits and corresponding elements of the circuits are obtained, these elements must be assigned to the microstructural characteristics of the material, provided that the measured response belongs entirely to the sample.

In the case where one would like to estimate the dimension and/or volume of a particular component in a sample using capacitance data, the permittivity of the region considered must be known. The samples studied are ferromagnetic and not ferroelectric, with a permittivity like that of an oxide, $\varepsilon = 10$. From the relation $C = \varepsilon_0 A/L$ a unit volume of such a material would have a capacitance of about 1 pF. Experimental data for capacitance C measured at 10 kHz for the samples studied were in the range from 3.2×10^{-6} to 4.2×10^{-7}F. Assuming A is unity, the thickness of this region must be reduced

$$\delta_{g.b.} = A\frac{\varepsilon}{C(pF)} = 3 - 21\,nm.$$

The capacitance is associated with thin non-ferroelectric regions, as indicated by their large capacitance value of a few μF, and these regions are therefore assigned to MnZn ferrite grain boundaries. According to the data obtained by fitting the measured data by an equivalent circuit, it is suggested that beside the extrinsic grain boundary a highly resistive surface layer on each MnZn ferrite grain can be present as well. The AC impedance spectra of the MnZn ferrite samples studied suggests that the electrical make-up of the MnZn ferrite ceramics is as shown in Fig. 6.

The resistances R_1, R_2 and R_3, representing the appropriate electrical elements (RC), must be related to the electrical scheme in Fig 6. R_3 can be assigned to the grain resistance due to the relatively low value of R_3, in accordance with the basic electrical properties of MnZn ferrite grains. On the other hand, R_1 and R_2 are related to the grain boundary and must therefore be assigned to the "extrinsic" grain boundary due to second phase formation at the boundaries, and to the "intrinsic" grain boundary due to the segregation effect.

In ferrites the basic electron conduction mechanisms have been studied by many investigators and reviewed by Klinger et al. /14/. Various models were proposed; however, the thermally activated hopping model has been shown to be appropriate in explaining qualitatively the electrical behavior of MnZn ferrites. The additional

electron on a ferrous (Fe^{2+}) ion requires little energy to move to an adjacent (Fe^{3+}) on the equivalent lattice sites (B sites). Under the influence of the electric field, these extra electrons hopping between iron ions constitute the electrical conduction. Therefore, any change in the divalent iron ion content in the spinel ferrite lattice and/or the distance between them is crucial to the intrinsic resistivity of MnZn ferrite grains, including the intrinsic grain boundaries.

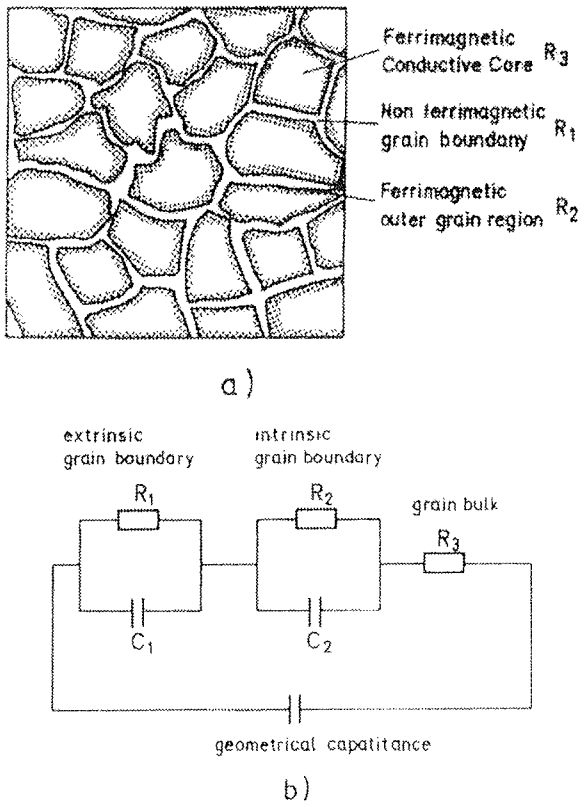

Fig. 6: Schematic model representing the electrical make-up: a) of polycrystalline MnZn ferrite; R_1-non ferrimagnetic grain boundary, R_2-ferrimagnetic outer grain region, R_3-ferrimagnetic conductive core b) the corresponding equivalent circuit.

If the introduction of another cation into the lattice causes a change in the valency distribution on the B-sites, then the number of electrons potentially available for transfer will be altered. On the other hand, the incorporation of foreign ions can change the distance between the B lattice-sites, which is crucial for the conduction mechanism. Thus, the formation of an "intrinsic" grain boundary in doped samples by the segregation of aliovalent ions must increase the intrincic grain boundary resistivity very much.

Due to their specific properties the grain boundaries are prone to the segregation of impurities. The driving forces for equilibrium segregation in ceramics are elastic and electrostatic interactions between segregation species in the bulk and in the interfacial region. The most important process occurring on the grain boundaries of MnZn ferrites during sintering are the segregation of aliovalent ions /15/, and Zn depletion /16/, caused by grain boundary diffusion of Zn to the surface of the sample and evaporation of ZnO from the sample surface. Besides, any change in the Fe/O ratio is usually identified on the grain boundary of MnZn ferrite grains.

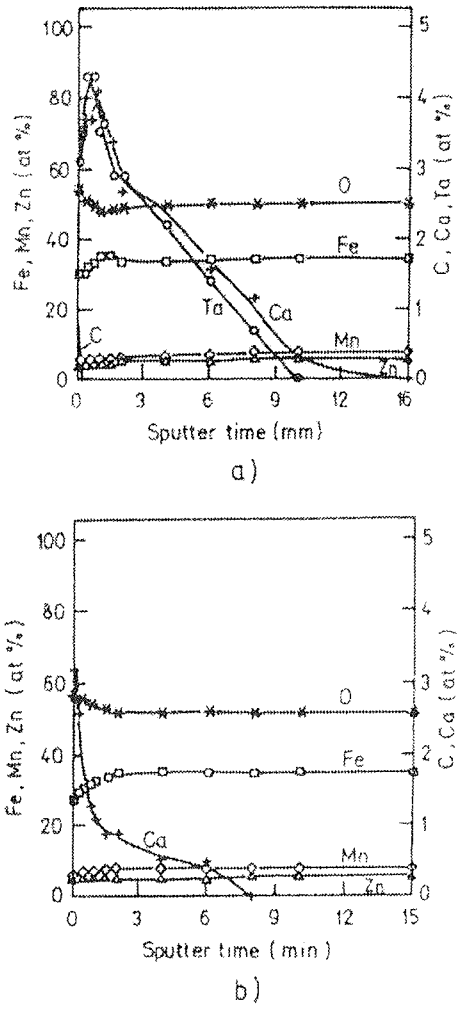

Fig.7(a,b): A typical AES concentration depth profile of MnZn ferrite grain boundaries containing Ta^{3+} dopants and Ca^{2+} impurities; Fig. 7a concentration depth profile of samples doped with Ta^{3+} ions and b) undoped sample where only impurities of Ca^{2+} ions can be identified

Extensive grain boundary analyses of MnZn ferrites were performed in the past /17,18/ where the grain boundary composition in the outer layer of MnZn ferrite grains was considered. Our results for grain boundary analyses are consistent with those previously reported. A decrease of the Fe/O ratio and a depletion of Zn was detected on the grain boundary of the samples analyzed. The segregation of Ca, which is an impurity, can be detected usually in ferrite samples exhibiting improved high frequency magnetic properties /19/ Figs. 7(a,b). In samples doped with Ta_2O_5 the segregation of Ta was confirmed, Fig. 7a. The Auger Electronic Spectra of fractured grain boundary surfaces showed the presence of a concentration depth profile of the aliovalent

ions Ca^{2+} and Ta^{5+} in the outer layer of the MnZn ferrite grains, and thus confirm the presence of an intrinsic grain boundary present in MnZn ferrite grains as identified by complex impedance spectra of ferrites studied.

5. FINAL REMARKS

Results reveal that the essential parameters which determine the P_E loss of MnZn ferrites in the frequency range up to 1 MHz are exclusively average grain size, grain boundary thickness and its resistance. Thus, when engineering the high frequency properties of MnZn ferrite the complex composition of the intrinsic grain boundary must be controlled in order to decrease the eddy current loss at high frequencies.

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MIXED SIGNAL ASICs - A MANUFACTURER´S VIEW

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Abstract: Mixed Signal ASICs play an important role in the ASIC market. In most applications, they fill the gap between internal information processing and the external world. This causes a need for a broad variety of microelectronic technologies aimed at fulfilling the often completely different requirements for supply and operating voltages, for input and output currents, for signal frequency ranges, for accuracy and signal resolution capabilities, for ESD, EMC and robustness in harsh environments etc.

Complex signal processing combined with analog front end in wireless and wirebound communication, high gate count embedded in high voltage interfaces for harsh environments in automotive and industrial electronic and the combination of signal conditioning in microsystems are the challenges for MS ASICs.

System integration on chip in submicron technologies including high performance analog blocks requires powerful and robust MS processes, a combination of high level design automation for digital blocks with interactively driven design tools for analog blocks and a changing cooperation between customer and ASIC supplier.

Mešana ASIC vezja - proizvajalčeva perspektiva

Ključne besede: polprevodniki, IC vezja integrirana, ASIC vezja, MS ASIC vezja za signale mešane, MS signali mešani, komunikacije žične, komunikacije brezžične, tehnologije mikroelektronske, zmogljivost visoka, tehnologije submikronske, trendi tehnologije, delitev tržišča, orodja snovalna, elektronika avtomobilska, elektronika industrijska

Povzetek: Mešana vezja igrajo pomembno vlogo na tržišču ASIC integriranih vezij. V številnih uporabah ta vezja premostijo prepad med notranjo obdelavo podatkov in zunanjim svetom. To ustvarja potrebo po širokem spektru mikroelektronskih tehnologij, ki naj bi zadostile velikokrat različnim zahtevam za napajalne in delovne napetosti, za vhodne in izhodne tokove, za različna frekvenčna območja signalov, za točnostjo in ločljivostjo signalov, za ESD in EMC odpornostjo v težkih pogojih delovanja itn.

Zapletena obdelava signalov, združena z analognimi izhodi v žičnih in brezžičnih komunikacijah, velika gostota elementov v visokonapetostnih vmesnikih v zahtevnem okolju industrijske elektronike in avtoelektronike ter prilagajanja obdelavi različnih signalov v mikrosistemih, so le nekateri izzivi za mešana integrirana vezja.

Integracija sistema na čip v podmikronskih tehnologijah vključno z zahtevnimi analognimi bloki zahteva zmogljive in robustne mešane procese, kombinacijo avtomatiziranega načrtovanja digitalnih blokov in interaktivna načrtovalska orodja za načrtovanje analognih blokov, kakor tudi stalno sodelavo med stranko in dobaviteljem ASIC vezijih

Introduction

Mixed Signal (MS) ASICs represent two coinciding worlds:

- the world of ASICs and
- the world of Mixed Signal IC-Design.

The ASIC world is part of the IC universe, which is expanding like the real cosmos after the big bang with unlimited speed but with some fluctuations (Fig.1).

The IC-market expansion is based on

- the, historically unprecedented, development of microelectronic technologies which is now rapidly approaching 0.1 μm (Fig. 2) and
- an ever growing demand of applications for processing, storage, generation and transfer of information starting from signal acquisition and binary handshaking in simple control systems and ending with personal and mobil computing, communication, multimedia and integrated microsystems.

From the first transistor in Si-planar technology in 1959 (Fairchild) over the first ICs with transistors, resistors and capacitances by Texas Instruments in 1960 and the first microprocessor with 2300 transistors in 1971 (Intel) until Intel´s Pentium II with 7.5 Mio transistors and 266 MHz clockfrequency in 1997, produced in 0.35 μm technologies (some versions now in 0.25 μm), the chip complexity has grown 10 times in six years (approx. 50 times in 10 years) and the chip performance (related to microprocessor power) has increased 10 times in eight years. The DRAM complexity is even growing with a factor four in three years almost exactly following

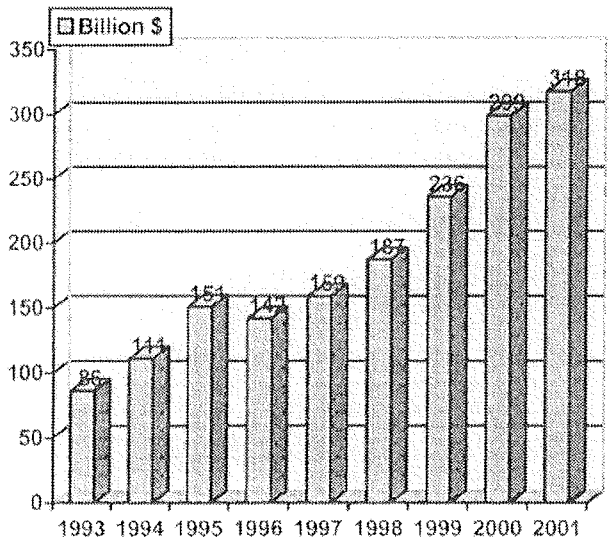

Fig. 1 Worldwide Semiconductor Market

Moore´s law (100 times in 10 years). Every 10 years the price/performance ratio (in stable currency) improved by a factor of 100.

Applying these breathtaking figures to the development of cars in the period 1960 - 1995, today one should be able to buy a Rolls Roys running 8 Mill. km with one litre petrol for less than 1.50 $.

Today highly improved production equipment in a perfect cleanroom environment allows the realisation of wafer defect densities in the order of 0.25 defects per sq.cm. Large chips with die sizes well over 1 sq.cm can be produced in volume production with yields exceeding 75-80 %. This trend is enforced by the econo-my of scale of growing wafer sizes leading to a more intense utilisation of the expensive production equipment. Nearly unlimited complexities can be integrated on chip with reasonable cost. The integration of separate functional components or subsystems on chip is substituted more and more by system integration on chip (or integration in dedicated chipsets). Memories are the only exception. Here the functional requirements for the main application areas (computers) with respect to memory size and speed („the hunger for information storage") have not yet reached a level of saturation, which would allow handling large memories like on-chip macros for system level integration. For instance, todays 64 Mbit RAMs are sufficient to store the information needed to code a genom of a bacteria; for the human genom 64 Gbit are required.

However, system integration has become a major target for many IC suppliers, because more and more customers discover the economy and relative simplicity of turnkey solutions in the form of systems or well defined subsystems on chip.

Especially ASIC suppliers are heavily confronted with this changing nature of the functional content of ICs. Indeed, system integration means the inclusion of product definition and functional system development in the ASIC development cycle, extending the classical implementation oriented IC design towards a complete product development. System design requires further specialisation and competence focusing. The broad range of applications served in the past by many ASIC suppliers has to be limited. New fabless design houses are filling the gap between specialised, system level supported IC and ASIC design and the need for serving an ever growing number of applications. Very often spin offs from universities or research institutes bring in special system level or architectural expertise, which is figured as starting capital of the new design house.

Also standardisation helps to bundle the technical requirements for similar applications or at least for similar subsystems and therefore limits this gap redu-cing the number of different components necessary for similar applications. Standards for cellular communi-cation systems like GSM and DCS 1800, DECT, CDMA or for broadband ISDN like ATM or for image coding like MPEG2 etc. have paved the way for open markets, higher volumes and represent an indispensable precondition to invest in very high integrated system solutions and components for them.

Parameter	1995	1998	2001	2004	2007	2010
Structure(μm)	0.35	0.25	0.18	0.13	0.1	0.07
DRAM (bits)	64M	256M	1G	4G	16 G	64 G
Gate/Chip	800k	2M	5M	10M	20 M	40 M
Supply (V)	3,3	2,5	1,5...2,5	1,5	1,2	0,9
Clock (MHz)	200	500	1000	1500	2000	2400
Metal-Layer	4...5	5	5...6	6	6...7	7...8
CPU-performance	15	30	40	120	200	240
I/O per Chip	750	1500	2000	3000	4000	5000

Fig. 2: CMOS Technology-Trends up to 2010

The technologies for most of the segments of the ASIC market - Gate Arrays including FPGAs, PLDs, Digital Standard Cell ASICs - follow the main stream microelectronic production processes with some delay (Fig. 3). However, driven by the price war in the DRAM sector and the quick alterations in microprocessor generations on the one side and the giant investment for new technologies and fabs on the other side, some large IC suppliers are pushing their way into the ASIC market using fabs and technologies, which were initially developed and used for DRAMs or microprocessors and which are no longer best suited for the newest technologies and products. Therefore, IC suppliers which concentrate on digital ASICs or on a mixture between dedicated logic ICs and digital ASICs are forced to speed up their development of minimum feature size technologies. All in all, the gap between the feature size of leading DRAM technologies and ASIC technologies becomes closer. In the area of MS ASICs (like in the Analog IC seg-ment) there are additional process requirements like analog performance, special RF or High Voltage features etc., which not only weaken this trend but lend a characteristic profile to the family of MS ASIC processes. For many applications specific performance parameters of active or passive devices are required which may outweigh digital performance parameters like gate density, gate delay, etc.

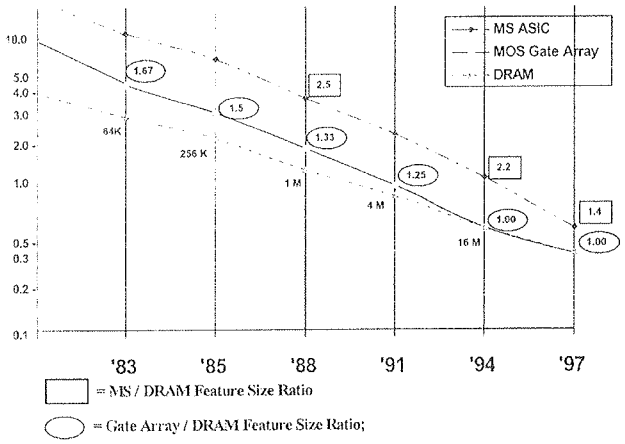

Fig. 3 ASIC Technology Trend

Very often the minimum size is not the most important requirement for MS ASICs (and even more for analog ICs), although with the growing content of digital blocks this basic characteristic of a process becomes increasingly important in the world of MS ASICs as well.

The specific requirements for some MS ASIC processes will be considered later.

The MS ASIC Market

Progress in process and technology development as well as the volume of investments in new fab lines and design tools are driven by the market situation. An ASIC manufacturer and even a MS ASIC manufacturer like Austria Mikro Systeme targets only a small, but important, segment of the IC market. However, this segment covers all application areas like Computing, Communication, Consumer electronics (the 3 large Cs), industrial and automotive electronics etc. and is closely linked to the whole IC market due to the simple fact that in most of the applications an appropriate mixture of the products of the different segments of the IC market has to be used.

The whole IC market, which drops in the critical year 1996 to an overall volume of $117 Bill., is growing with a compound annual growth rate (CAGR) of 19% . Memories and microprocessors/controllers represent nearly a two third share of the IC market. The dominant IC application areas are Computers with 55% of the worldwide IC usage (1996), Consumer Electronics with 16%, Communication with 15%, Industrial Electronics with 8% and Automotive Electronic with 5%.

Computer and Communication shares are expected to grow slightly in the next five years, however more important is the merge between computing and communication in networking and multimedia, the unbroken growth of mobile communication, the growing content of microelectronic components in cars, households and consumer goods and the entry of microsystems in the era of commercialisation.

According to Dataquest the content of microelectronic components in electronic products will double from 16% today to 32% in 2010, whereas the production of electronic products will triple in the same interval (750 Bill.$ in 1995). Microelectronics will penetrate in nearly every product. No reasons can be seen for slowing or even stopping the microelectronisation of todays technique.

ASICs will remain an important part of the IC production, offering the possibility of a customised solution for a special application and a given customer.

However, the nature of ASICs is changing. The boundary between ASICs and Application Specific Standard Products (ASSPs) developed for one application but for more than one customer become more and more fuzzy. Based on their own system definitions, ASIC vendors develop core products for selected application areas which can be used as ASSPs or modified for customer specific solutions (ASICs). This approach is especially important for complex systems and/or for a significant content of high performance analog blocks on chip which require a large design effort.

For Standard Cell or even Full Custom ASICs the time to market can be shortened considerably starting the ASIC design based on an appropriated core product or ASSP. Generally, in correspondence with the changing relation among design effort, production cost and the related customer benefits , the various segments of the ASIC market (Fig. 4) grow differently. Today (1996) the whole ASIC market with approx. $ 17 Bill. represents a 15 % share of the complete IC market. Due to the higher average sales prices per unit nearly four times, the market share in units is considerably smaller.

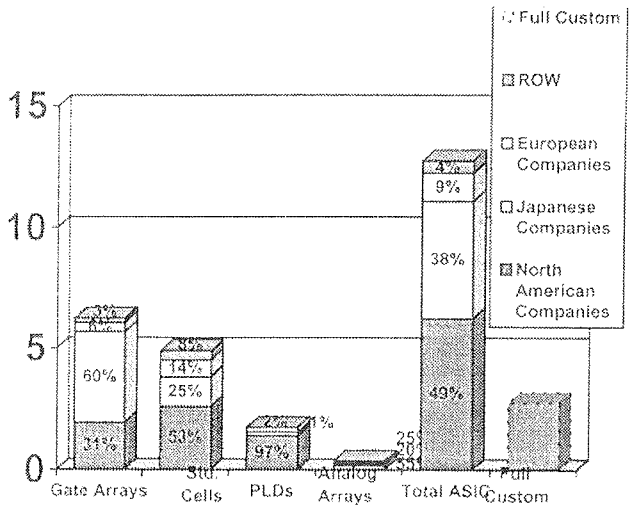

Fig. 4 ASIC Segment Market Share 1995

The ASIC market increases at an estimated rate of 18 % per year.

The fastest growing segment is (beside the FPGA subsegment) even the MS Standard Cell ASIC area with an expected annual growth rate of 26-30% (according to ICEs „ASIC 1997"/ „ASIC 1996"), which is well over the average growth of most of the other IC market segments. Some uncertainties in the whole MS ASIC area are caused by the lack of information on the Mixed Signal part of the Full Custom ASIC segment. The 26% to 30% are therefore related to the MS Standard Cell ASICs, which represent the largest part of the MS ASICs.

Gate Arrays are losing, complex PLDs are gaining some additional shares.

The driver applications for MS are

- the global wireless communication including cellular voice and data communication as well as multimedia and
- the local wireless or wire bound communication based on RF to Infrared local communication for voice and data transfer and for local multimedia access.

(Laurie Stanley from Cadence called this convergence of multimedia, communication and computing the consumerization of electronics /1/.)

In 1996, the market for cellular communication has seen more than 50 Mill users. For 1999 optimistic forecasts expect more than 500 Mill new subscribers.

Spin-offs are GPS, environmental, traffic and industrial control, medical care and households.

Austria Mikro Systeme is well established in the $ 6,2 Bill Standard Cell ASIC market and ranks sixth in the approx. $ 2 Bill MS ASIC market (1996). The Austria Mikro Systeme Group has to be placed as Number 5. MS Std. Cell ASICs represent more than 75% of the business of the company. The main application areas are Communication, Industrial and Automotive Electronics.

In front of the weak position of European companies in the IC market which serve only a 9% share of the worldwide IC market, the 14% share in the Standard Cell ASIC segment and the even higher share of more than 25% in MS-Standard Cell ASIC is a remarkable exception demonstrating the often stated European competence in Mixed Signal design and production. Austria Mikro Systeme is one of the representatives of this leading European position. The leading US publication „Semiconductor International" in its March issue rates Austria Mikro Systeme as one of the very few companies which will have a fundamental influence on the strategically important segment of ASICs in the future.

Driving Forces for Mixed Signal Design

MS design is not the simple sum of digital design of well defined parts of the chip plus transistor level oriented design of predefined analog blocks. The latter is typical for analog ICs. MS design is a tightly coupled design of digital and analog functions including their definition, architectural mapping, block specification, circuit design including MS simulation, and physical implementation.

Not seldom the analog part in modern ICs represent only a small part of the area. However the design time occupies an inversely large part of the whole design cycle, the design has a much higher risk and often causes redesigns.

There are three tendencies in the world of MS design:

1. the growing role of analog and MS effects and of MS parts in deep submicron digital ICs
2. the increasing importance of digital signal processing (DSP) forcing the substitution of analog functions by their digital functional equivalents
3. the rapid growth of MS ICs, especially ASICs and ASSPs

1. Analog effects at gate, block and system level in deep submicron digital ICs like interconnect delay, power dissipation, complicated timing behaviour of digital standard cells for a large range of operating conditions, substrate crosstalk, ground bounce and power bus noise, electromigration, dependencies from neighbourhood etc. confront the digital designer with typical MS design problems. Additionally, analog blocks like VCOs and PLLs for high performance clock distribution become an indispensable part of the design.

Most of the new problems in digital submicron design are attacked by the whole EDA industry and the large IC players by developing new tools, methods and design flows. Quick and safe solutions are necessary in order not to delay the comprehensive usage of the newest manufacturing technologies. New products like SNAKE TECHNOLOGIES´ Layin-software for substrate modelling and crosstalk analysis based on 3D extraction of coupling models, CADENCE´s 2 1/2 D extraction software or IBM´s power bus noise analysis methodology /3/ (not yet commercialised) demonstrate that not only the key problems of digital design can be effectively

solved but MS design can benefit from the „analogisation" of digital submicron design.

2. The tendency towards digitalisation of signal processing seems rather to increase the MS- IC world than to weaken it. Indeed, in the past, digital signal processing was mainly realised as PCB- integrated systems based on dedicated Digital Signal Processors and analog ICs for signal conditioning, pre- and postfiltering and AD and DA conversion. These solutions migrate more and more in one chip MS systems often including additional functions. DSP cores like GOULD´s PINE or OAK or Austria Mikro Systeme´s GEPARD as well as improved design environments for hardware-software codesign support this migration and open the way for new applications. Powerful analog blocks like high performance AD and DA converters are crucial elements in expanding the digital signal processing to higher signal frequencies, increased accuracy, low supply voltages and low power consumption.

3. The area of MS ICs covers a broad spectrum from simple extensions of digital circuitry towards the integration of analog I/0 functions up to the realisation of high performance analog and complex digital blocks on chip.

The functional and structural partitioning of an ASIC in analog and digital subfunctions and blocks requires a careful evaluation by experienced designers. The advantages of digital parts like robustness and easy design as well as the disadvantages of analog circuitry like sensitivity against noise disturbances and interference, susceptibility to process variations, to mismatching, to inaccurate device models, high design effort and risk etc. must be weighted against the cost of an appropriate manufacturing process, the die size, the power consumption, the reliability, the overall design costs, the possibilities of sharing design work, the test effort etc. In conjunction with the growing submicron possibilities, digital realisations will substitute analog functions where possible.

However, very often the driving force for an analog realisation of functional blocks is the impossibility of a digital realisation. The limitations for digital realisations are determined by

- the necessity of analog interfaces to the external world
- high signal frequencies not allowing precise AD-conversion and/or real time digital signal processing

For many interface functions, digitalisation is taking place, too, e.g. for driving an external load with low pass characteristic like a loudspeaker membrane. Here the analog output amplifier can often be substituted by a simple digital output stage driven by a pulse modulated signal. Pulse based techniques (pulse width, pulse frequency, pulse density, stochastic logic) are the favourites for digitalisation at the border area between analog and digital. However, for high voltage environments or smart power applications an analog signal conditioning, power matching and/or distur-bance handling is necessary. Special high voltage processes with usually purer digital performance are required here to handle the necessary voltage range.

Mixed Signal Process Technologies:

MS processes have to keep the digital performance of the basic process but are enhanced by different features necessary for the realisation of analog blocks. It has to be emphasised that one of the basic requirements for a MS process is not only the addition of new analog properties respectively process modules like linear poly capacitances and resistances or special active devices but a perfect control and an excellent characterisation of the basic process itself. Low threshold voltage spread, good matching properties of active and passive devices, stable and well controlled AC-parameters of MOS transistors in the saturation region, low resistive and capacitive device and interconnect parasitics etc. can be obtained using a well controlled and characterised digital process may be with slight modifications as for instance for improved active area surfaces necessary for better noise behaviour.

Of course, dedicated processes for MS RF or for High Voltage applications have to start from appropriate device concepts rather than to take a high density process and to extend this process for RF or HV requirements.

Let´s consider the most important requirements for MS ASIC technologies and some consequences for the MS design:

1: Noise

The accuracy of voltage (or current) levels in digital systems must be sufficient for an error-free recognition of the status information. In binary systems only two levels have to be differentiated. In analog systems the signal is characterised by a continuous set of states which must be recognised with an accuracy sufficient for the reconstruction in a given failure interval. The accuracy limits are determined by static and dynamic distortions and by the Signal to Noise Ratio.

The theoretical limit for the required power to achieve a given SNR over a given bandwidth f is

$$P = 8xkTxSNRxf$$

In practice, the additional power consumption due to auxiliary circuitry as well as the additional noise coming from the whole environment will increase the necessary power by up to more than one order of magnitude. However, the basic dependencies such as the usualy linear impact of SNR and bandwidth are sufficiently correct reflected: good SNRs over large bandwidths require large currents and consequently large transistors.

This situation is nearly independent on the process technology because the SNR for MOS transistors does not change significantly with the transfer to a new submicron technology.

Indeed, for the same device area the thermal noise of a transistor can be slightly reduced due to the increase of Gm. However, this will be roughly compensated by the reduction of the power supply in the deep submicron area shown in p.2.

Consequently, the area of low noise analog cells will remain nearly constant for different CMOS technologies whereby the digital cells approximately follow the area reduction of the minimum devices.

In Fig. 5, a Mixed Signal ASIC with relatively high analog content in the form of some low noise amplifiers is shown, ported from 1.2 μm to 0.6 μm. The analog part couldn't be reduced. The digital part was reduced in area by nearly a factor of four.

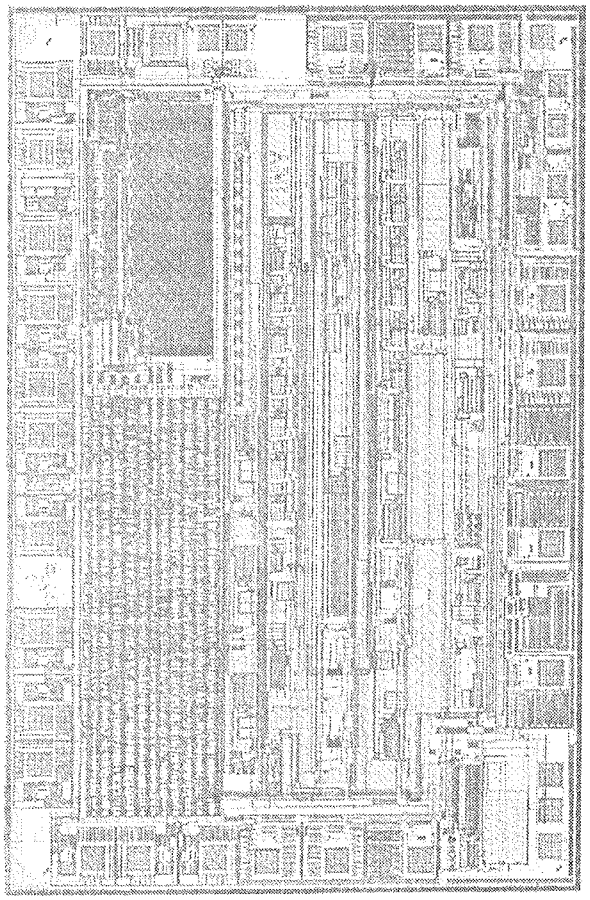

Fig. 5 Mixed Signal ASIC

As can be seen, the improvement of analog noise performance is barely related to the minimum feature size as is the case for digital systems. However, in case the noise is not the dominant factor, analog design benefits from improved dynamic behaviour of active and passive elements in the submicron area.

2: Power consumption

The on chip system integration requirement drives MS technologies in the submicron area. ICs with large digital part as for instance baseband chip sets for mobile communication represent an increasing share of MS ASICs. Therefore, gate density and speed remains an important criteria and the trend to submicron processes is nearly as important as for digital processes (at least for CMOS based technologies). The typical power problems of submicron LSI are imported in the MS area. Roughly speaking, they can be divided into the followings:

- power necessary for fast internal circuit switching must be dissipated
- large currents are needed for fast output drivers and limits their numbers
- the large currents need lower wiring and bonding resistances

For instance, the switching power P = fxCx V^2 for a f=250 MHz clock speed and an overall active load of C=10 000 pF results for a p-p swing of V=5 V in more than 60 W which have to be dissipated requiring a careful thermal management. To avoid unacceptable derating the junction temperatures should be not higher than approx. 120 °C. Low thermal resistances between junction and package as well as special, expensive packages with enlarged surfaces and good airflow are required. However reducing the peak to peak swing to 1 V drops the power down to 2.5 W - a value which can be much more easily handled. Sophisticated design techniques to reduce switching activities (asynchronous logic) and/or load capacitance (Full Custom design) can further help to decrease power consumption. However, the quadratic impact of V is the most important limitation forcing the decrease of the supply voltages at least at the entry to the sub-half micron area (Fig.6). The consequence is a reduction in the dynamic range of analog signals. This, in conjunction with the nearly constant threshold voltages of MOS devices (lightly decreasing with smaller feature sizes), requires new and more powerful circuit techniques to be developed, with the emphasis on low current and low power even at high frequencies.

The low power design of analog blocks at low voltage supply is one of the biggest challenges in deep submicron MS design.

The current necessary to switch a single output at a given speed is I = CxdV/dt.

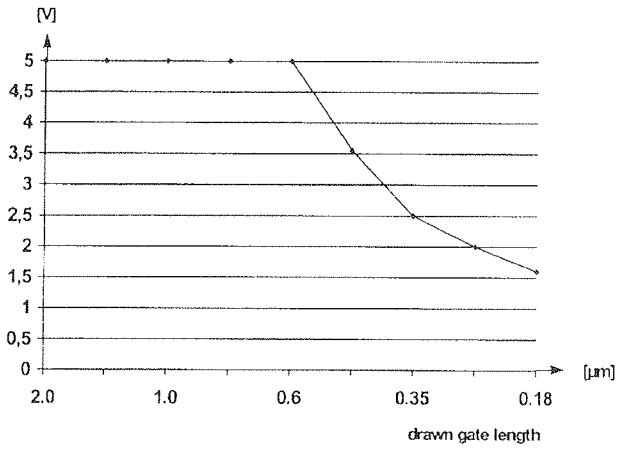

Fig. 6 Supply Voltage Reduction

Assuming a load capacitance of 10 pF, rise time of 100 psec and a swing of 1 V, a peak current of 100 mA is necessary. Only a large transistor in the order of some hundreds of the minimum device will guarantee a small enough output drop of say 100 mV. Intermediate buffers between the minimum internal gate and the final output device are needed. Therefore, a large area is required for handling the output. For a 32 bit bus interface, the peak current will reach 3.2 A. The examples can be easily extrapolated for higher speeds and gate counts.

Adding together current hungry outputs, switching power and current consumption for even current intense analog blocks, a power consumption in the order of Watts become a typical value rather than an exception. According to SIA´s roadmap the maximum power consumption for ASICs will be in the order of 5 W/ sq.cm for 0.5-0.35μm technologies and increase up to 10W/sq.cm for 0.18μm technologies.

The required currents of some Amps must be brought on chip and distributed. This means that power distribution in bond and interconnect wires becomes a significant factor. The cross-sectional area must be high enough and the specific conductance must be decreased. Copper-doped aluminium instead of aluminium seems to be the next choice for the submicron metallisation followed possibly by pure copper wires.

The consequences for analog blocks on chip are positive because analog parts do not shrink in the same order as digital logic with the migration to submicron technologies. The internal interconnect wires may remain in the same dimension as active analog elements. Therefore the weight of resistive parasitics should decrease.

3: Matching

Good matching of active and passive devices is one of the most important criteria for analog design. The process dependent parameter spread of all devices is in the order of some percent. Typical 3 sigma values are well over 10%. The only way for the construction of precision analog blocks is to exploit the much better relative accuracies of devices which inversely improves with the distance between them.

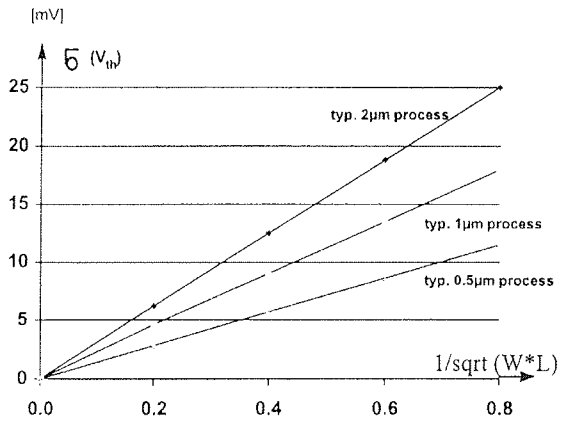

Fig. 7 Area Dependence of Vth Matching

The matching parameters improve for submicron technologies. According to /4/ the threshold voltage matching for a 0.5μm process is more than two times better than for a 2.0 μm process. Fig. 7 shows this behaviour for different transistor areas.

Passive linear elements like poly resistors and capacitors in Austria Mikro Systeme technologies can be matched with accuracies in the order of 0,1% or even less, high resistive poly resistors with 0.15-0.3% precision, however according to Austria Mikro Systeme´s internal measurements, there is no signifi-cant improvement with scaling down technologies.

4: High frequency analog processing

Wireless communication is the driving force for the on chip integration of high frequency analog processing (as for low noise input amplification, up and down mixing, synthesis of local oscillator frequencies etc.) together with analog IF and/or baseband modules and digital baseband processing / system control.

For input frequencies in the GHz range fast bipolar transistors must be combined with dense CMOS devices leading to modern BiCMOS processes. Modern BiCMOS processes like Austria Mikro Systeme´s 0.8 μm BYE (Fig. 8) combine

- vertical npn-transistors with high ft and low parasitic capacitances to substrate
- capacitors and linear resistors with low parasitics
- CMOS devices and
- the possibility for the integration of inductances.

	0.8 µm	0.6 µm
Status	production	in developt.
Technology	2 poly/2 metal	2 poly/2 metal
	15 masks	16 masks
poly/poly caps	+ 1 mask	+ 1 mask
High Res resistor	+ 1 mask	+ 1 mask
trench isolation	optional	+ 1 mask
CMOS		
Vth/Vtp (V)	0.70/-0.75	0.70/-0.80
L_{eff}	0.65 µm	0.55 µm
Bipolar		
Ft	12 GHz	20 GHz
Beta	110	110
Cjs (fF)	57(trench:30)	45(trench:20)

Fig. 8 AMS BiCMOS Technology

The low impedance substrate requires special attention to avoid noise coupling between CMOS logic and analog blocks (e.g. differential logic in ECL or CMOS with separate substrate connections). SOI processes which offer excellent substrate isolation properties, are under discussion. SiGe Heterojunction Bipolar Transistors integrated in CMOS may be another alternative to improve RF integration on chip.

5:High Voltage inputs and outputs

At present some automotive and industrial peripheral ASICs must withstand static levels up to 50 V and even higher impulse levels. Special high voltage NMOS and PMOS transistors must be integrated. To easily adapt low voltage parts, floating NMOS, PMOS and DMOS devices are advantageous. More expensive processes have additional vertical bipolar devices (BCD processes). Austria Mikro Systeme´s 2.0μm and 0.8μm CMOS technologies are used for ASICs with high voltage in- and outputs, voltage regulators and level shifters as well as with analog and digital blocks working at 5V supply voltage, which is generated on chip. The transfer of this concept in even deeper submicron areas is a big challenge as well as the extension of the voltage range up to 100V and higher, which opens the way in complete new application areas.

6: Adding Microsystem Technologies

Microsystems are leaving the halls of academic research and entering into a growing number of indu-strial and commercial ventures. With the industrialisation of microsystems the link between microelectronic and microsystem technologies have become closer and closer. For cost reasons, microelectronic compatible technology steps, which can be piggybacked to a MS-base technology, have proven to be crucial for the success in microsystems.

However, microsystems are not based on a generic element as is the case in micro-electronics. Here the transistor is used as a switch for voltages (or currents) in digital systems or as element operating voltages and currents at the same time in analog systems. Microsystems bring in additional physical domains like mechanical deflections, electric, magnetic and electro-magnetic fields - later up to optical wavelengths etc. Handling these domains usually requires exploiting effects and structures, which are foreign to microelectronic systems. Some well known exceptions are the usage of „parasitic" dependencies in microelectronic structures like the temperature dependency of transistors or resistors which can be the basis for temperature measurements, or the dependency of current distribu-tion in a resistive plate (n-well) which can be the base for magnetic field measurements by constructing Hall elements on chip. However, even in these cases, special package technologies for adapting the chip to the new application must be added.

Generally, a nearly unlimited number of already existing and new technologies has to be integrated in microelectronics to cover all possible effects. A carefully evaluated selection of piggyback technologies is necessary to cover effects and applications as much as possible.

Austria Mikro Systeme has developed a special etching technology for bulk micro-machining and a special joining technology for sealing together conducting Si-structures. So, mechanical beams and membranes can be integrated in an MS ASIC. These technologies open the way to a broad range of acceleration and pressure sensors.

Similar combinations - some of them integrated under one roof, others handled in cooperation between different technology suppliers - will enhance MS proces-ses and enforce the merge between microelectronics and microsystems.

7: Robustness and statistical models

Typical volumes for ASICs cover a broad range from some thousands up to millions of units. Prototype runs for products under development represent very low volume production. MS ASICs are implemented in the best suited, but different processes. Therefore, an ASIC fab has to run a broad spectrum of different products in different processes and relatively low volumes.

Due to the increasing wafer size (8" and even 12" wafers) the number of wafers needed for a given product will decrease down to single (and sub-single) wafer production. Statistical monitoring of fab in-line and electrical test parameters will become insufficient for process fine tuning. Robust, insensitive against small modifications of primary process input parameters (equipment, material etc.) processes have to be established based on sensitivity simulations.

However, robustness does not only mean insensitivity against primary process parameter variations but includes insensitivity against environmental parameters like humidity, pressure, radiation as well as ESD, EMV and latchup. A basic requirement is a negligible impact of a given layout on the electrical test and device parameters.

The process sensitive design of high performance analog blocks as well as the analysis of sensitive MS effects require a hierarchy of statistical models of electrical test parameters, device model parameters, parameters of the elementary building blocks and of subsystems. This hierarchy can be used for statistical simulations at various levels and for optimisation of a given design (design related yield improvement). Statistical matching models must be integrated. The methodology for automatic generation of the parameter distributions for the various models at different design levels as well as the automatic generation of compact parameter sets for Monte Carlo simulations at this design levels has to be improved and integrated in the standard MS design flow. Hierarchical optimisation techniques are needed for a sophisticated truncation of the parameter space at a given design level.

European semiconductor companies have concentrated their efforts to develop sophisticated mixed analog/digital sub half micron processes in the framework of the European SHAPE project. The goal is to further improve the good position of European companies in the MS area. Participating in SHAPE Austria Mikro Systeme focuses now on the implemen-tation of a powerful 0.35 μm MS process fulfilling the above mentioned criteria.

MS Design Tools and Environments

Design efficiency is the main target for creating MS design tools and environments. Efficiency includes safety because any faulty design may cause an additional fabrun and a redesign.

The growing gap between chip complexity and design productivity must be closed

- by fully integrated design environments even for MS design
- by standardisation of tools and languages
- by rapidly extended reuse of blocks, subsystems and complete designs.

Today, the leading edge MS design systems are top down oriented and based on a combination of second generation analog Hardware Description Languages like HDL-A, VHDL-A,VERILOG-A and well introduced digital HDLs like VHDL or Verilog.

Austria Mikro Systeme offers front-to-back design kits for CADENCE and MENTOR tools. Special userware and scripts guarantee a smooth integration and fast simulation.

The principal design flow is shown in Fig. 9. a and b.

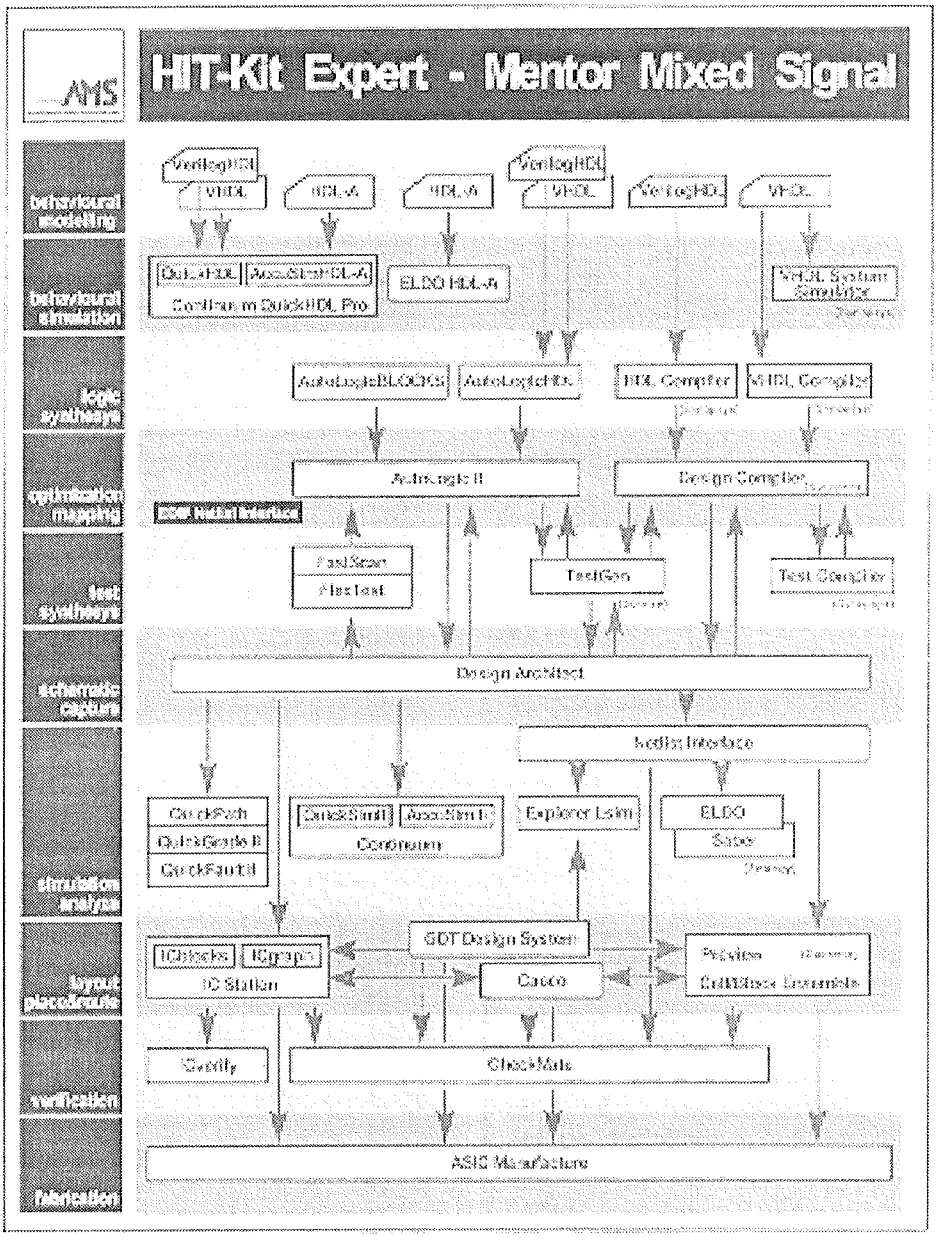

Fig. 9 a

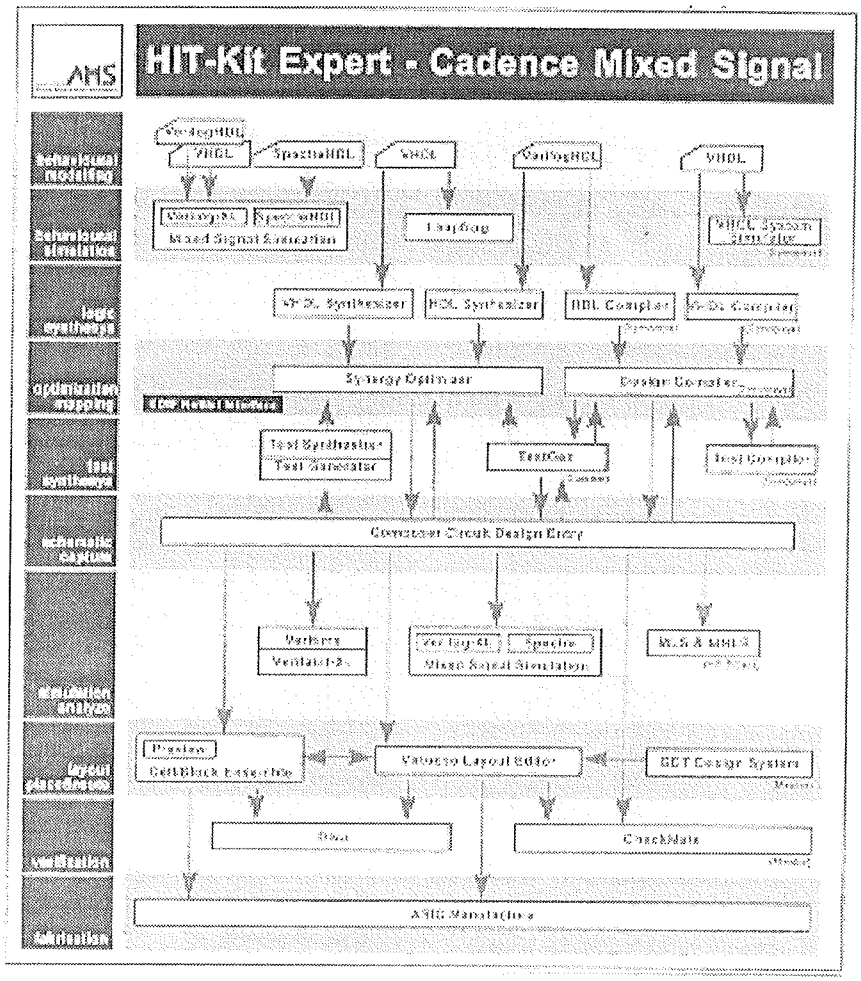

Fig. 9 b

Block type	Flexibility vs.predictability	Representation	Process technology	Portability
Soft	Very flexible, unpredictable	Behavioural: synthesizable RTL-description or netlist of generic library elements	Independent	Unlimited
Firm	Flexible, unpredictable	RTL, blocks: synthesizable RTL code or netlist of generic library elements, structurally and topologically optimised by floorplanning, placement for specific process families (not routing)	Generic	Library mapping
Hard	Inflexible, predictable	Polygon data -Layout	Fixed	Process mapping

Fig.10. Reusable blocks

HDL-A in combination with VHDL, Verilog A in combination with Verilog and other combinations can be used for high level simulation of MS systems. Different simulation techniques can be applied. Either cosimulation back-planes for synchronisation of analog and digital simulators such as ELDO, SpectreHDL (later with fully integrated Verilog A simulator) on the one hand and LEAPFROG, Quick-HDL on the other hand or digital extensions of analog simulators as announced for ELDO are state of the art. The EDA vendors permanently try to improve the tools and methodologies. The situation is changing very quickly confronting the design houses and ASIC suppliers often with new releases despite not having reached satisfactory performance level using the last release. Despite the success in language standardisation and simulation environments, there is still a long way to go until simulation engines become available based on standardised languages describing digital and analog functions with the same tool.

Verilog A/MS being the analog/mixed signal extension of Verilog by Open Verilog International (OVI) may be one of the candidates. Verilog A/MS standard was taken by the IEEE to create a more general version, compatible to the IEEE 1364 Standard from 1995. A new standard - IEEE 1364 - 1998 is planned and will be certified next year. An analog/mixed signal standard for VHDL-A is still missing.

Standardised MS HDLs shift the design from a schematic based methodology to a language based one. They are not only the precondition for the top down design but are absolutely necessary for Intellectual Property (IP) reuse, because proprietary descriptions are a serious barrier for mixing and matching foreign and own macros.

IP reuse has become a catchword. The invoked vision of a 90% share of reuse in designs in 2001 against a maximum of 10% reuse in 1991 seems to be unrealistic at least for MS designs.

However, the methodology and standardisation efforts for IP reuse are growing fast and are supported by a group of more than 80 leading electronic companies. The future reuse of System Level Macros (SLM), Cores and Megacells shall be based on the Virtual Socket Interface (VSI) concept, defining the form and content of information which has to be passed from the IP creators to the users. Interface standards shall transform the blocks into virtual components that fit into virtual sockets at functional and physical levels.

Soft, firm and hard blocks (Fig. 10) are the basic elements for a block based design.

A steadily growing number of companies are entering the IP supplier community. Nearly 2/3 of the worldwide IP business is created in California. However, only very few IP creators offer MS or analog blocks.

The reasons are principal: Process and design sensitive analog blocks have to be represented as hard blocks. Process mapping is then necessary which limits the applicability of IP reuse in MS design.

Analog synthesis would help to shift these borders. However, synthesising multi-parametrical, multistructural and multicriterial analog blocks is not comparable with digital synthesis. Digital synthesis is an intelligent decomposition of Boolean functions. The existing approaches for analog synthesis like simulation or equation based selection of structures and parameters or design plan based iterative searches are in fact analytic methods, applied to different representations of more or less predefined segments of the search space. Even the choice of the necessary minimal dimension of the structural search space is an unsolved problem.

Analog synthesis is not a problem of computational power but of adequate modelling of analog functions and their decomposition into elements, which can be mapped onto simple topological structures. Progress in analog synthesis will be made only in small steps. IP reuse of analog macros will remain rather the exception than the rule. However, the creation of analog macros by specialists or specialised small teams , which offer appropriate support for the adaptation of these blocks to a target process, seems to be a promising way for the reuse of analog core competencies.

Conclusion

Mixed Signal ASICs are quickly entering the sub half micron technologies. The integration of complex systems on chip changes the nature of design. System design aspects become as important as the implementation. Specialisation at system level changes the whole IC industry, creating fabless design houses supplementary to the well established in-house development of IC companies. Foundry business is growing correspondingly. The MS ASIC industry supports this trend offering steadily improving design support at the implementation level. Dedicated MS processes and powerful design tools are being developed and made available to customers and design houses. Analog effects such as noise, parasitic couplings, distributed system behaviour at RF, on chip statistical variations of device parameters etc. must be simulated and integrated into the top-down and bottom-up design flows. The standardisation of MS hardware description languages for the behavioural description of blocks and ICs supports shared design and IP reuse. High performance MS ASICs will be used in well known application areas such as communication, industrial and automotive electronis and will open the door for new applications, many of which will be in conjunction with the entry of microsystems in all spheres of our daily life.

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ASPECTS OF SUBMICRON BiCMOS TECHNOLOGY INTEGRATION

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Key words: semiconductors, CMOS technologies, submicron technologies, IC, Integrated Circuits, BICMOS technologies, MS, Mixed Signals, basic bipolar modules, cost relations, technology trends, SiGe HBT, Silicion-Germanium Heterojunction Bipolar Transistors, ASIC BICMOS processes, BJT, Bipolar Junction Transistors, transistor architectures

Abstract: Despite tendencies that deep submicron CMOS technologies are replacing device solutions formerly realized in BiCMOS processes several applications for mixed signal digital analogue applications still require the performance of integrated BiCMOS processes. The issues of advanced process module integration (buried layers, trench isolation, self-aligned BJT and SiGe HBTs) into submicron BiCMOS processes will be covered with additional emphasis put on aspects arising from ASIC manufacturing.

Pogled na integracijo podmikronskih BiCMOS tehnologij

Ključne besede: polprevodniki, CMOS tehnologije, tehnologije submikronske, IC vezja integrirana, BICMOS tehnologije, MS signali mešani, moduli bipolarni osnovni, odnosi cenovni, trendi tehnologije, Si-Ge HBT transistorji bipolarni heterospojni, ASIC BiCMOS procesi, BJT transistorji s spojem bipolarnim, arhitekture transistorjev

Povzetek: Kljub željam, da bi podmikronske CMOS tehnologije nadomestile nekatere elektronske rešitve do pred kratkim izvedljive le v BiCMOS procesih, nekatere mešane, analogno-digitalne uporabe še vedno zahtevajo električne lastnosti, ki jih ponujajo samo integrirani BiCMOS procesi. V prispevku je obdelana integracija naprednih procesnih modulov, kot so pokopane plasti, izolacija s kanali, samonastavljivi BJT in SiGe HBT bipolarni tranzistorji, v podmikronske BiCMOS procese s stališča proizvodnje ASIC integriranih vezij.

1. Introduction

Although a bipolar transistor was the first semiconductor device demonstrated in 1947 by J. Bardeen, W. Shockley and W. Brattain, it was more or less the first realization of MOS technology in 1962, which lead the way to a worldwide growth of a semiconductor industry in the 1970s and 1980s. Due to the tremendous industrial impacts of silicon based semiconductor technology some people already address our current century as the „silicon age". The continuing advances in silicon integrated circuit technology have lead to today's VLSI and ULSI (very and ultra large scale integrated) circuits with up to several million transistors per single chip. The advantages of high density and low power consumption have made CMOS processes to the leading silicon fabrication technology. Although the implementation of both CMOS and bipolar structures on the same chip has already been demonstrated in the late 1960s /1/, the importance of BiCMOS processes emerged only in the late 1980s. The unavoidable drawbacks of the implementation like technology complexity and additional costs delayed its availability as a widely offered technology.

Two major facts have given rise to the BiCMOS technology in the last decade: growing demand for higher speed and better performance for analogue and mixed signal circuits and the reduction of some drawbacks related to BiCMOS processing, since the CMOS complexity has increased and many CMOS and bipolar process steps have converged.

The usage of BiCMOS process technology nowadays allows realization of mixed signal circuit applications 1-2 generations ahead of CMOS, unless high density digital functions set the requirements for dense chip layouts.

This article will give an overview of the basic bipolar modules used in submicron BiCMOS processes, their complexity and cost relations and an outlook to the next technology generations incorporating SiGe HBTs.

2. BiCMOS Technology for ASIC applications

Offering BiCMOS technology for mixed signal ASIC applications has to focus on the balancing between device performance and cost/complexity in manufacturing and design, as a broad range of applications for different customers has to be supported with design kits and simulation models. As BiCMOS gate array concepts can not really fulfill all requirements with respect to custom-specific mixes of bipolar and CMOS compo-

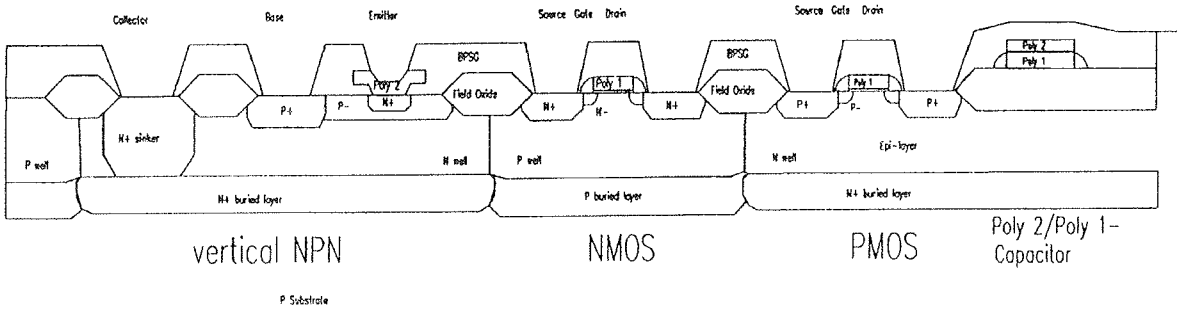

Fig. 1: Schematic cross-section of basic device elements implemented in a single poly BJT BiCMOS process /2/

nents together with resistors and capacitors the focus is put here on custom specific layout processing.

For an ASIC manufacturer not only the additional costs of highly integrated processes are of major interest, but also the associated increase of manufacturing times can be crucial with respect to fast turnaround cycles. Modular concepts for the introduction of additional process modules are envisaged to help decrease process complexity. It is even beneficial to try to reuse modules in different process technologies to keep a low number of complex process modules to be maintained. An optimum ASIC BiCMOS process will therefore try to fulfill most of the feasible applications, be as far as possible identical with the base CMOS processes and offer optional modules for special high performance functions.

2.1 Transistor architectures

2.1.1 Single poly BJT

Submicron BiCMOS processes typically incorporate buried layer architecture with a subsequent epitaxial Si-layer for formation of the twin well structure. This buried collector is contacted by a highly doped sinker to reduce the collector resistance required for high current drive applications. The BJT (bipolar junction transistor) of figure 1 is constructed by a single poly-Si layer used as emitter. In submicron processes the poly emitter module has emerged as the state of the art technology. Here the formation of the n^+ emitter contact is done by out-diffusion of Arsenic dopants from a poly-Si layer deposited in the emitter window over the base, thus allowing the formation of a very shallow emitter junction. Although there exist already sophisticated models for the poly emitter, which allow to predict the device characteristic and its various influences very well, the exact current gain mechanism is still not explained in every detail /3/.

In figure 1 the external base contacts are formed by P+ implants, usually done simultaneously with the P+ source/drain implant. The implementation of this type of bipolar transistor is commonly realized in BiCMOS processes from 1.2μm down to 0.6/0.5μm by the addition of only 3 - 4 extra masks to a double poly CMOS process (see also table 1). The performance of this architecture is limited to maximum transit frequencies F_T of 14 - 20 GHz.

For analogue applications f_{max} the maximum oscillation frequency is together with F_T an important figure of merit showing the transition performance. f_{max} is given by the simplified expression:

$$f_{max} = \sqrt{\frac{F_T}{8\pi R_B C_{JC}}} \qquad (1)$$

Consequently, to improve process performance we need a high F_T value, a low base resistance R_b and a low base-collector capacitance C_{jc}.

Especially for analogue applications the limitations are often set by R_b and the parasitic C_{jc}. The base resistance is made up by the contributions from the extrinsic P+ contact, the intrinsic part between P+ and the emitter region and the pinched base resistance under the emitter. Closer spacing of P+ to emitter is usually limited by lithographic variations, while the bipolar base doping is limited by the device operational characteristic. The base doping and width has to be optimized for the bipolar parameters current gain β, electrical breakdown voltages and leakage currents and base resistance. As the extrinsic P+ is the main contribution for the parasitic base collector capacitance C_{jc}, double base contacts to each side of the emitter for lower R_b consequently increase the required area and the parasitic capacitance C_{jc}. Thus layout optimization is essential to achieve the optimum bipolar transistor performance.

An additional enhancement, which is widely incorporated, is the salicidation of the base areas and the emitter poly /4/. It reduces the sheet resistances to a few Ohm/□ and allows also denser designs e.g. by strapping the emitter contact outside the active area.

2.1.2 Double poly self-aligned BJT

The limitations of the single poly BJT with respect to the parasitic components can be improved by the implementation of a double poly self-aligned BJT (figure 3). The base area is here formed by P+ poly in direct contact with the substrate, while the poly emitter is self-aligned in between /4/. Further improvements of the high frequency performance can be achieved with optimization of the collector and buried layer doping /5/.

The advantages of the self-aligned architecture are clearly depicted by the small P+ areas thus achieving

a reduction of the active area required for emitter and base of typically more than 50% for a double base contact bipolar transistor. Consequently the base collector capacitance C_{jc} is reduced together with the base resistance, as the P+ poly can be placed much closer to the emitter due to its self-aligned character. However, the critical part of this transistor architecture is the formation of the spacers and the integrity of the emitter area. This can lead to the use of three different composite layers (e.g. oxide, nitride, poly) for the spacer, if integration as a submicron BiCMOS process is envisaged.

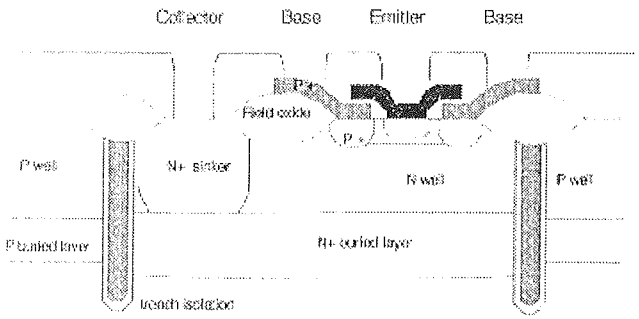

Fig. 2: Schematic cross-section of a double-poly self-aligned NPN BJT with additional poly/oxide filled trench isolation

Due to this complexity this process type is not widely offered in ASIC BiCMOS processes with geometries down to 0.6μm. However, for further scaling and the demand for higher performance this structure is mandatory in the submicron regime beyond.

Further improvements for the Si BJT focus on the base thickness and doping. Implanted and diffused base regions are limited in their width and achievable doping level due to defect enhanced Boron diffusion. Small base width and high doping must be balanced with the limitations often set by the electrical punchthrough characteristics and emitter/base leakage currents.

Further investigations have concentrated on epitaxial Si base deposition allowing a better boundary definition and higher base doping, but this approach limits the subsequent thermal budget for further process integration /6/. Although the implementation of epitaxial base structures has already demonstrated F_Ts higher than 70 GHz, the complexity of such a module is a systematic drawback as SiGe heterojunction bipolar transistors (HBTs) can offer much higher performance with moderately additional process efforts.

2.1.3 Trench isolation

The collector to substrate capacitance C_{js} consists of the components N+ buried layer area to the low doped substrate and the much larger contribution from N+/P buried layer sidewall capacitance (see figure 2). The perimeter part is becoming more important with shrinking device geometries as the ratio of perimeter/area is increasing. Therefore trench isolation is of growing importance in high performance processes. A 0.8μm oxide/poly filled trench can decrease the perimeter capacitance down to 20 - 25 % compared to a non-trenched version. In addition the spacing of bipolar transistors can be shrinked more aggressively.

Although the trench isolation module involves from a designers point-of-view only the drawing of one more mask layer, in wafer manufacturing it stands for much more complexity. The trench formation requires a hard mask oxide, the trench mask, the etching of the oxide hard mask and the trench grooves, removal of the oxide, oxide or oxide/poly filling and planarization by plasma etching or CMP. Looking at this list of process steps it is obvious, why this module is often offered only as an optional module for BiCMOS process generations down to 0.8 - 0.5 μm.

Further reduction of Cjs can be achieved by the use of SOI, but this combination will in the next years still stay a niche market for certain applications unless the price of SOI base material will drop much more in the future /4/.

2.2 Si/SiGe HBTs

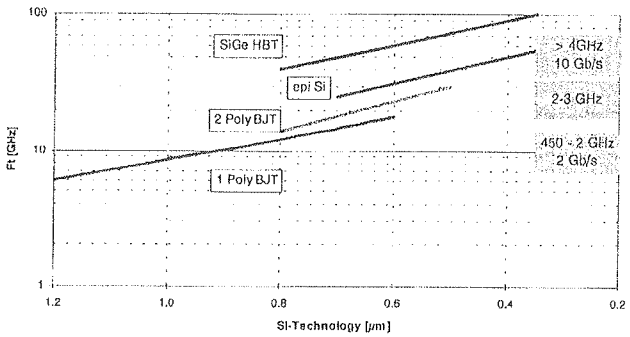

Fig. 3: Comparison of peak Ft performance of Si and SiGe bipolar transistor integrated in BiCMOS processes and their application ranges

As discussed above the restrictions of vertical scaling of emitter and base restrict Si BJTs in their practical cost-effective integration. Upper limits for Ft of 25 - 35 GHz are achieved, if processes which are available for a broader range of ASIC applications are considered.

Heterojunction bipolar transistors HBTs in silicon technology using SiGe base have emerged as a promising technology in the last decade investigated by several groups worldwide /6-10/. In contrary to a conventional silicon BJT, the epitaxial SiGe base HBT offers the possibility of decoupling current gain and low base resistance by independent adjustment of emitter and base doping. Although already very good frequency performances with F_T and f_{max} above 100 GHz have been achieved, the disadvantages of the HBT structure have so far delayed the integration in commercial HBT-BiCMOS processes. These limitations are caused by the mechanical stress in the pseudomorphic SiGe base

Table 1: Process flow examples of a BiCMOS and a post-CMOS HBT integration into a CMOS process

CMOS (1 P/2 M base process)	BiCMOS	HBT-CMOS	optional modules
	N+/P+ buried layer Epi Si deposition		
			Trench isolation
Twin well formation Active area definition LOCOS isolation MOS transistor implants Gate oxide / poly / etch N- /P- LDD Spacer formation	Twin well formation Active area definition LOCOS isolation Collector contact implant MOS transistor implants Gate oxide / poly / etch N- /P- LDD Spacer formation Bipolar base implant	Twin well formation Active area definition LOCOS isolation MOS transistor implants Gate oxide / poly / etch N- /P- LDD Spacer formation	
			Poly/poly capacitor
	Emitter opening Poly 2 deposition		
			High resistive implant
N+/P+ source/drain	Poly 2 mask/etch N+/P+ source/drain	N+/P+ source/drain CMOS protection HBT area opening Collector implant / anneal Si/SiGe- epi deposition Emitter opening Emitter poly2 / etch P+ Base implant Mesa mask/etch Collector contact implant Spacer formation Salucidation	
ILD deposition Contact maxk/etch TiN / W-plugs Metal 1 definition IMD 1/Planarization Via 1 mask/etch TiN / W plugs Metal 2 definition	ILD deposition Contact mask/etch TiN / W-plugs Metal 1 definition IMD 1/Planarization Via 1 mask/etch TiN / W plugs Metal 2 definition	ILD deposition Contact mask/etch TiN / W-plugs Metal 1 definition IMD 1/Planarization Via 1 mask/etch TiN / W plugs Metal 2 definition	
			IMD 2/ Planarization Via 2 mask/etch TiN / W plugs Metal 3definition
Passivation Pad mask/etch	Passivation Pad mask/etch	Passivation Pad mask/etch	

increasing with Ge content and SiGe layer thickness. This restricts the vertical Ge profile and the thermal budget must be kept low to avoid the relaxation and the Boron out-diffusion of the SiGe base. Despite the development work already performed and the fact that the epitaxial SiGe formation is already showing production worth repeatability /11/ is the availability as a commercial offered technology (e.g. for ASIC applications) still at its beginning. A practical hindrance with respect to industrial production seems also to be the additional effort for control of layer doping and gradient, as SIMS and X-ray analysis methods are not installed as frequent measurement tools in semiconductor production fabs today. However, with the repeated demonstration of better maturity of the deposition processes the control measurements could be reduced to reasonable efforts.

2.2.1 Epitaxial SiGe fabrication methods

From an industrial point-of-view out of the various methods applied to form the epitaxial SiGe (MBE, UHV-CVD and LPCVD) only the later two offer reasonable cost and throughput figures for implementation in a semiconductor fab. The type of epitaxial deposition (blanket, differ-

ential, selective) are more or less determining the yield and control issues associated with the procedure of integration into a CMOS process.

As the epitaxial SiGe base layer is grown on the collector tub in the silicon substrate any defect generated by the CMOS processing steps can potentially limit the yield by emitter pipe formation. This would suggest to implement the HBT part as early as possible into the CMOS process. However, as any out-diffusion of Boron or relaxation would deteriorate the HBT performance the subsequent processing steps are limited by a relatively low thermal budget /12/.

Another approach is a post CMOS implementation starting with the HBT part after the CMOS device formation. Such an approach will however only be successful, if the MOS LDD structures are capable of facing additional RTP-like steps. Practical employment seems therefore today limited to processes which are on one hand already based on RTP activation (typically in the submicron regime) and are not too sensitive to additional thermal treatment as observed beyond 0.5μm. Table 1 shows such an example of HBT integration into a CMOS process.

2.2.2 SiGe HBT performance considerations

The vertical doping profile of the bipolar transistor is dominating the high frequency performance both for a SiGe HBT as it is for a Si BJT. Purely by the incorporation of Ge into the base improvements in Ft from 30 to 49 GHz of bipolar transistors have been demonstrated /7/.

Major key figures of merit for the analogue and low power transistor performance can be improved in the SiGe HBT. The increased base doping allows a lower base resistance R_b to be obtained in SiGe than in Si for the same current gain β. Si/SiGe HBTs exhibit transition frequencies f_T and maximum oscillation frequencies f_{max} which are bout twice as large as in Si BJTs in combination with Early Voltages 5-6 times larger.

Device performance has been evaluated by a comparative simulation of representative BiCMOS applications in a 12 GHz 0.8μm BiCMOS process /2/ and a 45 GHz HBT process as available from IHP, Frankfurt/Oder /11/.

A VCO (voltage controlled oscillator) device for high output frequencies at low currents can typically realize up to 2.5 - 3.0 GHz at a current consumption of 5- 8 mA in the Si BJT process. If in this circuit HBTs replace the Si BJTs the device can either achieve frequencies up to 7.5 GHz for the same current levels or the current consumption can be reduced by 70 to 80% at 2.5 GHz.

On the other hand for applications like LNA (low noise amplifier) or mixers the parasitic transistor elements like base resistance and junction capacitances play a dominant role. In these cases the investigated SiGe HBT technology could not demonstrate dramatic performance improvement for the given set of SPICE parameters /13/. However, there are more technological opportunities to increase the base doping and therefore to reduce the base resistance in a SiGe HBT technology compared with Si BJT processes.

2.2.3 SiGe HBT integration

In a co-operation work with the Institute for Semiconductor Physics IHP Frankfurt/Oder and Austria Mikro Systeme International AG a SiGe HBT process has been demonstrated the first time to be capable of fabricating high performance SiGe HBTs after the completion of standard CMOS devices /11/.

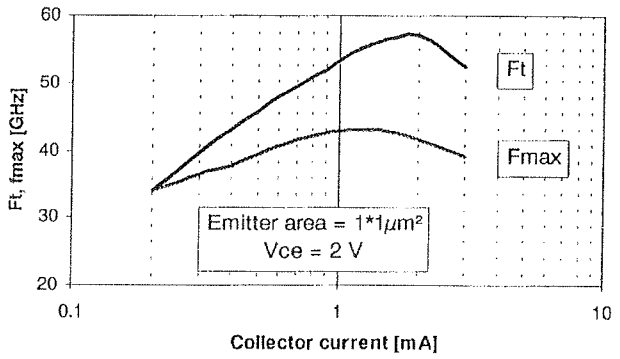

Fig. 4: HBT cut-off frequency ft and maximum oscillation frequency fmax vs. collector current

These post-CMOS integrated HBTs with 0.8μm design rules achieved f_T(f_{max}) values of up to 57(43) GHz (figure 4) without deteriorating the CMOS device parameters. Based on a 0.8μm ASIC-CMOS platform the MOSFET fabrication has been completed up to source and drain formation, and the wafers have been sealed with LTO-LPCVD oxide (table 1). The gate stack layers present on the areas reserved for the HBTs have been removed and a retrograde Phosphorus collector has been prepared in the normal CMOS well by implantation and appropriate annealing. A highly Boron doped SiGe base and a lightly doped Si emitter is then deposited by a single epitaxial RT-LPCVD step. The HBT base-collector mesa formation is continued by structuring, implantation and anneal for poly emitter and extrinsic base contact implants. Appropriate design of the base Ge profile and doping, and control of transient enhanced Boron diffusion due to the extrinsic base contact implant are of special importance to achieve the desired parameters /14/.

The emitter-pipe yield has been determined by leakage measurements of large emitter size macro HBTs with an emitter area of 10^4 μm^2 and has achieved average yields of greater than 80%.

This post-CMOS approach promises an relatively easy to implement HBT structure realizing performance figures typically achieved by special bipolar or BiCMOS processes with much more aggressive design rules.

2.3 Wafer processing costs

When balancing all technical advantages of new BiCMOS developments and their wafer processing complexity, the cost of additional manufacturing steps can also be an essential limitation, whether certain process versions can find their successful market seg-

ment. In the following a short investigation of costs correlated with process modules is given. However, it must be noted, that these calculations take only into account pure wafer processing costs consisting of operator costs, equipment costs determined by throughput and depreciation, facility utilization and material consumption. They do not contain yield issues, especially where new and advanced modules are investigated and yield models are not yet available due to lack of production data. Despite these restrictions, the figures for new process modules have been based on equivalent steps already available and thus represent realistic data gathered in an ASIC-manufacturing environment. Additionally it should be noted, that this data does not include electrical wafer test costs, as in advanced RF-analogue/digital wafer testing the testing costs can vary widely depending on the different application areas.

Table 2: Comparison of wafer processing costs for a 0.6μm CMOS process and implementation of bipolar process modules

0.6 μm CMOS 1P/2M	wafer processing cost
CMOS front end	52%
CMOS back end	48%
3. metal layer	+24%
18-20 GHz 2M BiCMOS (salicided)	+35%
add trench isolation to 2M BiCMOS	+17%
add 45 GHz HBT to 2M CMOS	+50%

Table 2 compares the costs related with the implementation of additional bipolar process modules into a 0.6μm CMOS process. Despite the use of advanced Al metal interconnect together with W-plugs and TiN layers, the basic CMOS front end costs account for 52% of the total wafer cost in manufacturing. Frontend of the process contains here all processing steps before the first inter level dielectric layer (e.g. BPSG). It is also interesting to see, that the cost for a trench isolation module is nearly in the range of an additional metal layer.

Due to a good merging of BiCMOS processing steps with the basic CMOS process the costs of a 18-20 GHz Si-BJT with salicided base and emitter and additional double poly capacitors (C= 1.8 fF/μm^2) can be kept at a level of +35%. Such a process allows applications of up to 2.5-3 GHz at a reasonable wafer price. However, the design margin might be narrow with respect to current consumption for certain low power applications in this frequency range (e.g. mobile telecom).

If the post-CMOS implementation of a HBT-module is considered (see table 1), the costs summarize up to additional +50% to the basic CMOS process. For the epitaxial SiGe step in this case the usage of a RT-LPCVD step has been assumed with a cost factor of 2.5x compared with standard Si-epi on a similar tool. For comparison, UHV-CVD tools promise already processing costs in the range of standard Si-epi-deposition.

Additionally it should be taken into account that the HBT integration realized here does not yet benefit from potential merging of deposition, etching or implant steps. We therefore strongly believe, that in the next future further optimization work can bring the additional cost for a HBT integration closer to the level of advanced Si BJTs, but will offer interesting opportunities for more advanced applications.

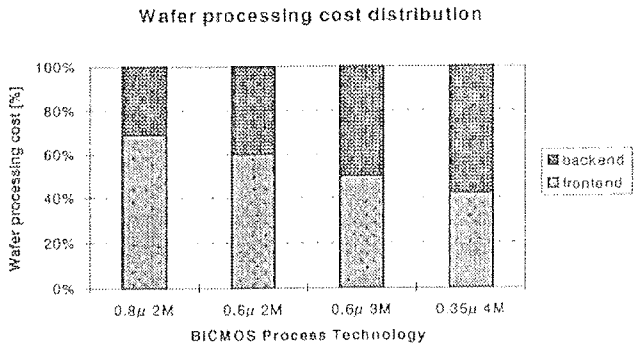

Fig. 5: Comparison of wafer cost distribution for front-end and backend processing of Si BJT BiCMOS processes for different technology generations

Figure 5 is comparing the partition of frontend and backend wafer processing costs. It is very obvious, that with the increasing complexity of the interconnect metal layers (e.g. TiN ARC layer, W-plugs, planarization) the cost of the backend in submicron processes is becoming the dominating factor. The data also indicates, that much higher complexity in the frontend process can be justified for future BiCMOS process generations without increasing the overall wafer cost uneconomically.

3. Conclusions

An overview of the common bipolar transistor architectures applied in submicron BiCMOS processes has been given with emphasis put on the correlated complexity of process integration for ASIC manufacturing.

A cost breakdown for BiCMOS modules has been presented and it has been illustrated that the additional costs incorporated with the integration of advanced frontend modules will become less important in future process technologies with smaller geometries due to the increasing costs associated with the growing number of interconnect layers.

The continuing research on Si and SiGe device and material physics and the availability of more advanced fabrication equipment have pushed the application of Si/SiGe based technology far in the regions, which were before considered of being only domains of III-V semi-

conductors. The superior device advantages of SiGe HBTs and the improvements in epitaxial processing towards production orientation will make the availability of HBT-CMOS more feasible in the near future.

Acknowledgments

I want to thank my colleagues from the R&D and design departments for the fruitful discussions on BiCMOS requirements and integration issues. Special thanks also to Dietmar Temmler and his staff at IHP for the very interesting and productive collaborative work.

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SCANNING PROBE MICROSCOPY AND SPECTROSCOPY: FROM BASIC RESEARCH TO INDUSTRIAL APPLICATIONS

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Keywords: semiconductors, semiconductor devices, semiconductor storage devices, UHDS devices, Ultra High Density Storage devices, SPM, Scanning Probe Microscopy, IC, Integrated Circuits, defect analysis, process characterization, process monitoring, creation of nanostructures, STM, Scanning Tunnelling Microscopy, SFM, Scanning Force Microscopes, nanolithography, SCM, Scanning Capacitance Microscopes, NOS heterostructures, Nitride-Oxide-Silican heterostructures, FWHM, Full Width at Half Maximum, ROD, Rotating Disk device, EFM, Electrostatic Force Microscopes, MFM, Magnetic Force Microscopes, SThM, Scanning Thermal Microscopes, SNOM, Scanning Near-field Optical Microscopes, LDD, Lightly-Doped Drain

Abstract: An overview of industrial applications of scanning probe microscopy (SPM) is given. The first part describes possible applications for the fabrication of semiconductor devices by SPM-methods and the use of SPM-based techniques for an ultra high density storage (UHDS) device. The second part shows the ability of SPMs as a characterization tool for integrated circuits (ICs). They can be used in defect analysis, process characterization, and monitoring. And they offer the measurement of each significant value with a spatial dimension of less than 100 nm. So the SPM is useful for a fab today, and irreplaceable for a fab in the future.

Vrstična mikroskopija in spektroskopija s sondo: Od osnovnih raziskav do uporabe v industriji

Ključne besede: polprevodniki, naprave polprevodniške, pomnilniki polprevodniški, UHDS naprave pomnilniške gostote ultravisoke, SPM mikroskopija s sondo vrstično, IC vezja integrirana, analiza hib, karakterizacija procesov, nadzor procesov, ustvarjanje nanostruktur, STM mikroskopija vrstična tunelna, SFM mikroskopi s silo vrstično, nanolitografija, SCM mikroskopi vrstični kapacitivni, NOS heterostrukture nitrid-oksid silicij, FWHM širina polna pri maksimumu polovičnem, ROD naprava z vrtečim se diskom, EFM mikroskopi s silo elektrostatično, MFM mikroskopi s silo magnetno, SThM mikroskopi vrstični terimični, SNOM mikroskopi vrstični optični s poljem bližnjim, LDD ponor dopiran rahlo

Povzetek: V prispevku podajamo pregled uporabe vrstične mikroskopije s sondo (SPM) v industriji.V prvem delu opisujemo možnosti uporabe SPM metod pri izdelavi polprevodniških elementov, kakor tudi uporabo SPM tehnik za izdelavo spominskih elementov z zelo visoko gostoto (UHDS) zapisa informacije.

V drugem delu prikažemo zmožnosti metod SPM kot orodja za vrednotenje integriranih vezij. Lahko jih uporabimo pri analizi napak ter vrednotenju in nadzoru procesov. Metode omogočajo meritve različnih parametrov s prostorsko ločljivostjo, boljšo od 100 nm. Danes je SPM zelo koristna metoda v proizvodnji integriranih vezij, v bodočnosti pa bo postala nenadomestljiva in nujno potrebna.

1. Introduction

Fifteen years after the invention of the scanning tunneling microscope (STM) /1/, scanning probe microscopy (SPM) /2/ is going to be a standard tool for industrial application. Two possible fields are visible today, first the field of fabrication of nanostructures, and second the field of analysis of nanostructures. Both fields are determined due to future development of structures of less than 0.3 μm. Not later than 2005, there must be inventions for the fabrication and analysis of structures with spatial dimensions of less than 100 nm.

SPM offers an interesting combination of high spatial resolution, high sensitivity, and applicability under ambient conditions. Selected examples of applications of SPMs are presented, including fabrication of nanostructures for semiconductor devices and for UHDS devices, as well as SPM-based characterization tools for ICs.

2. Applications of Scanning Probe Microscopy

All different types of SPMs are based on the same principle: a small probe is brought in close proximity to a surface, so that the near-field interaction can be measured. A feedback system keeps the interaction strength constant during the scan.

2.1 Applications of SPM for the creation of nanostructures

By SPM it is possible to create structures with spatial dimensions of less than 100 nm, due to an increase of the interaction between probe and sample. This ability can be used for the fabrication of semiconductor devices, as well as for basic technology for a future UHDS device.

2.1.1 Semiconductor devices

Atomic manipulation has been shown with a STM /3/, but this required a great technical effort (UHV, 4°K). Nanolithography has been demonstrated with a scanning force microscope (SFM) /4/ for integrated fabrication of semiconductor devices /5/ and of quantum electronic devices /6/. This manipulation has been done at ambient conditions.

A conducting SFM tip was used to write nanometer scale oxide patterns on a Si(100) surface and on amorphous silicon. These patterns can be used as masks for selective etching of the silicon, and enable the fabrication of a 0.1 μm metal-oxide semiconductor field-effect transistor (MOSFET) /5/. Based on anodic oxidation of thin Al films with an SFM, the fabrication of atomic point contacts has been shown /7/.

Furthermore, the SFM can be used to generate patterns on a photoresist. Wendel et al. /6/ generated hole arrays with a periodicity down to 35 nm and a hole diameter of only a few nanometer. Mechanical surface modification techniques have been applied to hard materials too, like superconducting ceramic, using a SFM with a diamond probe tip /8/.

All these nanolithography techniques work very well, but relatively slow. A commercial SFM works with scan velocities on the order of a few μm/s. To overcome this great disadvantage, Minne et al. /9/ have developed a cantilever with integrated piezoelectric actuator. With this cantilever, they have reached tip velocities in feedback operation of up to 1 cm/s, that leads to more than 20 frames (50 μm x 50 μm) per minute. Furthermore, they developed an array of 2 x 1 individually controlled cantilevers. Binnig et al./10/ presented the development of an array of 5 x 5 cantilevers. Future development will give us arrays of even 100 x 100 cantilevers, so we will be able to scan and manipulate a field of more than 2 cm x 2 cm per minute. From then on, we can use SPM technology for industrial fabrication of semiconductor devices of the 0.1 μm generation.

2.1.2 Ultra High Density Storage Devices

Another interesting field of application for SPM-based technologies are UHDS devices. Up to date hard disks reach data densities of less than 2 Gbits/in^2, and the border line for conventional storage technology is on the order of several tens of Gbits/in^2 because of limitations regarding superparamagnetics in magnetic recording and optical diffraction in optical recording. But nevertheless, there is an increasing demand for higher data capacities. So there must be research in unconventional developments for new storage devices. With a STM, one can manipulate single atoms and reach a data density of 10^6 Gbits/in^2. The disadvantages are the great technical effort and the slow scan speed and data transfer rate respectively. To use other types of SPMs seems to be a better approach.

Kino et al. /11/ developed a solid immersion lens scanning near-field optical microscope (SIL-SNOM). With this technique Terris et al. /12/ achieved a data density of 2.5 Gbits/in^2 and a data rate of 3.3 Mbits/s.

Recently, Martin et al. /13/ presented a scanning interferometric apertureless microscope (SIAM), where a resolution of 50 nm was achieved with visible light. This corresponds to a potential density of 256 Gbits/in^2. A theoretical calculation gives a possible data rate in the tens of MHz range. The scanned sample was an SiO_2-Si disk with smallest pits of 50 nm x 50 nm across, and 25 nm deep, fabricated by electron (e) -beam lithography and reactive ion etching.

Another read-only-memory (ROM) device with a data density of more than 50 Gbits/in^2 has been demon-

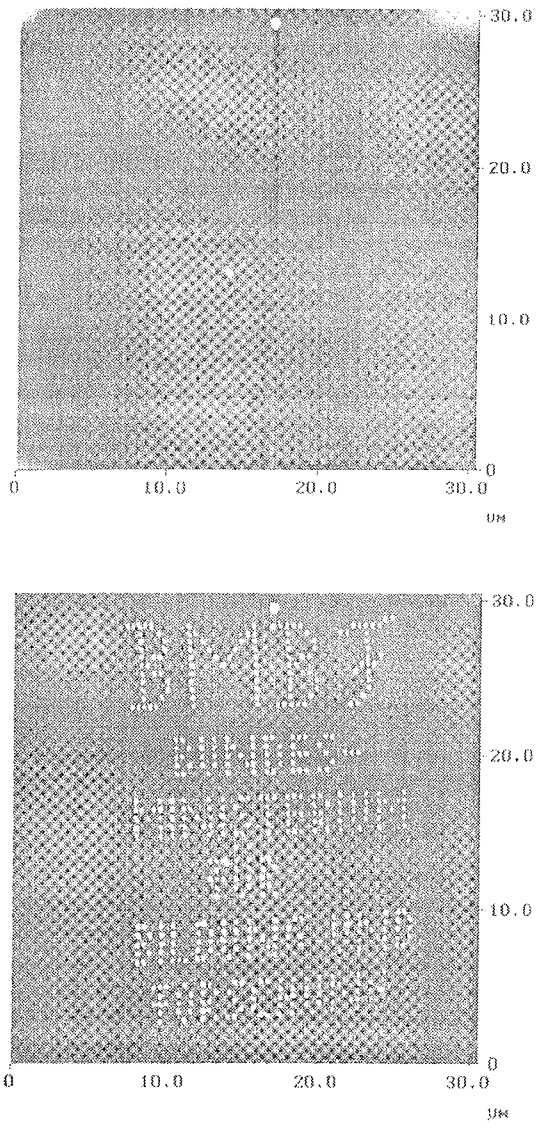

Fig. 1: Topography and capacitance image of a NOS heterostructure with stored charge dots.

strated by Terris et al. /14/. They used a polycarbonate disk with smallest pits of 100 nm, and an SFM for read out. The disk was manufactured from an e-beam generated master pattern. This technology enables mass production of samples with pits of less than 50 nm /15/. The used SFM works in contact mode with special high-frequency piezoresistive cantilevers with resonance frequencies of up to 10 MHz. Furthermore, Terris et al. have developed a SFM-based system with a rotating sample. A new autotracking system could maintain the tip on a particular data track. So they get a data density of 65 Gbits/in^2 and a data rate of more than 1 Gbits/s.

A possible random access memory (RAM) UHDS device is based on a scanning capacitance microscope (SCM) and on charge storages in a nitride-oxide-silicon (NOS) heterostructure (Fig. 1). A voltage pulse of typically 40 V and 10 μs allows the charging of the nitride-oxide interface, and a voltage pulse of the opposite direction can discharge this interface.

The smallest structure written in our laboratory had a full width at half maximum (FWHM) of 160 nm. The maximum data density reached is more than 30 times higher than in today's commercial storage memories. The theoretical data density limit determined by the overlap of the depletion areas is more than a hundred times higher. To reach high data rates, a SCM-based prototype (rotating disk (ROD) -device) has been developed that rotates the sample (Fig. 2).

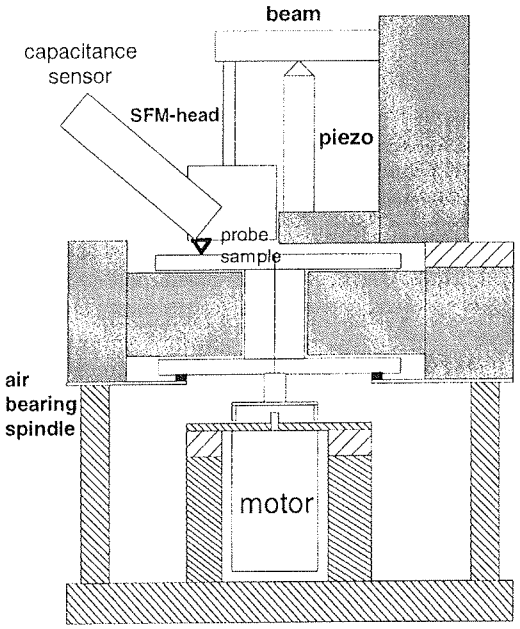

Fig. 2: Schematic of the ROD-device.

The SCM head can be moved by a high-power piezoelectric element in z-direction, so that the cantilever is pressing on the surface with a force as small as possible. First tests gave us data rates of more than 100 kHz, with a signal to noise ratio of 60 dB. The great problem of this storage technology is the contact between the metallic tip of the cantilever and the very hard silicon-nitride surface. At relative velocities of some meter per second, the tip gets rubbed off and the resolution of the system and its data density decrease as a function of time. This wear problem can be expected to be diminished by development of new coating technologies or non-contact measurements.

All these approaches show the possibility to use SPM-based techniques for a future UHDS device.

To summarize: SPM offers a great potential for the creation of nanostructures, and can be used for the fabrication of 0.1 μm semiconductor devices and for UHDS devices.

2.2 Application of SPM for the analysis of nanostructures

SPMs are predestined for the characterization of ICs, due to their two-dimensional (2-d) imaging capabilities, high spatial resolution, and nondestructive nature. There is a great need for nanometer-scale measurements in the semiconductor industry. The family of SPMs offers the detection of each significant value (Fig. 3).

Interaction	Microscope	Abbreviate
Electric field	Electrostatic force microscope	EFM
Magnetic field	Magnetic force microscope	MFM
Heat	Scanning thermal microscope	SThM
Light	Scanning near-field optical microscope	SNOM
Capacitance (doping profile)	Scanning capacitance microscope	SCM

Fig. 3: Overview of SPM types for the characterization of ICs.

A SFM can be used for cross section inspection and metrology /16/. The measurement error introduced by the finite size of the cantilever tip can be calculated due to computer models. Therefore, the SFM image gives us the exact values compared with a scanning electron microscope (SEM) measurement, but without the effort of specially prepared samples.

An electrostatic force microscope (EFM) enables the measurement of an electric field and therefore a voltage on an IC, with spatial dimension of less than 100 nm. Furthermore, special techniques (heterodyne mixing) enable the measurement of voltages with frequencies of some tens of GHz /17/.

The magnetic stray field of a conductor track can be measured by a magnetic force microscope (MFM). A calculation gives us the current of the conductor. In addition, the MFM has been used for the measurement of the stray field of write-read heads of hard disks.

The scanning thermal microscope (SThM) allows us the detection of hot spots on an IC with 100 nm resolution /18/.

A very interesting analytical device is the scanning capacitance microscope /19/. The SCM offers the detection of 2-d doping profiles with lateral resolution of less than 100 nm and dopant concentrations of 10^{15} to 10^{20} cm^{-3}. The „National Technology Roadmap for Semiconductors" describes this measurement as decisive technology for the next generation of ICs. The SCM permits determination of the effective channel length and the lightly-doped drain (LDD). Exact data are very important for the optimization and calibration of technology computer aided design (TCAD) systems, and new designs of MOS-FETs and Bipolar-transistors require an exact knowledge of the 2-d doping profiles (Fig. 4).

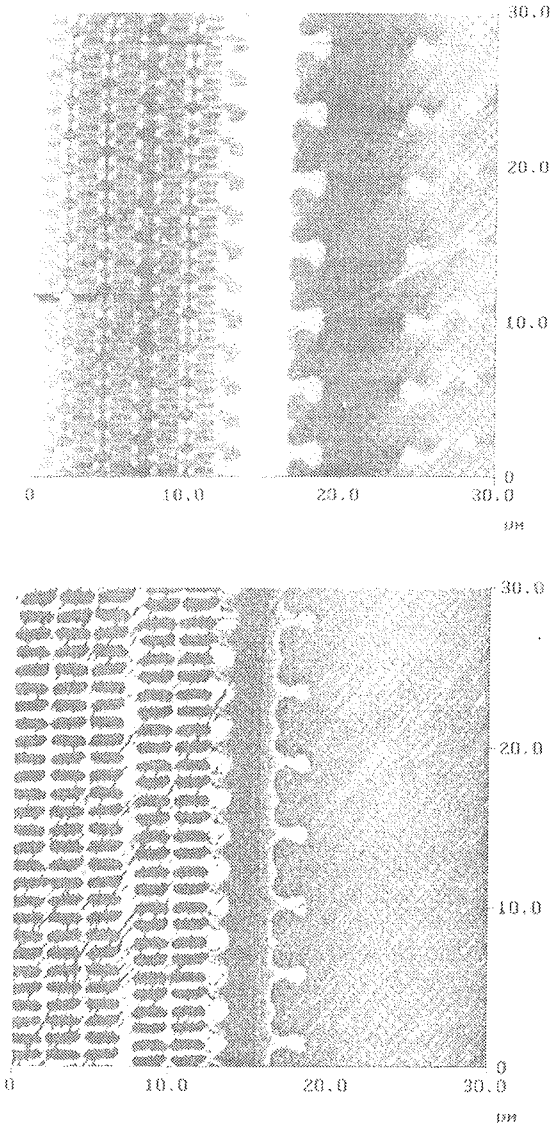

Fig. 4: Topography (upper) and capacitance image of a DRAM.

For spatially resolved SCM measurements complete C(V)-V-curves were not taken, but the capacitance was measured at a constant bias voltage. The result is a capacitance image of the sample. The problem of inversion - determination of the dopant concentration from measured capacitance images - is not solved yet, since too many factors are unknown.

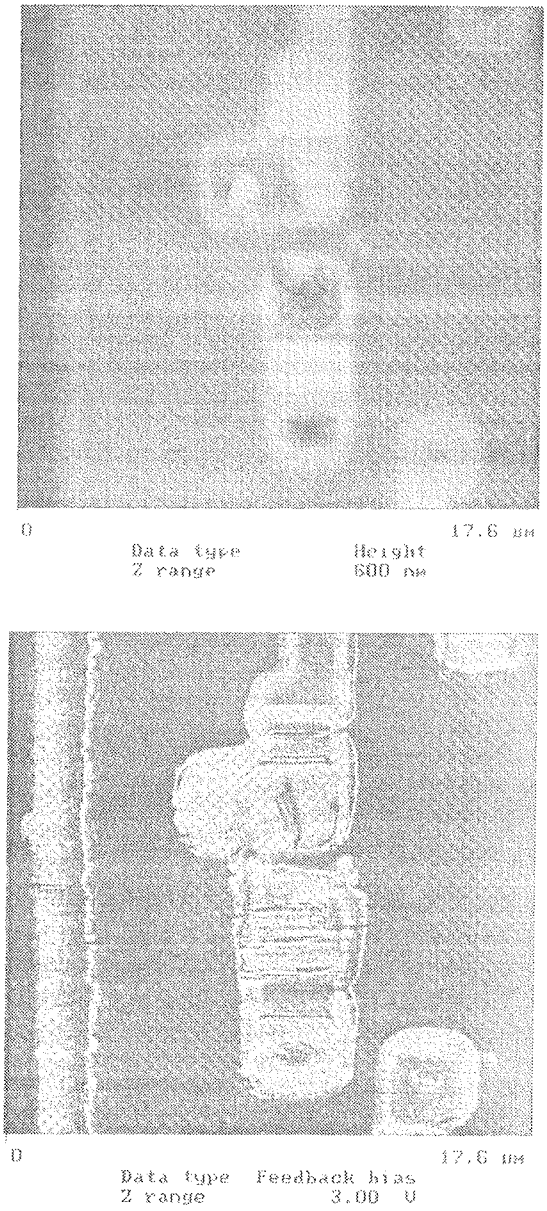

Fig. 5: Topography (upper) and capacitance image of an electrostatic discharge.

These unknown facts are, e. g., the influence of the shape of the probe, the thickness, and the dielectric constant of the oxide. Nevertheless, capacitance images of manufacturing IC-structures have a great potential for use in defect analysis, process characterization and monitoring. Fig. 5 shows the topography and the capacitance image of a sample with an electrostatic discharge. This is the main reason for ICs being destroyed, and often invisible in SEM. On the other hand, the SCM gives us an exact image of the topography and the expected flow of dopant atoms. So SCM is already

in use in industry and research institutions for process development and failure analysis.

3. Conclusion

SPM offers a great potential for the creation and analysis of structures with spatial dimensions of less than 100 nm. SPM can be used for fabrication of future masks and the fabrication of semiconductor devices, as well as basic technology for UHDS devices. Furthermore, SPM can be used as a characterization tool for the semiconductor industry.

To summarize: SPM is going from lab to fab.

4. Acknowledgments

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SiGe-HETEROJUNCTION BIPOLAR TRANSISTORS: KEY TECHNOLOGIES AND APPLICATIONS IN COMMUNICATION SYSTEMS

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Keywords: semiconductors, semiconductor devices, SiGe HBT, Silicon-Germanium Heterojunction Bipolar Transistors, key technologies, practical applications, communication systems, IC, Integrated Circuits, high frequencies f_{max}=160 GHz, noise figure <0.5 dB (at f=2GHz), electrical resistors, electrical inductors, spiral electrical inductors, electrical capacitors, MMIC, Monolithic Microwave Intergrated Circuits

Abstract: The SiGe HBT is attractive for future broadband and wireless communication ICs owing to its outstanding performance and from the fabrication point of view (fabrication costs ≈ 0.25 x GaAs and 1.3 x Si). Most processes of main-stream Si technology can be utilized for integration of the HBT on Si substrates. This is due to the similar chemical and physical behaviors of Si and SiGe with respect to reactive ion etching, low ohmic contact systems, isolation and passivation. Thus, several groups have integrated the SiGe-HBT in standard Bipolar and BiCMOS technologies using differential or selective Si/SiGe/Si-epitaxy. Others use blanket epitaxy of the Si/SiGe/Si layers to benefit from an easy technology to eliminate influences of the isolation oxide on the growth and doping, and to allow an easy characterization of the material including the doping profile with global physical diagnostic methods. In addition, there is a simple and low cost fabrication technology using blanket epitaxy and double mesa integration, which has led to several records of SiGe-HBTs in high-frequency (f_T=116 GHz, f_{max}=160 GHz) and noise data (F_{min} (at 2 GHz)<0.5 dB, F_{min} (at 10 GHz) <1 dB, F_C ≈ 100 - 2000 Hz).

SiGe heterospojni bipolarni tranzistorji: Ključne tehnologije in uporaba v komunikacijskih sistemih

Ključne besede: polprevodniki, naprave polprevodniške, Si-Ge HBT transistorji bipolarni heterospojni, tehnologije ključne, aplikacije praktične, sistemi komunikacijski, IC vezja integrirana, frekvence visoke f_{max} = 160 GHz, število šumno <0,5 dB (pri f = 2 GHz), upori električni, induktorji električni, induktorji električni spiralni, kondenzatorji električni, MMIC vezja integrirana monolitska mikrovalovna

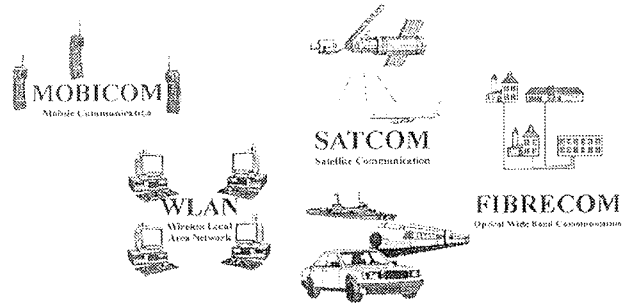
Povzetek: SiGe heterospojni bipolarni tranzistor (SiGe HBT) je privlačen element za bodoča integrirana vezja za brezžične in širokopasovne komunikacije predvsem zaradi izrednih lastnosti in kompatibilnosti z obstoječo proizvodnjo (cena izdelave ≈ 0.25 GaAs in 1.3 Si). Večino korakov glavne Si tehnologije lahko uporabimo za integracijo HBT na silicijeve substrate. To je možno predvsem zaradi podobnega kemičnega in fizikalnega obnašanja Si in SiGe glede na reaktivna ionska jedkanja, nizkoomske kontaktne sisteme ter glede na tehnike izolacije in pasivacije. Tako je že večim skupinam uspelo integrirati SiGe HBT v standardne bipolarne in BiCMOS tehnologije z uporabo diferencijalne ali selektivne Si/SiGe/Si epitaksije. Drugi zopet uporabljajo slepi nanos Si/SiGe/Si plasti, kar je enostavnejše, saj se ognemo vplivom izolacijskega oksida na rast in dopiranje in nam to hkrati omogoča lažje vrednotenje nanešenih plasti, vključujoč meritev koncentracijskega profila z globalnimi fizikalnimi diagnostičnimi metodami. Nadalje, obstaja dokaj enostavna in poceni tehnologija, ki uporablja slepi nanos epi plasti in dvojno mesa strukturo, s pomočjo katere je bilo do sedaj izdelano več visokofrekvenčnih SiGe HBT tranzistorjev (f_T = 116 GHz, f_{max} = 160 GHz) z ustreznimi šumnimi lastnostmi (F_{min} (pri 2 GHz) < 0.5 dB, F_{min} (pri 10 GHz) <1 dB, F_C ≈ 100 - 2000 Hz).

1. Introduction

For the steadily increasing communication market the acceptance of new communication services depends on the costs of the terminals. Low cost and high performance chip sets are needed. SiGe heterojunction bipolar transistors (SiGe-HBTs) meet these requirements since a few years. SiGe/Si offers high speed, low noise, high power, low power consumption and cost effective production in existing Si-lines. Consequently SiGe heterodevices are for the high volume market and should be produced by large chip manufacturers. Indeed, companies like IBM, Siemens, NEC, Philips and Temic (a company of Daimler-Benz) are active in SiGe. It was the early pioneering activities and results of IBM and AEG Telefunken (later belonging to Daimler-Benz) that have stirred up the interest of others. From year to year the SiGe community becomes larger.

The high volume market for these SiGe hetero-chips can be divided into four segments represented by their operation frequency (Fig. 1). The mobile communication (1-2 GHz), wireless local area network (2.4-5.8 GHz), satellite communication (10.7-14.5 GHz) and the wide-band communication via cable or optical fibre (3-40 Gbit/s) are united to communication networks offering numerous services such like private/business contacts, entertainment music/video, telecommuting,

telemedicine, distance learning, fabrication robot check, workforce training, Internet, interactive/multmedia video, disaster management, mailbox/messaging, interactive home banking/shopping, goverment services, wireless scientific backdone collaborative groupwork, etc.



MOBICOM	WLAN	SATCOM	FIBRECOM
1-2 GHz	2.4-5.8 GHz	10.7-14.5 GHz	3-40 Gbit/s

Fig.1: Scenario: SiGe-HBTs for communication markets.

1.1 SiGe-HBT integration into the Si standard technology

Since the discovering of the bipolar transistor by W. Shockley, J. Bardeen und W. Brattain in the year 1947 the technological evolution mainly concerned the following topics: the implantation and the base epitaxy improved the internal transistor, whereas the trench isolation reduced the parasitic collector-substrate-capacitance and increased the package density /1-3/. The novel double polysilicon technology was an innovative technique to optimize the lateral and vertical transistor. The emitter efficiency increased and the self-aligment of the emitter to the base contacts reduced the emitter-base and base-collector-capacitance. The lateral scaling of the bipolar transistor was supported by the shrinking of the minimum feature size driven by the mainstream technologies (DRAMs, CMOS-logic). The vertical optimization of the bipolar transistor was dominated by the reduction of the base width, because the transit time is one of the most important factors determining the speed of bipolar circuits and is in first-order calculation proportional to the square of the base width /6/.

When reducing the base width in bipolar transistors there are some physical constraints to be considered. Since punchthrough between emitter and collector must be avoided, a reduction of the base width must be accompanied by a corresponding increase in maximum base doping concentration N_A. However, a limit is set by trap-assisted forward tunnelling in the emitter-base-junction, which leads to strongly nonideal behaviour of the base current at large values of N_A, a reduction of the current gain, and an increase of the emitter transit time and the emitter-base-capacitance.

These drawbacks of a conventional silicon homojunction bipolar transistor (BJT) can be overcome by the HBT with an epitaxial silicon-germanium alloy narrow-gap base region. It offers the possibility of decoupling a reasonable current gain and a low base resistance leading to an independent adjustment of emitter and base doping /4,5/. The current gain itself is much higher due to the B/E heterojunction, which allows an increased base doping and a thinner base to get the same current gain β compared with Si. Because of the thin base SiGe-HBTs exhibit a very low transit time τ_F. In addition the optimization of the lateral structure is a very important issue for improving device performance for low power and low noise applications. This is because lateral scaling means the reduction of parasitic components of the extrinsic transistor, which slow down the intrinsic transistor and dissipate power.

The first SiGe-HBT was realized in the year 1987 by S.S. Iyer /7/, when III/V-HBTs were standard devices at this time. The main difficulties were related to the growth of pseudomorphic SiGe-layers, because of the lattice mismatch of SiGe and Si /8/. The mechanical stress in the pseudomorphic SiGe base increases with the Ge content and the SiGe layer thickness. The Ge content is limited and the thermal budget has to be low to prevent the relaxation and the boron outdiffusion of the SiGe base. In early years simple double mesa transistor structures were used for electrical characterisation of the Si/SiGe/Si layers /7,9-12/. These structures allowed a fast and simple processing at low temperatures.

Basically the SiGe-HBT is a new version of the Si-BJT now having an optimized vertical structure. From the fabrication point of view, one major advantage of an HBT on a Si substrate is the utilization of most processes of mainstream Si technology for the integration. This is due to the fact that Si and Ge have similar chemical and physical behaviour with respect to reactive ion etching, low ohmic contact systems, isolation and passivation, the precondition for a seamless transfer of this novel device into standard Si-production lines /14,16,17,22, 25,52-54/.

Si/SiGe/Si-epitaxy

Different to Si-BJTs the Si/SiGe/Si-epitaxy is a new central process step, which must fullfil the following points in correlation with the integration concept: (1) Reproducible control of the n- and p-doping and gradients and the Ge content, (2) good homogeneity of these parameters and sufficient throughput, (3) high interface and crystal quality at a low contamination level (e.g. metals, C, O, B,..), (4) low temperature epitaxy (<800°C) to minimize the boron outdiffusion and the SiGe relaxation and (5) the possibility for blanket, differential and selective epitaxy. Solid source MBE /7,9-15/, gas source MBE /16/ or CVD in different process windows (UHVCVD /17,18/, APCVD /19/, RTCVD /20,21,53/, LPCVD /22,23,52,54/ or LRP /24/) are used for the definition of the vertical SiGe-HBT profile. Because of its high flexibility MBE is used in research, whereas CVD is used in the production lines due to its higher throughput.

There are three basic Si/SiGe-HBT fabrication concepts which differ in the position of the SiGe-base epitaxial growth within the process flow (see Fig.2). The epitaxial growth within the field oxide windows and polycrystalline layer outside is called differential epitaxy. Selective epitaxy is a monocrystalline deposition only in the field oxide windows. The blanket epitaxy (homogenious epitaxial Si/SiGe/Si growth on the whole Si substrate) seems to have some advantages: There is no influence of the isolation oxide on growth and doping, and the material parameters can be characterized with global physical diagnostic methods (SIMS, SNMS, x-ray, optical methods). The differential epitaxy (**A2**) is used by most production lines (e.g. IBM /17/, NTT /16/, DBAG/TEMIC /14/, Motorola /22/, AT&T (Lucent Technology) /53/). While NEC /25/, Siemens /52/, Philips /54/ and HP /23/ focus on the selective epitaxy (**A3**). The research centers prefer the SiGe blanket epitaxy (e.g. /10-12,15,20, 26-29/). The integration of the SiGe-HBT into a Si BiCMOS technology was shown by IBM /30/ (**A2**) and NEC /31/.

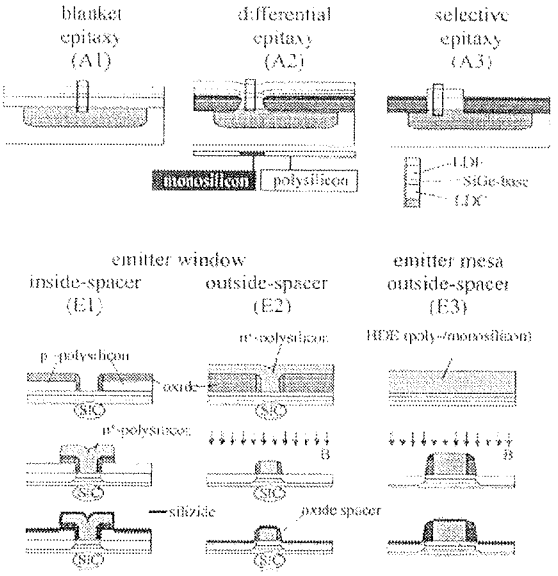


Fig.2: The different concepts for the integration of the Si/SiGe/Si-epitaxy and the emitter constructions.

Emitter definition

After the low-doped collector (LDC)/SiGe-base/low doped emitter (LDE) epitaxy, the emitter can be definied using inside- or outside-spacer- polysilicon technology (see **E1**, **E2** and **E3** in Fig. 2). The outside-spacer structure can be generated by a polysilicon deposition or monocrystalline high-doped emitter (HDE) epitaxy followed by a mesa etching (**E3**).On the other hand an oxide hole filled with polysilicon can be planarized (**E2**). For **E1** und **E2** the emitter width can even become smaller than the minimum feature size using an oxide inside-spacer. In addition the integration of the SIC (**S**elective **I**mplanted **C**ollector) can easily be realized by the self-aligned implantation through the emitter window. **E1** and **E2** dominate in the SiGe-IC technology (e.g. IBM /19/, NTT /16/, NEC /25/, Motorola /22/, DBAG/TEMIC /54/, AT&T (Lucent Technology) /53/, Siemens /52/, Philips /54/ and HP /23/).

Base contact

The three HBT versions A1-A3 have different contacts to the exstrinsic base (Fig. 3). In the differential SiGe-HBT **A2** the polycrystalline layer on the field oxide regions acts as a lateral base contact with the smallest contact resistance between the mono- and polycrystalline silicon. The selective SiGe-HBT **A3** utilizes the conventional double polysilicon technology with a negligible contact resistance between the monocrystalline extrinsic base and the deposited B-doped polysilicon. A further reduction of the external base resistance can be achieved either by an additional B implantation /17, 45/, a low ohmic salicide /53, 32/ or a selective deposited metal /16/.

For the blanket double mesa SiGe-HBT a significant reduction of parasitic resistances and capacitances can be achieved by using additional self-aligning processes like planarization for transistor contacts and outside-spacer-technology for micromasking /55, 56/. The size of the base-collector area depends strongly on the integration concept. For **A2** /14,16,17/ the area can be minimized owing to the sidewall contacted base. In **A1** and **A3** a defined parasitic base contact area remains /10,12,25,26,56/. Sophisticated concepts for self-aligned lateral base contact of Si-BJTs /50,51/ are not useable for the SiGe-HBT.

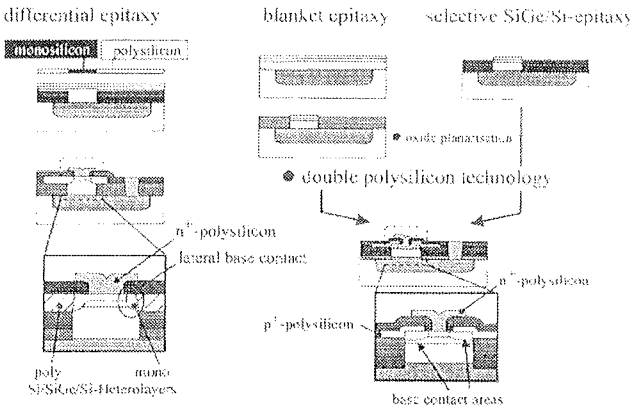


Fig.3: Optimization of the base contact and the parasitc base-collector-area in correlation with the integration of the SiGe epitaxy.

2. Experimental results

(a) SiGe-HBT

A non-passivated and non-implanted double mesa HBT can quickly be processed. The zero thermal budget processing prevents any outdiffusion of the boron doping profile and any SiGe layer relaxation. Therefore it is suited best to obtain optimum performance. The process flow for such a test transistor is shown in Fig. 4a. The 300nm thick PtAu metallisation defined in a lift off

process masks the wet chemical etching of the emitter in KOH solution, which stops at the SiGe base. The undercut of the emitter mask results in a self-aligned base metallisation also structured in a lift-off process. After the lift-off of the collector contact metal, air bridges are etched in an isotropic SF_6/O_2 plasma in order to reduce the parasitic elements. Using such a double mesa test transistor a high transit cutoff frequency f_T of 116 GHz /57/ has been obtained for a single emitter transistor. A multi emitter finger structure with an optimized vertical doping profile has increased the maximal oscillation frequency f_{max} up to 160 GHz /44/. Fig. 5 shows the remarkable improvement of the f_T and f_{max} values in the last years.

In order to integrate a SiGe-HBT, the device should be passivated and have all elements of a high integrability including contact implantation and self-aligned low ohmic contacts (see Fig. 4b). The process starts with the implanted buried layer formation into the 5-10 Ωcm p (100) 4" substrate. After the blanket epitaxy of the entire LDC/SiGe-base/LDE/ HDE layer structure the emitter mesa is defined by reactive ion etching masked by oxide.

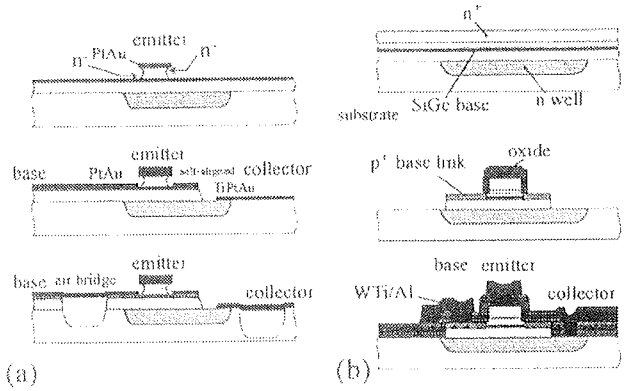


Fig.4 Process flow of (a) a non-passivated quick test SiGe-HBT and (b) a passivated double mesa SiGe-HBT

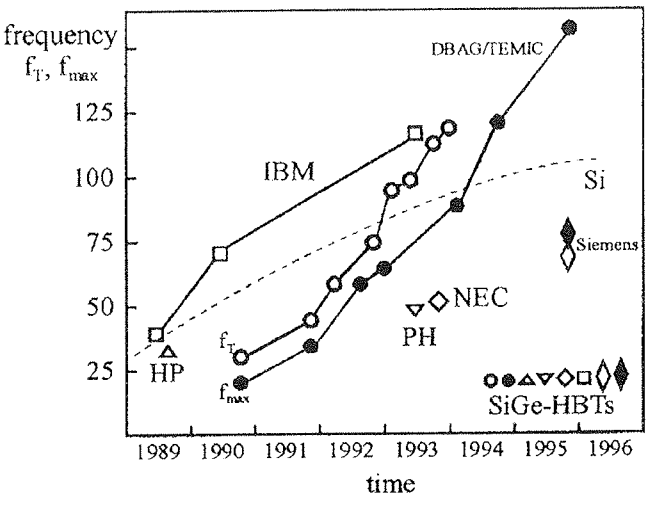


Fig 5: Development of the frequencies f_T and f_{max} of SiGe-HBTs

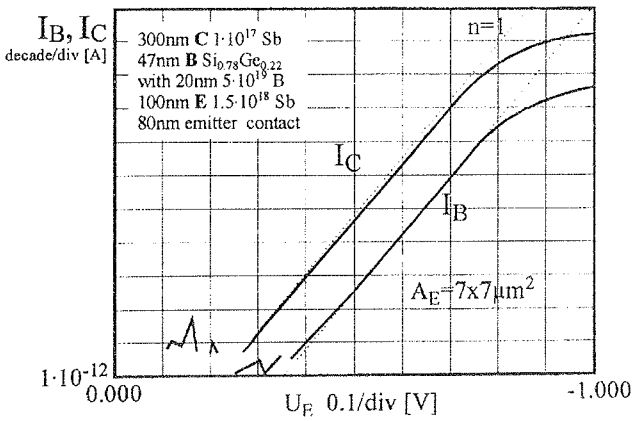


Fig.6: I-V characteristic of a passivated Si/SiGe-HBT

An outer base contact implantation is necessary to reduce the parasitic resistances. Low temperature passivation (LTO) by CVD SiH_4/O_2 at 300°C follows after etching of the BC-mesa and annealing of the contact implantation. Contact holes are defined and the WTi/Al-metallisation is wet chemically etched. Conventional silicon process technologies use high temperature oxidation and high temperature gettering processes to ensure a high quality surface passivation of the active and passive device areas and a low level of active metal contaminants. That is not acceptable for Si/SiGe-HBTs, because of the strong outdiffusion of the base and the SiGe layer relaxation. The Gummel plot in Fig. 6 shows a low temperature budget SiGe-HBT after a 450°C N_2/H_2-anneal. The passivation seems to be sufficient for Si/SiGe/Si double mesa transistors, according to the good ideality at low currents.

For the production of SiGe-HBTs TEMIC uses their Si-bipolar production line. The process, which was recently described in /58/, starts with a buried layer formation and a channel stop implantation in a 20 Ωcm substrate. The collector layers are formed by a 700 nm CVD silicon deposition and seperated by a recessed LOCOS process. The collector contact regions are implanted with phosphorus. Subsequently the differential CVD or MBE growth of the SiGe-base and the n-emitter follows. The 24-26% Ge and the $4\text{-}5\cdot10^{19}cm^{-3}$ boron are kept constant in the SiGe-base. The growth is monocrystalline in the oxide windows and poly-crystalline on the SiO_2. The CVD/MBE-poly-silicon, originally n-type, is converted to p by a BF_2 implantation. A selectively implanted collector offers the possibility to build transistors with high breakdown voltage and low collector-base capacitance and on the same wafer HBTs with higher current densities and higher f_T, but higher capacitance and lower breakdown voltage. In order to reduce the lead and the contact resistances titanium silicide is formed by a salicide process. The fabrication process ends with a two level Al metallization. Fig. 7 shows a top view of the transistor and Fig. 8 presents the transistor parameters.

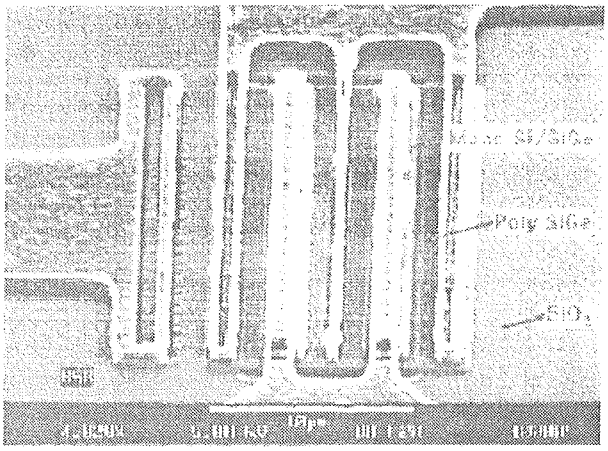


Fig.7: Top view of SiGe-HBT fabricated in a production line (TEMIC)

Parameter		no SIC	SIC
A_E	[μm^2]	1.2x2	1.2x2
N_C	[cm^{-3}]	3E16	1E17
BV_{CE0}	[V]	6.0	3.5
R_{sbi}	[Ω/]	1200	1200
h_{FE}	[ ]	150	150
V_A	[V]	50	40
f_T	[GHz]	30	50
f_{max}	[GHz]	50	50
F_{min}(2GHz)	[db]	1	1
R_B	[Ω]	140	140
C_{BC}	[fF]	10	15
C_{CS}	[fF]	22	22

Fig. 8: Transistor Parameter (TEMIC)

(b) passive components

High performance communication ICs need not only active but also passive devices. Fig. 9 gives an overview of the technological concept for resistors (R), inductors (L) and capacitors (C). After having processed the SiGe-HBT following layers are sputter-deposited: A 100 nm PECVD-oxide, the WSi_x-layer, the thin insulator IN_C of the integrated capacitors (SiO_2, Si_3N_4, AlN or TiO_2), the 50 nm WTi barrier and the 50 nm $Al_{(SiCu)}$ top layer. The MIM-structure for the capacitors is defined by the wet chemical etching of the $Al_{(SiCu)}$ and the WTi barrier.

An additional 300 nm PECVD-oxide insulates the upper electrode of the MIM-capacitor. After the contact hole etching and the wet chemical etching of the first metallization (WTi/$Al_{(SiCu)}$) the resistors and the capacitors are processed. A 3 μm thick polyimide is spun on and forms the IML (**I**nter **M**etal **L**ayer) for the isolation to the second metallization (100 nm WTi and 4 μm $Al_{(SiCu)}$). A second polyimide (1.5 μm) covers the second metallization and is opened only in the pad area.

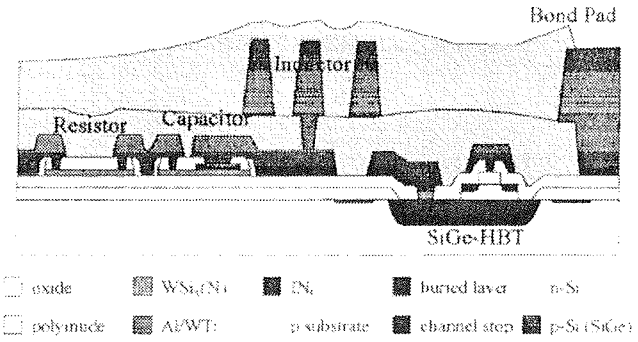


Fig. 9a: Schematic cross section of the two level metallization with the passive RLC-devices

L[nH]	n	D_a [μm] W/S=10/10	D_a [μm] W/S=10/5
1.25	2	190	175
	3	155	140
	4		130
3.00	2	330	315
	4	210	185
7.50	5	300	265
	7	280	240
15.0	6	385	
	8	350	340
	9		305

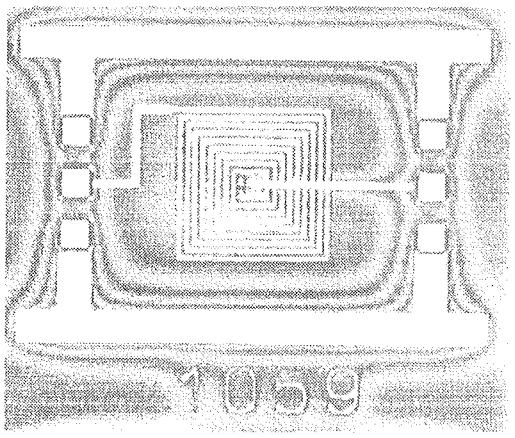


Fig. 9b: Table with the geometry of the spiral inductor (n=number of turns, L=inductivity, D_a=outer diameter, W=width of the Al-lines, S=distance between the lines) and a top view of a integrated inductor with polyimide between the to metallizations.

Resistors: For high performance analog and digital circuits there is a great interest for integration of thin film resistors (TFRs), because of the poor longterm stability of polysilicon resistors due to their polycrystalline structure. The materials of integrated TFR are WSi_x or WSi_yN_z /59/, $FeSi_x$ /60/, NiCr and $NiCr_xO_y$ /61,62/, Ta_2N /63/ or RuO_2 /64/. In contrast to VLSI integration, for most of these materials the lateral definition is done by lift off techniques or wet chemical etching. However sputtered $WSi_x(N_y)$ can be structured in F-based plasma or reactive ion etching and has a long term stability against temperature and current stress and has a sufficient resistance for most applications. The conductivity of the $WSi_x(N_y)$-TFRs is defined by the DC-power and the Ar/N_2 gas flow. Target values are R_S=100Ω (**WSi_x**: 30sccm Ar, 220W, 0.51Ωcm, d=52nm) and R_S=1000Ω (**WSi_xN_y**: 30sccm Ar, 4sccm N_2, 220W, 6.00Ωcm, d=58nm). The homogenity of the sheet resistance R_S across a 4 inch wafer is below 2% for R_S=100Ω and around 10% for R_S=1000Ω, with a high batch to batch reproducibility.

Capacitors: The integration concept for the capacitors has already been described above. The main advantage is the planar deposition of the bottom electrode (WSix), of the insulator IN_C and of the upper $WTi/Al_{(SiCu)}$ electrode e.g. in one multi target PVD machine. We use 20 nm PVD-SiO_2 and 45 nm AlN and receive capacitances of C*=6.0 fF/μm^2 and 2.3 fF/μm^2. In addition other materials with higher dielectric constants have to be tested to reduce the parasitic inductor.

Inductors: In monolithic microwave integrated circuits (MMICs) spiral inductors are used. They will be applied as reactive loads, for low-noise coupling purposes and in matching networks. From these applications inductors should have a high imaginary part and a high quality factor Q. The layout optimization of the spiral inductors for applications in the 2 (7.5 nH), 5 (3.0 nH) and 12 GHz (1.25 nH) range is shown in Fig. 9b. The inductivities are calculated using the Greenhouse Algorithmus /65/. Some of the measured inductivities and quality factors are plotted in Fig. 10. The difference between the measured and target inductivity values is due to the Ing contact lines. The quality factors increase with decreasing substrate loss and thicker second metallization and/or a thicker IML. The maximum of the quality factors is near the operating frequency.

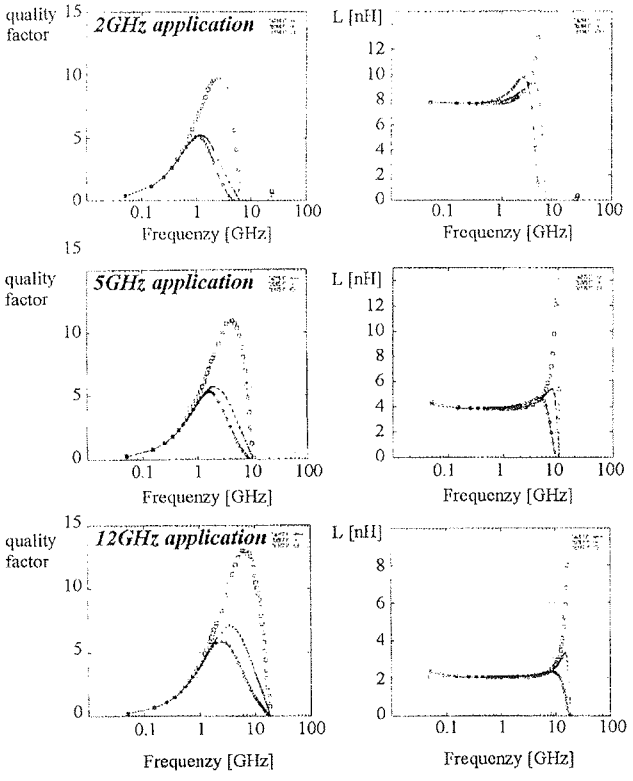


Fig. 10: Measured inductivity and quality factor for different frequency ranges.

3. SiGe-HBT circuits

Various HBT-ICs have been reported so far, some with outstanding, some at least with promising performances. Fig. 11 shows a chip with circuits for 5 to 40 GHz operation realized on semiinsulating Si-substrate. More production like are circuits on 20 Ωcm substrates (one example in Fig. 12), has under development at TEMIC/66/. ECL ring oscillators realized by Siemens, Philips, IBM, NEC, or Temic together with our house (DBAG) exhibit 11 to 20 ps /52,67-69/. A 12 bit DAC operating at 1 GHz has been demonstrated by IBM together with ADI /70/. NEC has reported on D-type flip-flop for 20 Gbit/s, a selector for 30 Gbit/s and 33 ps, a 2:1 multiplexer for 20 Gbit/s and a preamplifier with 19 GHz and 36 dB /71,72/. Multiplexer and demultiplexer

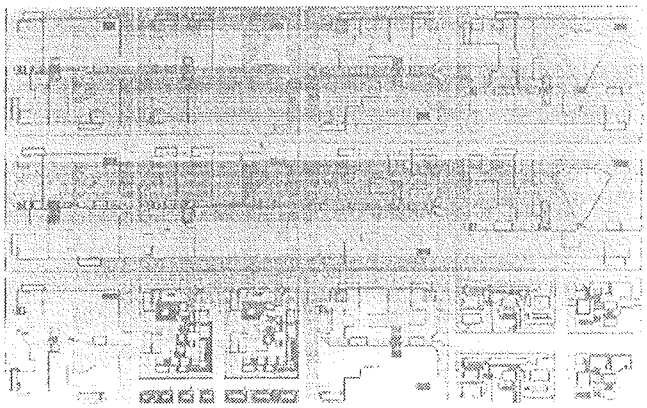


Fig.11: SiGe-HBT chip with circuits for 5-40 GHz.

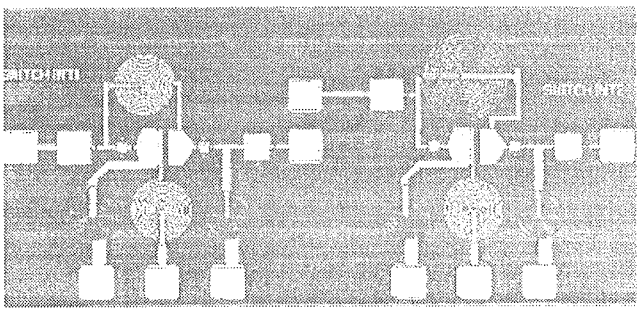


Fig.12: SiGe-HBT switches for 2 GHz with spiral inductors (Temic) /66/

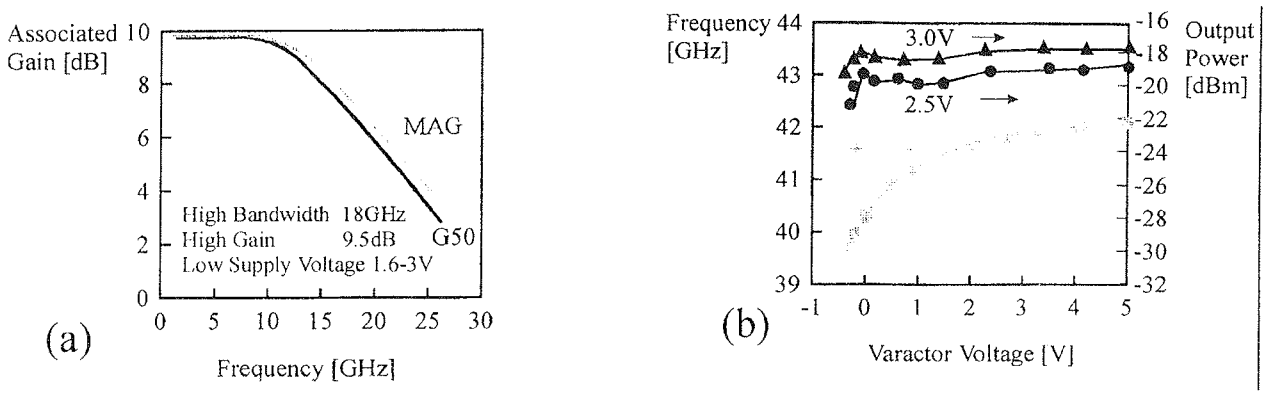


Fig.13: Low power consumption broad-band amplifier a) and varactor controlled oscillators with SiGe-HBTs /74,75/

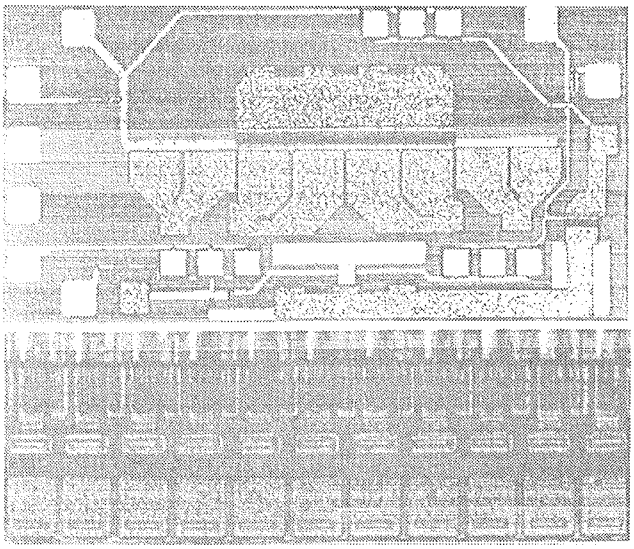


Fig. 14: SiGe-HBT power amplifier and enlarged emitter area

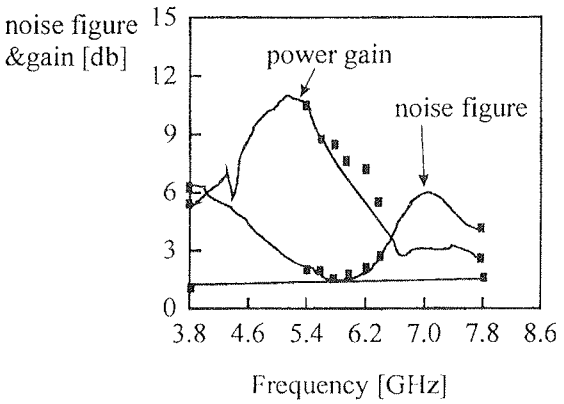


Fig. 16: Hybrid active antenna with a SiGe HBT yielding low noise at a receiving frequency of 5.8 GHz (Uni Ulm)

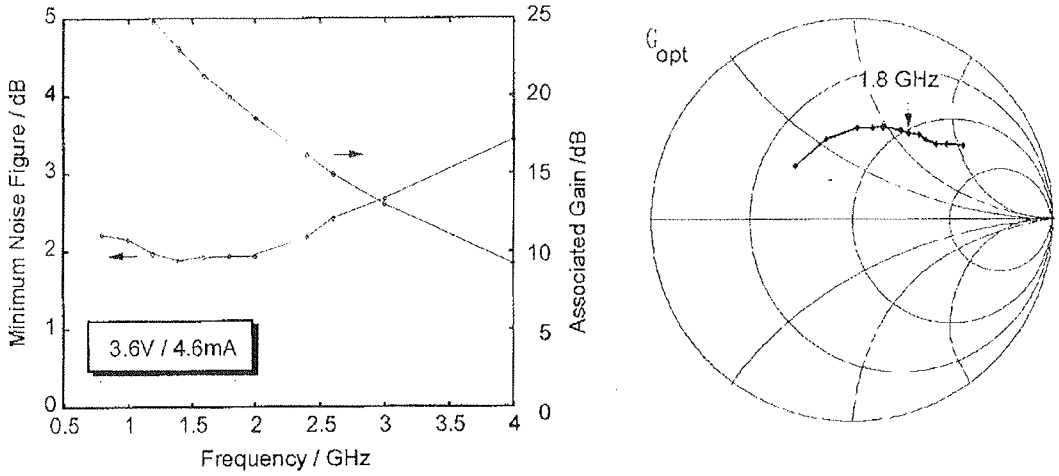


Fig. 15 Low-Noise Amplifier using SiGe HBTs for DECT Receivers (Uni Ulm) /76/.

with 28 Gbit/s have been realized by the Ruhr University Bochum using samples from DBAG /73/. A wideband amplifier capable of 9.5 dB gain with 18 GHz bandwidth while drawing only 50 mW from a 3 V supply and operating even at 1.6 V was realized (Fig. 13a) /74/. Varactor controlled oscillators for different frequency ranges of 1.8, 11, 26, 28, 40 GHz (e.g. see Fig. 13b) were presented by Nortel together with IBM, by TEMIC, by IBM and by DBAG /75, 76/. Power amplifiers for 0.9 to 2 GHz have been realized by Temic together with DBAG (Fig. 14) and by Philips /54, 77/. LNAs with F_{min} of 1.7 to 1.9 dB came from Temic together with DBAG and the University of Ulm (Fig. 15) A frequency devider of 42 Gbit/s was recently realized by Siemens /78/. We have used SiGe HBTs for hybrid intergration, too: A dielectric resonator oscillator (DRO) for 9.6 GHz and a 8-12 GHz VCO were reported by DBAG and Dornier /79/. Very recently an active antenna for receive at 5.8 GHz with the excellent noise Figure of 1.4 dB was reported by the University of Ulm using a device of DBAG (Fig. 16) /80/.

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AN EVALUATION OF AN EXPERIMENTAL GLASS FRIT FREE THICK FILM METALLIZATION FOR AIN-CERAMICS

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Keywords: semiconductors, semiconductor devices, power electronics, AIN ceramics, aluminum nitrides ceramics, thick film metallization, metallization of AIN ceramic, electrical conductive pastes, metallization pastes, thick film pastes, glass frit free metallization pastes, TiCuAg thick film metallization, SEM analysis, Scanning Electron Microscope Analysis, surface analysis, evaluation of experiments

Abstract: A glass frit free thick film paste has been especially developed for metallization of AIN ceramic. The metallized ceramic has been characterized theoretically as well as by experiment. A numerical analysis of temperature distribution induced by a continuous and pulsed mode operating heat source has been conducted by means of a finite element program. With regard to evaluate the adhesion properties of the metal film the tensile strength of the metallization has been determined.

Vrednotenje eksperimentalne prevodne debeloplastne paste brez steklene faze za metalizacijo AIN keramike

Ključne besede: polprevodniki, naprave polprevodniške, elektronika močnostna, AIN keramika nitridi aluminijevi, metalizacija debeloplastna, metalizacija AIN keramike, paste prevodne, paste metalizacijske, paste debeloplastne, paste metalizacijske brez zmesi kalcinirane za steklo, Ti-Cu-Ag metalizacija debeloplastna, SEM analize, analiza površine, vrednotenje preskusov

Povzetek: Razvili smo prevodno debeloplastno pasto brez steklene faze, namenjeno posebej za metalizacijo AIN keramike. Metalizirano keramiko smo ovrednotili teoretično in eksperimentalno. Numerična analiza porazdelitve temperature substrata za stalni in pulzni izvor toplote smo opravili s pomočjo programa, ki uporablja tehniko končnih elementov. Oprijemljivost metalnega filma pa smo določili z meritvijo natezne trdnosti metalizacije.

I. INTRODUCTION

Aluminium nitride shows an excellent thermal conductivity and a thermal expansion coefficient which is well matched to that of silicon. The lack of toxicity in comparison to beryllia makes AIN-ceramic a very competitive substrate material for power electronics application. A range of standard thick film pastes are available for the metallization of ceramics. Glass frits or different oxides which are added to thick film conductor pastes are responsible for the adhesion of the metal film on conventional alumina substrates. During the firing cycle the glass frits form a glass phase which interlocks the metallic conductive phase and the substrate. The thermal expansion coefficient of the glass phase must be matched to that of alumina. In contrast to the so called glass bonded systems the oxides of chemical bonding systems interact during the firing cycle with the alumina and form spinels which are responsible for adhesion of metallization. Mixed bonding conductive pastes comprise both kinds of bonding systems. The selection of a conductor paste with a specific bonding system depends on the requirement of application. Conductor pastes based on a chemical bonding system are very well suited for circuits built up in chip and wire technique. On the other hands the glass phase of glass bonding systems penetrates frequently the surface of metallization which consequently impedes the development of reliable bonding sites. Metallized substrates carrying power devices are acting as heat sinks and are

responsible for heat removal. For an efficient heat management it must be provided that the thermal resistance between the power dissipating device and the substrate is as small as possible. The thermal resistance formed by the glass phase of a glass bonding conductor system becomes critical if a substrate with a high thermal conductivity is applied while it is ignorable for a standard alumina substrate.

Although thick film technique enables to realize conductor lines with a sufficient thickness which is necessary for circuits carrying high current some problems arise with regard to its application to AlN-ceramic substrates. There exists often paste incompatibilities between standard thick film pastes utilized for conventional Al_3O_2-substrates and AlN-substrates which result in poor adhesion and blistering of metallization. Unfortunately only glass frit containing pastes are suitable for applications onto AlN ceramic substrates. The advantage of the high thermal conductivity of the AlN-ceramic will be affected by the *glass* phase acting as interlocking layer. Till today not any chemical bonding thick film conductor system for AlN is available which would provide an interface of low thermal resistance between AlN and the metallization.

2. TiCuAg-METALLIZATION SYSTEM

In our project we have developed a glass free conductor thick film system which would be accommodated to the requirements of AlN. Actually a TiCuAg thick film composition has been prepared where the amount of added Ti varied between 1 at% and 20 at%. The Ti should act as bonding agent between the metallic AgCu-solution and the AlN ceramic. The considered thick film paste must be fired under an inert atmosphere to avoid oxidation. It was expected that at the interface between the aluminium nitride ceramic and the thick film metallization a continuous titanium nitride layer and a compound of $(TiCuAl)_6N$ a so called η-phase should be formed (Figure 1).

The latter compound and other related nitrides play a significant role with regard to the adhesion and the development of stresses at the interface. Aluminium nitride and TiN grains comprise arrays of dislocations which are presumably arising from thermal expansion mismatch between the involved materials. Above the TiN layer a continuous layer of equiaxed and nearly defect free η-phase grains is formed. Beyond this η-phase layer the metallic solution of Cu and Ag is built up. These structures and the morphology of the interface between metallization and AlN-ceramic have been detected by studying the reactive bonding mechanism of Ti doped metal foils and aluminium nitride. By analogy with the metal foil-AlN ceramic compound the same phases should develop at the interface between AlN ceramic substrate and corresponding thick film metallization.

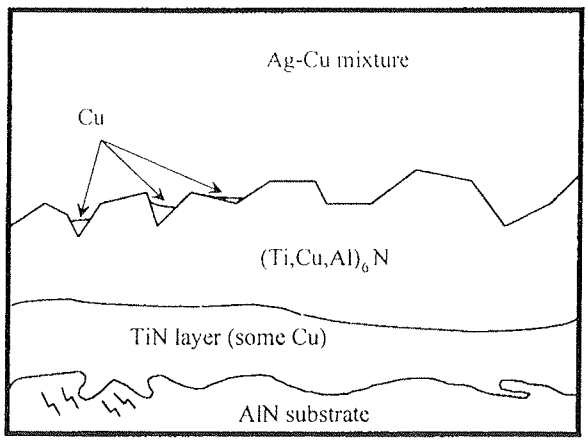

Figure 1: Structure of interface between glass frit free metallization and AlN /1/

2.1 Paste formulation

By application of the so called polyol process Ag and Cu frits with a grain diameter <3 µm have been produced. Ti frits have been prepared by cracking and milling the intermetallic compound Cu_3Ti_2. A binder system on the base of polyacrylic acid (PAS) has been selected. This binder organic provides a paste rheology suitable for the screen printing process and enables a firing process under a non oxidizing atmosphere, as well. The binder should decompose and evaporate completely during the firing cycle. A typical paste composition is listed in Table 1 /2/.

Table 1: Typical paste composition

Component	Weight%
PAS	13,1
α-terpineol	12,9
metal powder	60,7
dibutylphtalate	5,4
tertbutanol	7,9

2.2 Preparation of metallization

The experimental paste was printed on AlN-substrates by a conventional screen printing process utilizing a 200 mesh screen as well as a metal stencil of 100 µm thickness. The printed layer was leveled at room temperature for few minutes and dried at 75°C for 10 minutes in a drying furnace.

Firing of the samples has been carried out in a conventional thick film furnace under a nitrogen as well as an argon atmosphere with a maximum oxygen content of 15 volppm at a standard heat profile with a peak temperature of 850°C or 950°C, respectively, a dwell time of 10 minutes and a total heat cycle time of 60 minutes.

3. CHARACTERISTICS OF METALLIZATION

Different types of effects have been observed on the fired metal films. The paste fired at 850°C shows cracks extending to the bottom of metallization (Figure 2). The metallization exposed to firing temperature of 950°C shows ball shaped structures dispersed on its surface as well as cracks (Figure 3).

By means of microprobe analysis the ball shaped structures have been identified as grains especially containing Ti and Cu. Sometimes the irregularities of the surface finish of the metallization may be related to the marks of wire mesh caused by the screen printing process. In this case an improvement should be achieved by stencil printing. Neither by screen printing nor by stencil printing an uniform crack free metallization surface has been obtained.

To study the influence of film thickness on crack formation paste has been applied with increasing thickness by a single free hand stroke utilizing a rubber blade. The sample has been exposed to the above mentioned standard drying and firing process. This experiment reveals that with increasing layer thickness the cracks develop already during the drying process while during the firing cycle the growth of cracks only proceeds. Regions of the thin layer exhibit a crack free surface (Figure 4) while areas with high layer thickness are perforated by cracks extending to the surface of the substrate (Figure 5). To provide a voidfree uniform paste coverage of AIN-substrate the paste with the considered formulation has to be applied by screen printing of three layers. Each layer was dried and tired separately. The fired metallization thickness varied between 80 and 100 μm.

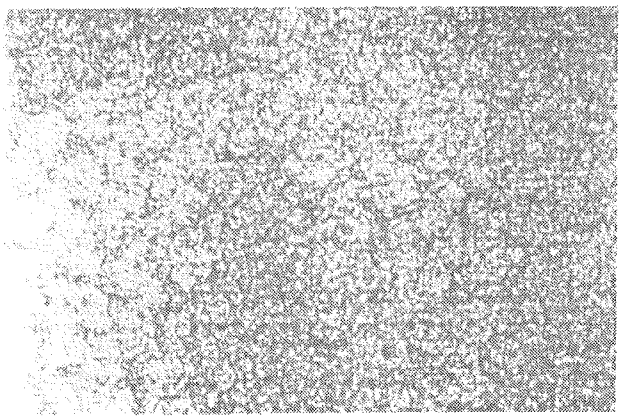

Figure 2: Metallization with cracks (paste containing 1 at% Ti, firing temperature: 850°C).

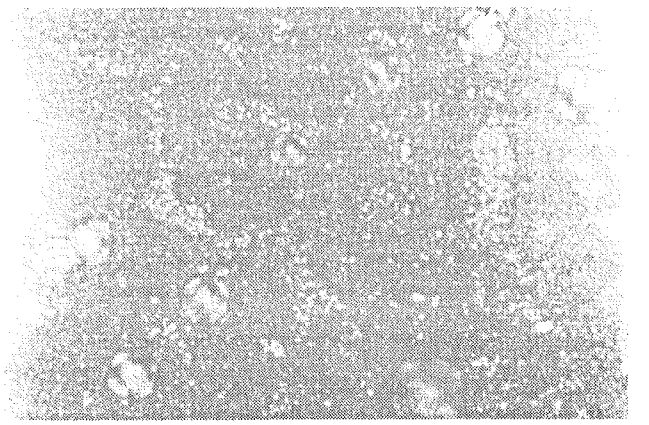

Figure 3: Metallization surface with dispersed ball shaped structures (paste containing 1 at% Ti, firing temperature: 950°C).

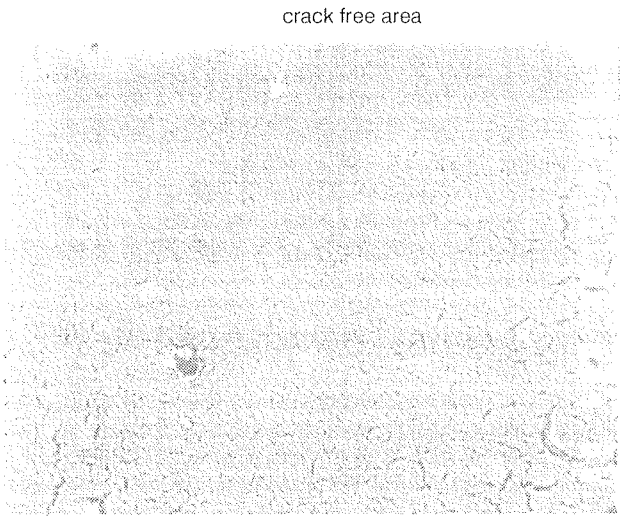

Figure 4: Crack free metallization (paste containing 2,5 at% Ti, firing temperature: 850 °C, dwell time: 30 minutes, firing atmosphere: argon, film thickness: <10 μm).

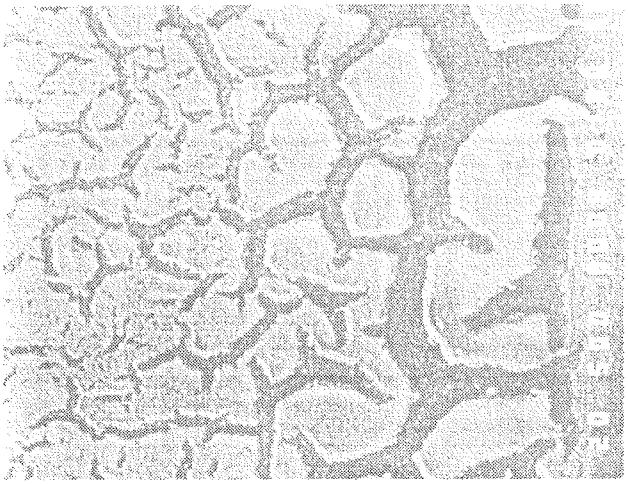

Figure 5: Metallization perforated by cracks (paste containing 2,5 at% Ti, firing temperature: 850 °C, dwell time: 30 minutes, firing atmosphere: argon, flm thickness: 25-30 μm).

3.1 Formation of TiN-interface and adhesion strength

A cross sectional view of a metallographically prepared metallized aluminium nitride fired under nitrogen is shown in Figure 6. The titanium distribution analysis carried out by means of an energy dispersive spectroscopy shows not any agglomeration of titanium at the interface between metallization and the ceramic (Figure 7). The adhesion strength of metallization is a significant measure if a TiN layer has been already developed.

The pull test has been conducted with the metallizations realized by our glass frit free conductor system as well as by commercially available glass frit containing copper pastes for comparison purpose. Epoxy precoated aluminium nail head pins were bonded to the surface of the metallization pads. The test samples were inserted in a pull tester. A pulling force was applied on the pins and continuously increased until failure occurred. Because of the significant poor adhesion strength and the lack of any Ti agglomeration at the substrate/metallization interface the time of firing at peak temperature has been increased from 10 minutes to 120 minutes. An increase of exposure time should promote the Ti-diffusion to the interface and subsequently the formation of TiN which would improve adhesion strength.

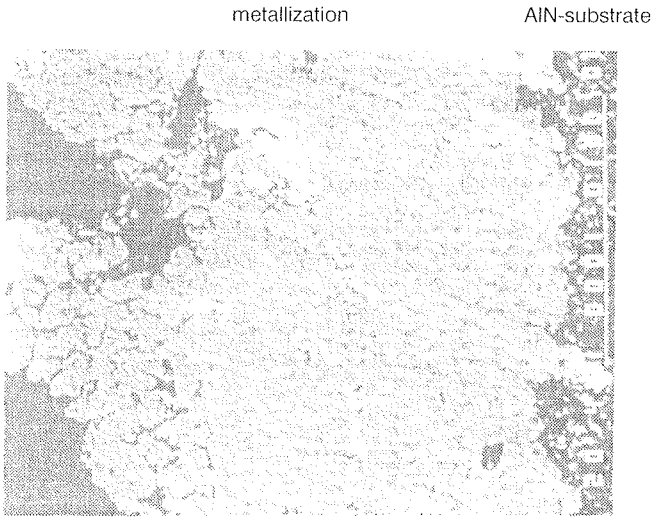

Figure 6: SEM image of the metallization cross section (paste containing 2,5 at% Ti, firing temperature: 850 °C).

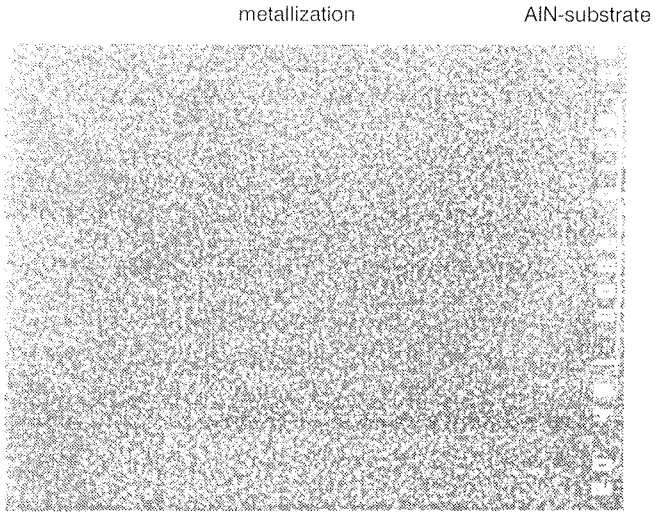

Figure 7: Ti-distribution along the cross section of metallization (paste containing 2,5 at% Ti, firing temperature: 850 °C).

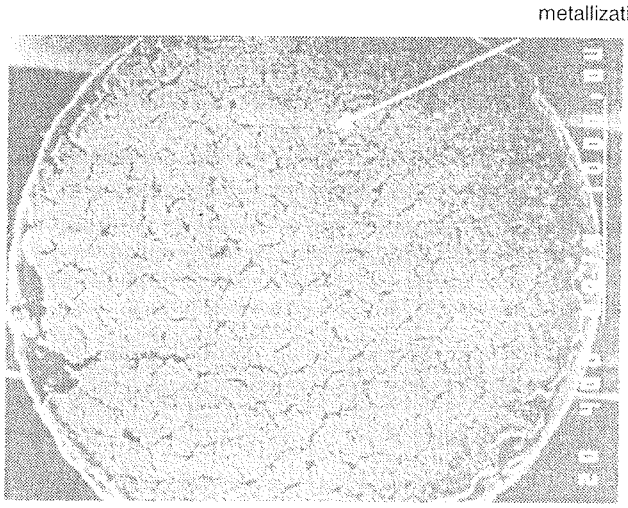

Figure 8a: SEM micrograph of the nail head after exposure to pull test (paste containing 2,5 at% Ti, firing temperature: 850 °C. dwell time: 30minutes. firing atmosphere: nitrogen).

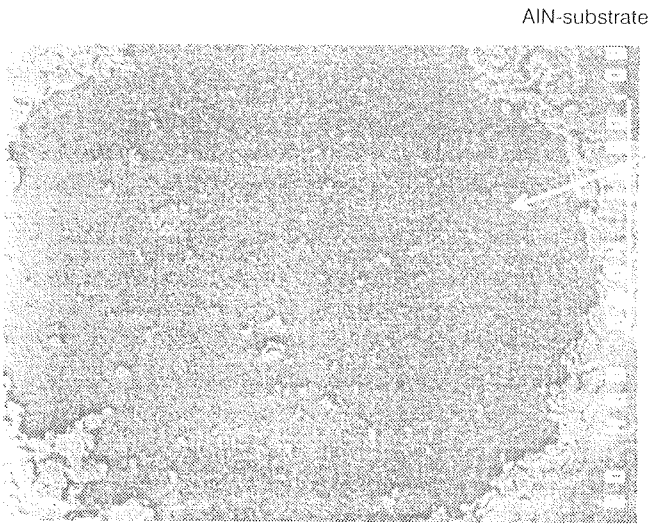

Figure 8b: SEM micrograph of the AlN-substrate after exposure to pull test (paste containing 2,5 at% Ti, firing temperature: 850 °C, dwell time: 30 minutes, firing atmosphere: nitrogen).

Actually, an increase of firing time contributes to an improvement of adhesion strength but nevertheless the results are quite unsatisfactory. The recorded adhesion strength of our experimental metal films amounts only 20 to 50 percent of the values achieved with glass containing metallizations. Figure 8 shows SEM-photographs of the nailhead and the corresponding area of aluminium nitride ceramic after the pull test has been carried out. Nearly all the metallization film has been lifted off from the ceramic and adheres consequently on the nail head.

A change of processing conditions has resulted in a drastical increase of adhesion strength. Instead of nitrogen the samples were purged with an argon-atmosphere during firing cycle. Evidently under the nitrogen atmosphere the dispersed Ti-particles react already with the surrounding atmosphere and TiN is formed. Consequently, the driving force for the Ti diffusion to form TiN at the interface between metallization and the ceramic is missing. In contrary the argon atmosphere does not react with titanium. This fact evidently provides the ability of titanium to react with the nitrogen sites of AlN and is the driving force for the Ti-diffusion.

Although the titanium element distribution analysis carried out on argon fired metallizations shows also not any agglomeration of Ti (similar to that of Figure 7) the TiN-layer must have been already formed. The adhesion strength of the metallization is already comparable to that of the different glass bonded copper pastes. Therefore it must be supposed that the amount of added Ti to the paste is still so small that an agglomeration of Ti in a very thin layer is not detectable by means of microprobe analysis. The excellent adhesion of metallization is also documented by the REM-photographs (Figure 9) of the lifted off nail heads and the corresponding area of the metallized AlN-substrate where the studs have been attached. The metallization could not be removed from the substrate by the applied force.

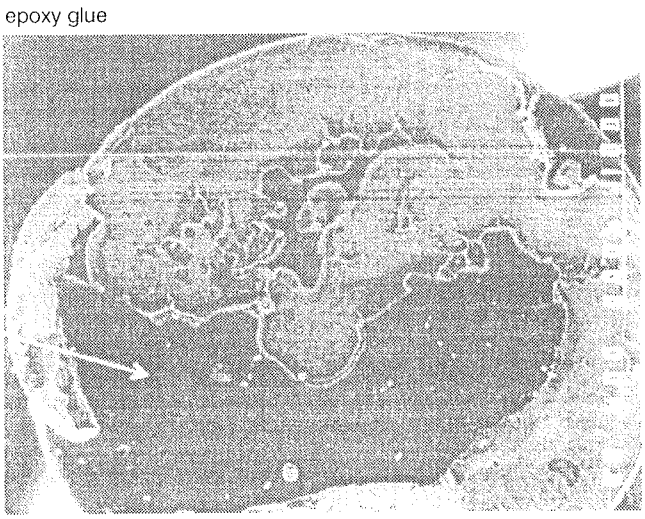

Figure 9a: SEM micrograph of the nail head after exposure to pull test (paste containing 2,5 at% Ti, firing temperature: 850 °C. dwell time: 30 minutes, firing atmosphere: argon).

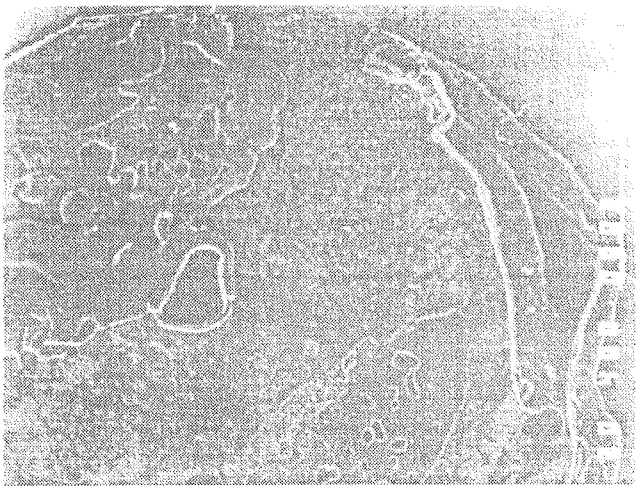

Figure 9b: SEM micrograph of the corresponding AlN-substrate area after exposure to pull test (paste containing 2,5 at% Ti, firing temperature: 850 °C, dwell time: 30 minutes, firing atmosphere: argon).

Actually, the adhesion strength of the metallization must be higher as recorded in the graph of Figure 10. Actually the tensile strength was limited by the bonding strength of the epoxy glue.

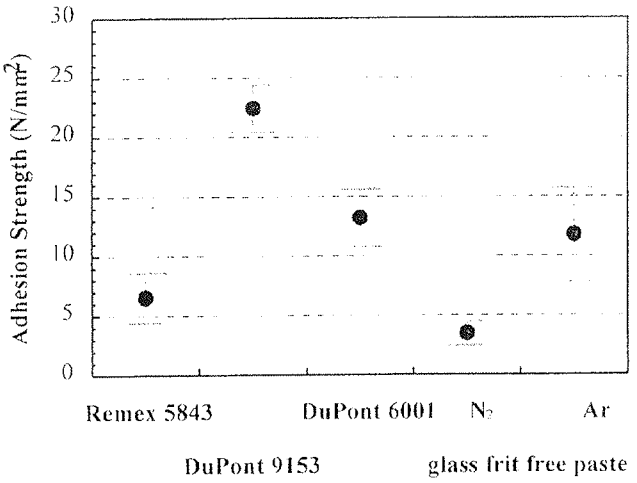

Figure 10: Adhesion strength distribution of commercially available glass frit containing copper pastes and experimental glass frit free Ag-CuTi-paste containing 2,5 at% Ti, firing temperature: 850°C, dwell time:30 minutes) fired under nitrogen as well as under argon.

4. NUMERICAL SIMULATION

Beside the practical investigations numerical analyses of metallized ceramic substrates have been carried out by means of a finite element program. The aim of the numerical simulation was to quantify the influence of the interlocking phase between ceramic and metallization. The object of simulation concerns a ceramic substrate

Table 2: Materials property data

Material	Density ρ [kg/m^3]	Thermal Expansion α [$10^{-6}K^{-1}$]	Thermal Conductivity k [W/mK]	Specific Heat c_p [J/kgK]
AlN	3 260	4,9	170	72
Al_2O_3	3 780	6,8	24	800
Lead-Boron-Silicate-glass	4 650	6,96	1,5	669
Copper	8 960	17	394	386
TiN	5 220	6	20	650
Ti_3Cu_2AlN (η-phase)	5 622	-	45,2	536

where a metallized pad was positioned in the center of the substrate surface. Aluminium nitride as well as conventional alumina for comparison purpose have been considered as substrate material. The metallization thickness was committed to be 15 µm a thickness which is usually achieved by thick film technique. Table 2 shows the data of materials properties utilized for computer simulation.

The models considered in this simulation are based on the assumption that the pads consists of a layered structure with different performances (Figure 11).

Because of the symmetrical structure of the metallized substrate it is sufficient to restrict the simulation model to one quadrant of the substrate. Actually, the results of simulation will be identical for all remaining three quadrants. The computations were carried out for different power applied on the surface of the copper film. The absorbed power flows vertically through the metal film into the substrate where it dissipates.

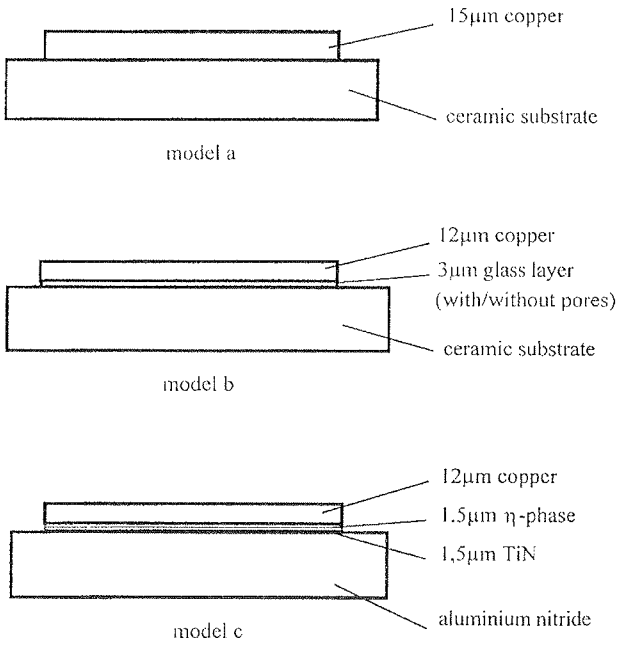

Figure 11: Models of layered metallization pads.

An applied power of 1 W induces a temperature distribution in the compound after a settling time of 100 s as shown in Figure 12. The temperature distribution analysis yields nearly identical results for all considered metallization models.

A summary of the resulting peak temperatures for the different metallization models are shown in Table 3. T_1 and T_{100} denote the temperature (peak temperature) in the center of the surface of the substrate after a settling time of 1 s and 100 s, respectively. T_{100} is characterizing already the steady state condition. Evidently there exists not any significant differences for a bulk layer (model a) or a copper pad comprising a glass phase which may also contain pore inclusions (model b). Significant temperature differences with regard to the steady state condition may be contributed to the thermal properties of the different substrate materials. While the performance of the interface layer between metallization and ceramic is of negligible interest for a power device operated in a continuous mode the thermal resistance of the interface governs the thermal management of devices working in a pulsed mode.

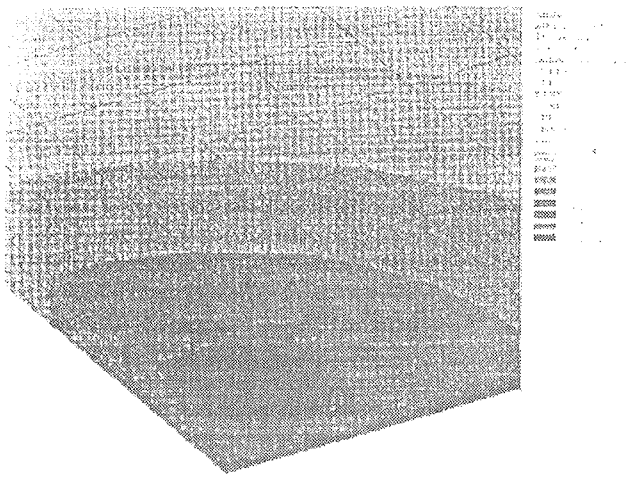

Figure 12: Temperature distribution after a settling time of 100 s of a metallized aluminium nitride substrate induced by a power of 1 W.

Table 3: Peak temperature of metallization pads.

		1 Watt (10^5 W/m^2)		10 Watt (10^6 W/m^2)	
		Al_2O_3	AlN	Al_2O_3	AlN
model a	T_1/°C	28,79	22,72	107,94	47,16
	T_{100}/°C	58,31	38,14	403,05	201,44
model b: without pores	T_1/°C	29,15	22,92	111,51	49,23
	T_{100}/°C	58,47	38,35	404,68	203,52
model b: 50 vol% pores	T_1/°C	29,17	23,25	111,65	52,51
	T_{100}/°C	58,77	38,61	407,74	206,14
model c	T_1/°C	-	22,73	-	47,68
	T_{100}/°C	-	38,31	-	202,75

Figure 13 shows the temperature swing of a metallization with a glassy interface and an interface built up by an TiN-layer induced by a device operating in a pulsed mode. The temperature difference within a metallization containing pores amounts approximately 7°C while the temperature drop in a glass frit free layer is negligible. The advantage of a glass frit free metallization becomes especially evident for high power circuits operating in a pulsed mode.

5. SUMMARY

The development of a glass frit free thick film metallization for AlN-ceramic substrates shows already promising results. It shows an excellent adhesion to the AlN-ceramic. Nevertheless the morphology of the metallization layer has to be improved. Surface topography and morphology of metallization are governed by paste formulation. The reason for a rough surface as well as the development of cracks may be caused by a low solid content of the paste or by a small surface area of added metal frits. An increase of solid content of the paste seems therefore to be advisable. Unfortunately an increase of solid content would impair the printability of paste. Another binder and organic system must be selected and evaluated.

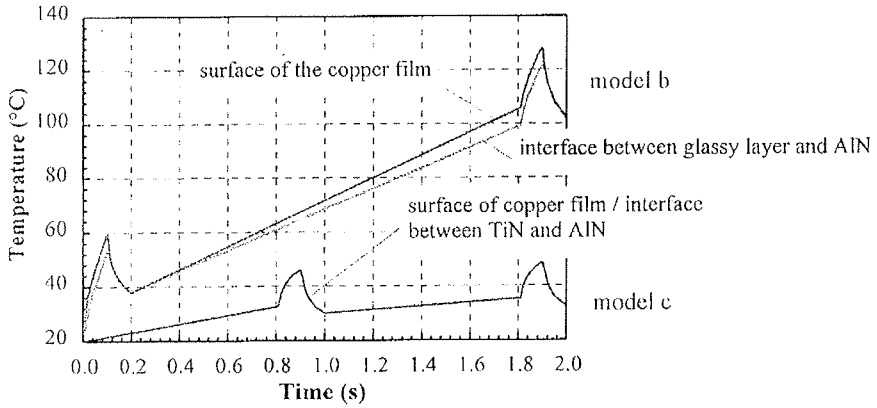

Figure 13: Temperature characteristic of metallization pads (model b comprising 50 vol% pores in glass layer and model c) operated in a pulsed mode (1 W, 5 Hz).

The electrical characteristic as well as solderability of the metallization are further topics of investigation.

6. REFERENCES

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/2/ A. Adlassnig, J.C. Schuster, R. Reicher, W. Smetana, "Synthesis of TiCuAg-Thick Film Inks for Glass Frit Free Metallization of Aluminium Nitride", Proceeding of the Workshop on Metal Ceramic Materials for Functional Applications and 3rd Workshop on Metal-Ceramic Composite Structures (Taiwan-Austrian Scientific Collaboration), June 1997, Vienna, 334-347.

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MIDEM´97 KONFERENCA: Predstavitev laboratorijev in sponzorjev
MIDEM´97 CONFERENCE: Presentation of Laboratories and Sponsors

Iskraemeco

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Introduction

Iskraemeco d.d. is the fourth largest European, and one of the world´s largest manufacturers of meters for electric energy. Our electricity meters with the Iskra trademark are well known throughout the world. Iskraemeco is increasing activities in the electronics line, especially in industrial multifunction meters and systems for management and billing of electric energy.

Iskraemeco´s History

The Iskra company began to produce single-phase electromechanical meters in 1946. The beginning of three phase meter production was in 1958. The application of modern science and technology, special microelectronics, has enabled the development of electronic meters and other modern measuring systems. We started to produce electronic precision meters in 1975, and in 1992 we began the regular production of household electronic meters based on full integration Hall-sensor.

Status

The Iskraemeco company was founded as a private joint-stock company in 1994.

Through the process of privatisation the company has reached ownership structure, where internal ownership takes precedence over external ownership. Now 60% of its ownership is possessed by internal owners.

Sales

In 1996, the income from the sales of products and services was approximately 150 million German marks. In the last 5 years the sales have increased fast in all markets - especially in the electronic line. Iskraemeco exports in 45 countries on all continents.

We own or hold shares in production companies in Russia, Malaysia, Croatia, Italy and trade companies in Germany, Sweden and Great Britain. Our induction electricity meters are being manufactured under licence in Spain, Tunisia, Colombia and Argentina.

Employees

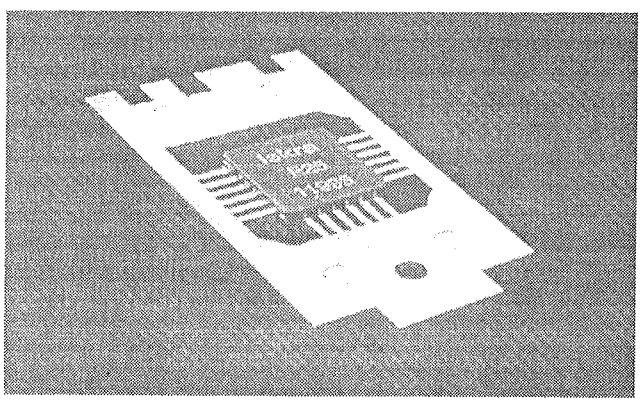
Parallel to the development and growth of Iskraemeco, the number of employees has increased for approximately 6 per cent a year in the last 5 years. Now there are approximately 2100 employees in Iskraemeco.

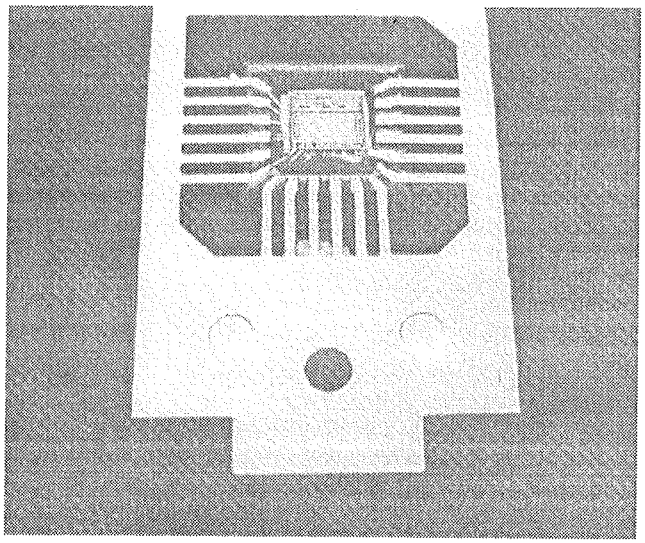
Development

The basic strategic orientation of our company in the area of development is to ensure a profitable and promising production line through investments in our own technological development.

The R&D sector today includes development groups working in different fields and technologies, the office for standardisation and documentation and laboratories. There are employed engineers of all educational levels and profiles.

We have worked in the microelectronics and sensoric area for many years, and many of our products are based on the microelectronic components, that we have developed.





For R&D and laboratory activities we allocate an average 6 percent of our total revenues.

Microelectronic History

We began activities on microelectronic design in the early 70´s. The first chip for time division meter was designed in 1974 by the Laboratory for Microelectronics at the University of Ljubljana.

In the 80´s many decoders and switched capacitor filters for ripple control receivers were designed. Research of integrated circuit for electrical metering with integrated Hall sensor also began. Currently, electronic electricity meters made by Iskraemeco are integrated on one chip. This chip is provided with the Hall sensor and analogue and digital circuits.

Microelectronics Now

In the R&D Department we have our own microelectronic design group and group for sensors researching. Many projects are in different development phases. We use some of the best software packets existing in the market (Cadence-Anacad) and we cooperate with the best Silicon manufactures in Europe. The professional level of these groups is compared to the European level of similar design houses. Our main work is based in mixed analog digital signal design. The latest projects we are working on are: Analog interfaces for different energy meters, A/D Converters, special purpose DSPs, custom cells for different applications and development of new sensor structures and magnetic systems.

KONFERENCA MIDEM´97 - POROČILO
MIDEM´97 CONFERENCE REPORT

33rd International Conference on Microelectronics, Devices and Materials - MIDEM´97

The 33rd International Conference on Microelectronics, Devices and Materials, MIDEM´97, continued the tradition of the annual international conferences organized by MIDEM, Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia. Traditionally, these conferences have provided an opportunity for experts from all over the Europe to meet and discuss new developments in the fields covered by the Conference. The goal of connection and building of the friendship among the scientists and their companies remained the keystone of the organizer.

As well, the Conference has always attracted distinguished guest speakers.

This time we had the opportunity to meet Dr. M. Drofenik, from Jožef Stefan Institute, whose paper "Microstructure and Physical Properties of MnZn Ferrites for the High-frequency Power Supplies" described MnZn ferrites as the currently most important electronic ceramics for applications up to the frequencies of 1 MHz. Next guest speaker, Dr. V. Kempe from AMS, Unterpremstaetten, Austria, in the paper "Mixed Signal ASICs - a Manufacturer´s View", showed that the mixed signal ASICs play very important role in the ASIC market, in most of the applications filling the gap between internal information processing and the external world. Dr. E. Wachmann from AMS, Unterpremstaetten, Austria, in the paper "Aspects of Submicron BiCMOS Technology Integration", showed the need for the integrated deep submicron BiCMOS processes for ASIC manufacturing. Dr.A.Born from the University of Hamburg, Germany, in his paper "Scanning probe Microscopy and Spectroscop: From Basic Research to Industrial Applications" showed that the development of scanning probe microscopy and spectroscopy had led to new insight into physics of the nanometer scale, as well as had become indispensable tool for the characterization and quality control of semiconductor devices. Dr. D. Behammer from Daimler-Benz Research Center, Ulm, Germany, in his paper "SiGe-Heterojunction Bipolar Transistors: Key Technologies and Applications in Communication Systems" described SiGe HBT as very attractive device for future broadband and wireless communication ICs due to its outstanding performance and low fabrication cost. The last guest speaker, Dr. W. Smetana from Technische Universitaet, Wien, Austria, in the paper "An Evaluation of an Experimental Glass Frit Free Thick Film Metallization for AlN-ceramics" presented theoretical and experimental characterization of a glass frit free thick film paste especially developed for metallization of AlN ceramics.

Also this year, special session devoted to presentation of microelectronics laboratories, enterprises and conference sponsors was held. The aim of the presentation was getting acquainted with the work and possibilities of different research groups, companies and their projects.

The work of the Conference was divided into several sessions as follows : Ceramics, Metals and Composites; Integrated Circuits; Technology and Devices; Thin Films; Device Physics and Modeling; Thick Films; Optoelectronics; Sensors.

The Conference Proceedings which was published along with the Conference has a volume of 391 pages

and is divided into several parts according to the Conference sessions. The Proceedings is assessed into INSPEC database.

The Conference was held at HOTEL ŠPIK, Gozd Martuljek, Slovenia, September 24th - 26th 1997. Its excellent conference capabilities and technical as well as menagerial support brought this Conference to a successfull end.

Let me add some statistical data:

On the Conference 6 invited and 49 regular papers were presented in the following sessions:

- Ceramics, Metals, Composites: 8
- Integrated Circuits: 8
- Technology and Devices: 6
- Thin Films: 6
- Device Physics and Modeling: 6
- Thick Films: 4
- Optoelectronics: 3
- Sensors: 8

There were totally 67 participants from the following countries: Slovenia, Italy, Germany, Austria, Hungary and Croatia

Iztok Šorli

MIDEM´97 PARTICIPANTS

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4	BERNIK SLAVKO	JOŽEF STEFAN INSTITUTE	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
5	BORN AXEL	UNIVERSITY OF HAMBURG	JUNGINS STR. 11a	D-20355	HAMBURG	GERMANY
6	BRAČUN DRAGO	FACULTY OF MECHANICAL ENG.	TRŽAŠKA 6	1000	LJUBLJANA	SLOVENIA
7	CVIKL BRUNO	FACULTY OF CIVIL ENG.	SMETANOVA 17	2000	MARIBOR	SLOVENIA
8	DEGEN ANDREJ	JOŽEF STEFAN INSTITUTE	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
9	DRAŽIČ GORAN	JOŽEF STEFAN INSTITUTE	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
10	DROFENIK MIHA	JOŽEF STEFAN INSTITUTE	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
11	FERK BRANKO	FACULTY OF ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
12	FURLAN JOŽE	FACULTY OF ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
13	HORVATH ZSOLT J.	RESEARCH INST.FOR TECH.PHYSICS	P.O.BOX 76	H-1325	BUDAPEST	HUNGARY
14	HROVAT MARKO	JOŽEF STEFAN INSTITUTE	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
15	JENČIČ IGOR	JOŽEF STEFAN INSTITUT	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
16	JENKO BOJAN	MZT	SLOVENSKA 50	1000	LJUBLJANA	SLOVENIA
17	JENKO MONIKA	IMT	LEPI POT 11	1000	LJUBLJANA	SLOVENIA
18	KAMIN MATEJ	FACULTY OF ELECTICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
19	KEMPE VOLKER	AUSTRIA MIKRO SYTEME INT.	SCHLOSS PREMSTAETTEN	A-8141	UNTERPREMSTAETTEN	AUSTRIA
20	KOPAČ DRAGO	ISKRAEMECO	SAVSKA LOKA 4	4000	KRANJ	SLOVENIA
21	KOROŠAK DEAN	FACULTY OF CIVIL ENG.	SMETANOVA 17	2000	MARIBOR	SLOVENIA
22	KOSEC MARIJA	MIDEM	DUNAJSKA 10	1000	LJUBLJANA	SLOVENIA
23	KOSMAČ TOMAŽ	JOŽEF STEFAN INSTITUTE	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
24	KOVAČ JANEZ	INST.OF SURFACE ENG. AND OPTOEL.	TESLOVA 30	1000	LJUBLJANA	SLOVENIA
25	KRIŽAJ DEJAN	FACULTY OF ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
26	KRNEL KRISTOFFER	JOŽEF STEFAN INSTITUTE	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
27	KUNC VINKO	FACULTY FOR ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
28	KUŠČER DANJELA	JOŽEF STEFAN INSTITUTE	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
29	LIMPEL META	MIDEM	DUNAJSKA 10	1000	LJUBLJANA	SLOVENIA
30	MAČEK JADRAN	FAC. OF CHEMISTRY AND CHEMICAL TECH.	AŠKERČEVA 5	1000	LJUBLJANA	SLOVENIA
31	MAČEK MARJAN	FACULTY OF ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
32	MAČEK SREČKO	JOŽEF STEFAN INSTITUT	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
33	MALI TADEJ	JOŽEF STEFAN INSTITUTE	JAMOVA 37	1000	LJUBLJANA	SLOVENIA
34	MALNARIČ SAMOEL	FACULTY OF ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
35	MARINŠEK MARJAN	FAC. OF CHEMISTRY AND CHEMICAL TECH.	AŠKERČEVA 5	1000	LJUBLJANA	SLOVENIA
36	MCGUINESS PAUL	JOŽEF STEFAN INSTITUTE	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
37	PANJAN PETER	JOŽEF STEFAN INSTITUTE	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
38	PAVLIN MARKO	HIPOT-RSS	TRUBARJEVA 7	8310	ŠENTJERNEJ	SLOVENIA
39	PERNE JOŽEF	ISKRAEMECO	SAVSKA LOKA 4	4000	KRANJ	SLOVENIA
40	PEVEC ALBIN	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
41	PIGNATEL GIORGIO	UNIVERSITI TRENTO	MESIANO 77	I-38050	TRENTO	ITALY
42	PLETERŠEK ANTON	FACULTY OF ELECTRICAL	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
43	RAIČ DUŠAN	FACULTY FOR ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
44	REICHMANN KLAUS	GRAZ UNIVERSITY OF TECHOLOGY	STREMAYRGASSE 16	A-8010	GRAZ	AUSTRIA
45	RESNIK DRAGO	FACULTY OF ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
46	ROČAK DUBRAVKA	JOŽEF STEFAN INSTITUTE	JAMOVA 39	1000	LJUBLJANA	SLOVENIA
47	ROČAK RUDI	MIKROIKS	DUNAJSKA 5	1000	LJUBLJANA	SLOVENIA
48	SLOKAN MILAN	MIDEM	DUNAJSKA 10	1000	LJUBLJANA	SLOVENIA
49	SMETANA WALTER	TECHNI. UNIV. WIEN	GURTHANS STR. 27-29	A-1040	WIEN	AUSTRIA
50	SMOLE FRANC	FACULTY OF ELECTICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
51	SOMOGYI KAROLY	RESEARCH INST. FOR TECHNICAL PHYSICS	FOTI UT 56	H-1325	BUDAPEST	HUNGARY
52	STARIŠINIČ SLAVKO	FACULTY OF ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
53	STRLE DRAGO	FACULTY FOR ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
54	SUHADOLNIK ALOJZ	FACULTY OF MEC. ENG.	AŠKERČEVA 6	1000	LJUBLJANA	SLOVENIA
55	ŠOBA STOJAN	HIPOT HYB	TRUBARJEVA 7	8310	ŠENTJERNEJ	SLOVENIA
56	ŠORLI IZTOK	MIDEM	DUNAJSKA 10	1000	LJUBLJANA	SLOVENIA
57	TASEVSKI MILAN	SIPO	KOTNKOVA 6	1000	LJUBLJANA	SLOVENIA
58	TOPIČ MARKO	FACULTY OF ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
59	TRONTELJ JANEZ	FACULTY OF ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
60	TROST ANDREJ	FACULTY OF ELECTROCAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
61	VODOPIVEC ANDREJ	FACULTY OF ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
62	VOJTEH MOČNIK	ISKRAEMECO	SAVSKA LOKA 4	4000	KRANJ	SLOVENIA
63	VRTAČNIK DANILO	FACULTY OF ELECTRICAL ENG.	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA
64	WACHMANN E.	AMS AUSTRIA	SCHLOSS PREMSTAETTEN	A-7141	UNTERPREMSTAETTEN	AUSTRIA
65	ZALAR ANTON	ITPO	TESLOVA 30	1000	LJUBLJANA	SLOVENIA
66	ZUPAN KLEMENTINA	FACULTY OF CHEMISTRY ANC CHEM. TECH.	AŠKERČEVA 5	1000	LJUBLJANA	SLOVENIA
67	ŽEMVA ANDREJ	FACULTY OF ELECTRICAL ENGINEERING	TRŽAŠKA 25	1000	LJUBLJANA	SLOVENIA

PREDSTAVLJAMO PODJETJE Z NASLOVNICE
REPRESENT OF COMPANY FROM FRONT PAGE

Murata
Manufacturing Co., Ltd.

New quality electronic equipment begins with new quality components and new quality components begin with new quality materials

Murata was founded in 1944 as a manufacturer of Titanium Oxide (TiO_2)-based ceramic capacitors. Since then, it has developed a wide range of ceramic materials including Barium Titanate ($BaTiO_3$), a material with an exceptionally high dielectric constant which was discovered simultaneously in Japan, the USA and the former Soviet Union; and Zirconium Lead Titanate ($Pb(ZrTi)O_3$, a material with a high piezoelectric constant. With this strong technical foundation, Murata has, over the years, developed and commercialized new functional ceramics with a wide range of electrical characteristics and its ceramic electronic components have always been at the leading edge of technology.

By virtue of its fully integrated production system, which covers all stages from raw materials to finished product, Murata has accumulated wideranging versatile expertise in various technologies associated with functional materials. Vertical integration with circuit design technology, processing and production technology, and measurement and evaluation technology, has allowed us to develop hybrid ICs (HIC®) and products based on ceramic multilayer technology. Presently, the horizon of our development activities is extending to include the planned commercialization of integrated module products.

As a company, Murata was quick to expand its business to manufacturing and selling its major products overseas, and as a result now enjoys a precious flow of information on advanced technology from markets right around the world. This information is utilized in all areas of research activily throughout the Murata organizations, so that technical development is implemented as efficiently as possible. Another important strategy for the future is our early stage involvement in the key customers' development of next-generation technology from the design stage. This strategy exemplifies our two-way approach, that is, needs-oriented from one angle and seeds-oriented from another angle, steering an access to the development of the next generation of technologies.

Magnetism

Magnetic substance stores magnetism

Magnetic bodies are materials which generate strong magnetism even in a weak magnetic field, or lines of magnetic force even where there is no magnetic field; in other words materials which have the property of storing magnetic energy. Ferrites are typical of magnetic ceramic materials. They are classified, according to their characteristics, as hard or soft ferrites. At Murata, we are exploiting these magnetic properties in EMI suppression filters and to tackle the problems of noise interference.

Dielectricity

Dielectricity stores electricity

Dielectric materials store electricity by polarization. Under the application of a voltage, positive and negative electric charges are separated, but no direct current (DC) flows. Dielectric ceramics are widely used in capacitors because of their high dielectric constant and excellent insulating properties. Murata has taken advantage of the dielectric properties of such ceramics to develop and market a wide range of capacitor products. Making use of Barium Titanate, a material with ferroelectric properties, Murata has commercialized a range of valuable products such as ultra-compact high-capacitance monolithic ceramic capacitors without lead terminals, which facilitate surface mounting. Such innovative technology and a reputation for quality has established Murata as a world leader in this field.

Piezoelectricity

Stone expands and contracts

Piezoelectric materials convert mechanical energy to electrical energy and vice versa. Murata has conducted extensive research into the piezoelectric characteristics of ceramics and, through the development of piezoelectric ceramic products, has remarkably enhanced the performance of electronic equipment and communications equipment. Murata is also a pioneer in the commercial development and volume production of ceramic filters (CERAFIL®) which result in higher-quality image and sound reproduction in televisions and radios. We have taken the same technology further in applying it to the creation of (CERALOCK®) reference resonators, piezoelectric buzzers and a host of other piezoelectric products.

Pyroelectricity

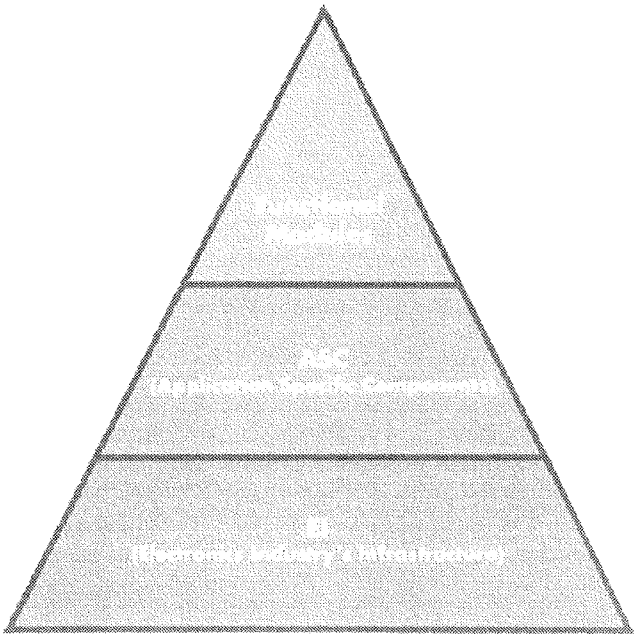
Ceramics which become electrically charged with temperature change

Among materials electrically polarized due to crystal structure, pyroelectric materials are such that they become electrically polarized with changes in temperature, the amount of electric charge produced varies according to temperature change. Using such materials, Murata has succeeded in mass producing pyroelectric infrared sensors that are able to detect changes in the temperature of people and objects at a distance. Murata's pyroelectric ceramics find application in contactless switches and temperature sensors, satisfying a wide range of needs in the sensor market.

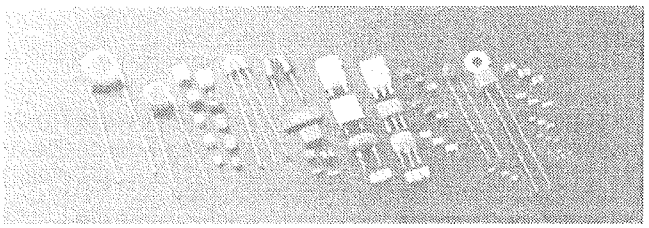
Semiconductivity

In-between insulators and conductors

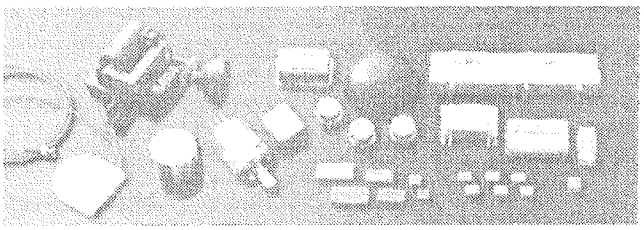
In terms of their ability to conduct electricity, semiconductors lie half way between insulating materials such as glass, which have high resistance, and conductors such as metals, which have low resistance. At Murata, it was noted that the resistance of semiconductors increases at a certain temperature, preventing the flow of current. This means that such semiconductive materials can act as PTC (positive temperature coefficient) thermistors. Exploiting this property, Murata successfully mass produces positive thermistors. In addition, Murata has also commercialized various types of capacitors using semiconductive materials to form "negative" thermistors, with semiconductor grain boundaries acting as insulators.



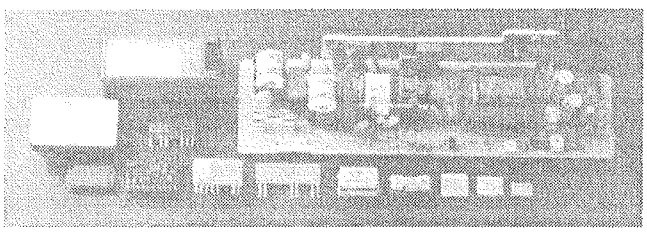
Major EI products



Major ASC products



Major functional modules



Company Profile

Trade Name:	Murata Manufacturing Company, Ltd.
Date of Incorporation:	December 23,1950 (established in October 1944)
Paid-in Capital:	Yen 64,325 million (as of May 1,1997)
Number of Employees:	4,329 (23,558 on a consolidated basis)
Offices and Plants	
Head Office:	26-10, Tenjin 2-chome, Nagaokakyo-shi, Kyoto 617
Phone:	(075) 951-9111
Plants:	Yokaichi Plant, Yokaichi, Shiga
	Yasu Plant, Yasu-cho, Yasu-gun, Shiga
	Yokohama R&D Center, Midori-ku, Yokohama-shi, Kanagawa
Divisional Office	Kawasaki Division, Nakahara-ku, Kawasaki-shi, Kanagawa
Overseas Branch and Offices:	Seoul Branch (S. Korea)
	ASEAN Representative Office (Singapore)
Domestic Subsidiaries:	Fukui Murata Manufacturing Co., Ltd.
	Izumo Murata Manufacturing Co., Ltd.
	Toyama Murata Manufacturing Co., Ltd.
	Kanazawa Murata Manufacturing Co., Ltd.
	Komatsu Murata Manufacturing Co., Ltd.
	and 19 other companies
Overseas Subsidiaries:	
North & South America	Murata Electronics North America Inc.(USA)
	Murata World Comercial Ltda.(Brazil)
	Murata Amazoia Industria E Comercio Ltda.(Brazil)
	Murata Electroica Do Brasil Ltda.(Brazil)
	and two other companies
Europe	Murata Europe Management GmbH (Germany)
	Murata Elektronik GmbH (Germany)
	Murata Elektronik Handels GmbH (Germany)
	Murata Electronics (Netherlands) B.V.(Netherlands)
	Murata Electronics (UK) Ltd.(UK)
	Murata Manufacturing (UK) Ltd. (UK)
	Murata Electronique S.A. (France)
	Murata Elettronica S.p.A. (Italy)
	and another company
Asia	Beijing Murata Electronics Co., Ltd. (China)
	Wuxi Murata Electronics Co., Ltd. (China)
	Murata Electronics Trading (Shanghai) Co., Ltd. (China)
	Taiwan Murata Electronics Co., Ltd. (Taiwan)
	Murata Co., Ltd.(Hong Kong)
	Murata Electronics Singapore (Pte.) Ltd. (Singapore)
	Murata Electronics (Thailand), Ltd. (Thailand)
	Thai Murata Electronics Trading, Ltd. (Thailand)
	Murata Electronics (Malaysia) Sdn. Bhd. (Malaysia)
	Murata Trading (Malaysia) Sdn. Bhd. (Malaysia)

For more information on Murata products, please call

Mr. Iztok Šorli, MIKROIKS, d.o.o.
Dunajska 5
1000 Ljubljana
tel. 061 312-898
fax 061 319 170

KONFERENCE, POSVETOVANJA, SEMINARJI, POROČILA
CONFERENCES, COLLOQYUMS, SEMINARS, REPORTS

NUCLEAR SCIENCE SYMPOSIUM AND MEDICAL IMAGING CONFERENCE
(9-15 nov. 1997, Albuquerque, New Mexico, ZDA)

Poročilo z IEEE konference

Od 9. do 15. novembra 1997 je bila v mestu Albuquerque, New Mexico, ZDA IEEE konferenca Nuclear Science Symposium and Medical Imaging Conference. Glede na ime konference se dozdeva, da je konferenca namenjena nuklearnim fizikom in doktorjem medicine. V resnici pa je glede na organizacijo, ki je v rokah IEEE (Institute of Electrical and Electronic Engineers) sekcije "Nuclear Sciences", konferenca usmerjena predvsem v raziskave in razvoj detektorjev za raziskave v fiziki visokoenergijskih delcev, detektorjev za medicinske aplikacije in seveda metodam za analizo rezultatov. Poleg te konference je potekala tudi konferenca "Medical Imaging Conference", ki v največji meri izkorišča znanja, pridobljena iz NSS konference, in jih aplicira v medicini. Še najbolje prikažejo razsežnost konference naslovi sekcij (posebej za NSS in MIC):

NUCLEAR SCIENCE SYMPOSIUM

- Analog and Digital Circuits
- Radiation Damage
- Space and Astrophysics Instrumentation
- Environmental and Personnel Alpha Monitoring
- Data Acquisition and Analysis Systems
- Detectors and Instrumentation
- Scintillators
- Tracking for high energy and nuclear physics
- Nuclear Safeguards and Disarmament Technology
- Posters
- Scintillation Detectors
- Solid State Devices
- Particle ID in High Energy and Nuclear Physics

MEDICAL IMAGING CONFERENCE

- Instrumentation/Detectors
- Image Reconstruction
- Modeling & Data Analysis
- Poster session
- MRI, CT, Ultrasound
- Scatter and Attenuation Correction

Natančnejše informacije in tudi pregled sprejetih člankov s povzetki si lahko ogledate na internetu na strani: **http://zebu.uoregon.edu/-nss97**

Zaradi zelo velike udeležbe je konferenca koncipirana tako, da poteka več sekcij vzporedno. To pomeni, da si je za vsak dan posebej potrebno pripraviti natančen izbor najzanimivejših referatov in sekcij. Mene je zanimalo vse, kar se tiče načrtovanja, izdelave in uporabe silicijevih detektorjev radiacije. To področje je zelo široko, saj se silicijeve detektorje uporablja tako za odkrivanje visokoenergijskih delcev, nizko-energijskih alfa delcev, X-žarkov ter vidne svetlobe v primeru uporabe scintilatorjev. Kljub pospešenim raziskavam na drugih materialih kot je Ge, CdZnTe, GaAs in diamant, silicijevi detektorji še vedno pokrivajo najširše področje delovanja in uporabe. V okviru silicijevih detektorjev se največ uporabljajo strukture na visoko-ohmskih substratih, predvsem t.i. strip detektorji. To so v bistvu PIN diode z difundiranimi trakovi (običajno) p-tipa in omogočajo detekcijo pozicije visokoenergijskih delcev v eni smeri. Za določitev točne pozicije je potrebno vzeti dva prekrižana detektorja ali pa detektor, ki ima na nasprotni strani difundirane trakove n-tipa dopiranja. Seveda so pomembne tudi CCD strukture, predvsem zaradi možnosti združitve s scintilatorji za uporabo v radiografiji in pa plazovite (avalanche) fotodiode, ki bi lahko v primeru možnosti izdelave na večjih površinah izpodrinile ali pa vsaj bistveno zmanjšale potrebo po PMT-jih (foto-pomnoževalne cevi). Nekoliko bolj eksotične, pa vendar izredno zanimive zaradi nizke kapacitivnosti so t.i. drift diodne strukture. Praktično vse do sedaj naštete strukture delujejo na principu popolnega osiromašenja substrata, kar je potrebno za čimboljši izkoristek detektorja. Zaradi uporabe visokoohmskih substratov so potrebne zaporne napetosti za popolno osiromašenje relativno nizke, pod 100 voltov, lahko pa se bistveno zvišajo v primeru delovanja v močnem radiacijskem okolju. Take razmere se predvideva predvsem pri bodočih eksperimentih v fiziki osnovnih delcev. V delu z naslovom "Investigation of efficient termination structure for improved breakdown properties of radiation detectors" sem na konferenci predstavil drugačen način načrtovanja zaključitve detektorjev radiacije, ki omogoča visoke prebojne napetosti tudi po radiacijskih poškodbah. To delo smo v Laboratorju za elektronske elemente Fakultete za elektrotehniko opravili v sodelovanju s sodelavci iz Odseka za eksperimentalno fiziko delcev (F9) na Inštitutu Jožef Stefan.

Konferenca je bila zelo dobro organizirana, z vrsto spremljajočih srečanj, plenarnih predavanj, kratkih tečajev (short courses) itd. Posebno odobravanje je požela soba z računalniki, navadnimi terminali in nekaj Mac-i, kjer si lahko kadarkoli pogledal in poslal elektronsko pošto (ideja za naslednjo MIDEM konferenco?!).

Nekoliko manj navdušenja je bilo nad samo lokacijo konference. Albuquerque je mesto s približno toliko prebivalci kot Ljubljana, ki pa jih je videti le podnevi, ko se vsi več ali manj ob istem času vsujejo v junk-food lokalčke. Ko pa se spusti tema, Albuquerque postane mesto duhov. Sprehajalcev praktično ni, kar pomeni, da si brez avta nemočen. V centru mesta ni možno kupiti praktično ničesar, niti kosa kruha ne, vsi shopping-centri so daleč na periferiji mesta. Zvečer na ulicah ostanejo le berači, postopači, odvisniki, zadrogiranci in podobne združbe, s katerimi je bolje ne imeti opravka. Slab vtis popolnoma nezanimivega centra mesta (downtown) nekoliko omili stari del mesta (old town), ki je od centra oddaljen eno miljo. Sestavljajo ga prijetne nizke stavbe v starem adobe stilu, praktično vse spremenjene v prodajalne spominkov in "restavracije". Za opevano lepoto New Mexica se je potrebno odpeljati ven iz mesta, v vasice domorodnih Indijancev (Pueblos), ki so dejansko zanimive. Obisk katere od teh vasic sem želel opraviti po koncu konference, pa mi je to žal vreme onemogočilo. Cel teden konference so bile temperature za tisto okolje zelo nizke zaradi prodora hladnega zraka iz severa (tako imenovani El Nino). Za nameček je za konec tedna začelo snežiti, kar je nevajene voznike popolnoma presenetilo in praktično omrtvilo celoten promet. Obisk konference je bil torej strokovno uspešen sicer pa le delno.

Kogar zanimajo članki, objavljeni v zborniku konference, pa tole: zbornik in CD bosta poslana udeležencem naknadno in bosta na voljo pri avtorju tega prispevka.

dr. Dejan Križaj
Fakulteta za elektrotehniko
Laboratorij za elektronske elemente Tržaška 25
1000 Ljubljana
(dejank@fe.uni-lj.si)

SODOBNA ELEKTRONIKA 1997

Zahvaljujemo se Vam za udeležbo na sejmu SODOBNA ELEKTRONIKA´97, v Ljubljani, od 6. do 10.10.1997. Sejem smo zaključili s pričakovanim uspehom in upamo, da ste na njem uresničili svoje načrte tudi sami. Dovolite, da Vam predstavimo nekatere bistvene podatke iz statistike sejma in rezultate ankete med razstavljalci in obiskovalci.

Med 540 podjetji, ki so bila predstavljena na sejmu, je bilo 262 prisotnih neposredno, in sicer iz 10 držav, 325 pa je bilo zastopanih iz skupno 22 držav. Tujih neposrednih razstavljalcev je bilo 56, največ iz Avstrije (16), Švice (15), Hrvaške (9) in Nemčije (9), iz Italije (2), Vel. Britanije (2), po eden pa iz Madžarske, Finske in Francije.. Med zastopanimi podjetji jih je največ iz Nemčije (74), ZDA (62), Vel. Britanije (22), Italije (22) in Avstrije (21), Japonske (19). V razstavnem programu je največ komponent (26%), avtomatizacije (18%), telekomunikacij (17%), opreme za proizvodnjo (8%), merilne elektronike (6%), radiodifuzije (5%) in audio video elektronike (2%). Zasedeno je bilo 8000 m^2 neto razstavnih površin.

Sejem si je ogledalo po naši oceni okoli 31.000 ljudi (število prodanih vstopnic po mednarodni reviziji FKM znaša 26.841). Struktura obiskovalcev je še nekoliko boljša kot lani, saj je že vsak četrti obiskovalec registriran s poslovnim kuponom. Anketa je letos pokazala, da se 34% obiskovalcev na sejmu odloča o nakupu. Večina (63%) obiskuje sejem vsako leto.

Večina razstavljalcev je registrirala tudi tuje obiskovalce (86%), sicer največ iz Hrvaške (79%), Avstrije (36%) in Nemčije (36%), Italije (30%) ter Bosne in Hercegovine (32%). Opazen je ponovno večji obisk iz ZRJ, ki ga je potrdilo 18%, razstavljalcev iz Makedonije pa 13%. V celoti je anketa potrdila obiskovalce iz 20 evropskih držav ter ZDA, Japonske, Koreje in Tajvana. Le 5% razstavljalcev meni, da struktura obiskovalcev ni ustrezna in le 2% ocenjuje svoj nastop kot neuspešen. Kar 68% razstavljalcev je v anketi že napovedalo udeležbo tudi na naslednjem sejmu elektronike v Ljubljani.

Večina anketiranih razstavljalcev želi, da sejem vsako leto spremlja tudi mednarodni simpozij. Z zadovoljstvom Vas zato lahko obvestimo, da je v letu 1998 ponovno na sporedu VITEL - Mednarodni simpozij o telekomunikacijah (5. - 6. oktober).

Podrobnejši podatki iz statistike sejma in anket so Vam na voljo pri projektnemu vodji sejma.

Vabimo Vas, da nam posredujete Vaše pripombe in predloge tudi med letom, do prihodnjega sejma SODOBNE ELEKTRONIKE, ki bo ponovno na sporedu

od 5. do 9. oktobra 1998

V pričakovanju še nadaljnega uspešnega sodelovanja Vas lepo pozdravljamo.

Ljubljanski sejem d.d. Ljubljana fair
Dunajska 10, p.p. 3558
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tel. +386/61/173 53 31
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+386/61/131 71 01

IMAPS CHAPTER CHARTER

Granted to the

Slovenia Chapter

On application duly received and accepted this date by the Executive Council of the International Microelectronics And Packaging Society.

James R. Kelly
PRESIDENT

October 13, 1997
DATE

FOUNDING MEMBERS

Darko Belavic
Marko Hrovat
Marija Kosec

INTERNATIONAL MICROELECTRONICS AND PACKAGING SOCIETY

VESTI - NEWS

CMP introducing .25 μ CMOS for prototyping at Education/Research Institutions

In cooperation with SGS-Thomson Microelectronics, CMP is introducing a high performance deep submicron .25 μ CMOS process from SGS-Thomson (Crolles).

The HCMOS7 process has the following features:

- Gate length (0.25 μ drawn, 0.2 μ effective).
- Shallow trench isolation process.
- Up to 6 levels metal layers with fully stackable contacts and vias.
- Power supply: 2.5 V.
- Threshold voltage: VTN = 0.5 V, VTP = - 0.5 V.
- I_{on}: TN @ 2.5 V : 600 μA/μm
- I_{on}: TP @ 2.5 V : 300 μA/μm

Design kits are supported under Cadence, Synopsys and Eldo.

Full custom designs are supported using Virtuoso layout editor and LAS synthesizer. The layout verifications (DRC, ERC, extraction, LVS) are fully supported for Diva and Dracula. Transistorlevel simulations are only supported under Eldo Level 59.

Standard-cell designs are supported using Verilog/VHDL descriptions for synthesis and simulation. Synthesis is supported under Synergy or Synopsys. Simulation is supported under Verilog-XL, Leapfrog and VSS. The automatic place & route is supported under Cell3.

The current supported CAD software versions are:

Cadence/OPUS	*version 4.3.4.50.106*
Cadence/Dracula	*version 4.3.0996*
Eldo	*version 4.4.1*

This process is available for prototyping to Education Institutions and Research Laboratories, on a cooperation basis. No commercial designs are accepted at this early stage. It is expected that later on, the process will be available on a commercial basis for small volume production to Education Institutions, Research Laboratories and specified Companies. A .18 μ process would then be made available for Education and Research.

CMP is the first prototyping/small volume production service to introduce a .25 μ CMOS process, ahead of any other service available in the U.S. or in Europe. CMP consolidates its leadership: CMP has been a pioneer to start serving Education and Research Institutions for NMOS IC prototyping in 1981. CMP introduced then CMOS and BiCMOS, and later MESFET and HEMT GaAs. The most recent developments are on small volume production and micromachining.

Small volume production has been strongly expanding during the last years, mostly for the benefit of Small and Medium sized enterprises:

- small volume in 1993: 3 circuits
- small volume in 1994: 12 circuits
- small volume in 1995: 24 circuits
- small volume in 1996 : 39 circuits

Also, the number of prototypes manufactured yearly is steadily increasing (about 20 %).

On MEMS (micro-electromechanical systems), CMP was the first non-US service to introduce MEMS prototyping in 1995. In addition, CMP and MENTOR GRAPHICS have together introduced the first industrially supported MEMS engineering kit ensuring a continuous design flow from front-end to back-end.

Contact: B. COURTOIS, Tel: +33 4 76 57 4615

CMP is a broker for a number of technologies (prototyping and low volume production).

- ***Integrated circuits***
  - 0.7 μ CMOS DLM from ATMEL-ES2
  - 1.2 μ, 0.8 μ, 0.6 μ CMOS DLP/DLM from AMS
  - 1.2 μ, 0.8 μ BiCMOS DLP/DLM from AMS
  - 0.6 μ GaAs MESFET from VITESSE (0.4 μ starting Q2 1998)
  - 0.2 μ GaAs HEMT from PHILIPS (up to 90 Ghz)
- ***Micromachining***
  - 1.2 μ CMOS DLP/DLM from AMS, compatible front-side bulk micromachining
  - 0.2 μ GaAs HEMT from PHILIPS, compatible front-side bulk micromachining
  - Diffractive Optical Elements (DOE) from CSEM

Design kits are available for MENTOR GRAPHICS and CADENCE.

- ***CAD software:***
  CADENCE, COMPASS, MENTOR GRAPHICS, VIEWLOGIC, TANNER,... .
- ***MCM and 3D packaging***
  - MCM-L from BULL, Les Clayes-Sous-Bois, France.

- MCM-C from DASSAULT ELECTRONIQUE, Saint Quentin en Yvelines, France.
- MCM-C/HTCC from Montpellier Technologies-IBM, Montpellier, France.
- MCM-D from Thomson-CSF Microelectronique, Massy, France.
- MCM-V (3-D packaging) from 3D-Plus, Buc, France.

- ***Design kits:***
  available for most of the processes from:

ALLIANCE
DOLPHIN
MAGIC
MENTOR GRAPHICS
CADENCE
EXEMPLAR
MDS
SYNOPSYS
COMPASS
TANNER
VIEWLOGIC

Circuits Multi-Projects
46 avenue Felix Viallet
38031 Grenoble Cedex
France
Tel. : +33 4 76 57 45 00
Fax : +33 4 76 47 38 14
E.mail: cmp@archi.imag.fr
WWW: http://tima-cmp.imag.fr

News from AMS

New Single Chip 2 Wire Intercom IC

Austria Mikro Systeme announces the introduction of a new single chip CMOS integrated circuit - the AS2507 - for application in 2-wire intercom networks. The device incorporates 2/4 wire conversion (hybrid), soft clipping for high speech quality, FSK signalling and a simple interface to a microcontroller.

Key features include:

- Only 2 wires are needed for the power supply, for signalling and speech;
- Low standby power consumption **allows parallel operation of all terminals on one bus pair**;
- Soft clipping, side tone cancellation, low noise - excellent quality;
- Very few external components required.

The signalling mode can be adjusted to select between FSK modulation and burst mode. The low standby current of typically 1 mA allows several devices to listen to the 2-wire line. The speech circuit is designed for compatibility with commonly used handsets (150 ohm ear piece and electret microphone) with a receive gain of -6 dB and a transmit gain of 32 dB relative to the line.

The AS2507 is available in 14 pin DIP and 16 pin SOICw packages. Samples and production quantities are available now. For a free data sheet and further detailed information please contact your local Sales Office or

Austria Mikro Systeme Corporate Communications, A-8141 Unterpremstatten, Austria

Thesys Marketing Communications, Haarbergstrasse 61, D-99097 Erfurt, Germany

Sames Marketing Communications, P.O. Box 15888, Pretoria, Rep. of South Africa.

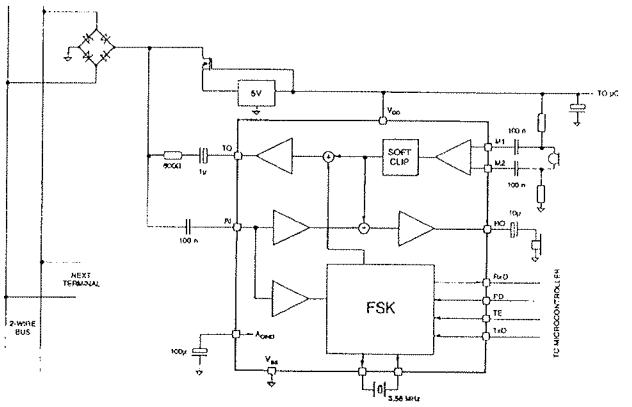
Note to the Editor: *Intercoms generally require one dedicated wire line to each separate unit mounted. With this IC only one wire pair is required for all terminals interconnected. Hence, there is virtually no limit to the number of intercoms which can be linked to one another. Intercom wiring in buildings becomes simpler and more cost effective over traditional systems and installations. To our knowledge the AS2507 provides better speech quality than in commonly used intercom systems. This is a result of nearly 1 % decades of dedication to telecommunication handset products.*

Key Features

- Line/speech circuit and signalling on one 14 pin CMOS chip
- Only 2 wires needed for power supply, signalling and speech
- Soft clipping to avoid harsh distortion
- Fully integrated 2/4 wire conversion
- Side tone cancellation
- Low noise
- Signalling with FSK modem
- Low standby power consumption allows parallel operation of up to 20 terminals on each bus pair
- Controllable via simple µC interface
- Very few extemal components

Application

Entrance telephone system, intercom, toy phone



General Description

The AS2507 is a CMOS integrated circuit that contains all the functions needed to build a 2-wire intercom network.

The device incorporates 2/4-wire conversion (hybrid), soft clipping for high speech quality, FSK modem and a simple interface to a microcontroller.

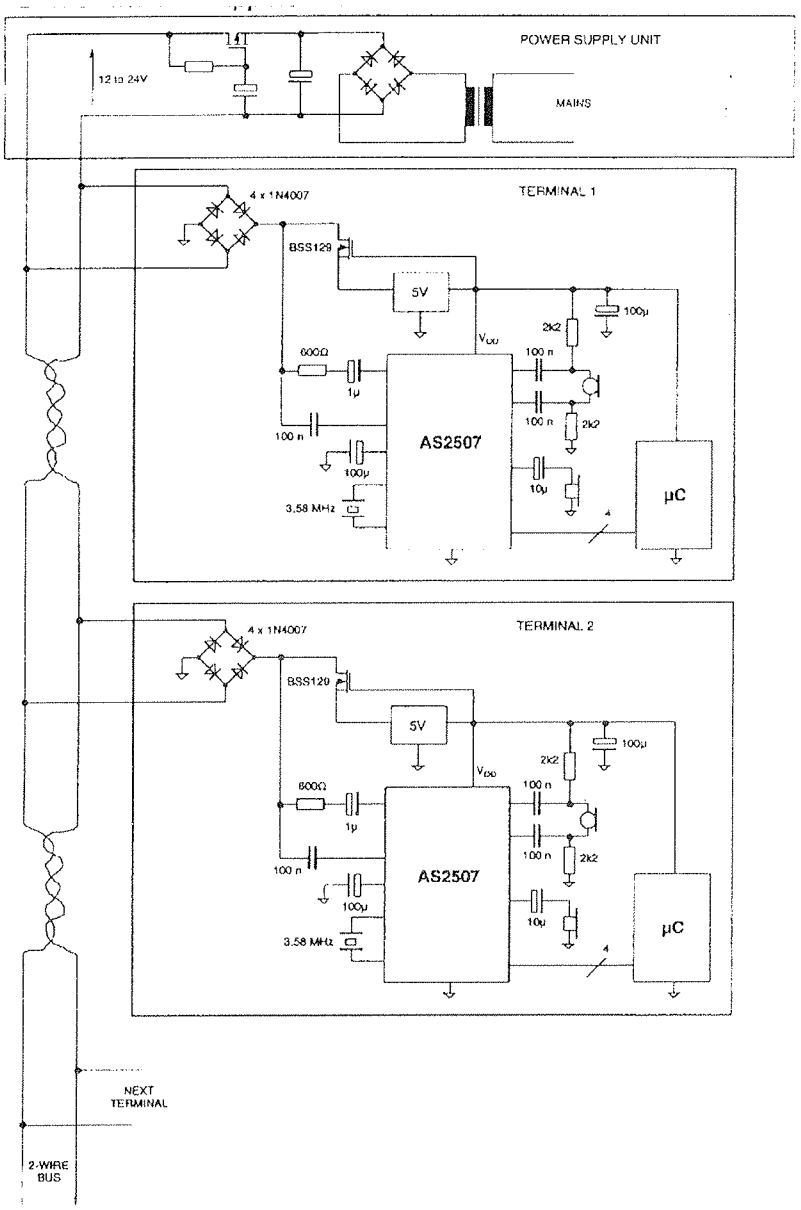
The signalling mode is selectable between FSK modulation and burst mode.

The low standby current (typ. 2 mA) allows several devices to listen to the 2-wire line.

The speech circuit is designed for compatibility with commonly used handset (150 ohm earpiece and electret microphone) with receive gain of -6 dB and transmit gain of 32 dB (relative to line).

Package

Available in 14 pin DIP and 16 pin SOICw.



Extended Foundry Services

To meet the increasing demand for customer ASIC designs to be completed and to be manufactured even more quickly, the Austria Mikro Systeme Group now offers extended foundry services at attractive pricing.

The advantages of the Group´s foundry capabilities for the customer are:

- thorough design support with most comprehensive documentation and informal access to technical assistance
- most reliable device models
- an even wider choice of CMOS and BiCMOS process technologies to choose from: high voltage, low voltage, mixed signal and EEPROM processes from 0.6 to 1.2 micron
- more affordable sample and prototyping services
- shorter mask, fab and packaging cycles

The Group also provides unique *multi-product wafer capabilities* and *multi-level* mask services. By splitting wafer and mask costs among several projects, significant savings can be passed on to the customer.

All stages of manufacturing can be completed under one roof - R & D, design, mask lithography, wafer fabrication, assembly and test which allow for most competitive lead times for processing and highest quality. The products of the customer can be manufactured at any of the three locations of the Group:

- Thesys in Erfurt, Germany
- Austria Mikro Systeme in Austria, with more than one decade of focused customer support experience
- SAMES in Pretoria, South Africa.

Whatever the design resource, interface and experience of the customer the Group has the flexibility to quickly deliver the ASIC product the customer needs.

This text is available *on the Internet* Address: *http://www vertical-global.com*

sames

opens new international design centre

SAMES, South African Micro-Electronic Systems (Pty) Ltd, a joint venture between the IDC (Industrial Development Corporation) of South Africa and Austria Mikro Systeme International AG, Austria announce the opening of their new design centre for integrated circuits at the Centurion Technopark located between Pretoria and Johannesburg (close to SAMES headquarters).

A total of 30 top international and South African design specialists provide ASIC solutions at the new site with over 600 square meters office area, equipped with state-of-the-art hardware and software platforms allowing for a total of 60,000 engineering man-hours annually. As a result the SAMES design centre will more than double its capacity for mixed signal/analogue product development.

The new design centre is directly linked into the Group´s international design centres in Unterpremstätten - Austria, Erfurt and Dresden in Germany and Budapest in Hungary. The world wide network structure of the Group secures the exchange of data and experience for customer on-line.

As a member of the Austria Mikro Systeme Group, together with Thesys, the major strategic focus was to change from contract manufacturing dependency to ASIC (application specific integrated circuits) specialisation. This is also consistent with the Group stratgy to further globalize its operations and use innovative talent wherever it is available.

The major market segments addresed by SAMES are in the areas of energy measurement, telephony, ID and security and general analogue mixed signal ASICs.

The SAMES designers will have access to a comprehensive range of technologies ranging from 0.6 micron to 2.0 micron, featuring EEPROM, low voltage, high voltage capabilities in CMOS and BiCMOS processes which can be produced in any of the Group´s manufacturing facilities.

The design centre was opened today by the Minister of Arts, Culture, Science and Technology emphasising the importance placed by the South African government on information technology.

News from Advanced Packaging

Nov/Dec 1997

IMAPS 30th Anniversary Celebration

The International Microelectronic And Packaging Society (IMAPS) unveiled its new logo last October to a packed Philadelphia audience at the annual IMAPS symposium and exhibition. Sponsored by both IMAPS and the American Ceramics Society (ACerS), the show consumed a hearty chunk of the new Pennsylvania Convention Center and resulted in record numbers of attendees (5,500 attendees - a 35 percent increase over last year's show), exhibitors and course attendees (professional development course registration was up 20 percent to 500 people).

Marking the beginning of the event was the annual keynote luncheon, which highlighted remarks from past, present and future presidents, as well as a speech from Dr. Joseph Bordogna of the National Science Foundation. The "four horsemen" of ISHM, Harry Charles, Kinzy Jones, Richard Breck and Jim Drehle, were also awarded ruby-studded society pins for their past efforts and self sacrifice in preserving the financial health of the society. Other awards included the Hughes Memorial Award, given *to Advanced Packaging* advisory board member R. Wayne Johnson, the Wagnon Technical Achievement Award given to Kashmir Mittal, and the Corporate Recognition Award granted to Motorola Ceramic Products.

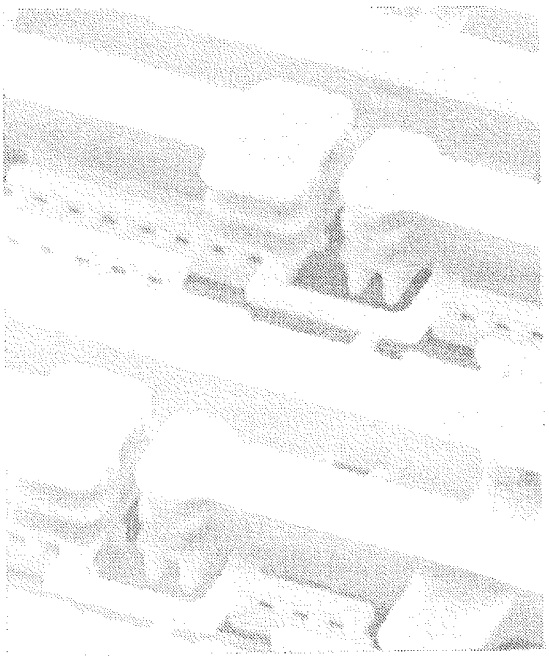
One highlight of the festivities included the introduction of Phil Garrou, who will serve as first president of the new IMAPS society. A 12-year veteran of ISHM and Chief Scientist of Microelectronic Packaging at The Dow Chemical Company, Garrou has definite plans on where he would like to take the society over the coming year. He first emphasized his intent to continue and further the globalization efforts set in place over the past year, appointing Rao Tummala as the VP of International Development to aid in these efforts. Referencing ISHM´s previous progress in bringing microelectronics to China, India, Brazil and **Slovenia**, Garrou added that "The goal is to get in while the microelectronics industry is in its infancy and establish "beachheads" there. We want to get traffic started before companies start to move in."

Garrou's second goal as president of the society is to broaden IMAPS' technical horizon to cover everything from back-end packaging through systems design. Though he hastily admits that there are already too many industry conferences to choose from, Phil aims to help broaden the scope of their technical offerings by partnering with other industry societies to host advanced technology conferences. "If a new technology comes into play, we'll address it," he assures. "But we're approaching /other/ societies up front to see if they're willing to do a joint effort." Phil Garrou's third and perhaps most revolutionary goal is his emphasis on information transfer - an area that called for the appointment of Wayne Johnson as the new VP of Information Dissemination. "We are part of a microelectronics professional society, and I feel it is incumbent on us to make information available to our membership in the latest ways possible." In addition to providing conference materials on CD-ROM and maintaining their existing arsenal of publications and journals, IMAPS has plans for a new website to be located at www.imaps.org. Bringing their server from its former home at Virginia Tech to society headquarters and fashioning a new web page will allow the society to provide members with access to technical papers, industry links and member information at the click of a mouse. "There are more clever ways to access information," finished Garrou, "and we want to provide that as IMAPS."

News from European Semiconductor

Nov. 97

IBM´s copper exposed



In the isometric of IBM's recently announced SA-27 ASIC process pictured above, three of the six levels of copper interconnects are clearly revealed above the (pale coloured) tungsten plugs and (metal-0) local interconnect. (L_{drawn} = 0.16 μm, $L_{effective}$ = 0.12 μm.)

At the International Electron Devices Meeting in Washington DC next month both IBM and Motorola will be giving presentations on their respective sub 0.25 μm six-level dual-inlaid copper technology.

Also at the meeting, Texas Instruments will be presenting what is claimed to be the first integration of damascenecopper and and ultra-low dielectric constant xerogel. The porosity of the xerogel was tuned to approximately 75% for a dielectric constant of 1.8 and an optional oxide sidewall formed in the trenches etched in the xerogel. For copper deposition, a PVD Ti/TiN barrier layer preceded a PVD copper seed layer before electroplated copper trench fill and CMP Resistance of the copper/xerogel is 28-30% less than aluminium while the calculated capacitance for an aluminium/oxide structure with the same resistance as the copper/xerogel structure would be 29% higher.

French defence

The French defence industry is to be consolidated around Thomson-CSF under government plans. Alcatel Alsthom will have a leading role in the new national defence group which will also include Dassault electronics and Aerospatiale satellites.

The government will retain a 45% stake but Alcatel's chair, Serge Tchuruk, is expected to have a big influence in the company. The move is seen as making flotation of at least part of GEC-Alsthom (jointly owned by Alcatel and GEC) more likely.

GEC welcomed the French consolidation plans but an international consortium led by Largardere and supported by Dasa and British Aerospace that had hoped to buy control of Thomson expressed disappointment.

Patent jukebox

IBM is working with the Netherlands Industrial Property Office on a project to store and access patents on CD jukeboxes linked to the internet. Four out of 25 of its patent collections currently on CD-ROM are to be put on the system - representing 6000 disks with 4 Tbytes of information. The first phase will grant access to NIPO staff and library users on-site. The next phases will open the system to Dutch innovation centres and universities and finally all interested Dutch end-users.

PFC removal

Air Liquide has received "Scientific American's" R&D innovation award for work on recycling gases containing fluorine such as the perchlorofluorocarbons (PFCs) used in semiconductor production. PFCs contribute to ozone layer depletion and the greenhouse effect. The process was developed by two Air Liquide research teams at its US Chicago research centre. It enables such gases to be captured and purified for total recycling.

Applied Materials has introduced a zero-consumables chamber cleaning process to virtually eliminate PFC emissions from its dielectric CVD processes. The "remote plasma clean" process converts source gas into active atoms in a plasma upstream from the chamber. The neutral atoms move to the process chamber where they selectively remove surface material but do not attack metallic or ceramic parts. The process is part of Applied's "Green Initiative" programme. Applied says that for critical applications like shallow trench isolation the process lowers metallic contamination, improves film quality and increases device yield.

KOLEDAR PRIREDITEV

MARCH

02.03. - 08.03.1998
Cleanrooms '98 East
Baltimore, MD, USA
Info.: + 603/891-9267

17.03. -19.03.1998
NEPCON UK
Birmingham, UK
Info.: + 171/ 837 8727

23.03. - 27.03.1998
1998 International Conference on Characterization and Metrology for ULSI Technology
Gaithersburg, MD, USA
Info.: + 301/975-2054

31.03. - 02.04.1998
SEMICON Europe
Geneva, Switzerlamd
Info.: + 171/ 837 8727

APRIL

18.04. - 23.04.1998
41th Annual Technical Conference
Society of Vaccum Coaters
Boston, MA, USA
Info.: + 505/ 856 7188

20.04. - 22.04.1998
Expo Electronica'98
Moscow, Russia
Info.: + 1787 / 37 2345

22.04. - 23.04.1998
SEMICON China 98
Shanghai, China
Info.: + 650 / 940 6943

27.04. - 30.04.1998
1998 International Conference on Gallium Arsenide Manufacturing Technology
Seattle, WA, USA
Info.: + 972/ 995 6978

28.04. - 30.04.1998
Control and Instrumentation
Birmigham, UK
Info.: + 171/ 837 8727

MAY

04.05. - 05.05.1998
Metrology for Electronic Packaging and Interconnection
Gaithersburg, MD, USA
Info.: +301/975 6741

04.05. - 05.05.1998
SEMICON '98 Singapore
Singapore
Info.: www.semi.org

18.05. - 22.05.1998
MIPRO '98
Opatija, Croatia
Info.: + 1/612 9936

19.05. - 20.05.1998
4th Annual IPC/SMTA Ball Grid Array National Symposium
Minneapollis, MN, USA
Info.: + 847/ 509 9700

26.05. - 27.05.1998
4th International Workshop on Advanced Plasma Tools and Process Engineering
Millbrae, CA, USA
Info.: + 408/737 2403

JUNE

03.06. - 05.06.1998
Third International Symposium on Plasma Process-Induced Damage (P2ID 98)
Honolulu , Hawai, USA
Info.: + 408/737 0767

24.06. - 26.06.1998
3rd European Workshop on Low-Temperature Electronics
San Miniato, Tuscany, Italy
Info.: fax + 39/2 2392 624

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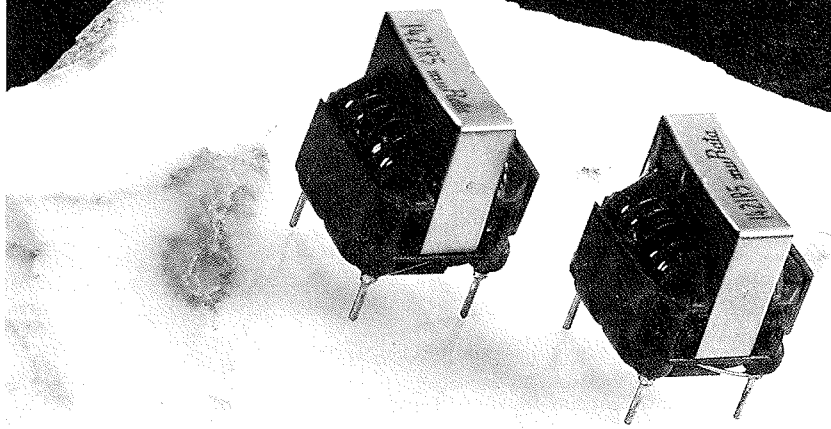

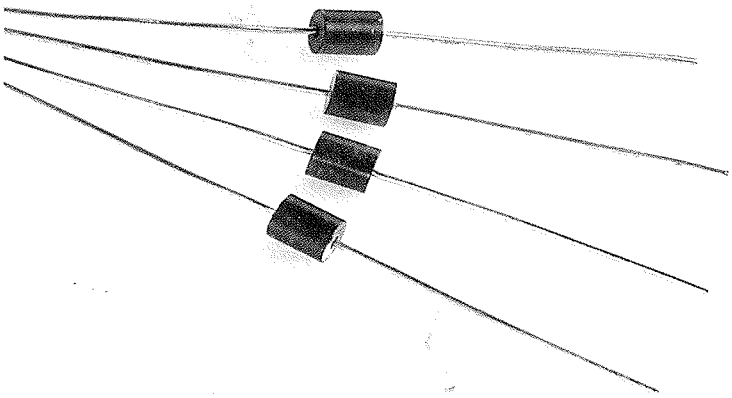

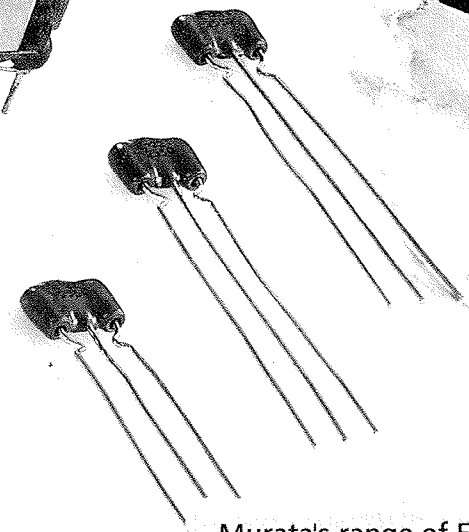

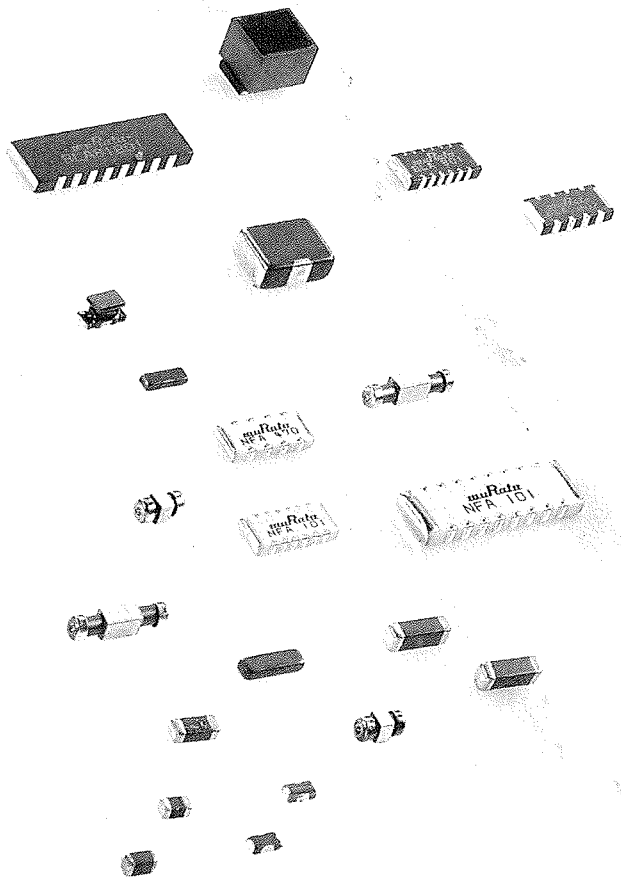

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