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# ELECTROMAGNETIC COMPATIBILITY IN INTEGRATED CIRCUITS: A REVIEW

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**Key words:** electromagnetic compatibility, electromagnetic interference, measurement methods, measurement setup.

**Abstract:** Electromagnetic compatibility (EMC) studies the unintentional generation, propagation and reception of electromagnetic energy with reference to the unwanted effects. Its goal is to avoid any interference between different equipment, which uses electromagnetic phenomena, in the same electromagnetic environment. This paper is focused on EMC of integrated circuits (ICs) and presents a review of EMC history, IEC standards for EMC in ICs, measurement methods and measurement setups.

# Elektromagnetna združljivost v integriranih vezjih: pregled

**Kjučne besede:** elektromagnetna združljivost, elektromagnetna interferenca, merilne metode, merilni sistemi.

**Izvleček:** Elektromagnetna združljivost preučuje nenamerno generiranje, prenašanje in dovzetnost elektromagnetne energije v odnosu z neželenimi efekti. Njen cilj je izogniti se interferencam med različnimi napravami, ki delujejo na elektromagnetnem pojavu, v skupnem elektromagnetnem okolju. Članek je osredotočen na elektromagnetno združljivost v integriranih vezjih in obravnava pregled zgodovine elektromagnetne združljivosti, IEC standarde za elektromagnetno združljivost v integriranih vezjih, merilne metode in merilne sisteme.

## 1. Introduction

Electromagnetic compatibility is the branch of electrical sciences which studies the unintentional generation, propagation and reception of electromagnetic energy with reference to the unwanted effects (Electromagnetic Interference or EMI) that such energy may induce. The goal of EMC is the correct operation, in the same electromagnetic environment, of different equipment which uses electromagnetic phenomena, and the avoidance of any interference effects.

In order to achieve this, EMC pursues two different kinds of issues. Emission issues are related to the unwanted generation of electromagnetic energy, and to the countermeasures which should be taken in order to reduce such generation and to avoid the escape of any remaining energies into the external environment. Susceptibility or immunity issues, in contrast, refer to the correct operation of electrical equipment in the presence of unplanned electromagnetic disturbances.

Electrostatic discharge (ESD) and latchup effect are also connected with EMC phenomena. *Latchup* may be defined as the creation of a low-impedance path between power supply rails as a result of triggering a parasitic device. In this condition, excessive current flow is possible, and a potentially destructive situation exists. After even a very short period of time in this condition, the device in which it occurs can be destroyed or weakened; and potential damage can occur to other components in the system. Latchup may be caused by a number of triggering factors including overvoltage spikes or transients, exceeding maximum ratings, and incorrect power sequencing.

ESD is the sudden and momentary electric current that flows between two objects at different electrical potentials and is a serious issue in solid state electronics. Integrated circuits are made from semiconductor materials such as silicon and insulating materials such as silicon dioxide. Either of these materials can suffer permanent damage when subjected to high voltages, as a result there are a number of antistatic devices that help prevent static build up.

Interference, or noise, mitigation and hence electromagnetic compatibility is achieved by addressing both emission and susceptibility issues, i.e., quieting the sources of interference, making the coupling path between source and victim less efficient, and making the potential victim systems less vulnerable.

## 2. A brief historical review

It started more than forty year ago, when in 1965, Gordon Moore co-founder of Intel Corporation, published his long term vision of the evolution of integrated circuit. He point out a trend in integrated circuit complexity and predicted an exponential growth in the available memory and calculation speed of microprocessors, doubling every year /1/. With minor correction (doubling every 18 months), Moore's law still holds today.

The American army was a pioneer in the field of integrated circuit EMC. In 1965 they studied the effects of the electromagnetic fields due to nuclear explosions on electronic devices used in launch missile sites. The result was simulating software SCEPTRE /2/ that was developed at IBM, for simulating the effect of nuclear radiation on electronic

components and it was used to correlate simulations and experimental measurements.

One of the earliest academic publication was the simulation of the 741 integrated operational amplifier published by Wooley in 1971 /3/. The author simulated the different stages of this IC with the simulating software CANCER (an ancestor of today's simulator SPICE).

In 1975, Whalen published studies on the radio-frequency pulse susceptibility of discrete transistors /4/. He also edited special issue about interference between electromagnetic sources in the very high frequency band (VHF 30 MHz-300 MHz), ultra high frequency band (UHF 300 MHz-3 GHz) and even extremely high frequencies with radars (EHF 3 GHz-30 GHz) /5/. Two years later in 1981 Roach characterized the sensitivity of 1 Kbyte NMOS memories /6/. Some years later, a study by Tront was published /7/. The topic of the study was about the behavior of the 8085 processor in presence of 100 and 220 MHz radiofrequency interference. By using simulation software SPICE, he reproduced some phenomena observed during measurements.

In 1990 H. Bakoglu published a book /8/ witch comprehend a summary of the parasitic effects in integrated circuits, packaging and printed circuit boards (PCB's). His book describes different problems linked to transient current consumption at active edges of the clock and detailed basic mechanisms for integrated circuit resonance. In the same year Kenneally et al. published measurement results for simple integrated circuit in CMOS and TTL technologies /9/. His results showed that the sensitivity of circuit decrease when interfered frequency (1-200 MHz) increases. He also discovered significant differences between fabrication technologies. CMOS circuits tend to be less robust than TTL circuits.

Synchronous switching noise is most significant chip-level concerns for EMC and signal integrity engineers. In 1993, R. Downing et al. published a paper with a topic on the characterization of decoupling capacitance effects including on-chip decoupling and decoupling in proximity to the integrated circuit.

The research on susceptibility of integrated circuits continued in 1995 with published paper by Laurin et al. The research focused on the effects of an electromagnetic wave coupling to PCB traces and the consequences of this coupling on simple circuit behavior /10/. The researchers observed no perturbations on the component with field strengths of 200 V/m, which is specified field strength in MIL-STD-461B. By adding long metal wire that was a half-wavelength long at the interference frequency, the field was reduced to 2 V/m. This low field caused severe malfunctions due to erroneous switching. The research also comprehends the difference between a static and transient regime. In the static regime, only perturbations with high en-

*Table 1: Standards for EMC emission, susceptibility and impulse immunity measurement of integrated circuit*

| Standard | Description | Status in 2008 |
|---|---|---|
| | | |
| IEC 62215 Measurement of impulse immunity up to 1 GHz | | |
| IEC 62215 1 | Definitions | |
| IEC 62215 2 | Synchronous transient injection method | Published in 2007 |
| IEC 62215 3 | Electrical fast transient (EFT), ESD immunity | New proposal |
| | | |
| IEC 62132 Measurement of electromagnetic immunity up to 1 GHz | | |
| IEC 62132 1 | Definitions | Published in 2006 |
| IEC 62132 2 | TEM/GTEM Cell method | Committee draft for voting |
| IEC 62132 3 | Bulk current injection (BCI) | Published in 2007 |
| IEC 62132-4 | Direct RF power injection (DPI) | Published in 2006 |
| IEC 62132-5 | Workbench Faraday cage | Published in 2005 |
| | | |
| IEC 61967 Measurement of electromagnetic emission up to 1 GHz | | |
| IEC 61967 1 | Definitions | Published in 2002 |
| IEC 61967 2 | TEM/GTEM Cell method | Published in 2005 |
| IEC 61967 3 | Surface scan method | Published in 2005 |
| IEC 61967-4-ed 1.1 | 1 Ω/150 Ω direct coupling method | Published in 2006 |
| IEC 61967 4 am1 | 1 Ω/150 Ω direct coupling method | Published in 2006 |
| IEC 61967-4-1 | 1 Ω/150 Ω direct coupling method | Published in 2005 |
| IEC 61967-5 | Workbench Faraday cage | Published in 2003 |
| IEC 61967 6 | Magnetic probe method | Published in 2002 |
| IEC 61967 6 am1 | Magnetic probe method | Published in 2008 |

ergy affected logic levels were in the transient regime, even weak perturbations could affect switching delays.

Two years later J. F. Chappel investigated and proposed a new technique that raised the immunity level of ICs from less than 1,5 V to over 5 V in the frequency range 1 to 10 MHz. Other circuits have been proposed because of their high immunity to radio frequency interference (RFI) including Schmidt triggers, low-voltage differential swing circuits and delay-insensitive structures.

In year 2000, NASA published an updated version of the handbook on EMI immunity /11/, which gave valuable information on the immunity of integrated circuits with frequency up to 10 GHz. The author presents measurement results concerning simple components and comparison with measurements taken in the 70's.

Fiori published a study of RFI effects on analog amplifier up to 2 GHz /12/. The measurement equipment involved microwave probes, positioned directly on chip, to maintain 50-ohm impedance from the measurement equipment to the integrated circuit. The author observed that DC shift of the amplifier offset increases with RFI amplitude but it remained almost constant from 100 MHz to 2 GHz.

# 3. EMC measurement methods

## 3.1. EMC Standards

A set of EMC regulations which fixed the maximum limits for parasitic emission and immunity levels for electronic devices were established in Europe in 1996. The probable result of these regulations was revived interest of the researchers and engineers for this subject.

The International Electrotechnical Commission (IEC) is one of the standard bodies that are addressing the need for standardized IC EMC measurement methods. At the component level, the most important standards were developed under the supervision of the Technical Committee 47A, which is focused on integrated circuits.

This committee prepares international standards with a focus specifically on logic circuits, memory, converters and hybrid modules.

## 3.2. Measurement of IC emission

The measurement of the conducted or radiated emissions from IC, under specified conditions, can give useful information about the potential and severity of emissions in a tested application. IEC 61967 standard defines measuring method, measurement conditions, test equipment, specific PCB requirements, consistent test procedures as well as contest of the test report.

## 3.3. Radiated emission

There are two basic methods for evaluating ICs of being the source of radiated EM emissions: TEM/GTEM cell test and near-magnetic field scan. The transverse electromagnetic mode (TEM) cell and the gigahertz TEM (GTEM) cell are commonly used for measuring EM emissions radiated by an IC, but can be also used for measuring IC immunity to EM fields. EM radiated emission measurement method by TEM/GTEM is standardized as IEC 62967-2 (Table 1). The TEM cell (Fig. 1) is an expanded rectangular waveguide with an inner conductor called the septum, whose characteristic impedance is set to 50 Ω. It is terminated by two tapered ends to connect 50 Ω - adapted coaxial cables.

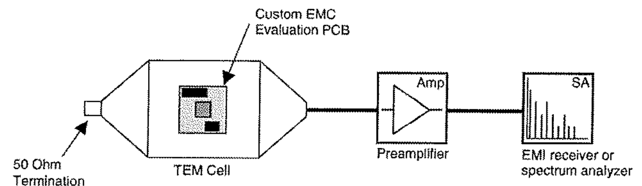


*Fig. 1: IEC 62967-2 TEM cell radiated emissions test setup /13/*

The GTEM cell (Fig. 2) was designed to overcome the TEM cell frequency limitation. It consists of a tapered section of rectangular transmission line, with an offset and sloping septum plate. The septum is tapered so that the characteristic impedance is maintained to 50 Ω along the length of the cell. The wide extremity is terminated by a distributed resistive load that operates as a 50 Ω load circuit at low frequency and by pyramidal foam absorbers that attenuate the EM wave at high frequency.

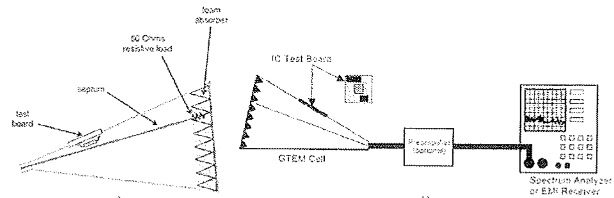


*Fig. 2: a) GTEM cell, b) IEC 62967-2 GTEM cell radiated emission test setup /14/*

Measuring the radiation from the same IC in TEM or GTEM cells can be compared using the correlation factor between two cells /14/.

The near-field scanner was introduced to the EMC problem of the IC by K. Slattery /15/. Measurement methods which determine the EM field by using RF receiver can be classified in two main techniques. The direct technique involves a coaxial cable who connects the probe to the receiver (Fig. 3).

The second technique creates a perturbation by introducing a scatterer at the desired observation point, to enhance the spatial resolution and to reduce the parasitic coupling between the probe and device under test (DUT).

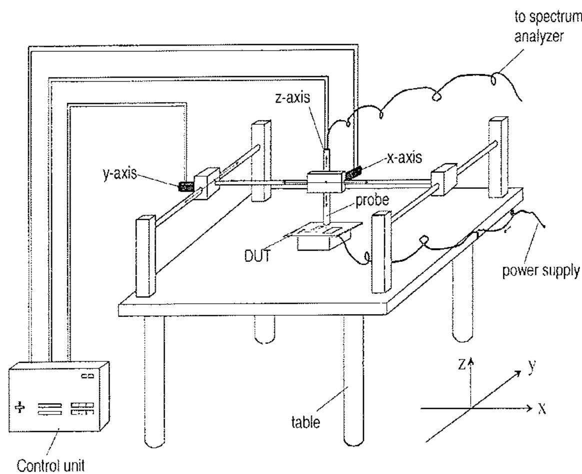


*Fig. 3: IEC 61967-3 near-field radiated emission test setup /14/*

## 3.4. Conducted emission

Another method for evaluating ICs is to measure the conducted noise currents on each pin.

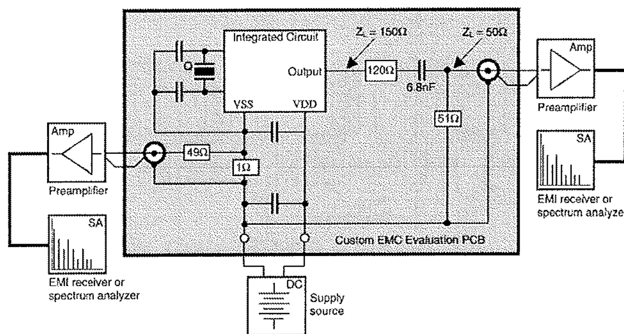


*Fig. 4: IEC 61967-4 conducted emission test setup /14/*

IEC 61967-4 defines a method of determining an IC's conducted electromagnetic emissions by measuring the RF voltage developed across a standardized load as shown in Fig. 4. For high power ICs, the 1 Ω probe is replaced by a 0.1 Ω resistance, or split among the return current paths /14/.

The Workbench Faraday Cage (WBFC) method is used for conducted emission measurements. IEC 61967-5 defines a method of measuring the conducted electromagnetic emissions at defined common-mode points in order to estimate the emissions radiated by connected cables in an application /16/. A schematic of the test setup are shown in Fig. 5.

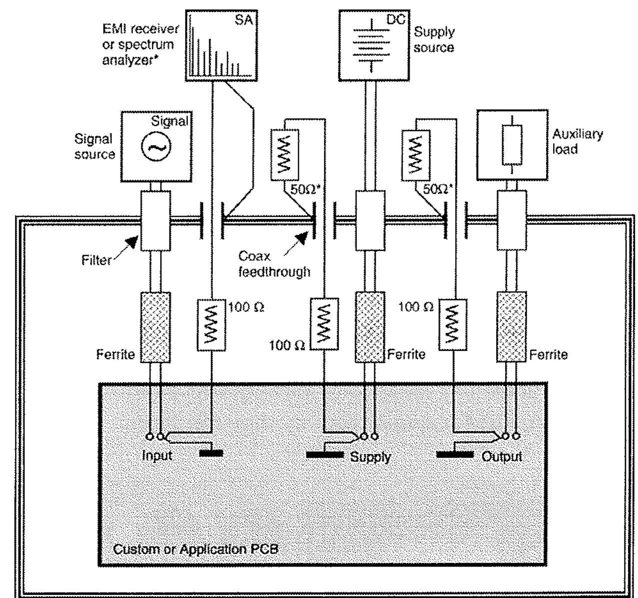


*Fig. 5: IEC 61967-5 WBFC conducted emission test setup /13/*

The method will apply for those cases where the wires and cables connected to the sources and victims are much longer than the largest dimension of the integrated circuit.

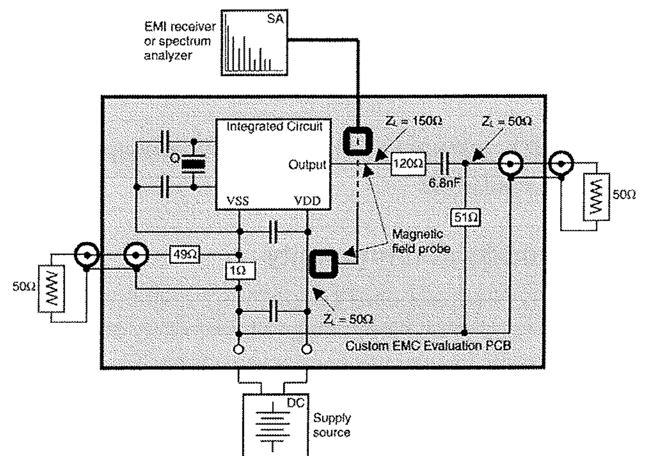


*Fig. 6: IEC 61967-6 conducted emission test setup /13/*

IEC 61967-6 is defines a method of calculating the conducted electromagnetic emissions from an IC pin by using a magnetic field probe to measure the magnetic field associated with a connected PCB trace /16/. A diagram of the test setup is shown in Fig. 6. The preferred test configuration is with the DUT mounted on an IC EMC test board with standardized layout patterns to maximize repeatability and minimize probe coupling to other circuits. With care, this method can also be applied to application boards.

## 3.5. Measurement of IC immunity/ susceptibility

As for emissions, the assessment the conducted or radiated immunity performance of an IC, under controlled conditions, can yield useful information about the potential and severity of RF immunity in an application. The test methods in IEC 62132 standard utilize a continuous wave signal, either modulated or unmodulated. The required mod-

ulation, if any, is specified in the individual test method. This standard consists of five parts: a general guidance document and four immunity test methods /17/.

## 3.6. Radiated immunity

The TEM/GTEM cell can be used also as immunity tests setup. Test setup is similar to emissions setup only that EMI analyzer and pre-amplifier are exchanged with signal generator and power amplifier. DUT is tested in at least two orientations to ensure complete exposure to the generated electric field. Signal generator generates signal, which is amplified to achieve strength of electric field in the TEM/GTEM cell specified by the standard.

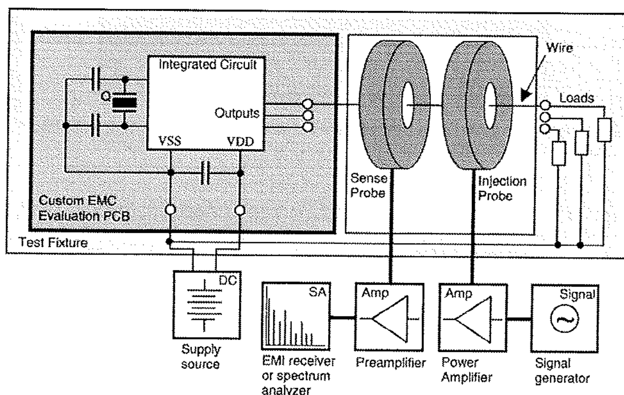


*Fig. 7: IEC 62132-3 BCI conducted immunity test setup /13/*

## 3.7. Conducted immunity

IEC 62132-3 is a standard that defines a method of evaluating the conducted electromagnetic immunity of an IC to noise currents injected on connected cables (Fig. 7). This method is based on bulk current injection (BCI) methods used for equipments and systems such as ISO 11452-4. The intent of this method is to evaluate the immunity of IC pins connected to cables. The injection coil induces by magnetic coupling a current (usually up to 100 mA) that may produce faults on the DUT at particular frequencies. The faulty state is recognized by a real-time monitoring of the device activity.

Direct power injection (DPI) method (Fig. 8) evaluates the immunity of IC pins connected to cables. The immunity signal is directly injected (capacitively coupled) onto the conducted conductor (cable, trace, etc.) instead of being inductively coupled to the cable or cable bundle. Signals issued from the DUT are analyzed in real-time by special oscilloscopes that alter the control software in case of abnormal waveform.

Other susceptibility measurement method for evaluating the conducted immunity of an IC to noise signals injected at defined common-mode points in order to simulate exposure to any connected cables to the radiated electromagnetic environment in an application is workbench fara-

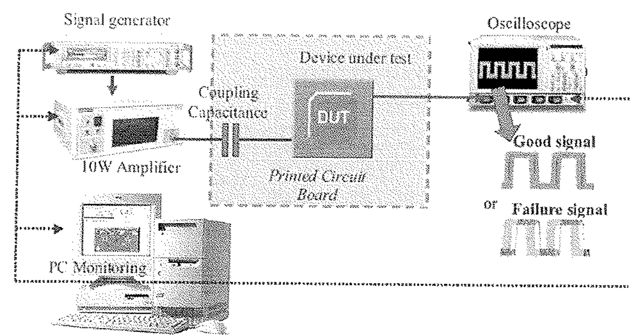


*Fig. 8: IEC 62132-4 DPI conducted immunity test setup /18/*

day cage method (IEC 62132-5) (Fig. 9). The DUT is mounted on either IC EMC test board or an application board subject to the size limitations of the WBFC. With all input, output and power connections to the test board filtered and connected to common-mode chokes, the conducted noise is injected at PCB locations specified by the standard.

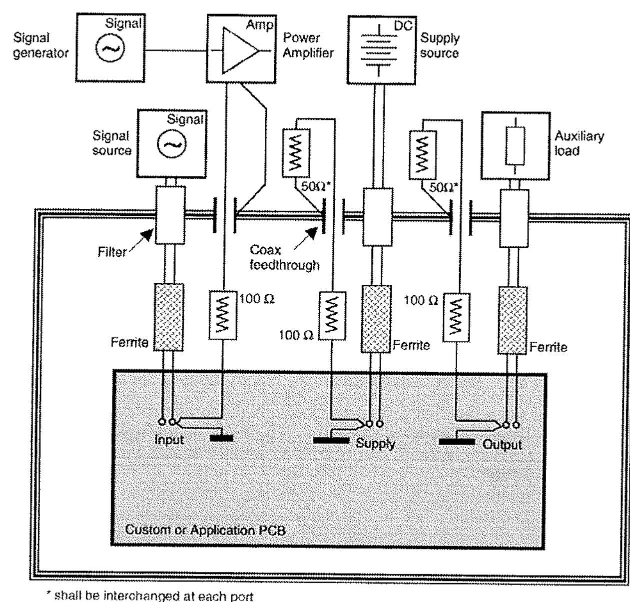


*Fig. 9: IEC 62132-5 WBFC conducted immunity test setup /13/*

## 3.8. Impulse immunity

A reason for investigating the IC immunity to impulse waveforms is that the impulse immunity tends to decrease with newer technology, as observed by researchers /19/. Reasons might be the decreased noise margins, the clock frequency increase or the increase of IC complexity /18/.

A new standard (IEC 62215) is under discussion to establish measurement techniques for measuring impulse immunity of ICs. Most of the documents are at the status of new proposals, as shown in Table 1 /20/.

## 4. Conclusions

This paper has presented some important aspects of EMC in ICs and its history. While the EMC evaluation of ICs is still in development, international standardized methods (IEC 61967, IEC 62132 and IEC 62215) are available for use. A comprehensive set of standardized IC EMC test methods with application has been presented. As it is shown in table 1, standards for radiated/conducted emissions and immunity has been developed and published by IEC in recently. In the future, focus will be on transient immunity evaluation, which is still in its infancy.

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