THE PRINCIPLE OF NEW SIGMA DELTA MODULATION TECHNIQUE BASED UPON THE USE OF A FLIP-FLOP

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Key words: sigma delta modulation, flip-flop, capacitive accelerometers

Abstract: This paper describes a new sigma delta modulation technique. This technique is used for measurement of changes in half capacitive bridge to detect deflections, which can result from acceleration input in practice. The half bridge is connected to a modified flip-flop circuit, the outputs of which are used for one-bit force feedback. The modification of flip-flop consists in the implementation of a switched capacitor structure to achieve a perfect flip-flop value symmetry and compensation of a flicker noise. Some theoretical considerations are verified by experimental results. An experimental circuit has been constructed from discrete elements.

Osnove nove sigma-delta tehnike modulacije na osnovi uporabe flip-flopa

Kjučne besede: sigma-delta modulacija, flip-flop, kapacitivni merilniki pospeška

Izvleček: V prispevku opisujemo novo sigma-delta tehniko modulacije. Uporabljamo jo pri meritvi spremembe kapacitivnosti na mostičku namenjenemu zaznavanju odmikov pri pospeševanjih. Mostiček je priklopljen na flip-flop vezje, katerega izhode uporabljamo za povratno vezavo na mostiček. Mostičku je dodana struktura stikalnega kondenzatorja, s pomočjo katerega dosežemo popolno simetrijo izhoda flip-flopa in kompenziramo šum. Nekatere teoretične predpostavke smo preverili s preiskusi. Preizkusno vezje smo izdeleli z diskretnimi elementi.

I. Introduction

A. Capacitive accelerometers

In a typical capacitive accelerometer, the proof mass is suspended above a substrate by compliant springs. Two nominally equal-sized sense capacitors are formed between the electrically conductive proof mass and stationary electrodes /1/. When the substrate undergoes acceleration, the proof mass displaces from the nominal position, causing an imbalance in the capacitive half-bridge, shown in Fig.1a. This imbalance can be measured using charge integration technique /1/. Other techniques can be found in reference /2/.

Force balancing of the proof mass is attained by enclosing the proof mass in a negative feedback loop. The feedback loop measures deviations of the proof mass from its nominal position and applies a force to keep the proof mass centered. The accelerometer output is taken as the force needed to null, or zero, the position, shown in Fig.1b.

Taking into account only electronics of the system, the precision of measurement largely depends on position sense

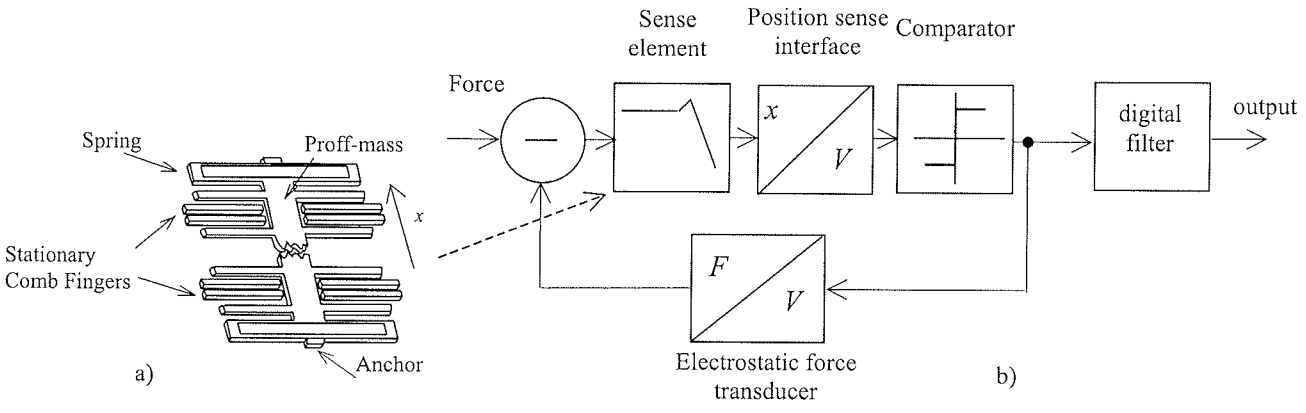

Figure 1a) Sense element, b) schematic of sigma- delta feedback loop

interface. A great deal of contributions therefore focuses on elimination of errors of charge amplifier as a main part of the sense interface. Common-mode rejection ratio, flicker noise, dc offset of operational amplifier, and mismatches in reference capacitors are the main problems that must be solved. An excellent solution can be found, for example, in /1/. In this solution, the op-amp flicker noise and dc offset are measured and subtracted using correlated double sampling /1/. By using an input common-mode feedback /1/, the problems with common-mode rejection ratio and with mismatches in reference capacitors are solved. However, using this approach the system complexity rapidly increases.

Considering the above-mentioned discussion, this paper explores a new sigma-delta technique based upon the use of a flip-flop circuit. Properties of the flip-flop and some topics are therefore depicted in the following paragraph.

B. Utilization of the flip-flop circuits in sensor-based systems

First idea to use the flip-flop in sensor-based systems can be found in /3/. The circuit in Fig.1 as the sensor based on a flip-flop circuit has been introduced in this reference. In comparison to the standard flip-flop, the control impulses are not applied to the bases of the transistors but the circuit is repeatedly connected to a voltage source, shown in Fig.2. Note that flip-flop can be also controlled by a triangular or sine wave signal. The standard flip-flop consisting of two transistors and two resistors is characterized by two stable states, one and zero. In case of ideal value symmetry because of a noise it is not possible to decide that the stable state will be final. However, over a large number of cycles the ratio of ones to zeros will be one - 50 % state of the flip-flop /3/.

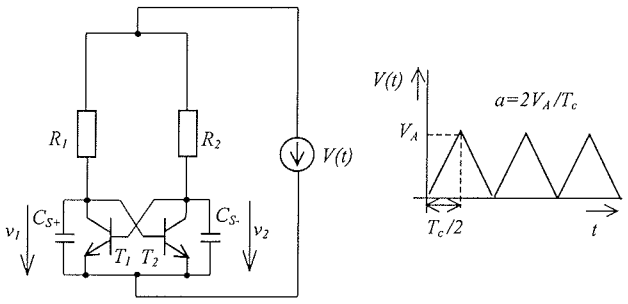

Figure 2. A flip-flop circuit with triangular control signal

As described in /4/, when $C_{S+}>C_{S-}$ and other parameters are identical, the flip-flop takes the stable state 'one'. It means that a high potential V_h is applied across capacitor C_{S+} while a low potential V_l is applied across capacitor C_{S-}. Assume that standard capacitors of the flip-flop are replaced by sense capacitors according to Fig.3.

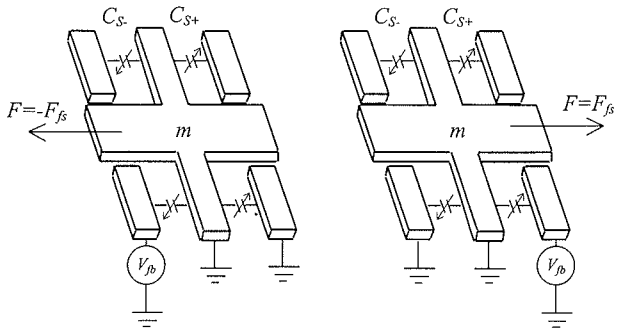

Figure 3. Schematic of capacitors C_{S+},C_{S-}

An electrostatic force between parallel plates of capacitor C_{S+} is given by

$$F_{+} = \frac{1}{2}\frac{\partial C_{S+}}{\partial x}V_h^2 \tag{1}$$

while between parallel plates of capacitor C_{S+} it is a force given by

$$F_{-} = \frac{1}{2}\frac{\partial C_{S-}}{\partial x}V_l^2 \tag{2}$$

The resultant force $F_{fs}=F+-F-$ may be shown to be

$$F_{fs} = \frac{1}{2}\frac{\partial C_S}{\partial x}V_{fb}^2 \tag{3}$$

where $\frac{\partial C_S}{\partial x} = \frac{\partial C_{S+}}{\partial x} = \frac{\partial C_{S-}}{\partial x}$ and $V_{fb}^2 = V_h^2 - V_l^2$. In case that flip-flop holds the stable state 'zero' it is a force $F=-F_{fs}$, shown in Fig.3. Hence, controlling the flip-flop by a triangular signal, the force is applied between parallel plates of the sense capacitors to keep the proof mass m centered, which corresponds with the principle of a capacitive accelerometer.

To use the above mentioned principle, the perfect value symmetry of the flip-flop must be achieved. Note that manufacture inaccuracy of the resistors in the standard CMOS technology is at least 15 %. Primarily, the problem with mismatches in resistances of the flip-flop must be solved. A modification of the flip-flop is described in the following section.

II. Modified flip-flop circuit

A. Switched capacitor based flip-flop circuit

As it can be seen in Fig.4a, the standard resistors are replaced by switched capacitors. The switches are repeatedly turned on and off in the following order S3,S2,S1 and again S3. Corresponding control signals are shown in Fig.5. When control frequency f_{SW} of the switched capacitor C is at least two orders higher than the frequency fc of the triangular impulse generator V, the circuit is equivalent to the scheme shown in Fig.4b. To the point 1 as

well as to the point 2 an equivalent resistance R_{eqv} is connected.

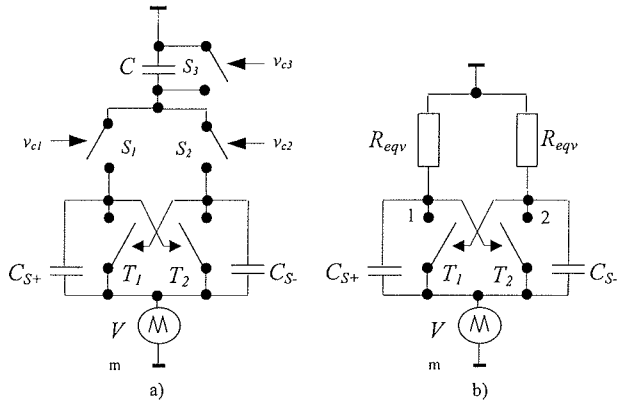

Figure 4a) Flip-flop with the switched capacitor,b) equivalent circuit diagram

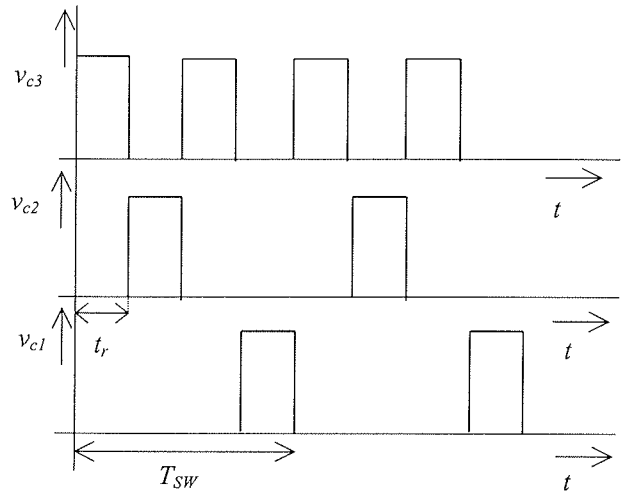

Figure 5. Control signals vc1,vc2, and vc3 of the switches S1,S2, and S3

Equivalent resistance R_{eqv} is given by well-known formula

$$R_{eqv} = \frac{1}{Cf_{SW}} \tag{4}$$

The approach shown in Fig.4a has several important advantages, including its non-sensitivity to changes of the capacitor C and the control frequency f_{SW}. The circuit is also realizable using CMOS technology. On the other hand, switch charge injection as a new influence must be taken into account. Switch charge injection and a noise within the flip-flop are analysed in the following paragraphs.

B. Analysis of a flicker noise

Flicker noise in the flip-flop is mainly due to switches S1,S2,S3. Flicker noise due to unipolar transistors T1,T2 can be omitted because these transistors are turned off in the moment of turnover. Fig.6 shows a CMOS switch. Since the switches are repeatedly turned on and off, a non-stationary model and usage of time domain analysis is needed to analyse the influence of flicker noise.

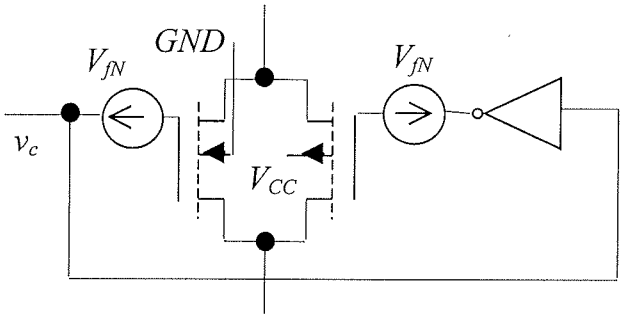

Figure 6. CMOS switch

As shown in /5/, the root mean square (RMS) of noise voltage V_{fN} relating to the control circuit is given by

$$V_{fN} = \left(\frac{q}{AC_{ox}}\right)^2 \frac{1}{t_r^2} \int_0^{t_r}\int_0^{t_r}\int_{\lambda_L}^{\lambda_H} g(\lambda) C_\lambda (s_1, |s_1 - s_2|) d\lambda ds_1 ds_2 \tag{5}$$

where C_{ox} is the gate oxide capacitance, A is the channel area, q is the elementary charge, λ_H is the fastest transition rate, and λ_L is the slowest transition rate of the carriers, g represents the distribution of λ, C_λ is an autocovariance in the time domain /5/ and t_r is the time during which the switch is turned on. Typical values for 0.8μm CMOS process are as follows: $\lambda_H = 10^{10} s^{-1}$, $\lambda_L = 4.10^{-21} s^{-1}$, $C_{ox} = 0.8$ fFμm^{-2}, $k_F = 10^{-27}$, A=1 μm^2. By numerical solving of (5), for t_r=0.1 μs, we get V_{fN}=1.2 μV. Because of such a small noise voltage, the influence of the flicker noise can be neglected.

C. Analysis of kT/C and shot noise

Because both kT/C and shot noise are high frequency, they are analysed in this paragraph together. To quantify the effects of the noise on the value symmetry of the flip-flop, it is useful to refer all noise sources to the points 1,2, shown in Fig.4b.

As it is described in paragraph IIa, the switches of the flip-flop are repeatedly turned on in the following order S_3,S_2,S_1, and again S_3. When it holds that C_{S+},C_{S-}>>C_{SW}, where C_{SW} is an output capacitance of the switch, kT/C noise is largely due to sense capacitors C_{S+},C_{S-} . Therefore, RMS of the noise relating to the points 1,2 (see Fig.4a) is given by $V_{Th} = \sqrt{2kT\ C_S}$, where k is the Boltzman constant, T is the thermodynamic temperature, and C_S=(C_{S+}+C_{S-})/2.

Shot noise is due to switches S_1,S_2. Shot noise due to switch S_3 can be omitted, because the noise of this source is equally distributed to the right and left side of the flip-flop. As shown in /5/, RMS of the shot noise of the switch, which is repeatedly turned on and off, leads to

$V_{sh} = \sqrt{qV_m / (2C_{SW})}$ where V_m is maximal voltage across the switch and q is the elementary charge. By means of Duhamel's integral it can be shown that v_1

$$v_1 = at - aR_{eqv}C_{S+} \quad (6)$$

and v_2

$$v_2 = at - aR_{eqv}C_{S-} \quad (7)$$

where function *at* describes the triangular control signal of the flip-flop (see Fig.2). Therefore, the maximal voltage across the switch S_1 is $aR_{eqv}C_{S+}$ and across the switch S_2 it is a value $aR_{eqv}C_{S-}$. In case of our circuit, shot noise due to the switches S_1,S_2 is given by $V_{sh} = \sqrt{\frac{qaR_{eqv}C_S}{4C_{SW}}}$. Thus, the resultant high frequency noise between the points 1,2 of the flip-flop is given by

$$V_{no} = \sqrt{\frac{qaR_{eqv}C_S}{4C_{SW}} + \frac{kT}{C_S}} \quad (8)$$

III. Experimental results

A. Verification of the flip-flop functionality

An experimental circuit was constructed from discrete elements. The switches were realized by means of an integrated circuit 74HCT4066, and the transistors T_1,T_2 in N3515 differential pair were used. Primarily, the existence of two stable states had to be verified. The flip-flop was controlled by triangular impulses with the parameters as follows: $a=0.85\ 10^{-4}\ Vs^{-1}$, T_c=340 μs, and other parameters were t_r=0.1 μs, T_{SW}=0.4 μs, C_{SW}=3.5 pF, and C_{S+} ,C_{S-} about 28 pF.

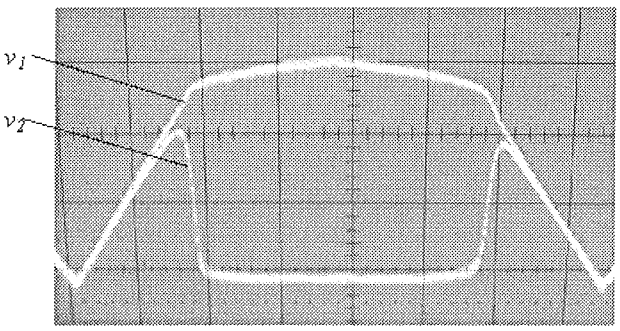

Figure 7. Courses of voltages v_1,v_2

Fig.7 shows oscilloscope courses of the voltages v_1,v_2 . During the experiment the flip-flop according to Fig.4a took the stable state one or zero. It is sufficient evidence of the existence of only two stable states.

B. Influence of a noise

Using (4), (8) and parameter values shown in the previous paragraph it follows that RMS of the total high frequency noise should be about 20 μV.

Fig.8a) shows the change of voltage v_1 which is caused by a charge injection of the switch S_1. When the switch S_1 is turned on, the switch S_2 is turned off and therefore switch charge injection can break the value symmetry of the flip-flop. However, a frequency jitter of the triangular signal must be taken into account in relation to the control frequency f_{SW} of the switches. From this point of view the influence of switch charge injection relating to the points 1,2 (see Fig.4b) is only an additive noise. The resultant probability of distribution is then shown in Fig.8b. As it can be seen, expected RMS of the total noise V_{nois} is 260 μV. Experiments have been carried out to verify this value. The measurement set up is shown in Fig.9a. The impulses from flip-flop outputs were processed, through additive invertors T_3,R; T_4,R, in a personal computer (PC). The measurement procedure first involves the adjustment of the offset compensation voltage V_{of} until 50 % state of the flip-flop is obtained, as shown in Fig.9b. This voltage is then again

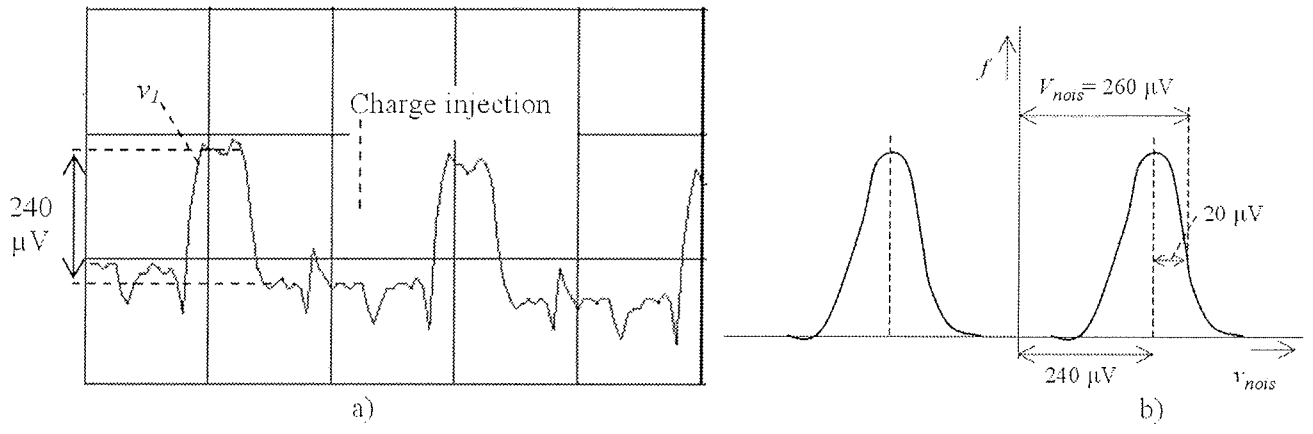

Figure 8a) Charge injection, b) resultant probability of distribution

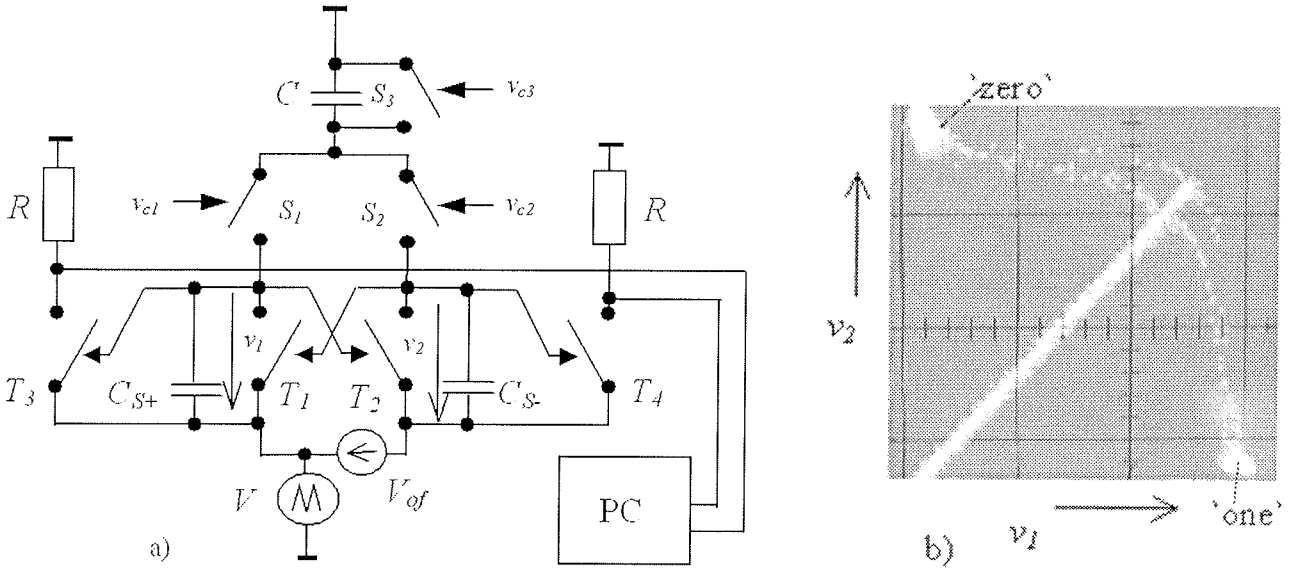

Figure 9a) Measurement set up, b) 50 % state of the flip-flop

tuned until 84 % is obtained. The difference in the two offset voltages is then the RMS of the noise. "Eighty-four percent" is used because this is the probability of obtaining a `one` when the shift in the distribution equals V_{nois}. According to the theoretical conclusion, V_{nois} is 260 μV, whereas the measured V_{nois} was 290 μV.

It is useful to know the measured capacitive error caused by the noise. Since V_{of} is defined as a difference between v_2 and v_1, by means of (6) and (7) we get $V_{of}=aR_{eq}(C_{S+}-C_{S-})$. According to the parameters of our circuit it follows that $V_{of}/(C_{S+}-C_{S-})=1$ mV/pF. Therefore, the noise causes the capacitive error 290 fF.

In another experiment, soma extra capacitors were added to the capacitor C_{S+}. Predicted and measured values of the offset voltage V_{of} are shown in Tab.1.

Table 1. Predicted and measured values of V_{of} in the dependence on an additive capacitance

Additive capacitance [pF]	*Measured voltage* [mV]	*Predicted voltage* [mV]
5.5	5.7	5.5
11.9	11.7	11.9
12.7	13	12.7

IV. Conclusions

A new capacitive sigma-delta modulation technique has been presented. This technique consists in usage of a switched capacitor based flip-flop. Equivalent circuit is then characterized by perfect matched load resistances. Another main advantages in comparison to the ordinary approaches are as follows: negligible flicker noise (only a few μV), simplicity (charge amplifier, comparator and another compensating circuits are not needed), high capacitive sensitivity (in relation to an offset voltage it is 1mV/pF). The capacitive sensitivity may be at need regulated by a control frequency of the switches. A disadvantage is relatively high charge injection of the switches. However, tested circuit was made only from discrete elements. By realization on a chip the substantial enhancement can be expected.

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