ELEKTROTEHNIŠKI VESTNIK 78(5): 304-311, 2011
ENGLISH EDITION

Effective Controller Design for the Dynamic Voltage Restorer (DVR) for Voltage Sag Mitigation in Distribution Utilities

Lin Xu[1], Yang Han[2]

[1]*Sichuan Electric Power Research Institute, No.24, QingHua Road, QingYang District, 610072 Chengdu, China*
E-mail: xulin198431@hotmail.com
[2]*School of Mechatronics Engineering, University of Electronics Science and Technology of China, No.2006 XiYuan Road, West Park of Chengdu High-Tech Zone, 611731 Chengdu, China*
E-mail: hanyang_facts@hotmail.com

Abstract. The voltage sag detection algorithm and control algorithm synthesis of the dynamic voltage restorer (DVR) are proposed. The double synchronous reference frame phase-locked loop (DSRF-PLL) is applied for the voltage sag detection, which is able to calculate the phase angle of the positive-sequence fundamental component of grid voltages even under unbalanced and distorted grid voltages. The effective control strategy of the DVR is proposed, which includes the reference compensation voltage generation, the control scheme for the shun-connected voltage source converter (VSC) and the control algorithm for the series-connected voltage source inverter (VSI). Finally, extensive simulation results are presented to verify the validity and effectiveness of the proposed control strategy.

Keywords: Dynamic voltage restorer, phase locked loop (PLL), voltage sag, sequence decoupling, proportional resonant controller.

1 INTRODUCTION

The modern industrial plant is subjected to abnormal shutdown or malfunction due to the power quality problems. One of the most concerning disturbances affecting power quality are voltage sags. Their major source are short-circuits on the utility lines. Faults many kilometers from the disturbed process will generate a momentary voltage sag in the electrical environment to the end user. A reduction of the short-circuit current magnitude may lead to a substantial power quality improvement because the majority of the sensitive industrial processes (including computer system, power electronics and variable speed drives) are capable of riding through a sag of a very limited amplitude [1-5,8].

In retrospect, many researchers have discussed the various algorithms to calculate voltage sag phenomena. In [6], a simple approximated method for calculation of voltage sags in an electrical network was presented. The paper illustrates the construction of a square matrix that, under acceptable assumptions, directly provides voltage drops at each node of the network and for each faulted node. The voltage sags matrix of the network, gives a representation of sags produced by symmetrical faults for the overall network. In [7], a three-phase precision measurement system for the electronic electricity meter was presented, which is based on a digital signal processor (DSP) in combination with a multichannel analog-to-digital (A/D) converter. Besides, the analyzer functions are implemented in compliance with the European EN5160 Standard, and they include detection of short- and long-term voltage sags, swells and outages, harmonic analysis of current and voltage signals as well as assessment of voltage flicker.

The solutions to mitigate the consequences of voltage sag have also attracted attention of the academic community in recent years. In [8], it was reported that, independently on its magnitude and shape, each voltage sag lasts as long as the protection equipment allows fault current to flow. A reduction of the clearing time of the lines protection equipment may lead to a substantial power quality improvement because the majority of sensitive industrial processes are capable to ride through the sag of very limited duration. In [9], the effects of limiting reactors (LR) connected at the beginning of the medium-voltage (MV) feeders are investigated, which allow for effective mitigation of voltage dips and are considered as a trivial solution, attractive for the reason of a very low cost, simplicity and reliability.

With the development of modern power electronics, digital controllers, such as digital signal processors (DSPs), the dynamic voltage restorer (DVR) has been recognized as the best choice to protect the industrial facilities from voltage sag and other voltage disturbances. Fig.1 shows the typical circuit diagram of

Received November 15, 2011
Accepted December 16, 2011

the DVR in a distribution system. It demonstrates that voltage sag may be incurred by the fault from the adjacent feeder or the fault from the transmission network. Therefore, the DVRs can be applied to protect the sensitive loads of high-tech industries with adjustable speed drives and other power electronic loads. For the industries with a high penetration of the induction motors, the energy storage might be used and a sophisticated controller must be adopted due to the inherit inertia of induction motors and their capability to withstand short duration, shallow sags and phase jumps [10].

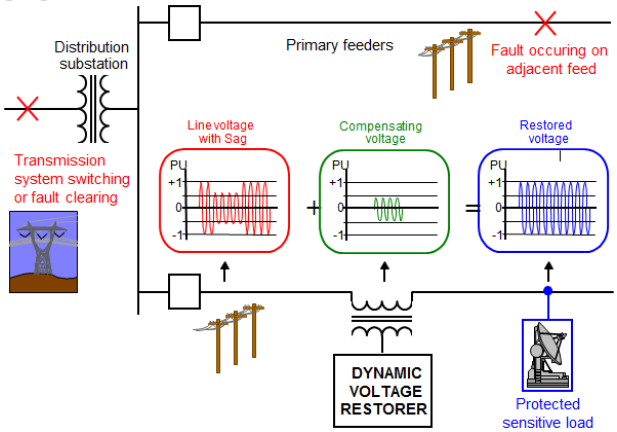


Figure 1. The circuit diagram of the dynamic voltage restorer (DVR) for voltage sag mitigation in the distribution utilities.

A schematic diagram of DVR is shown in Fig.2. The DVR inverters are based on three single-phase full-bridge voltage-source inverters (VSI) using common dc-link.These inverters are series coupled into the utility grid using three single-phase transformers to ensure galvanic isolation and to step-up the injected voltage. A capacitive filter is located at the line side to filter out the switching harmonics generated by the inverter. The dc link can be charged with voltage source rectifier (VSR) which is connected to the utility grid side [10].

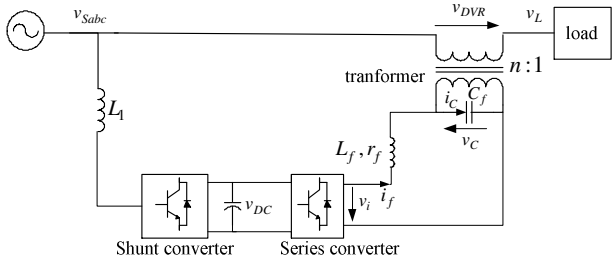


Figure 2.Single-phase representation the DVR system.

In order to generate a fast and accurate reference voltage, the most important aspect to consider in the control of the DVR system is the proper synchronization with the utility voltages. Specifically, in case of voltage sag or harmonics, the detection of the positive-sequence voltage components at fundamental frequency is essential for the control of DVR. The detection of the amplitude and the phase angle of the positive-sequence component must be fast and accurate, even if the utility voltages undergo sag, distortion and/or unbalanced.

In this paper, an effective controller design method for the DVR is proposed, which is based on the double synchronous reference frame phase-locked-loop (DSRF-PLL) for grid-synchronization, the reference injection voltage generation, the control schemes for the PWM voltage source converter (VSC) and series-connected PWM voltage source inverter (VSI). To ensure accurate compensation for the grid distortion, the proportional-resonant current controller is adopted in the inner current loop, which provides infinite controller gain at the selected harmonic frequencies. Hence, the DVR is capable to mitigate voltage sag, grid unbalance and distortion. Finally, the simulation results are presented to verify the validity and effectiveness of the proposed control algorithms.

2 Grid-Synchronization Algorithm using Double Synchronous Reference Frame PLL

Considering a three-phase three-wire system, the zero-sequence component is null. To introduce the decoupling network for grid-synchronization, one supposes the voltage vector consisting of two generic components rotating with $n\omega$ and $m\omega$ frequencies respectively, where n and m can be either positive or negative with the fundamental frequency ω. Hence, the voltage vectors in the α-β plane can be denoted as [10]:

$$v_{S(\alpha\beta)} = \begin{bmatrix} v_{S\alpha} \\ v_{S\beta} \end{bmatrix} = V_S^n \begin{bmatrix} \cos(n\omega t + \phi^n) \\ \sin(n\omega t + \phi^n) \end{bmatrix} + V_S^m \begin{bmatrix} \cos(m\omega t + \phi^m) \\ \sin(m\omega t + \phi^m) \end{bmatrix} \quad (1)$$

Additionally, two rotating reference frames are considered, dq^n and dq^m, whose angular positions are $n\theta$ and $m\theta$ respectively, where θ is the phase angle detected by the PLL. Hence the voltage vector v_s can be expressed in the dq^n and dq^m synchronous frame as [11]:

$$v_{S(dq^i)} = \begin{bmatrix} v_{Sd^i} \\ v_{Sq^i} \end{bmatrix} = \left[T_{dq^i}\right] \cdot v_{S(\alpha\beta)}$$

$$= V_S^n \begin{bmatrix} \cos(n\omega t + \phi^n - i\theta) \\ \sin(n\omega t + \phi^n - i\theta) \end{bmatrix} + V_S^m \begin{bmatrix} \cos(m\omega t + \phi^m - i\theta) \\ \sin(m\omega t + \phi^m - i\theta) \end{bmatrix} \quad (2)$$

where $\left[T_{dq^i}\right] = \begin{bmatrix} \cos i\theta & \sin i\theta \\ -\sin i\theta & \cos i\theta \end{bmatrix}, i = n, m$.

When the grid synchronization using the proposed PLL is achieved, that means $\theta=\omega t$, hence we get:

$$v_{S(dq^n)} = V_S^n \begin{bmatrix} \cos(\phi^n) \\ \sin(\phi^n) \end{bmatrix} + V_S^m \begin{bmatrix} \cos(m\omega t + \phi^m - n\omega t) \\ \sin(m\omega t + \phi^m - n\omega t) \end{bmatrix}$$

$$= V_S^n \begin{bmatrix} \cos(\phi^n) \\ \sin(\phi^n) \end{bmatrix} + V_S^m \cos(\phi^m) \begin{bmatrix} \cos((n-m)\omega t) \\ -\sin((n-m)\omega t) \end{bmatrix}$$

$$+ V_S^m \sin(\phi^m) \begin{bmatrix} \sin((n-m)\omega t) \\ \cos((n-m)\omega t) \end{bmatrix} \quad (3)$$

The same expression in dq^m axes may be deduced by just interchanging m and n. The amplitude of the signal oscillation in the dq^n axes depends on the mean value of the signal in the dq^m axes, and vice versa. Therefore, in order to cancel the oscillations in dq^n axes, the decoupling algorithm between the d-axis and q-axis quantities is proposed, as shown in Fig.3. The same cell may be used in dq^m axes by just interchanging m and n in Fig.3.

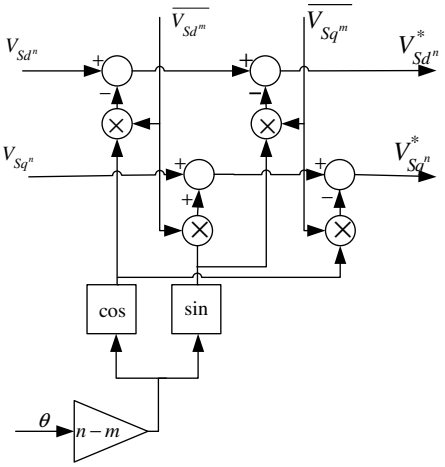


Figure 3. Decoupling cell for canceling the effect of v_S^m on the dq^n frame signals.

In order to calculate the averaged quantities (dc values) of v_{sd}^n, v_{sq}^n, v_{sd}^m, v_{sq}^m, the cross term decoupling network is proposed, as shown in Fig .4. Notably, the low-pass filer (LPF) is introduced herein to calculate the dc components of these quantities in the synchronous frame (d-q frame) with the transfer function $LPF(s)=\omega_f/(s+\omega_f)$, where ω_f denotes the cut-off frequency and ω_f=35Hz is selected herein.

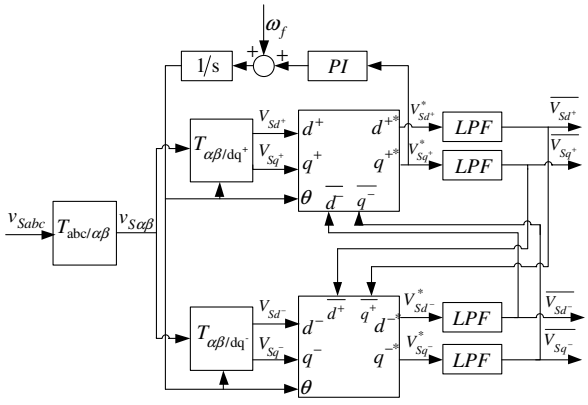


Figure 4. Block diagram of the double synchronous reference frame PLL.

The mathematical model of the double synchronous frame PLL can be derived by manipulation in the frequency domain. Referring to Fig.3, the unit sinusoidal functions are defined as: u_1=cos[$(n$-$m)\omega t$], u_2=sin[$(n$-$m)\omega t$], the averaged quantities (dc values) of v_{sd}^n, v_{sq}^n, v_{sd}^m, v_{sq}^m can be derived in the frequency domain as in the following equations:

$$\overline{v_{Sd^n}}(s)=\frac{\omega_f}{s+\omega_f}(v_{Sd^n}(s)-u_1(s)*\overline{v_{Sd^m}}(s)-u_2(s)*\overline{v_{Sq^m}}(s)) \quad (4a)$$

$$\overline{v_{Sq^n}}(s)=\frac{\omega_f}{s+\omega_f}(v_{Sq^n}(s)-u_1(s)*\overline{v_{Sq^m}}(s)+u_2(s)*\overline{v_{Sd^m}}(s)) \quad (4b)$$

$$\overline{v_{Sd^m}}(s)=\frac{\omega_f}{s+\omega_f}(v_{Sd^m}(s)-u_1(s)*\overline{v_{Sd^n}}(s)+u_2(s)*\overline{v_{Sq^n}}(s)) \quad (4c)$$

$$\overline{v_{Sq^m}}(s)=\frac{\omega_f}{s+\omega_f}(v_{Sq^m}(s)-u_1(s)*\overline{v_{Sq^n}}(s)-u_2(s)*\overline{v_{Sd^n}}(s)) \quad (4d)$$

Note that the asterisk '*' represents the convolution product of the signals in the frequency domain (s-domain). These equations can be transformed back to the time domain as:

$$\dot{\overline{v_{Sd^n}}}=\omega_f(v_{Sd^n}-\overline{v_{Sd^n}}-u_1\overline{v_{Sd^m}}-u_2\overline{v_{Sq^m}}) \quad (5)$$

$$v_{Sd^n}=V_S^n\cos(\phi^n)+u_1V_S^m\cos(\phi^m)+u_2V_S^m\sin(\phi^m) \quad (6)$$

Moreover, Equation (6) can be rewritten:

$$\dot{\overline{v_{Sd^n}}}=\omega_f[V_S^n\cos(\phi^n)+u_1V_S^m\cos(\phi^m)+u_2V_S^m\sin(\phi^m)-\overline{v_{Sd^n}}-u_1\overline{v_{Sd^m}}-u_2\overline{v_{Sq^m}}] \quad (7)$$

Followed by the same procedure, the mathematical equations for the as shown in Eq.(4) can also be derived. After manipulation of these equations, the following state-space model is obtained:

$$\begin{cases}\dot{X}(t)=A(t).X(t)+B(t).U(t)\\ Y(t)=C.X(t)\end{cases} \quad (8)$$

where $Y_{(t)}^T=X_{(t)}^T=\left[\overline{v_{Sd^n}},\overline{v_{Sq^n}},\overline{v_{Sd^m}},\overline{v_{Sq^m}}\right]$, $C(t)=I_{4\times4}$

$$U(t)=\begin{bmatrix}V_S^n\cos(\phi^n)\\ V_S^n\sin(\phi^n)\\ V_S^m\cos(\phi^m)\\ V_S^m\sin(\phi^m)\end{bmatrix},\ A(t)=-B(t)=\omega_f\begin{bmatrix}-1&0&-u_1&-u_2\\ 0&-1&u_2&-u_1\\ -u_1&u_2&-1&0\\ -u_2&-u_1&0&-1\end{bmatrix}.$$

In the case of n=1, m=-1, the positive and negative fundamental frequency components in the dq^+ and dq^- axes are decoupled.

Meanwhile, the DSRF-PLL should cancels the double frequency oscillation terms at 2ω in the voltage V_{sq}^{*+1}. With the aim of V_{sq}^{*+1}=0, a proportional-integral (PI) control loop is added to manipulate V_{sq}^{*+1} where the phase error is [as shown in Fig.4]:

$$\theta_{err}=(k_p+\frac{k_i}{s})\times(V_{Sq^{+1}}^*-0) \quad (9)$$

where $k_i=\frac{\omega_c^2}{V_s^{+1}}$, $k_p=2\xi\sqrt{\frac{k_i}{V_s^{+1}}}$, $\omega_c=2\pi\times25\,rad/s$, $\xi=1/\sqrt{2}$.

To show the promising behavior of the proposed DSRF-PLL, unbalanced and distorted grid operating conditions are simulated using Matlab/Simulink, and the detected phase angle of the fundamental component as

well as the detected positive sequence components in grid voltages are provided. Fig.5 shows the simulation waveforms of the grid voltages of the typical 380V low voltage (LV) distribution network. The 10% unbalance and 5% fifth order harmonic voltages are applied to the grid at t=0.1s to test the dynamic response of the DSRF-PLL algorithm.

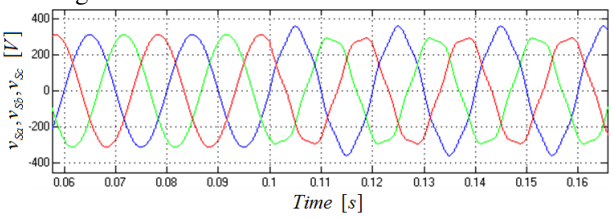


Figure 5. The waveform of the three-phase grid voltages.

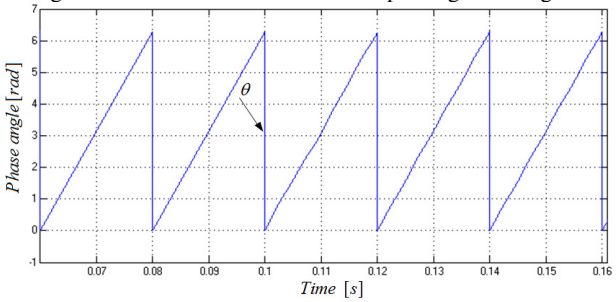


Figure 6. The phase angle [rad] detected from the DSRF-PLL.

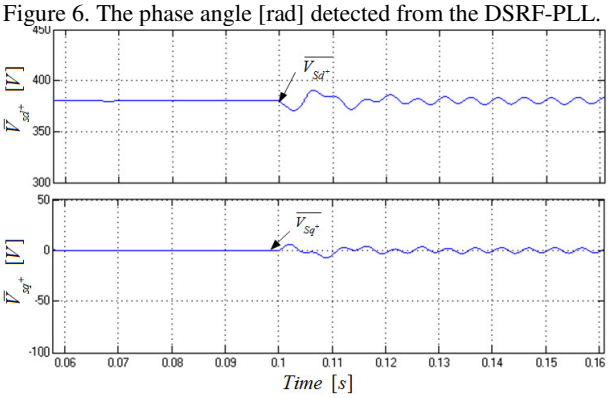


Figure 7. The detected positive sequence voltage components from the DSRF-PLL.

Fig.6 and Fig.7 show the detected phase angle and the amplitudes of the positive sequence components of the grid voltages, respectively. It shows that the positive sequence components are detected with a sufficient high precision with a response time of half a cycle. The simulation results confirm that the proposed DSRF-PLL is an effective solution to detect the positive sequence fundamental components from the unbalanced and distorted utility voltages. These detected quantities are utilized as grid-synchronization signals for the control algorithm of the DVR, as discussed in the next section.

3 CONTROL STRATEGY OF THE DYNAMIC VOLTAGE RESTORER

3.1 Generation of Reference Injection Voltage

The proposed DSRF-PLL is used to generate appropriate reference waves in any case of the line voltage disturbances. The acquisition of the source side voltages and the DVR Ac side voltages are required for control algorithm synthesis. Notably, the zero-sequence voltage component is neglected herein since we are dealing with three-phase three-wire system.

The source side terminal voltages, v_{Sa}, v_{Sb}, v_{Sc} are transformed to the synchronous reference frame by using the *abc/αβ* and *αβ/dq*$^+$ transformation, and the *d-q* frame quantities of the positive sequence grid voltages V_{sd}^+ and V_{sq}^+ are obtained. The V_{sd}^+ component consists of an Ac component $V_{sd}^+{}_{ac}$ and a dc component $V_{sd}^+{}_{dc}$. Similarly, the V_{sq}^+ component also consists of an Ac component $V_{sq}^+{}_{ac}$ and a dc component $V_{sq}^+{}_{dc}$. The quantities $V_{sd}^+{}_{dc}$ and $V_{sq}^+{}_{dc}$ are the positive-sequence components of the grid voltages. The Ac components $V_{sd}^+{}_{ac}$ and $V_{sq}^+{}_{ac}$ are related with nonideal voltage conditions such as the negative-sequence component and harmonics.

Therefore, in order to control the output terminal voltages to be symmetrical and in-phase with the reference waves $V_{sd\text{-}ref}$ and $V_{sd\text{-}ref}$, the *q*-axis component of the positive sequence voltage V_{sq}^+ must be compensated to zero and the *d*-axis component of the positive sequence voltage V_{sd}^+ has to be controlled to the reference dc value $V_{sd\text{-}ref}$=380V.

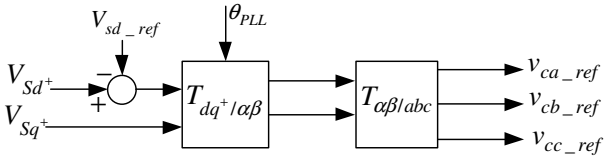


Figure 8. Block diagram of the reference voltage generation

Fig.8 shows the simplified block diagram for the reference injection voltage generation algorithm. The quantities $u_{DVR\text{-}d}$=V_{sd}^+-$V_{sd\text{-}ref}$ and $u_{DVR\text{-}q}$=V_{sq}^+ are compensated for the *d*-axis and *q*-axis, respectively. With the reference value, the magnitudes of the output terminal voltages are regulated to the constant rated line voltage $V_{sd\text{-}ref}$. The control variables in the *d-q* coordinates $u_{DVR\text{-}d}$, $u_{DVR\text{-}q}$ are transformed back to the *a-b-c* coordinates by using inverse Park's transformation. Hence, the reference compensating voltages for the DVR in the *a-b-c* coordinates $v_{ca\text{-}ref}$, $v_{cb\text{-}ref}$, $v_{cc\text{-}ref}$ are calculated. Next, the control scheme for the series connected voltage source inverter and shunt connected voltage source converter would be explained.

3.2 Control Strategy for the Series-Connected Voltage Source Inverter

To achieve a good transient and steady-state performance, a multi-loop proportional-integral (PI) controller is proposed to control series converter of the DVR. As shown in Fig.9, an inner current control loop (feedback filter capacitor current i_C) is adopted for ensuring fast response as well as attenuation of the filter *LC* resonance. The outer voltage loop is used for reference signal tracking. Normally, the control

bandwidth of the outer voltage control loop is designed to be five or ten times lower than that of the inner current control loop. The proposed controller achieves the response time of about 500μs to sudden voltage sag or swell in the grid without any oscillation, the performance of the proposed control strategy is validated by simulation results.

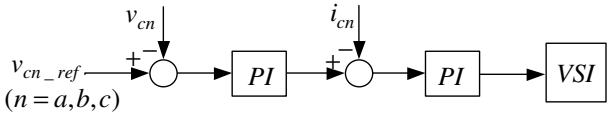


Figure 9. The simplified diagram for the multi-loop control strategy of VSI

3.3 Control Strategy for the Shunt-Connected Voltage Source Converter

As it is known, DVR operates to maintain the load supply voltage at its rated value, and during a voltage distribution, the DVR exchanges active and reactive power with the grid. If active power is supplied to the load from the DVR, it needs a source for this energy. In this paper, the dc link voltage is charged with the voltage source converter shunt connected to the grid. The dc voltage can be controlled to almost constant. Fig.10 shows the complete control diagram for the DVR, which is capable of mitigating voltage sag disturbances even under unbalanced and distorted grid scenario.

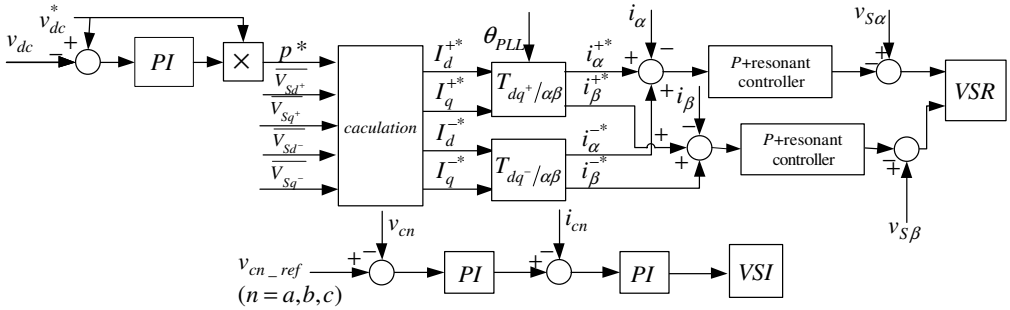


Figure 10. A complete control strategy of the shunt-connected VSR and the series-connected VSI.

Both positive and negative sequence currents are controlled, the current command I_{dc}^* is determined by the dc-link voltage controller, the required power P_0 is obtained by multiplying v_{dc}^* to the output of the voltage controller i_{dc}^*, i.e., $p^*=v_{dc}^* i_{dc}^*$, the current commands are obtained as:

$$\begin{bmatrix} I_d^{p*} \\ I_q^{p*} \\ I_d^{n*} \\ I_q^{n*} \end{bmatrix} = \frac{2}{3D} v_{dc}^* \times (PI) \times (v_{dc}^* - v_{dc}) \begin{bmatrix} \overline{V_{sd}^+} \\ \overline{V_{sq}^+} \\ \overline{V_{sd}^-} \\ \overline{V_{sq}^-} \end{bmatrix} \tag{10}$$

where $D=(\overline{V_{sd}^+})^2+(\overline{V_{sq}^+})^2-(\overline{V_{sd}^-})^2-(V_{sq}^-)^2$.

The positive and negative sequence components of supply voltages are achieved by using the DSRF-PLL. To reduce the control parameters and complexity, the controller is based on α-β coordinates where i_α, i_β would track the sum of i_α^{+*} and i_α^{-*}, i_β^{+*} and i_β^{-*}, respectively.

Notably, the proportional-integral (PI) regulator shows unsatisfactory performance for current tracking in case of alternating reference signal, which results in remarkable phase angle and amplitude errors. The proportional resonant (PR) current controller, on the other hand, achieves perfect tracking performance for the alternating signal, which mimics the PI regulator implemented in the synchronous reference frame (SRF) with the following transfer function:

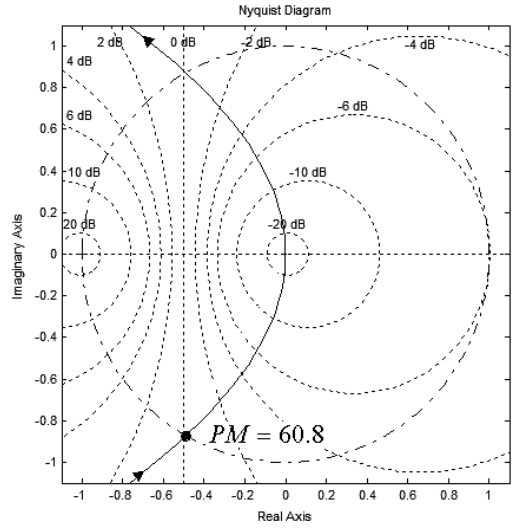
$$G_{PR}(s) = K_{cc}[1+\frac{1}{\tau}\cdot\frac{2s}{(s^2+\omega_0^2)}] \tag{11}$$

where the parameter τ is defined as the time constant for the PR controller, ω_0 denotes the angular frequency of fundamental grid voltage. Hence the PR regulator achieves zero steady-state error for the alternating signal at ω_0 due to the infinite open-loop gain introduced by the PR current regulator. Notably, the angular frequency ω_0 should be replaced by $n\omega_0$ (n is integer) in case of harmonic compensation in case of grid distortion. Hence, the open loop transfer function of the current loop for the shunt-connected converter is derived as:

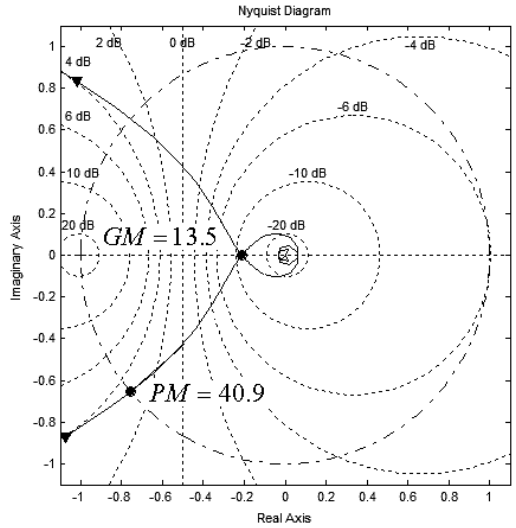
$$G_{open,PR}(s) = G_{PR}(s)\cdot\frac{1}{1+T_d\cdot s}\cdot\frac{1}{R+L_1\cdot s} \tag{12}$$

Fig.11 shows the Nyquist plot of Eq.(12) under different control delays but the same proportional gain K_{cc} and the time constant τ are assumed. Fig.11(a) shows the case when T_d=0. It can be observed that the PR controllers achieve the phase margin (PM) of 60.8 degree and an infinite gain margin (GM). Fig.11(b) shows the case when the control delay equals to the PWM switching frequency of the IGBT, i.e., $T_d=T_{sw}$. It can be observed that the PR controllers achieve the phase margin (PM) of 40.9 degree with the gain margin of 13.5dB.

Notably, the advantage of the PR regulator at the target frequency is appreciated for its infinite open-loop gain, thus it provides much better tracking performance compared to the PI regulator. By varying the controller gain K_{cc} and time constant τ in the Nyquist plot, a compromise can be achieved between the tracking performance and the stability margin.



(a)



(b)

Figure 11. Nyquist plot of the open-loop transfer function of the current tracking scheme using proportional-resonant (PR) controller. (a) T_d=0; (b) T_d=T_{sw}.

4 SIMULATION RESULTS

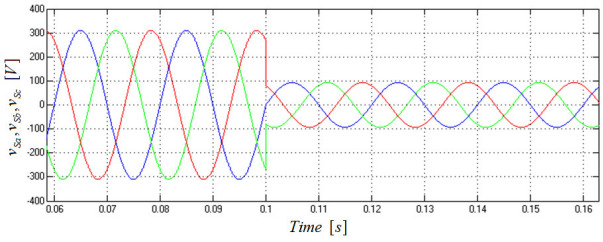
To verify the validity of the proposed DVR system for voltage mitigation performances, the simulation study has been implemented using Matlab/Simulink software. Notably, the simulations are based on the 380V/50kVA power rating system as shown in Fig.2 and the system parameter is shown in Table 1.

Table 1: Specifications and system parameters.

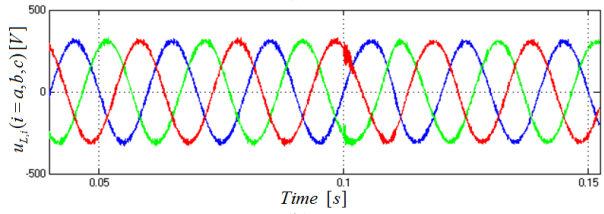
System Parameters	Values
Grid voltage	380V
Compensation power	50kVA
Transformer turns ratio	1:1
Dc-link capacitor	10000μF
Dc-link voltage	650V
Filter capacitance C_f	55μF
Filter inductance L_f	500μH
Coupling inductance L_1	1500μH

To test the robustness of the devised control algorithms for the dynamic voltage restorer (DVR), three types of voltage sags were generated by using the programmable voltage source in the Matlab/Simulink, which are summarized as follows:

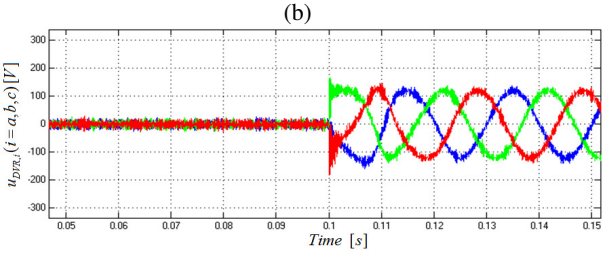
Case 1: A typical three-phase fault is considered, where all the phase voltages are symmetrically decreased to 70% from the rated value. Fig.12 shows the simulated waveforms for the grid voltages, the load voltages and the injection voltages of DVR when symmetrical sag occurred. It can be observed that the DVR compensates the symmetrical sag rapidly when the grid side voltage dip occurs, and the response time is about half cycle owing to the perfect performance of the grid synchronization algorithm achieved by the DSRF-PLL. As a result, the sinusoidal waveforms are ensured at the load side.



(a)



(b)



(c)

Figure 12. The simulated waveforms of the source voltages, load voltages, and the injection voltages of DVR when symmetrical sag occurred (case 1). (a) The grid voltages; (b). The load side voltages; (c). The compensation voltages.

Case 2: A typical unbalanced fault with harmonic distortion is simulated, where the grid voltage in phase 'A' is increased by 20%, the phase angle of grid voltage in phase 'B' jumped by 20° and the amplitude decreased by 20%, and the phase angle of grid voltage in phase 'C' jumped by -20° and the amplitude decreased by 20% from the normal condition. Meanwhile, 10% fifth order harmonic component is abruptly applied to all the three phase voltages.

Fig.13 shows the simulated waveforms of the grid voltages, load voltages, and the injection voltages of

the DVR when asymmetrical sag occurred with distortion in the grid voltages. Owing to the sequence decoupling performance of the DSRF-PLL, accurate detection of the positive sequence fundamental component of the grid voltages is achieved. Besides, the proportional-resonant (PR) controller provides infinite control gain at the target harmonic frequencies. Hence, the DVR also compensates the harmonics with a sufficient precision, as indicated by the simulation results in Fig.13. It can be observed that the load side voltages are harmonic-free and sinusoidal waveforms are guaranteed.

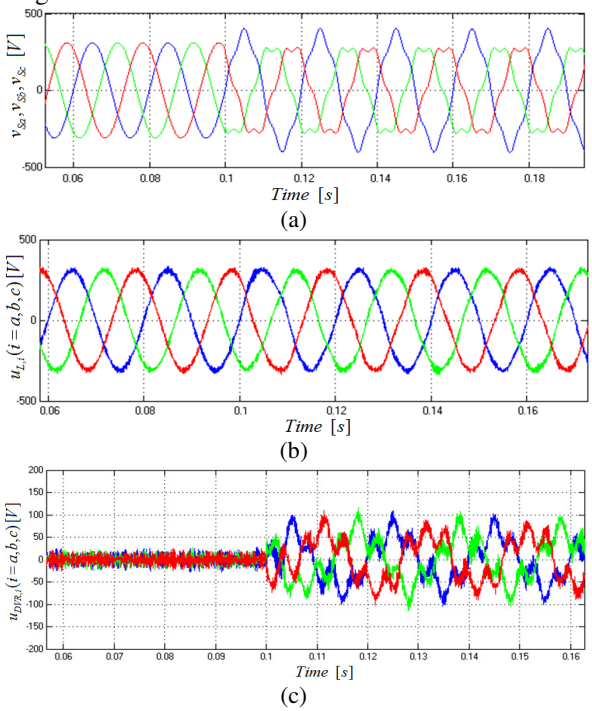


Figure 13. The simulated waveforms of the source voltages, load voltages, and the injection voltages of DVR when asymmetrical sag occurred with distortion in the grid voltages (case 2). (a) The grid voltages; (b). The load side voltages; (c). The compensation voltages.

Case 3: A typical single-phase to ground (SFG) fault is simulated, where the phase voltage in phase 'A' decreased to zero. Fig.14 shows the simulated waveforms for the source side voltages, the load voltages and the injected voltages of DVR when single-phase to ground fault occurs. It can be observed that the load side voltages are harmonic-free and sinusoidal waveforms are guaranteed.

It can be concluded from the simulation results of the three typical voltage sag scenarios that, the completely symmetrical load terminal voltages can be ensured without noticeable transient problem when the DVR is used for voltage sag mitigation purposes. And the DVR can not only compensate positive-sequence but also compensates negative-sequence and harmonic components in the grid voltages, thus pure sinusoidal waveforms are ensured at the load side.

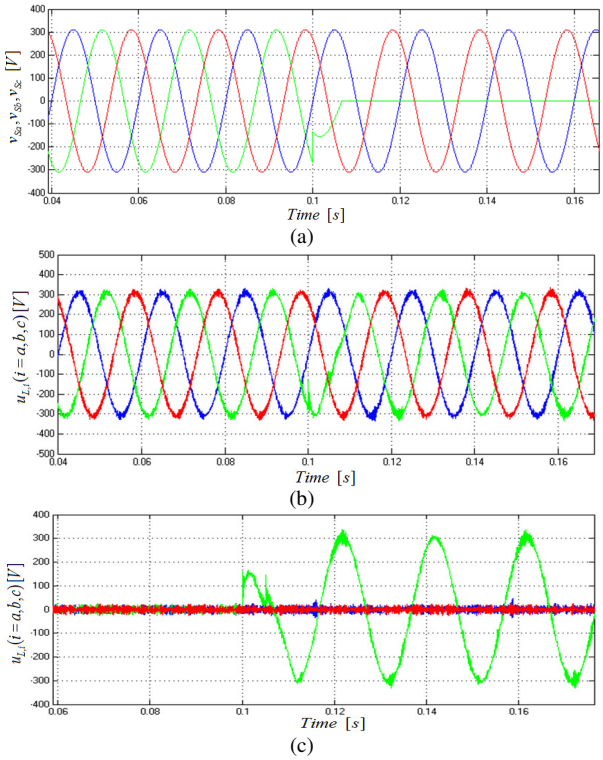


Figure 14. The simulated waveforms of the source voltages, load voltages, and the injection voltages of DVR when single-phase fault occurs (case 3). (a) The grid voltages; (b). The load side voltages; (c). The compensation voltages.

5 Conclusion

The dynamic voltage restorer (DVR) is considered as the best choice to protect the industrial facilities from voltage sag and other utility voltage disturbances. This paper aims to propose an effective control algorithm for the DVR for voltage mitigation in the distribution utilities. The control scheme of the DVR is presented, which includes the grid-synchronization algorithm based on the double reference frame PLL (DSRF-PLL), the reference compensation voltages generation, the shunt converter control algorithm and the series inverter control algorithm.

It is found that the double synchronous rotating reference frame PLL (DSRF-PLL) is effective to detect the positive-sequence fundamental component of grid voltages in case of severe voltage unbalanced and/or distortion. Meanwhile, an effective control algorithm is proposed by using the proportional resonant (PR) controllers in the current loop of voltage source rectifier, which provides infinite controller gain at the selected harmonic frequencies to guarantee a high accuracy. The simulation results under three voltage sag scenarios are presented, which demonstrates that the DVR is capable of compensating both balanced and unbalanced grid voltage sag, as well as the harmonic contamination in the grid voltage. The validity and effectiveness of the devised control algorithms are confirmed by the simulation results.

REFERENCES

[1] T. Fabio, Q. Stefano, "Power quality enhancing in distribution utilities," *Elektrotehniski Vestnik* / Electrotechnical Review, Vol.68, No.5, pp.271-276, 2001.

[2] J. Godsk Nielsen, F. Blaabjerg, "A Detailed Comparison of System Topologies for Dynamic Voltage Restorers," *IEEE Trans. Ind. Applicat.,* vol. 41, no.5, Sep/Oct. 2005.

[3] J. G. Nielsen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump," in *Proc. IEEE APEC'01*, vol. 2, 2001, pp. 1267–1273.

[4] J. G. Nielsen, M. Newman, H. Nielsen, and F. Blaabjerg, "Control and testing of a dynamic voltage restorer (DVR) at medium voltage level," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 806–813, May 2004.

[5] C. Fitzer, M. Barnes, P. Green, "Voltage sag detection technique for a dynamic voltage restorer," *IEEE Trans. Ind. Applicat.,* vol. 40, no.1, Jan. 2004.

[6] Q. Stefano, T. Fabio, "The voltage sags matrix: A useful tool for power quality analysis," *Elektrotehniski Vestnik* / Electrotechnical Review, Vol.69, No.3-4, pp.171-174, 2002.

[7] M. Rok, Z. A., "A polyphase DSP-based electricity measurement system a with network analyzer," *Elektrotehniski Vestnik* / Electrotechnical Review, Vol.76, No.1-2, pp.1-6, 2009.

[8] T. Fabio, Q. Stefano, "Equipment fault-clearing time reduction: An approach to utility voltage sag mitigation," *Elektrotehniski Vestnik* / Electrotechnical Review, Vol.67, No.5, pp.294-299, 2000.

[9] Q. Stefano, C. Simone, "Impact of limiting reactors for voltage sag mitigation in distribution utilities," *Elektrotehniski Vestnik* / Electrotechnical Review, Vol.71, No.5, pp.301-307, 2004.

[10] S. Lee, H. Kim, S. K. Sul, and F. Blaabjerg, "A novel control algorithm for static series compensation by use of PQR instantaneous power theory," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 814–827, May 2004.

[11] P. Rodriguez, J. Pou, J. Bergas, "Decoupled Double Synchronous Reference Frame PLL for Power Converters Control," *IEEE Trans. Power Electron.,* vol. 22, no.2, Mar. 2007.

Lin Xu received the B. E. degree in electrical engineering from University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2006, and received the Ph.D. degree in electrical engineering from Shanghai JiaoTong University (SJTU), Shanghai, China, in 2011. Currently, she is working at Sichuan Electric Power Research Institute, Chengdu, China. Her research interests include power system analysis and real-time digital simulator (RTDS), flexible Ac transmission systems (FACTS), such as TCSCs, STATCOMs, and power quality conditioners (DVRs, APFs). She is an active reviewer for the IEEE Transactions on Industrial Electronics, IEEE Transactions on Power Electronics, Electric Power Components and Systems, etc.

Yang Han (S'08–M'10) received the B. E. degree in electrical engineering from University of Electronic Science and Technology of China (UESTC), Chengdu, P. R. China. He received the Ph. D. degree in electrical engineering from Shanghai JiaoTong University (SJTU), Shanghai, China, in 2010. He is a member of the IEEE Industrial Electronics Society and IEEE Power Electronics Society. He is a Senior Member of China Power Supply Society (CPSS), a member of the Chinese Society for Electrical Engineering (CSEE). He is a member of the organizing committee of the 2011 International Conference on Electric Information and Control Engineering (ICEICE). He is an active reviewer for the IEEE Transactions on Industrial Electronics, IEEE Transactions on Power Electronics, Electric Power Components and Systems, European Transactions on Electrical Power and International Journal of Electronics.

Currently, he is with the Univerity of Electronic Science and Technology of China (UESTC), Chengdu, China. He is the editors of many international journals: *Trends in Electrical Engineering*, *Journal of Power Electronics & Power Systems*, *Indonesian Journal of Electrical Engineering*, *International Journal of Power Electronics and Drive Systems* (*IJPEDS*). His research interests include power system analysis and simulation, power quality conditioners, voltage source inverters and multilevel converters for static var compensations (STATCOMs) and active power filters (APF) applications.