TESTABILITY ISSUES OF SYSTEM-ON-CHIP DESIGN

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Keywords: microelectronics, SOC, System-On-Chip, SECT IEEE P1500, Standards for Embedded Core Test, design, testability, IC, integrated circuits, embedded cores, core wrapper, computer languages, CTL, Core Test Languages, testing strategies, TAM, Test Access Mechanisms, STAM, Serial Test Access Mechanisms, Automatic Test Equipment, BIST, Built-In Self-Test, STIL IEEE P1450, Standards Test Interface Language IEEE P1450, WIP, Wrapper Interface Port, WIR, Wrapper Instruction Registers, WBR, Wrapper Boundary Registers

Abstract: The paper describes current trends in standardisation of design-for-testability approaches for complex circuits with embedded cores also referred to as system-on-chip. The concept of core wrapper and the corresponding core test language, the main two issues of the forthcoming IEEE P1500 Standard, are briefly introduced. Possible strategies for test integration of cores conforming to the standard are discussed. References to the available IEEE P1500 Standard documents and papers are given. The goal of the paper was to enlighten the issues that may be of most interest to a potential user/designer in the applications of our national electronic industry.

Upoštevanje zmožnosti testiranja pri načrtovanju sistema-v-čipu

Ključne besede: mikroelektronika, SOC sistem-v-chip-u, SECT IEEE P1500 standardi za preskušanje jeder vgrajeno, snovanje, preskusljivost, IC vezja integrirana, jedra namenska, ovoj jedra testni, jeziki računalniški, CTL jeziki za opis preskušanja jeder, strategije preskušanja, TAM mehanizmi dostopa za testiranje, STAM mehanizmi dostopa za preskušanje serijski, ATE oprema za preskuse avtomatska, BIST preskušanje vgrajeno vase, STIL IEEE P1450 standardi za jezik preskuševalni vmesniški, WIP vrata ovoja vmesnika, WIR registri ovoja inštrukcijski, WBR registri ovoja mejni

Povzetek: V članku opisujemo sedanje smeri razvoja standardizacije postopkov načrtovanja zmožnosti testiranja kompleksnih vezij z vgrajenimi namenskimi jedri, imenovanih tudi sistem-v-čipu. Na kratko sta opisana zasnova testnega ovoja jedra in jezik za opis testiranja jeder, ki predstavljata glavni značilnosti prihajajočega standarda IEEE P1500. Opisane so strategije povezovanja jeder, ki ustrezajo standardu, v sistem, ki ga bo možno učinkovito testirati. Navedene so reference na dokumente o standardu IEEE P1500 dosegljive preko spletne strani delovne skupine ter objavljene članke in referate. Cilj prispevka je osvetliti tiste vidike standarda, ki bi bili najzanimivejši za potencialnega uporabnika/načrtovalca v aplikacijah domače elektronske industrije.

1 Introduction

Recent technology advances allow to integrate functions that have been traditionally implemented on one or more complex printed circuit boards into one single IC, often referred to as system-on-chip (SOC). The development of this new class of ICs is based on the design technique which integrates large reusable blocks (i.e. cores) that have been designed and verified in earlier applications in practice, /1/. A core may be soft, firm or hard, /1/-/4/. A *soft* core is a synthesizable register-transfer level code of a logic block. It allows much flexibility to the designer and can be realised by different technological processes. A *hard* core consists of a technology-dependent layout and lacks flexibility since it has been optimised for a given performance requirements. A *firm* core contains a gate-level netlist that is ready for placement and routing and thus represents a compromise between the two. Embedded cores provide a wide range of functions, like CPUs, DSPs, interfaces, controllers, memories, and others. The advantage of embedding reusable cores in the design of a new product is a shortened design cycle resulting in reduced time-to-market and reduced cost.

The design of a complex system-on-chip normally requires expertise in different technology areas which is difficult to find in a single design house. Consequently, embedded-core design involves two parties: *core providers* and *core users*. In most cases, the core user (i.e., system integrator) does not have the knowledge about the design of the building blocks (cores). It is neither the interest of core providers to reveal design and implementation details in order to protect their intellectual property. However, the core user is responsible for manufacturing and testing the whole system-on-chip including cores, interconnect logic and possible additional user-designed logic. Complexity of the design and limited knowledge about implementation of cores make the problem of SOC testing rather challenging to the core user. The problem could only be adequately handled by involving both core providers and core users in a joint effort to develop efficient test solutions. In order to provide an independent openly defined design-for-testability method for integrated circuits containing embedded cores, an initiative to develop a standard has been taken by the IEEE P1500 Working Group, /6/.

2 Testing of core-based chips

The SOC designer (core user) has limited knowledge about the adopted cores and he cannot develop adequate tests for them. The core providers need to provide tests for the cores and all the necessary information (i.e., test patterns, timing and protocol description). A SOC normally consists

of cores from different providers and the integration of different core tests into a composite SOC test may become a difficult job because of the diversity of descriptions and test implementation details. Core internal tests need to be described in a commonly accepted way. The forthcoming IEEE P1500 standard defines standard format (i.e., Core Test Language) for the description of core test /6/.

Conventional production test of assembled boards consists of a sequence of separate component tests, bare board test, static test of assembled board (detecting shorts and opens) and dynamic functional test (detecting timing faults). In the case of testing SOC, all the above tests are merged into one composite test instance. Furthermore, in most cases direct access to the core terminals is not provided which makes it difficult to run internal tests of deeply embedded cores. The principle of embedded core testing is presented in terms of conceptual test architecture /3/ consisting of *test pattern source* and *sink*, *test access mechanism* (TAM) and *core test wrapper* (Figure 1). In order to test a core, a test source (i.e., test pattern generator) generating test stimuli and a test sink (i.e., response compactors, current monitors, etc.) collecting the test responses must be provided. Test access mechanism transports test patterns from the source to the core and test responses from the core to the test sink. Finally, the core test wrapper, a thin shell around the core, provides interface between the embedded core and its environment. It connects the terminals of the core to the rest of SOC (in the normal mode) and to the test access mechanism (in the test mode). The IEEE P1500 Standard defines the structure and the operation of the test wrapper /6/.

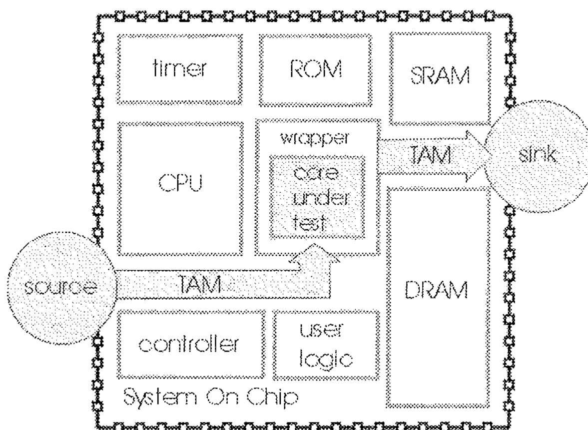

Figure 1: Embedded core testing involves source, sink, TAM and wrapper

The described test architecture is implemented in various ways depending on the type of the core (i.e., logic, memory, analog or mixed-signal), type of pre-defined tests provided by the core vendor, and required test quality. For example, test patterns can be generated by external automatic-test-equipment (ATE) or built-in self-test (BIST) logic implemented in SOC. Likewise, test results can be evaluated by external ATE or compressed to a signature and compared to a reference value by the BIST logic on SOC. More details on this are given in Zorian *et al.* /3/.

3 IEEE P1500 Standard for Embedded Core Test (SECT)

Activities on IEEE P1500 SECT started in 1995, and have been officially approved by the IEEE Standards Activities Board in 1997. The work currently focuses on a standard for testing digital logic and memory cores, future extensions will include also analog and mixed-signal cores. The mission statement defines the following scope /6/:

"This project will develop a standard test method for Integrated Circuits containing embedded cores, i.e. reusable megacells. This method will be independent of the underlying functionality of the Integrated Circuit or its individual embedded cores. The method will create the necessary testability requirements for detection and diagnosis of such integrated Circuits, while allowing for ease of interoperability of cores originated from distinct sources. This method will be usable for all classes of digital cores including hierarchical ones."

The two primary issues are to provide means for (1) efficient core test knowledge transfer, and (2) the test access to the embedded cores. Accordingly, the standard defines (1) a language for the description of the test-related information for the cores embedded in the SOC, and (2) the test wrapper architecture of the embedded core. The work on the standard has progressed to the draft version IEEE P1500/D0.3 and aims to be ready for ballot in 2001 /6/.

3.1 Core test language

IEEE P1500 SECT defines the Core Test Language (CTL) in order to facilitate the transfer of the core test-related information from the core provider to the core user. CTL uses the syntax of IEEE 1450, Standard Test Interface Language (STIL), /7/, and describes test information including test data, test methodology, core configurations and necessary connectivity information for system integration. The objective is to provide all the necessary information for the implementation of core wrapper including the description of core signals, timing, electrical characteristics, core external connections, protocol for applying test patterns to the core terminals, etc. Detailed description of CTL is beyond the scope of this paper. Interested readers can find more information on this subject together with an illustrative example describing the way of transforming a bare core into a 1500-compliant core in /4/.

3.2 Core test wrapper

Test wrapper is a thin shell around the core and serves as an interface between the core and the test access mechanism(s). During normal operation, wrapper connects core inputs and outputs to SOC functional wires. For testing purposes, wrapper has modes in which core inputs

and outputs are connected to a mandatory serial TAM (one-bit wide) and optional scalable parallel TAMs which provide access for core-internal and core-external tests. Wrapper operation is controlled by a set of control and clock signals provided at the Wrapper Interface Port (WIP). WIP also includes serial scan terminals WSI and WSO which are used to shift-in and shift-out serial test data. (The function of WSI and WSO is similar to TDI and TDO terminals of IEEE 1149.1, digital boundary-scan architecture /8/). Test wrapper contains the following mandatory registers:

- *wrapper instruction register* (WIR) which is similar to IEEE 1149.1 instruction register and controls the operation of the wrapper. WIR receives instructions via wrapper serial input WSI.
- *wrapper boundary register* (WBR) to which the core functional terminals are connected. It is a serial shift register similar to the IEEE 1149.1 boundary-scan register.
- One-bit *bypass register* which is similar to IEEE 1149.1 bypass register. It is used to bypass the WBR. In a single scan path configuration, where WSI and WSO terminals of cores are connected in series, it may become inconvenient to shift data through the entire sequence of WBRs. Bypass registers enable to skip out the WBRs of the cores that are not being tested.

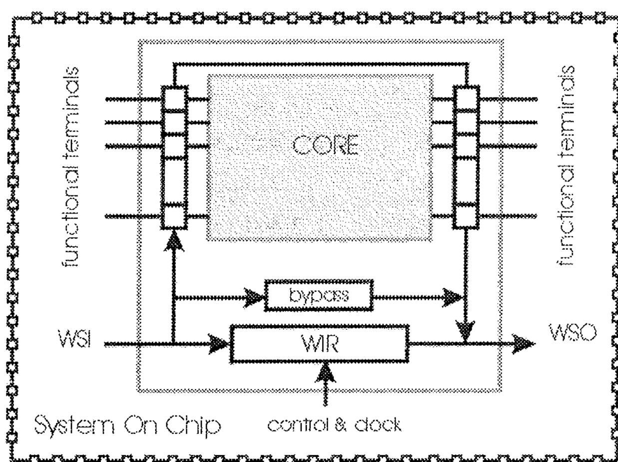

Figure 2: Test wrapper structure

Serial TAM and (if available) parallel TAMs provide means for performing core-internal and core-external tests. Core-internal test is based on the test information that the core user gets from the core provider. It may consist of the application of test patterns within a specified test protocol, or of initiation of a built-in self-test of the core. Core-external test checks external connections between the cores and additional glue logic designed by the SOC integrator.

For the core-internal tests, test stimuli are provided via TAM to wrapper boundary at the core input terminals and test results are read via TAM from the wrapper boundary at the core output terminals. For the core-external tests, initial logical values are set-up via TAM at the wrapper boundary at the core output terminals and results are observed at the wrapper boundary at the core input terminals.

4 Possible test configurations

From the conceptual point of view one may notice several points of similarity between IEEE P1500 SECT and IEEE 1149.1. For example, wrapper registers WIR, WBR and bypass have similar role as instruction, boundary-scan and bypass register in IEEE 1149.1. Furthermore, as mentioned above, the function of WSI and WSO is similar to TDI and TDO in digital boundary-scan architecture. But there are also substantial differences: the operation of the TAP Controller which is the "heart" of the IEEE 1149.1 compliant circuit is given by the state diagram which unambiguously defines the test protocol - on the other hand, IEEE P1500 SECT does not define the operation of the test wrapper by a state diagram, and allows the designer of a test wrapper a lot of freedom.

SOC integrator can choose different strategies of implementing STAM and parallel TAMs of individual wrappers depending on the complexity of core-internal tests, the amount of additional user defined logic, overall complexity of the SOC and on the conditions imposed by the available ATE that will be used in production test. For example, for a core with a built-in self-test it may be sufficient to provide test wrapper only with STAM. On the other hand, some other core may need extensive amount of test patterns that can only be transferred in reasonable time via parallel TAM. Wrappers can be connected in different configurations (i.e., multiplexing, daisychain, etc.) differing in test time, wiring and SOC performance. Besides, possible implementation of boundary-scan at the level of individual cores and requirements for its implementation at the level of SOC will impact the selection of wrapper test features and system level core configurations. Effective combination of IEEE 1149.1 and IEEE P1500 SECT infrastructure in SOC test is an interesting problem in practice.

5 Conclusion

SOC testing is one of the current hot topics in the field of electronic test. Several papers and vivid discussions at recent European Test Conference /9/ confirm the importance of providing efficient solutions to the problem of testing embedded cores integrated in a complex SOC. In the paper, the basic approach to testing SOC formalised in IEEE P1500 SECT is described. Another issue concerns intellectual property of core providers. Due to the opposite interests of core providers and core users regarding the level of the core implementation details that should be revealed to the user (making SOC testing easier) the problem of information transfer remains a challenge for both participating parties. Here again, IEEE P1500 SECT offers means that may help them in achieving a reasonable solution.

Finally one could ask: what consequences will the forthcoming IEEE P1500 SECT have to those users that do not produce complex SOC but rather use them in their products? We can expect from the SOCs producers to provide some information related to testing embedded cores in a SOC for the purpose of debugging and for performing system functional test. Besides, cores including scalable test wrapper are likely to become a standard product on the market, ready for integration as well in simple electronic systems (e.g., intelligent sensors) which makes the IEEE P1500 SECT interesting to a broader group of potential users.

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Prispelo (Arrived): 18.05.01 *Sprejeto (Accepted): 01.06.01*