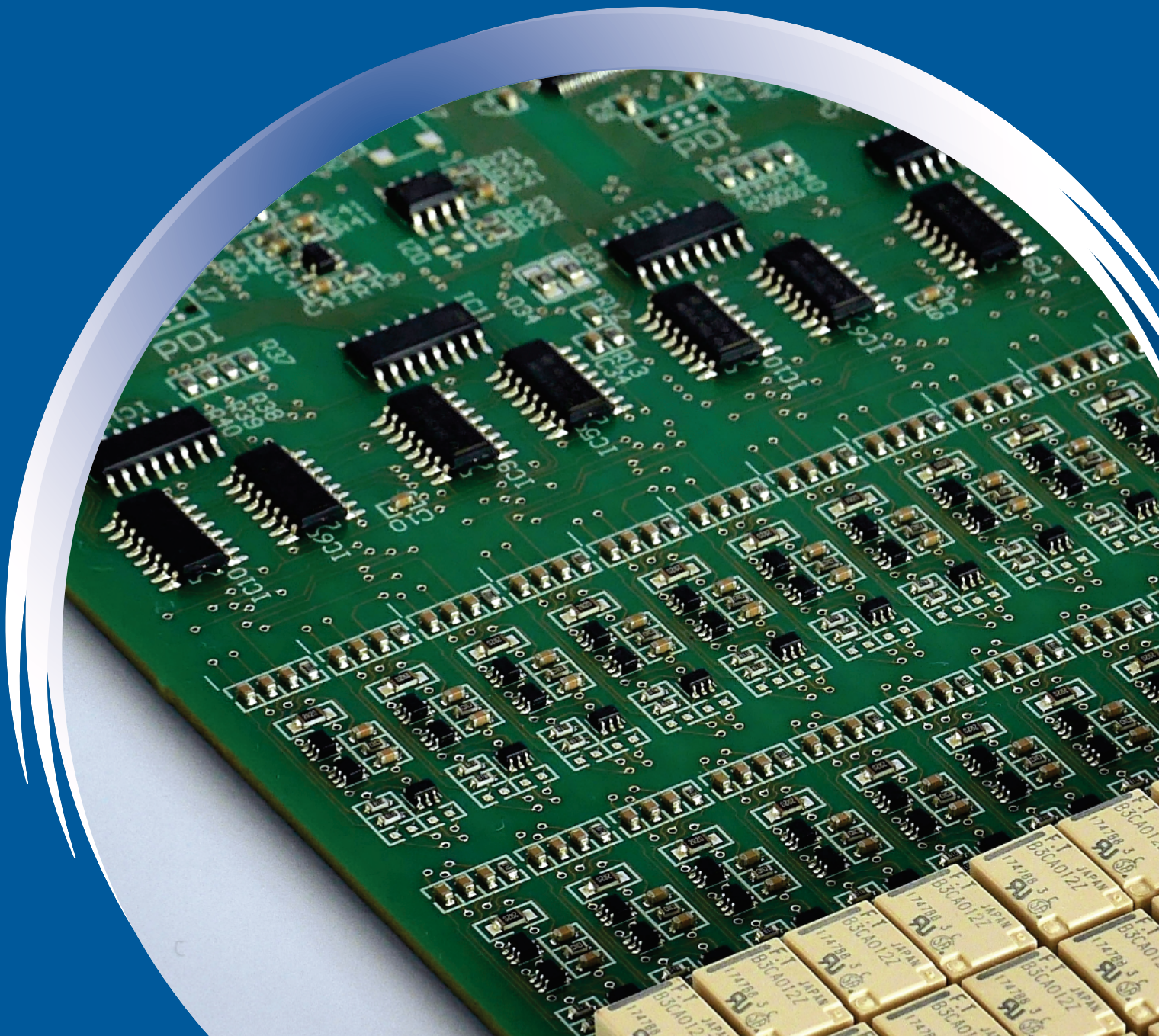
ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 53, No. 1(2023), March 2023

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 53, številka 1(2023), Marec 2023



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *1-2023*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 53, NO. 1(185), LJUBLJANA, MARCH 2023 | LETNIK 53, NO. 1(185), LJUBLJANA, MAREC 2023

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Headquarters | Naslov uredništva
Uredništvo Informacije MIDEM
MIDEM pri MIKROIKS
Stegne 11, 1521 Ljubljana, Slovenia
T. +386 (0)1 513 37 68
F. + 386 (0)1 513 37 71
E. info@midem-drustvo.si
www.midem-drustvo.si

Annual subscription rate is 160 EUR, separate issue is 40 EUR. MIDEM members and Society sponsors receive current issues for free. Scientific Council for Technical Sciences of Slovenian Research Agency has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials. Publishing of the Journal is cofinanced by Slovenian Research Agency and by Society sponsors. Scientific and professional papers published in the journal are indexed and abstracted in COBISS and INSPEC databases. The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™. |
Letna naročnina je 160 EUR, cena posamezne številke pa 40 EUR. Člani in sponzorji MIDEM prejemajo posamezne številke brezplačno. Znanstveni svet za tehnične vede je podal pozitivno mnenje o reviji kot znanstveno-strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinancirajo ARRS in sponzorji društva. Znanstveno-strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC. Prispevke iz revije zajema ISI® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™.

Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 53, No. 1(2023)

Content | Vsebina

Original scientific papers | Izvirni znanstveni članki

Original scientific paper
https://doi.org/10.33180/InfMIDEM2023.101

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 53, No. 1(2023), 3 – 13

Design and comparative analysis of Inter Satellite- Optical Wireless Communication (IS-OWC) for Return to Zero (RZ) & Non-Return to Zero (NRZ) modulation formats through channel diversity technique

Nirmal Jothi[1], Santhana Krishnan[2], Lakshminarayanan[3]

[1]Department of Electronics and Communication Engineering, Vel Tech Rangarajan, Dr.Sagunthala R&D Institute of science and technology, Tamilnadu, India
[2]Department of Electronics and Communication Engineering, SCAD College of Engineering and technology, Tirunelveli, Tamilnadu, India
[3]Department of Electronics and Communication Engineering, Francis Xavier Engineering College, Tirunelveli, Tamilnadu, India

Abstract: Inter-Satellite Optical Wireless Communication (IS-OWC) is a novel strategy for establishing an inter-connection between two satellites. The IS-OWC is focused on the use of lasers rather than conventional radio and microwave structures for wireless optical communication. Optical wireless communication between satel-lites is being developed by integrating optical wireless communication technology and space technology. IS-OWC can connect satellites in the same orbit or different orbits. When compared to the single channel, the channel diversity strategy produces better results. The channel diversity techniques use the IS-OWC devices, in which several signal paths are available for allowing the Q factor and signal intensity, which is extended or en-larged over a large distance. In this paper, the Q factor and Bit Error Rate (BER) are reviewed with diverse mod-ulation designs for Return to Zero (RZ) and Non-Return to Zero (NRZ) using the channel diversity technique. The simulation is conducted on opti-system-16.0 software with 32768 numbers of samples with a bit rate of 109 bits/ sec. The Q factor attained a maximum in the 8-channel OWC is 19.4385, whereas the Q factor attained min-imum in the 2-channel OWC is 19.4385. Moreover, the number of channels increased may develop the profi-ciency of minimum power inter-satellite relation.

Keywords: Optical Wireless Communication (OWC), BER, Q-factor, Return to Zero (RZ), Non-Return to Zero (NRZ).

Zasnova in primerjalna analiza medsatelitsko-optičnih brezžičnih komunikacij (IS-OWC) za modulacijske formate povratek v ničlo (RZ) in nepovratek v ničlo (NRZ) s tehniko kanalske raznolikosti

Izvleček: Medsatelitska optična brezžična komunikacija (IS-OWC) je nova strategija za vzpostavitev medsebojne povezave med dvema satelitoma. IS-OWC se osredotoča na uporabo laserjev namesto običajnih radijskih in mikrovalovnih struktur za brezžično optično komunikacijo. Optična brezžična komunikacija med sateliti se razvija s povezovanjem tehnologije optične brezžične komunikacije in vesoljske tehnologije. IS-OWC lahko povezuje satelite v isti orbiti ali različnih orbitah. V primerjavi z enim kanalom daje strategija raznolikosti kanalov boljše rezultate. Tehnike kanalske raznolikosti uporabljajo naprave IS-OWC, v katerih je na voljo več signalnih poti za omogočanje faktorja Q in intenzivnosti signala, ki se poveča na veliki razdalji. V tem članku sta raziskana faktor Q in stopnja napake v bitu (BER) z različnimi modulacijskimi zasnovami za vrnitev v nič (RZ) in brez vrnitve v nič (NRZ) z uporabo tehnike kanalske raznolikosti. Simulacija je izvedena s programsko opremo opti-system-16.0 s 32768 vzorci s hitrostjo prenosa 109 bitov na sekundo. Faktor Q, dosežen pri 8-kanalnem OWC, je 19,4385, medtem ko je faktor Q, dosežen pri 2-kanalnem OWC, 19,4385. Poleg tega se lahko s povečanjem števila kana-lov razvije spretnost najmanjše moči medsatelitskega razmerja.

Ključne besede: Optične brezžične komunikacije (OWC), BER, faktor Q, povratek v ničlo (RZ), nepovratek v ničlo (NRZ).

** Corresponding Author's e-mail: drnj2023@gmail.com*

How to cite:
N. Jothi et al., "Design and comparative analysis of Inter Satellite- Optical Wireless Communication (IS-OWC) for Return to Zero (RZ) & Non-Return to Zero (NRZ) modulation formats through channel diversity techniqu", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 53, No. 1(2023), pp. 3–13

1 Introduction

With the utilization of satellite communication short-ly, the optical wireless communication mode has undoubtedly evolved. Individual OWC systems have standards due to their outstanding performance [1]. The IS-OWC systems performance multiplexing techniques are used with extended distance trans-mission. The inter-satellite link of 10 Gbit/s data rate has modelled with 5000 kilometres of communica-tion range [2, 3]. Therefore, the validation of com-parative analysis shows that the RZ and NRZ model modulation are changing input power stages [4]. The lightwave system preserves a high data rate for the upcoming generations, and the data rate can grasp user capacity [5]. The network configuration has high speed due to the minimal linear and non-linear distortions by increasing the demand of assert lookup for robust networks. In the case of optical fibers, chromatic diffusion and polarization mode diffusion comprise linear and nonlinear damage such as self and cross-phase modulation and so on. [6, 7]. It is necessary to avoid the optimal modula-tion design by the narrow optical spectrum and not to resist excessive distortion by improving spatial performance.

The self-phase and cross-phase modulation with the constant optical power modulation format is a smaller amount of susceptible [8]. The amplified spontaneous emission (ASE) in case of long haul optical network, noise enters the image that may reduce and choose the optimum modulation format. The modulation format plays a vital role in commu-nication [9]. Microwave communication system for satellite communication is important assistance over the optical wireless communication (OWC) system is occupied with the communication world in huge applications [10]. The minimum power consumption and extensive distance transmission application are set by the low-cost landmark function in the OWC system and it is tough to organize the extended fiber optic cables [11, 12]. Thus, the effectiveness of the satellite application of the IS-OWC system is compatible with communication training. The com-munication system is needed to overcome better efficiency in erroneous transmission, power con-straints and noise.

The goal of every link involving a communications satellite is to provide the highest-quality signal with the least amount of bandwidth and power while utilising the most suitable technology. In a small-satellite constellation system, the design decreases the system's complexity and implementation costs, lowers the necessary transmission power, which improves the signal-to-noise ratio, and condenses the frequency spectrum. The Starlink satellite broadband communications network created by American company SpaceX is evaluated in this paper. The key technical features of this particular area of broadband communications networking based on constellations of tiny satellites are exam-ined and discussed. The paper's primary goal is to demonstrate the technical details of the Starlink network that SpaceX withholds in popular-science presentations [13].

IS-OWC system is the adaption of wireless technolo-gy in the modern period. Present microwave satel-lite systems in maximum bandwidth, minimum size, and least power demand offered by the IS-OWC system [14]. The RF signal is compared with the laser signal providing lower loss. Lasers are associ-ated with the RF wavelength [15]. Joining altered positions on the earth's surface is a fascinating ob-jective. The earth station and satellite are establish-ing a network. Consequently, an inter-satellite link (ISL) contains the energetic influence under the optimal communication implication [16]. Owing to propagation loss being weighty, the time lag in extensive transmission for Geo stationary Earth Orbit (GEO). The globular link and communication function are extremely desirable for the Low Earth Orbit (LEO) as well as Medium Earth Orbit (MEO) satellites [17]. Two satellites in IS-OWC technology act as transmitters and receivers at the propagation chan-nel. The tracking system's highly accurate signal is required for beacon signal and quadrant detector with connected satellite, which makes sure that the tracking system, has orientation and correct line of sight (LOS) [18]. The major problem of the system is closed-loop tracking. Servo motors are addressing the problem and blocking the beacon signals on satellites. The other satellites are expanding the ephemeris data to accurately pinpoint and track the other satellites [19]. The IS-OWC system develops link distance into the modulation system that is uti-lized for input power level, operation wavelength, receiver sensitivity, and diversity methods. Some of the techniques are used to compensate for the ef-fects that damage the link efficiency [20, 21]. The minimum BER is obtained by the ISL link; a low transmitter divergence is utilized for delivering the greatest power level on the receiver side and re-moves that difficulty in power degeneracy.

Any two satellites in this connection are used for IS-OWC if the satellite is in a similar orbit or dissimilar orbit. The most common orbits used by the satellite are LEO, MEO and geostationary earth orbit. On the other hand, the tracking system is highly accurate and it is used for the beacon signals on the hand and quadrant detector. The accurate line of sight has aligned and ensures that the linked satellite is prop-agative. The light travels at 3 x 108 m/s in data that can send without delay and attenuation. The maxi-mum speed of data is transmitted over thousands of kilometres with minor payload with radio frequency (RF) links over the benefits of optical links.

The main contributions of this manuscript are summarized below,

- In this manuscript, the design and compara-tive analysis of the IS-OWC for RZ and NRZ modulation formats through channel diver-sity techniques are proposed.
- The IS-OWC is concerned through the em-ployment of lasers based on traditional ra-dio and microwave systems for the OWC.
- When compared to the single channel, the channel diversity strategy produces better results.
- The IS-OWC device uses a diversity tech-nique, in which several signal paths are available, allowing the Q-factor and signal intensity to be extended or increased over a large distance.
- In this manuscript, the Q-factor with BER is estimated with diverse modulation formats, like RZ and NRZ using the channel diversity technique.
- Here, a channel variety strategy with multi-ple transmitter and receiver antennas is used to investigate the results for various types of adjustment techniques in NRZ and RZ.
- Finally, the experiment is simulated with optisystem-16.0 software. The proposed system is simulated using 32768 numbers samples with a bit rate of 109 bits/sec.

The rest of this manuscript is structured as: Section 2 describes the literature review of various research papers associated with IS-OWC for channel diversity schemes. Section 3 illustrates the proposed IS-OWC for RZ and NRZ modulation through the channel diversity technique. Section 4 demonstrates the experimental outcomes and discussion of the pro-posed method. At last, section 5 concludes the manuscript.

2 Related Work

Among the various research works on the IS-OWC for channel diversity techniques, some of the most recent works are reviewed here,

In 2020, Singh et al [22] presented the 3D orthogonal modulation scheme by incorporating the band-width-efficient with a high-speed IS-OWC link. Here, three autonomous 40 Gbit/s information signals were sent on a similar wavelength channel that was modulated through the parameters of the various signals of the optical carrier. The IS-OWC link effi-ciency of the presented method has been re-searched for growing point errors with simulation results showing that the presented IS-OWC link was extended until the link distance was 16,000 in the effect of pointing error was 3.5 with satisfactory BER.

In 2018, Sharma et al [23] presented wireless com-munication in the dynamic field of IS-OWC. In nu-merous counts of channels under the structure, the Q factor value maximizes as the count of channels maximizes with minimized BER value. In the signal received as dissimilar routes, the strength and ca-pacity of the signal increase with numerous counts of the channel have numerous counts of transmitter and receiver antenna. The performance of the pro-posed method improved the low power and in-creased the count of channels.

In 2018, Khichar et al [24] presented the IS-OWC system in filter and amplifier diversity techniques utilized for data transmission. The diversity tech-nique of higher Q factor and improved bit rate was suggested with noise power separation and re-ceived noise power amplification. A wavelength of 1550 nm was the modulation of NRZ. The system has 30 dBm input power with a 7000 km link distance over the 40 Gbit/s has improved the data rate. For additional development, under link distance and system data rate were evaluated.

In 2020, Sivakumar et al [25] presented the DSP algorithm to improve the link range with the coherent detection technique for the IS-OWC system based on high-speed single channel PDM-QPSK. Here, the presented method performance in the influence of receiver pointing error with OSNR system demand to achieve the acceptable level of BER maximizes the pointing error angle increases. An efficient IS-OWC transmission system with long-distance and high-speed bandwidth is used.

In 2019, Sri et al [26] presented the revolutionary technique in IS-OWC that establishes genuine com-munication. Here, the RF satellite links in the knowledge transmit with a similar speed of around Mbps. Therefore, reaching the highest knowledge rate in optical links for homes over optical lasers (OLs) is necessary for exploitation. The light beam from the OLs offers less probability for detective work, interrupting with diminishing the possibility of electronic signal congestion. OISL systems were faster and safer information measures in the trans-mission of knowledge.

In 2018, Viswanath et al [27] presented that the transmitter power condition was comparatively greater for a greater value of turbulence at ground level. Here, the power demand for uplink was 8-10 dB as likened to downlink. In the event, that trans-mitter power was required for non-feasibility, it can be transported with possible level through trans-mitter spatial diversity or MISO approach for the receiver of uplink diversity or SIMO approach for downlink is aperture averaging. The practical rele-vance of the laser communications satellite launched into geostationary orbit, ground-satellite and satellite-ground links must be recognized.

In 2017, Pradhan et al [28] presented the IS-OWC system for space and polarization diversity methods. Here, 25 dBm input power and 7.63 Gbit/s data rate were achieved for the 6,000 km for link length. The diversity technique was polarized by the perfor-mance of system development also evaluated. The system can be evaluated by enhancing link distance with data rate.

3 Proposed methodology

All communication schemes involve a transmitter, propagation medium, and receiver. Two or more satellites are developed by an inter-satellite link that one satellite communicates with another using OWC. Both the satellite transmitter and receiver hold that monitoring system for decreasing signal misalignment. Here, the IS-OWC method with chan-nel diversity technique, a transmitter, a propagation medium and a receiver make up the IS-OWC system. And then the binary signal is generated by a pseu-do-random bit sequence (PRBS) that is converted into the electric signal, such as RZ and NRZ in pulse generators. In RZ and NRZ generators through carri-er signal (laser light) using modulator Mach - Zender (MZ) supports in modulating the voltage. With the help of a power combiner, the optical signal is propagated to the 1: N fork that provides independent signal copies with N number of OWC. An avalanche photodiode (APD) is utilized in the receiv-er for converting the optical domain signal with an electric signal. The redundant signal is filtered with Low Pass Bessel Filter (LPBF). For different modula-tion schemes, the BER analyzer performance is as-sessed based on the Q factor or BER. Figure 1 por-trays the IS-OWC block diagram method with the channel diversity technique.

3.1 Inter satellite-optical wireless communica-tion (IS-OWC)

This is utilized for the carrier signal to transmit the signal as laser light. The system is dependent on numerous limitations, such as laser light wave-length, transmitted power, modulation technique in different types, antenna size of the receiver and transmitted signal. The laser light signal is utilized to deliver wireless connectivity between the source and the destination. The free - space is the medium utilized here to take the message. The receiver sig-nal power level in the IS-OWC system is calculated [18] using equation (1)

$$Q_S = W_Q W_F S_F W_H S_H W_K S_K \left(\frac{\omega}{4\pi S}\right)^2 \quad (1)$$

Where QS represents the received power, WQ represents the transmitted power, WF describes the opti-cal

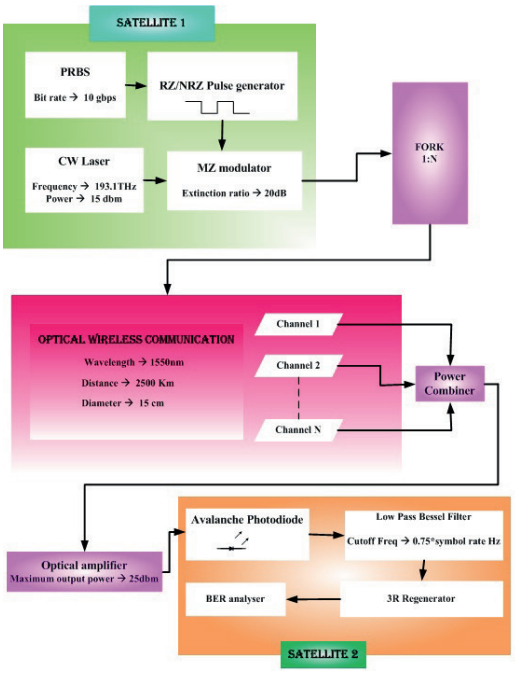


Figure 1: Block diagram of the IS-OWC method with the channel diversity technique.

performance of transmitter signal, SF describes that optical performance of receiver signal, WH de-notes that transmitter signal gain, SH denotes that receiver signal gain, WK indicates the transmitter pointing loss factor, SK indicates the receiver point-ing loss factor, ω represents the operational wave-length, S represents the link distance among the transmitter and receiver.

3.2 Flow chart

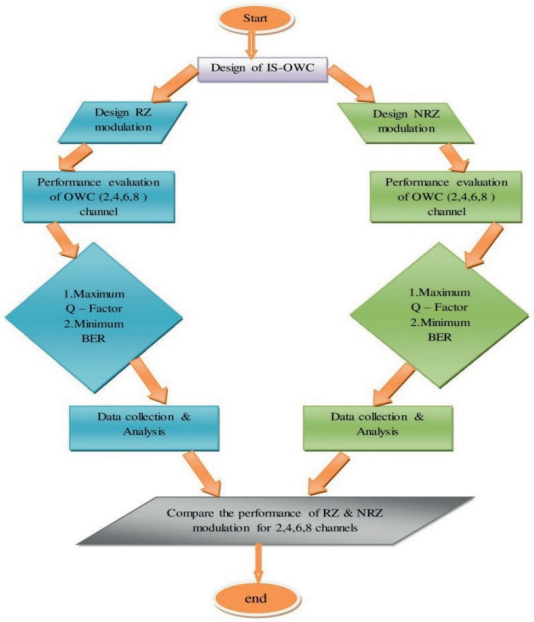


Figure 2: Flow chart of IS-OWC system using channel diversity technique

3.3 Return to zero modulation format

A pseudorandom pulse generator produces the information to be broadcasted in the structure of binary data and comprises the layout that desig-nates the transmitted segment. The binary data is served into a return to zero pulse generator, which converts it into the electrical pulses for transmission. RZ pulse generator output is directed to an MZ modulator. The MZ modulator modulates the elec-trical pulse through a continuous wave laser with 1,550 nm. The main use of the optical antenna is the optical signal output in the MZ modulator that is directed near the n-OWC channel. The IS-OWC link's receiving end consists of an optical receiving anten-na that receives the incoming signal. The signal is guided to a photodiode called APD that transforms the optical domain signal (ODS) into its electrical equivalent. A Bessel low-pass filter surveys the APD photodiode, and then high-frequency noise in the received signal is eliminated. The Q-factor, BER, and SNR of the received signal are calculated using the BER analyzer.

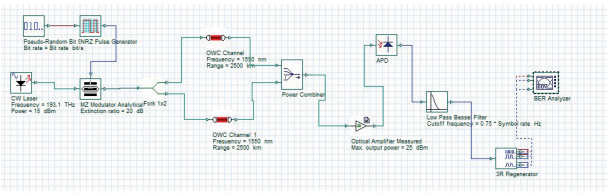


Figure 3: Layout diagram of 2-OWC

Figure 3 shows the layout diagram of 2 channels OWC for return to zero modulation. In this, the bina-ry signal is generated by the PRBS that is converted into an electric signal via pulse generator RZ. The MZ modulator helps modulate the voltage of the RZ generator through the carrier signal (laser light) extinction ratio of 20 dB. And then the carrier signal is converted into two channels with a frequency of 1550 nm and a range of 2500 km. With the help of a power combiner, the optical signal has been propa-gated to an optical amplifier measured with a max-imum output power of 25 dBm. An APD is used in the receiver for converting ODS with an electric signal. The redundant signal is filtered out using LPBF. For the modulation scheme, the performance of the BER analyzer rate is. 6.4925*10-015.

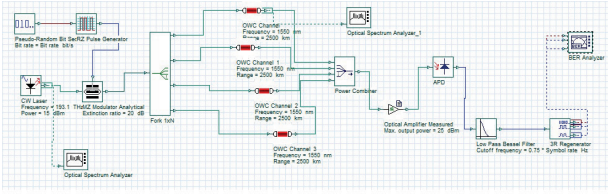


Figure 4: Layout diagram of 4-OWC

Figure 4 shows the layout diagram of 4 channels OWC for return to zero modulation. Here, the optical signal propagates with a 1: N fork that provides independent signal replicates with N number of OWC and the signal is converted into four channels with a frequency of 1550 nm and a range of 2500 km. For the modulation scheme, the performance of the BER analyzer rate is 1.96543*10-030.

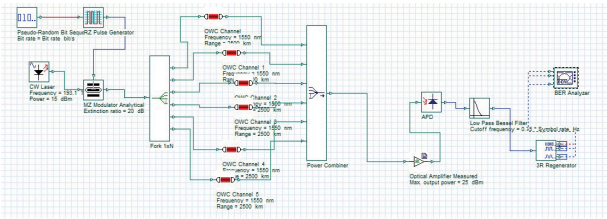


Figure 5: Layout diagram of 6-OWC

Figure 5 shows the layout diagram of 6 channels OWC for return to zero modulation. Here, the binary signal is generated through PRBS that is converted into an electric signal via pulse generator RZ. The MZ modulator helps in modulating the voltage of the RZ generator with carrier signal in the extinction ratio of 20 dB. For the modulation scheme, the per-formance of the BER analyzer rate is 8.58148*10-052.

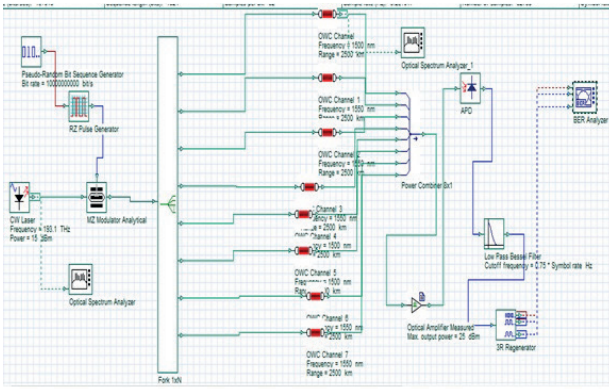


Figure 6: Layout diagram of 8-OWC

Figure 6 shows the layout diagram of 8 channels OWC for return to zero modulation. The optical sig-nal propagates with a 1: N fork that provides inde-pendent signal replicas with N number of OWC, and the signal is converted into eight channels with a frequency of 1550 nm and a range of 2500 km. By using the power combiner, the optical signal has been propagated to the optical amplifier measured with the maximum output power of 25 dBm. An APD is used in the receiver for converting ODS with an electric signal. The redundant signal is filtered using LPBF. For the modulation scheme, the performance of the BER analyzer rate is 3.29942*10-066.

3.4 Non return to zero modulation layouts

The binary signal is made by the PRBS that is transformed using an electrical signal via an NRZ pulse generator. The NRZ generator output is modulated by the carrier signal utilizing the MZ modulator, which is propagated optically to Fork 1: N, it pro-vides the N number of the optical wireless channel and separates the signal imitations utilizing the power combiner. An APD is used in the receiver for converting ODS with an electric signal. The removal of an unwanted signal is used by the LPBF. Then the use of the BER analyzer is a view of the results of the Q factor or BER form. The efficiency of the proposed method improves the number of channels, and transmitters and increases the receiver antenna.

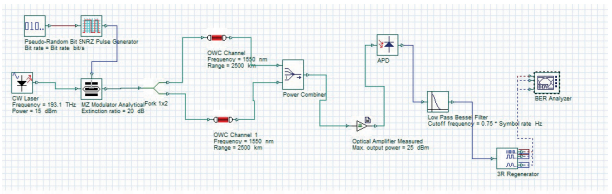


Figure 7: Layout diagram of 2-OWC

Figure 7 shows the layout diagram of 2 channels OWC for non-return to zero modulation. For the modulation scheme, the performance of the BER analyzer rate is 1.34606*10-020.

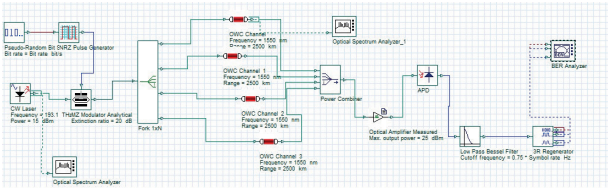


Figure 8: Layout diagram of 4-OWC

Figure 8 shows the layout diagram of 4 channels OWC for non-return to zero modulation. For the modulation scheme, the performance of the BER analyzer rate is 5.53168*10-044.

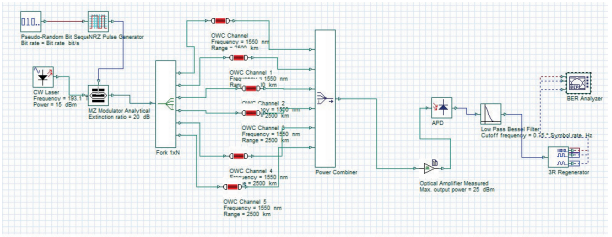


Figure 9: Layout diagram of 6-OWC

Figure 9 shows that the layouts diagram of 6 chan-nel OWC for non-return to zero modulation. For the modulation scheme, the performance of the BER analyzer rate is 8.86894*10-064.

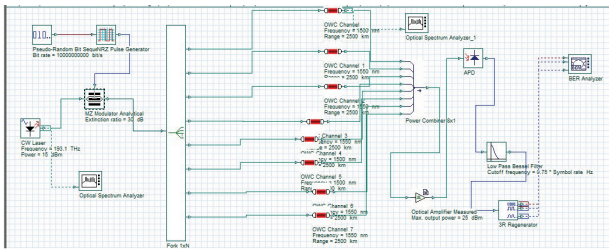


Figure 10: Layout diagram of 8-OWC

Figure 10 shows the layout diagram of 8 channels OWC for non-return to zero modulation. Here, the performance of the BER analyzer rate is 1.67178*10-088.

4 Results and discussion

This section describes the implementation of the experiment and carried out the details. The simula-tion is performed in opti-system-16.0 software. And the simulation parameters utilized under experi-ments are tabulated in Table 1. Here, table 1 por-trays the simulation parameters advanced to im-plement the proposed IS-OWC system. Continuous wave laser (CWL) utilized a source with 193.1 THz transmitted frequency. The proposed method is simulated with 32768 samples with 109 bits/sec bit rate. The transmitter frequency 100 GHz spacing with the transmitted power is 15 dBm is occupied and 1550 nm wavelength is used for simulation.

4.1 Performance evaluation

The performance measures such as gain, pointing loss, bit error rate (BER) are discussed below,

4.1.1 Gain

The antenna gain is the measure of effectiveness that is maximum with the antenna can emit the de-livered power by the transmitter side, and the transmitter is given [23] by equation 2

$$H_W^{'} = \left(\frac{\pi \, d_W}{\omega} \right)^2 \tag{2}$$

The gain of the receiver side antenna is given by equation 3,

$$H_S^{'} = \left(\frac{\pi \, d_S}{\omega} \right)^2 \tag{3}$$

Where, dW represents the transmitter telescope diameter, dS denotes the diameter of the destina-tion of telescope.

Table 1: Simulation parameters

Parameter	Value
Simulation Window	
Bit Rate	109 bits/sec
Samples number	32768
Transmitter	
Frequency	193.1 THz
Laser	CWL
Spacing Frequency	100GHz
Power	15dBm
Extinction ratio	20dB
Line width	0.01MHz
Type of Modulation	RZ/NRZ
Optical Wireless Channel	
Range	2500km
Wavelength	1550nm
Transmitter Aperture diameter	15cm
Receiver Aperture diameter	15cm
Attenuation	0
Optical Efficiency	1
Transmitter &Receiver Pointing Error	1.1μrad
Additional losses	1.5dB
Propagation delay	0
Receiver	
Responsively of APD	1 A/W
Cut off frequency (LPBF)	0.72*Symbol Rate in Hz

4.1.2 Pointing loss

The transmitter side of pointing loss [2] is calculated by given equation,

$$K_W = e^{-H_W \in_W} \tag{4}$$

The receiver side of pointing loss [2] is calculated by given equation,

$$K_S = e^{-H_S \in_S} \tag{5}$$

Where, implicates the pointing errors of transmitter and receiver respectively.

4.1.3 Bit Error Rate (BER)

System representation indicates the BER and com-munication quality in the OWC system. The accepta-ble signal level includes below 10-9 of the BER value. Subsequently, the BER value for the optical system is less; it is hard for analyzing the Q factor employed as the performance of the system. Q factor contains a straight relationship through the BER signal [15].

$$BER = \frac{1}{2} erfd\left(\frac{P}{\sqrt{2}}\right) \tag{6}$$

$$BER = \frac{e\left(-P^2/2\right)}{P\sqrt{2\pi}} \tag{7}$$

4.2 Q- factor analysis for RZ and NRZ

Figure 12 and 13 shows the Q factor modulation formats in RZ and NRZ system. Based on the eye diagram the channel 2, 4, 6 and 8 results in RZ with NRZ formats are shown below. The "eye" of the digi-tal signal of a human eye is formed on an oscillo-scope, which displays the transmission system out-put, and the eye reflects the consistency of SNR at the "eye" of a digital signal. The sampling process with the largest "eye-opening" is the best place to determine if a given bit is "1" or a "0." The largest "eye-opening," is higher variance among the mean values of signal levels for "1" and "0." The eye dia-gram for channels 2, 4, and 6 furnishes a small eye-opening, which means that the Inter Symbol Inter-ference (ISI) is high. The eye diagram of channel 8 provides a big opening that refers to the ISI being low.

4.2.1 2 and 4 channel Q factor analysis

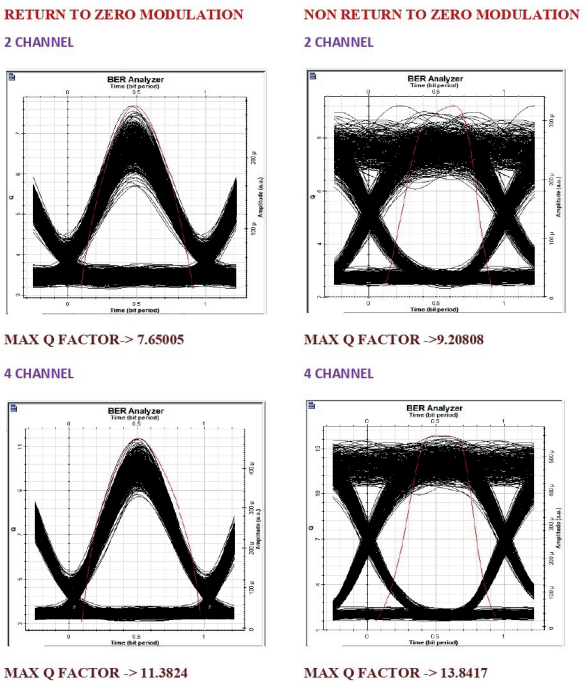


Figure 11: Maximum Q-factor of 2 and 4 Channel for RZ with NRZ modulation

Figure 11 shows the maximum Q factor in the second channel and fourth channel for RZ and NRZ modulation. Q factor and BER denote the converse relationship

in the 2 and 4-channel modulation schemes. Here, two channels in re-turn to zero modulation produce the maximum Q factor value is 7.65005, two channels in non-return to zero modulation produce the maximum Q factor value is 9.20808, four channels in return to zero modulation produce the maximum Q factor value is 11.3824, simi-larly, four channels in non-return to zero mod-ulation produces the maximum Q factor value is 13.8417.

4.2.2 6 and 8 channel Q factor analysis

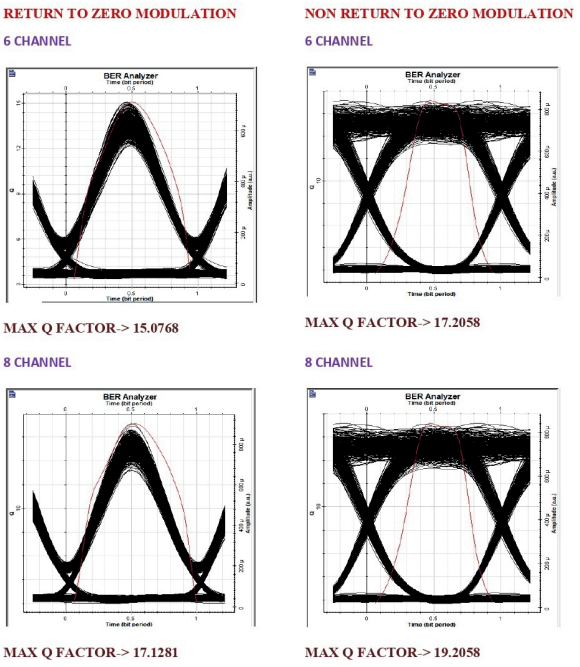


Figure 12: Maximum Q-factor of 6 and 8 Channel for RZ with NRZ modulation

Figure 12 depicts the maximum Q factor in the sixth channel and eighth channel for RZ and NRZ modula-tion. Q factor with BER denotes the converse rela-tion-ship in the 6 and 8-channel modulation scheme. Here, the sixth channels in return to zero modulation pro-duce the maximum Q factor value is 15.0768, the sixth channels in non-return to zero modulation pro-duce the maximum Q factor value is 17.2058, eight channels in return to zero modulation produce the maximum Q factor value is 17.1281, similarly, eight channels in non-return to zero modulation produces the maximum Q factor value is 19.2058.Figure 12 depicts the maximum Q factor in the sixth channel and eighth channel for RZ and NRZ modulation. Q factor with BER denotes the converse relationship in the 6 and 8-channel modula-tion scheme. Here, the sixth channels in return to zero modulation produce the maximum Q factor value is 15.0768, the sixth channels in non-return to zero modu-lation produce the maximum Q factor value is 17.2058, eight chan-nels in return to zero modulation produce the max-imum Q factor value is 17.1281, similarly, eight channels in non-return to zero modulation produces the maximum Q factor value is 19.2058.

4.3 BER Analysis for RZ & NRZ

Figures 13 and 14 show the minimum BER of channels 2, 4, 6 and 8 of RZ and NRZ modu-lation format. The BER specifies the possibility of wrong bit identifica-tion through the decision circuit. The design of OWC systems depends on performance estimation like BER figures. The channel comparison 2, 4, 6 and 8 suggests that the bit error rate is within the minimum target.

4.3.1 2 and 4 channel BER analysis

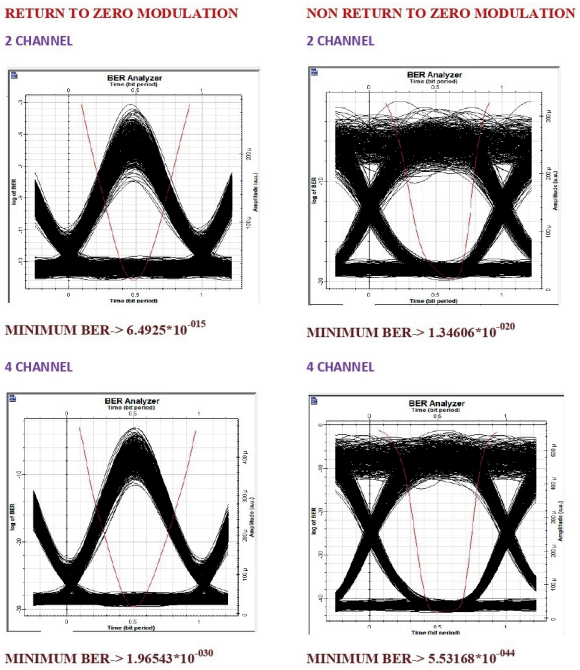


Figure 13: Minimum BER of 2 and 4 channel for RZ and NRZ modulation

Figure 13 shows the minimum BER in the second chan-nel and fourth channels for RZ and NRZ modula-tion. Q factor and BER are the converse relationship in the 2 and 4-channel modulation scheme. Here, two channels in RZ modulation produce that mini-mum BER value indicates, two channels in NRZ mod-ulation produce that minimum BER value indicates, four channels in RZ modulation produce that mini-mum BER value is, simi-larly four channels in NRZ modulation produces that minimum BER value indi-cates. 5053168*10-044

4.3.2 6 and 8 channel BER analysis

Figure 14 shows the minimum BER in the sixth chan-nel and eighth channel for RZ and NRZ modulation. Q

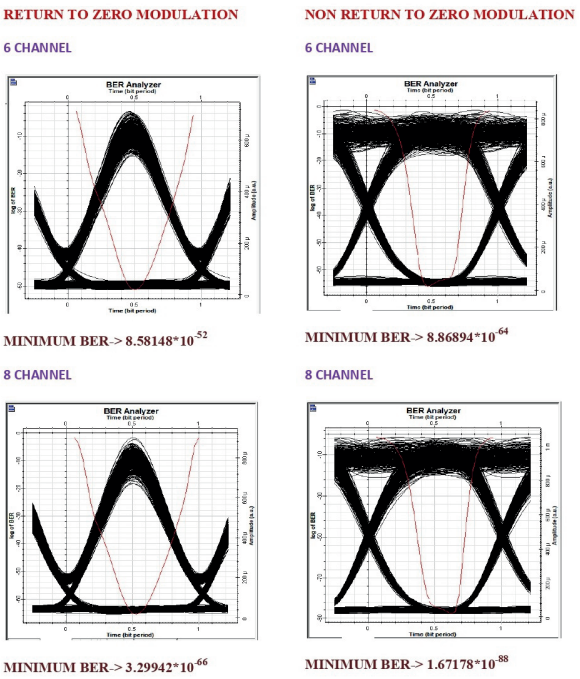


Figure 14: Minimum BER of 6 and 8 channel for RZ and NRZ modulation

factor and BER indicate the converse relationship in the 6 and 8-channel modulation schemes. Here, the sixth channels in RZ modulation produce that minimum BER value indicates, sixth channels in NRZ modulation produce that minimum BER value is, eight channels in RZ modulation produce that mini-mum BER value indicates, similarly eight channels in NRZ modulation produce that minimum BER value indicates 1.67178-10-88.

5 Conclusions

In this manuscript, the compara-tive analysis of IS-OWC for RZ and NRZ modulation formats for chan-nel diversity techniques is pro-posed. An n-channel IS-OWC sys-tem functioning at 10 Gbit/s with several inflexions setups for 15 dBm instance of power is encom-passed in the modeled scheme. The Inter-satellite signals are improved and let they portable to extended distances are done by connecting several OWC channels between the transmitter and the receiver. In an optical wireless communication device, the NRZ modulation is much superior to RZ modulation since in this BER is lesser and the Q factor is higher. The Q factor at-tained a maximum in the 8-channel OWC is 19.4385, whereas the Q factor attained minimum in the 2-channel OWC is 19.4385. Moreo-ver, the increased number of chan-nels may develop the proficiency of low power inter-satellite relations.

6 Conflict of Interest

The author of this document does not have any Conflict of Interest (COI) in publishing this paper.

7 References

1. Kaur, R. and Kaur, H., 2018. Comparative analysis of chirped, AMI and DPSK modulation techniques in IS-OWC system Optik, 154, pp.755-762 https://doi.org/10.1016/j.ijleo.2017.10.108
2. Kumari, G. and Selwal, C., 2018. Performance Improvement in Inter-satellite Optical Wireless Communication to Mitigate Losses Using Diver-sity Technique, In Optical and Wireless Technol-ogies (pp. 375-382).Springer, Singapore https://doi.org/10.1007/978-981-10-7395-3_42
3. Karpagarajesh, G., Blessie, A. and Krishnan, S., 2021. Performance Assessment of Dispersion Compensation Using Fiber Bragg Grating and Dispersion Compensation Fiber Tech-niques. Informacije MIDEM, 51(4), pp.215-223. https://doi.org/10.33180/InfMIDEM2021.402
4. Kong, M., Kang, C.H., Alkhazragi, O., Sun, X., Guo, Y., Sait, M., Holguin-Lerma, J.A., Ng, T.K. and Ooi, B.S., 2020. Survey of energy-autonomous solar cell receivers for satellite–air–ground–ocean optical wireless communication, Progress in Quantum Electronics, p.100300 https://doi.org/10.1016/j.pquantelec.2020.100300
5. Escribano, F.J., Wagemakers, A., Kaddoum, G. and Evangelista, J.V., 2020. A spatial time-frequency hopping index modulated scheme in turbulence-free optical wireless communication channels. IEEE Transactions on Communications, 68(7), pp.4437-4450 https://doi.org/10.1109/TCOMM.2020.2987561
6. Kaur, R. and Kaler, R.S., 2020. Performance of zero cross correlation resultant weight spectral amplitude codes in lower Earth orbit-based op-tical wireless channel system. International Journal of Communication Systems, 33(12), p.e4456 https://doi.org/10.1002/dac.4456
7. Zhu, C., Li, Y., Zhang, M., Wang, Q. and Zhou, W., 2020, May. An Optimization Method for the Gateway Station Deployment in LEO Satellite Systems. In 2020 IEEE 91st Vehicular Technology Conference (VTC2020-Spring) (pp. 1-7).IEEE. https://doi.org/10.1109/VTC2020-Spring48590.2020.9128413
8. Dubey, D., Prajapati, Y.K. and Tripathi, R., 2020. Error performance analysis of PPM-and FSK-based hybrid modulation scheme for FSO satel-lite down-

link. Optical and Quantum Electron-ics, 52, pp.1-16 Optical and Quantum Electron-ics (2020) 52:286 https://doi.org/10.1007/s11082-020-02404-7
9. Garg, N. and Ahmad, A., 2021. Performance of Outdoor Optical Wireless Communication Chan-nel through Gamma-Gamma Turbulence at Dif-ferent Frequency In Advances in Electromechan-ical Technologies (pp. 551-560).Springer, Singa-pore https://doi.org/10.1007/978-981-15-5463-6_49
10. Karpagarajesh, Guruviah, and Helen Anita. "Maximizing the area spanned by the optical SNR of the 5G using digital modulators and filters." Int. Arab J. Inf. Technol. 18, no. 3 (2021): 306-311 https://doi.org/10.34028/iajit/18/3/6
11. Malik, S. and Sahu, P.K., 2020. Performance analysis of free space optical communication system using different modulation schemes over weak to strong atmospheric turbulence channels. In Optical and Wireless Technologies (pp. 387-399). Springer, Singapore https://doi.org/10.1007/978-981-13-6159-3_41
11. Elsayed, E.E. and Yousif, B.B., 2020. Performance enhancement of M-ary pulse-position modulation for a wavelength division multiplexing free-space optical systems impaired by interchannel crosstalk, pointing error, and ASE noise. Optics Communications, 475, p.126219. https://doi.org/10.1016/j.optcom.2020.126219
12. Andreje, Ž. and Batagelj, B., 2021. Vrednotenje tehničnih lastnosti komunikacijskega omrežja majhnih satelitov Starlink. Elektrotehniski vestnik, 88(1/2), pp.1-7. https://ev.fe.uni-lj.si/1-2-2021/Andrejc.pdf
14. Sri, I.K. and Srinivasulu, A., 2019. Perfor-mance Analysis of Inter-satellite Optical Wireless Communication Using 12 and 24 Transponders. In Proceeding of the Second Microelectronics, Computing & Communication Systems (MCCS 2017) (pp. 811-821). Springer, Singapore https://doi.org/10.1007/978-981-10-8234-4_66
15. Patnaik, B. and Sahu, P.K., 2012. Inter-satellite optical wireless communication system design and simulation. IET Communications, 6(16), pp.2561-2567. https://doi.org/10.1049/iet-com.2012.0044
16. Sharma, V. and Kumar, N., 2013. Improved analysis of 2.5 Gbps-inter-satellite link (ISL) in inter-satellite optical-wireless communication (IsOWC) system. Optics Communications, 286, pp.99-102. https://doi.org/10.1016/j.optcom.2012.08.055
17. Pandi, V.S., Singh, M., Malhotra, J. and Grover, A., 2021. A spectral-efficient 1 Tbps terres-trial free-space optics link based on super-channel transmission. Optical and Quantum Electronics, 53(5), pp.1-12. https://doi.org/10.1007/s11082-021-02931-x
18. Anyanhun, A.I., Anzagira, A. and Edmonson, W.W., 2020. Intersatellite Communication: An MBSE Operational Concept for a Multi-orbit Disaggregated System. IEEE Journal on Miniaturization for Air and Space Systems,1(1),pp.56-65 https://doi.org/10.1109/JMASS.2020.3001080
19. Kumar, N., 2014. Enhanced performance analysis of inter-satellite optical-wireless communi-cation (IsOWC)system. Optik, 125(8),pp.1945-1949. https://doi.org/10.1016/j.ijleo.2013.11.008
20. Lu, K., Xiao, G. and Chlamtac, I., 2005. Anal-ysis of blocking probability for distributed lightpath establishment in WDM optical net-works. IEEE/ACM Transactions on networking, 13(1), pp.187197. https://doi.org/10.1109/TNET.2004.842233
21. Ravishankar, C., Gopal, R., BenAmmar, N., Zakaria, G. and Huang, X., 2021. Next-generation global satellite system with mega-constellations.International Journal of Satellite Communications and Networking, 39(1), pp.6-28 https://doi.org/10.1002/sat.1351
22. Singh, M., Malhotra, J. and Dhasarathan, V., 2020. A high-speed single-channel inter-satellite optical wireless communication link incorporating spectrum-efficient orthogonal modulation scheme. Microwave and Optical Technology Letters, 62(12),pp.4007-4014 https://doi.org/10.1002/mop.32511
23. Sharma, P. and Meena, S., 2018, July. Per-formance Analysis of Inter-Satellite Optical Wireless Communication (Is-OWC) System by using Channel Diversity Technique.In 2018 Inventive Research in Computing Applications (ICIRCA) (pp. 477-480).IEEE https://doi.org/10.1109/ICIRCA.2018.8597344
24. Khichar, S. and Inaniya, P.K., 2018, April. Inter-Satellite Optical Wireless Communication Sys-tem Design Using Diversity Technique with Filter and Amplifier.In 2018 Communication and Signal Processing (ICCSP)(pp.0481-0484).IEEE. https://doi.org/10.1109/ICCSP.2018.8524366
25. Chaudhary, S., Sharma, A. and Singh, V., 2019. Optimization of high speed and long haul inter-satellite communication link by incorporating differential phase shift key and orthogonal frequen-cy division multiplexing scheme. Optik, 176, pp.185-190. https://doi.org/10.1016/j.ijleo.2018.09.037
26. Karpagarajesh, G., Krishnan, R.S., Robinson, Y.H., Vimal, S., Kadry, S. and Nam, Y., 2021. Investigation of digital video broadcasting application employing the modulation formats like QAM and PSK using OWC, FSO, and LOS-FSO channels. Alexandria Engineering Journal. https://www.sciencedirect.com/science/article/pii/S1110016821004014
27. Viswanath, A., Jain, V.K. and Kar, S., 2015. Analysis of earth-to-satellite free-space optical link performance in the presence of turbulence, beam-wander induced pointing error and weather condi-

tions for different intensity modulation schemes. IET Communications, 9(18), pp.2253-2258. https://doi.org/10.1049/iet-com.2015.0379

28. Pradhan, S., Sahu, P.K., Giri, R.K. and Patnaik, B., 2017, December. Inter-satellite optical wireless communication system design using diversity tech-niques. In 2017, Optical and Communication Engi-neering (ICMOCE)(pp.250-253).IEEE https://doi.org/10.1109/ICMOCE.2015.7489738

Arrived: 09. 09. 2022
Accepted: 23. 12. 2022

Original scientific paper
https://doi.org/10.33180/InfMIDEM2023.102

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 53, No. 1(2023), 15 – 30

Loss reduction and reliability improvement in distributed network using HF-SOA based optimal installation of DG, SCs and STF

Ithaya Rajagopalan[1], Jagatheeswari Ponnuswamy[2]

[1]Department of Electrical and Electronics Engineering, Arunachala college of engineering for women, Manavilai Road, Manavilai, Nagercoil, Tamil Nadu, India
[2]Department of Electronics and Communication Engineering, Ponjesly college of Engineering, College Road, Parvathipuram, Nagercoil, Tamil Nadu, India

Abstract: In recent years, most of the research works related to Distributed Generation (DG), targeted on the loss minimization and reliability enhancement due to the existence of intermittent Renewable Energy Sources (RES). In this research work, this target is attained by an optimal installation of DG, shunt capacitors (SCs) and single tuned filter (STF) through a novel hybrid fuzzy based seagull optimization algorithm (HF-SOA) in a distributed power network. Compared to the literatures better harmonics mitigation is achieved in this research work due to the presence of STF. The proposed research problem is considered as multi-objective and a novel objective function that incorporates, minimization of power loss, harmonics and enhancement of voltage profile (VP) as well as system reliability is introduced in this research article. The fuzzy membership function is framed for each objective function parameter and the fuzzified membership functions are considered as an objective function for the SOA approach. Three case studies are conducted in both IEEE 33 and 69 radial networks to examine the influence of the HF-SOA algorithm in satisfying the proposed multi-objective function (MOF). In the case studies, the percentage loss, THD reduction, VP enhancement, cost reduction of DG and reliability improvement measured through expected interruption cost (ECOST) are analyses in detail. The coding of HF-SOA and analysis of the proposed work are resolved in the MATLAB R2022a Editor Software. The simulation results confirms that the proposed HF-SOA is superior than the with the recently published optimization approaches named genetic moth swarm algorithm (GMSA) and salp swarm optimization algorithm (SSA).

Keywords: Distributed Generation (DG); hybrid fuzzy based seagull optimization algorithm (HF-SOA); Power loss minimization; reliability improvement; seagull optimization algorithm (SOA); Shunt Capacitors (SCs)

Zmanjšanje izgub in izboljšanje zanesljivosti v porazdeljenem omrežju z uporabo optimalne namestitve DG, SC in STF na podlagi HF-SOA

Izvleček: V zadnjih letih je večina raziskovalnih del, povezanih z razpršeno proizvodnjo električne energije (DG), usmerjena v zmanjševanje izgub in povečanje zanesljivosti zaradi obstoja nestalnih obnovljivih virov energije (RES). V članku je ta cilj dosežen z optimalno namestitvijo DG, vzporenih kondenzatorjev (SC) in enojnega uglašenega filtra (STF) s pomočjo novega hibridnega optimizacijskega algoritma na osnovi fuzzije (HF-SOA) v distribuiranem elektroenergetskem omrežju. V primerjavi z literaturo je v tem raziskovalnem delu zaradi prisotnosti STF dosežena boljša ublažitev harmonikov. Predlagan problem je obravnavan kot večpredmeten, predstavljena je nova ciljna funkcija, ki vključuje minimizacijo izgube moči, harmonikov in izboljšanje napetostnega profila (VP) ter zanesljivosti sistema. Za vsak parameter ciljne funkcije je oblikovana mehka funkcija pripadnosti, mehke funkcije pripadnosti pa se obravnavajo kot ciljna funkcija za pristop SOA. Da bi preverili vpliv algoritma HF-SOA pri izpolnjevanju predlagane večobjektivne funkcije (MOF), so izvedene tri študije primerov v radialnih omrežjih IEEE 33 in 69. V študijah primerov so podrobno analizirani odstotki izgube, zmanjšanje THD, izboljšanje VP, zmanjšanje GD in izboljšanje zanesljivosti, merjeno s pričakovanimi stroški prekinitve (ECOST). Kodiranje HF-SOA in analiza predlaganega dela sta rešena v programski opremi MATLAB R2022a Editor. Rezultati simulacije potrjujejo, da je predlagani HF-SOA boljši od nedavno objavljenih optimizacijskih pristopov, imenovanih algoritem genetskega roja (GMSA) in algoritem optimizacije roja Salp (SSA).

Ključne besede: razpršena proizvodnja (DG); hibridni mehki optimizacijski algoritem (HF-SOA); minimizacija izgube moči; izboljšanje zanesljivosti; optimizacijski algoritem (SOA); vzporedni kondenzatorji (SC)

** Corresponding Author's e-mail: ithayaithaya777@gmail.com*

How to cite:
I. Rajagopalan et al., "Loss reduction and reliability improvement in distributed network using HF-SOA based optimal installation of DG, SCs and STF", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 53, No. 1(2023), pp. 15–30

1 Introduction

Nowadays, the conventional energy sources are replaced with the RES due to the increasing energy crisis and lack of availability of fossil fuels. Hence, the research platform widens by virtue of power quality (PQ) issues occurring in Radial Distributed Network (RDN) including intermittent RES. The crucial factors commonly considered in most of the earlier research works to mitigate PQ issues in RDN are power loss minimization, VP improvement and reliability improvement. To effectively meet these factors, the distributed generation system is suggested as an alternate solution instead of expanding the network infrastructure since, its limited commissioning time and its effectiveness in minimizing network losses. In recent research works, the SCs are installed along with distributed generation as it provides reactive power compensation for enhancing the VP. Hence, both real as well as reactive powers could be improved with the combination of distributed generation and SCs in RDN. However, the optimal selection and installation of DG and SCs is a challenging task since the cost of installation of distributed generation should overcome the energy losses. So many optimization approaches are being developed to optimize the siting and sizing of distributed generation and SCs and some of them are presented below:

Most of the earlier research articles reported so far aimed to optimize the sitting and sizing of DG only [1-3]. The optimal siting and sizing are commonly termed as optimal installation in this research article. The artificial intelligence (AI) based optimization algorithms which mimic the social behavior of living organisms were suggested to foreseeing the optimization installation of distributed generation. The particle swarm optimization (PSO) algorithm was proposed to predict the cost-effective installation of DG to reduce the power losses, and harmonics [4]. The artificial bee colony (ABC) algorithm was reported to optimize the size and installation node of DG by minimizing the multi-objective function such as cost, voltage drop and power loss in the network [5]. The Manta Ray Foraging optimization algorithm (MRFO) was suggested to diminish the network loss in RDN by optimal installation of DG in power network. The result analysis of MRFO was performed with 3, 69 and 85 bus system [6].

However, the presence of inductive components in power network induces lagging power factor which minimize the VP and increases the network losses. Hence, it is necessary to improve the power factor and VP by installing the SCs thereby reduce the network losses. Belkacem Mahdad and K. Srairi presented the adaptive differential algorithm-based optimization of siting and sizing of DG in presence of static VAR compensator (SVC) in RDN to reduce the cost and loss functions [7].

A fuzzy based optimal installation of DG using Genetic Algorithm (GA) to reduce real and reactive power supply as well as losses, stability index and enhancement minimum bus voltage was introduced by Srinivasa Rao Gampa et.al [8]. In this approach the fuzzy membership functions are framed based on the proposed objective function and the selection of nodes for distributed generation and SCs with different power factors were optimized with GA approach. The experimental analysis was performed in both 51 and 69 node RDN and successfully obtained the proposed objective function.

In the same manner, optimal integration of capacitor and DG using Bat Algorithm (BA) was proposed by Thangaraj Yuvaraj et.al which was aimed to reduce the power loss and stability improvement of the RDN. The load variations such as constant, industrial, residential and commercial were also considered as one of the main factors in that research work [9]. The experimental study in that article was performed in 33 and 69 node network and the superiority of the Bat Algorithm was proved over conventional methodologies.

The ant lion optimization (ALO) was suggested by Ahmed R. and Abul'Wafa to select the optimal node for the installation of DG and SCs based on the proposed multi-objective function [10]. The ALO algorithm was examined on the IEEE 118 node network and the installation of various RES and the SCs were optimized in that article. Amirreza Naderipour et.al have presented the spotted hyena optimizer (SHO) approach for optimizing the DG and SCs in a cost-effective manner. The SHO approach was tested in both island and grid connected mode with different modes of operation and power factors and the superiority was proved over grey wolf optimization (GWO) algorithm [11].

In similar manner, many research articles were published based on the optimal sizing and installation nodes of DG and SCs combination so as to reduce both real and reactive power losses [7, 12-14]. Commonly, in most of the article, the power loss minimization was considered as the fundamental objective function related to the proposed research arena. Furthermore, the minimization of installation and operating cost and enhancement of VP, system stability and reliability were also reported as effective objective functions in some of the research articles [9, 10, 15, 16].

Optimization techniques like Constriction Coefficient Particle Swarm Optimization (CPSO) are used to reduce the loss of renewable energy resources (RES) in distributed generation systems. By used this method, losses

are reduced by 63.90 % [27]. To reduce voltage regulation issues, non-sorting dominated genetic algorithms (NSGAs) were employed to allocate battery energy storage systems and distributed energy resources optimally [28]. The Modified Shuffled Frog Leaping Algorithm (MSFLA) was proposed to minimize energy loss, operational costs, and energy not supplied by DG systems [29]. Using an AC optimal power flow (OPF) and genetic algorithm (GA) for 24 hours, [30] minimize investment and operation costs in renewable energy systems integrated with battery banks. In [31] an optimal allocation of DG and D-STATCOM within a distribution system using the Bat Algorithm, in which the loss sensitivity factor (LSF) is utilized to find the optimum location for distribution generation systems. The minimum loss obtained is 31.94 kW, which is 89.88 %.

In some of the recent articles the single tuned filters (STF) were also installed in the distribution network which consist of a series connected resistor, inductor and a capacitor. The number of harmonics presented in the network is measured with Total harmonics distortion (THD) and it is added as one of the prime factors in multi-objective function of the optimization problem. The comparative THD values of the network in the presence and absence of STF undoubtedly confirms that the THD is much reduced in the presence of STF [17].

A technical research growth was observed from the literature survey. Most of the earlier research works presented so far have initially targeted only on DG installation to minimize the power loss with analytical calculations. Subsequently, intelligent algorithms were proposed to optimize the installation of DG with a single objective function. Afterwards, the multi-objective functions were introduced which incorporated minimization of losses, harmonics, voltage drop, cost also to improve VP, stability as well as reliability. To provide the reactive power compensation and to enhance the VP the compensating devices such as static VAR compensator, shunt capacitor and DSTATCOM were then installed and their location are optimized along with DG.

2 Materials and methods

From the observations made from the literature study, the following research gaps are identified:

i. However, enormous optimization methodologies have been proposed so far to predict a suitable sizing and location of DG so as to compensate the suggested objective functions, the research works are still in progress on developing the novel metaheuristic approaches to reimburse the objective functions in a better way.
ii. Most of the articled focused only on optimal DG installation and very few articles include the presence of shunt capacitors.
iii. The multi-objective functions proposed in earlier literatures employed mainly with loss reduction and VP improvement and little effort has been expended on reliability enhancement and harmonic mitigation.

By reviewing the literatures related to the proposed research problem, and to overcome the research gap stated above the following augmentation are presented in the proposed research work:

According to the research gap, the contributions of the proposed work is described as follows;

- (i) A novel HF-SOA optimization algorithm is proposed in this research article to optimize the siting and sizing of GD, SCs and STF and better results are produced compared to GMSA and SSA approaches.
- (ii) The SCs also included in the power network and its influence on enhancing the VP and diminishing of power losses are proved in this article.
- (iii) The STF is installed in the power network and a novel multi-objective function that incorporates network loss minimization, harmonics mitigation, VP enhancement, reliability improvement and total cost minimization of DG is developed in this proposed research problem. The effectiveness of the proposed algorithm is also experimented in standard IEEE 33 and 69 node networks with three case studies and its dominance is confirmed over genetic moth swarm algorithm (GMSA) [18] and salp swarm optimization algorithm (SSA) [19].

The content presented in this research work are structured as follows: Section 2 describes the distributed power network with 33 and 69 node RDN. Section 3 explains the system description of DG network. The problem formulation and the (HF-SOA) optimization approach proposed in this research work is apprized in section 4. The section 5 acquainted with detailed computational analysis performed in this paper out and their results and discussions. Finally, section 6 describes the conclusion of proposed work together with the future scope.

3 Distributed power network

3.1 System description

While integrating the intermittent renewable energy system in DG the distributed power network faces the

problems such as voltage fluctuations, intensifies the network losses and increases the THD. Hence, the future development of power systems is mainly targeted to develop smart distributed power networks which attracts the focus of so many researchers to work towards it [20]. One of such attempts is made in this proposed research article by developing an optimization algorithm to foreseeing the siting and sizing of DG, SCs and STF. In this proposed research work, the solar photo voltaic (PV) and wind turbines are considered to be integrated in DG system and the SCs and STFs are shunted with the buses. The rating of SCs might be carefully chosen that the voltage rise problem not occurring in power system. In general, the optimization problems are experimented in reconfigured IEEE systems. In the similar manner, the proposed HF-SOA based installation of DG, SCs and STF is examined in 33 and 69 RDN which are illustrated in Fig 1 and Fig 2. Prepare the figures and tables according to these instructions

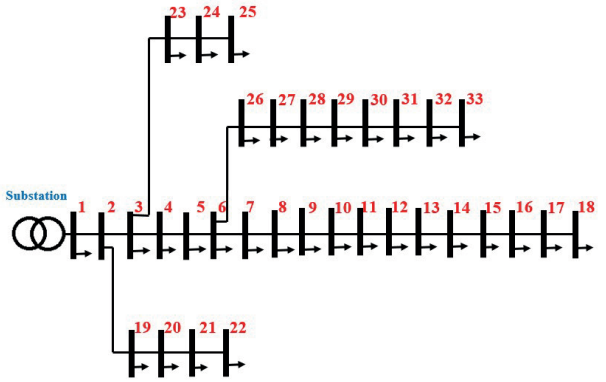


Figure 1: IEEE 33 node reconfigured RDN

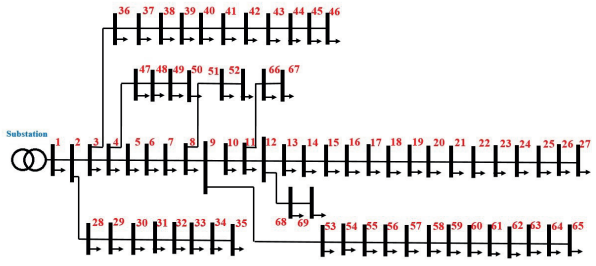


Figure 2: IEEE 69 node reconfigured RDN

When the RES is connected with the DG, the intermittent nature of RES and the power converter arrangements equipped with the utility grid makes nonlinear DG (NLDG) and generates harmonics in the power network system. Very few recent research works related to DG allocation are focused on harmonics mitigation using either active or passive filters [21, 22]. In the research work the single tuned filter (STF) is preferred which consist of series connected resistor, inductor and a capacitor. The THD is considered as the measuring factor for the harmonics analysis and it is included as the minimization function in the optimization problem to mitigate the harmonics.

4 Optimizing the size and allocation of DG with proposed AO algorithm

4.1 Problem Formulation

The optimal installation of DG, SCs and STF is the proposed research problem and the results are optimized with the HF-SOA approach. The multi-objective function is developed for this optimization problem that incorporates loss minimization, harmonics mitigation and VP improvement. The development of multi-objective function parameters and the constraints are described as below. The overall objective function for the proposed research problem is developed as stated below (0a,0b):

$$Obj_{fn} = min\sum\left(Obj1 + Obj3 + Obj5\right) + max\sum\left(Obj2 + Obj4\right) \quad (0a)$$

$$Obj_{fn} = \sum_{i=1}^{N} w_n \left(\min\left(P_{TL} + \mathrm{THD} + Cost_{DG}\right) + max\left(R_{index} + V_P\right)\right) \quad (0b)$$

Where, *Obj*1 represents the power loss minimization (P_{TL}), *Obj*2 represents the reliability index (R_{index}), *Obj*3 represents the Harmonics minimization (THD), *Obj*4 represents the Voltage profile improvement (V_p), and *Obj*5 represents the overall cost of the DG system. w_n indicates the weighting factor used to emphasize the importance of lowering each term of the objective function, $w_1 = 0.4$, $w_2 = 0.1$, $w_3 = 0.1$, $w_4 = 0.4$, and $w_5 = 0.1$ attributed to power loss, reliability index, THD minimization, Voltage profile and overall cost of the DG system.

4.1.1 Power loss minimization (Obj 1):

The power loss (P_L) minimization is the parameter is commonly considered in most of research work related to DG installation. The optimal sizing and allocation of DG alone supports only for the real power losses and the installation of SCs along with DG assist for reactive power compensation in addition. The active and reactive power losses between *i* and *i* + 1 are denoted in (1) and (2) moreover, the voltage and power losses for real power and reactive power could be evaluated as illustrates in equations (3) and (4), respectively.

$$P_{i+1} = P_i - P_{L(i+1)} + R_i \frac{P_i^2 + Q_i^2}{V_i^2} \quad (1)$$

$$Q_{i+1} = Q_i - Q_{L(i+1)} + X_i \frac{P_i^2 + Q_i^2}{V_i^2} \quad (2)$$

Whereas, P_i and P_{i+1} are the real power at the sending as well as receiving end, Q_i and Q_{i+1} are the reactive power at the sending as well as receiving end, $P_{L(i+1)}$ and $Q_{L(i+1)}$

are the real and reactive power losses at the receiving end and V_i is the voltage at the sending end.

$$V_{i+1}^2 = V_i^2 - 2\left(R_i \cdot P_i + X_i \cdot Q_i\right) + (R_i^2 + X_i^2)\frac{P_i^2 + Q_i^2}{V_i^2} \quad (3)$$

$$P_{L(i,i+1)} = R_i * \frac{P_i^2 + Q_i^2}{V_i^2} \quad (4)$$

Whereas, R_i and X_i are the resistance and reactance of the transmission line. The total loss of the distributed power network is represented in equation (5). The n represents the number of nodes in the network.

$$P_{TL} = \sum_{i=1}^{n-1} P_{L(i,i+1)} \quad (5)$$

4.1.2 Reliability Index (Obj 2):

The reliability index is one of the essential terms that might be considered during the development of objective function. In this research work, the economical oriented reliability parameter which describes the ratio between the expected interruption cost in the presence and absence of DG, SCs and STF respectively (6) is considered as one of the parameters in the objective function.

$$R_{index} = \frac{ECOST_{DG,SCs,STF}}{ECOST} \quad (6)$$

Where, expected interruption cost (ECOST) is an effective tool in system planning which decides the adequate level of reliability for users. Accordingly, the ECOST without the installation of any DGs and capacitors ($ECOST_i^{without\ DG,Cap}$) is evaluated as follows:

$$ECOST_i^{without\ DG,Cap} = \sum_{i=1}^{N_{bus}} Load_{avg_i} \times C_i \times \lambda_i^{uncomp} \quad (7)$$

$$ECOST_i^{without\ DG,Cap} = \sum_{i=1}^{N_{bus}} Load_{avg_i} \times C_i \times \lambda_i^{uncomp} \quad (8)$$

Where, $Load_{avg_i}$ is the average load in KW, C_i is the interruption cost and $\lambda_{i_{new}}$ is the modified rate of failure after the capacitor placement, λ_i^{uncomp} is the without DG and capacitor installation case.

Following optimal DG and capacitor installation, the cost benefit from reduced ECOST can be expressed as following Eq. (9):

$$ECOST_{CB} = ECOST_i^{without\ DG,Cap} - ECOST_i^{with\ DG,Cap} \quad (9)$$

The installation of capacitor has a direct influence on the reliability as it moderates the rate of failure. The current induces due to the capacitor placement reduces the temperature as well as the loss of transmission line. Active and reactive power requirements in distribution networks can be met by the utilization of DGs and capacitor allocation. The losses efficiently decrease as a result of a reduction in current magnitude. Due to this, higher temperatures have a less destructive effect on the reliability indices of both overhead and underground lines. Distribution feeder components will have a lower failure rate as a result of these impacts. If the ith feeder is not equipped with DGs and capacitors, it has an uncompensated failure rate of λ_i^{uncomp} In feeder laterals with fully compensated active and reactive current components, failure rate drops to λ_i^{comp} . It can be observed that if the active and reactive elements of the current are not compensated, the failure rate will be linearly related to the level of compensation. The change in real and reactive currents due to the capacitor placement is measured by the compensation coefficient $\propto_i$ (10). The I_{real}, and I_{reac} in equation (10) represents the real and reactive current components respectively.

$$\propto_i = \frac{I_{reac}^{new}}{I_{reac}^{old}} * \frac{I_{real}^{new}}{I_{real}^{old}} \quad (10)$$

Moreover, the modified rate of failure after the capacitor placement ($\lambda_{i_{new}}$) could be derived as shown below (11).

$$\lambda_{i_{new}} = \propto_i \left(\lambda_i^{uncomp} - \lambda_i^{comp}\right) + \lambda_i^{comp} \quad (11)$$

4.1.3 Harmonics minimization (Obj 3):

The harmonics minimization is computed through Total Harmonic Distortion (THD) presented in the signal (12) [23].

$$THD = \sum_{i=1}^{N}\left(\frac{1}{V_{1i}}\sqrt{\sum_{h=2}^{H} V_{hi}^2}\right) \quad (12)$$

Whereas, V_{1i} is the fundamental bus voltage, V_{hi} is the order of harmonics at i^{th} bus.

4.1.4 Voltage profile improvement (Obj 4):

In DG system the power generated from the various distributed energy sources are linked to the common distributer. The sudden change in load conditions affects the VP. Hence, the improvement of voltage profile is considered as one on the objective in this research work which is stated in equation (13).

$$Voltage\_profile = \sum_{i=1}^{N}\left(\frac{V_i - V_i^{spec}}{V_i^{max} - V_i^{min}}\right)^2 \quad (13)$$

Whereas, V_i is the i^{th} bus voltage, V_i^{spec} is the specified voltage magnitude (1.0 p. u) and V_i^{max}, V_i^{min} are the i^{th} bus minimum and maximum voltage respectively.

4.1.5 Cost minimization for the DGs (Obj 5):
Different types of DG have different costs. There will be a variation in the total cost of the DGs as the size and number of the DGs change. To minimize the cost of the DG, the objective can be formulated as follows:

$$Cost_{DG} = \left[\frac{Cap_c * Capacity * K_{DG_i}}{lifetime * 8760 * LF}\right] + \left[\left(C_{Fuel} + C_{O\&M}\right) * K_{DG_i}\right] \quad (14)$$

Where, $Cost_{DG}$ is the DGs' overall cost, Cap_c is the capital cost of DG system, LF is the load factor K_{DG_i} is the size of the i[th] DG, C_{Fuel} is the size of the ith DG system, and $C_{O\&M}$ is the operation and maintenance cost of DG system.

4.2 Hybrid Seagull Optimization Algorithm (HF-SOA)

4.2.1 Fuzzification of objective function parameters
This research work is targeted to foreseeing the optimal installation of DG, SCs and STF by satisfying the objective function stated above Eq. (0). In HF-SOA approach initially the fuzzification of this multi- objective function is performed corresponding to the membership functions selected. In this proposed problem the trapezoidal membership function is commonly chosen for fuzzification of all the fitness function parameters such as loss, the VP, ECOST and THD. The membership functions for the proposed research problem are illustrated in Fig3.

(i) Fuzzification of Power loss:
The power loss is stated in equation (5). The active power loss index (APLI) is evaluated as the ratio between the active power loss in the presence $(APL_{DG,SCs,STF})$ and absence (APL) of DG, SCs and STF (15).

$$APLI_{index} = \frac{APL_{DG,SCs,STF}}{APL} \quad (15)$$

Using the trapezoidal membership function depicted in Fig 3a, the APLI is fuzzified as described in the fuzzy set (16) given below.

$$\mu_{APLI} = \begin{cases} 1 \; for \; APLI \le APLI_{min} \\ \dfrac{APLI_{max} - APLI}{APLI_{max} - APLI_{min}} \; for \; APLI_{min} < \\ 0 \; for \; APLI > APLI_{max} \end{cases} \quad (16)$$

$$< APLI \le APLI_{max}$$

Where, $APLI_{min}$ and $APLI_{max}$ are the minimum maximum limits of power loss index. This minimum limit depends on the utility requirement and for the proposed problem the maximum value is chosen as 1.

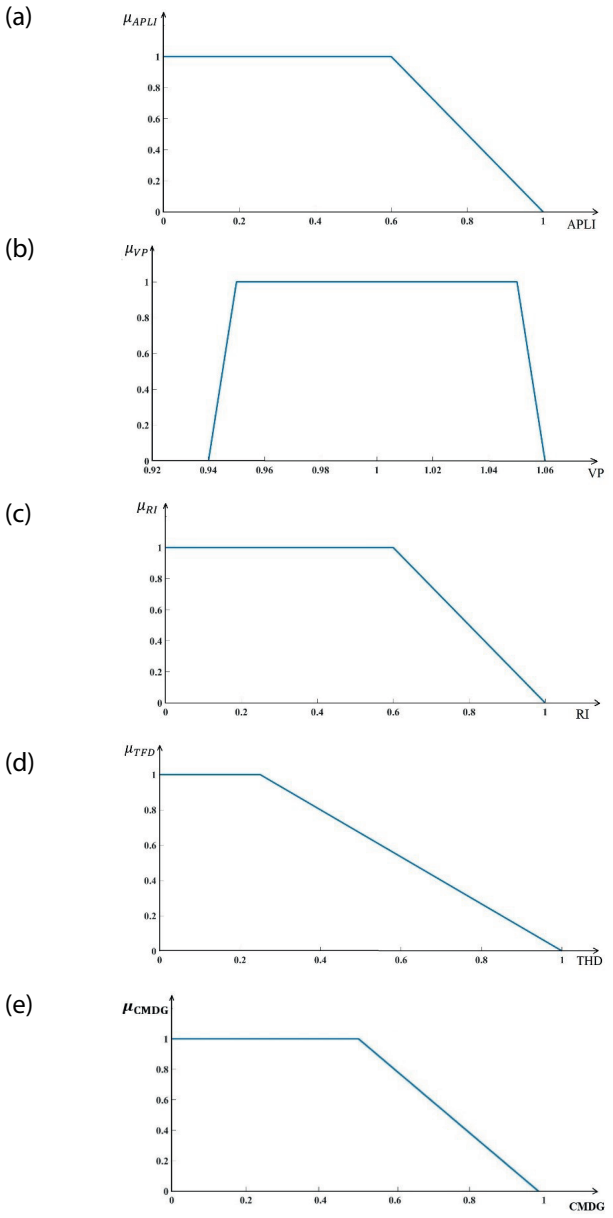


Figure 3: Fuzzy membership function for the objective function parameters

(ii) Fuzzification of minimum and maximum voltage profiles (VPs):

The VP is stated in equation (13). Using the trapezoidal membership function the VP is fuzzified as described in the fuzzy set (17) given below.

$$\mu_{VP} = \begin{cases} 0 & for \; VP \le VP_{L1} \\ \dfrac{VP - VP_{L1}}{VP_{min} - VP_{L1}} & for \; VP_{L1} \le VP \le VP_{min} \\ 1 & for \; VP_{min} \le VP \le VP_{max} \\ \dfrac{VP_{L2} - VP}{VP_{L2} - VP_{max}} & for \; VP_{max} \le VP \le VP_{L2} \end{cases} \quad (17)$$

Where, VP_{L1} and VP_{L2} are the minimum and maximum VP limits of the membership function and VP_{min} and VP_{max} are the primary and secondary limits represented in Fig 3b. These limits are chosen as VP_{L1} =0.94, VP_{min} =0.95, VP_{max} =1.05 and VP_{L2} =1.06 respectively.

(iii) Fuzzification of Reliability Index (RI):
The RI describes the ratio between the expected interruption cost in the presence and absence of DG, SCs and STF respectively which is stated in equation (6). Using the trapezoidal membership function depicted in Fig 3c, the RI is fuzzified as described in the fuzzy set (18) given below.

$$\mu_{RI} = \begin{cases} 1 \; for \; RI \le RI_{min} \\ \dfrac{RI_{max} - RI}{RI_{max} - RI_{min}} \; for \; RI_{min} < \\ 0 \; for \; RI > RI_{max} \end{cases} \quad (18)$$

$$< RI \le RI_{max}$$

Where, RI_{min} and RI_{max} are the minimum maximum limits of reliability index and their values are chosen as 0.6 and 1.0 for the proposed research problem.

(iv) Fuzzification of total harmonics distortion (THD):
The THD describes the harmonics presented in the bus voltage and it is stated in equation (12). This research work aimed to mitigate the harmonics to a minimum value Using the trapezoidal membership function depicted in Fig 3d, the THD is fuzzified as described in the fuzzy set (19) given below.

$$\mu_{THD} = \begin{cases} 1 \; for \; THD \le THD_{min} \\ \dfrac{THD_{max} - THD}{THD_{max} - THD_{min}} \; for \; THD_{min} < \\ 0 \; for \; THD > THD_{max} \end{cases} \quad (19)$$

$$< THD \le THD_{max}$$

Where, THD_{min} and THD_{max} are the minimum maximum limits of harmonic distortion and their values are chosen as 0.25 and 1.0 for the proposed research problem.

(v) Fuzzification of Cost minimization for the DGs (CMDG)
As shown in Fig 3(e), the DG cost function has been modeled as a fuzzy function. The cost minimization presented in the bus voltage and it is stated in equation (14). Eq. (20) represents the fuzzy membership function of the cost that is under or equal to the permissible cost as follows:

$$\mu_{\text{CMDG}} = \begin{cases} 1 & CMDG \le CMDG_{min} \\ \left(\dfrac{CMDG_{max} - CMDG}{CMDG_{max} - CMDG_{min}} \right) & CMDG_{min} \le CMDG \le CMDG_{max} \\ 0 & CMDG \ge CMDG_{max} \end{cases} \quad (20)$$

Where, $CMDG_{min}$ and $CMDG_{max}$ are the minimum and maximum DG cost.

4.2.2 Seagull Optimization Algorithm (SOA)
SOA is the most persuasive recently developed metaheuristic algorithm which is framed from the inspiration of hunting behavior of the bird Seagulls which are technically known as Laridae. It follows two significant strategies called exploration and exploitation to catch the prey. In this research, the proposed SOA algorithm is used to tune the membership function of fuzzy rules. The effectiveness of SOA algorithm has been proved in various engineering studies [23, 24]. The elucidation of hunting strategies of this algorithm with its mathematical modelling is presented in this section.

Migration (exploration):
In migration, the mathematical modelling of the particle movement is developed in a grouping pattern with respect to each other by satisfy the following three steps.

- Avoiding collision- To avoid collisions, while moving to the new position C_s) the current position ($\overrightarrow{P_s}(x)$) of particles are multiplied with the variable *A* (21). The variable *A* is represented in equation (10). The f_c represented in equation (22) regulate the frequency of retaining *A* which is decreased from f_c to 0.

$$\overrightarrow{C_s} = A \times \overrightarrow{P_s}(x) \quad (21)$$

$$A = f_c - \left(x * \left(\frac{f_c}{Max_{iteration}} \right) \right) \quad (22)$$

- Move towards optimal solution- In this step, the particles are moving towards its neighbor with best fitness value (23). Where, the $\overrightarrow{M_s}$ represent new particle position after moving towards best solution, $\overrightarrow{P_{bs}}(x)$ is the particle best solution and $\overrightarrow{P_s}(x)$ is the current position of particle. The *B* is represented in equation (16). The *rd* in equation (24) states the random number between 0-1.

$$\overrightarrow{M_s} = B \times (\overrightarrow{P_{bs}}(x) - \overrightarrow{P_s}(x)) \quad (23)$$

$$B = 2 \times A^2 \times rd \tag{24}$$

- Stay nearer to the particles with best fitness-In this step the position of particles is updated according to the best position (25).

$$\overrightarrow{D_s} = \left| \overrightarrow{C_s} + \overrightarrow{M_s} \right| \tag{25}$$

Attacking (exploitation):
In this process the Seagulls makes a spiral movement in the air to reach the prey. The best positions with optimal fitness values are finally achieved in this position with respect to the distance of each particle from the best fitness position and their movement in x, y and z plane (26).

$$\overrightarrow{P_s}(x) = \left(\overrightarrow{D_s} \times x' \times y' \times z' \right) + \overrightarrow{P_{bs}}(x) \tag{26}$$

Finally, the optimal solutions are reached in SOA with a smooth transition between exploration and exploitation moves.

5 Results and discussions

The optimal installation of DG, SCs and STF is the research problem and the solution is optimized using an effective proposed HF-SOA algorithm to predict the proposed fitness functions (objective function). The novel fitness function suggested in section 3.1 (1) is used for this optimization problem. With deterministic demand of load and DG system, the present article presents optimum location and size of DG in radial distribution network (RDN) to reduce network loss. The DG in this study is selected by Locating the bus in the network with the highest level of sensitivity. The study examines the placement of three DGs in both networks. Loss sensitivity analysis is used to determine the location of DG, one bus at a time, by selecting the most sensitive. The next sensitive bus is determined after employing DG at the selected bus. In order to find the next sensitive bus, the process is repeated once again. Therefore, DGs are placed in the respective RDNs based on the loss-sensitive buses in the network. For both 33-bus and 69-bus RDNs, the procedure identifies the loss-sensitive buses. A detail performance study of locating the DG, SCs and STF in standard IEEE 33 and 69 RDN which are depicted in Fig 1 and Fig 2 is conferred in this section. In each IEEE RDN under consideration, three case studies are acquired to perform the proposed optimization problem such as installation of DG alone, installation of both DG and SCs and installation of DG SCs and STF using the software MATLAB R2022a. Whereas, the term installation in this section represents both sitting and sizing of energy components presented in this research work.

5.1 Analysis of HF-SOA in IEEE 33 RDN

The computational analysis of RDN is normally tested in reconfigured IEEE test systems. In this research study, two IEEE test systems with 33 and 69 nodes are considered for analysis purpose. The schematic layout of standard IEEE 33 bus considered in this research study is shown in Fig 1. The DG system considered in this research work includes 25MW of grid capacity with the fuel cost of 0.044 $/ /kWh, 1 MW of solar PV with the installation as well as operation and maintenance cost of 3985.0121 $/ /kWh and the 5 MW of wind turbine (WT) with the installation as well as operation and maintenance cost of 1822.0095 $/ /kWh [19, 26]. The optimal installation of DG, SCs and STF are analyzed with three case studies as follows:
Case 1: Optimal installation of DG alone
Case 2: Optimal installation of DG and SCs
Case 3: Optimal installation of DG, SCs and STF

(i) Case 1
The optimal DG installation alone is performed in this case using the HF-SOA algorithm, by averting harmonic parameter (Obj 3) in objective function (1) without violating the constraints. The harmonic load flow was simulated using MATLAB as a statistical method to account for uncertainty of input values. This problem represents the input data as random values from some specified, measured range. To work with and create a database for the proposed algorithm, the load flow method has been modified. A classical harmonic flow also takes into account the effect of background harmonics in the network. For HF-SOA, SSA and GMSA approaches, harmonic load flows are applied to systems with DG in three cases. To estimate different DG production losses, voltage drops, and THD online, the proposed HF-SOA is used. The optimized solutions are denoted in Table 1. These solutions confirms that the loss reduction obtained with the proposed HF-SOA is 68.31% with reference to the base case (without DG installation), which is higher than the results of SSA and GMSA approaches. Similarly, the maximum and minimum VP of the network is obtained as 0.9991 p.u and 0.9742 p.u correspondingly which is also higher than the results of the literature [18, 19]. Hence, the results confirms that the suggested HF-SOA algorithm outperforms SSA and GMSA approaches with, higher VP and less losses while installing the DG in bus numbers 13, 17, 24, 30 and 32 of an IEEE 33 bus networks, with the corresponding sizes denoted in Table 1.

Table 1: Case 1: Comparative analysis of optimal DG installation - IEEE 33 bus network

Optimization techniques	V_{min} (p.u)	V_{max} (p.u)	DG size (kW) and Placement (Bus Number)	Power Loss (kW)	Loss of reduction (%)
Base case	0.903	0.997	-	210.98	-
Proposed HF-SOA	0.9732	0.9991	541.32 (13), 301.20 (17), 978.74 (24), 505.54 (30), 407.61 (32)	66.84	68.31
SSA [19]	0.9686	0.9988	753.6 (13), 1100.4 (23), 1070.6 (29)	71.456	66.12
GMSA [18]	0.9725	0.9988	445.4 (29), 399.1 (10), 439.4 (15), 495.3 (25), 495.3 (26), 461.8 (32)	67.97	67.78

ii) Case 2

The SCs are also installed along with DG system in the same 33 node system and their installation criterions are optimized with the proposed HF-SOA algorithm in this case. The objective function preferred in case 1 is used for this case also. The optimal siting and sizing of DG as well as SCs are foreseeing by the HF-SOA and the resultant solutions are illustrated in Table 2. This table reveals that the network losses are considerably diminished to 7.56 kW (96.41%) with the proposed HF-SOA algorithm, which is precisely lesser than the power losses developed by SSA and GMSA approaches. Moreover, the total operating cost of the RDN with the proposed algorithm is evaluated as 236.51 $/h which is less than the operating cost of SSA (238.8 $/h). The minimum and maximum VPs are also enhanced to 0.9946 p.u and 1.0012 p.u which are comparatively higher than the alternate approaches depicted in Table 2 [18, 19]. Hence, it is confirmed that the HF-SOA could effectively reduce the power losses, operating cost, and maximize the VP compared to SSA and GMSA approaches while analyzing the DG and SCs installation in IEEE 33 network.

(iii) Case 3

The STF is installed along with DG and SCs in this case to support for harmonics mitigation. Whereas, the STF contains series connected resistor, inductor and capacitor and the configurations are directly referred from earlier research articles [17] such as C_m=29.8572μF, L_m=7.7793mH, R_m=0.2056Ω respectively. Fig 4 shows the waveform and harmonic spectrum of the source voltage waveform with a THD of 15.2314%, dominated by the 8th, 10th, and 12th harmonics. The THD of the source voltage and the perfor-

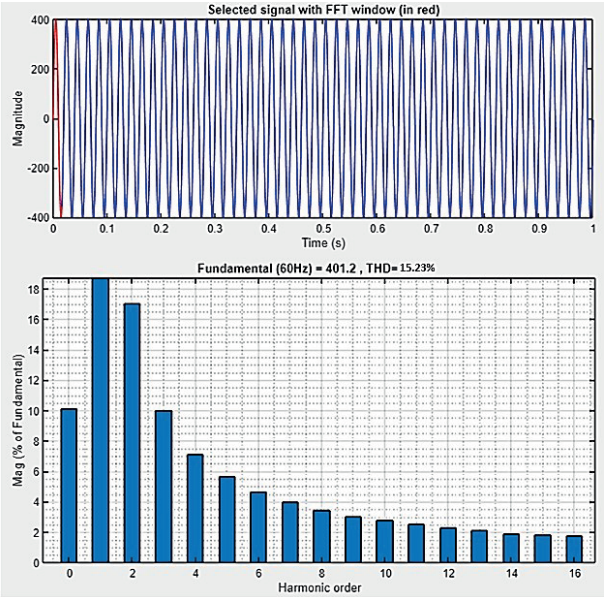


Figure 4: Source voltage waveform and its harmonic spectrum when passive filter connected

Table 2: Case 2: Comparative analysis of optimal DG and SCs installation - IEEE 33 bus network

Optimization techniques	V_{min} (p.u)	V_{max} (p.u)	Optimal DG installation (kW)	Optimal SCs installation (kVAr)	Power Loss (kW)	Loss of reduction (%)
Base case	0.903	0.997	-		210.98	-
Proposed HF-SOA	0.9946	1.0012	392.14 (13), 738.12 (24), 999.87 (29), 451.43 (32)	350 (13), 300 (23), 450 (29), 500 (32)	7.5651	96.41
SSA [19]	0.9918	1.0010	746.6 (13), 1078.9 (23), 1049.2 (29)	300 (13), 600 (23), 1050 (29)	11.8	94.41
GMSA [18]	0.9938	1.0010	418.2 (24), 474.8 (28), 478.6 (32), 448.7 (11)	600 (30), 350 (11), 450 (31), 150 (14)	7.94	96.24

mance can be improved by appending the passive filter into the existing passive filter system.

The optimal installation of filter in IEEE 33 RDN to minimize the objective function (1) that includes THD component is performed with the HF-SOA algorithm in this study. The solutions are presented in Table 3. This table reveals that the optimal location of STF is identified as bus 8 and the minimum and maximum THD values are obtained as 2.3221 and 4.3287 respectively. The graphical bar chart representation of THD level in each bus is depicted in Fig 5. The minimum and maximum THDs in the presence and absence of STF in bar chart are highlighted in brown and blue color in Fig 5. Similarly, the power loss also reduced by 96.48% with respect to the base case after the STF installation, which is comparatively higher than the power loss in base case and IEEE 33 network with only DG and SCs. In similar manner the minimum and maximum VPs are also enhanced after the installation of STF. The ECOST is also reduced from 316.58 $/h to 252.23 $/h which is nearly reduced to 20.64% with reference to the base case (without DG, SCs and STF) which ensures the reliability of operation after the installation of DG, SCs and STF. All the results clearly reveal that the proposed HF-SOA approach could effectively mitigate the harmonics after the installation of filter.

The comparative VPs of Case 1 Case 2 and Case 3 optimized with HF-SOA are shown in Fig 6(a) which evidently illustrates that the VP has been considerably improved in Case 3 and Case 2 related to Case 1. Hence, it is confirmed that, the VP is considerably enhanced after the installation of SCs as well as STF. The fig in 6(b) illustrates the reduction in the cost of DG system based on the analysis of the HF-SOA, the GMSA, the SSA and the base case of different cases in IEEE 33 RDN. As a result, the proposed method has a better performance than the existing.

The convergence of the proposed HF-SOA is examined with the five samples of power loss convergence characteristics for all the three cases. Here, the sample is considered as DG size and bus number in a test system. The power loss plot over consecutive iterations for five samples for Case 1, 2 and 3 are illustrated in Fig 7. It

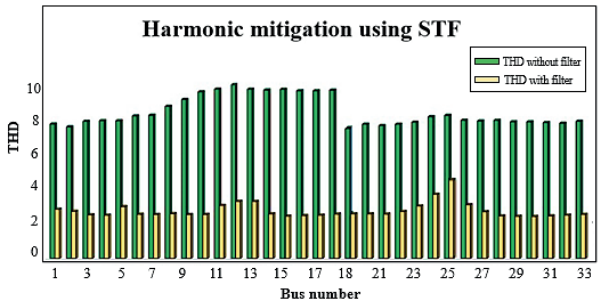
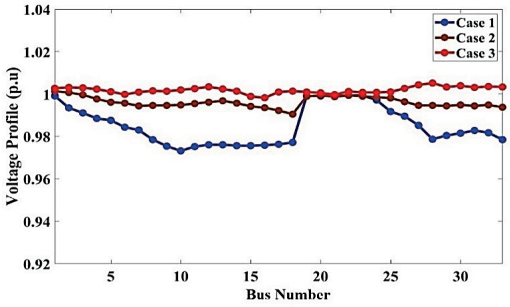


Figure 5: Percentage THD of bus voltage in IEEE 33 RDN

(a)



(b)

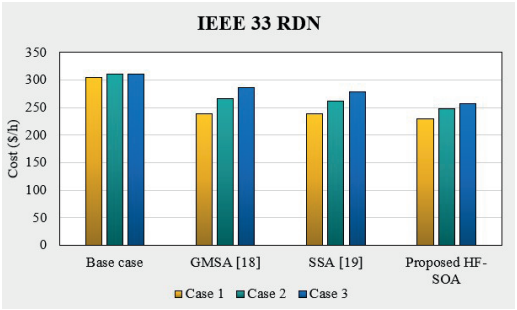


Figure 6: Comparative analysis of different cases in IEEE 33 RDN of (a) VP (b) DG cost

is evident from this figure that, fast convergence could be obtained with the proposed HF-SOA approach with minimum power loss in all the cases. The power loss at Case 3 is comparatively lower than other two cases. Hence, it is confirmed that fast convergence with least fitness values could successfully obtained with the proposed algorithm.

The Power losses, VP as well as the THD values for the three cases with and without filter are compared using

Table 3: Case 3: Comparative analysis of optimal DG, SCs, STF installation - IEEE 33 bus network

Condition	V_{min} (p.u)	V_{max} (p.u)	Filter Location	THDmax	THDmin	Power Loss (kW)	Loss of reduction (%)
Base case	0.9036	0.9971	-	15.2314	10.5269	210.98	-
With DG and SCs	0.9946	1.0010	-	9.6967	7.2924	7.5651	96.41
With DG, SCs and STF	0.9987	1.0052	8	4.3287	2.3221	7.4278	96.48

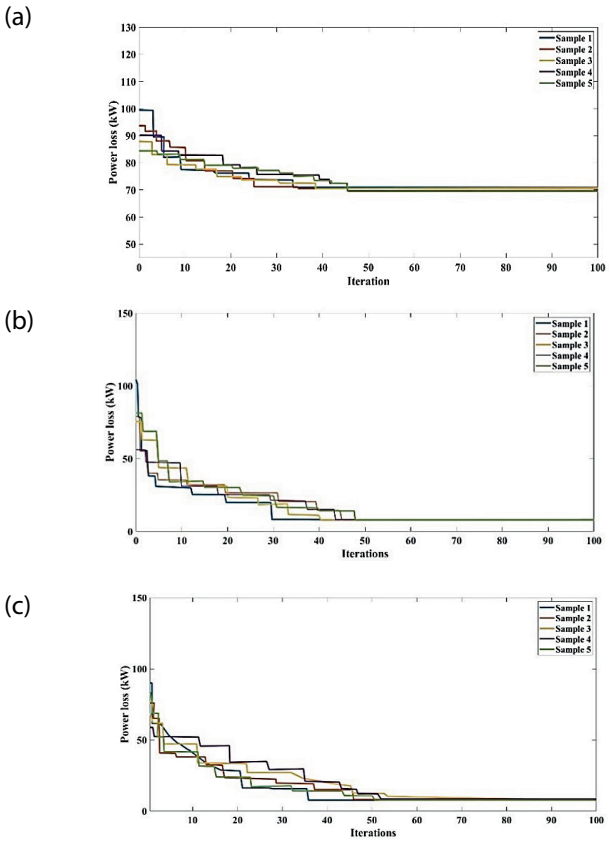


Figure 7: Power losses convergence - IEEE 33 bus system (a) Case 1(b) Case 2 (c) Case 3

bar chart analysis as illustrated in Fig 8. It is evidently clear from Fig 8(a) and Fig 8(b) that the minimum and maximum VPs are enhanced in Case 3 after the installation of DG, SCs and STF in IEEE 33 bus network related to Case 1 and 2. In similar manner, the Fig 8(c) reveals that the power loss is also considerably reduced in Case 3 compared to Case 1 and 2. Meanwhile, the comparative analysis of VP illustrated in Fig 8(b) evidently reveals that the presence of both SCs and STF could effectively minimize the THD values. Hence, the Fig 8 ensures that the presence of SCs and filters in power network could diminish the harmonics, losses and improve the VP. In similar manner, maximum THD values with and without filter is presented in Fig 8(c) clearly confirms the need of filter installation in power network for the purpose of harmonic mitigation.

5.2 Performance analysis on IEEE 69 RDN

The installation of DG, SCs and STF in 69 RDN shown in Fig 2 are optimized in this section using HF-SOA. Similar to the section 4.1 three cases are framed to examine the effectiveness of proposed HF-SOA algorithm in foreseeing the installation of DG, SCs and STF integrated in an IEEE 69 network.

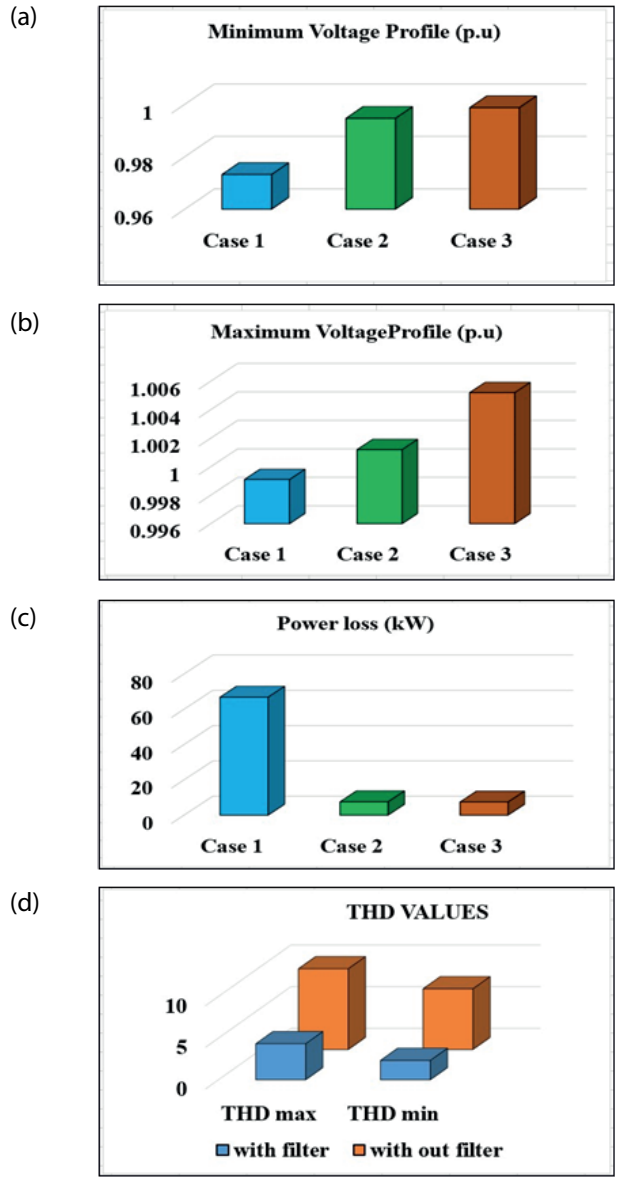


Figure 8: Comparative analysis of objective function parameters in three cases of IEEE 33 bus (a) Minimum voltage profile (b) Maximum voltage Profile (c) Power loss (d) THD values

Case 1: Optimal installation of DG alone
Case 2: Optimal installation of DG and SCs
Case 3: Optimal installation of DG, SCs and STF

The objective functions considered in the three cases of IEEE 33 bus study is considered in IEEE 69 bus also.

(i) Case 1
The installation of DG system in a 69 RDN is optimized in this case using the proposed HF-SOA approach and the solutions are represented in Table 4 which, reveals that the optimized siting of DG in IEEE 69 RDN using proposed HF-SOA approach are 17, 21, 42, 61 and 62 respectively. Meanwhile, the percentage reduction in

power losses is also stated as 70.25% which is higher than the SSA and GMSA algorithms. In the same way the minimum and maximum VPs are also improved to 0.9732 and 0.9991 respectively which is higher than the results of GMSA and SSA algorithms [18, 19]. Table 4 ensures that the proposed HF-SOA outperforms the earlier published articles. Hence, the dominance of the proposed HF-SOA is confirmed in this case study.

(ii) Case 2

Both DG and SCs are integrated in IEEE 69 bus system in this case, and their size as well as locations are optimized with HF-SOA algorithm. The resultant solutions are shown in Table 5. This table reveals that the optimal locations of DG in IEEE 69 bus system are 17, 23, 61 and 63 and the locations of SCs are 16, 35, 23 and 61, respectively. It is also revealed that the percentage power loss reduction (97.79%) is high in proposed approach compared to GMSA approach. The minimum and maximum VPs are also enhanced to 0.9986 and 1.0021 using the proposed hybrid algorithm, which is higher than the results documented earlier in the literature [18, 19]. From this case study, the dominance of HF-SOA over SSA and GMSA in optimizing the siting and sizing of DG and SCs in IEEE 69 bus system is evidently proved.

(iii) Case 3

The installation of STF along with DG and SCs in IEEE 69 RDN is discussed in this case for effective mitigation of harmonics. The STF with same configurations as discussed in IEEE 33 case study is considered in this case also. The bar chart representation of THD in each bus in this optimization process is depicted in Fig 9 which demonstrates that the optimal location of STF is identified as bus 37 and the minimum and maximum VP values are obtained as 0.9987 and 1.0032 respectively. The minimum THDs with and without STF in the bar chart representation are highlighted in brown and blue color in Fig 9. For detailed analysis the minimum and maximum THD values are from this figure and listed in Table 6. This table clearly describes that the harmonics are mitigated after the installation of STF in the bus number 37 which is optimized with the proposed intelligent algorithm. It is also revealed from the table that, the minimum and maximum THD values of the power network without DG, SCs and STF are 9.5126 and 17.2562 and this value has been reduced by 77.22 % and 49.92 % after the installation of DG and SCs which is further reduced to 84.49 % and 73.32 % after the installation of STF. In addition, the losses of the network also minimized by 97.83 % compared to base case. The ECOST is also reduced from 421.65 $/h to 314.23 $/h which is nearly reduced to 25.47% related to the base case. Thereby, the reliability is also ensured. This case study confirms the dominance of proposed HF-SOA approach over SSA and GMSA in terms of power loss, harmonics minimization and VP and reliability improvement.

The comparative voltage profiles of the three cases optimized using proposed HF-SOA approach is depicted in Fig 10 (a). This figure clearly describes that the VP is

Table 4: Case 1: Comparative analysis of optimal DG installation - IEEE 69 bus network

Optimization techniques	V_{min} (p.u)	V_{max} (p.u)	DG size (kW) and Placement (Bus Number)	Power Loss (kW)	Loss of reduction (%)
Base case	0.909	0.999	-	224.98	-
Proposed HF-SOA	0.9802	1.0010	341.32 (17), 524.65 (21), 387.23 (42), 542.34 (61), 687.32 (62)	66.9314	70.25
SSA [19]	0.9789	1.0003	380 (17), 527 (10), 1718 (60)	69.41	69.14
GMSA [18]	0.9725	0.9988	359.8 (53), 282.2 (67), 100.1 (42), 281.07 (62), 307.04 (60)	67.79	69.87

Table 5: Case 2: Comparative analysis of optimal DG and SCs installation - IEEE 69 bus network

Optimization techniques	V_{min} (p.u)	V_{max} (p.u)	Optimal DG installation (kW)	Optimal SCs installation (kVAr)	Power Loss (kW)	Loss of reduction (%)
Base case	0.909	0.999	-	-	224.98	-
Proposed HF-SOA	0.9986	1.0021	592.14 (17), 320.89 (23), 951.77 (61), 851.65 (63)	420 (16), 490 (35), 650 (23), 750(61)	4.9623	97.79
SSA [19]	0.9971	1.0010	358 (19), 518 (10), 1673.5 (60)	600 (11), 600 (48), 1200 (60)	4.837	97.85
GMSA [18]	0.9976	1.000	346.5 (69), 383.2 (18), 446.4 (62), 360.7 (58)	450 (50), 150 (48), 450 (61), 1200 (23), 150 (10)	5.093	97.74

Table 6: Case 3: Comparative analysis of optimal DG, SCs, STF installation - IEEE 69 bus network

Condition	Vmin (p.u)	Vmax (p.u)	Filter Location	THDmax	THDmin	Power Loss (kW)	Loss of reduction (%)
Base case	0.909	0.999	-	17.2562	9.5126	224.98	-
With DG and SCs	0.9986	1.0021	-	8.6426	2.1669	4.9623	97.79
With DG, SCs and STF	0.9987	1.0032	37	4.6032	1.4748	4.8656	97.83

considerably increased in third case compared to other two cases. Further, the convergence analysis of HF-SOA is also examined with IEEE 69 bus network by examining the most fundamental parameter of objective function called power loss for the three cases. The figure in 10(b) illustrates the reduction in the cost of DG system based on the analysis of the HF-SOA, GMSA, SSA and the base case of different cases in IEEE 69 RDN. As a result, the proposed HF-SOA method has a better performance than the existing.

The power loss plot over consecutive iterations for five samples for Case 1, 2 and 3 are illustrated in Fig 11. This figure ensures the earliest convergence of proposed algorithm with minimum fitness value. In addition, it is also observed that the fitness value of power loss in Case 3 is less when compared to other two cases. Hence, the convergence ability of the HF-SOA approach is proved while optimizing the installation of DG, SCs and STF in the 69 RDN.

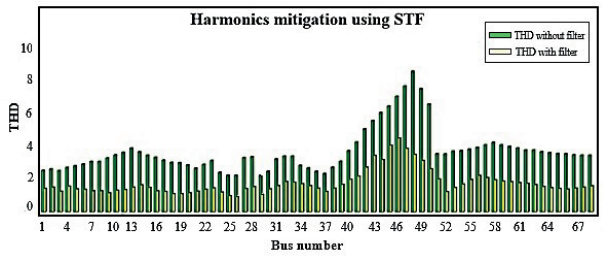


Figure 9: Percentage THD of bus voltage in IEEE 69 RDN

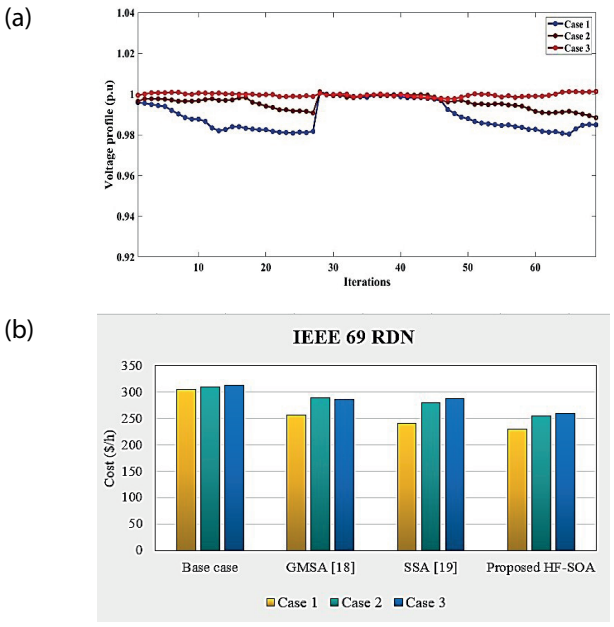


Figure 10: Comparative analysis of different cases in IEEE 69 RDN of (a) VP (b) DG cost

The comparative analysis of minimum and maximum VPs and power losses for the three cases as well as the THD values with and without filter are presented with the bar chart representation as depicted in Fig 12. Fig 12(a) and Fig 12(b) describes that the minimum and maximum VPs are enhanced in Case 3 after the installation of DG, SCs and STF in IEEE 69 bus network related to Case 1 and 2. In similar manner, it is understood from Fig 12(c) that the power loss is also considerably reduced in Case 3 compared to Case 1 and 2. In the same way, the Fig 12(d) confirms the mitigation of har-

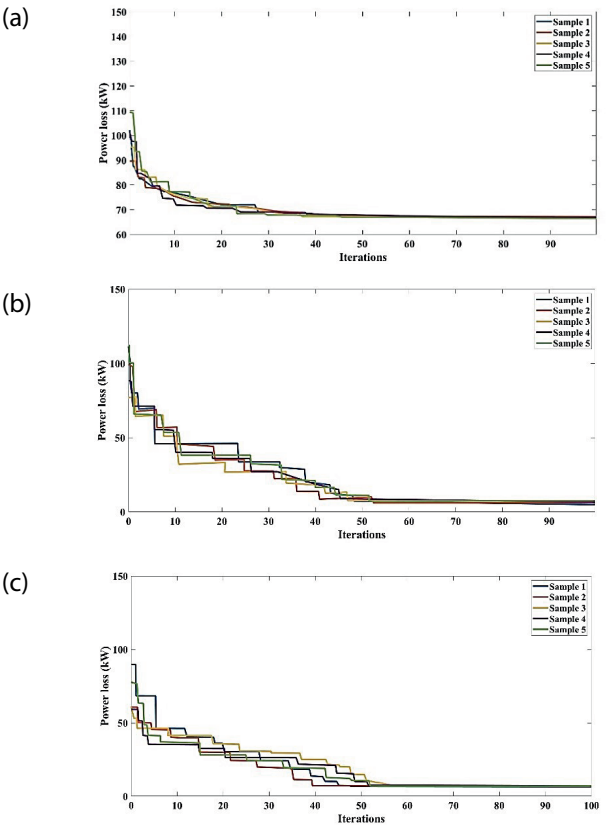
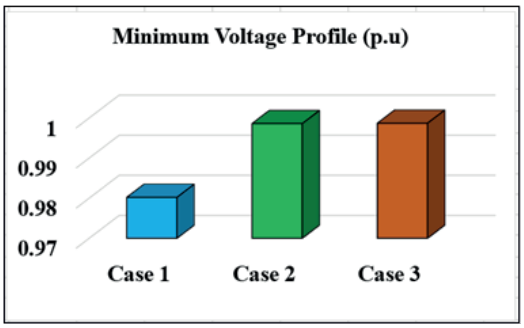
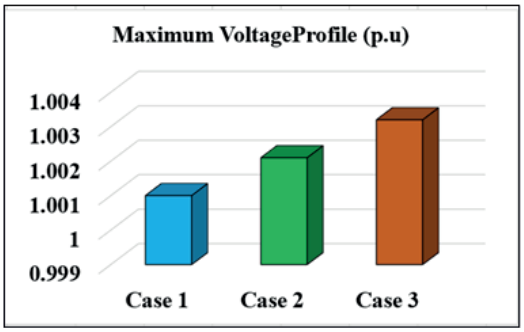


Figure 11: Convergence of power losses in IEEE 69 bus system (a) Case 1(b) Case 2 (c) Case 3

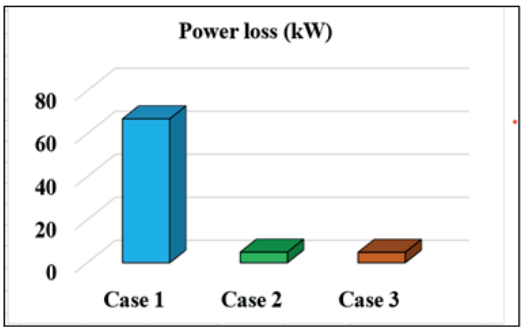
(a)



(b)



(c)



(d)

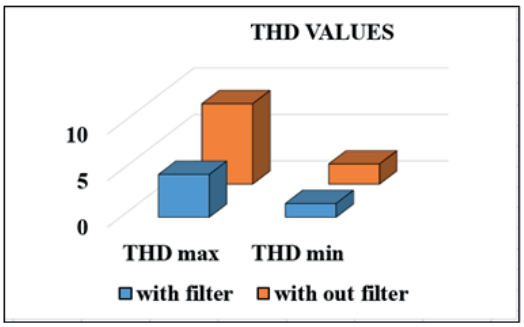


Figure 12: Comparative analysis of objective function parameters in three cases of IEEE 69 bus (a) Minimum voltage profile (b) Maximum voltage Profile (c) Power loss (d) THD values

monics after the installation of single tuned filter in Case 3. Hence the effectiveness of proposed HF-SOA in optimizing the siting and sizing of DG, SCs and STF is confirmed by this analysis.

6 Conclusion

A novel HF-SOA algorithm is proposed in this article to optimize the installation of DG, SCs and STF in a distributed network. The reduction of power losses, harmonics, and enhancement of VP and reliability are considered as the fundamental parameters in the proposed novel multi-objective function of this proposed research problem. Three case studies are conducted in standard IEEE network with 33 and 69 nodes, to examine the effectiveness of proposed intelligent algorithm. The results optimized with the HF-SOA in IEEE 33 bus system ensures that the power losses in Case 1, Case 2 and Case 3 are reduced by 68.31%, 96.41% and 96.48% respectively when compared to the base case. In the same way, the power losses are minimized by 70.25%, 97.79% and 97.83% compared to base case while optimizing with proposed intelligent algorithm. In addition, the minimum and maximum THD values are also reduced by 77.94% and 71.58% in IEEE 33 bus system and 84.49 % and 73.32 % in IEEE 69 bus system. The reliability enhancement is also proved with ECOST minimization which is reduced by 20.64% in 33 node and 25.47% in 69 node system. The effective VP enhancement is also achieved through the proposed intelligent algorithm. The results of convergence analysis revealed that earlier convergence could be obtained by the proposed HF-SOA approach with minimum power loss. Hence, with the proposed novel HF-SOA algorithm based on the novel fitness function, the optimal size and allocation of DG, SCs and STF are obtained successfully. This research work could be extended in near future with the following suggestions:

- In this research article, only the ECOST is considered in the objective function to improve the reliability however, the other cost parameters such as energy not supplied (ENS) could also be considered.
- In this article the filter parameters are referred from literature instead, they could be optimized along with siting of filters.

7 Acknowledgments

The Author with a deep sense of gratitude would thank the supervisor for his guidance and constant support rendered during this research.

8 Conflict of Interest

Authors do not have any conflicts.

9 References

1. T. Yuvaraj, K. Devabalaji, and K. Ravi, "Optimal allocation of DG in the radial distribution network

using bat optimization algorithm," in Advances in power systems and energy management: Springer., pp. 563-569, 2018, https://doi.org/10.1007/978-981-10-4394-9_55.
2. K. Varesi, "Optimal allocation of dg units for power loss reduction and voltage profile improvement of distribution networks using PSO algorithm," International Journal of Computer and Systems Engineering., vol. 5, no. 12, pp. 1847-1851, 2011.
3. S. R. Ghatak and P. Acharjee, "Optimal allocation of DG using exponentential PSO with reduced search space," in 2016 second international conference on computational intelligence & communication technology (CICT)., 2016, pp. 489-494: IEEE, https://doi.org/10.1109/CICT.2016.103.
4. H. HassanzadehFard and A. Jalilian, "Optimal sizing and location of renewable energy-based DG units in distribution systems considering load growth," International Journal of Electrical Power & Energy Systems., vol. 101, pp. 356-370, 2018 https://doi.org/10.1016/j.ijepes.2018.03.038.
5. E. A. Al-Ammar et al., "ABC algorithm based optimal sizing and placement of DGs in distribution networks considering multiple objectives," Ain Shams Engineering Journal., vol. 12, no. 1, pp. 697-708, 2021, https://doi.org/10.1016/j.asej.2020.05.002.
6. M. G. Hemeida, A. A. Ibrahim, A.-A. A. Mohamed, S. Alkhalaf, and A. M. B. El-Dine, "Optimal allocation of distributed generators DG based Manta Ray Foraging Optimization algorithm (MRFO)," Ain Shams Engineering Journal, vol. 12, no. 1, pp. 609-619, 2021, https://doi.org/10.1016/j.asej.2020.07.009.
7. S. G. Naik, D. Khatod, and M. Sharma, "Optimal allocation of combined DG and capacitor for real power loss minimization in distribution networks," International Journal of Electrical Power & Energy Systems., vol. 53, pp. 967-973, 2013, https://doi.org/10.1016/j.ijepes.2013.06.008.
8. S. R. Gampa and D. Das, "Simultaneous optimal allocation and sizing of distributed generations and shunt capacitors in distribution networks using fuzzy GA methodology," Journal of Electrical Systems and Information Technology., vol. 6, no. 1, pp. 1-18, 2019, https://doi.org/10.1186/s43067-019-0003-2.
9. T. Yuvaraj et al., "Optimal integration of capacitor and distributed generation in distribution system considering load variation using bat optimization algorithm," Energies., vol. 14, no. 12, p. 3548, 2021, https://doi.org/10.3390/en14123548.
10. A. R. Abul'Wafa, "Ant-lion optimizer-based multi-objective optimal simultaneous allocation of distributed generations and synchronous condensers in distribution networks," International Transactions on Electrical Energy Systems., vol. 29, no. 3, p. e2755, 2019, https://doi.org/10.1002/etep.2755.
11. A. Naderipour et al., "Spotted hyena optimizer algorithm for capacitor allocation in radial distribution system with distributed generation and microgrid operation considering different load types," Scientific reports., vol. 11, no. 1, pp. 1-15, 2021, https://doi.org/10.1038/s41598-021-82440-9.
12. S. C. Reddy, P. Prasad, and A. J. Laxmi, "Placement of distributed generator, capacitor and DG and capacitor in distribution system for loss reduction and reliability improvement," Editors-in-Chief., p. 198, 2013.
13. R. Baghipour and S. M. Hosseini, "Placement of DG and capacitor for loss reduction, reliability and voltage improvement in distribution networks using BPSO," International Journal of Intelligent Systems and Applications., vol. 4, no. 12, p. 57, 2012, https://doi.org/10.5815/ijisa.2012.12.08.
14. R. Baghipour and S. M. Hosseini, "Optimal placement and sizing of distributed generation and capacitor bank for loss reduction and reliability improvement in distribution systems," Majlesi Journal of Electrical Engineering, vol. 7, no. 3, pp. 59-66, 2013.
15. M. Salari and F. Haghighatdar-Fesharaki, "Optimal placement and sizing of distributed generations and capacitors for reliability improvement and power loss minimization in distribution networks," Journal of Intelligent Procedures in Electrical Technology., vol. 11, no. 43, pp. 83-94, 2020.
16. P. Reddy, V. Reddy, and T. G. Manohar, "Whale optimization algorithm for optimal sizing of renewable resources for loss reduction in distribution systems," Renewables: wind, water, and solar., vol. 4, no. 1, pp. 1-13, 2017, https://doi.org/10.1186/s40807-017-0040-1.
17. V. R. Pandi, H. Zeineldin, and W. Xiao, "Passive harmonic filter planning to overcome power quality issues in radial distribution systems," in 2012 IEEE Power and Energy Society General Meeting, 2012, pp. 1-6: IEEE, https://doi.org/10.1109/PESGM.2012.6345247.
18. E. A. Mohamed, A.-A. A. Mohamed, and Y. Mitani, "Hybrid GMSA for Optimal Placement and Sizing of Distributed Generation and Shunt Capacitors," Journal of Engineering Science & Technology Review., vol. 11, no. 1, 2018, https://doi.org/10.25103/jestr.111.07.
19. K. S. Sambaiah and T. Jayabarathi, "Optimal allocation of renewable distributed generation and capacitor banks in distribution systems using salp

swarm algorithm," International journal of renewable energy research., vol. 9, no. 1, pp. 96-107, 2019.
20. J. Liu et al., "Modelling and analysis of radial distribution network with high penetration of renewable energy considering the time series characteristics," IET Generation, Transmission & Distribution., vol. 14, no. 14, pp. 2800-2809, 2020, https://doi.org/10.1049/iet-gtd.2019.1874.
21. A. Lakum and V. Mahajan, "Optimal placement and sizing of multiple active power filters in radial distribution system using grey wolf optimizer in presence of nonlinear distributed generation," Electric Power Systems Research., vol. 173, pp. 281-290, 2019, https://doi.org/10.1016/j.epsr.2019.04.001.
22. B. Singh, K. Al-Haddad, and A. Chandra, "A review of active filters for power quality improvement," IEEE transactions on industrial electronics., vol. 46, no. 5, pp. 960-971, 1999, https://doi.org/10.1109/41.793345.
23. A. S. Abbas et al., "Optimal harmonic mitigation in distribution systems with inverter based distributed generation," Applied Sciences., vol. 11, no. 2, p. 774, 2021, https://doi.org/10.3390/app11020774.
24. A. Appathurai, et al., "An efficient optimal neural network-based moving vehicle detection in traffic video surveillance system," Circuits, Systems, and Signal Processing., vol.39, no.2, pp.734-756, 2020, https://doi.org/10.1007/s00034-019-01224-9.
25. P. Samal, "Optimal DSTATCOM Allocation Using a Hybrid Seagull-Differential Evolution Algorithm," in 2020 IEEE 17th India Council International Conference (INDICON)., 2020, pp. 1-6: IEEE, https://doi.org/10.1109/INDICON49873.2020.9342524.
26. A. A. Abou El-Ela, R. A. El-Sehiemy, and A. S. Abbas, "Optimal placement and sizing of distributed generation and capacitor banks in distribution systems using water cycle algorithm," IEEE Systems Journal., vol. 12, no. 4, pp. 3629-3636, 2018, https://doi.org/10.1109/JSYST.2018.2796847.
27. A. Rathore, and N.P. Patidar, "Optimal sizing and allocation of renewable based distribution generation with gravity energy storage considering stochastic nature using particle swarm optimization in radial distribution network," Journal of Energy Storage., vol. 35, pp. 102282, 2021, https://doi.org/10.1016/j.est.2021.102282.
28. R. Siddique, S. Raza, A. Mannan, L. Khalil, N. Alwaz, and M. Riaz, "A modified NSGA approach for optimal sizing and allocation of distributed resources and battery energy storage system in distribution network," Materials Today: Proceedings., vol. 47, pp. S102-S109, 2021. https://doi.org/10.1016/j.matpr.2020.05.669.
29. H. Lotfi, "Optimal sizing of distributed generation units and shunt capacitors in the distribution system considering uncertainty resources by the modified evolutionary algorithm," Journal of Ambient Intelligence and Humanized Computing., vol. 13, no. 10, pp. 4739-4758, 2022. https://doi.org/10.1007/s12652-021-03194-w
30. F. García-Muñoz, F. Díaz-González, and C. Corchero, 2021. "A novel algorithm based on the combination of AC-OPF and GA for the optimal sizing and location of DERs into distribution networks," Sustainable Energy, Grids and Networks., vol. 27, p.100497.s, https://doi.org/10.1016/j.segan.2021.100497
31. S.R. Salkuti, "Optimal allocation of DG and D-STATCOM in a distribution system using evolutionary based Bat algorithm," International Journal of Advanced Computer Science and Applications., vol. 12, no. 4, 2021,

Arrived: 15. 08. 2022
Accepted: 30. 12. 2022

Original scientific paper
https://doi.org/10.33180/InfMIDEM2023.103

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 53, No. 1(2023), 31 – 37

Liquid Metal Droplet Tunable RF MEMS Inductor

Issam El Gmati[1,2], Ridha Ghayoula[3]

[1]College of Engeneering Al Qunfudha Umm al Qura University, KSA
[2]Higher school of sciences and technology of Hammam Sousse, Tunisia
[3]Department of Electrical and Computer Engineering, Laval University, Quebec City, Canada

Abstract: A new variable inductor has been simulated, manufactured and tested. The idea is based on changing the morphology of a Galinstain droplet by electrostatic actuation. A drop of 200 µm diameter is used and the applied voltage is limited to 100 V. We demonstrate a tunable inductor that simultaneously achieves wide tuning range of 400 % with high inductance from 1.8 nH to 9.1 nH with a measured quality factor of 26 at 2 GHz and the self-resonance frequency is 4 GHz. Their results were compared. The conclusion showed that simulation results matched well with measurement. The Comparison between our work and other published works show excellent performance.

Keywords: Tunable inductor, radiofrequency, MEMS, droplet, Galinstain

Nastavljiva mikrofluidna RF MEMS tuljava

Izvleček: Simuliran, izdelan in preizkušen je bil nova spremenljiva tuljava. Zamisel temelji na spreminjanju morfologije kapljice Galinstain z elektrostatičnim vzbujanjem. Uporabljena je kapljica s premerom 200 µm, napetost pa je omejena na 100 V. Prikazali smo nastavljivo tuljavo, ki hkrati dosega široko območje nastavitve 400 % z visoko induktivnostjo od 1,8 nH do 9,1 nH z izmerjenim faktorjem kakovosti 26 pri 2 GHz, samorezonančna frekvenca pa je 4 GHz. Njihovi rezultati so bili primerjani. Zaključek je pokazal, da se rezultati simulacije dobro ujemajo z meritvami. Primerjava med našim delom in drugimi objavljenimi deli je pokazala odlično učinkovitost.

Ključne besede: nastavljiva tuljava, radio frekvenca , MEMS, kaplica, Galinstain

** Corresponding Author's e-mail: iagmati@uqu.edu.sa*

1 Introduction

Passive RF MEMS (Radiofrequency Micro-Electro-Mechanical Systems) components play a primary role in modern transceiver and receiver architectures. They provide significant gains in terms of miniaturization, motivating performance in the gigahertz band as well as low power consumption. Many MEMS components have been developed for radio frequency application; in particular inductors. Micro inductors are used in, for example, RF MEMS [1–8], micro-actuators [9-11], bio-sensors [12], micro-actuators [13], power MEMS [14], energy harvesters [15], transformers and electromagnetic motors [16]. Most inductors have fixed inductance value. The new generations of communications systems, on the other hand, aim to use very wide frequency bands to simplify these systems, reduce the number of transmission / reception channels, and consequently reduce their costs. To achieve these goals, it is important to replace fixed components with variable components. [17]. Variable inductors have the same performance as fixed inductors; to vary inductance. We can play on several geometric or technological parameters as well as on the variation techniques [18]. In the work [19] and in order to vary the inductance having discrete values, the researchers used micro-relays. Other techniques have been invented by modifying the magnetic flux [20-21], or by playing on mutual inductance [22-23]. Other works have proposed the micro-fluidic action by using liquids [24-26]. The common objective of all this work is to achieve a good variation of the inductance, a good quality factor as well as a high resonant frequency in the gigahertz band allowing the integration of these components in the application devices. Until today, none of the published structures have corresponded to our objectives, namely a high variation ratio, a good quality factor, a

How to cite:
I. El Gmati et al., "Liquid Metal Droplet Tunable RF MEMS Inductor", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 53, No. 1(2023), pp. 31–37

variable inductance working in the gigahertz bands. In order to achieve our goals, we were able to design a new method to vary the inductance. The idea is to slide a droplet of Galinstain horizontally above the inductor and control it by electrostatic actuation. The structure is manufactured and tested. Good performances have been shown.

2 Design of inductance

Figure 1 shows the model of the designed inductance and the principle used to vary the inductance. The structure consists of a planar spiral inductor and a liquid metal such as Galinstain. The metal drop is placed above the spiral inductor.

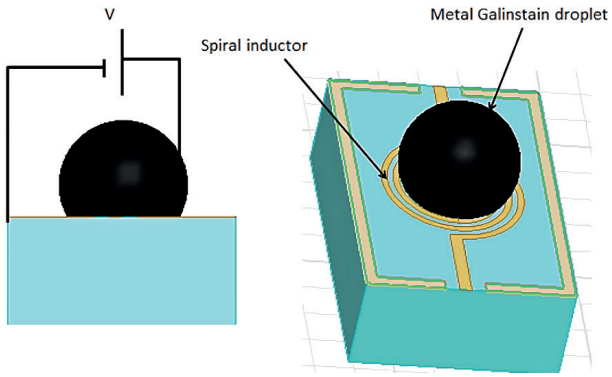


Figure 1: Model of the designed inductance and principle used to vary the inductance.

The planar inductor fabricated on a glass substrate; designed in double circular form with 3 turns with a coil 20 µm wide, spaced 20 µm. The length of the internal diameter is 600 µm so the external one is 1200 µm. The basic idea is to place a drop above the metal coils and thus modify the geometric parameters of the inductance by short-circuiting a portion of the coil. This allows a reduction in the current path and consequently a change in the inductance value. Figure 2 shows the steps followed in a clean room to fabricate the inductor. The gold coils were deposited on a glass substrate. This manufacturing process requires 3 masks.

A Ti/Au (500 Å/500 Å) seed layer was regularly popped on highest side of a 500 µm thick glass substrate. The Ti layer was placed to improve the bond, and a positive photoresist (AZ 4562) was next spotted in order to form the electroplating mould (thickness ≈ 5.5 µm). A 2 µm thick gold were electroplated into the resist mould. The photoresist mould was then removed and the seed layer was chemically etched. Finaly, a droplet of 200 µm is used and the applied bias voltage is limited to 100 V. Figure 3 shows a top view of the circular shaped inductor made of gold on a glass substrate.

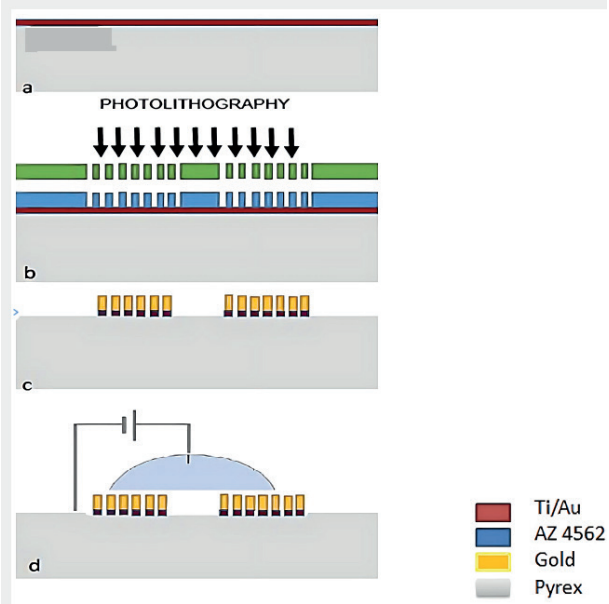


Figure 2: Schematic cross section of the fabricated inductor.

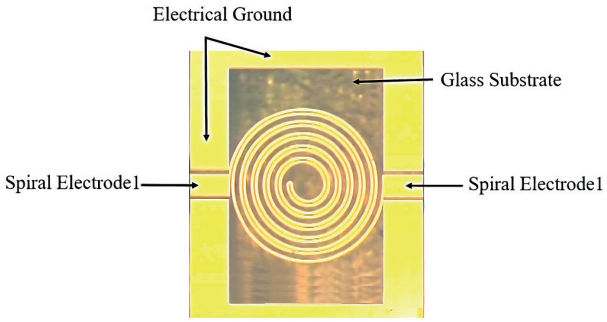


Figure 3: Photography of one inductor under fabrication.

Table 1 shows physical properties of materials used in fabrication process.

Table 1: Physical properties of materials used in fabrication process.

Materials	Relative Permittivity	Dielectric Loss	Relative Permeability	Bulk Conductivity (S/m)
Glass	5.5	0.0037	1	0
Gold	1	0	0.99996	41E6

3 Results and discussion

This section may be divided by subheadings. It should provide a concise and precise description of the experi-

mental results, their interpretation, as well as the experimental conclusions that can be drawn. The measurements shown in figure 4 were carried out under spikes with a vector network analyzer (VNA 'Vector Network Analyzer') HP 8510 which has a frequency range of 50 MHz-13 GHz using GSG 'Ground Signal Ground' microprobe RF tips. The inductance L and the quality factor Q were calculated by using the following equations [27]

$$L = \frac{1}{2\pi f} Im\left(\frac{1}{Y_{11}}\right) \quad (1)$$

$$Q = \frac{Im\left(\frac{1}{Y_{11}}\right)}{Re\left(\frac{1}{Y_{11}}\right)} \quad (2)$$

Y^{ind}, Y^{meas} and Y^{open} are the two-port admittance matrix the admittance matrices of the measured inductor and the open pattern, respectively.

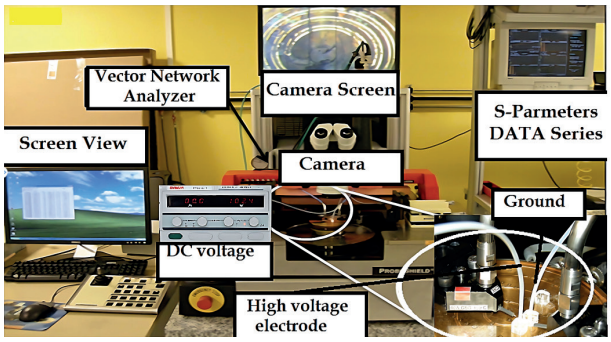


Figure 4: Test bench for S-parameters characterization.

During the measurements droplets of Galinstain [28] with conductivity of the order than 3.46 10^6 S/m at 20° C were used. The inductance varies by touching the liquid metal droplet upon the spiral inductor shown in figure 5. The Galinstain droplet is flattening out as applying a voltage. Measurements were taken for 6 voltage levels applied to the liquid metal droplet for a frequency span of 100 MHz to 10 GHz.

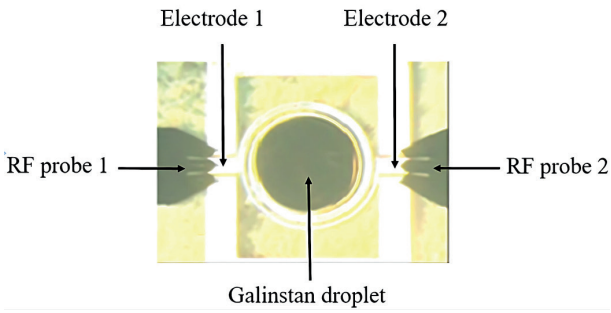


Figure 5: Galinstain droplet placed above the spiral inductor for different applied voltage.

As shown in figure 6 (a) the inductor has a peak of 25 at 2 GHz, and the self-resonance frequency is 4 GHz. The quality factor decreases from Q_{max} = 26 when the applied voltage is 100 V to Q_{min} = 12 when it is equal to 0 V. As demonstrated in figure 6(b), the measured inductance at high frequency increases continuously between L_{min} =1.8 nH and L_{max} = 9.1 nH at 2 GHz by applying voltage. A 400 % tuning range is achieved at 2 GHz.

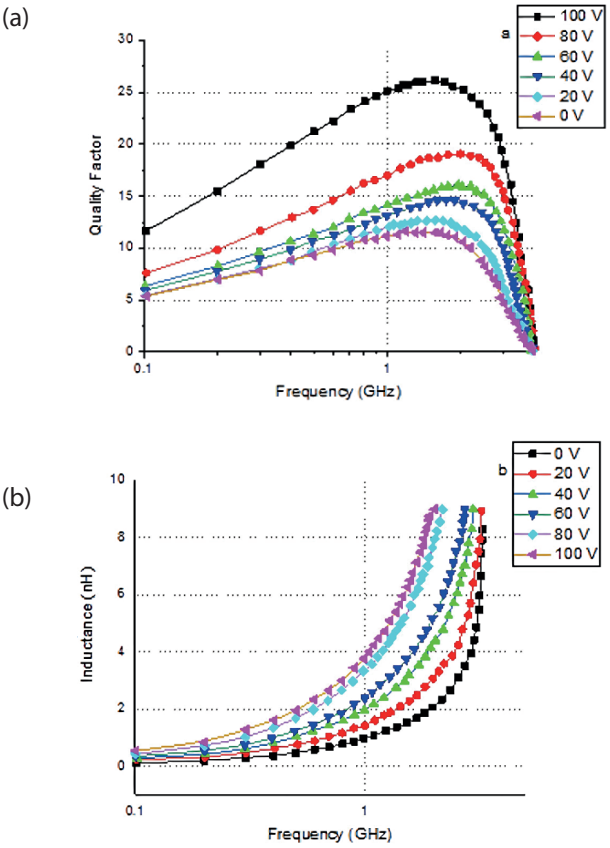
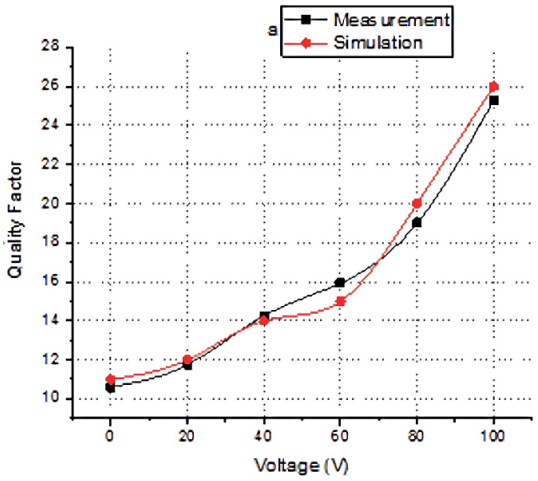


Figure 6: Measured results a Quality factor by frequency (a) and inductance (b) of a fabricated tunable RF MEMS inductor by applied voltage.

HFSS (3D Electromagnetic Field Simulator for RF and Wireless Design) software was used to simulate an inductor 3D model structure. Figures 6 show the variations of the measured results as a function of the voltage at a frequency of 2 GHz.

When the Galinstain droplet is present on the metal coils, it short-circuits a portion of the coil allowing a reduction in the number of coils of the inductance and subsequently a decrease in the value of the inductance. On the other hand, this reduction in the number of turns allows an increase in the quality factor shown in figure 7(a). The inductance L varies proportionally as a function of the number of coils N. The variation in the quality factor is inversely proportional to N.

(a)



(b)

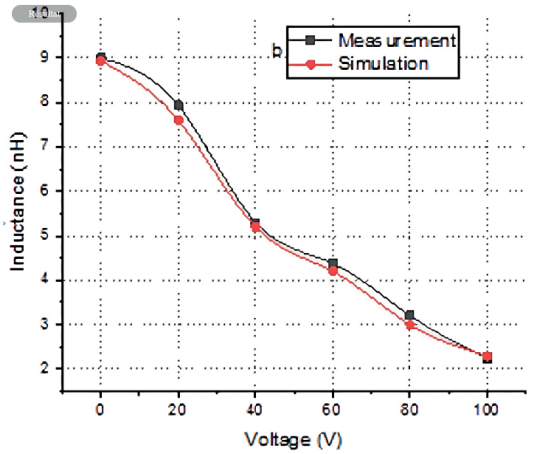


Figure 7: Comparison between simulated and measured inductance (a) and Quality Factor (b) of the tunable inductance at 2 GHz by applied voltage.

Variations in inductance shown in figure 7 (b) values have been visualized for different Galinstain contact pins on metal coils. You can notice a slight difference of around 5% between the measurement results and the simulation results. This can be attributed to other factors due to the existence of an external potential. The position of the liquid droplet above the metal coil may cause this slight difference. In fact, the drop can either be in direct contact with the gold turns, or it can form a capacitive contact through a thin layer.

In the presence of the Galinstain droplet, the magnetic flux of the inductance infiltrates the Galinstain droplet causing the creation of an eddy current inducing a counteractive magnetic field according to Lenz's law causing magnetic loss. When the droplet is moved away from the metal spires, the inductance exhibits very low loss.

A comparison of the measurement results of this variable inductance with others published and presented in Table 2.

Table 2: Performance comparison published works and our work.

Operating Frequency GHz	Inductance	Quality fac tor	Tunability%	Ref
6	1.1	46	47.5	[29]
1	8.86	25.5	27.7	[30]
2.5	3.3	>20	230	[31]
2	0.93	0.96	10	[32]
1.5	1.2	2.87	191	[33]
4	0.3	8	60	[34]
5	1.2-2.3	38.2	90	[35]
4	2.8	18	380	[36]
2	1.8-9.1	26	400	This work

We can notice that our inductor showed good performance in terms of variation, quality factor as well as reasoning frequency by comparing it with other works. The inductance produced is an ambitious solution in terms of small size in micrometers, energy consumption, low cost meeting the objectives set at the beginning such as a good inductance variation of the order of Nano-henry, a good quality factor in the Gigahertz frequency band and a resonance frequency of the order of Giga-hertz. The works cited in Table 1; not been able to group all these constraints together. To implement this inductor in real applications, you would need a wrapper or something to keep the liquid metal from moving around.

The inductance is modelled by L_s, and the finite conductivity of the metal is represented with the series resistance R_s. The capacitive coupling of the windings between the input and output is modelled by C_s shown in Figure 8.

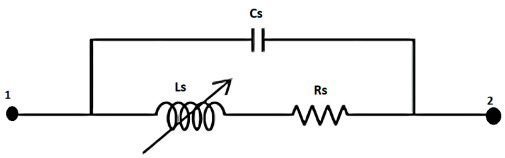


Figure 8: Electric Equivalent model for tunable inductor.

The compact model was fitted to the measured S-parameters. The fitted model parameters for different applied voltage are listed in Table 3.

Table 3: Fitted compact model parameters from Measured.

Frequency GHz	Applied voltage	Ls (nH)	Rs (Ω)	Cs (fF)
2	0	9.1	10	0.83
2	20	8	13	0.85
2	40	5.25	15	0.87
2	60	4.3	17	0.91
2	80	3.1	20.4	0.98
2	100	1.8	24	1.01

The fitted L_s correspond to the measured results in Figure 6 (b). The R_s does fluctuate with injected fluid, indicating that the proximity effect of neighboring conductors induces some losses. The compact model of the inductor serves as a reasonable approximation for low frequency performance and gives some insight on the effects of the parasitic. The R_s does fluctuate with applied voltage, indicating that the proximity effect of neighboring conductors induces some losses. The C_s is very low since there is no coupling with an underlying metal layer, and the crosstalk between adjacent turns is not significant.

4 Conclusion

In this work a new variable inductor was designed, manufactured and tested. A liquid metal was used to vary the inductance. The fabricated tunable RF inductor demonstrates a wide tuning range of 400%. Inductance varied between 1.8 nH and 9.1 nH with a measured quality factor of 26 at 2 GHz, and the resonant frequency is 4 GHz. Variable inductance can be exploited in the design of mobile communication systems for new compatibility and improved electrical performance over a wide range and frequency. The Inductor considered ambitious in terms of small size, power consumption and low cost. To implement this inductor in real applications, you would need some packaging or something to prevent liquid metal from moving.

5 Acknowledgments

The authors would like to thank the Deanship of Scientific Research at Umm Al-Qura University.

Funding: The authors would like to thank the Deanship of Scientific Research at Umm Al-Qura University for supporting this work by GRANT Code 23UQU4361156DSR02

6 Conflict of Interest

The authors declare no conflict of interest

7 References

1. Yao JJ. RF MEMS from a device perspective. Journal of Micromechanics and Microengineer- ing 2000; 10: 9–38.
2. Yoon JB, Kim BK, Han CH et al. Surface micromachined solenoid on-Si and on glass inductors for RF applications. IEEE Electron De- vice Letters 1999; 20: 487–489.
3. Kral A, Behbahani F, Abidi AA RF-CMOS oscillators with switched tuning. Proceedings of the IEEE in Custom Integrated Cir-cuits Con- ference; Santa Clara, CA; 1998: 555-558.
4. Young DH, Malba V, Ou JJ et al. A low-noise RF voltage-controlled oscillator using on-chip high Q three dimensional coil inductor and micro machined variable capacitor. Proceedings of the Solid-State Sensor and Actuator Work- shop; Cleveland, OH, USA; 1998: 128-131.
5. J. J. Yao, "RF MEMS from a device perspective," Journal of Micromechanics and Micro engineering, vol. 10, no. 4, pp. 9–38, Dec. 2000. https://doi.org/10.1088/0960 -1317/10/4/201.
6. J.-B. Yoon, B.-K. Kim, C.-H. Han, E. Yoon, and C.-K. Kim, "Surface micro machined solenoid on-Si and on-glass inductors for RF applications," IEEE Electron Device Letters., vol. 20, no. 9, pp. 487–489, Sep. 1999. https://doi.org/10.1109/55.784461.
7. Yasser Mafinejad, Abbas Kouzani, Khalil Mafinezhad, «Review of low actuation voltage RF MEMS electrostatic switches based on metallic and carbon alloys», Journal of Microelectronics, Electronic Components and Materials, Vol. 43, No. 2 (2013), 85 – 96.
8. Alireza Ardehshiri, Gholamreza Karimi, Ramin Dehdasht-Heydari, «Optimization of shunt capacitive RF MEMS switch by using NSGA-II algorithm and utility algorithm» Journal of Microelectronics, Electronic Components and Materials, Vol. 49, No. 1(2019), 43 – 50,
9. Ahn CH, Allen MG. A planar micro machined spiral inductor for integrated magnetic micro actuator applications. Journal of Micromechanics and Micro engineering 1999; 3: 37–44.
10. Fulcrand R, Bancaud A, Escriba C et al. On chip magnetic actuator for batch-mode dynamic manipulation of magnetic particles in compact lab-on-chip. Sensors and Actuators B: Chemical 2011; 160: 1520–1528.

11. Olivo J, Carrara S, De Micheli G. Micro-fabrication of high-thickness spiral inductors for the remote powering of implantable biosensors. Microelectronic Engineering 2014; 113: 130–135.
12. S. S. Bedair, J. S. Pulskamp, C. D. Meyer, M. Mirabelli, R. G. Polcawich, and B. Morgan, "High-performance micro machined inductors tunable by lead zirconate titanate actuators," IEEE Electron Device Lett., vol. 33, no. 10, pp. 1483–1485, Oct. 2012. https://doi.org/10.1109/LED.2012.2207700.
13. M. B. Coskun, K. Thotahewa, Y.-S. Ying, M. Yuce, A. Neild, and T. Alan, "Nanoscale dis- placement sensing using micro fabricated variable inductance planar coils," Appl. Phys. Lett., vol. 103, Oct. 2013, Art. no. 143501. https://doi.org/10.1063/1.4823828.
14. Araghchini M, Member S, Chen J et al. A technology overview of the power chip development program. IEEE Transactions on Power Electronics 2013; 28: 4182–4201
15. R. Wu, J. Chen, and X. Fang, "A novel on-chip transformer with patterned ground shield for high common-mode transient immunity isolated signal transfer," IEEE Electron Device Lett., vol. 39, no. 11, pp. 1712–1715, Nov. 2018. https://doi.org/10.1109/LED.2018.2871049.
16. Y. Wang, Q. Zhang, L. Zhao, Y. Tang, A. Shkel, and E. S. Kim, "Vibration energy harvester with low resonant frequency based on flexible coil and liquid spring," Appl. Phys. Lett., vol. 109, no. 20, 2016, Art. no. 203901. https://doi.org/10.1063/1.4967498.
17. J. Y. Park and J. U. Bu, "Packaging compatible micro transformers on a silicon substrate," IEEE Trans. Adv. Packag., vol. 26, no. 2, pp. 160– 164, May 2003. https://doi.org/10.1109/tadvp.2003.817341.
18. Yen-Chung Chiang and al, "A Study on the Variable Inductor Design by Switching the Main Paths and the Coupling Coils" Electronics 2021, 10, 1856. https://doi.org/10.3390/electronics10151856
19. Y. Yokoyama, T. Fukushige, S. Hata, K. Masu, and A. Shimokohbe,"On-chip variable inductor using micro electromechanical systems technology," Jpn. J. Appl. Phys., vol. 42, no. 4B, p. 2190, 2003.
20. S. Zhou, X.-Q. Sun, and W. N. Carr, "A micro variable inductor chip using MEMS relays," in Proc. Chicago Int. Conf. Solid State Sens. Actuators TRANSDUCERS, vol. 2. Jun. 1997, pp. 1137–1140.
21. H. Sugawara, Y. Yoshihara, H. Ito, K. Okada, and K. Masu, "Wide range RF variable inductor on Si CMOS chip with MEMS actuator," in Proc. 34th Eur. Microw. Conf., Oct. 2004, pp. 701–704.
22. H. Sugawara and al, "Variable RF inductor on Si CMOS chip," Jpn. J. Appl. Phys., vol. 43, no. 4B, pp. 2293–2296, 2004.
23. J. M. Dell, K. Winchester, C. A. Musca, J. Antoszewski, and L. Faraone, "Variable MEMS based inductors fabricated from PECVD silicon nitride," in Proc. Conf. Optoelectron. Microelectron. Mater. Devices, Dec. 2002, pp. 567–570.
24. V. M. Lubecke, B. Barber, E. Chan, D. Lopez,M. E. Gross, and P. Gammel, "Self-assembling MEMS variable and fixed RF inductors," IEEE Trans. Microw. Theory Techn., vol. 49, no. 11, pp. 2093–2098, Nov. 2001.
25. B. Assadsangabi, M. S. Mohamed Ali, and K. Takahata, "Ferrofluidbased variable inductor," in Proc. IEEE 25th MEMS Conf., Jan./Feb. 2012, pp. 1121–1124.
26. I. E. Gmati et al., "Fabrication and evaluation of an on-chip liquid micro-variable inductor," J. Micromech. Microeng., vol. 21, no. 2, p. 025018, 2011.
27. Jyh-Chyurn Guo and Teng-Yang Tan, "A Broadband and Scalable Modelfor On-Chip Inductors Incorporating Substrate and Conductor Loss Effects". IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 3, MARCH 2006.
28. Ahlberg, P. et al. Graphene as a Diffusion Barrier in Galinstain-Solid Metal Contacts. IEEE Trans. Electron Devices 1–5 (2014).
29. F. Khan, Y. Zhu, J. Lu, and J. Pal, "MEMS- based tunable meander inductor," Electron. Letters vol. 51, no. 20, pp. 1582–1583, Oct. 2015. https://doi.org/10.1049/el.2015.2495
30. A. Bhattacharya, D. Mandal, and T. K. Bhattacharyya, "A 1.3–2.4-GHz 3.1-mW VCO using electro-thermo-mechanically tunable self-assembled MEMS inductor on HR substrate," IEEE Trans. Microw. Theory Techn., vol. 63, no. 2, pp. 459–469, Feb. 2015 https://doi.org/10.1109/TMTT.2014.2380357
31. A. Shirane, H. Ito, N. Ishihara, and K. Masu, "Planar solenoid inductor in radio frequency micro-electro-mechanical systems technology for variable inductor with wide tunable range and high quality factor," Jpn. J. Appl. Phys., vol. 51, no. 5S, p. 05EE02, May 2012. https://doi.org/10.1143/JJAP.50.05EE01
32. Tengxing W; Wei J; Ralu D; Daniel R; Leonidas E. O; Yujia P;Guoan W "Novel electrically tunable microwave solenoid inductor and com- pact phase shifter utilizing permaloy and PZT thin films," IEEE Trans. Microw. Theory Techn., vol. 65, no. 10, pp. 3569–3577, Oct. 2017. doi https://doi.org/10.1109/TMTT.2017.2731765
33. H.Chen,X. Wang, Y. Gao, X. Shi, Z. Wang, N. Sun, M. Zaeimbashi, X. Liang, Y. He, C. Dong,Y. Wei, J.G. Jones, M.E. McConney, M.R. Page, B.M. Howe, G.J. Brown, N.-X. Sun "Integrated Tunable Magnetoelectric RF Inductors". IEEE Trans. Microw. Theory Tech. 2020

https://doi.org/10.1109/TMTT.2019.2957472
34. Yen-Chung Chiang, Juo-Chen Chen and Yu- Hsin Chang « A Study on the Variable Inductor Design by Switching the Main Paths and the Coupling Coils» Electronics 2021, 10, 1856. https://doi.org/10.3390/electron- ics10151856
35. Alexander M. Watson; Thomas F. Leary; Jonathan Itokazu; Aji G. Mattamana; Tony Quach; Aaron T. Ohta; Wayne A. Shiroma; Christopher E. Tabor "Tunable Microwave Inductor Using Liquid-Metal Microfluidics" 2021 IEEE Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS), May 2021.
36. N. Lazarus and S. S. Bedair, "Bubble inductors: pneumatic tuning of a stretchable inductor," AIP Advances, vol. 8, p. 056601, 2018.

Arrived: 21. 09. 2022
Accepted: 23. 02. 2023

Original scientific paper
https://doi.org/10.33180/InfMIDEM2023.104

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 53, No. 1(2023), 39 – 48

Power and Area Efficient Sense Amplifier Based Flip Flop with Wide Voltage and Temperature Upholding for Portable IoT Applications

Prashant Teotia, Owais Ahmad Shah

Department of Electronics & Communication Engineering, Noida International University, Gautam Budh Nagar, Uttar Pradesh, India

Abstract: A sense amplifier based flip-flop (SAFF) capable of operating unfailingly at wide voltage and temperature ranges is proposed in this work. The proposed flip-flop (FF) has a single ended latch design which results in a significant improvement in power and area requirements. The modified sense amplifier along with the single ended latch design enables robust and low power operation at all variations in the input data activity. The proposed SAFF is developed in 32nm CMOS technology, and a thorough and conclusive investigation with corner case simulation for wide process, voltage and temperature (PVT) variations is carried out in order to verify the design utilization. Comprehensive comparison and analysis with previously available state-of-the-art SAFFs validate that the proposed SAFF is functional at wide voltage ranges for temperature changes of 120 ° to -40 ° while upholding better and optimal power and power delay product (PDP) results. The proposed FF, because of its power efficiency, is best suited for portable Internet of Things (IoT) devices.

Keywords: low power design; CMOS digital circuit; sense amplifier based flip-flop; single ended; IoT

Energetsko in prostorsko učinkovit senzorski ojačevalnik na osnovi flip flopa s širokim razponom napetosti in temperature za prenosne aplikacije interneta stvari

Izvleček: V članku je predlagan flip-flop, ki temelji na senzorskem ojačevalniku (SAFF) in lahko deluje brezhibno v širokem razponu napetosti in temperature. Predlagan flip-flop (FF) ima enonivojski zapah, kar znatno izboljša zahteve po moči in površini. Spremenjen ojačevalnik zaznavanja skupaj z enonivojskim zapahom omogoča zanesljivo delovanje z nizko porabo energije pri vseh spremembah vhodne podatkovne aktivnosti. Predlagani SAFF je razvit v 32 nm tehnologiji CMOS, za preverjanje uporabe zasnove pa je opravljena temeljita in prepričljiva raziskava s simulacijo robnih primerov za velike spremembe procesa, napetosti in temperature (PVT). Obsežna primerjava in analiza s predhodno razpoložljivimi najsodobnejšimi SAFF potrjujeta, da je predlagani SAFF funkcionalen v širokem razponu napetosti za temperaturne spremembe od 120 ° do -40 °, hkrati pa zagotavlja boljše in optimalne rezultate glede moči in zakasnitve moči (PDP). Predlagani FF je zaradi svoje energetske učinkovitosti najprimernejši za prenosne naprave interneta stvari (IoT).

Ključne besede: zasnova z nizko porabo energije; digitalno vezje CMOS; flip-flop, ki temelji na senzorskem ojačevalniku; enonivojsko vezje; internet stvari

** Corresponding Author's e-mail: mail_owais@yahoo.co.in*

How to cite:
P. Teotia et al., "Power and Area Efficient Sense Amplifier Based Flip Flop with Wide Voltage and Temperature Upholding for Portable IoT Applications", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 53, No. 1(2023), pp. 39–48

1 Introduction

Smart and IoT based technologies have advanced swiftly, creating a wide range of prospects for technological advances in many different areas of life. The main goals of IoT technologies are to improve quality of life, ensure improved system (or process) efficiency, and streamline processes across a range of industries. IoT technologies are rapidly evolving and providing a number of beneficial outcomes, but in order to prevent negative environmental effects and ensure the sensible use of limited global resources, this rapid development must be closely monitored and analyzed from an environmental point of view [1]. In the former sense, significant research is required to thoroughly examine the benefits and drawbacks of IoT technologies. For IoT applications like wearable technology and portable medical equipment, on-chip security mechanisms are essential [2]. Memory offers a physically unclonable function that can be employed in security implementation. Problems with resistive RAM memory applications stem from its stochastic switching process and the resistance's inherent unpredictability. For use in smart mote devices, biomedical implants and wireless sensor nodes, the present IoT era requires ultra-low power System on Chip (SoC) designs and architectures [3].

In modern digital circuit design, flip-flop is the critical part of most essential circuit components since they synchronize data flow and allow for local data storage [4]. A typical processor requires a lot of flip-flops, often hundreds of thousands, because this synchronization must take place across the whole clock domain [5]. Due to their high density, flip-flops consume a substantial amount of both space and power in the overall circuit architecture [6]. In light of this, minimizing the power dissipation of flip-flops has a major effect on system level power efficacy, particularly for IoT applications with constrained energy resources [7]. For IoT Integrated Circuits (IC) to maximize battery life, power consumption must be kept to a minimum. However, a significant percentage of power, specifically the dynamic power dissipation, in a synchronous system is used by flip-flops, which can change its state at every clock pulse. Due to this, numerous research projects have been carried out in an effort to create flip-flops that use less energy and are more efficient.

The overall system architecture greatly benefits from the chip area and power consumption that FFs provide. In order to satisfy varied application requirements, many FF designs have been presented [8]–[12]. One of them is the sense amplifier-based FF architecture, which comprises of a latch and a dynamic logic sense amplifier [13]. It is thought to be a superior design choice to meet both low power and high speed requirements because it has a shorter set-up time and greater power output than standard FF. But there are two real-world issues with this FF architecture. First, switching power reduction becomes less effective at reduced or no data activity and power dissipation may be more at sense amplifier's pre-charge processes. Second, a longer clock-to-output delay results from the NAND latching stage receiving the data from the sense amplifier stage. Additionally, it has been shown that complementary FF outputs are not always required in applications.

A sense amplifier based flip flop suited for the low power domain is proposed in this study. The structure of the paper is as follows: The prior-art SAFFs are examined in Section 2, along with their advantages and disadvantages. The proposed SAFF, which is intended for reliable and low power operations, is presented in Section 3. The simulation findings and evaluations with existing SAFFs are presented in Section 4. Finally in section 5 the proposed SAFF is experimented in an actual digital circuit along with power measurements to verify its worthiness.

2 Related work

A basic sense amplifier based flip-flop consists of two stages: a sensing stage and a latching stage. The sensing stage uses a fast differential sense amplifier having two outputs (SB and RB), which is followed by a slave latch. The principle of operation of this flip-flop may be described as follows:
The precharge state: When the clock is low, both the sensing stage's outputs, SB and RB are high. The latch stage retains the prior value.
The evaluation state: When clock is high, one of the outputs of sensing stage is low. If the input is high, the sensing stage's SB output terminal will be low, and if the input is low, the sensing stage's RB output terminal will be low. At this point, the state of SB and RB determines how the output of the latch stage is driven. On the rising edges of the clock, for instance, if SB is low, the output is driven to a high state logic, and if RB is low, the output is driven to a low state logic.

Fig. 1 shows the prior-art SAFF, known as CBSAFF, proposed by [14]. The sensing stage in this FF uses a capacitive boosting approach. The capacitive boosters which are actually MOS transistors that are being used as capacitors amplify the data signal and provide a big enough voltage swing to trigger the latch stage from −β.VDD to β.2VDD. Here, the value of "β" (the boosting efficiency) is <1 due to parasitic capacitances. The buffer turns on the pre-charge transistor to charge the

boost capacitor to provide voltage when the clock input is '0'. This buffer is utilized to help boost the voltage to twice the value when the clock input becomes '1' and to stop the clock signal from being loaded with capacitor.

In Fig. 2, Strollo's SAFF [15] is schematically depicted. The output stage can be thought of as a combination of the N-C MOS circuit and the typical NAND based SR latch. The high-to-low output transition is accelerated using the additional transistors. In this design, removing the speed up network and condensing the sizes of few transistors significantly minimize power dissipation. As a result, the capacitive load is reduced, which permits a reduction in the size of the driving transistors at the sensing stage. In order to improve latency and power dissipation during the "1" to "0" transition a PMOS is added to the output stage, this further reduces the current (crow-bar).

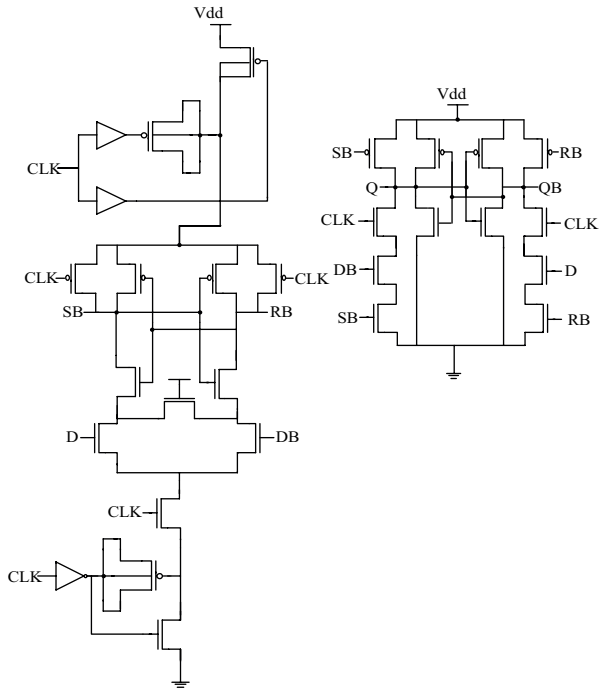


Figure 1: Architecture of CBSAFF [14]

A SAFF based on a transition complete (TC) signal was introduced by Jeong in [16] in order to address the issues with earlier SAFFs at low voltages. This SAFF-structure is depicted in Fig. 3. The sensing stage's outputs are the two inputs of a NAND gate, which produces the TC signal. Only after SET output of sensing stage is charged up, the signal TC discharges. As a result, at the clocks falling edge, both TC and SET signal are briefly high, which could result in an output glitch. However, compared to the SAFF-related issue, this hiccup is minor and far smaller. This kind of FF prevents the current

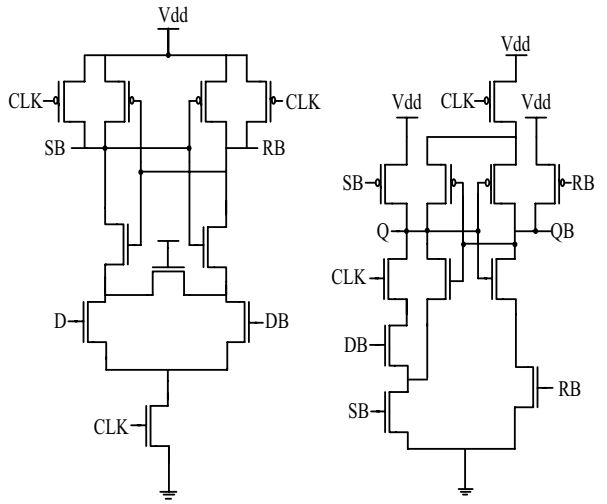


Figure 2: Architecture of Strollo's FF [15]

conflict between latching pMOS transistors and output or compliment output pull-down pathways.

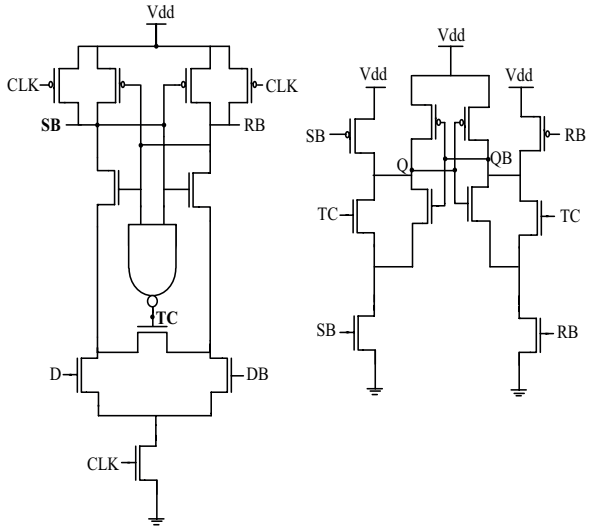


Figure 3: Architecture of Jeong's FF [16]

Another example of SAFF is the Nikolic's SAFF [17] depicted in Fig. 4. The sense amplifier is the same as that in Fig. 2. Latching stage allows for small keeper transistors because only one transistor is active in each branch when the state is changed. The slave latch has symmetric true and complementary trees, which causes the delays at both outputs to be the same. The small size of the keeper transistors causes them to quickly turn off during the transition. This enables the load to be driven and the latch's status to be changed by exterior driver transistors. This characteristic makes the procedure of output transistor size optimization simple. The resistance of the output stage to crosstalk when there is a low clock pulse is the only restriction on minimizing the keeper transistors. It enables reduced clock-swing operation as well as logic integration inside the

flip-flop. Additionally, just one transistor being active during the changeover improves the output stage's capacity to drive other transistors and prevents crowbar current, which lowers power consumption.

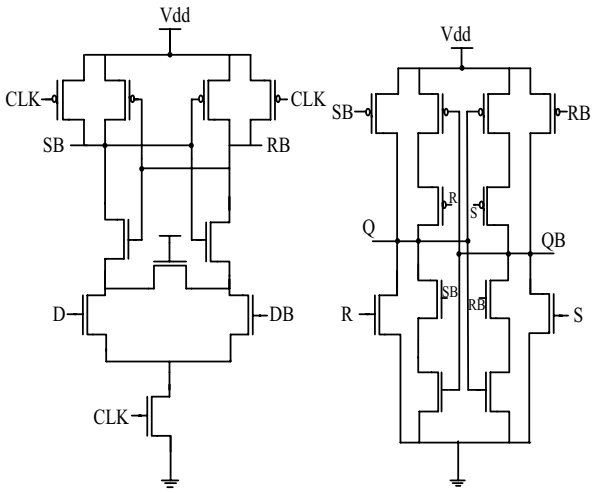


Figure 4: Architecture of Nikolic's FF [17]

Kim proposed a SAFF in [18] with updated N-C2MOS latches shown in Fig. 5. The sense amplifier is the same as it was in the conventional SAFF. Since the coupled inverters are constructed using transistors of the smallest possible size, the additional capacitive loadings they cause at the output nodes are insignificant (less than 10% of the total capacitance value). The differential output nodes are completely separated, therefore the load capacitance at the other output node does not affect the transition speed of one output node.

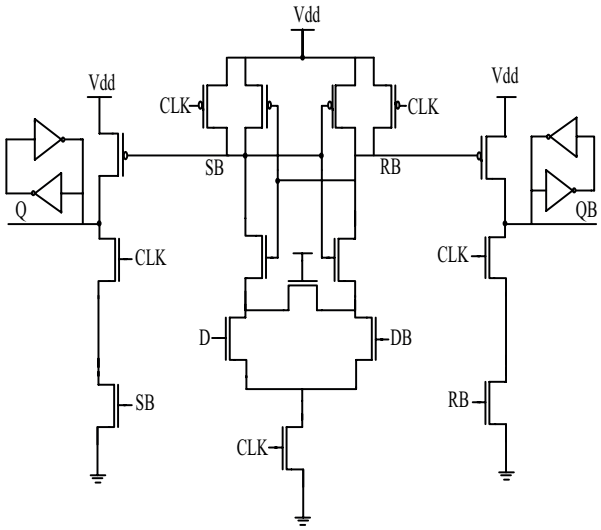


Figure 5: Architecture of Kim's FF [18]

3 Proposed SAFF

Fig. 6 shows the architecture of proposed SAFF. An input/output structure with a novel sense amplifier design and a single-ended pass transistor logic-based latch is used. This design optimization technique helps the leading sense-amplifier stage's transistor size requirement be reduced. The resulting design is more efficient than traditional designs in terms of layout and performance. A real single-ended latch is used to overcome the shortcoming of the dynamic latch. This improves the speed and power performances by significantly reducing the loading effect on the sensing amplifier. To create signal S from the output signal SB of the sense amplifier, an additional inverter INV1 is introduced. Signal RB is in the interim removed from the latch design's list of inputs. This results in a genuine single-ended latch circuit as depicted in Fig. 6.

The operation of the FF can be realized as when clock signal is low, both the outputs of sensing stage RB and SB are precharged to logic '1', transistors N1 and N2 are turned ON, X stays low during the '0-1' transition of clock. During this, the latching stage maintains the state of the flip-flop. At the time when clock changes to '1', the sense amplifier stage starts the transition. One of RB or SB will drop if the shift is successful, raising X. Because of the connection between X and the transistor associated with it remains OFF during the sensing stage transition and is only turned ON when the sensing stage transition is over (i.e one of the precharged node is either brought down to low logic via by transistor N1 or N2 whereas the other precharged node continues to be at logic high). Therefore both the operational yield and speed loss of this transistor is not

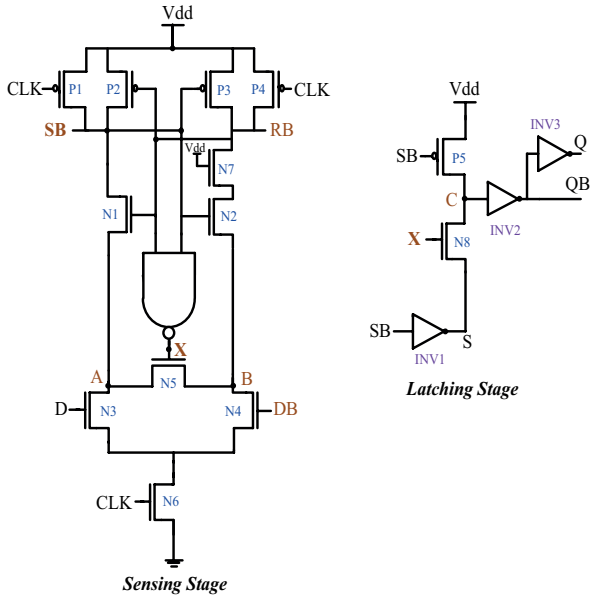


Figure 6: Proposed SAFF

present as compared in the sense amplifiers discussed in previous sections. Remember that as soon as the sensing stage swings, either N1 or N2 will switch off, and as a result, any further change in input will not be able to affect the state of the reset and set terminals. The transistor N7 adds better power efficiency to the FF at the cost of small delay. Nevertheless this small delay is compensated by the latching stage's single-ended structure.

When the clock is low (precharge state), the fact that two nodes A and B are not equalized is another notable aspect of this design. Also at the rising edge of clock, the voltages at the nodes A and B are the same which lessen the effect of mismatch. Conversely, the proposed design has the potential for nodes A and B to diverge at the rising edge of the clock, in turn may reduce the stability of the sensing stage. Nevertheless, the beneficial impact obtained by turning OFF the transistor while high clock outweighs the unfavorable impact of node "A" equal to "B".

For the latch of the proposed design the signal X produced in the sensing stage is applied in place of the global clock. The signal RB is not present in the latching stage since it has a single-ended form. If the input signal data D is low at the rising edges of the clock, SB will remain at operating voltage, and node C will be discharged to low through transistor N8. The transistor P5 will switch ON if the input data D is high, in a similar manner to how node SB will discharge to low if D is high. Now, transistors P5 and N8 together are pulling Node C to operating voltage. The outputs QB and Q are driven by two inverters that are coupled at node C. The operational waveforms in Fig. 7 corroborate and make clear this entire process.

The transistor size of the proposed SAFF is listed in Table 1. The sizes of N3 and N6 are selected to be larger because it controls the performance of the FF since it directly influences the pull down speed of SB. The single-ended structure of the SAFF latch stage allows transistors N2, N4, and N7 to be of minimal size. In addition, since the load on RB is "0" than that on SB, reducing the widths of the transistors N2, N4, and N7 may

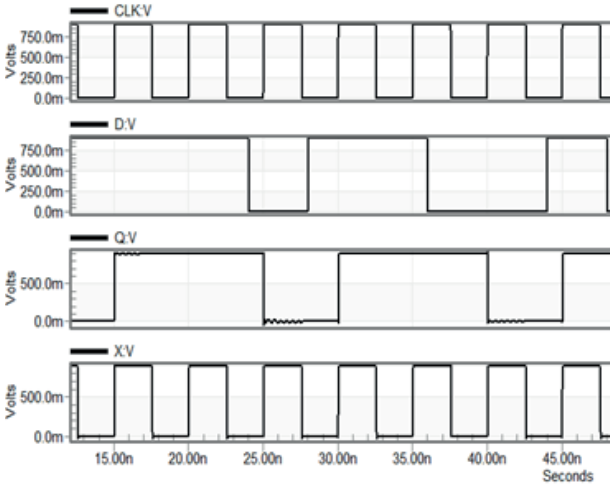


Figure 7: Transient waveform of proposed FF

stabilize the pull down operations on SB. This leads in a shorter hold and setup time for the proposed SAFF. The standard sizes of the transistors are maintained at the latching stage for P5 and N8. Since the inverter's driving capabilities are unnecessary, the size of the invertor transistors can be minimized, resulting in significant power savings.

Table 1: Transistor size of proposed SAFF

Component	W (nm)	Component	W (nm)
P1-P5	320	N6	800
N1, N2, N4, N5, N7 & N8	160	P (Inv1-Inv3)	320
N3	320	N (Inv1-Inv3)	160

4 Simulation results & discussions

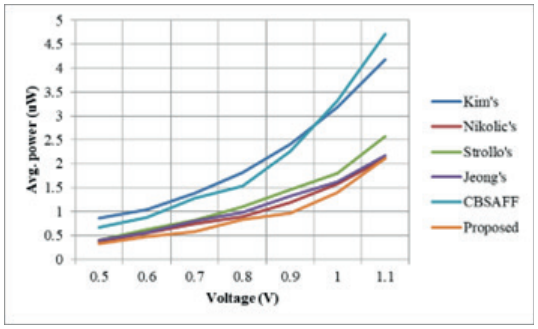
The proposed architecture is tested with available designs to show its competitiveness and performance. The simulations are carried out at 32 nm CMOS technology node in SPICE using PTM models [19]. The nominal working parameters are 25 °C temperature, 200 MHz frequency and 0.9 V operating voltage. A 16-bit input data is used with data activity of 50%.

Table 2: Performance comparison of flip-flops.

Flip Flop	Layout area (um^2)	No. of Transitors	PDP @0.7 V (uW)	PDP @0.8 V (uW)	PDP @0.9 V (uW)	C-Q delay @0.9 V (ps)
Kim's	0.352	26	62.971	66.685	72.239	30.065
Nikolic's	0.262	28	34.061	26.155	31.431	26.408
Strollo's	0.279	23	26.673	24.898	24.693	16.948
Jeong's	0.247	26	33.916	27.874	17.84	13.424
CBSAFF	0.316	38	159.698	70.594	127.457	56.22
Proposed	0.209	25	23.325	21.134	18.666	19.266

The simulation results for power consumption at supply voltage variation between 0.5 V to 1.1 V and at variations in temperature from 0 °C to 100 °C are shown in Fig. 8. This figure makes it very clear that, for all the variations considered in this paper, the proposed design consumes the least amount of power at various voltage levels and temperature changes.

(a)



(b)

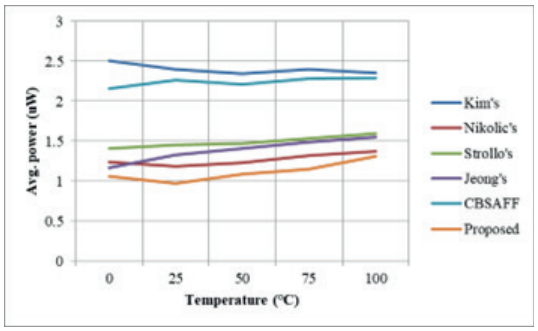
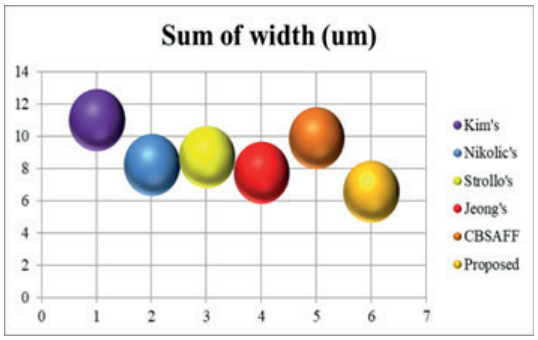


Figure 8: Average power at variations in (a) Voltage (b) Temperature

(a)



(b)

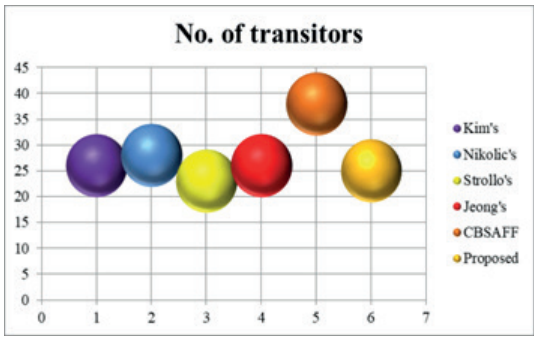


Figure 9: Area requirements (a) Sum of width (b) Number of transistors

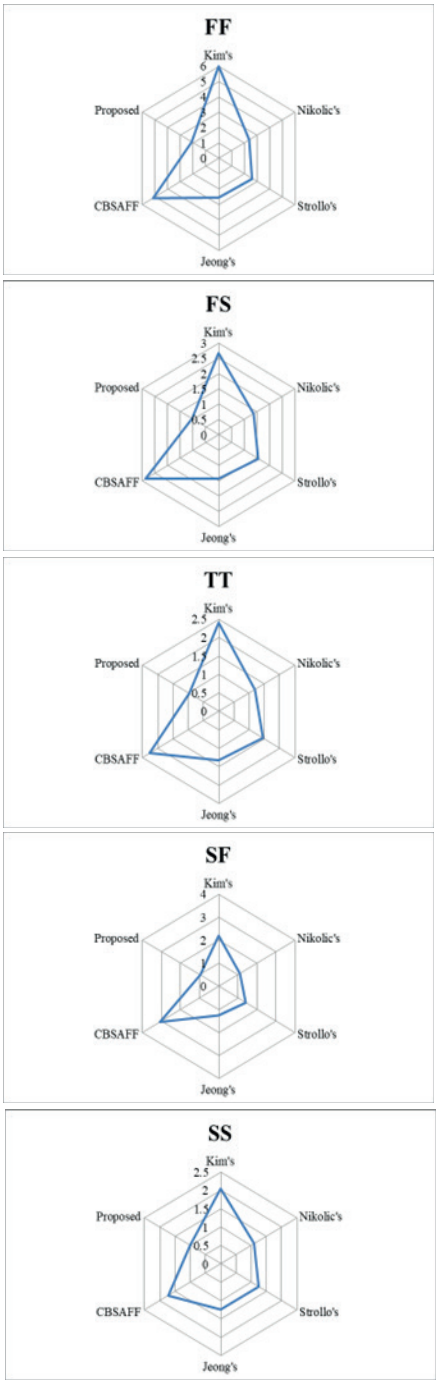
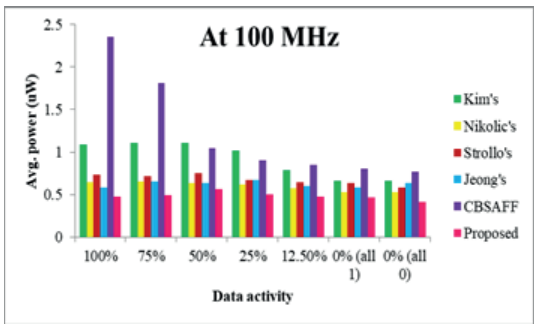


Figure 10: Corner case analysis

Table 2 is the detailed comparison of proposed sense amplifier based flip flop with existing FFs. It includes the layout area, the clock to Q delay and the power delay product at variations in supply voltage. It was observed that at nominal operating conditions, Jeong's FF was the fastest followed by Strollo's FF. The proposed flip flop was third fastest but nearly comparable to its rivals. When power and delay both were taken into account, the proposed flip flop showed better results. The PDP at three different voltage variations of 0.7 V, 0.8 V

(a)



(b)

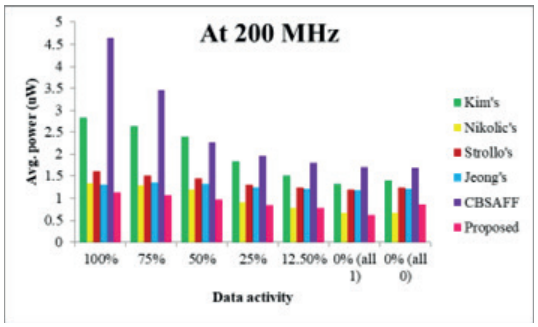


Figure 11: Average power at variation in data activity (a) at 100 MHz (b) at 200 MHz.

and 0.9 V showcases the worthiness of proposed design for portable power efficient devices.

Although in terms of number of transistors the proposed design has second least count but the overall layout area of the proposed design is smaller compared to any other design. This difference and area advantage of proposed design can be seen in Fig. 9.

In any VLSI design, it is important to know the effect of process, voltage and temperature variations at extreme corners. This test was conducted with corner cases of FS 0.9 V /25 °C, SF 0.9 V /25 °C, TT 0.9 V /25 °C, SS 0.8 V /125 °C and FF 1.1 V /-40 °C. The power results of proposed design at all extreme corners were far better than its counterparts. These corner results are shown in Fig. 10.

Fig. 11 is the power results at variations in data activity. Wide variation in input data from 0% to 100% was taken into account. For 0% both all input high and all input low were obtained. This test was conducted at two different frequencies i.e. at 100 MHz and 200 MHz.

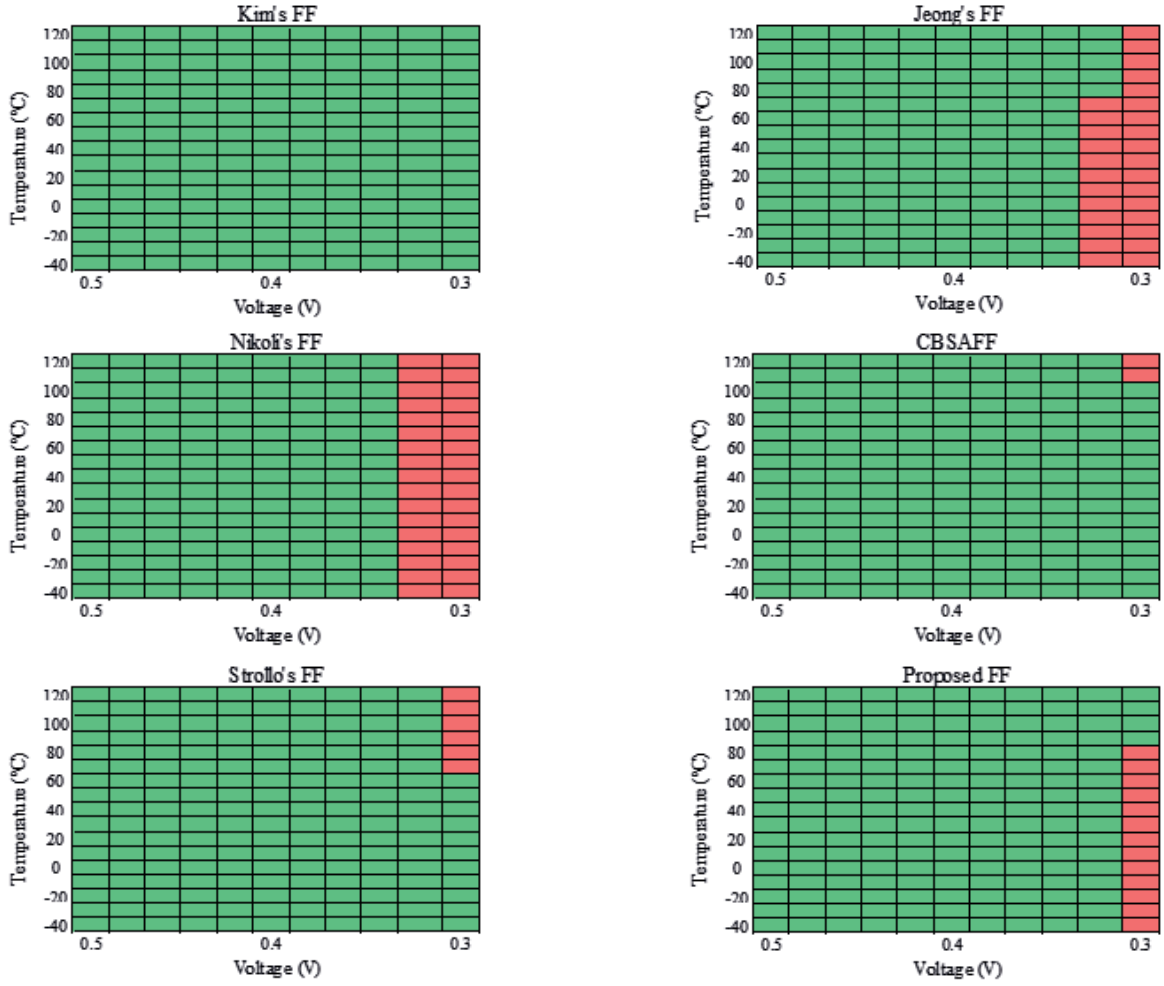


Figure 12: Results of aggressive temperature and voltage scaling (Green: Pass-case; Red: Fail-case)

Results in Fig. 11(a) and 11(b) showcases the proposed design's superiority over other designs at all trails.

Simulations so far have shown that the proposed design is resilient, however, additional testing is conducted against changes in voltages for the near-threshold to sub-threshold range along with the effects of a wide range of temperatures. To test this, Monte Carlo simulations are conducted with aggressive voltage scaling across the range of 0.3 V to 0.5 V with 0.02 V increments (20 mV) and over the range of temperature with 10 °C steps from -40 °C to 120 °C. The results of the tests performed on all of the flip-flops are shown in Figure 12. A 'pass' case test is represented by a green box, while a 'fail' case test is represented by a red box. Kim's FF was the only one to pass all of the tests, followed by CBSAFF with 2 fail instances and Strollo's FF with 6 fail cases. Notably, neither Kim's FF nor the CBSAFF performed well throughout the analysis. In addition, the proposed SAFF has also restricted functioning when subjected to sub-threshold voltage levels and temperature ranges and is therefore recommended for use at voltage levels of more than 0.34 V.

(a)

(b)

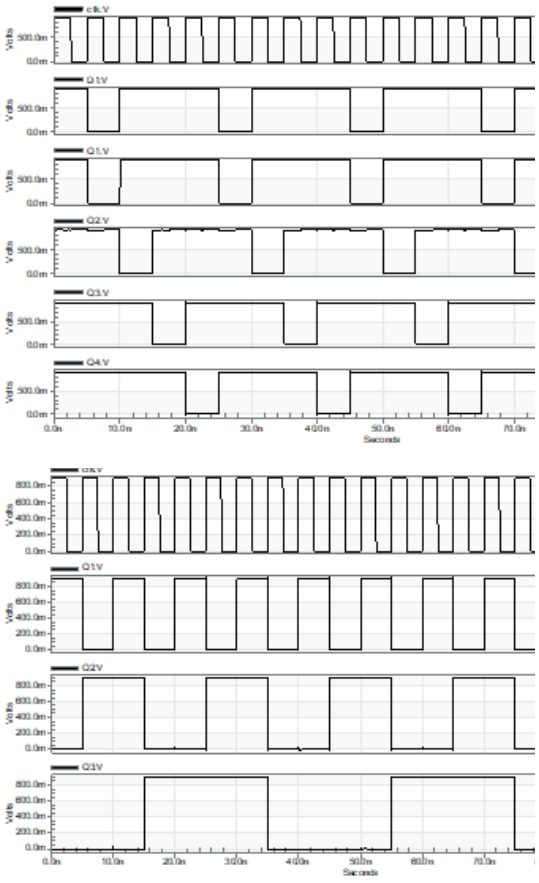


Figure 13: Transient waveform of proposed FUT as (a) 4-bit shift register (b) 3-bit counter

5 Experimental verification

In order to illustrate and validate the correct logical operation and power performance of the proposed design, the proposed SAFF is tested for use in complex digital circuitries. The flip-flop under test (FUT) was evaluated as a four-bit shift register and a three-bit counter in simulation settings under the nominal conditions of 25 °C temperature, 0.9 V supply voltage, and 200 MHz frequency. Figure 13 are the transient waveforms of these tests thereby demonstrating the correct circuit functionality of the proposed design.

The test was also conducted on existing FFs to determine and compare the power performance of all the designs. The average power was determined at voltages of 0.8 V, 0.9 V and 1 V and at variations in temperature of -40 °C, 25 °C and 125 °C. Figure 14 and 15 shows the results obtained from these tests, the proposed FUT demonstrated better power performance at all conducted tests and therefore is worthy of consideration in designs requiring low power operations.

(a)

(b)

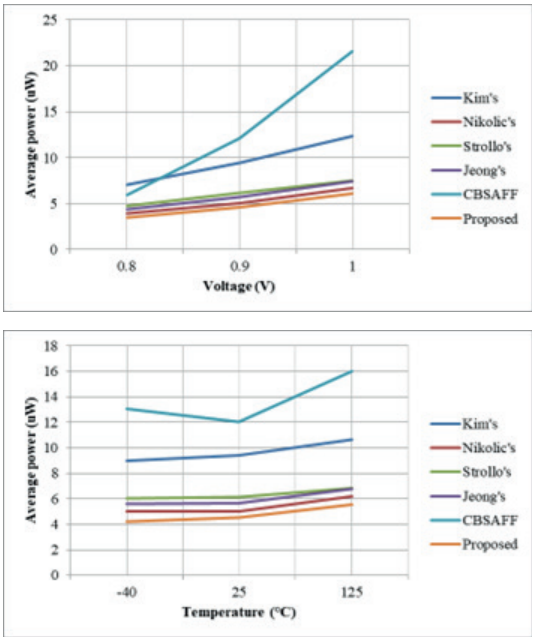
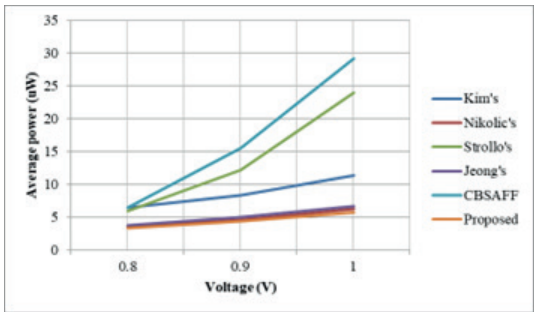


Figure 14: Power results of shift register at variation in (a) voltage (b) temperature

6 Conclusion

A modified sensing stage is used to create a sense amplifier based flip flop. The major goal was to reduce power consumption so that the proposed flip flop will be a viable option for digital circuits and IoT applications. After comprehensive simulations, the proposed design excelled practically all other designs in metrics

(a)



(b)

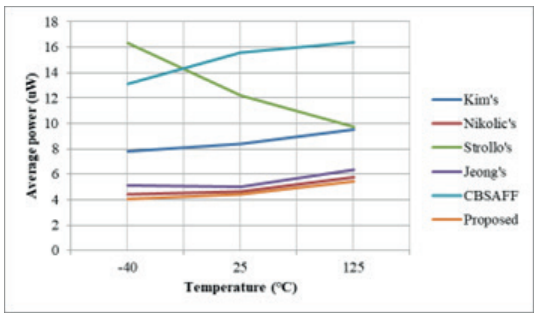


Figure 15: Power results of counter at variation in (a) voltage (b) temperature

like as average power, PDP, data activity, and in especially layout area. The proposed design also upheld the voltage variation of 0.5 V to 1.1 V and corner case temperature variation of -40 °C to 120 °C. Further advantage of the novel design includes the power efficiency at input data activity variation. In addition, the proposed FF is recommended for designs with minimum voltage of 0.34 V.

7 Conflict of interest

The authors declare no conflict of interest.

8 References

1. M. A. S. Bhuiyan, "CMOS series-shunt single-pole double-throw transmit/receive switch and low noise amplifier design for internet of things based radio frequency identification devices," Informacije MIDEM, vol. 50, no. 2, pp. 105–114, Sep. 2020, https://doi.org/10.33180/InfMIDEM2020.203.
2. M. Arunraja, V. Malathi, and E. Sakthivel, "Distributed Energy Efficient Clustering Algorithm for Wireless Sensor Networks," Informacije MIDEM, vol. 45, no. 3, pp. 180–187, 2015..
3. S. Raj and S. S. Ramapackiam, "Energy Efficient and Low dynamic power Consumption TCAM on FPGA," Informacije MIDEM, vol. 51, no. 3, Nov. 2022, https://doi.org/10.33180/InfMIDEM2022.304.
4. O. A. Shah, I. Ahmed Khan, G. Nijhawan, and I. Garg, "Low Transistor Count Storage Elements and their Performance Comparison," in 2018 International Conference on Advances in Computing, Communication Control and Networking (ICACCCN), Greater Noida (UP), India, Oct. 2018, pp. 801–805. https://doi.org/10.1109/ICACCCN.2018.8748364.
5. H. You, J. Yuan, W. Tang, Z. Yu, and S. Qiao, "A Low-Power High-Speed Sense-Amplifier-Based Flip-Flop in 55 nm MTCMOS," Electronics, vol. 9, no. 5, p. 802, May 2020, https://doi.org/10.3390/electronics9050802.
6. I. A. Khan, O. A. Shah, and M. T. Beg, "Analysis of different techniques for low power Single Edge Triggered Flip Flops," in 2011 World Congress on Information and Communication Technologies, Mumbai, India, Dec. 2011, pp. 1363–1367. https://doi.org/10.1109/WICT.2011.6141447.
7. Y. Lee, G. Shin, and Y. Lee, "A Fully Static True-Single-Phase-Clocked Dual-Edge-Triggered Flip-Flop for Near-Threshold Voltage Operation in IoT Applications," IEEE Access, vol. 8, pp. 40232–40245, 2020, https://doi.org/10.1109/ACCESS.2020.2976773.
8. D. Pan, C. Ma, L. Cheng, and H. Min, "A Highly Efficient Conditional Feedthrough Pulsed Flip-Flop for High-Speed Applications," IEEE Trans. VLSI Syst., vol. 28, no. 1, pp. 243–251, Jan. 2020, https://doi.org/10.1109/TVLSI.2019.2934899.
9. A. Karimi, A. Rezai, and M. M. Hajhashemkhani, "A novel design for ultra-low power pulse-triggered D-Flip-Flop with optimized leakage power," Integration, vol. 60, pp. 160–166, Jan. 2018, https://doi.org/10.1016/j.vlsi.2017.09.002.
10. O. A. Shah, G. Nijhawan, and I. A. Khan, "Low power area efficient self-gated flip flop: Design, implementation and analysis in emerging devices," Engineering and Applied Science Research, vol. 49, no. 6, pp. 744-752, 2022, https://doi.org/10.14456/EASR.2022.72.
11. J. Lin, Y. Hwang, C. Wong, and M. Sheu, "Single-ended structure sense-amplifier-based flip-flop for low-power systems," Electron. lett., vol. 51, no. 1, pp. 20–21, Jan. 2015, https://doi.org/10.1049/el.2014.3922.
12. S. Lapshev and S. M. R. Hasan, "New Low Glitch and Low Power DET Flip-Flops Using Multiple C-Elements," IEEE Trans. Circuits Syst. I, vol. 63, no. 10, pp. 1673–1681, Oct. 2016, https://doi.org/10.1109/TCSI.2016.2587282.
13. O. A. Shah, G. Nijhawan, and I. A. Khan, "Improved Sense Amplifier Based Flip Flop Design For Low Power And High Data Activity Circuits," Journal of Applied Science and Engineering, vol. 26, no. 7, pp. 1047–1053, Oct. 2022, https://doi.org/10.6180/jase.202307_26(7).0015.

14. A. Ramaswami Palaniappan and L. Siek, "Wide-input dynamic range 1 MHz clock ultra-low supply flip-flop," Electron. lett., vol. 54, no. 15, pp. 938–939, Jul. 2018, https://doi.org/10.1049/el.2018.1134.
15. A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high-speed sense-amplifier-based flip-flop," IEEE Trans. VLSI Syst., vol. 13, no. 11, pp. 1266–1274, Nov. 2005, https://doi.org/10.1109/TVLSI.2005.859586.
16. H. Jeong, T. W. Oh, S. C. Song, and S.-O. Jung, "Sense-Amplifier-Based Flip-Flop With Transition Completion Detection for Low-Voltage Operation," IEEE Trans. VLSI Syst., vol. 26, no. 4, pp. 609–620, Apr. 2018, https://doi.org/10.1109/TVLSI.2017.2777788.
17. B. Nikolic, V. G. Oklobdzija, V. Stojanovic, Wenyan Jia, James Kar-Shing Chiu, and M. Ming-Tak Leung, "Improved sense-amplifier-based flip-flop: design and measurements," IEEE J. Solid-State Circuits, vol. 35, no. 6, pp. 876–884, Jun. 2000, https://doi.org/10.1109/4.845191.
18. J.-C. Kim, Y.-C. Jang, and H.-J. Park, "CMOS sense amplifier-based flip-flop with two N-C2MOS output latches," Electron. Lett., vol. 36, no. 6, p. 498, 2000, https://doi.org/10.1049/el:20000409.
19. "Predictive Technology Model," PTM. https://ptm.asu.edu (accessed Oct. 10, 2022).

Arrived: 29. 01. 2023
Accepted: 20. 04. 2023

Original scientific paper
https://doi.org/10.33180/InfMIDEM2023.105

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
Vol. 53, No. 1(2023), 49 – 53

The Design of Frequency-tunable Mechanical Tuning Coupler Based on Coupled Line Structure

Jiayi Wang[1,2], Yuepeng Yan[1,3]

[1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
[2]University of Chinese Academy of Sciences, Beijing, Beijing, China
[3]Beijing Key Lab of New Generation Communication RF Chip Technology, Beijing, China

Abstract: In the current study, a frequency-tunable mechanical tuning coupler based on coupled line structure is proposed, which shall have high stability and high flexibility of tuning. This mechanical tuning coupler is based on coupled line structure of microstrip technology. This coupler is composed by baseplate for signal transmission and mobile plate for mechanical tuning. By mechanically tuning the rotation angle, the coupling length is changed and tunability is achieved. The operating frequency can be tuned from 1.02 GHz to 1.27 GHz while the rotation angle is tuned from 180° to 135° approximately. The design principle is based on quarter-wave resonance phenomenon of coupled line.

Keywords: frequency-tunable, coupled line, mechanical tuning, microstrip

Načrtovanje mehanskega spojnika z možnostjo nastavitve frekvence na podlagi strukture sklopljene linije

Izvleček: V pričujoči študiji je predlagan frekvenčno nastavljiv mehanski sklopnik, ki temelji na strukturi sklopljene linije in ima visoko stabilnost in prilagodljivost uglaševanja. Ta mehanski nastavljiv sklopnik temelji na strukturi sklopljene linije mikropasovne tehnologije. Sestavljata ga osnovna plošča za prenos signala in premična plošča za mehansko nastavljanje. Z mehanskim nastavljanjem kota vrtenja se spreminja dolžina sklopke in doseže nastavljivost. Delovno frekvenco je mogoče nastaviti od 1,02 GHz do 1,27 GHz, kot vrtenja pa približno od 180° do 135°. Načelo zasnove temelji na resonančnem pojavu četrtvalovne resonance sklopljene linije.

Ključne besede: frekvenčno uglaševanje, sklopljena linija, mehansko uglaševanje, mikropasec

** Corresponding Author's e-mail: safe_iluosi@163.com*

1 Introduction

Coupler, known as an important communication electronics, plays an essential role in optical and microwave system [1-4]. Couplers are usually used for power distribution, phase shift and so on [5]. Among them, tunable couplers can realize further functionality for its tunability of coupling coefficients or frequency. Most tunable couplers realize tunablility by using reconfigurable components, such as tunable capacitors or Micro Electro Mechanical Systems (MEMS) switches [6-10]. Besides, some couplers also use magnetic material to realize tunablility [11].

Coupled line is a popular structure in microstrip industry. When two waveguides get close to each other, the function of power redistribution can be realized. This structure is popular in the application of couplers [12-13]. The principle of coupled line coupler is based on quarter-wave resonance phenomenon. Their operating frequencies depend on coupling length mostly.

How to cite:
J. Wang et al., "The Design of Frequency-tunable Mechanical Tuning Coupler Based on Coupled Line Structure", Inf. Midem-J. Microelectron. Electron. Compon. Mater., Vol. 53, No. 1(2023), pp. 49–53

In this study, a frequency-tunable mechanical tuning coupler based on coupled line structure is proposed. This tunable coupler uses two-layer structure. Using two-layer structure can realize much functions like refining smoothness and reducing size [14]. In current study, the tunability of component is achieved by using this two-layer structure.

Mechanical tuning is a popular tuning way in the design of tuning resonators and filters [15-17]. Tuning screw structure is a popular structure in mechanical tuning. This coupler is made by printed circuit board (PCB) technology, which should have high stability and low manufacturing cost. This mechanical tuning coupler can be driven by a stepper micromotor [18]. By changing rotation angle of mobile plate, the coupling length of coupler can be changed leading to the shifting of operating frequency. The coupling lines is deformed into semicircle-ring type. It still obeys the law of quarter-wave resonance phenomenon, but some differences exist.

2 The simulation of miniature tunable inductor

The principle diagram of this frequency-tunable mechanical tuning coupler can be given by Fig. 1.

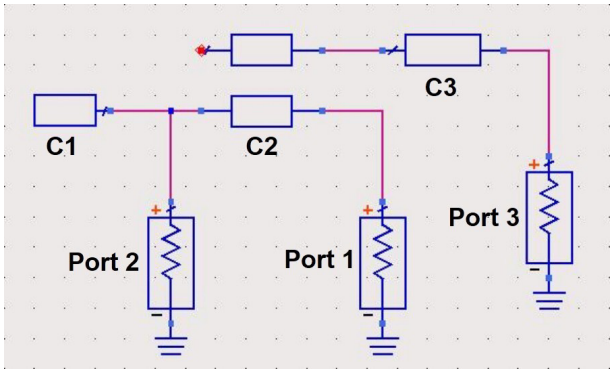


Figure 1: principle diagram of frequency-tunable mechanical tuning coupler

C1 means the length of microstrip which does not participate in coupling in signal transmission end. C2 means the length of coupling part. C3 means the length of microstrip which does not participate in coupling in coupling end. The coupling length C2 decides the operating frequency. By mechanically tuning the length of C2, tunability of frequency can be realized. According to the simulation of Advance Design System (ADS), the ratio of C2/C1 and C2/C3 is better to be larger than 300%, or the reflection coefficients S11 and transmission coefficient S21 will deteriorate gradually.

Fig. 2 shows the perspective model of frequency-tunable mechanical tuning coupler with a rotation angle at 135°.

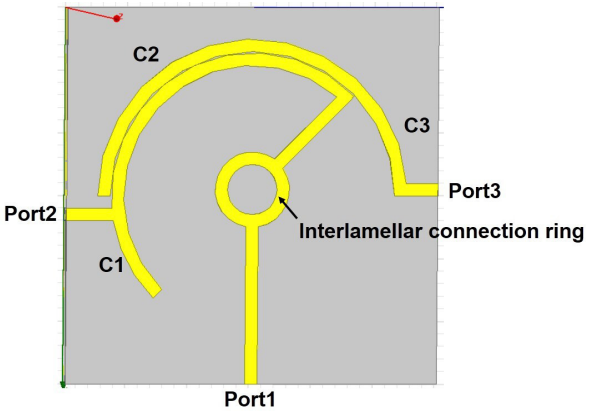


Figure 2: perspective model of frequency-tunable mechanical tuning coupler

The coupler includes baseplate for signal transmission and mobile plate for mechanical tuning. The inner metal ring is printed on mobile plate. By rotating the mobile plate, the coupling length C2 is changed leading to the tunability of frequency. The coupling signal is conducted to Port 3 by the coupled lines. The end of inner metal ring is open circuit. C1 will lead to the deterioration of reflection coefficient S11, so the ratio of C2/C1 shall be controlled. The mathematic relation of operating frequency can be written as Eq. 1 [19]

$$f_0 = \frac{c}{4\alpha L \varepsilon_r^{0.5}} \tag{1}$$

where f_0 is operating frequency, c is light speed, α is shape correction factor, L is arc length of coupled lines, ε_r is relative permittivity of dielectric material.

The structure of frequency-tunable mechanical tuning coupler is shown as Fig. 1. The substrate material is FR4 with a relative permittivity ε_r about 4.2-4.7 with a height h of 1 mm. The metal line is made by gold with a height of 35 μm. The total size of the coupler is 40 mm×30 mm. Fig. 3 is the structure of frequency-tunable mechanical tuning coupler.

The parameter r1, r2, s and w in Fig. 3 mean external radium of inner ring, external radium of outer ring, interval between coupled lines and width of metal line which equal to 11.45 mm, 12.5 mm, 0.05 mm, 1 mm respectively. The mobile plate is connected to a stepper micromotor, which drive the mobile plate rotating from the bottom. The micromotor has a small volumn of Φ3.4 mm ×10.75 mm, which can ensure the compactness of this component. Besides, stepper motor

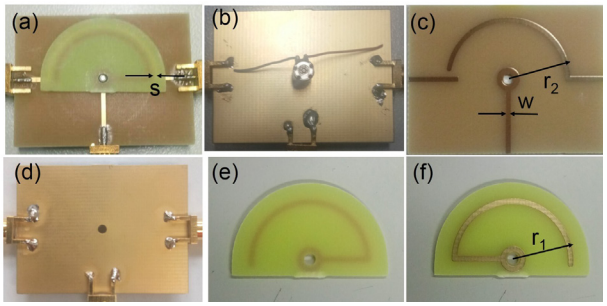


Figure 3: (a) top view of frequency-tunable mechanical tuning coupler (b) bottom view of frequency-tunable mechanical tuning coupler (c) top view of baseplate (d) bottom view of baseplate (e) top view of mobile plate (f) bottom view of mobile plate

means a motor driven by electric pulse signal. Each electric pulse signal will make the motor rotate for a certain degree, ensuring the controllability and stability of tuning. The operating frequency is determined by its rotation angle. The simulation and measurement result is shown in Fig. 4.

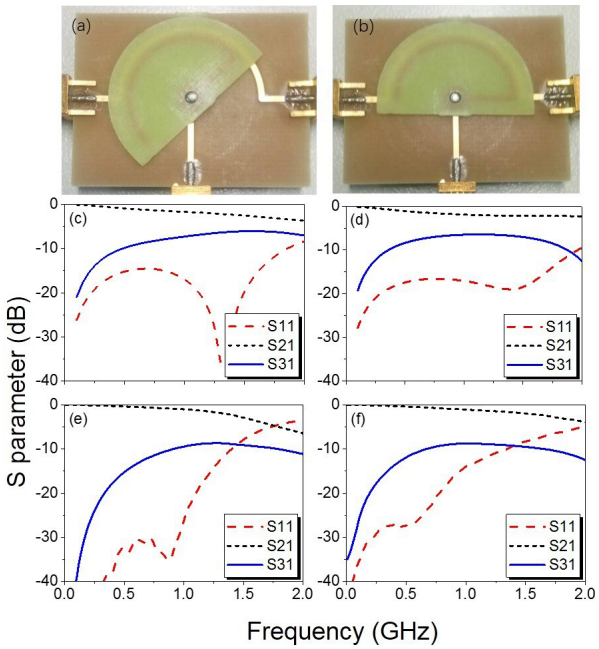


Figure 4: (a) (b) tunable coupler with a rotation angle about 135° and 180° (c) (d) simulation and (e) (f) measurement result of tunable coupler with a rotation angle about 135° and 180°

S31 in measurement is weaker than that in simulation for a distance. The metal line is set as perfect conductor in simulation, while real gold line has a weaker conductivity than perfect conductor. It causes some difference between simulation and measurement. The height of metal lines can be improved to reduce this difference. The tightness between two plates is another important factor.

The 1 dB-passband of Fig. 4(e) is from 0.97 GHz to 1.69 GHz with a coupling coefficient S31 around -8.66 dB at a center frequency of 1.27 GHz. While the 1 dB-passband of Fig. 4(f) is from 0.71 GHz to 1.58 GHz with a coupling coefficient S31 around -8.75 dB at a center frequency of 1.02 GHz. The transmission coefficient S21 of 135° deteriorates a bit than that of 180° in passband, but it is still in reasonable range.

3 Result and discussion

This coupler is based on quarter-wave resonance phenomenon, so the tuning range appears inapparently for the limited change of coupling length in lower frequency. In theory, the tuning range is 24.5% with the rotation angle tuned from 180° to 135°. So the tuning range can be more apparent in higher operating frequency. Table 1 shows the comparison with other works.

Table 1: Comparison of measurement result.

	Tuning range (GHz)	Coupling (dB)	NNC
This work	1.02-1.27 (24.5%)	-8.66	1
[5]	1.6-2.3 (36%)	-3~-4	4
[6]	6.7-7.1 (5.7%)	3~-6	4
[7]	1.3-1.9 (46%)	-3~-10	4

NNC means number of necessary tuning components.

As a passive component, the properties of current coupler is based on the structure of coupled line itself. Compared with active tunable couplers, current couplers cannot realize the tunability of S31 or signal amplification. However, the tuning of former works need to adjust their four tuning components (variable capacitors or RF switches) into respective certain value. While the tuning of this work relies on one micromotor, which has more flexibility of tuning.

The coupled lines of this coupler is semicircle-ring type, whose properties are similar to common linear coupled line coupler. So when this coupler is designed, classical equations of common linear coupled line coupler can be used as reference to choose parameters as shown in Eq. 2 and Eq. 3 [19]

$$Z_0^2 = \alpha_e Z_{0e} \alpha_o Z_{0o} \tag{2}$$

$$K = \frac{\alpha_e Z_{0e} - \alpha_o Z_{0o}}{\alpha_e Z_{0e} + \alpha_o Z_{0o}} \tag{3}$$

where Z0 is characteristic impedance of microstrip, αe is shape correction factor of even mode, αo is shape

correction factor of odd mode, Z0e is even mode characteristic impedance and Z0o is odd mode characteristic impedance. The width of microstrip w determines Z0 mostly, the relation is shown as Eq. 4 approximately. w shall be calculated to make impedance matched [19].

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \log\left(\frac{8h}{w} + \frac{w}{4h}\right) \quad (4)$$

Besides, the interval between coupled lines s determine coupling degree K and S31. In general, a larger interval between coupled lines s gets a smaller S31. S31 goes from -8.6 dB to -12.4 dB when s goes from 0.05mm to 0.5mm in measurement of this study. Therefore, s shall be chosen according to desired S31. The height of metal lines can be improved to intensity the coupling degree *K* in some degree as well. The tunability of S31 can be realized if the tuning of *s* is achieved.

Some differences caused by shape difference can be adjusted by simulation software subsequently.

Port 1 and Port 2 are connected by the mobile plate. If the metal lines do not contact tightly, the signal will not transmit normally. The height of metal line can be thicked for strengthening tightness. Besides, the equivalent impedance of interlamellar connection ring shall be well designed and impedance matched in case of return loss. The interlamellar connection ring is better to be a small circle whose diameter is similar to the width of metal line. Besides, the ratio of C2/C1 and C2/C3 will influence the reflection coefficient S11, especially C2/C1. Namely, the C2 cannot be close to C1. If this ratio is too small, reflection coefficient S11 will improve largely and deteriorates transmission coefficient S21. So the rotation angle shall be controlled in reasonable range.

4 Conclusions

In this study, a frequency-tunable mechanical tuning coupler is proposed. By changing rotation angle of mobile plate, the coupling length of coupled line is changed leading to tunability of operating frequency. The operating frequency of this coupler can be tuned from 1.27 GHz to 1.02 GHz while the rotation angle is tuned from 180° to 135°, the tuning range is 24.5%.

5 Conflict of Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

The funding sponsor of this work is Institute of Microelectronics of the Chinese Academy of Sciences.

6 References

1. A.M. Abbosh. A Compact UWB Three-Way Power Divider[J]. IEEE Microwave and Wireless Components Letters, 2007, 17 (8): pp.598-600. https://doi.org/10.1109/LMWC.2007.901777)
2. H. L. Ting, S. K. Hsu, T. L. Wu et al. A Novel and Compact Eight-Port Forward-Wave Directional Coupler With Arbitrary Coupling Level Design Using Four-Mode Control Technology[J]. IEEE Transactions on Microwave Theory & Techniques, 2016, 1 (1): pp.1-9. https://doi.org/10.1109/TMTT.2016. 2623709)
3. C. Caloz, A. Sanada, T. Itoh et al. A Novel Composite Right-/Left-Handed Coupled-Line Directional Coupler with Arbitrary Coupling Level and Broad Bandwidth[J]. IEEE Transactions on Microwave Theory & Techniques, 2004, 52 (3): pp.980-992. https://doi.org/10.1109/TMTT.2004.823579)
4. M. Kaneta, K. Yashiro, S. Ohkawa et al. A Magnetostatic Forward Volume Wave Directional Coupler with a Guiding Slot Structure[C]. International Microwave Symposium Digest IEEE. 1988. https://doi.org/10.1109/MWSYM.1988.22174)
5. A. Babnik, A. Suhadolnik, J. Mozina, "Single-Mode Optical Fiber Directional Coupler," Informacije MIDEM, vol. 21 (1991), no. 3, pp. 145-150, http://www.midem-drustvo.si/Journal%20papers/MIDEM_21(1991)3p145.pdf
6. O. D. Gurbuz, G. M. Rebeiz. A 1.6–2.3-GHz RF MEMS Reconfigurable Quadrature Coupler and Its Application to a 360 Reflective-Type Phase Shifter[J]. IEEE Transactions on Microwave Theory & Techniques, 2015, 63 (2): pp.414-421. https://doi.org/10.1109/TMTT.2014.2379258)
7. B. Hur, W. R. Eisenstadt. Tunable Broadband MMIC Active Directional Coupler[J]. IEEE Transactions on Microwave Theory & Techniques, 2013, 61 (1): pp.168-176. https://doi.org/10.1109/TMTT.2012.2228218)
8. Y. F. Pan, W. S. Chan, S. Zheng et al. A Highly Reconfigurable Coupler with Tunable Frequency, Phase Difference and Coupling Coefficient Based on Circular Patch[C]. 2020 IEEE Asia-Pacific Microwave Conference. 2020: pp.1033-1035. https://doi.org/10.1109/APMC47863.2020.9331573)
9. S. M. Wang, C. Y. Chang, J. S. Lin et al. A Software Configurable Coupler with Programmable Coupling Coefficient[C]. 2007 IEEE/MTT-S International Microwave Symposium. 2007: pp.185-188. https://doi.org/10.1109/MWSYM.2007.380321)
10. S. Toyoda. Variable Coupling Directional Couplers Using Varactor Diodes[C]. 1982 IEEE MTT-S International

Microwave Symposium Digest. 1982: pp.419-421. https://doi.org/10.1109/MWSYM.1982.1130742)
11. M. Kaneta, K. Yashiro, S. Ohkawa et al. A Magnetostatic Forward Volume Wave Directional Coupler with a Guiding Slot Structure[C]. International Microwave Symposium Digest IEEE. 1988. https://doi.org/10.1109/MWSYM.1988.22174)
12. X. Li, Z. H. Shao, M. K. Shen et al. High Selectivity Tunable Filtering Power Divider Based on Liquid Crystal Technology for Microwave Applications[J]. Journal of Electromagnetic Waves and Applications, 2016, 1 (1): pp.1-10. https://doi.org/10.1080/09205071.2016.1155500)
13. L. Guo, H. Zhu, A. Abbosh et al. Phase Reconfigurable Microwave Power Divider[J]. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 1 (1): pp.1-5. https://doi.org/10.1109/TCSII.2018.2829200)
14. J.Y. Wang, Y. P. Yan et al. Coupled line coupler with smooth passband based on two-layer structure [J]. IEICE Electronics Express, 2022, 19 (17): pp.1-4. https://doi.org/10.1587/elex.19.20220292)
15. F. Mira, J. Mateu, C. Collado et al. Mechanical Tuning of Substrate Integrated Waveguide Resonators[J]. IEEE Microwave and Wireless Components Letters, 2012, 22 (9): pp.447-449. https://doi.org/10.1109/LMWC.2012.2208735)
16. F. Mira, J. Mateu, C. Collado et al. Mechanical Tuning of Substrate Integrated Waveguide Filters[J]. IEEE Transactions on Microwave Theory and Techniques, 2015, 63 (12): pp.3939-3946. https://doi.org/10.1109/TMTT.2015.2490144)
17. S. Kurudere, V. B. Ertürk. Novel Microstrip Fed Mechanically Tunable Combline Cavity Filter[J]. IEEE Microwave and Wireless Components Letters, 2013, 23 (11): pp.578-580. https://doi.org/10.1109/LMWC.2013.2281432)
18. Zhaowei Machinery & Electronics Co., Ltd, 3.4mm stepper motor. Available from: https://www.zw-gearbox.com/stepper-motor/3-4mm-stepper-motor
19. Microstrip circuit compilation Group of Tsinghua University. Microstrip Circuit[M]. Tsinghua University, 2017.

Arrived: 6.2.2023
Accepted: 22.6.2023

Boards of MIDEM *Society* | *Organi društva* MIDEM

MIDEM *Executive Board* | *Izvršilni odbor* MIDEM

President of the MIDEM Society | Predsednik društva MIDEM
Prof. Dr. Barbara Malič, Jožef Stefan Institute, Ljubljana, Slovenia

Vice-presidents | Podpredsednika
Prof. Dr. Janez Krč, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Dr. Iztok Šorli, Mikroiks d.o.o., Ljubljana, Slovenia

Secretary | Tajnik
Olga Zakrajšek, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia

MIDEM Executive Board Members | Člani izvršilnega odbora MIDEM
Prof. Dr. Slavko Bernik, Jožef Stefan Institute, Slovenia
Assoc. Prof. Dr. Miha Čekada, Jožef Stefan Institute, Ljubljana, Slovenia
Prof. DDr. Denis Đonlagić, UM, Faculty of Electrical Engineering and Computer Science, Maribor, Slovenia
Prof. Dr. Leszek J. Golonka, Technical University, Wroclaw, Poljska
Prof. Dr. Vera Gradišnik, Tehnički fakultet Sveučilišta u Rijeci, Rijeka, Croatia
Mag. Leopold Knez, Iskra TELA, d.d., Ljubljana, Slovenia
Mag. Mitja Koprivšek, ETI Elektroelementi, Izlake, Slovenia
Asst. Prof. Dr. Gregor Primc, Jožef Stefan Institute, Ljubljana, Slovenia
Prof. Dr. Janez Trontelj, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Asst. Prof. Dr. Hana Uršič Nemevšek, Jožef Stefan Institute, Ljubljana, Slovenia
Dr. Danilo Vrtačnik, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia

Supervisory Board | Nadzorni odbor

Prof. Dr. Franc Smole, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Prof. Dr. Drago Strle, UL, Faculty of Electrical Engineering, Ljubljana, Slovenia
Igor Pompe, retired

Court of honour | Častno razsodišče

Darko Belavič, Jožef Stefan Institute, Ljubljana, Slovenia
Dr. Miloš Komac, retired
Dr. Hana Uršič Nemevšek, Jožef Stefan Institute, Ljubljana, Slovenia

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
ISSN 0352-9045

Publisher / Založnik:
MIDEM Society / Društvo MIDEM
Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia
Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, Ljubljana, Slovenija

www.midem-drustvo.si