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VERTICAL SILICON-ON-NOTHING FET: SUBTHRESHOLD SLOPE CALCULATION USING COMPACT CAPACITANCE MODEL

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Key words: Silicon-on-Nothing, fully-depleted MOSFET, vertical SONFET, subthreshold slope, compact model

Abstract: The subthreshold slope model of the Vertical Silicon-on-Nothing FET, extracted from the compact capacitance model, has been developed. For short-channel effects modeling the voltage-doping transformation is used. The analytical model is verified by comparison to the two-dimensional numerical device simulator, MEDICI, over a wide range of different device structures. Good agreement is obtained for channel lengths down to 50 nm.

Vertikalni SONFET: modeliranje podpragovne tokovne karakteristike

Kjučne besede: SONFET, vertikalni SONFET, naklon podpragovne tokovne karakteristike, modeliranje

Izvleček: Razvili smo model podpragovne tokovne karakteristike vertikalnega tranzistorja SONFET (Silicon-on-nothing FET). Analitični model smo preverili s primerjavo rezultatov dobljenih z dvodimenzionalno simulacijo s programom MEDICI. Dobili smo dobro ujemanje izračunanih in izmerjenih vrednosti za dolžine kanala navzdol do 50nm.

1 Introduction

The scaling of conventional CMOS is approaching technological limits /1/, and the need for replacement device architecture is growing. A possible alternative is the Silicon-on-Nothing (SON) technology /2/, where the epitaxial process is used for the formation of the sacrificial SiGe layer and top Si layer for the active device part. The sacrificial SiGe region is later removed below transistor channel and replaced by an insulating material, resulting in quasi-SOI structure in the active region. However, the SON MOSFET (SONFET) transistors are processed on bulk Si wafers with reverse biased source and drain junctions to the substrate. This eliminates one of the major advantages of standard SOI technologies, which is the reduction of parasitic capacitances. The SON technology can also be transferred to SOI substrate, but with considerable increase in process complexity.

The Vertical Fully-Depleted SONFET (VFD SONFET) is developed as a further evolution of the lateral SONFET /3, 4, 5/. The channel length of the vertical SONFET is defined by the molecular-beam epitaxy (MBE), allowing the channel-length reduction into the sub-30 nm region without the need for high-resolution lithography. Furthermore, standard bulk region underneath the buried oxide is eliminated (Fig. 1.). The absence of the transistor bulk is a unique property of the VFD SONFET, not present in either bulk or SOI CMOS.

The subthreshold slope value is one of the key issues for deep-submicrometer devices, with the target value of 60 mV/dec at temperature of 300 K. In this paper, we give an analytical solution for the VFD SONFET subthreshold slope based on the compact capacitive model in subthreshold region. The voltage-doping transformation (VDT) is used for short-channel effects modeling and the solutions are verified in comparison to the results of two-dimensional device simulator.

2 Modelling

2.1 Capacitive model in subthreshold region

The analytical solution for subthreshold slope is based on the capacitive model in subthreshold region (Fig. 2.). The compact capacitive component model for the VFD SONFET operating in accumulation, depletion and inversion condition is presented in /6/.

Intrinsic capacities include the capacitance of the depleted silicon body $C_{Si,d}$, gate oxide capacitance $C_{GOX}=k_{GOX}L_{eff}/t_{GOX}$, and buried oxide capacitance C_{BOX}:

$$C_{BOX} = \frac{2k_{BOX}}{\pi} \ln\left(1+\frac{L_{eff}}{2\,d_{BOX}}\right) \quad (1)$$

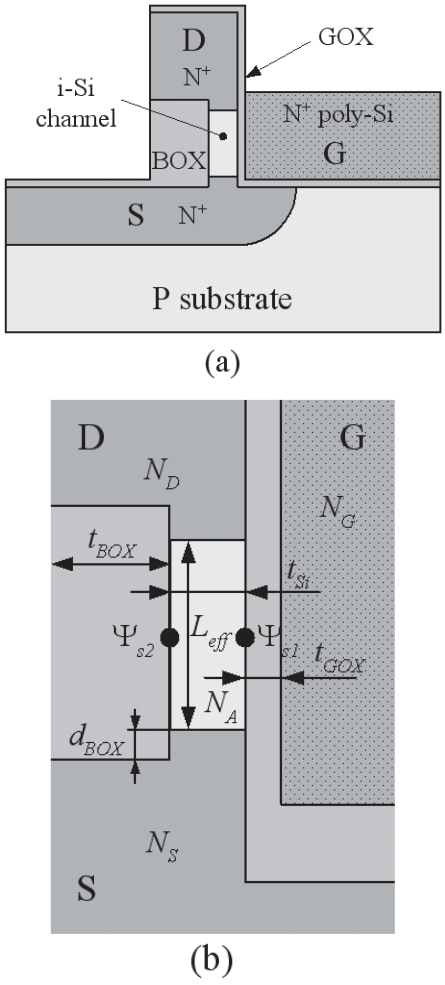

Fig. 1. (a) VFD SONFET structure cross-section, (b) VFD SONFET structure close-up.

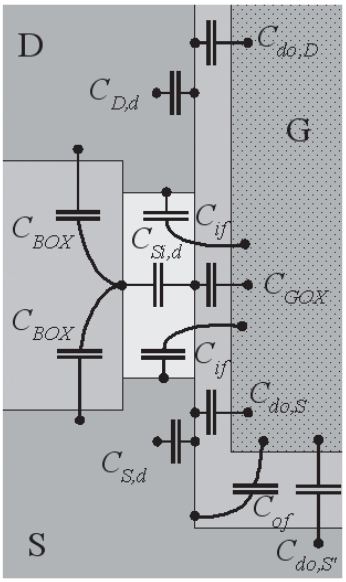

Fig. 2. Capacitive model of the VFD SONFET in the subthreshold region.

The buried oxide capacitance C_{BOX} of the VFD SONFET has specific, two-dimensional properties and its analytical relation is given with an approximation by perpendicular planes. For the effective channel lengths that are $t_{BOX} < L_{eff}/2$ analytical relation is given:

$$C_{BOX}\Big|_{t_{BOX}<\frac{L_{eff}}{2}} = \frac{2k_{BOX}}{\pi}\ln\left(1+\frac{t_{BOX}}{d_{BOX}}\right) \quad (2)$$

Overlap, fringe and source/drain depletion capacitances are also included in Fig. 2, but do not have significant influence on the subthreshold slope. Equivalent capacitive circuit of the VFD SONFET in the subthreshold region is shown on the Fig. 3.

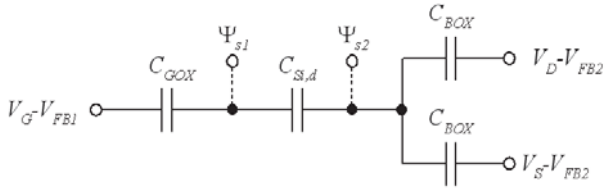

Fig. 3. Equivalent capacitive circuit of the VFD SONFET in the subthreshold region.

Applying the Ohms law at each node, we calculate the relation between the front-gate surface potential ψ_{S1} (interface gate-oxide/Si-film) and the back-gate surface potential ψ_{S2} (interface Si-Film/BOX) /Fig. 1 (b)/:

$$\Psi_{s1}\left(C_{GOX}+C_{Si,d}\right)= C_{GOX}\left(V_G - V_{FB1} + \frac{Q_{Si,d}}{2C_{GOX}}\right)+ C_{Si,d}\Psi_{s2} \quad (3)$$

$$\Psi_{s2}\left(2C_{BOX}+C_{Si,d}\right)= \\ = C_{BOX}\left(\left(V_D - V_{FB2}\right)+\left(V_S - V_{FB2}\right)+\frac{Q_{Si,d}}{2C_{BOX}}\right)+ C_{Si,d}\Psi_{s1} \quad (4)$$

where $Q_{Si,d}=-qN_At_{Si}$ is the depletion charge, $V_{FB1}=V_T\ln(N_GN_A/n_i^2)$ is the top-gate flat-band voltage, $V_{FB2}=V_T\ln(N_{S\text{-}D}N_A/n_i^2)$ is the back-gate flat-band voltage, and V_D and V_S are drain and source voltages, respectively. With source voltage being zero (V_S=0), the following relations can be used: $V_D+V_S=V_D=V_D-V_S=V_{DS}$. From the equivalent capacitive circuit, the analytical solution for the gate voltage V_G is extracted:

$$V_G = V_{FB1} + \Psi_{s1}\left(1+\frac{C_{Si,d}\,2C_{BOX}}{C_{GOX}\left(C_{Si,d}+2C_{BOX}\right)}\right)+ \\ + \frac{qN_At_{Si}}{C_{GOX}}\cdot\left(\frac{1}{C_{Si,d}}+\frac{1}{C_{BOX}}\right)\cdot\left(\frac{C_{Si,d}C_{BOX}}{\left(C_{Si,d}+2C_{BOX}\right)}\right)- \\ - V_{DS}\frac{C_{Si,d}C_{BOX}}{C_{GOX}\left(C_{Si,d}+2C_{BOX}\right)}+2V_{FB2}\frac{C_{Si,d}C_{BOX}}{C_{GOX}\left(C_{Si,d}+2C_{BOX}\right)} \quad (5)$$

2.2 Two-Dimensional Effects: Voltage Doping Transformation

An elegant and compact solution for two-dimensional model is offered by the concept of Voltage-Doping Transformation (VDT) /7/. VDT enables to account for 2D-effects into

quasi 1D-analysis of the VFD SONFET. According to this concept, the influence of the lateral field initiated by the junctions is equivalent to a reduction in the effective channel area doping. The effective doping in channel area:

$$N_A^* = N_A - \frac{\varepsilon_{Si} 2V_{DS}^*}{qL_{ef}^2} \tag{6}$$

Where

$$V_{DS}^* = V_{DS} + 2(V_{bi} + \Psi_{s2} - \Psi_{s1}) \pm \\ \pm 2\sqrt{(V_{bi} + \Psi_{s2} - \Psi_{s1})(V_{DS} + V_{bi} + \Psi_{s2} - \Psi_{s1})} \tag{7}$$

where V_{DS} is the drain-source voltage, $\psi_{bi}=V_T\ln(N_{S\text{-}D}N_A/n_i^2)$ is the built-in potential. The back-gate surface potential ψ_{s2} is given:

$$\Psi_{s2} = \frac{qN_A t_{Si} L_{eff}}{C_{BOX}} \tag{8}$$

The silicon body capacitance with short channel effects (VDT) taken into account is therefore:

$$C_{Si,d}^* = \frac{dQ}{d\Psi} = \frac{qN_A^* t_{Si} L_{eff}}{\Psi_{s1} - \Psi_{s2}} \tag{9}$$

As the subthreshold slope is defined in the regime before the onset of the strong inversion, the silicon body capacitance $C^*_{Si,d}$ will be evaluated for the front gate surface potential:

$$\Psi_{s1} = \Psi_{s1}(\text{inv}) = 2\Psi_b \tag{10}$$

where $\psi_b=V_T\ln(N_A/n_i)$ is the difference between Fermi level and intrinsic level.

2.3 Subthreshold slope model

Using the definition for the subthreshold slope as the gate voltage variation needed for the change of one decade in the drain current /8/ and applying the gate voltage solution (5) and the VDT approximation (6–10), the subthreshold slope follows as:

$$S = \frac{dV_G}{d\log I_D} = \ln(10)\cdot\frac{kT}{q}\cdot\frac{dV_G}{d\Psi_{s1}} = \\ = \ln(10)\cdot\frac{kT}{q}\cdot\left(1 + \frac{2C_{Si,d}^* C_{BOX}}{C_{GOX}(C_{Si,d}^* + 2C_{BOX})}\right) \tag{11}$$

The complex influence of the VFD SONFET parameters are combined in a simple form of (11) with second term in the bracket being responsible for the difference from the ideal S value of 60 mV/dec at 300 K. The scaling tendencies are clear from the capacitance ratio, where C_{GOX} should be increased and $C^*_{Si,d}$ and C_{BOX} decreased to approach the ideal value.

3 Calculation and simulation results

In order to verify the accuracy of the analytical model for the subthreshold slope, the calculated results are compared to a two-dimensional numerical device simulator, MEDICI /9/. Concentration dependent model for the low-field carrier mobility and the velocity saturation mobility model at high parallel electric field were used. Band-gap narrowing in silicon and polysilicon, Shockley-Read-Hall recombination and Auger recombination are taken into account. The gate current was modeled by the Lucky-electron gate current model and the simulation temperature was 300 K. The simulator does not include quantum effects. Focus of this paper is the device subthreshold characteristics where the quantum effects are less pronounced and the drift-diffusion model can be considered accurate.

The calculated and simulated subthreshold slope values plotted against effective channel-lengths L_{eff} are shown in Fig. 4. for different: (a) gate oxide thickness t_{GOX}, (b) gate dielectric k_{GOX}, (c) BOX dielectric k_{BOX}, and (d) BOX thickness t_{BOX}. The examined devices take advantage of the fully-depleted structure and have an effectively undoped channel for higher mobility. The range of effective channel-lengths investigated was between 288 nm – long channel case, and 22 nm – very short-channel. The simulated structures in each plot varied only in the effective channel-length with other dimensions and technological parameters kept the same.

For the effective channel lengths down to 100 nm, subthreshold values are close to ideal values of approximately 60 mV/dec. Agreements between the values obtained by the numerical simulations and analytical model are within 2 mV/dec (3%) for the channel lengths down to 50 nm. For shorter channel lengths (<50 nm) the deviation of our model is mainly due to the rough VDT approximation of the effective doping in channel area N^*_A and thus the calculation of the silicon body capacitance $C^*_{Si,d}$. As the channel length is reduced the influence of the last term in relation (11) becomes higher and more accurate modeling of $C^*_{Si,d}$ is necessarry.

The subthreshold slope can be improved by increasing the value of the gate oxide capacitance C_{GOX}, or by decreasing the value of the buried oxide capacitance C_{BOX}. If the gate oxide thickness t_{GOX} is scaled down /Fig. 4. (a)/ or the material with higher dielectric constant k_{GOX} is used for the gate oxide /Fig. 4. (b)/ the characteristics show expected improvements. The case of material with the lower dielectric constant k_{BOX} used for the buried oxide /Fig. 4. (c)/ also improves the subthreshold slope, as well as thinner buried oxide thickness t_{BOX} /Fig. 4. (d)/.

4 Conclusions

The subthreshold slope model extracted from the compact capacitance model of the VFD SONFET has been demonstrated. It has been shown that the developed model has high accuracy for channel lengths down to 50 nm and can be extended even further with improvement of the voltage-doping transformation, which is used to account for short-channel effects. With the simple processing of the VFD SONFET, devices with very short gates can be fabricated and the presented model used for the prediction of the subthreshold behavior. The specific, two-dimensional

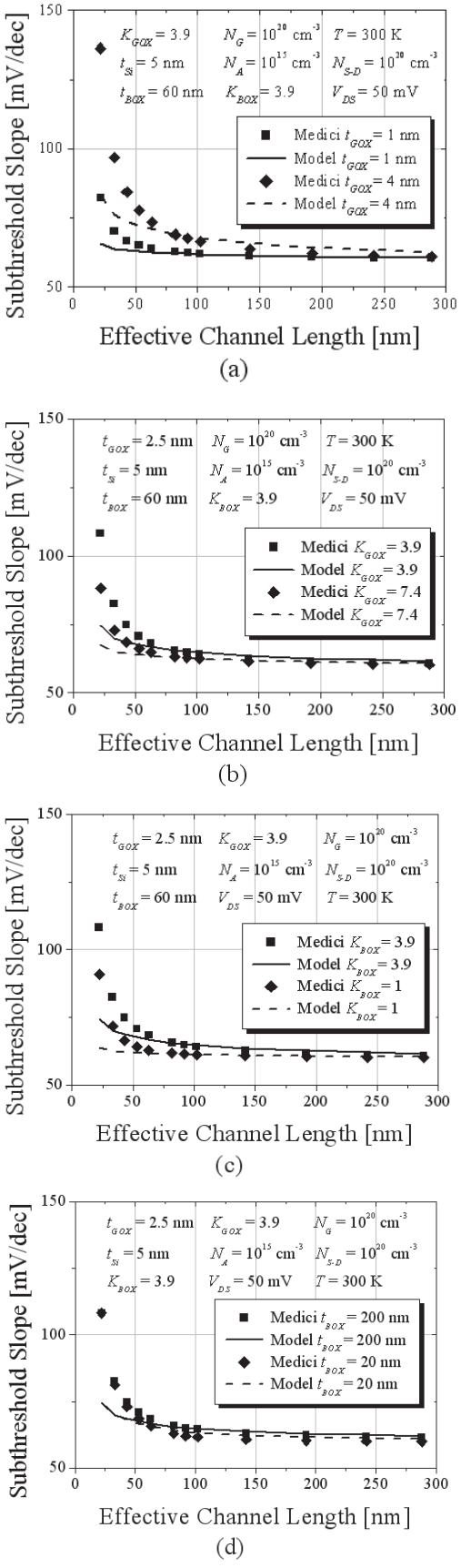

Fig. 4. Comparison of subthreshold slope values against effective channel lengths obtained by MEDICI simulations and analytical model for different: (a) t_{GOX}*, (b)* k_{GOX}*, (c)* k_{BOX}*, (d)* t_{BOX}*. K=k/*ε_0*.*

characteristics of the VFD SONFET structure are accurately described in the model and combined in a simple relation for the subthreshold slope. This offers clear insight into influences of different parts of the structure and can be used to estimate the performance of scaled devices.

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TWO-DIMENSIONAL OPTICAL MODEL FOR SIMULATING PERIODIC OPTICAL STRUCTURES IN THIN-FILM SOLAR CELLS

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Key words: optical modelling, thin-film solar cells, periodic structures, light management

Abstract: Novel optical concepts based on periodic structures such as diffractive gratings are important for thin-film solar cells since they exhibit high potential of light management. In order to simulate and optimize the periodic structures different approach is needed in comparison to widely used one-dimensional approaches. In this paper a two-dimensional finite element numerical approach is described to solve the Maxwell's differential equations of the propagating light in thin-film structures. The different boundary conditions that can be applied at the borders of the simulation domain are presented. The concepts how to efficiently solve the system and how to obtain the final optical parameters of the solar cells - reflectance, absorptances in the layers, charge carriers generation rates - are described. The model is verified with the measurements of the total reflectance at realistic diffractive gratings. Simulation results of a complete amorphous silicon solar cell with the diffractive gratings are presented.

Dvo-dimenzionalni optični model za simulacijo periodičnih optičnih struktur v tankoplastnih sončnih celicah

Kjučne besede: optično modeliranje, tankoplastne sončne celice, periodične strukture, vodenje svetlobe

Izvleček: Novi optični pristopi osnovani na periodičnih strukturah, kot so uklonske mrežice, so v tankoplastnih sončnih celicah pomembni, saj izkazujejo velik potencial pri vodenju svetlobe v strukturi. Za simulacijo periodičnih struktur ne zadostuje samo uporaba klasičnih eno-dimenzionalnih pristopov pač pa se moramo poslužiti dvo-dimenzionalnih simulacij. V prispevku je predstavljen dvo-dimenzionalen simulator, ki temelji na reševanju valovne Maxwellove enačbe širjenja svetlobe znotraj sončne celice na podlagi metode končnih elementov. Opisani so različni robni pogoji, ki jih uporabimo v simulacijah za zaključitev računskega območja. Podani so načini, kako določiti izhodne optične parametre simuliranih sončnih celic (odbojnost, absorpcija svetlobe v plasteh, profili generacij prostih nosilcev naboja). Rezultati simulacij so ovrednoteni s primerjavo izmerjenih odbojnosti izdelane uklonske mrežice. Na koncu so prikazani rezultati optične simulacije celotne tankoplastne amorfno-silicijev sončne celice.

1. Introduction

In thin-film (TF) solar cells light trapping is of great importance, since absorber layers are very thin (from one hundred nanometers to few micrometers). To capture light inside the absorber layer efficiently the scattering of light at internal interfaces is needed. In this way light paths throughout the layers are prolonged and the number of light passes increased due to enhanced back reflectances at internal interfaces. In current state-of-the-art silicon TF solar cells randomly textured substrates are used to introduce interface texture in the cell structures /1-3/. However, to further improve and use the potential of light scattering process, new approaches of light management are becoming important. One of them are periodic structures, such as diffractive gratings, which can be applied to the interfaces to efficiently scatter light only into specific, but very large angles /4/. Large angles can consequently lead to a significant increase of the light paths and to the total internal reflectance of the scattered light rays at the front interfaces of the solar cell structures. The integration of diffractive gratings in thin-film solar cell structures have already been investigated experimentally /5, 6/ and by numerical simulations /7-10/. The results of current structures of solar cells, including the gratings, indicate that the potential of the diffractive gratings has not been exploited fully. Thus, further investigations of diffractive gratings and especially of their integration and optimization in the TF solar cell structures is of great importance. Numerical modelling and simulation present here an important tool.

To analyse optical situation at the grating, implemented in the structure of thin-film solar cells, at least a two dimensional simulator is needed. Some two- or three- dimensional (2-D, 3-D) simulators for the analysis of the diffractive gratings in the solar cells have already been reported e.g. /7-10/. However, the simulators have certain drawbacks, since they are mostly developed for general usage in the field of electromagnetic wave propagation and are not adapted and optimized to the specific structures, such as TF solar cells. One of the drawbacks is, for example, that is difficulty to simulate not-rectangular shapes of the grating features (triangles, sine shape etc.). The slopes of the different shapes are usually roughly approximated by rectangular steps, which can not give good representative results especially if only a few steps are used for approximation. Sharp edges of even small rectangles can affect the simulation results noticeably. Another drawback is that the output results are not the quantities that are important for TF solar cells (like optical reflectance, R, absorptance, A, charge carrier generation rate, G_L).

In this paper we present our 2-D optical simulator which has been developed for the analysis of TF solar cell structures including diffractive gratings and other periodic structures. The model is based on the finite element numerical method (FEM) /11/. One of the specialities of the model is that the simulation domain is represented by triangular elements rather than rectangular. These way different shapes can be more easily and effectively described. The details of the model and other advantages of the simulator, based on the model are presented. The boundary conditions that can be applied at the borders of the simulation domain are described. The determination of the electric and magnetic field distribution in the structure will be explained. The methods to calculate standard optical quantities used in the field of photovoltaics, such as R, A, G_L will be presented. Mathematical methods and techniques how to manipulate large data matrix and how to calculate out the desired results are briefly described. The verification results of the simulator and the simulations of the complete amorphous silicon solar cell are presented.

2. Optical model

2.1 Electromagnetic background

The optical model is based on Maxwell's wave equations in the frequency domain (Eqs. 1).

$$\nabla\times(\frac{1}{\mu}\nabla\times\mathbf{E})-\omega^2\varepsilon\mathbf{E}=-j\omega\mathbf{J}$$

$$\nabla\times(\frac{1}{\varepsilon}\nabla\times\mathbf{H})-\omega^2\mu\mathbf{H}=\nabla\times(\frac{1}{\varepsilon}\mathbf{J}) \qquad \text{Eqs 1.}$$

where E and H are the complex vectors of the electric and magnetic field of propagating waves, $\mu = \mu_r\mu_0 = (\mu_{Re} - j\mu_{Im})\mu_0$ and $\varepsilon = \varepsilon_r\varepsilon_0 = (\varepsilon_{Re} - j\varepsilon_{Im})\varepsilon_0$ are the complex permeability and the complex permittivity of the material ($\mu_0 = 4\pi\times10^{-7}$ H/m, $\varepsilon_0 = 8.854\times10^{-12}$ F/m), ω is the angular frequency and J is the complex vector of the current density. In a 2-D space problem it is assumed that the field components (E and H) and media (μ_r, ε_r) do not change in the third dimension (axis z in our case). Thus, the Eqs. 1 can be written in the form of differential equations for two dimensions as given in Eqs. 2.

$$\left[\frac{\partial}{\partial x}(\frac{1}{\mu_r}\frac{\partial}{\partial x})+\frac{\partial}{\partial y}(\frac{1}{\mu_r}\frac{\partial}{\partial y})+k_0^2\varepsilon_r\right]E_z=$$

$$=jk_0Z_0J_z \text{ - TE wave}$$

$$\left[\frac{\partial}{\partial x}(\frac{1}{\varepsilon_r}\frac{\partial}{\partial x})+\frac{\partial}{\partial y}(\frac{1}{\varepsilon_r}\frac{\partial}{\partial y})+k_0^2\mu_r\right]H_z=$$

$$=-\frac{\partial}{\partial x}(\frac{1}{\varepsilon_r}J_y)+\frac{\partial}{\partial y}(\frac{1}{\varepsilon_r}J_x) \text{ - TM wave} \qquad \text{Eqs 2}$$

where x and y are the spatial directions (x – lateral, y - vertical), k_0 is the wavenumber in vacuum and is defined as $\omega\sqrt{\varepsilon_0\mu_0}$, Z_0 is the impedance of vacuum ($Z_0=\sqrt{\mu_0/\varepsilon_0}$). The subscripts of the field and current components indicate the directional component of the vectors. In Eqs. 2 it is considered that the electromagnetic wave is transversal (electric and magnetic field vectors perpendicular to each other) /11/. The wave is divided into the transverse Electric (TE) and transverse magnetic (TM) wave. In the case of TE wave, the wave is entirely represented by electric field component in z axis, E_z, whereas in the case of TM wave, the wave is entirely represented by the magnetic field in the z axis, H_z. Since the incident light consists both components of polarization (TE and TM), both equations included in Eq. 2 need to be considered.

The geometry of the periodic structure was described by choosing the triangular elements as basic building elements of mesh (Fig. 1a and 1b). Eqs. 2 have to be solved for each element in the mesh-grid, where we assume that the properties of material (μ_r and ε_r) are constant within the element. The alignment of the triangular elements in the grid is shown in Fig. 1c. All the elements are of the same size.

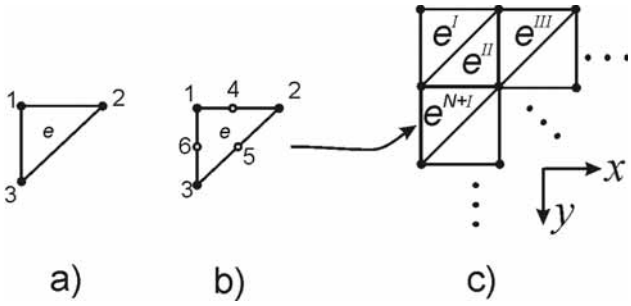

Fig. 1: Basic elements used in our optical model: a) triangular element for linear approximation of unknown function (field), b) triangular elements for quadratic approximation of unknown function and c) discretization of simulation domain with triangular elements (with either linear or quadratic approximation).

For each triangular element the unknown function ϕ (representing E_z or H_z) at the position of the element has to be determined along the three borders of the element. In our simulator we have implemented two options: a) linear approximation (Fig. 1a, Eq. 3) and b) quadratic approximation (Fig. 1b, Eq. 4) of the unknown function along the borders of the element.

$$\phi^e(x,y)=a^e+b^ex+c^ey \qquad \text{Eq. 3}$$

$$\phi^e(x,y)=a^e+b^ex+c^ey+d^ex^2+e^exy+f^ey^2 \qquad \text{Eq. 4}$$

In Eq. 3 and 4, x and y are the 2-D spatial directions (see Fig. 1), where the superscript e indicates that the approximation is related to one-element level. The symbols a-f are the constants that have to be determined in the calculation process. In the case of linear approximation the function Φ is determined for the three nodes presenting the corners of the triangle (Fig. 1a). In the case of the quadratic approximation at each border line of the element an additional node is added, resulting in six calculation nodes

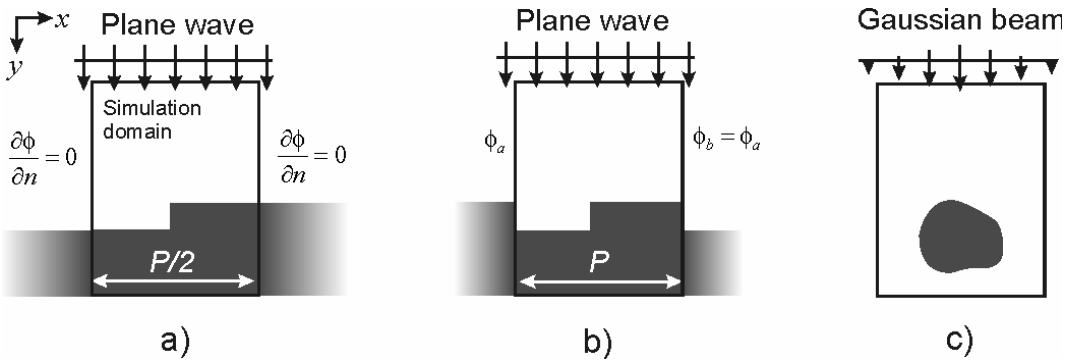

Fig. 2: Different boundary conditions for different configurations of simulation domain: a) periodic symmetric configuration, b) general periodic configuration and c) open region configuration - bounded system.

(Fig. 1b). The use of quadratic approximation has found to be useful when the abrupt changes in the field or spikes in the field are expected.

2.2 Boundary conditions

Determination of the size of the simulation domain and application of the mesh-grid to our periodic structure are crucial steps, which are both related to the boundary conditions applied to the borders of simulation domain.

Typically the structures are periodically repeated (infinitely) in lateral direction in our case. Two different types of boundary conditions applicable to the problem will be explained here. One type is related to the periodicity and lateral symmetry (left and right border according to examples in Fig. 2), whereas the other one is related to the incident (radiated) and outgoing field (top and bottom border of the simulation domain).

In the case of first type of boundary conditions (left, right border), application of three different boundary conditions is illustrated in Fig. 2a, 2b. In Fig. 2a the example of the application of the homogeneous Neumann condition /11/ is shown. In this case the first derivative of the field at the left and right border is zero (the divergence of field is zero). According to the figure this condition enables that only half of the period (*P*/2) is included in the simulation domain. Next, taking the whole period of the structure in the simulation domain (Fig. 2b) the field at the left and the right borders should be set to the equal values (virtually connected boundary system). The reason is the periodicity of the structure acquired in the simulation domain. Therefore, this condition is assigned to the periodic boundary condition /11/. The third condition which can be applied to the left and right border is absorbing boundary condition (ABC, Fig. 1c) /11/. This case is assigned to an open-region configuration in the lateral direction (structure with limited lateral dimensions, the whole structure is included in the simulation domain). An ideal boundary condition here would be zero reflectivity of waves at the borders. To approach this ideal case different orders of the ABC conditions can be used /11/.

For the second type of the boundary conditions (top, bottom border of the simulation domain) the above mentioned ABC condition is applied at the top and bottom border in all the cases.

In Fig. 2a and Fig. 2b for the illumination source the perpendicular plane wave is used, in Fig. 2c, a laterally limited illumination is applied (e.g. Gaussian beam). This enables us to simulate also the laterally limited non-periodic structures with limited area of light illumination.

In Figs. 2 the structures consists of only one layer (the diffractive grating below) and the incident medium above. However, in the model more layers (e.g. complete solar cell structures) can be applied with different type of the interface morphology. The vertical and lateral geometry are described with optical properties (ε and μ) for each node in the mesh-grid.

2.3 Solving the system

To solve the differential equations (Eqs. 2) for each node of the element the Ritz method is applied /11/. Boundary conditions, linear or quadratic approximation of Φ, illumination source (plane wave or Gaussian beam) are considered. In the Ritz method the differential equations are transformed in the mathematical functional. Finding solutions for Φ at each node is based on minimising the functional /11/. As a final result of the Ritz method the following matrix description is obtained (Eq. 5)

$$\mathbf{K\Phi}=\mathbf{b} \qquad \text{Eq. 5}$$

where K is the matrix of the system coefficients (the size of *N* x *N*; *N* – number of all nodes in the simulation domain), Φ is the vector (the size of *N*) of the system unknowns (*E* or *H*) and *b* is the vector (the size of *N*) of the light sources (different than zero only at the nodes at the top border, where the incident field is applied). The matrix **K** is sparse, symmetric, with complex numbers and it is not positive-definite. Its elements consist information of the material properties (ε and μ) at the nodes.

It has to be noted that *N* in our case can even be more than a million, depending on the problem. Due to the large

size of the matrix K (N x N) the memory consumption in the computer program can become a problem, especially if the direct methods for solving (e.g. Gauss elimination, LU decomposition /12/) are used, due to generation of new non-zero elements. To solve such a system, iterative methods are recommended /12, 13/. We found out that in our case the solution can be efficiently obtained by using non-stationary gradient iterative methods: the special form of Conjugate Gradient (CG) method /11/, Bi-Conjugate Gradient (Bi-CG) and Quasi-minimal residual (QMR) method /12/. The CG method was found to be slow, but relatively stable, however the Bi-CG and QMR were found to be fast but less stable. In order to improve the condition of matrix and also to stabilize the method different preconditions were implemented into CG, QMR and Bi-CG algorithms. The easiest precondition used was the Jacobian precondition /13/, leading to a good convergence. However, in some special cases with the Bi-CG method we could still obtain divergence of the method, especially when the sharp metal structures were simulated, where the high spikes in the field might occur. In order to stabilize the method we have implemented the Symmetric Successive Over-Relaxation (SSOR) precondition /13/. The simulations with the SSOR precondition needed less iterations to obtain the result compared to Jacobian precondition.

The very large sparse system needed to be efficiently solved in the fastest time as possible and also with using very low memory consumption. Special attention has to be paid on the description of sparse matrixes in order to fasten the computation time when calculating the product of the sparse matrices with vectors in the calculation procedure, since these products have been found as the most time consuming. Another simplification considering the solving of system is to use mesh-grid consisted of the elements of the same size and of same orientation in the grid (pre-defined regular grid, Fig 1c). This way we do not need additional large matrix to describe the mesh.

2.4 Determination of the output parameters of the simulation

After the field E_z or H_z has been obtained at each node, the calculation of the final output parameters is performed. In our optical analysis, optoelectronic structures like thin-film solar cells are investigated. The following parameters are defined as the main output parameters: the total reflectance from the structure, R_{tot}, the absorptance inside individual layers of the structure, A_{layer}, and the 2-D generation rate across the structure, G_L, of the photo generated electrons and holes in the active layers.

The R_{tot} of the structure is calculated at the top border, where also the incident wave is generated. The basis for the R_{tot} calculation presents the Poynting vector **S** = (**E** x **H***)/2 ("*" presents the conjugated value). By considering only its normal direction (y axis) the R_{tot} can be determined as $R_{tot} = S_{y\_refl} / S_{y\_inc}$, where the subscripts "refl" and "inc" correspond to the reflected and the incident component of the Poynting vector. These two components can be obtained from the calculated total and known incident field values at the top border ($E_{refl} = E_{tot} - E_{inc}$, $H_{refl} = H_{tot} - H_{inc}$). This results in the final equation for R_{tot} (Eq. 6):

$$R_{tot}(TE) = \left| \frac{\mathrm{Im}\left(\frac{E_{refl}}{\mu}\frac{\partial E^*_{refl}}{\partial y}\right)}{\mathrm{Re}\left(\frac{k_m}{\mu}E_{inc}E^*_{inc}\right)} \right|$$

$$R_{tot}(TM) = \left| \frac{\mathrm{Im}\left(\frac{H_{refl}}{\varepsilon}\frac{\partial H^*_{refl}}{\partial y}\right)}{\mathrm{Re}\left(\frac{k_m}{\varepsilon}H_{inc}H^*_{inc}\right)} \right| \qquad \text{Eq. 6}$$

Absorption inside the single element in the layer A_l^e and inside entire layer A_l can be calculated as (Eq. 7), which is derived from Poynting's theorem.

$$A_l^e = \frac{\omega\mu_0\mu_i}{2}HH^* + \frac{j\omega\varepsilon_0\varepsilon_i}{2}EE^* \quad A_l = \sum A_l^e \qquad \text{Eq. 7}$$

where μ_i and ε_i are imaginary parts of permeability and permittivity corresponding to the element. To obtain absorption of a layer one has to sum up all the absorptions of the elements which are composing specific layer.

Generation rate profile is calculated from the local absorption (absorption of the elements) and is given by Eq. 8 for one element e.

$$G_L^e(\lambda) = \frac{\lambda}{hc}\frac{A_l^e I_{inc}}{\frac{dxdy}{2}}l_x \qquad \text{Eq. 8}$$

where h is Planck constant, c is speed of light and I_{inc} is illumination power density.

3. Verification results and simulations of the solar cells

Based on the presented optical model a computer simulator FEMOS-2D was developed. A user friendly interface enables simple simulation of the multilayer structures, including diffractive gratings, in the entire solar spectrum. The results of simulations were verified by comparing them to the measurements obtained on realistic samples. In Fig. 3 the structure of one of the samples as well as the Atomic Force Microscopy (AFM) scan of its surface is shown. On the polycarbonate substrate, which is typically used for CDs, DVDs or BDs, the periodic grating structure was embossed with the periodicity of P = 700 nm. On the top of the polycarbonate substrate 100 nm thick layer of an aluminium alloy was deposited. By means of AFM the shape of the grating surface was determined. In our case the sine shape was used in simulator to describe the grating shape with the height of h = 40 nm as determined from the AFM measurements. The sine shape agrees with the measured AFM profile very well, however, realistic shape of the profile can be imported in our simulator. The other input pa-

rameters for simulation were realistic wavelength dependent refractive indices of the layers and polarization of light. In simulations we used un-polarized light, 50 % of TE and 50 % of TM polarization, approaching to the realistic illumination in our measurement. In Fig. 4 the measurements and simulation of the R_{tot} of the grating as a function of light wavelength is shown. All measurements of R_{tot} were done with Lambda950 spectrophotometer from which unpolarized monochromatic light in the range from 400 to 1000 nm was obtained.

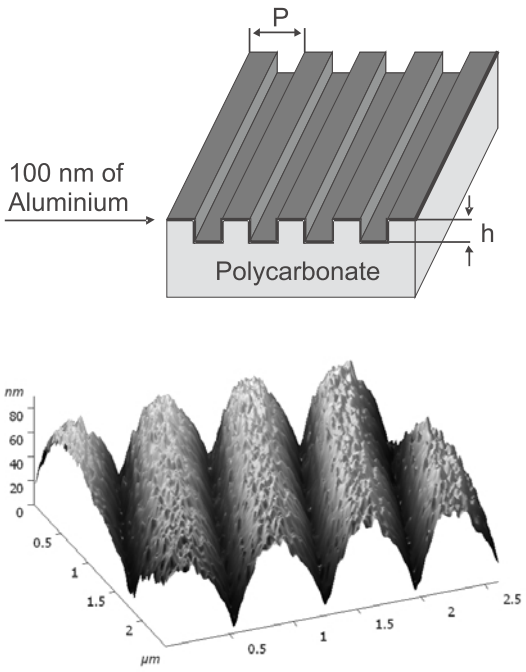

Fig. 3: Analysed grating structure with thin film aluminium layer (100 nm) on the top of the polycarbonate substrate. On the right the AFM measurement of the left structure is presented.

Good agreement is observed between the measured (dashed curve) and simulated (full curve) R_{tot} of the grating structure. For comparison also the simulation of the flat structure is shown (dash-dot curve). In this relatively simple structure the effect of the grating is related to the decreasing spike at the wavelength of 700 nm. This spike is due to additional absorption in aluminium alloy at the grating structure in the mentioned wavelength region. In this wavelength region the anti-reflective effect and light scattering in the first diffraction order /4/ occur. In the simulation and measurement (not shown in the figure) of the flat structure no spike is observed.

In the next step we simulated the whole thin-film amorphous silicon solar cell deposited on the 2-D grating (substrate configuration). The structure of the cell is as follows: Al/n-a-Si:H(20 nm) / i-a-Si:H(200 nm) / p-a-Si:H(10 nm) / ZnO:Al(500 nm) on the top (see insert in Fig. 5). At all interfaces the sine shape of gratings was used, with the height of 150 nm and with two different periods (300 and 400nm). The wavelength dependent refractive indices, $N(\lambda)$

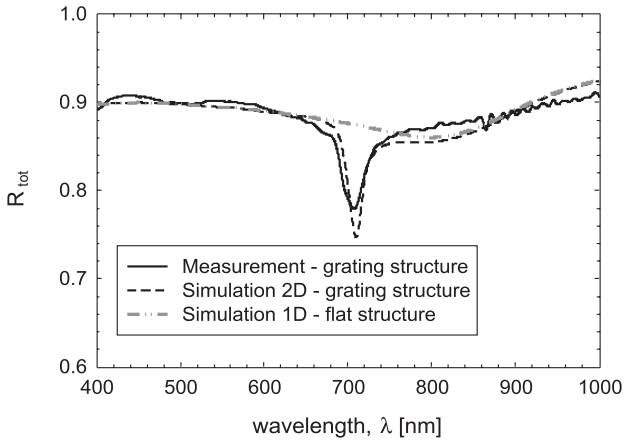

Fig. 4: Measured and simulated total reflectance of the aluminium grating structure with P*=700 nm and* h *= 40 nm showing in Fig. 3.*

of the realistic layers were used to determine the $\varepsilon(\lambda)$ of the materials needed in the simulation.

In Fig. 5 the simulated absorptance in the i-a-Si:H layer of the solar cell is plotted for selected grating parameters. The grating should act as an efficient scatterer in the cell, leading to enhanced absorptance in the i-a-Si:H layer. Higher absorptance in the mentioned active layer leads to a higher short-circuit current and quantum efficiency of the solar cell. The 2-D simulations reveal the increase in absorptance is partly due to antireflective effect of the textured front interfaces and partly due to scattering effect of gratings at the interfaces. The simulations showed that by changing the period of the grating (in Fig. 5 shown for the case of P = 300 nm and 400 nm) in this case it is affecting the position of the interferences in the absorptance curve.

The presented simulator enables the direct study of the relation between the (periodic) surface morphology and light scattering. This is a very important point in the simulations of photovoltaic devices with textured interfaces (most of them), where the optical situation inside the structure cannot be measured, thus, simulations are needed to optimize the structures. This way the direction towards the optimal texturing can be indicated. Extending the simulator to the randomly textured interfaces it can be used to evaluate and select different TCO substrates from the light scattering point of view. However, analysis of the regularly textured interfaces (such as gratings) can already give useful information about improvements of randomly textured interfaces. Further on, special optical effects in the solar cell structure can be investigated with the simulator, such as plasmon absorption at textured metal back contacts. Minimizing the optical losses in metal, related to this absorption, by possibly optimizing the texture shapes is one of the important issues, other advantage of our simulator is also that it is highly customized for a solar cell application, but can be also used for other EM problem.

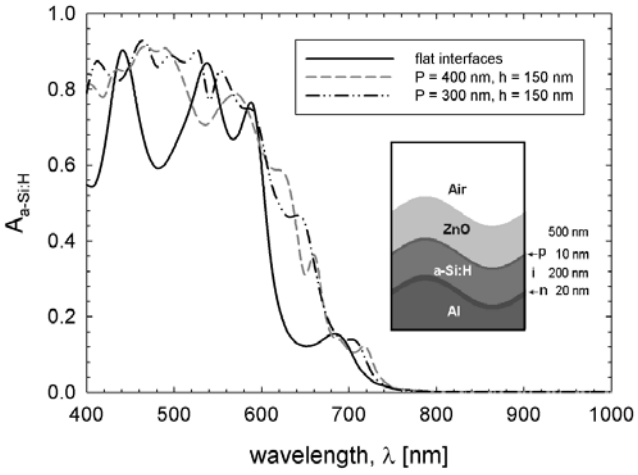

Fig. 5: Simulated absorptance of the i-a-Si:H layer in the complete amorphous silicon solar cell structure with the sine grating applied to all interfaces.

4. Conclusions

Two-dimensional optical model for solving electromagnetic wave equations at periodical structures - diffractive gratings - was presented. The model is based on robust FEM method and solves differential equation for both (TE and TM) polarizations. Special attention was paid on boundary conditions and how to effectively solve the system discretized differential equations. This way we were able to obtain accurate results of simulation in the shortest time.

One of the main advantages of the optical model is simulation of arbitrary (periodic) interfaces shapes, where a good approximation of the interface texture can be achieved by using triangular elements instead of rectangular. The simulator based on the developed model is especially dedicated to simulation of optoelectronic structures such as thin-film solar cells. It automatically calculates the main optical output parameters from the field, such as absorption in individual layer of the structure, total reflectance and 2-D generation rate profile at each discrete element. The simulator is optimised for speed of the calculation and for low memory consumption to allow large number of discretization points.

Simulation results of Al based grating structure with the period of 700 nm is compared with the measured total reflectance of the sample. Good agreement is observed, indicating the validity of the simulations. The result of optical simulation of a complete amorphous silicon solar cell with different periods of the incorporated grating is presented. The developed optical simulator presents a powerful tool for further investigation of light management in thin-film solar cell with the diffractive gratings and other textures.

5. Acknowledgement

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SMD FILM CAPACITORS FOR INTEGRATING A/D CONVERTERS

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Key words: integrating A/D converter, SMD film capacitor, dielectric absorption, humidity, surface resistance, polymer dielectric

Abstract: Lead free technology has significantly influenced the choice of commercially available capacitors, especially those intended for surface mount. A case study of the appropriate SMD capacitor selection for a high accuracy integrating A/D converter is presented. The converter is part of a smart sensor that encompasses a simple microcontroller and an analog transducer, which is in this case a platinum resistor. An overview of traditional and new polymer dielectric materials is given with the emphasis on the commercial selection of SMD capacitors. Trends of the film capacitor industry in the recent years are explained through the physical properties of the materials used and the imposed legislative restrictions. The often overlooked pitfalls of capacitor selection are sequentially described. The effect of the dielectric absorption of the charge on the conversion error is theoretically analyzed for the intermittent mode of operation. Inaccuracy due to the recovery of the absorbed charge is eliminated by the use of a polyphenylene sulfide (PPS) film capacitor; however, at high humidity some capacitive sensors exhibit abnormal deviations.

Based on some additional experiments, we determine the influence of the capacitor's parallel resistance on the conversion result. The synergic impact of high humidity, temperature, and flux residues on the surface resistance of stacked capacitors is proven by experimental measurements carried out in a climatic chamber. The experimental measurements of SMD capacitor insulation resistance show that naked stacked capacitor construction is not suitable for relative humidity above 80%. In such cases, slightly larger encapsulated SMD capacitors must be used to maintain the desired high accuracy.

SMD filmski kondenzatorji za integracijske A/D pretvornike

Kjučne besede: integracijski A/D pretvornik, folijski SMD kondenzator, dielektrična absorpcija, površinska upornost, polimerni dielektrik

Izvleček: Prepoved uporabe svinca v tehnologiji izdelave tiskanih vezij je pomembno vplivala na tržno ponudbo kondenzatorjev, namenjenih za površinsko montažo. V prispevku je podan potek izbire ustreznega kondenzatorja za integracijski A/D pretvornik z visoko ločljivostjo. Sam D/A pretvornik je del inteligentnega senzorja, ki ga sestavlja mikrokrmilnik in ustrezen analogni merilni pretvornik, v opisanem primeru je to platinski upor. V delu je najprej podan pregled polimernih dielektrikov s poudarkom na njihovi rabi za SMD komponente. Trendi zadnjih let v industriji kondenzatorjev za elektroniko, so opisani s stališča fizikalnih lastnosti dielektričnih filmov in prepovedi rabe svinca v elektronskih napravah. Spregledane pomanjkljivosti izbranega tipa, so podane zaporedno, kot so se pojavljale pri razvoju. Izpeljali smo analitično zvezo med dielektrično absorpcijo kondenzatorja in pogreškom posamične pretvorbe. Merilno napako zaradi sproščanja absorbiranega naboja v času pretvorbe, smo odpravili z uporabo polifenil sulfidnega (PPS) kondenzatorja.

Z eksperimenti v klimatski komori smo ugotovili, da imajo nekatera vezja nenormalno velika odstopanja, ki nastanejo zaradi vpliva vlage na gole PPS kondenzatorje. Izpeljali smo analitično zvezo med velikostjo skupne upornosti med sponkama kondenzatorja in merilno napako. Ugotovili smo sinergični vpliv vlage, temperature in ostankov fluksa na površinsko upornost nezaščitenih kondenzatorjev, ki so izdelani z zlaganjem metaliziranega filma. Meritve izolacijske upornosti so pokazale, da takšni kondenzatorji niso primerni za vlažnosti zraka nad 80 %. Za precizni integrator so primernejši dimenzijsko nekoliko večji SMD kondenzatorji v plastičnem ohišju.

1. Introduction

Electronic integrators offer a simple solution for achieving an accurate A/D conversion of low voltage levels whenever the speed of conversion doesn't play a significant role. Dual slope integrating A/D converters can be implemented by low cost digital microcontroller and a simple additional analog circuit. Such A/D converters can be used for accurate conversion voltages that are proportional to slowly varying physical quantities like temperature or atmospheric humidity.

Conversion errors due to the non-idealities of the analog components, i.e., the input offset voltage of the operational amplifier (opamp), are minimized by a simple solution, so that low-cost analog components can be used. The choice of utilized capacitor seems unimportant since the value of capacitance does not appear in the conversion equations at all/1/. Such an approach is over-simplified but this fact does not become obvious until experimental measurements of prototypes under various climatic conditions are performed. The physical dimensions of electronic circuits are steadily decreasing, which is a consequence of the growing demand for hand-held devices. The introduction of surface-mount technology (SMT), which became widely used around the year 1990, engendered important changes in the field of high performance metallized film capacitors. The small size of SMD capacitors has raised many problems in their construction, because of the intense heat transfer from the metallized soldering pads to the plastic dielectric film during the reflow soldering process.

The first widely used SMD capacitors were multilayer ceramic chips (MLCC). This construction and the high relative dielectric constant of the ceramics result in such capacitors having a high capacitance packing density and relatively low equivalent serial resistance (ESR). The inorganic nature of the dielectric used in MLCCs minimizes the impact of the thermal stress during soldering. Polymer film capacitors are much more affected by the raised tem-

perature levels because of the thermoplastic nature of the dielectric film. The choice of SMD polymer film capacitors on the electronic components market is predominated by trough-hole film types and by ceramic SMD chips. As a consequence, film capacitors are rather expensive, therefore cheaper alternatives are used wherever it is possible.

In the next chapter an overview of the important polymer dielectric materials is given, followed by a case study of the capacitor selection for an integrating A/D converter. Finally, the results of practical experiments are presented. The comments on the outcomes and some practical hints for the selection of appropriate SMD polymer film capacitors conclude the paper.

2. Materials for film capacitors

The traditionally used plastic materials for dielectric films in capacitors are polystyrene (PS), polyester (PE), polycarbonate (PC) and polypropylene (PP). These materials are used for film capacitors with low loss and stable capacitance in the range from 1 nF up to 10 mF. Film capacitors below 1 nF are offered only by a small number of producers; and especially SMD types are very rare. The range of capacitances below 100 pF is almost exclusively covered by C0G ceramic capacitors, which are featured with a low capacitance temperature coefficient a_C and the dissipation factor tan$d$.

2.1 Polystyrene capacitors

For years, polystyrene (PS) capacitors were the best choice for critical analog applications. In the middle of the 1990s the production of PS capacitors slowly ceased. There were several reasons that caused polystyrene capacitors to disappear from production. The maximal operating temperature of PS film and capacitors is very low, only 85°C (see Table 2). Additionally, the low heat resistance of PS film allows neither the construction of SMD components nor the vacuum-deposition of aluminum, hence only film/foil capacitors were (are) produced. This construction lacks the self-healing capability, i.e., the ability to clear faults (such as pores or impurities in the film) under the influence of voltage. Although PS capacitors have low absorption of moisture, they can be easily damaged by printed board cleaning solvents. PS capacitors that are still available from old stocks are not intended for new designs. New materials like polyphenylene sulfide (PPS) should be used instead of PS.

2.2 Polycarbonate capacitors

Polycarbonate (PC) metallized film and film/foil capacitors were traditionally the logical choice in high performance applications for operation at elevated temperatures. This material is featured with a negligible temperature coefficient α_C for temperatures in the range of 20°C ÷ 40°C, which is the common operating temperature range of precision electronic equipment. In spite of the higher operating temperatures of this film, commercially available PC capacitors for surface mount were never produced. In the year 2000, the major producer of PC capacitors WIMA from Germany /2/, ceased their production after finding it unprofitable. This decision caused the major producer of capacitor grade PC film, Bayer AG, to stop its production upon completion of the final order. Nevertheless, PC film capacitors are still available and produced at least by Electronic Concepts Inc. from USA with its own in-house produced dielectric film /3/. Polycarbonate film is almost the perfect material for high performance capacitors but is very sensitive to moisture absorption, thus good encapsulation is required to protect the dielectric film against humidity. Hermetically sealed PC capacitors are available only with wired trough-hole terminals and are primarily intended for military applications.

2.3 Polyester capacitors

Polyester films have become the standard dielectric for capacitors in electronic applications. Polyester film for capacitors is biaxially oriented polyethylene terephthalate (PET) developed by DuPont in the mid-1950s and is well-known under the trade name Mylar. This material has good mechanical and electrical properties for temperatures in the range from -55°C to +125°C. Their high dielectric strength, and the highest dielectric constant among commercially used dielectric films, make PET capacitors low-cost and volume-effective. Metallized PET film capacitors are produced in any combination of the construction alternatives given in Table 1.

Table 1: Manufacturing and construction alternatives of PET capacitors

Parameter	Alternative	
Environmental protection	Naked	Protected
Mounting terminals	SMD	Trough hole
Construction	Stacked	Wound
RoHS compliance	Yes	No

These capacitors are the most frequently used type of plastic film capacitors in electronic circuits – primarily for DC or low frequency purposes - because the dissipation factor tan$d$ of polyester is the highest among contemporary film materials. Even though it is not a high quality material, in many respects, PET films perform much better than multilayer ceramic capacitors (MLCC) using X7R or Z5U dielectric ceramics. Some producers, e.g., AVX /4/, offer PET-HT capacitors with an improved temperature range of up to +125°C with a nominal voltage derating factor of 1.25 %/°C above T_R = 105°C, which represents an increase of 20°C with respect to the standard types.

2.4 Polypropylene capacitors

Polypropylene (PP) film has, for many years, been used for high performance applications, especially for medium and high power electronic circuits where high impulse current capability is required. This material has very low dielectric absorption *DA* making a PP capacitor the best choice for the charge-storing device in precision integrators, sample and hold amplifiers and other electronic circuits that retain analog signals in the form of electric charge. Additionally, PP capacitors are characterized by a constant temperature coefficient α_C = -200 ppm/°C and the second highest volume resistivity among dielectric film materials (Table 2). The main deficiency of PP is its somewhat limited temperature range, which prevents the construction of PP as an SMD component. Standard PP capacitors use metallized film and film/metal foil construction for self-healing and high impulse current capability, respectively.

2.5 Polyphenylene sulfide capacitors

Polyphenylene sulfide (PPS), a dielectric material with excellent electrical and thermal properties, was invented by Toray/Japan. This chemical company started the production of capacitor grade PPS film in 1988 under the trade name of Torelina®, and is still the only producer. In the same year PPS capacitors were made commercially available by WIMA/Germany, but their production was plagued with many difficulties. In 2001 WIMA /2/ temporarily ceased their production due to problems connected with inconsistent film quality and availability. A detailed examination of self-healing of different metallized polymer films by Walgenwitz et. al. /5/ has shown only insignificant distinctions among PET, PEN and PPS. In any case, achieving self-healing in PPS film is not a particular problem. The problematic availability of PC capacitors, the European Council Directive on the Restriction of Hazardous Substances (RoHS Directive, 2002/95/EC) /6/, and good mechanical properties of biaxially oriented PPS film at higher temperatures have prompted numerous activities for the reliable production of PPS capacitors. The construction of SMD film capacitors has become very demanding due to the elevated melting point of leadless soldering compounds. After the break in 2000 WIMA restored the production of PPS capacitors, encouraged by a mixture of technological and commercial factors. After 2001 both trough hole and SMD types of PPS metallized capacitors were made generally available by several manufacturers.

PPS has excellent electrical properties that exceed PC in many aspects. Almost no sensitivity to humidity and a far higher operating temperature range are the most important attributes of PPS when compared to PC. Despite the advantages of PPS film (expressed by the figures in Table 2), this material has two shortcomings. Firstly, it is expensive and secondly, it is produced only by Toray/Japan, which may cause hitches in its supply.

2.6 Polyethylene naphtalate capacitors

Polyethylene naphtalate (PEN) was not used for film capacitors until 2000. The RoHS directive adopted by the EC in 2003 caused producers of electronic components to utilize substitutes for the existing materials as these could not stand the thermal stress generated by elevated soldering temperatures without significant degradation. The electrical properties of PEN film are very similar to those of PET, but the overall performance of PEN is inferior – provided that the maximum operating temperature is not taken into account /7/. PEN capacitors are larger than the corresponding PET types because the dielectric constant ε_r and the dielectric strength E_B of PEN are lower. The ratio of PEN capacitor size to the corresponding PET capacitor is between 1.5 and 2. PEN film SMD capacitors are in compliance with the RoHS directive, and are suitable for IR or vapor phase reflow processes. PEN capacitors are

Table 2: Properties of capacitor dielectric materials

Parameter	Unit	Dielectric								
		PS	PC	PET	PEN	PP	PPS	PTFE	C0G	X7R
Dielectric constant ε_r		2.2	2.9	3.3	3.0	2.2	3.0	2.0	12…40	700...2000
Dielectric strength	V/µm	100	200	400	300	600	250	150	200	
C temperature coefficient α_C	Ppm/°C	-120	±80	+600	+200	-300	-150	-80	±30	±1000
Dissipation factor tanδ (1 kHz)	10^{-4}	5	15	80	80	5	20	1	15	350
Volume resistivity ρ	Ωcm	10^{18}	10^{16}	10^{17}	10^{17}	10^{18}	10^{17}	10^{19}	10^{17}	10^{16}
Dielectric absorption *DA*	%	0.01	0.1	0.5	1.2	0.02	0.05	0.01	0.6	2.5
Operating temperature T_{min}/T_{max}	°C	-55 125	-55 100	-55 105	-55 125	-55 100	-55 140	-55 200	-55 125	-55 125
Self-healing		no	yes	yes	yes	yes	yes	no	no	no
SMD configuration		no	no	yes	yes	no	yes	no	yes	yes

also featured with improved temperature stability with respect to PET. The capacitance temperature coefficient α_C of PEN is approximately only one third of the α_C of PET. The dielectric absorption *DA* of PEN is the biggest among the polymer film dielectrics. Its value of approximately 1 % is the order of magnitude of *DA* specified for MLCCs using X7R ceramics.

2.7 Other dielectric materials

Three types of dielectric materials, that have not been mentioned previously, are also listed in Table 2. Polytetrafluoroethylene (PTFE) better known under DuPont Company's trade name Teflon®, is an excellent insulating material, but PTFE film capacitors are very rare. Proper metallization of PTFE film is very difficult, this material is very expensive and films of a thickness < 6 µm are not commercially available /7/. PTFE capacitors are used in high power applications where their high operating temperature range and low dissipation factor justify their high price.

The data on ceramic dielectric materials in Table 2 are given for comparison, since MLCC chips are very popular and cheap. In fact only C0G ceramics, also known as NP0, are a real match for polymer films as far as stable high performance capacitors go. In addition to the materials discussed, X7R ceramics offer a cost and room efficient solution when large capacitances in small packages with low equivalent serial resistance (ESR) are required.

3. Capacitor for integrating A/D converter

3.1 Four slope integration

Dual slope integration is a well-known method for accurate A/D conversion /1/. Accuracy and resolution are two distinctive features of such A/D converters. The resolution of integrating converters is determined by the ratio between the period of the clock that is used for counting and the time of integration, which is measured in clock periods. Arbitrary resolution can be achieved by appropriate selection of these two parameters, but at high resolutions conversion times can become unacceptably long, since maximal counter frequencies are limited. On the other hand, the accuracy of the result is determined by the used reference, if everything else is done ideally.

Integrating A/D conversion is very useful for measuring slowly varying quantities, e.g., strain, temperature, humidity, illumination etc. Furthermore, smart sensors with digital output can be designed as a combination of a standard microcontroller, an integrating A/D converter, and an analog sensor of a physical quantity. Low cost uncalibrated sensor devices may be used, without compromising the accuracy of the final result because the deficiencies of the analog sensing device are compensated numerically. The required signal conditioning data are obtained by calibration in the final stage of production and consequently stored in the nonvolatile portion of memory.

The pitfalls of capacitor selection are illustrated by the case of the small resistive temperature sensor. The important, i.e., the analog part of the smart sensor is shown by the simplified schematic diagram in Figure 1.

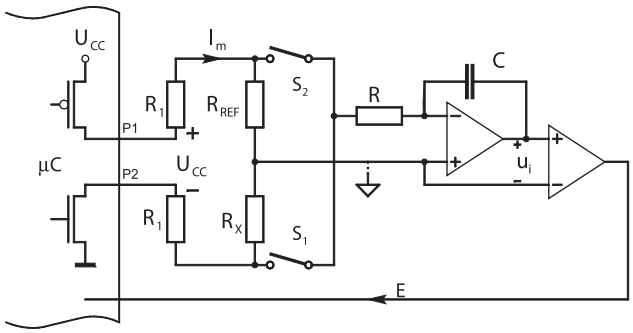

Fig. 1: Integrating A/D converter

The conversion is initiated by closing switch S_1 for fixed time t_0 determined by a certain number of clock periods. The integrator output voltage u_i ramps up, reaching a maximum value that is proportional to the voltage across the sensor resistance R_X. At the end S_1 is opened and S_2 is closed. The output ramps down with a slope that is proportional to the voltage of a very stable resistor R_{REF}. When the integrator voltage becomes negative with respect to analog ground, the timer inside the microcontroller is stopped by the negative edge of the comparator output *E*. The plots of main converter signals are shown in Figure 2.

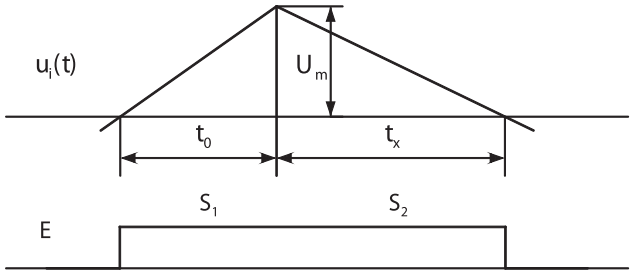

Fig. 2: Time diagram: u_i integrator output, E comparator output

The peak integrator voltage can be expressed by

$$U_m = I_m R_x \cdot \frac{t_0}{RC} = I_m R_{REF} \cdot \frac{t_x}{RC} \qquad (1)$$

where I_m represents the measuring current through the sensor R_X and reference resistor R_{REF}, respectively. From the unknown resistance of the sensor is given by

$$R_x = R_{REF} \frac{t_x}{t_0} \qquad (2)$$

meaning that only the stability of R_{REF} has influence on the result accuracy. This would be true if the opamp and comparator were ideal. The dual slope principle is not sensitive to the instability of the integrator time constant *RC* as

long as the constant remains unaltered during conversion time $t_0 + t_x$. The integrator peak voltage U_m given by remains unaffected by the comparator input offset voltage, since the counting of both times, charging t_0 and discharging t_x, are started and stopped at the same integrator voltage, respectively. The actual conversion is started by closing S_2 until the integrator output u_i becomes negative then both switches (S_1 and S_2) are toggled. The charging time t_0 counter is not triggered until the rising edge of the comparator output *E.*

The input offset voltage U_0 of the opamp in the integrator induces an error that can be expressed as

$$\Delta R_X = \frac{2U_0}{I_m} \tag{3}$$

with I_m denoting the measuring current (Figure 1). As it is shown in /8/ this error is compensated by reversing the polarity of the measuring current I_m, which is done by negation of the logic outputs P1 an P2 (Figure 1). The accurate result is the mean of the results obtained with both polarities of the current I_m

$$R_x = R_{REF}\,\frac{t_{x1} + t_{x2}}{2\,t_0} \tag{4}$$

The procedure with four slopes of integration, shown in Figure 3, doubles the required conversion time, but low cost opamps with offset voltages $|U_0| \leq 1$ mV may be used.

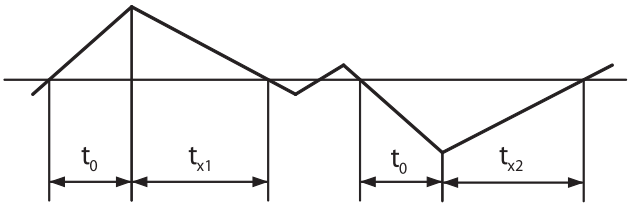

Fig. 3: Plot of the integrator output $u_i(t)$ in the four slope A/D converter

3.2 Dielectric absorption

The analyzed integrator is part of an intelligent resistive sensor of small physical dimensions (25 × 9 mm), therefore small passive components are used. The long integration time, which is necessary to achieve the prescribed resolution, and the low supply voltage require relatively large capacitance C = 100 nF that prevents the integrator output from reaching saturation. The first logical choice was an X7R ceramic chip capacitor, characterized by its small dimensions and SMD package. The value of capacitance appears neither in eqn. nor in , therefore the temperature coefficient and tolerance are not important for this purpose.

Experimental tests have shown poor accuracy in the intermittent mode of operation. The sensor was designed for battery powered systems, so the analog part of the circuit is powered only when the conversion takes place. Dielectric absorption of the capacitor has been overlooked, and the effect of the absorbed charge has not been noticed in continuous mode since the capacitor mean voltage is zero.

For the great majority of capacitor applications the dielectric absorption coefficient *DA* is not an important parameter. It matters only in some sample and hold circuits, and obviously in integrators that operate once in a while and have long integrating times. This phenomenon can be measured as a small voltage that reappears across the open capacitor terminals after a charged capacitor has been thoroughly discharged /10/. When voltage is applied to the capacitor plates a certain small part of the stored charge becomes bound on the surface of the dielectric. The process of charge recovery is governed by pretty long time constants that depend merely on the used dielectric material. Measurement of the absorption coefficient *DA* according to the standard MIL-C-19978 D /9/ is depicted in Figure 4.

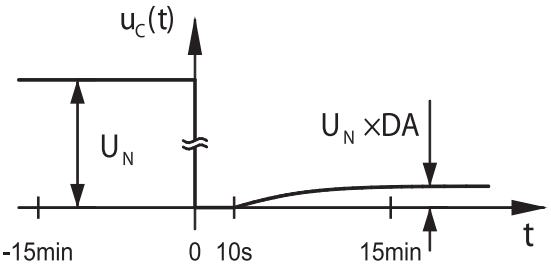

Fig. 4: Timing and definition of voltages associated with the measuring of the dielectric absorption (U_N denotes nominal voltage).

The effects of dielectric absorption in electric circuits are studied by suitable models that replace the capacitor in question. These models /11/, /12/ can be quite complex but in most cases a simple model shown in Figure 5 is sufficient for basic understanding. For commonly used dielectrics, 50% of the final voltage is recovered in 1 to 10 seconds, whereas it can take as much as 15 minutes to reach within 5% of the final value.

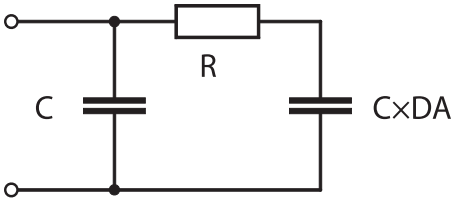

Fig. 5: The basic model of the dielectric absorption in capacitors

The resistance in the model of Figure 6 is given by

$$R = \frac{\tau}{DA \cdot C}, \tag{5}$$

where τ denotes the dominant recovery time constant and *DA* is the absorption coefficient (Table 2). The values of τ for particular materials are usually not specified and have to be determined by experimental measurements if a greater accuracy than the generally presumed range from 1 to 10 s is desired.

Detailed analysis has shown that the integrating capacitor was charged almost to supply voltage (U_{cc} = 3.3 V) when

the negative supply pin of the amplifier chip was not tied to ground to reduce supply current. The error caused by recovered charge is drastically reduced by the four slope integration method. The error of *n*-th successive measurement after the amplifier is turned on is given by

$$\frac{\Delta R_X}{R_X} = \frac{U_{C0}\, DA}{2U_m}\left(1 - e^{-\frac{T}{\tau}}\right)^2 e^{-\frac{2T}{\tau}(n-1)} \qquad (6)$$

where U_{C0} is the integrating capacitor initial voltage, $T = t_0 + t_X$ is the conversion time of one polarity, τ is the dominant time constant of the absorbed charge recovery, and U_m is the peak voltage of the integrator (Figure 2). The used ceramic chip capacitor has turned out to be completely inadequate for accurate temperature measurements on the basis of platinum resistors. Errors due to the dielectric absorption of the consecutive resistance measurements of the platinum resistor R_x (Pt 1000) are shown in Table 3. The results are expressed as temperature errors in °C using the temperature coefficient of platinum 3850 ppm/°C. The values in Table 3 are calculated using for two different absorption coefficients, whereas the other parameters are the same: U_{C0} = 3.3 V, U_m = 1V, τ = 3s, T = 1s. The errors calculated for X7R ceramics are in good agreement with the measurements, which have initiated more detailed analyses.

Table 3: Error of consecutive A/D conversions expressed in temperature

Consecutive measurement no.	ΔT [°C]	
	DA = 2.5% (X7R)	*DA* = 0.05% (PPS)
1	0.860	17×10^{-3}
2	0.442	8.84×10^{-3}
3	0.227	4.54×10^{-3}
4	0.116	2.33×10^{-3}
5	0.059	1.19×10^{-3}

The theoretical error caused by the absorption of PPS film SMD capacitor is smaller than the desired resolution of the design, therefore raw conversion data, i.e., timer counts that measure time t_x, have been observed. The raw results of consecutive conversions (after power up) are within plus minus one count, provided that the temperature is constant.

4. Tests in climatic chamber

4.1 Naked PPS SMD capacitor

Encouraged by the theoretical results (Table 3) an adequate substitution for the X7R MLCC has been found in the form of the stacked PPS film capacitor. These capacitors are almost a perfect choice and feature a very low absorption coefficient *DA* and very low dissipation $\tan\delta < 5\cdot10^{-4}$ in the temperature range from -25°C to 80°C. The data for PPS shown in Table 2 are rather misleading because the worst values over the whole temperature range are given. In addition, PPS capacitors are available as small SMD components that save space on the PCB and fit on solder pads provided for the former ceramic capacitor. The construction of naked stacked film capacitors is shown in Figure 7. The lateral side is usually left without any coating /4/.

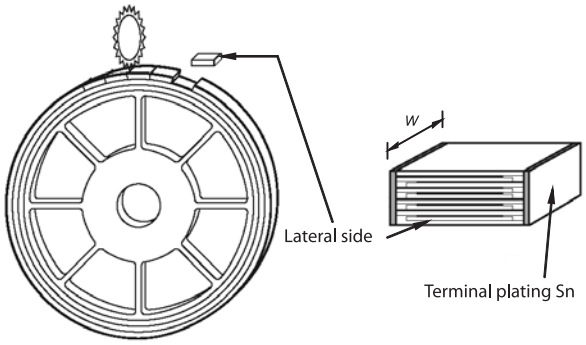

Fig. 6: Production and construction of stacked naked PPS film chip capacitors

In stacked-film production technology, large rings of metallized film are wound onto core wheels with diameters up to 60 cm. Then the rings are sawed apart obtaining well defined width (dimension *W* in Figure 6). In this way, capacitances with very low tolerances are obtained, since the active body is very homogenous, without the air pockets which are typical of flattened wound bodies. Actual measurements have proved that PPS capacitors have negligible dielectric absorption; hence no differences have been detected between the results of the first and immediately repeated measurements.

Upon the verification of the calibrated sensors, some of them returned values that were up to 2°C lower than the actual temperature in the chamber, which was 12°C. Among the 120 devices under test, about 10% were bad, i.e., $|\Delta T| > 0.1$°C. It turned out that humidity inside the chamber had run out of control. At temperatures around 12°C the humidity had exceeded 90%. The deviation of certain circuits was obviously influenced by humidity, so protection against moisture should improve the performance of the PCB in humid environments. Polyurethane coating applied to the assembled PCBs did not help. The deviations of the bad circuits remained unacceptable.

Since it was not clear which part of the circuit was affected by humidity, several experiments were carried out. The results in Figure 8 show that high humidity and temperature affect the four slope A/D converter. In this experiment the temperature dependent resistors (Pt1000) of three sensors were kept outside the climatic chamber at a constant temperature, while the PCBs were exposed to temperatures increasing in increments at high humidity and decreasing at low humidity, respectively. As one can note from the plots in Figure 7, the impact of the temperature increments in the presence of high humidity is not the same

for all circuits, but when humidity is low the circuits are left virtually unaffected.

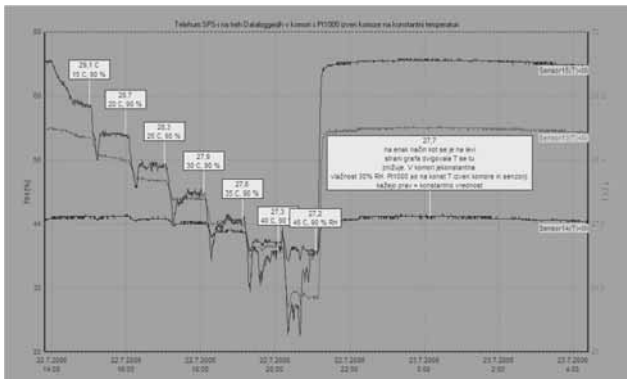

Fig. 7: Measurement results of three sensors with naked PPS capacitors: at high humidity RH = 90% the chamber temperature was increased in 5°C increments from 15°C to 45°C, then the air was dried to RH = 30% and the temperature was decreased to 15°C, again in decrements of 5°C. Each step of this temperature reduction lasted 1hour.

Next, the integrating PPS chip capacitors of the three tested samples were replaced by encapsulated PET capacitors with wire terminals and then the same experiment was repeated. The plots that are shown in Figure 8 reliably indicate that certain PPS chip capacitors were affected by high humidity and not the PCB itself. The results registered by the third sensor are meaningless since a fault occurred during the replacement of the capacitor. The steps in the upper and middle plot are a consequence of the temperature coefficients of each reference resistor R_{REF}, because the sensors were kept at different, i.e., constant temperatures during the test.

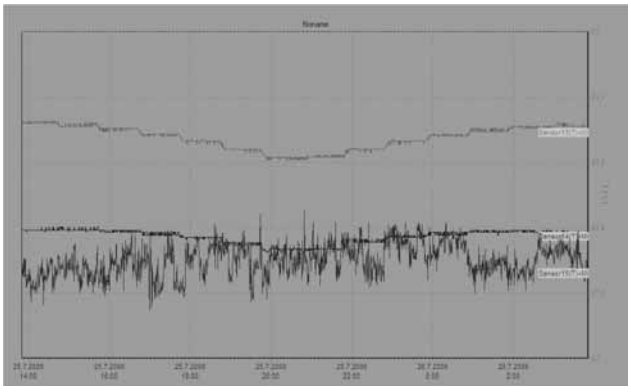

Fig. 8: Measurement results of three sensors with encapsulated PET capacitors: at RH=90% the chamber temperature was increased in increments of 5°C from 15°C to 45°C (the left half of the diagram), then the air was dried to RH=30% and the temperature was decrementally reduced down to 15°C.

4.2 The influence of humidity on insulation resistance

Obviously, some of the used PPS capacitors were influenced by moisture. The influence of absorbed moisture on capacitance was excluded by empirical immersion tests, so only the surface resistance between capacitor terminals R_P remains as the possible cause of inaccurate conversion, if this resistance is decreased due to air humidity. First, we have to estimate the order of magnitude of such a decrease of resistance that could cause the observed inaccuracies. As is shown in Figure 9, the parallel resistance represents a leak for the charge stored in the integrating capacitor. The sensitivity can either be derived from the exact analytic solution, or a few simple approximations can be used. The latter alternative is presented as follows.

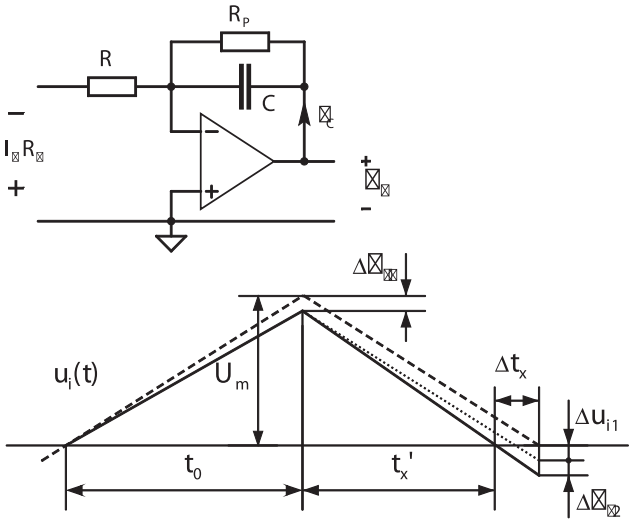

Fig. 9: Integrator with insulation resistance R_P (above), plot of integrator output voltage u_i with (–––) and without R_P (- - -) (bellow)

At the end of the first step of conversion the peak integrator output is reduced by

$$\Delta u_{i1} = \frac{\Delta q}{C} = -\frac{1}{C}\int_{t}^{t+t_0} \frac{u_i(t)}{R_P}\,dt = -\frac{1}{2}\cdot\frac{U_m\, t_0}{R_P\, C} \qquad (7)$$

with Δq denoting the charge that leaks through R_P and U_m is the voltage that would be reached if there were no leakage, i.e., $R_P \to \infty$. The shape of $u_i(t)$ in is considered straight and $\Delta u_{i1} = U_m$ is neglected in the integral. During the second step of conversion, $u_i(t)$ decreases faster than in the ideal case (Figure 9) and after discharging for t_0 it would become negative. The relative error of the conversion

$$\frac{\Delta t_x}{t_x} = \frac{\Delta u_{i1} + \Delta u_{i2}}{U_m} = \frac{2\Delta u_{i1}}{U_m} = -\frac{t_0}{R_P\, C} \qquad (8)$$

where t_x is approximated by t_0, hence $\Delta u_{i2} = \Delta u_{i1}$. In our special case where the actual input voltage is proportional to the resistance of the platinum temperature sensor it is convenient to express the difference between the measured and the actual temperature

$$\Delta T = \frac{\Delta R_x}{R_x} \cdot \frac{1}{\alpha_R} = -\frac{t_0}{R_P C \cdot \alpha_R} \qquad (9)$$

where α_R denotes temperature coefficient of platinum. The plot of this temperature deviation for C = 100 nF, t_0 = 0.5 s and α_R = 3850 ppm/°C is shown in Figure 10.

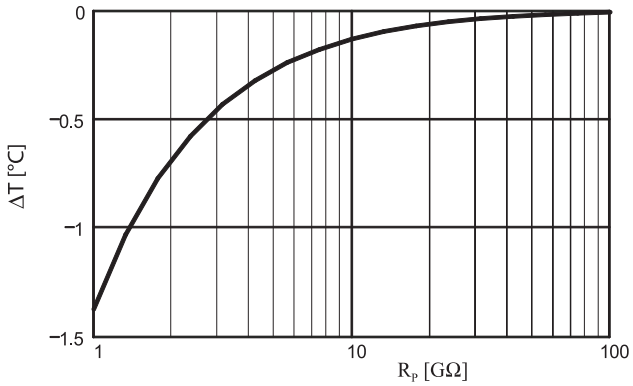

Fig. 10: Deviation of measured temperature vs. insulation resistance R_P

The derivation of eqn. is carried out only for the first phase of A/D conversion because both phases of the actually implemented four slope conversion are equally influenced by the charge leak. According to capacitor producer AVX /4/ the insulation resistance of a 100 nF capacitor is > 60 GΩ for T < 75 °C. Under normal conditions such values of R_P cannot engender noticeable deviations. Moreover, the constant resistance that appears between the capacitor terminals is taken into account during calibration, so that the conversion results in operation are influenced only if this resistance is decreased owing to environmental influences.

The theoretical plot in Figure 10 shows that the parallel resistance has to decrease to about 1 GΩ when the result fails for approximately -1.5 °C. Such errors can be noted in the experimental results shown in Figure 7, where it is obvious that in the presence of damp air the parallel resistance of some capacitors is reduced to 50% or less by rising the temperature for 5°C.

4.3 Insulation resistance measurements

Both our theoretical and experimental findings have been verified by measurements of two sets of PPS film capacitors (100 nF/16 V), i.e., brand new capacitors and the desoldered ones, which were removed from the assembled PCBs that turned out as bad. The new capacitors were immersed for 24h in a 20% isopropyl alcohol (IPA) water solution. The immersion caused no measurable differences in the capacitance and dissipation factors. The measured capacitance tolerance of all samples was les than 1%. Furthermore, the insulation resistance of the devices was measured at different air humidities. The leakage current at the applied voltage 1V was measured by a precise picoampermeter. The results are summarized by mean values in Table 4.

Table 4: Mean values of insulation resistance at U_{DC}=1V and T= 25°C,

Relative Humidity [%]	R_i	
	new	*desoldered*
35%	100 GΩ	100 GΩ
60%	40 GΩ	100 MΩ
90%	10 GΩ	30 MΩ

The results in Table 4 clearly indicate that the origin of the noticed inaccuracies lies in the resistance between the capacitor terminals. PPS capacitors have very low moisture absorption, but the naked types are affected by the side effects of PCB assembly, because the new devices perform much better when leakage is involved. The work of Hunt and Zou /13/ has shown the importance of appropriate selection of the flux in the soldering paste. The residues of soldering fluxes contribute to the surface conductivity as the humidity is increased. This effect is especially pronounced for weak organic acid (WOA) based fluxes at high humidity (> 85%). It has been already mentioned that the PCB's were protected against moisture but that these efforts turned out to be unsuccessful. The tested sensors were washed in deionized water, dried and protected with a thin polyurethane coating (Urethane 71) but the surface of some PPS chip capacitors remained contaminated by flux residues. The applied coating should be substantially thicker, which is a rather unpractical solution.

The weak point of the naked chips is the exposed lateral sides (Figure 7) on which the metal atoms that form the capacitor plates can be found. These lateral sides are additionally vulnerable due to the small gaps between the clusters of stacked dielectric film. It is almost impossible to clean these gaps once they get contaminated. The first prototypes were soldered by hand using ordinary soldering wire filled with resin. In this case, increasing the humidity does not reduce the surface resistivity /13/, therefore the high humidity effects were not noticed until a different technology of PCB assembly was used. It is important to note the fast response of the observed leakage current to the changes in humidity, which obviously points to the fact that only the surface of the capacitor is involved in this process.

5. Conclusion

The choice of SMD film capacitors on the market has gone through significant changes that were initiated by the EC RoHS directive. New high temperature dielectric materials have been introduced in production. PET, PEN and PPS films are used for plastic film SMD capacitors. Special attention must be paid during the assembly of PET capacitors with regard to the reflow soldering process. PEN and PPS capacitors tolerate slightly higher temperatures in the reflow soldering process which in turn is beneficial for the reliability and quality of the leadless solder contacts. PEN

capacitors should be avoided if dielectric absorption is important. PPS capacitors are now commonly available from various producers, but are the most expensive.

The construction of the capacitor should be carefully selected for each particular application. Stacked film capacitors have tight tolerances and require the least space on the PCB. As described in this paper, their naked construction is vulnerable to humidity, which reduces the parallel resistance due to surface conductivity. Wound capacitors are made by individually rolling the metallized film ribbons into cylindrical rolls which are then flattened to a prismatic shape. Wound capacitors are less sensitive to humidity, since the outer layers of the roll protect the capacitor core inside. Wound types are available naked or encapsulated in plastic boxes that provide additional protection against the environmental influences. Both variants of wound capacitors require more space on the PCB than the stacked one.

The described case study shows the importance of careful component selection from amongst the variety that is offered on the market. Besides choosing the right dielectric material, it is equally important to consider the construction of the capacitor. Of course, it is almost impossible to anticipate the behavior and interactions of real components that are exposed to harsh climatic conditions. In addition, accurate integrating ADCs that require high insulation resistances ($R \geq 50$ GΩ) are suitable only for applications that are well protected against humidity. If such protection cannot be provided in a simple and cost-effective way other ADCs should be used. In any case, intensive computer-controlled testing of prototypes in climatic chambers is an important step in the good design of demanding electronic products.

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COMPARISON OF INDUCTOR MODELS USED IN ANALYSIS OF THE BUCK AND BOOST CONVERTERS

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Key words: dc-dc converters, SPICE, inductor models

Abstract: The inductive devices with the ferromagnetic core are widely used in many electronic circuits, for example in the buck and boost converters, to store magnetic energy. They should be treated as nonlinear devices, and the nonlinearity of their characteristics arises from the dependence of inductance on current. In the paper the influence of the nonlinear and linear inductor models on some selected characteristics of the above-mentioned converters is compared. As a tool to compute these characteristics SPICE was used.

Primerjava modelov induktivnosti uporabljenih pri analizi konverterjev

Kjučne besede: DC-DC konverterji, SPICE, modeli induktivnih komponent

Izvleček: Induktivne komponente na feromagnetnih jedrih pogosto uporabljamo v mnogih elektronskih vezjih, npr. v DC-DC konverterjih, za shranjevanje magnetne energije. Potrebno jih je obravnavati kot nelinearne elemente , saj njihova nelinearna karakteristika izhaja iz tokovne odvisnosti induktivnosti. V prispevku primerjamo vpliv linearnih in nelinearnih modelov induktivnosti na delovanje konverterjev. Pri analizi smo uporabili program SPICE.

1. Introduction

In the dc-dc converters, which are the basic part of switched voltage regulators, the inductors with ferromagnetic core are used to store magnetic energy /1, 2/. These inductors should by characterized by the high value of the permeability and the high value of the saturation induction. The inductor with the ferromagnetic core is a nonlinear device, what results from the dependence of its inductance on current. The inductance decreases strongly with current, when the operation point of the core is moved to the saturation range of the magnetic induction, and it can cause the limitation of the allowable output current (or the load resistance) of a voltage regulator.

To design the dc-dc converters and other electronic circuits computer programs are used, and nowadays SPICE belongs to the most popular computer tools /3, 4/. In SPICE the models of many electronic devices are built-in, and to obtain reliable results of analysis, they should be simple, accurate and with credible values of their parameters. As far as inductors are concerned their linear and nonlinear SPICE models are described in /5/.

In Sec. 2 the nonlinear model of inductor is presented, and the basic characteristics and parameters of the selected inductor under consideration are given. As the main purpose of this paper is to show the influence of the nonlinear model of the inductor on some important characteristics of the typical buck and boost converters, therefore the basic characteristics of these circuits with the linear and nonlinear inductor models taken into account were computed to this end, and they are shown and discussed in Sec. 3. By comparing the characteristics obtained on the nonlinear model with the characteristics obtained on the linear one some remarks concerning the usefulness of the nonlinear model in the analysis of the converters are given in Sec. 4.

2. Nonlinear model of inductor

In SPICE two nonlinear models of the inductors with the ferromagnetic core are attainable: Jiles-Atherton model (JA model) /6/ and SPICE Plus model. On the models the hysteresis curve B(H) causing this nonlinearity can be calculated. In the paper /9/ the results of the computations obtained on SPICE, showing the sensitivity of the nonlinear dependence L(i) on the parameters of the JA model, are given.

In SPICE the isothermal analysis, which is the analysis at any constant ambient temperature, is possible, without taking into account the temperature rise caused by energy losses (the self-heating phenomenon) in the inductor. The electrothermal model of the inductor allowing the electrothermal analysis with the self-heating taken into consideration is proposed in /7/.

The essential dependences of the JA model needed to compute the curve B(H) are as follows

$$B = \mu_0 \cdot (H + M) \tag{1}$$

$$M_{an} = \frac{MS \cdot H}{/H/ + A} \tag{2}$$

$$\frac{dM}{dH} = \frac{1}{1+C} \cdot \frac{M_{an} - M}{K} + \frac{C}{1+C} \cdot \frac{dM_{an}}{dH} \tag{3}$$

where: B — magnetic induction, μ_o – permeability of vacuum, H – magnetic field, M – magnetisation, M_{an} – initial magnetisation, and the parameters of the model are: MS – saturation magnetisation, A – thermal energy parameter, K – domain anisotropy parameter, C – domain flexing parameter. On the computed dependence B(H) the incremental permeability μ can be obtained, which is needed to calculate the inductance L.

To compute the dependence L(i), at first the magnetic field H is calculated at any assumed current i according to

$$H = \frac{i \cdot z}{l} \tag{4}$$

where: z – number of coils, l – length of the magnetic path (core model parameter PATH). When H is given, the hysteresis curve B(H) can be computed on the basis of the formulae (1-3), then the incremental permeability μ at the assumed current can be calculated, and the inductance L is given as follows /8/

$$L = \frac{z^2 \cdot \mu_0 \cdot S}{l} \cdot \frac{dB}{dH} \tag{5}$$

where S – the cross-section of the core (core model parameter AREA).

In the computations presented below the following values of the parameters of the considered core were assumed /9/: MS = 412.2 A/m, A = 44.82 A/m, K = 25.74 A/m, C = 0.411 A/m (taken from SPICE library MAGNETIC.LIB for K528T500_3C8 core). The magnetic path was l = 3.84 cm, the coil number z = 10 and the cross-section area of the core S = 0.63 cm^2. The hysteresis curve at the frequency f = 10 kHz and the dependence L(i) of the inductor computed with the above given parameters values are shown in Fig. 1a, b, respectively.

As seen from Fig. 1a, the saturation induction of the considered core amounts about 430 mT (after converting units of measure, as in SPICE the magnetic field is denominated in oersted (Oe) and the magnetic induction in gauss (Ga)). The derivative dB/dH attains its maximum value at the inductor current equal to about 100 mA .

As seen from Fig. 1b, for the inductor under consideration the inductance L decreases with current increase from L = 590 μH in low and medium current range to L = 35 μH at 1 A, what corresponds to the start of the saturation range of the B(H) curve, and next up to L = 0.2 μH at the high current equal to about 100 A, when the operation point is placed in the deep saturation range of the dependence B(H).

3. Influence of inductor models on the characteristics of converters

The computations of the selected characteristics were carried out for the buck (Fig. 2a) and boost (Fig. 2b) converters. The following basic characteristics were considered: the dependence of the output voltage V_o and the

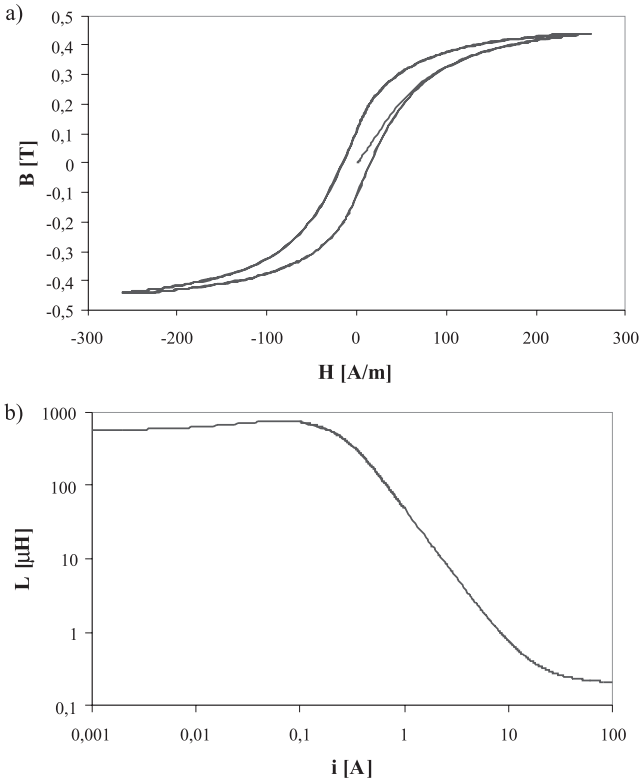

Fig. 1. The hysteresis curve B(H) of the core (a), and the dependence of the inductance on the inductor current (b)

efficiency η on the load resistance R_o, on the duty factor d and on the input voltage V_i. Additionally, the dependence of the peak-to-peak output voltage (ripples) V_{pp} on the load resistance was computed as well. These dependences were computed with the nonlinear model of the inductance L, which characteristics (Fig. 1) and parameters values are given in Sec. 2, and, for comparison, with the linear model at three values of the inductance L equal to 590 μH (corresponding to the low and medium current range), with 35 μH (corresponding to i = 1 A) and with 0.2 μH (corresponding to i = 100 A). The computations were carried out by SPICE at the ambient temperature T = 300 K. In these computations the SPICE built-in models of the diode and MOS transistor were used with their parameters values taken from library EVAL.LIB for diode 1N4148 and transistor IRF150. For two considered converters R2 = 10 Ω and C= 470 μF were assumed. The voltage source V2 supplies the trapezoidal pulse run with the low and high levels of the transistor input voltage v_{GS} equal to 0 and 10 V, respectively; the period of this run is equal 10 μs (Fig. 2).

3.1 The buck converter

For the buck converter (Fig. 2a), the dependences $V_o(R_o)$ and $\eta(R_o)$ with the duty factor d = 0.5 and the input voltage V_i = -20 V, next the dependences $V_o(d)$ and $\eta(d)$ with R_o = 100 Ω and V_i = -20 V were computed, while the dependences $V_o(V_i)$ and $\eta(V_i)$ with d = 0.5 and R_o = 0.5 Ω, respectively. These all characteristics were calculated at three

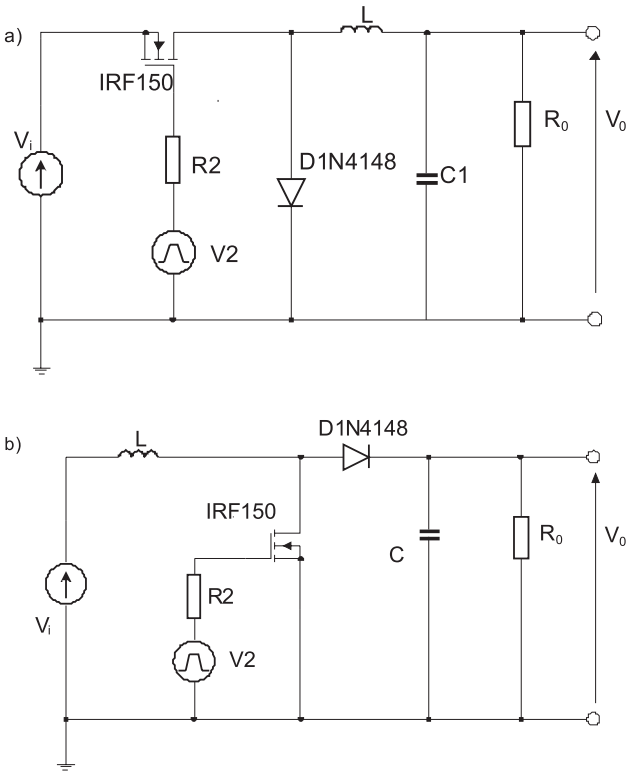

Fig. 2. The schemes of the buck (a), and boost (b) converters

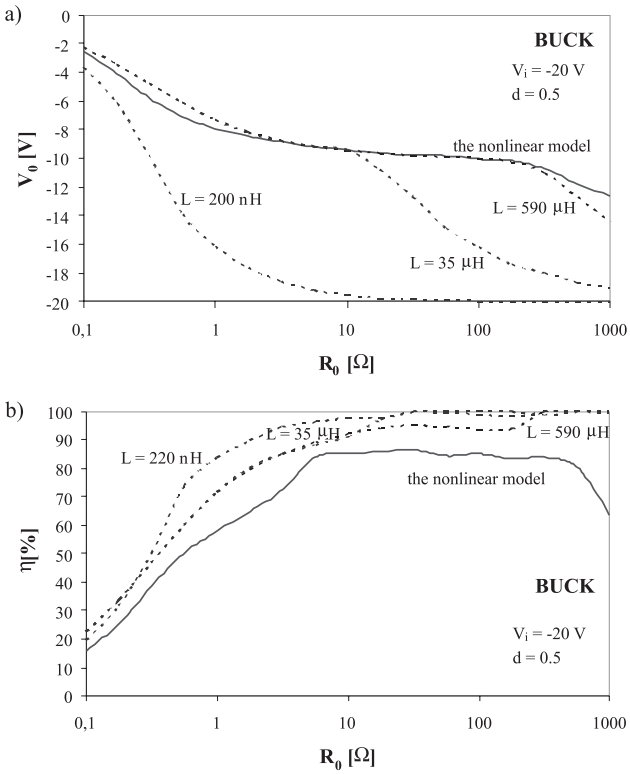

Fig. 3. The dependences of the output voltage (a), and the efficiency (b) on the load resistance for the buck converter

values of the linear inductance taken from the different current ranges of the dependence L(i) and with the nonlinear model of L(i) described in Sec. 2.

In Figs 3a, b the characteristics $V_o(R_o)$, and $\eta(R_o)$ are shown, respectively. As seen from Fig. 3a, at low load resistances (high currents), when the core saturates, the dependences $V_o(R_o)$ do not differ considerably for the nonlinear model, the linear model with at L = 590 µH and at L = 35 µH, while at high resistances (low currents), without core saturation, only the results obtained on the nonlinear model of L(i) and on the linear model at L = 590 µH are similar to each other. In the whole resistance range the characteristic with L = 0.2 µH differs from other characteristics considerably.

As it results from computations (Fig. 3a), the converter operates in the current continuous mode (CCM) at R_0 < 200 Ω as the nonlinear model L(i) was used, while on the linear model the lower values of this resistance are obtained: R_0 = 10 Ω at L = 35 µH and R_o = 0.2 Ω at L = 0.2 µH, what, in turn, leads to high differences in the computed values of the output voltage obtained on the considered models in the discontinuous current mode (DCM) especially.

From Fig. 3b it results that the computed efficiency η obtained on the nonlinear model of L(i) is lower than η resulting from the linear model in the whole range of the assumed values of R_o. These divergences result from the energy losses in the core taken into account in the nonlin-

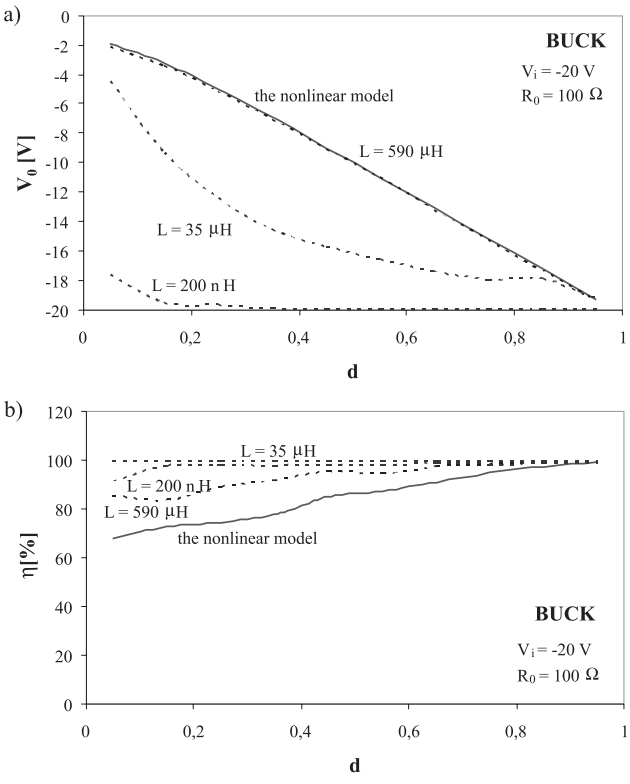

Fig. 4. The dependence of the output voltage (a), and the efficiency (b) on the duty factor for the buck converter

ear model. With the decreasing inductance the efficiency increases.

In Figs 4a, b the characteristics $V_o(d)$ and $\eta(d)$ are shown, and as seen from Figs 4a the essential difference is observed between the dependence $V_o(d)$ with L = 200 nH and L = 35 µH in relation to other curves. As stated before, at R_o = 100 Ω the core does not saturate.

From Fig. 4b it results that, as before, the computed efficiency η obtained on the nonlinear model is lower than η resulting from linear model in the whole range of the assumed duty factor d practically, what is caused by the energy losses taken into account in the nonlinear model.

In Figs 5a, b the characteristics $V_o(V_i)$ and $\eta(V_i)$ are shown with R_o = 0.5 Ω and d = 0.5 assumed. In this case these characteristics computed with L = 35 µH and L = 590 µH are practically identical. The voltage transfer characteristic with L = 200 nH (Fig. 5a) differs from the curves with other values of the inductance considerably. The efficiency η (Fig.5b) obtained on the nonlinear model is lower about 20% than η obtained on the linear model.

The dependence of the ripples of the output voltage on the load resistance $V_{pp}(R_o)$ is shown in Fig. 6. As it could be expected /1/, the ripples decrease with the increase of the inductance. The highest ripples are at low values of R_o – for the nonlinear model they amount above 100 mV, and at L = 590 µH they amount about 100 µV.

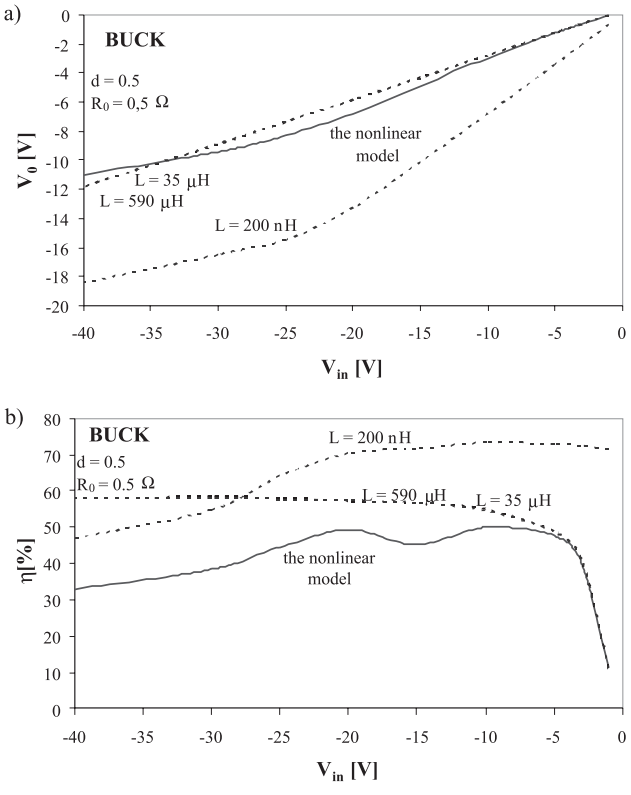

Fig. 5. The dependence of the output voltage (a), and the efficiency (b) on the input voltage for the buck converter

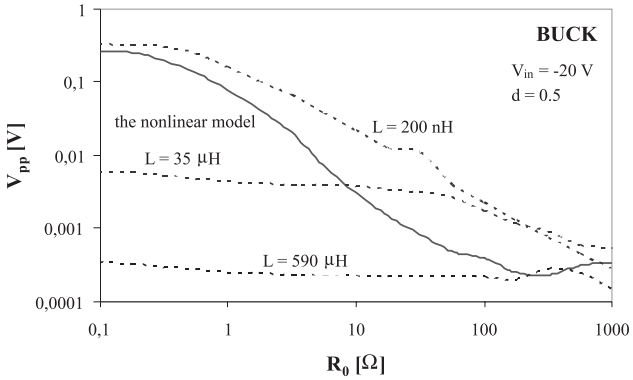

Fig. 6. The dependence of the ripples of the output voltage on the load resistance for the buck converter

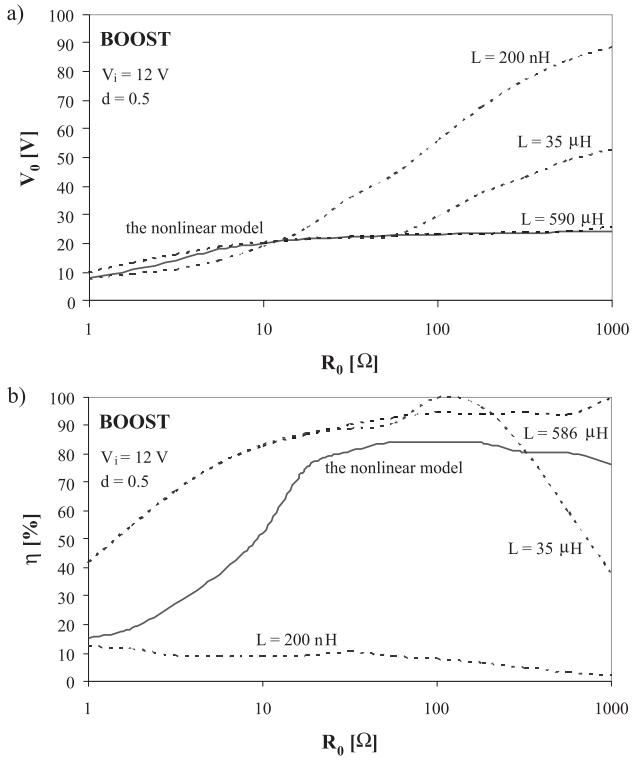

Fig. 7. The dependences of the output voltage (a), and the efficiency (b) on the load resistance for the boost converter

3.2 The boost converter

For the boost converter (Fig. 2b) the characteristics $V_o(R_o)$ and $\eta(R_o)$ were computed with d = 0.5 and V_i = 12 V, next $V_o(d)$ and $\eta(d)$ with R_o = 3 Ω and V_i = 12 V, and $V_o(V_i)$ and $\eta(V_i)$ with d = 0.5 and R_o = 3 Ω.

In Figs 7a, b the characteristics $V_o(R_o)$ and $\eta(R_o)$ are shown. As seen from Fig. 7a, the noticeable differences between the curves for all inductances assumed are at higher values of the load resistance, when the core does not saturate. At L = 590 µH and at the nonlinear model of the inductance the converter operates in CCM in the whole considered range of the load resistance. At the lower induct-

ances this mode is limited to R_o = 70 Ω (at L = 35 µH) and R_o = 10 Ω (at L = 0.2 µH).

The dependences η(R_o) (Fig.7b) obtained at four inductances differ from each other considerably, at higher values of the load resistance especially, and the highest differences – even 80%, are visible at L = 200 nH with respect to other curves.

In Figs 8a, b the characteristics V_o(d) and η(d) are shown. As seen form Fig. 8a the differences between the obtained dependences V_o(d) for the nonlinear model L(i) and at L = 0.2 µH are similar, while at L = 35 µH and at L = 590 µH the values of V_o are about 100 % higher than those for the nonlinear model.

From Fig. 8b it results that the dependences η(d) obtained on the linear model of L differ from the dependence obtained on the nonlinear model considerably. For all considered inductor models the efficiency decrease with increasing duty factor.

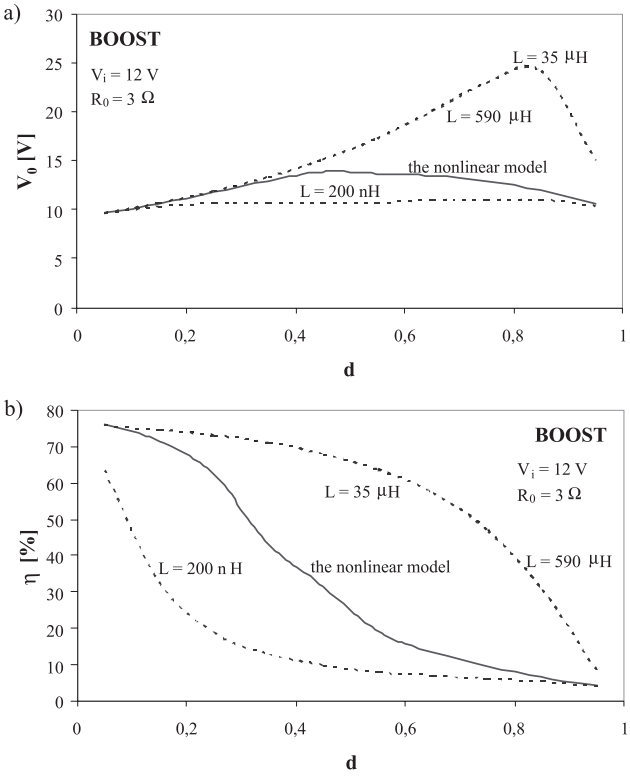

Fig. 8. The dependence of the output voltage (a), and the efficiency (b) on the duty factor for the boost converter

In Figs 9a, b the dependences V_o(V_i) and η(V_i) are shown. As seen from Fig. 9a, at low values of V_i there are no essential differences between the curves with the considered values of L, while at higher values of the input voltage they become visible.

As seen from Fig. 9b, the lowest values of the efficiency η are at L = 200 µH - they amount about 10% only. For the nonlinear model the dependence η(V_i) has the maximum at V_i = 4 V.

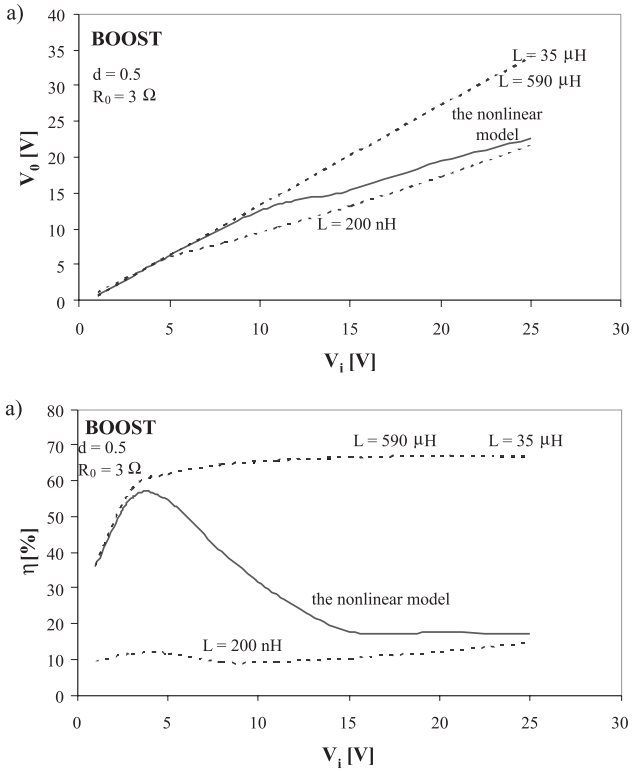

Fig. 9. The dependence of the output voltage (a), and the efficiency (b) on the input voltage of the boost converter

For the boost converter the dependence of the ripples of the output voltage on the load resistance V_{pp}(R_o) is shown in Fig. 10. The ripples decrease with increasing the load resistance, and the increase of the inductance causes decreasing the ripples as well.

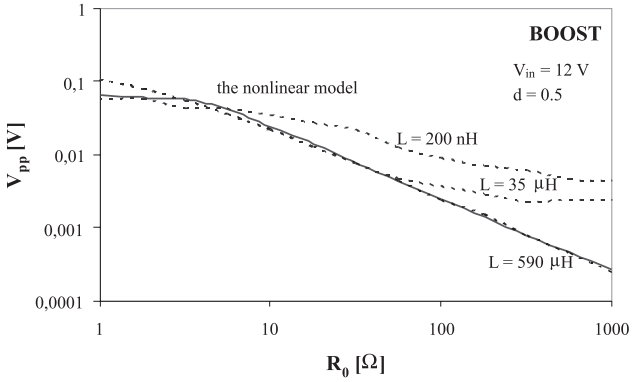

Fig. 10. The dependence of the ripples of the output voltage on the load resistance for the boost converter

4. Conclusions

In this paper the influence of the inductor model form on the selected characteristics of the buck and boost converters are discussed. The computations results are given for two models of inductance: the nonlinear JA model and

the linear one with the different values of L assumed. On these results one can estimate if the nonlinear model of the inductance is needed in the computer analysis of the converter to obtain reliable results. To this end the inductor current range should be evaluated in the first place.

If the core operates without saturation, then the divergences between the computations of the output voltage on the nonlinear model of L and on the linear one with the value of the inductance taken from the low current range are not essential. As the energy losses in the core are included in the nonlinear model of L, then the efficiency obtained on this model is typical lower than on the linear model, and the differences between these computations results of ç can even amount some tens of percents.

It is worth-mentioning to compare the computation times of the characteristics presented in Sec. 3. Owing to the use of the linear model of the inductor the time needed to analyse any converter circuit is shortened up to 50%.

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A NEW APPROACH TO OPTIMIZATION OF TEST PATTERN GENERATOR STRUCTURE

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Key words: test pattern generator, design, optimization, genetic algorithm.

Abstract: This paper presents a new approach to design and structure optimization of a deterministic test pattern generator (TPG). The TPG is composed of a linear register and a non-linear combinational function that can invert any bit in the generated patterns. Consequently, any arbitrary test sequence can be produced. Such a TPG is suitable for on-line built-in self-test (BIST) implementations where functional units are tested in their idle cycles. To reduce the gate count of the BIST structure a genetic algorithm (GA) is employed. This approach and its multi-objective nature allows concurrent optimization of multiple parameters within multiple design aspects (register cells type, patterns order in the generated test sequence, bit order of a test pattern), which influence the final solution. Experimental results on combinational ISCAS benchmarks demonstrate the efficiency of the proposed evolutionary approach.

Nov pristop k optimiranju strukture generatorja testnih vzorcev

Kjučne besede: generator testni vzorcev, načrtovanje, optimiranje, genetski algoritem.

Izvleček: V članku je predstavljen nov pristop k načrtovanju in optimiranju strukture generatorja testnih vzorcev (TPG). TPG je sestavljen iz linearnega registra in nelinearne kombinacijske funkcije, ki lahko invertira katerikoli bit generiranega vzorca. Tako lahko dobimo poljubno testno sekvenco. Takšen TPG je primeren za on-line built-in self-test (BIST) izvedbe, kjer se funkcijske enote testirajo v njihovih prostih ciklih. Za zmanjšanje števila logičnih vrat strukture BIST, je uporabljen genetski algoritem (GA). Večkriterijska narava tega pristopa omogoča sočasno optimiranje več parametrov na več načrtovalnih nivojih (tip pomnilnih registrov, vrstni red vzorcev, vrstni red bitov v vzorcih), kar vse vpliva na končno rešitev. Rezultati testiranja s kombinacijskimi testnimi vezji ISCAS so pokazali uspešnost uporabljenega pristopa.

1 Introduction

The complexity of modern integrated circuits and rapid changes in technology pose an ever-increasing number of challenges in testing electronic products. With the introduction of surface mounted devices, small pitch packaging becomes prevalent, which makes the access to the test points on a board either impossible or at least very costly. Traditional in-circuit test techniques that utilize a bed-of-nails to make contact to individual leads on a printed circuit board have become inadequate. To cope with this problem, boundary-scan approach has been developed and is now widely adopted in practice /3//25/. Another problem originates from the fact that the number of transistors in a chip increases faster than the pin count and consequently internal chip modules become more and more difficult to access. Limited number of I/O pins represents a bottleneck in testing of complex embedded cores where transfers of large amounts of test patterns and test results between the automatic test equipment (ATE) and the unit-under-test (UUT) are required, /4/. One of the alternative solutions is to implement a built-in self-test (BIST) of the UUT, /28/, with on-chip test pattern generation (TPG) and on-chip output response analysis logic. In this way, the test circuitry is incorporated on-chip and communication with external ATE is reduced to test initiation and transfer of test results /22/. Besides, self-test can be performed at the circuit's normal clock rate. This may increase the coverage of faults that could otherwise be detected only during normal system operation. In addition, BIST can be used for periodic testing and/or to diagnose system failures in system maintenance. On the other hand, BIST implementation inevitably leads to area overhead, which typically results in performance penalties due to longer signal routing paths resulting from the inclusion of the BIST circuitry in the design. Minimization of the BIST logic is one of the commonly addressed problems in practice.

Different TPG approaches have been proposed. They can be classified as ROM-based deterministic, algorithmic, exhaustive and pseudo-random. In the first approach, deterministic patterns are stored in a ROM and a counter is used for their addressing, /10/. This simple approach is limited to small test pattern sets. Algorithmic TPG are mostly used for testing regular structures such as RAMs /30/. Exhaustive TPG is counter-based approach which suffers from the fact that it is not able to generate specific sequence of test vectors. With some modifications, however, counter-based solutions are able to generate deterministic test patterns, /5//16//18/. Pseudo-random TPG is most commonly applied technique in practice. In this approach Linear Feedback Shift Register (LFSR) or Cellular Automata (CA) are employed to generate pseudo-random test patterns. In order to decrease the complexity of a TPG, de-

signers usually try to embed deterministic test patterns into the vector sequence generated by some linear register. Such embedding can be done either by re-seeding a TPG or modifying its feedback function /17/. There are also solutions that modify or transform the vector sequence produced by a LFSR in such a way that it contains deterministic test patterns /29//2/. Most proposed LFSR structures are based on D-type flip-flops. In recent years, LFSR composed of D-type and T-type flip-flops is gaining popularity due to its low area overhead and high operating speed /13//14/.

In the paper an approach for the generation of deterministic TPG logic based on a Linear Feedback Shift Register (LFSR) composed of D-type and T-type flip-flops is described. The use of LFSR for TPG eliminates the need of a ROM for storing the seeds since the LFSR itself jumps from a state to the next required state (seed) by inverting the logic value of some of the bits of its next state. The approach for constructing the proper LFSR employs a genetic algorithm (GA) to find an acceptable practical solution in a large space of possible LFSR implementations. In the area of TPG, genetic algorithms have mainly been used for the derivation of test pattern sets for target UUTs /8//26/. As for the synthesis of the TPG logic for actual generation of the derived test patters, GA approach has been used for the solutions based on cellular automata /9/.

This work was motivated by the need of deterministic test pattern generation for the on line BIST of structure composed of idle function units and registers, originally proposed in /27/. In this approach, functional units and registers that are not used for the computations of the target application during individual time slots are organized into a structure that is continuously tested in parallel with normal system operation. Normally, pseudo-random test vectors can be employed for such on-line self-test. In critical applications, where low fault latency is required, test pattern generators (TPG) that generate deterministic test sequence are needed. Deterministic test sequences (i.e., in which non-useful test vectors are eliminated) may also considerably reduce diagnosis time in fault localization /19/.

2 Test pattern generator structure

A TPG can be regarded as an autonomous finite-state machine that is typically configured as a shift register with additional feedback connections. A TPG is said to be linear if its feedback logic is composed exclusively of XOR gates, otherwise it is said to be non-linear. A TPG is initialized to a known initial state, and the contents of its flip-flops in the initial state are called the seed. The flip-flops are clocked to cause the transitions, whose exact nature depends on the feedback connections. The values of the state variables in subsequent transitions are used as test patterns. Most reported TPGs are D flip-flop based linear feedback shift registers (LFSRs).

In a typical scenario, a TPG is initialized with a given deterministic seed and run until the desired fault coverage is achieved. The test application time using an LFSR is significantly larger than what is required for applying the test set generated using a deterministic TPG. This is due to the fact that vector set generated by a LFSR includes besides useful vectors also many other vectors that do not contribute to the fault coverage. In order to reduce test application time, current non-useful vectors should be replaced by useful vectors appearing later in the test sequence. This can be done in a number of ways. Most commonly used techniques are reseeding and weighted-random pattern generation.

In our approach, the goal is to develop a TPG that would generate only the required test vectors (i.e., with no intermittent non-useful vectors). The overall structure of the proposed *n* bit test pattern generator is presented in Fig. 1. It is composed of a Multiple-Input Signature Register (MISR) and a modification logic. The MISR has a form of a ring that is composed of *n* flip-flops with either active high or active low inputs. Any flip-flop of the MISR can be of T type or D type. Each flip-flop (D or T) can also have inverter on their input (denoted as $\overline{D}$ or $\overline{T}$). Thus, the register may have one of *4n* different structures. The inputs of the MISR are controlled by the modification logic. The outputs of the MISR are fed back to the modification logic which is a simple combinational logic and acts like a decoder.

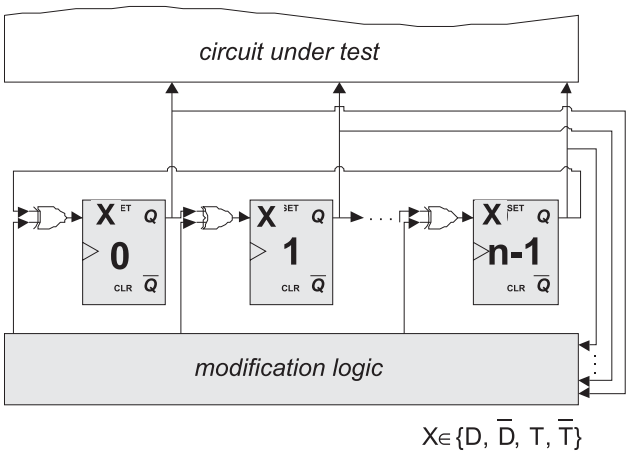

Fig. 1: Test pattern generator structure

In our case, MISR and the modification logic are application specific: they are synthesized according to the required test pattern set. The modification logic allows that in the subsequent clock cycles the contents of the MISR assume the values specified by the target test pattern set.

One of the parameters that are important for practical implementations of TPGs is area overhead. It is influenced by the structure of each MISR stage, the order of the test patterns in a test sequence and the bit-order of the test patterns. While the first property influences the complexity of both the MISR and the modification logic, the remaining two impact only the area of the modification logic.

3 Genetic algorithm

The population-based evolutionary approach - employed through GA /1//7//15/ was used for optimization because of its intrinsic parallelism that allows searching within a broad database of solutions in the search space simultaneously, climbing many peaks in parallel. Therefore, the risk of converging to a local optimum is low. Besides, promising results of our research work obtained in other optimization problem areas /20//21//23//24/ encouraged us to consider GA approach as one of the possible alternatives in TPG synthesis optimization.

The implementation of genetic operators is described with more details in /24/.

4 Structure evaluation

Operation of the *j*-th cell of the TPG register during one clock cycle can be expressed by the following equation:

$$Q_j = t_j\, q_j \oplus q_{j-1} \oplus i_j \oplus f_j$$
$$Q_1 = t_1\, q_1 \oplus q_n \oplus i_1 \oplus f_1 \qquad (1)$$

where q_{j-1} is the current state of the cell number $j-1$, q_j is the current state of the j-th cell, Q_j is the next state of the j-th cell, t_j is the coefficient determining type of the flip-flop in the j-th cell , i.e., 0 for D-type flip-flop, and 1 for T-type flip-flop, i_j is the coefficient determining whether there is an inverter at the input of the flip-flop in the j-th cell , i.e., 0 for absence of inverter, and 1 for presence of inverter, and f_j is the value of the j-th output of the modification logic. Thus, the value of the j-th output of the modification logic is:

$$f_j = t_j\, q_j \oplus q_{j-1} \oplus i_j \oplus Q_j$$
$$f_1 = t_1\, q_1 \oplus q_n \oplus i_1 \oplus Q_1 \qquad (2)$$

On the basis of these equations one can derive values of the outputs of the modification logic for each vector but last in the test sequence. In that way ON-set and OFF-set of the modification logic are defined.

Further, Espresso software /11/ was used for Boolean minimization of the modification logic and its approximate cost evaluation. This software takes a two-level representation of a two-valued (or multiple-valued) Boolean function as input, and produces a minimal equivalent representation (number of equivalent gates). It automatically verifies that the minimized function is equivalent to the original function. The algorithms used represent an advance in both speed and optimality of solution in heuristic Boolean minimization.

5 Results

The optimization process is shown in Figure 2, where the initialization phase determines the initial TPG structure through the desired sequence of test patterns. The GA tries to optimize the circuit (make new configuration) while checking the allowed TPG structure and using the external structure evaluation tool. The evaluation tool calculates the cost of a given structure through the input test patterns and TPG configuration. After a number of iterations the best structure is chosen and implemented through the hardware description language. Parameters of the GA used in our experiments are; a) for first three circuits: number of generations is 50, population size is 10, probability of crossover is 0.8, and probability of mutation is 0.01, and b) for the next three circuits: number of generations is 100, population size is 50, probability of crossover is 0.7, and probability of mutation is 0.05. The final solution for each circuit was the best one found after a few repetitions of optimization. There were few repetitions due to the non-deterministic nature of the genetic algorithm.

In Table 1 the results of the evaluation of the optimization process with the ISCAS test-benchmark combinational circuits are presented. The widely accepted ISCAS benchmark suite has been in use since being introduced in simple netlist format at the International Symposium of Circuits and Systems in 1985. In 1989 ISCAS symposium a set of sequential circuits was introduced, similar to the 1985 circuits, but with the addition of a D-type flip-flop element. These simple combinatorial circuits are used to benchmark various test pattern generation systems.

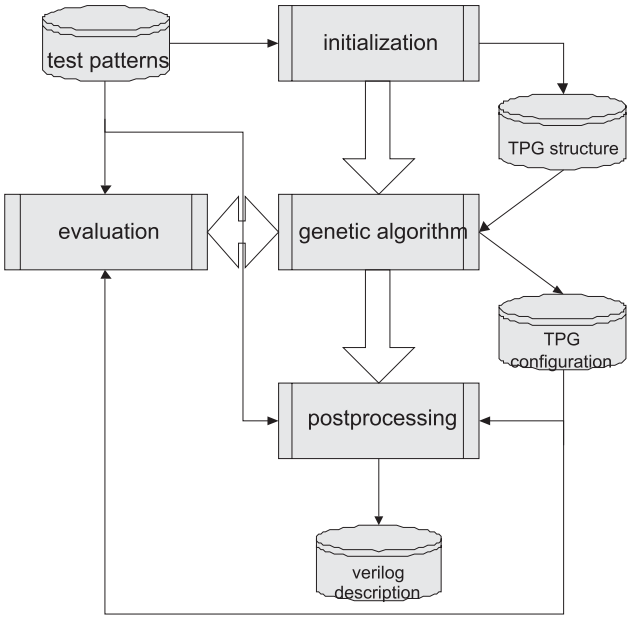

Fig. 2: The optimization process

All test circuits used in our evaluation were transformed by the input reduction procedure proposed in /6/. The test pattern width (denotes the number of the inputs) and the number of test patterns (number of different input test vectors to cover all possible faults) are presented in the second and the third column, respectively, for each benchmark. The next two columns present the total cost (number of equivalent gates) of the modification logic reported by Espresso for the initial and optimized TPG structure. The last column shows the achieved improvement between in-

itial and optimized structure. The execution time of the GA algorithm itself was always below a second, while the evaluation phase, performed by the external structure evaluation tool, took couple of seconds per evaluation. There is no report on total execution time, which in fact was measured in minutes, but since this is off-line optimization procedure, optimization effectiveness was considered more important as optimization time.

Table 1. Results of modification logic size (in total cost)

	test pattern width	number of test patterns	initial TPG	optimized TPG	improvement in %
c432	36	27	348	280	19.5
c499	41	52	312	164	47.4
c880	60	16	536	402	25.0
c1355	41	84	584	488	16.4
c1908	33	106	2077	1840	11.4
c6288	11	12	74	49	33.8

Since the bit-order of the test patterns and the order of the test patterns in a test sequence influence the area of the modification logic, it might be interesting to compare the results also with the results of column matching algorithm /12/. Both approaches use MISR of similar complexity, while the main differences are in the design of the modification logic. Table 2 shows the results of the comparison of the two approaches for the same benchmark circuits. The complexity figures in the 2nd and 3rd columns of Table 2 are expressed in terms of a total cost reported by Espresso per bit of the produced test pattern:

$$complexity = \frac{total\_cost}{test\_pattern\_width * number\_of\_test\_patterns} \quad (3)$$

Such a measure was applied because in experiments different test pattern sets were used than those reported in /12/.

Table 2. Comparison with results achieved in /12/

	complexity of TPG obtained by column matching	complexity of the proposed TPG obtimized by GA approach
c432	0.33	0.29
c499	0.13	0.08
c880	0.38	0.35
c1355	0.19	0.14
c1908	0.29	0.53
c6288	-	0.44

The comparison presented in Table 2 indicates that the proposed approach has a higher potential to provide solutions of TPG generating deterministic test patterns than column matching. Another big difference is also in testing time; in column matching solution all deterministic test patterns are embedded in a long test sequence composed of 5000 test vectors, which contains a lot of patterns not contributing to the fault coverage in the CUT. On the other hand, the GA based solution produces all deterministic test patterns as a one short test sequence that does not contain any superfluous vectors.

In Table 3 the comparison of the area of TPG logic for AMS 0.35 µm technology for the implementations reported in /2/ and the GA based solutions is presented. The area is expressed in terms of equivalent two input NAND gates. As in Table 2, a specific measure of the area overhead of the TPGs was applied due to the fact that different deterministic patterns sets have been used for TPG synthesis. The proposed measure is expressed by the following formula:

$$area\_per\_bit = \frac{area}{test\_pattern\_width * number\_of\_test\_patterns} \quad (4)$$

Table 3. Comparison with results achieved in /2/

	area_per_bit of the TPG in [2]	area_per_bit of the proposed TPG obtimized by GA approach
c432	0.22	0.11
c499	0.21	0.10
c880	0.19	0.29
c1355	0.20	0.09
c1908	0.19	0.32
c6288	0.24	0.54

Experimental results in Table 3 indicate that for some benchmarks the proposed TPG and the GA optimization procedure provide solutions with lower area overhead than the TPG presented in /2/ while for some other benchmarks the TPG in /2/ are better. This may be due to the fact that we used Espresso as a fast evaluation tool in the TPG optimization process and Synopsys as a tool for synthesizing the final solution. Therefore, applying Synopsys as both the evaluation tool and the final synthesis tool is likely to improve the results.

The above examples are good for illustrating the advantages of the proposed approach in comparison with the existing solutions. However, one should be aware that the employed benchmark circuits are relatively small. Realistic assessment of techniques for automatic deterministic test pattern generation requires more complex circuits. Since such examples are not reported in the referred papers, we performed GA optimization approach on some larger benchmark circuits. While the results regarding the complexity and the area per bit are in average comparable to the GA examples reported above, the computation time for larger circuits considerably increases and may represent a bottleneck in practical implementations. For example, the computation time for circuit s38417 was 140 times larger than for c880.

6 Conclusion

In many cases, pseudo random pattern generators provide reasonable fault coverage for different circuits-under-test. However, if a TPG fails to provide the desired fault coverage within the given test length, application specific deterministic TPGs are employed. Deterministic TPGs are by default more complex since they employ additional logic to prevent the generation of non-useful test patterns.

Area overhead is one of the important issues of the design of deterministic TPGs. In this paper, a new type of deterministic TPG is presented based on a feedback shift register composed of D- and T-type flip-flops and inverters. It is also equipped with a modification logic that can invert any bit in any pattern generated by the register. The search for the optimal structure of the TPG is performed by a genetic algorithm and some illustrative case studies were performed on ISCAS test-benchmark circuits. Promising initial results have been obtained on small and medium benchmark circuits. The computation time for larger circuits considerably increases and may represent a bottleneck in practical implementations.

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TWO OPTICAL RING COMMUNICATION BETWEEN POWER ELECTRONIC BUILDING BLOCKS: A CASE STUDY

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Key words: communication, power electronic building block, control

Abstract: Power electronic building blocks initiated and sponsored by the Office of Naval Research, are based on the integration of power semiconductor elements with some degree of intelligence and data communication capability in compact form.

This article addresses the communication issues of power electronic building blocks. After brief overview of common used topologies in power electronic building blocks there is an analysis of requirements of communication between power electronic building block and detailed description of case of the two-optical ring communication topology with schemas for of complete implementation of slave nodes in a single FPGA circuit.

Komunikacija dvojnega optičnega obroča med gradniki močnostne elektronike: študija primera

Kjučne besede: Komunikacije, gradniki močnostne elektronike, vodenje

Izvleček: Gradniki močnostne elektronike, ki jih je vpeljala in sponzorirala ameriška vojna mornarica (Naval Research Office) temeljijo na integraciji močnostnih polprevodnikov z določeno stopnjo inteligence in sposobnostjo prenosa podatkov v kompaktni obliki.

Članek se osredotoča na komunikacijo med gradniki močnostne elektronike . Po kratkem pregledu najbolj pogosto uporabljenih topologij v gradnikih močnostne elektronike naredimo analizo komunikacijskih zahtev med gradniki močnostne elektronike. Nadaljujemo z detajlnim opisom primera topologije dvojnega optičnega obroča in podamo sheme za implementacijo enot tipa suženj v FPGA vezju.

1. Introduction

Recently the development of the electric power supply systems as well as power supply equipment are directed toward miniaturization (doable with new semiconductor materials and use higher switching frequencies) and distribution/integration of supply sources with their loads enabling optimization of their joint features or achieve other desirable features as reliability, survivability, low cost production etc.

This new design paradigm, the first time clearly exposed by of the Office of Naval Research initiation for development of power electronic building block (PEBB), anticipate that each PEBB will have standardized input/output connections, some smartness enabling safe control, state observation with power electronics hardware managing, and software determination of their function/behavior. Further, introduction of digital communication ability between PEBBs and master or distributed control system open new bunch of operabilities for new developments, research and sophisticated solutions yet not imaginable /1/, /2/, /3/, /4/, /5/.

1.1 The most common PEBB topologies

Basic switching element in PEBB is half power switching bridge usually schematically presented independently of used switch technology by symbol for switch (Fig. 1). The PEBB also can be consisted from main power half bridge switch and auxiliary half bridge for so call zero-voltage or zero-current switches.

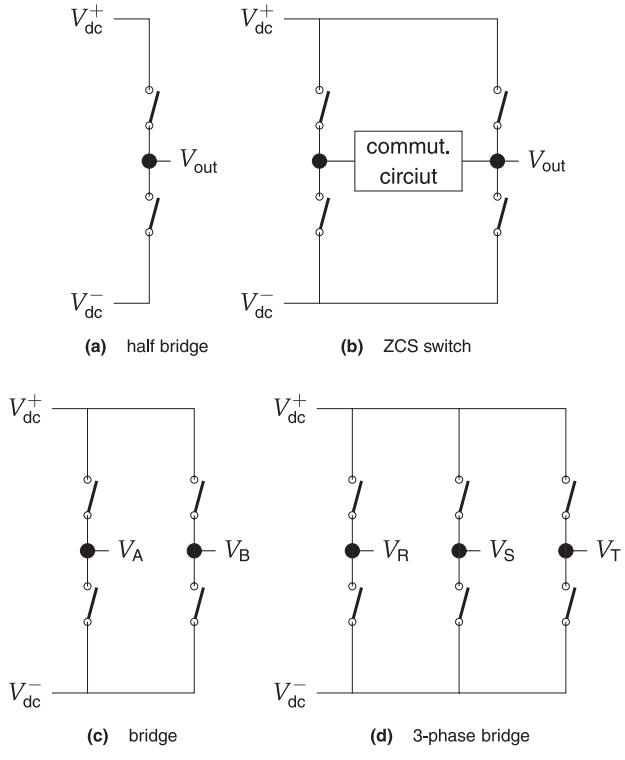

Fig. 1: The most common topologies of switches in PEBB

1.2 Universal PEBB Controller

Replacing control signals with digital communications lead to use of digital controller. This now can be universal and can be easily adapted to application with adequate algorithm software /1/, /3/, /4/.

The switching frequencies of today's medium power converters already cross a switching frequency of over 100 kHz and the recent development of fast semiconductor switches and converters' topologies shows that, in the near future medium power PEBBs will cross at a class higher switching frequency, consequently the controller as well communications connecting them to power switches should be capable to perform their tasks in 10 μs sample intervals. To copy with this it is sensible to use cascade control structure and divide task on high speed inner control loop and lower speed outer loop (Fig. 2).

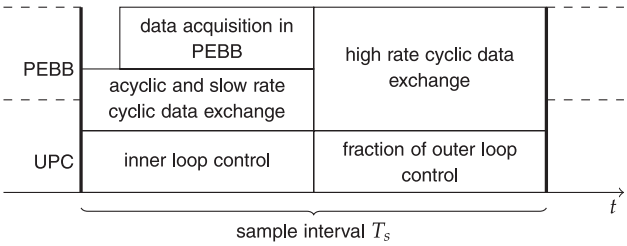

Fig. 2: Sample interval sharing between inner control algorithm, data acquisition and cyclical data communication. The outer control algorithm can be distributed over a number of cyclical data communication intervals.

Determining sample interval share for fast cyclic communication depends on the number of PEBB's linked by IPC, the kind of PEBB (for example direct controlled, PWM controlled) and a reasonable cost for communication hardware. Similarly, the duration of inner loop algorithm execution should be longer than data acquisition in PEBB.

1.3 Communication issues

The systems and equipment built-up with PEBBs, according to control and design strategy requires up to three levels of communication:

1. PEBB internal high speed serial communications connecting local Hardware Management Logic (HML) with PEBB components as analog-digital converters, timers, protection logic circuits etc,
2. fast local network linking PEBB's and central controllers, i.e. Inter-PEBB Communication (IPC), and
3. a local area network connecting equipment or systems based on PEBB to some central supervisor and monitoring system.

The major requirement for the first two communication levels is hard real-time /8/, /9/, /10/. This means that the data has to be correct in time, as well as in content. Any failure in both demands can lead to catastrophic events hazardous to devices, systems or even users. Therefore the requirements for IPC are:

1. deterministic,
2. immune to the disturbance, crosstalk, and interference as much as possible on the physical level already,
3. capable of allowing the diverse IPC traffic needed for normal PEBB functioning, support reconfiguration of PEBB, monitoring of PEBB states by boundary scan, etc,
4. capable to adopt to different control strategies of PEBB output voltage strategies (using pulse-width modulation or use of variable structure control approach with direct switch state control)
5. reliable, scalable, and survivable.

Analysis of enumerated requirements shows that the communication on one hand should be implemented in hardware and used optical fiber(s) for transmission media and on another hand to be adaptable to different control strategies and with this to be adaptable to different data formats.

2. A case study

The starting point of the case study was an existing IPC based on MACRO protocol /5/. From it the *master/slave* concept was preserved. The physical layer was enriched with the second optical ring with traffic direction opposite to the direction in the first ring (Fig. 3). Function of TAXI chips with the latter described extensions was implemented in FPGA (consequently achieved data rate on one ring due to speed limitation of used FPGA was reduced to 25 Mbit/s). New synchronizer was developed, as well as a function for topology reconfiguration. Besides this the new frame organization, forward error coding scheme, and the simplification of those protocols implemented in slave node, i.e. in a PEBB, were tested.

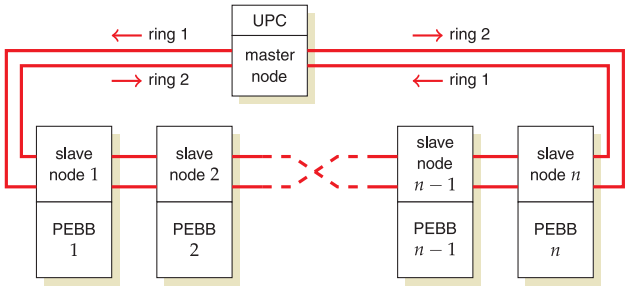

Fig. 3: IPC with two active optical ring topology.

Two optical rings topology gives opportunities as doubling the maximal number of PEBBs, or halving the sampling interval, and thus doubling the total switching frequency or halving the one ring IPC bit rate and not on the end gives very desirable reliability, scalability, and survivability. From the aforementioned possibilities, the following are consid-

ered in the case study:

- reconfiguration of two-ring topology in one sample interval,
- doubling the number of PEBBs in an IPC,
- locally performed synchronization, which is based on measurements of the frames' propagation times.

Besides the aforementioned, the structure of all frames was revised in comparison to known solutions /7/ for better utilizations of sampling intervals.

2.1 Frames

All frames have fixed length and are in the cyclic traffic send in convoys (Fig. 5). Data (i.e. information) frames (Fig. 4a), in short I-frames, contain two 16-bit long slots, which enables UPC to send two words of switch on/off occurrence data and, at the same time, to collect the same amount of fast changing measured data in PEBB. Two slots follow FEC which contain Bose-Chodhuri-Hasquenghen parity code generated by generator polynomial $x8+x2+x+1$, the same as used in ATM /6/. Parity bit gives enough redundancy for correction 1-bit error and discovering any 2-bit error and 8-bit burst error. The second slot also contains the address of PEBB, which is superimposed on the data. This additional PEBB address serves many purposes, as described later.

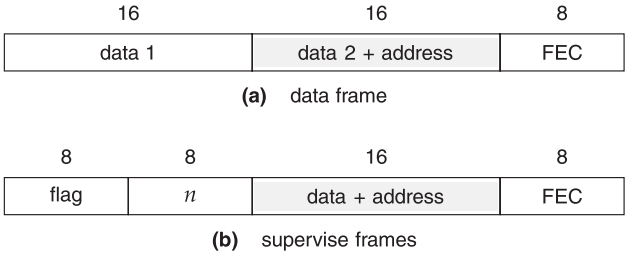

Fig. 4: Formats of frames (before 4B/5B encoding).

Supervise frames (Fig. 4b), in short S-frames, have the same size as I-frames. Instead of the first data slot they have an 8-bit long flag with repeated 4-bit code with a type of S-frame (Table I). The 8-bit field is followed by the number of I-frames.

Table I: S-frames.

from UPC to PEBB	from PEBB to UPC
Start of Convoy	Switching Error
Sample Instant Synchronization	Synchronization Mismatch
Master Reset	Broken Ring
Initialization	
Discover node	
Acknowledge	

During the cyclical data exchange, the data frames are sent in a convoys started with S-frame *Start of Convoy* as head and followed by I-frames in opposite order to PEBBs down the ring and with S-frame *Sample Instant Synchronization* as a trailer. The gap between the trailer and the end of sample interval is padded with padding bits (Fig. 5).

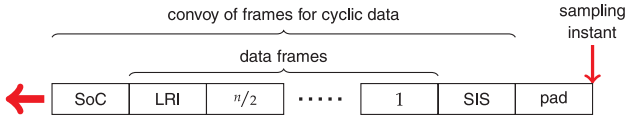

Fig. 5: Structure of convoy. SoC: S-frame Start of Convoy, LRI: low rate I-frame, SIS: Sample Instant Synchronization, pad: padding bits. The data frame numbers are equal to the position of slave nodes in the direction of the convoy propagation down the optical ring.

2.2 Transceiver circuit in the slave nodes

The core of IPC is transceiver circuit (Fig. 6). It is the same in slave and in the master nodes. Designed is FPGA and it enables wire speed detection of S-frames. Since the data frames travel in convoy with the SoC frame as header and the SIS frame as trailer, it is easy to determine those time slots in when ADM in particular PEBB's nodes copy data on the ring into the receiver shift register, and simultaneously, replace this data with their own. Slots are determined by the cyclical data frame counter and slot decoder, which is configured during the initialization phase using S-frame *Discover node*.

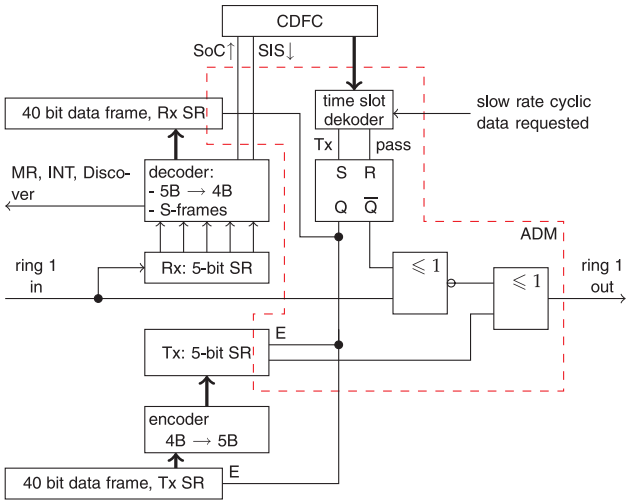

Fig. 6: Principle of innovative transceiver circuit in the first ring. CDFC: Cyclic Data Frame Counter, ADM: Add Drop-a-way Multiplexer.

2.3 Synchronization

The key problem in IPC is determining and maintaining sampling instants' synchronization in each PEBB. Synchronization is based on the measurement of time difference between SIS frame recognition instant in frame convoys which are simultaneously transmitted, each on its own ring. Since convoys propagate in opposite directions down the ring, both SIS frames pass each other close to midway. At this point the time difference between them is zero. At each other slave node this difference is twice the offset gap between the SIS frame recognition instant, and the sampling instant. This gap is padded with padding bits (Fig. 5).

Synchronization is performed by two counters, one buffer, a comparator, and two pre-scaler counters (Fig. 7). Counter 1 serves for determining the gap between the occurrence of synchronization frame detection and sampling instant, the second counter serves for measuring frame propagation time. It has a complex structure, because, for the sake of generality, it can determine half and full differences between both frames' convoys, and also supervise if a ring is broken. The measured difference is stored in a buffer since it is used for the next sampling interval. The buffer also stores data from this SIS frame, which determines ratio *VCO clock/bit rate* (×2,×4,×8,×16) and the ratio between the measured time difference of SIS frames, and the gap to sampling instant (can be 1:1 or 2:1).

Blocks "pad" and "pre-scaler" PS_2 serves for adjusting padding bits. When resetting PS_2 the first padding bit width is adjusted such that any jitter of sampling instants is minimized. The amount of jitter depends on the accuracy of the difference measurement, i.e. from ratio *VCO clock/bit rate*. If this ratio is 2:1, then the jitter is less than ± 0.*000*5 %, in the case of 16:1 it is improved to ±0.00006 %. Since only the length of the first padding bit in the sample interval can vary, this does not disturb the bit synchronization very much.

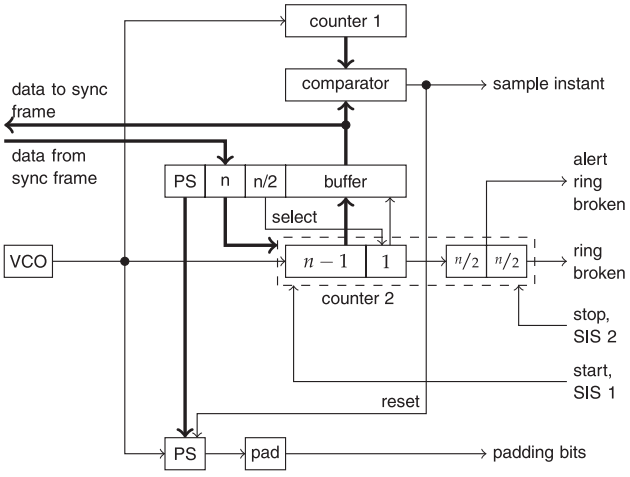

Fig. 7: Scheme of synchronizer. For meaning of label see text below.

3. Traffic

IPC traffic constitute:

- Connectionless cyclic data exchange, which in regular sample intervals deliver switching commands to the PEBB and collect data in acquired in them.
- Connectionless acyclic data with confirmation for irregular events and starting initialization.

Both traffic flows are in transmitter handled on the same way. In wire-speed the data ere exchanged between rings and PEBBs' nodes.

3.1 Acyclic traffic

Acyclic traffic is used on two occasions:

1. during the initialization phase,
2. When an irregular event in PEBB happens.

During the initialization phase, the traffic is initiated and controlled in a master/slave fashion by UPC. Among the S-frames used for initialization are *master reset*, *Initialization*, *Discover node*, *Acknowledge* and *Sample Instant Synchronization*.

When collecting irregular events, UPC, in the sample subinterval intended for acyclic traffic, successively sends empty frames *Switching Error* (SE) and *Synchronization Mismatch* (SM). These frames in the data field carry a set of 16 flags, each assigned to one PEBB. If the PEBB experiences this failure, PEBB's nodes set-up an assigned flag to it. If there are more than 16 PEBBs connected in one ring, they are segmented into groups of 16 PEBBs and the groups are assigned within the field *n*.

A broken ring is signaled by S-frame *Broken Ring* (BR) on the second ring, immediately after detecting ring breakdown. Apparently, the broken ring is detected successively in all nodes after failure (in the second ring direction) on the ring. For resolving possible collision and for detecting the place of failure, BR frames are sent successively as long as that slave nodes from the master node receive:

- ACK frame with instructions/confirmation for reconfiguration two-ring network into two one-ring networks, or
- MR frame with request to shutdown the PEBB (all switches go to the off-state)

A collision arises if the next node detects a broken ring before it detects the arrival of a BR frame from a node closer to failure. In this case the signal *alert rings broken* in nodes activate sending their BR frames, which is discontinued by detection of the incoming BR frame. With detection of an incoming BR frame, the flag *ring is broken before previous node*, is set. This flag after momentarily sending of BR frame heading prevents any further sending from this node (Fig. 8). Consequently, the master node rich least one complete BR frame header, which on its way to the master node set in the all passed slave nodes the flag *ring is broken before previous node*. This procedure clean-up the ring for the BR frame from node which is closest to the ring failure.

BR frame header, which on its way to the master node set in the all passed slave nodes the flag *ring is broken before previous node*. This procedure clean-up the ring for the BR frame from node which is closest to the ring failure.

Frames received without errors or with one error corrected by FEC, are acknowledged by the ACK frame in a packet of up to 16 data frames, following the initialization frame. Under normal circumstances the IPC is set-up during the design of PED/PES. For the sake of reliability at the fault

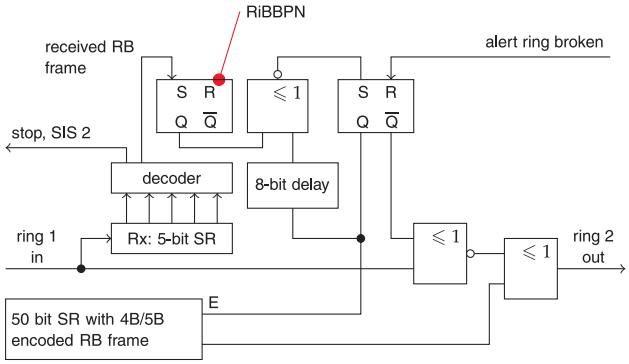

Fig. 8: Block scheme of transceiver circuit parts in the second ring involved in physical protocol "Broken Ring". RiBBPN: flag "Ring is Broken Before Previous Node", SR: Shift Register, E: enable.

tolerant design of PED/PES, the PEBB's nodes support reconfiguration, in the case of ring break as described in section 3-A, as well as the auto- configuration of IPC at the initialization of the communication system.

3.2 Initialization

Initialization has two parts:

1. initialization of PEBB
2. auto-configuration of communication system

Slave nodes executes initialization of equipment or system consist of PEBBs by delivering the received initialization data into the PEBB control registers, reading PEBBs' status registers, and supporting acknowledged connectionless services of the acyclic data transfer.

The main goal for the auto-configurations of PEBB's nodes is the determination of the nodes' serial order in the optical ring. This procedure has two steps. In the first step, the master node in the UPC sends S-frame "Discover node", which activates the automaton for setting-up the decoder for read or setting the flags in the S-frames (in accordance with a node place in the ring), in the second step the master node successively sends the logical addresses of the nodes by frame pairs 'Discover node" and I-frame. In the S-frame's data field node is assigned by its place in the ring, and in the followed data frame the data slots contain the nodes' logical addresses, determined by the master node.

4. Conclusions

IPC is very demanding at function execution times, consequently communication protocols have to be executed at so-called wire-speed at a bit rate of a least 100 Mbit/s. Therefore, all functions are simplified as much as possible and implemented by automaton, counters and registers like to physical protocols in ISO/OSI model. It can be easy implemented in FPGA.

Two-ring topology compensates for the double cost of transmission media and the necessary electro-optical couplers with high value benefits such as:

- enabling independent self synchronization in each node on IPC
- higher reliability and survivability of PED/PES

From the performed simulations in VHDL and the implemented parts of IPC, it can be concluded that, today, FPGA enables the building up of compact IPC slave nodes with integrated HML functions, in a single chip.

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ROBOTIZACIJA PROIZVODNJE – ROBOTSKO SESTAVLJANJE

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Kjučne besede: robotizacija, sezor Banner T18, prijemalo, model lesene hiške, tekoči trak, robotski krmilnik, vodenje po položaju in sili, robotsko pobiranje, robotsko sestavljanje.

Izvleček: V članku predstavljamo princip prepoznavanja, pobiranja, odlaganja in sestavljanja elementov lesene otroške hiške. Na kratko želimo predstaviti vzroke problematike robotskega sestavljanja in uporabljene rešitve, ki so pripomogle k rešitev problematike sestavljanja. Za lažjo predstavo smo izvedli primerjavo uporabljenih rešitev s tistimi, ki se v industriji uporabljajo kot profesionalne rešitve.

Robotization of manufacture yield – constructing with robot

Key words: robotization, sensor, grasper, wood house model, microcontroller, servofloat.

Abstract: Robotics is fast growing area, which achieves full bloom in last teen years. Now days, manipulators are indispensable part in industry. We use them for weld chassis, for steel and wood cultivation, for disperse coloring, steel cutting and so on. Since 1992, for each year, number of robots rapidly increases. Reason for that is their universality, but because of that property, people start initiates them into farms, agricultures, green houses, warehouses, into electronics production for composing electronic components… Today, robots using area expands wide around, specially to our homes.

Basically view, represent robot as movement machine or automatic machine with more free programmable axels, in some cases in combination with sensors or computer vision.

Our system consists with seven basic parts: the first one is operator and then follows programming device, microcontroller, robot hand, grasper, sensor and round movement ribbon. The main goal of this project is to incorporate all basic parts in to working process for composing elements of woody children house.

Second section in this article represents components, which are extremely important when we initiate robotization into industry. Here belong criteria, like choosing real and successful first application, choosing right robot, production speed, time requirements for implement equipment, and complexity of automation. In third section we made case study of hold comparison between human and robot, which is very important for understanding, how servofloat function work. Fig. 1 shows round movement riboon, with basic parts on taking away place. Servofloat function is described in session six. Fig. 3 represent barrier on trajectory between step 1 and step 2. With servofloat function can robot avoid this barrier and jump directly over shortest path to step 3. Chapter four give us some information about IR sensor, and basic work principle for light and dark places recognition. Table 1 shows possible combination, when we recognized parts of house, and Fig.2 shows basic principle of component recognition. Section five describes constructing algorithm procedure, where table 2 and their indicators illustrates course of construction phase. Chapters seven and eight are purposed for discussion about picking up elements from moving round ribbon and taking off the same elements on composing place. In this two sections we try to find answers on our problems, and solve them completely with suggest simple solutions. Fig. 4 under seven section illustrates left side element on round ribbon palette. Fig. 5 is placed in eight section, where illustrates decreasing tolerance between both big side elements. Under same section, Fig.6 illustrates cultivated bottom side of the smallest side element. Section 9 concludes the paper.

1 Uvod

Robotika se je v zadnjih desetletjih pojavila in utrdila v številnih industrijskih procesih v obliki moderne, ekonomične in človeku prijazne tehnologije. Robotski manipulatorji so nepogrešljivi del pri varjenju avtomobilskih ohišij, vstavljanju obdelovancev v stiskalnice, razpršilnem barvanju, služijo pa lahko tudi kot paletirni pripomoček oziroma kot manipulatorji za razrez, sestavljanje itd. Prav nobeno izjemo ne predstavljajo kirurški roboti ali servisni mobilni roboti, kateri so dandanes v veliko pomoč pri raznoraznih opravilih.

Cilj je usmerjen v postavitev in zagon proizvodne linije za sestavo lesenih hišk, kjer sestavni deli prihajajo na paletah, po tekočem traku, do mesta odjema, kjer se vrši prepoznava sestavnih delov s pomočjo infra-rdečega tipala. V navezi z logiko prepoznavanja se ustrezni element prenese na površino sestavljanja, v kolikor slednji ne ustreza zaporedju, se odpelje po traku naprej.

Osnovna tematika projekta temelji na prepoznavanju in prijemanju objektov, kjer igrajo pomembno vlogo tolerance. Sestavni gradniki hiše so oblikovani z obdelovalnimi stroji, ki imajo natančnost do enega milimetra, včasih celo več. Na drugi strani pa pri sestavljanju uporabljamo manipulator, ki je natančen do desetinke milimetra. To pomeni, da moramo najti most med dvema svetovoma z različnimi natančnostmi. Takšen most ponazarjajo predstavljene možne rešitve v tretjem poglavju, s katerimi lahko delno ali v celoti rešimo omenjeno problematiko. S tem smo želeli pokazati, na kakšen način lahko združimo povsem različna svetova, ob enem pa prejmemo rezultate, ki smo si jih na začetku le želeli. Razlog združevanja dveh povsem različnih svetov gre pripisati obstoječi opremi, ki je v laboratoriju na razpolago, s čimer lahko damo poudarek področjem, ki marsikateremu v začetku izvajanja podobnega projekta niso opazna.

Drugo poglavje je namenjeno predstavitvi najpomembnejših komponent, katere upoštevamo pri uvajanju robotizac-

ije. V četrtem poglavju predstavljamo študijo prijema pri človeku in stroju, v petem princip snovanja algoritma in v šestem način vodenja po položaju in sili. Sedmo in osmo poglavje ponazarjata metodologijo pobiranja in odlaganja elementov modela lesene hiške. Sklepi, spoznanja in zaključne misli, podane v devetem poglavju, zaključujejo raziskovalno delo.

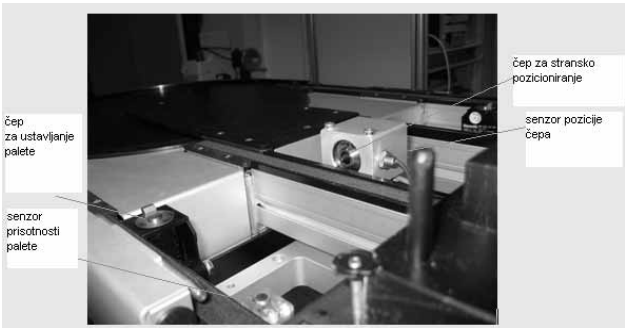
2 Komponente, ki vplivajo na uvajanje robotizacije

V primeru odločitve o robotizaciji posamezne delovne naloge, ali že obstoječega ročnega delovnega mesta, moramo biti pozorni na naslednje pomembne komponente:

- Izbira prave in uspešne prve aplikacije. Ne smemo izbrati prezahtevno nalogo, saj morda tehnično in kadrovsko ne bomo kos reševanju naloge. Izogibajmo se aplikacij, ki so zahtevne že same po sebi.
- Izbira in določitev robota (manipulatorja), ki bo najbolje zadostil našim zahtevam. Ko imamo enkrat določeno nalogo, moramo izbrati optimalni tip manipulatorja. Ne smemo pozabiti na zahtevano število prostostnih stopenj, obliko delovnega prostora, obliko in lastnosti nameščenega orodja ali prijemala, nosilnost (“bruto” teža).
- Kompleksnost avtomatizacije (enostavnejša kot je realizacija večji je zaslužek). Ne pozabimo na dejstvo, da preproste rešitve vodijo k lažjemu obvladovanju situacije in s tem posredno k manjšim stroškom zagona in vzdrževanja.
- Hitrost proizvodnje (roboti delajo načeloma počasneje kot človek, vendar bolj enakomerno). V praksi obstajajo različne metode za ocenjevanje potrebnega časa posameznih operacij. Pozorni moramo biti na ozka grla, ki nam kasneje omejujejo proizvodne sposobnosti.
- Eden izmed pomembnejših ciljev (ni potrebno, da je ravno glavni) je ekonomska upravičenost. Z robotizacijo seveda pričakujemo pozitivne učinke v smislu večje produktivnosti, manjšega izmeta, kvalitetnejših izdelkov itd.
- Časovno trajanje uvedbe (menjava proizvodnega programa). V fazi študije je potrebno predvideti, kolikšna bo delovna doba delovanja. To obdobje igra ključno vlogo pri amortizacijo vloženih sredstev.
- Prva namestitev (izkaže se, da je najboljši strokovnjak najcenejši). Brez ustreznega kadra se je težko lotiti takšnega projekta. Tudi če kupimo robotsko celico od dobavitelja na ključ, bomo potrebovali domači tehnični kader za vzdrževanje in odpravo napak. Robot, ki ne opravlja svoje funkcije, je nekoristen.
- (Ne)naklonjenost okolja (ljudje se pritožujejo in sabotirajo robote). Posebej v okoljih, kjer niso vajeni delati skupaj z roboti, lahko pride do pritožb in strahu pred njimi. Pomembno je, da pri uvajanju robotov ne zanemarimo ta psihološki vidik.

3 Prijem pri človeku in stroju

Ker se pri robotizaciji v veliki meri ukavarjamo z prijemi, Vam želimo v okviru tega poglavja predstaviti študijo prijema. Študija prijemanja z roko pri človeku, in neposredna primerjava z robotskimi prijemali je pomembna na številnih področjih. Tipičen primer je rehabilitacija roke, kjer nas zanima ocenjevanje funkcionalnosti le-te, ter povrnitev gibov ohromele roke. Ključno področje predstavlja interakcija človeka z računalnikom, kjer se uporabljajo namenski uporabniški vmesniki (haptične naprave) za delo v navideznem okolju. V industrijskem okolju se srečujemo z robotskimi mehanizmi, ki za prijemanje predmetov uporabljajo različna robotska prijemala. Slednja so lahko enostavna dvoprstna, katero tudi sami uporabljamo, pa vse tja do spretnejših in kompleksnejših več-prstnih prijemal.



Slika 1. Krožni tekoči trak s pozicionirnim čepom, čepom za ustavljanje palet in senzorjem prisotnosti palete na odjemalnem mestu

Fig. 1. Round movement ribbon with position bung, presence sensor and blockade for stopping paletts

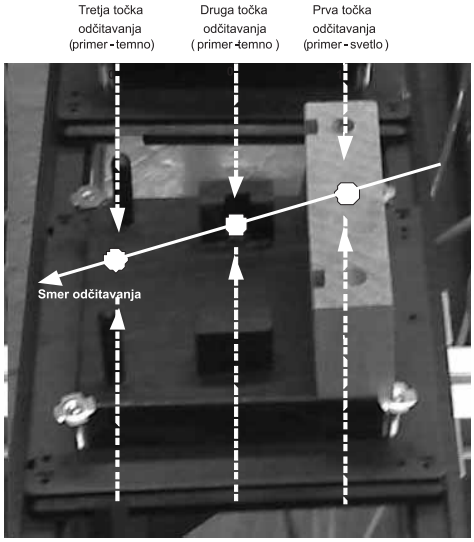
4 Opis uporabljenega tipala in princip prepoznavanja objektov

Način prepoznavanja objektov temelji na infrardečem tipalu Banner T18. Tipalo je nameščeno na nosilec, ki se nahaja na koncu robotske roke (manipulatorja). Tipalo je sposobno zaznavati svetla in temna področja. To pomeni, da svetlo območje ovrednoti z logično vrednostjo 1, temno območje pa z logično vrednostjo 0. Razločevanje med svetlim in temnim področjem temelji na principu količine odbite svetlobe. Kot primer vzamimo beli in črni list in ga primaknimo pod tipalo. Beli list veliko močneje odbija (sipa) svetlobo v primerjavi s črnim, ki velikšen del IR-žarka vpije, preostali del pa odbije nazaj v smeri proti tipalu. Del žarka, ki se odbije od površine moramo ponovno s površino tipala ujeti, kar pomeni, da mora površina tipala pri odčitavanju ležati vzporedno z odbojno ploskvijo. S tem zagotovimo, da žarek vpada na površino pod pravim kotom (popolni odboj). Ker moramo s slednjim prepoznati vsaj pet osnovnih elementov, v resnici jih je šest, le da sta srednji stranici identični, bo potrebno uporabiti za prepoznavo enega elementa vsaj tri bite oziroma logične vrednosti.

Uporabljeni deli so ovrednoteni z barvnimi kombinacijami, ki hkrati predstavljajo ekvivalentne kombinacije logičnih nivojev. Vrednotenje je ponazorjeno v tabeli 1:

Tabela 1: Prepoznane barve ovrednotene z logičnimi vrednostmi

Prepoznane barve ovrednotene z logičnimi vrednostmi			
0	**0**	**0**	Prazna paleta
0	**0**	**1**	Desna velika stranica
0	**1**	**0**	Majhna stranica
0	**1**	**1**	Napaka
1	**0**	**0**	Leva velika stranica
1	**0**	**1**	Dno hiške
1	**1**	**0**	Napaka
1	**1**	**1**	Streha



Slika 2. Postopek prepoznave sestavnh elementov
Fig. 2. Basic principle of component recognition

Na sliki 2 je prikazan osnovni princip prepoznave elementov s pomočjo infrardečega tipala. Glede na to, da je tipalo nameščeno na manipulator, je potrebno definirati tri točke, ki so znotraj območja nosilne palete, v katerih tipalo odčita vrednost. Na osnovi dobljene bitne kombinacije, ki jo sestavljajo trije biti, dobimo informacijo za kateri element v resnici gre. Točke se definirajo na trajektoriji giba manipulatorja, ki poteka nad paleto (pravokotno na postavljen element), tipalo pa odčita vrednost v definiranih točkah brez ustavljanja.

Vrednosti, ki jih navaja Tabela 1 ponazarjajo kombinacijo za vsak posamezen sestavni element, razen dveh kombinacij, ki vsebujeta po dve enici. Takšni kombinaciji sta nedovoljeni, saj nimamo nikdar na eni paleti tekočega traku po dva elementa. Če se povrnemo na sliko 2, bi kombinacija (1, 1, 0) pomenila, da se na paleti nahajata leva velika stranica in majhna stranica na sredini palete.

5 Snovanje algoritma

Pri izdelavi algoritma robotskega krmilnika NX100 si pomagamo z diagramom poteka, ki nam pomaga grafično ponazoriti posamezen korak. Diagram poteka nam predstavlja temelj, iz katerega začnemo snovati algoritem po metodi »top-down« (od zgoraj navzdol).Algoritem mora biti čimbolj enostaven, hiter in razumljiv, saj lahko le na ta način zagotovimo brezhibno delovanje, in se hkrati izognemo nepotrebnim pogojnim stavkom. Program smo gradili modularno, kar pomeni, da smo najprej zapisali strojno kodo za prepoznavanje in prijemanje elementov, ter šele nato, ko je ta delovala brezhibno, prešli na snovanje drugega dela algoritma, ki je namenjen sestavljanju elementov.

Za izvajanje naloge sestavljanja moramo imeti na voljo povratne informacije o prisotnih elementih na mestu sestavljanja. To pomeni, da moramo v pomnilniške lokacije krmilnika NX-100 shraniti informacijo o stanju na gradbišču (mestu sestavljanja), saj lahko le na takšen način robotu povemo, katere manjkajoče elemente še lahko vzame na odjemalnem mestu iz tekočega traku. Da bi bila zadeva čimbolj preprosta smo postavili pet spremenljivk z oznakami D001, D002, D003, D004, D005 katerim se bodo prirejali indikatorji. Stanja spremenljivk prikazuje tabela 2.

Tabela 2: Pomen indikatorjev, ki jih lahko posamezne spremenljivke zavzamejo

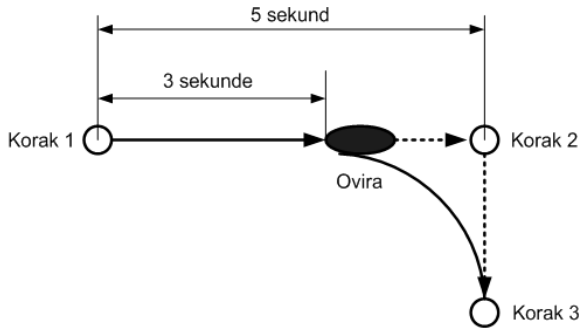
D0001	0	Prazno gradbišče
	1	postavljeno dno
	2	postavljeno dno + obe veliki stranici
	3	postavljeno dno + obe veliki stranici + obe mali stranici
	4	postavljeni vsi deli
D0002	0	ni nobene velike stranice
	1	postavljena LEVA velika stranica
D0003	0	ni nobene velike stranice
	1	postavljena DESNA velika stranica
D0004	0	ni nobene male stranica
	1	postavljena ZADNJA mala stranica

Pomen spremenljivk je naslednji; v kolikor je D0001 na vrednosti 0, je gradbišče prazno. To izda povelje, da mora manipulator poiskati dno hiše, kajti brez njega gradnje ne more pričeti. V trenutku, ko slednjega najde, poveča indikator na vrednost 1, s čimer sporoči da ima dno, hkrati pa takšna vrednost predstavlja pogoj za izvedbo drugega koraka v algoritmu. Ta korak je iskanje leve in desne velike stranice, za kateri ima rezervirani spremenljivki D0002 in D0003. V kolikor sta obe spremenljivki na vrednosti 0, bo manipulator začel iskati eno izmed njih (prvo, ki pride). Predpostavimo da je najprej našel levo in postavil indikator D0002 na vrednost 1, kar izda pogoj za iskanje desne velike stranice. Ko najde še to, postavi spremenljivko D0003 na vrednost 1, in ker sta sedaj obe spremenljivki na 1, se lahko vrednost D0001 poveča na 2. Podobno kot prej predstavlja to pogoj za izvedbo koraka iskanja malih stranic. Ko manipulator najde obe, in jih seveda uspešno postavi na svojo lokacijo, lahko ponovno inkrementira spremenljivko

D0001. Ko je slednji enak 3, se izvrši funkcija za iskanje zadnjega elementa (streha). V trenutku, ko je zadnji element uspešno postavljen na gradbišče, se D0001 postavi na vrednost 4, kar pomeni da je hiša sestavljena. Po izteku časa časovnika dveh sekund, se vsi indikatorji postavijo na vrednost 0, postopek sestavljanja nove hiše pa se lahko prične. Časovno obdobje dveh sekund je potrebno zagotoviti iz dveh razlogov, kjer prvi predstavlja varnostni razlog, drugi pa čas, ki je potreben, da se gradbišče sprazni.

6 Vodenje manipulatorja po položaju in sili (ang. servofloat)

Robotski mikrokrmilnik NX-100 nam omogoča vključitev funkcije vodenja robota po položaju in sili na dva načina. Sem spadata »link servofloat function« in »linear servofloat function«, kjer prva možnost nudi nadzorovanje navora nad vsako posamezno osjo posebej, medtem ko druga možnost nudi nadzorovanje navora nad trenutnimi koordinatami. Glede na potrebe pri izvajanju posamezne aplikacije izberemo ustrezno možnost. »Link servofloat function« omogoča vodenje po položaju, in vodenje po navoru (sili). V kolikor posamezna zunanja sila prepreči operiranje manipulatorja po vnaprej predvideni poti, slednji ne bo dosegel zadanega položaja. To velja za primere kjer je vključeno vodenje po položaju in sili. Kadar manipulator ne more doseči predvidene pozicije zaradi delovanja zunanje sile (ovire ipd.), slednji izvrši naslednjo instrukcijo. Takšen primer nam prikazuje slika 3, kjer je manipulator med obratovanjem naletel na nepredvideno oviro.



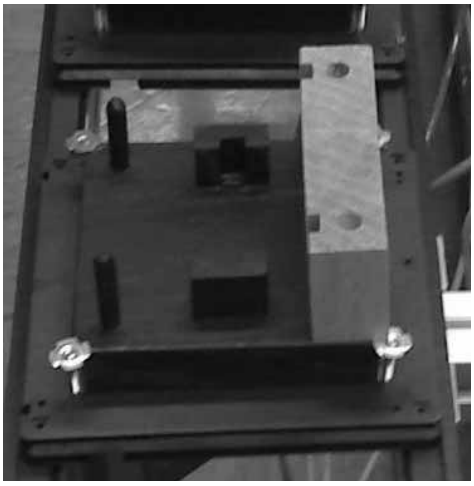
Slika 3. Ovira na poti trajektorije od koraka 1 do koraka 2, ki spremeni smer gibanja do končnega cilja
Fig. 3. Barier on trajectory between step 1 and step 2. With servofloat function can robot avoid this barier and jump directly over shortest path to step 3

Na preprostem primeru, ki je prikazan na sliki 3 uporabljamo zgolj linearne gibe med določenimi točkami, kjer imamo vključeno funkcijo vodenja manipulatorja po položaju in sili.

Manipulator se začne premikati v smeri iz točke 1 v točko dva, kjer po treh sekundah naleti na oviro. V istem trenutku se ob nasprotno delujoči sili ustavi, ter ostane v zaustavljenem položaju preostali dve sekundi. Po izteku skupnega časa petih sekund se manipulator sam prestavi v korak 3, vendar zaobide korak 2, ki ga zaradi nameščene ovire ne mora doseči (izvede naslednjo instrukcijo). Naslednjo instrukcijo lahko izvede samo v primeru vključene funkcije vodenja po položaju in sili.

7 Pobiranje sestavnih elementov hiše

Sestavni elementi hiše prihajajo na tekočem traku po naključnem zaporedju. Kot smo že omenili uvodoma, uporabljamo za prepoznavo elementov, infrardeče tipalo, ki deluje na količino odbite svetlobe od podlage. Preden začnemo vršiti postopek prepoznave elementov moramo izvesti postopek kalibracije tipala. Slednje postavimo v horizontalini položaj, kjer po empiričnem postopku določimo primerno višino za najboljšo možno prepoznavo elementov. Kalibracijo smo izvedli zaradi razlike v višini med paleto in elementi (streha je bližje tipalu, kot stranice oziroma dno, katero je najbolj oddaljeno). Iz tega razloga poiščemo optimalno točko, ki je rezultat empiričnih poizkusov, kjer dobimo najboljši vzorec pravilno prepoznanih elementov. Razliko v višini med stranico in paleto prikazuje slika 4.



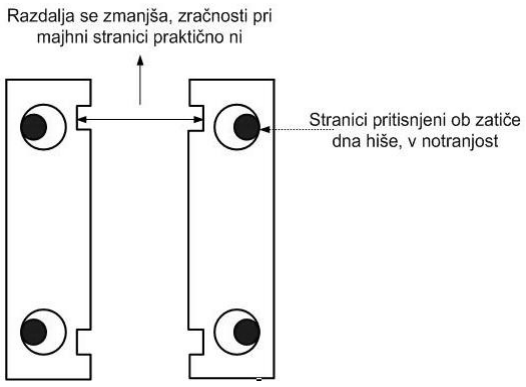
Slika 4. Element »leva stranica« na paleti tekočega traku
Fig. 4. Left side element on round ribbon palette

Po uspešni prepoznavi elementa sledi pobiranje le tega. Za prijem elementov uporabljamo dvo-prstno prijemalo, katerega prožimo in vzdržujemo pritisk s pnevmatskim signalom. Prijemalo je izvedeno tako, da ima na notranji strani »prstov«, kjer element primemo, nalepljeni 5 milimetrov debeli elastični gobici. Takšna izvedba nam pri prijemu zelo koristi (preprečuje zdrs elementa iz prijemala), vendar ima slabo lastnost, da nase »prilepi« pobrani element, kar predstavlja težave pri odlaganju. Za stisk prijemala je potrebno modificirati čeljusti v smislu, da ne stiskajo elementa premočno. Pomagali smo si s plastičnimi podlogami, s čimer povečamo ali zmanjšamo razmak med čeljustima prijemala. V kolikor je stisk še vedno premočan, lahko jakost uravnavamo še s pomočjo regulacije dovedenega pnevmatskega signala, ki je v optimalni rešitvi znašal dve atmosferi.

Sestavni deli, ki jih pobiramo iz strežnega mesta, so naloženi na lesene palete. Le te imajo različne tolerance, kar pomeni, da se lahko dve paleti medsebojno razlikujeta po višini, kakor tudi razmiku zatičev. Do razlik prihaja zaradi nenatančne izdelave, in uporabljenih lesenih neimpregniranih materialov, ki s časom spreminjajo strukturo, obliko in dimenzijo. To je razlog, da moramo dodeliti točno določeno paleto k točno določenemu elementu (gradniku hiše). Paleto in njen pripadni element moramo pri sestavljanju striktno uporabljati v navezi, saj se le tako definirani točki prijema in odlaganja ujemata.

8 Odlaganje sestavnih elementov hiše

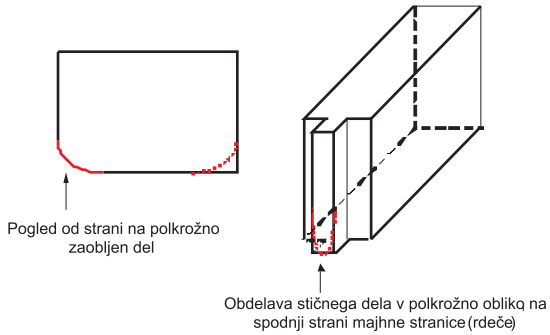
Pri odlaganju elementov imata najpomembnejši vlogi toleranca in natančnost določitve točk odlaganja. Pomembna je orientiranost elementov na prijemalnem mestu v vseh treh dimenzijah (roll, pitch, yaw), saj mora imeti element enako orientiranost, kot je bila v primeru določanja točke prijema in točke odlaganja. Takšen način je v nasprotju z načeli robotizacije proizvodnje. Pri robotskem sestavljanju, se v praksi uporabljajo identične odjemalne palete, in identični gradniki. Ker tega nimamo na voljo moramo poiskati kompromis in ustrezno rešitev za preizkus delovanja. Osnovna gradnika (leva velika in desna velika stranica) sta bila zasnovana z zračnostjo lukenj enega milimetra, kar je omogočalo lažje sestavljanje. Gledano iz vidika sestavljanja je to dobrodošla lastnost, s katero se izognemo zatikanju, vendar se takšnim tolerancam v praksi poizkušamo izogniti. Slabo lastnost vpliva velikih toleranc lahko opišemo na praktičnem primeru: ob postavitvi obeh velikih stranic s toleranco lukenj enega milimetra na vogalnike dna hiše, se lahko zgodi, da se obe stranici prislonita k notranjosti (slika 4), kar posledično zmanjša razdaljo med obema stranicama.



Slika 5. Tolerance zračnosti v reži za majhne stranice praktično ni
Fig. 5. Decreaseing tolerance between both big side elements. Distance between both side elements is under allowed level

Ob vstavljanju majhnih stranic (slika 5) nastopi težava, saj je razdalja manjša oziroma enaka dolžini majhne stranice.

Da se izognemu omenjenemu problemu, je potrebno majhne stranice ustrezno oblikovat. Spodnji del, ki pri sestavljanju najprej preide v utor, preoblikujemo v polkrožno obliko (slika 6). To nam omogoča, da se bosta obe veliki stranici postavljeni po scenariju prikazanem na sliki 5, pri vstavljanju majhnih stranic razmaknili na ustrezno razdaljo. Problem je moč rešiti še z uporabo funkcije vodenja po položaju in sili, ki naredi manipulator podajen. To pomeni, da se slednji podaja po prednastavljeni sili v definiranih smereh. S tem dosežemo kopijo obnašanja zapestja človeške roke.



Slika 6. Obdelan spodnji del utora majhne stranice
Fig. 6. Cultivated bottom side of the smallest side element

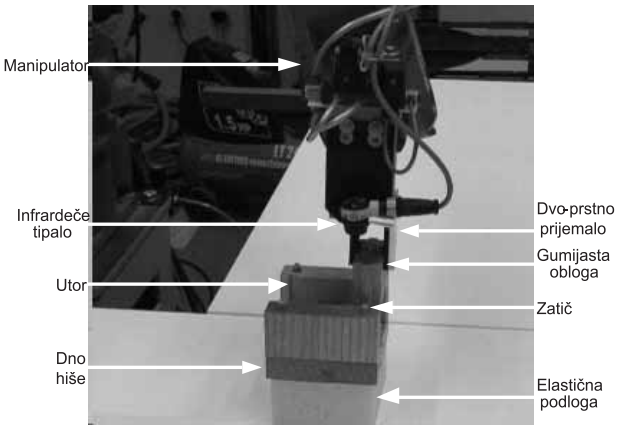
To lahko opišemo na primeru vstavljanja zatiča v luknjo, ki ima majhno zračnost. Človek bo pri vstavljanju zatiča izvajal akcije kroženja zapestja, s čimer bo zatič spravil v luknjo. Z uporabo vodenja po položaju in sili dosežemo ravno takšen učinek, s katerim si pomagamo pri sestavljanju elementov z majhnimi zračnostmi.

Beseda vodenje po položaju in sili pomeni, da naredimo manipulator podajen v želeni smeri. Podajnost lahko nastavimo v vseh smereh gibanja vključno s podajnostjo vrha orodja. V empiričnem poizkusu smo iskali ustrezne nastavitve posameznih parametrov, ki predstavljajo maksimalno uporabnost za izvajanje naše aplikacije. Zadovoljive rezultate je dajalo linearno vodenje po položaju in sili, kjer lahko podajnost manipulatorja nastavljamo v vseh smereh (X, Y, Z, R, B, T), oziroma samo v tisti smeri, ki deluje nasproti smeri odlaganja (smer X). Tovarniško pred-nastavljeni parametri za vodenju po položaju in sili niso določeni, zato moramo le te ugotoviti s pomočjo metode poizkušanja. Parametre izberemo po metodi najboljšega poizkusa. Vrednosti, ki jih nastavimo ne smejo biti premajhne, saj manipulator v takšnem primeru preveč niha. Vzrok nihanja gre pripisati delovanju sile težnosti na konec manipulatorja, kjer svoj delež doprinese še gradnik v prijemalu. Manipulator se skuša temu upirati in popravljati smer gibanja, kar se odraža v obliki nihanja. To nas prisili, da procentualne vrednosti povečamo, s tem pa izgubimo na dobri podajnosti, kar pomeni, da se manipulator že močneje upira postavljeni oviri. Vodenje po položaju in sili torej deluje na principu tokovnih omejevalnikov, ki omejujejo tok v sklepnih servomotorjih v skladu z nastavljenimi procentualnimi vrednostmi. Zaradi relativno visokih procentualnih vrednosti parametrov vodenja po položaju in sili, s katerimi odpravimo

nihanje manipulatorja, posledično pa ga napravimo manj podajnega, uporabili dodaten varnostni ukrep. Na mesto sestavljanja položimo elastično podlogo, ki predstavlja dodatno podajnost v navezi z manipulatorjem. Elastična podloga predstavlja tudi varovalni element, v kolikor bi pri sestavljanju šlo kaj narobe. S tem obvaruje delovno površino, sestavne gradnike, kot tudi sam manipulator.

Elastična podloga je fiksno pritrjena na delovno površino, kar pomeni, da se njena lokacija glede na referenčni koordinatni sistem manipulatorja ne spreminja. Eno izmed težav smo že omenili v predhodnjih poglavjih, ki se nanaša na lepljenje elementov k elastični oblogi prijemala. Ker goba (elastična podajna podlaga) nima na vrhu utora, z minimalnimi tolerancami, kamor bi dno hiše pričvrstili. Tako je ob vsakem odlaganju dno hiše obležalo na drugačni lokaciji. Vzrok za to, je lepljenje elementa na gumijasto podlogo prijemala, kar posledično pri neenakomernem odpiranju čeljusti postavi element venomer na drugačno pozicijo na odlagalnem mestu, glede na izhodiščni (referenčni koordinatni sistem). Neenakomernost odpiranja čeljusti prispeva k potiskanju dna hiše levo ali desno od želenega središčnega položaja. Tega si nikakor ne smemo privoščiti. Problematika je rešljiva na več načinov: prvi je ta, da izdelamo togi podstavek, ki se popolnoma ujema z dnom hiše (gradnikom), hkrati pa ima minimalne tolerance zračnosti. Takšni podstavek bi pritrdili na elastično podlogo, ter od tam naprej gradili skupek sestavnih elementov v celoto. Druga možnost, ki smo jo izbrali mi, je ta, da na vrh elastične podloge pritrdimo obojestranski lepilni trak, kjer pri odlaganju dna hiše, le tega najprej potisnemo centimeter v gobo, da se oba sprimeta, ter šele nato odpremo čeljusti prijemala.

Omenimo še nekaj dejavnikov, ki vplivajo na robotsko sestavljanje. Miza in tekoči trak nista fiksno pritrjena v tla, prav tako tudi nista medsebojno fiksno povezana. Pomanjkljivost kaže svoje rezultate prvič v primeru odčitavanja, drugič v primeru odjemanja elementov iz tekočega traku, tretjič pa pri odlaganju. Predpostavimo, da smo za določen primer fiksno določili tri točke odčitavanja za zdajšnjo pozicijo tekočega traku. Zgodi se lahko, da nam nekdo mizo tekočega traku premakne v drugo pozicijo. To pomeni, da se točke odčitavanja ne bodo skladale z želeno pozicijo elementov na paleti tekočega traku, kar povzroči nepravilno prepoznavo, oziroma napake pri prepoznavi posameznega elementa. V najslabšem primeru je lahko prepoznava izvedena pravilno, vendar se točka prijema elementa na odjemalnem mestu ne sklada s pred-definirano. Ker bomo s prijemalom v takšnem primeru prijeli element drugače, bo ta vzrok imel posledice pri odlaganju elementa. Posledice so lahko v obliki poškodbe sestavnega elementa, poškodbe delovne površine oziroma nenazadnje v obliki poškodbe manipulatorja.



Slika 7. Sestavljanje lesene hiše z manipulatorjem Motoman HP6

Fig. 7. Constructing wood house with robot Motoman HP6.

9 Zaključek

V članku smo želeli predstaviti dejavnike, ki vplivajo na robotizacijo proizvodnje. Tekom izvajanja projekta smo naleteli na številne pomankljivosti na katere v uvodu nismo računali, zato smo iz tega razloga predlagali možne rešitve, ki temeljijo na preprostih principih, le tem, pa smo za primerjavo ob bok postavili principe, ki se uporabljajo v profesionalne namene. Naš pristop je temeljil na preprostih rešitvah, s katerimi smo dosegli želene rezultate. Manipulator je v navezi s tekočim trakom brez vključene optimizacije hišo sestavil v časovnem intervalu od dveh do treh minut (odvisno od zaporedja elementov na tekočem traku). Z vključitvijo pohitritve gibov manipulatorja in optimizacijo sortiranja elementov na tekoči trak, lahko čas sestavljanja opazno zmanjšamo, kar predstavlja izzive za nadaljnje delo na omenjenem projektu. Prav tako je tematika nadaljnjega dela usmerjena na področje vključitve umetnega vida za prepoznavo objektov.

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THE ARISING OF ELECTRIC DISCHARGE ARCS

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Key words: discharging arc, corona, displacement current, excitation energy, gas ionization.

Abstract: From the viewpoint of electric arcs, electric contacts are systematized due to their mechanic and electric operations in this paper. During the contact operation, drawn and discharging arcs or other discharging phenomena can occur depending on load currents. The difference between the drawn arcs and the discharging arcs is also shown. Further on, the phenomenon of the arising of the discharging arcs from corona is discussed by analyzing this phenomenon through the authors' mathematical model. This model calculates an electron average kinetic energy obtained by its movement along its mean free path in the non-homogeneous electric field between two spherical electrodes. The excitation energy of a gas molecule produced by the electron impact is compared with the first ionization energy and with the dissociation energy of the gas molecule, and the carry-on electron kinetic energy is determined. The displacement current is introduced into the model in the case of the alternating electric field, and its active and reactive component are established due to a complex value of the relative permittivity of the gas. The active component of the displacement current is in the phase with the electric field intensity, and causes the excitation energy in the gas molecules. Ranges of highly ionized, partly ionized and non-ionized molecules are founded in the whole volume. At the end some conclusions are made by comparison of a breakdown voltage obtained by the mathematical model with Paschen's voltage and the measuring result of the discharging arc is also introduced.

Nastanek električnih razelektritvenih oblokov

Kjučne besede: razelektritveni oblok, korona, poljski tok, vzbujevalna energija, ionizacija plinov.

Izvleček: S stališča električnih oblokov so v tem članku električni kontakti sistematizirani glede na njihovo mehansko in elekrično delovanje. Med delovanjem kontakta lahko nastanejo potegnjeni in razelektritveni obloki ali druge oblike razelektritve, kar je v glavnem odvisno od bremenskega toka. Prikazana je tudi razlika med potegnjenimi in razelektritvenimi obloki. Nadalje je obravnavan nastanek razelektritvenih oblokov iz korone z analiziranjem tega pojava s pomočjo matematičnega modela avtorjev članka. Model izračunava povprečno kinetično energijo elektrona, ki jo doseže s preletom svoje srednje proste poti v nehomogenem električnem polju med dvema kroglastima elektrodama. Vzbujevalna energija plinske molekule, ki jo povzroča sila trka elektrona, je primerjana s prvo ionizacijsko energijo in z disociacijsko energijo plinske molekule, obenem je izračunana preostala energija elektrona, ki jo prenese na naslednji trk. Za primer izmeničnega električnega polja je v modelu določen poljski tok in ugotovljeni sta njegova delovna in jalova komponenta glede na kompleksno vrednost relativne dielektričnosti plina. Delovna komponenta je v fazi z električno poljsko jakostjo in povzroča vzbujevalno energijo v plinskih molekulah. V prostoru so ugotovljena območja z visoko vsebnostjo ioniziranih molekul, z delno vsebnostjo ioniziranih molekul in območje brez ionizacije. Na koncu so podani nekateri zaključki s pomočjo primerjave prebojne napetosti, dobljene z matematičnim modelom in Paschenovo napetostjo. Podan je tudi rezultat meritve razelektritvenega obloka.

1. Introduction

Dealing with electric arcs as phenomena occurring between electric contacts, we have to classify the electric contacts according to their mechanic and electric operation. Due to the mechanic operation, the electric contacts are axial switching contacts and sliding contacts. The axial switching contacts have contact members that move in perpendicular direction to contact surface when changing their position. But, with the sliding contacts, their members move along the contact surface that means the parallel moving of both contact surfaces. Due to the electric operation, the electric contacts are making, breaking and holding or permanent. The making contacts establish the electric connection between their members and electric discharge mainly occurs due electric charged capacitance in a circuitry and especially due to a bouncing phenomenon of the making contact members when they close. This paper is not going to deal with that kind of discharges. The breaking electric contacts disconnect the electric circuit and when the contact members are separating from each other, a gap opens between them. In the gap between the contact members, drawn and discharging arcs or other discharging phenomena can occur. The holding or the permanent contacts have contact members that are touching and the connection is not time-depended. While the axial switching contacts, when holding, are steady, the sliding contacts are either steady or slipping. The drawn arcs can occur also with the sliding contacts, although they are permanent, such as slip rings, because the microscopic gap between the contact members varies due to the roughness, contamination and damages of the surfaces of both contact members /1/. This paper deals with the discharging arcs, which are stable or unstable since the drawn arcs are discussed in other papers /1/, /2/. The difference between the drawn arc and the discharging arc is in the time-depended electric current flow through the medium between the contact members when separated. The electric current flow is continuous with the drawn arc and decreases with its length. The medium is the ionized vapour of the cathode and the anode materials. But, with the discharging arc, the current between the separating contact members instantly falls towards zero value, a transient voltage appears due to time derivative of the current, which extends to a breakdown voltage value of the neighbouring gas medium – Fig. 1.

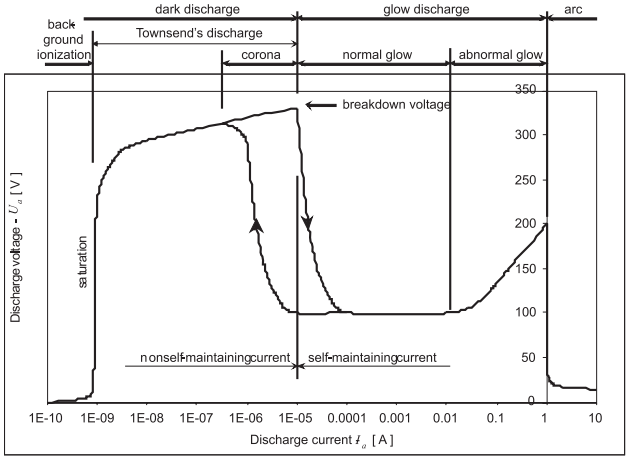

Fig. 1: The principle electric discharge UI *characteristics; the discharge current is relative to the infimum arc current.*

The medium is an existing gas in the surrounding space. When the breakdown voltage of the gas is exceeded by the transient voltage, the electric breakdown of the insulating gas occurs, the electric current increases. What kind of discharge follows, depends on the current through the gas: the dark discharge, the glow discharge or the discharging arc. The later one is either the stable or the unstable arc. Nevertheless, which arc occurs, it arises from the ionized gas molecules. If there is no existing gas in the surrounding space of the contacts, the discharging arc begins by the ionization of the cathode material vapour. This kind of arcs is vacuum arcs.

Therefore the mathematical model of a spark gap of two spherical electrodes was developed to study the electric field and the ionizing process in the gap. The spherical electrodes were an approximation of the contact members (rivets) with the gap between them when breaking an electric circuit load. The electric load was an inductance-capacitance parallel circuit with a resistance in the inductive branch. The response of the circuit on the breaking manoeuvre was the damped oscillation at the series resonance of the circuit. This circuit represents an air coil in the most simplified way.

2. The mathematical model of a spark gap of two spherical electrodes

The mathematical model is based on two spherical electrodes with the same radius r_0 and separated by the distance d_{sur} between their surfaces. An anode is positively charged and a cathode has a negative charge by the same absolute amount of charge. The cathode is earthed so that there is a positive charge flow from the cathode to the earth. Due to the mutual influence of the anode and the cathode charges, the equivalent point charges of the anode and the cathode lie in the eccentric positions in the relevant spheres – Fig. 2. The mathematical model is solved in two dimensional space because the electric field is rotary symmetrical. The eccentric positions of the equivalent point charges are defined by eccentric radius r_{ecc} as it is defined in this paper and shown in Fig. 2, and further on, the eccentric position of the cathode equivalent point charge is the zero point of the coordinate system. A potential of any point $T(r,\varphi) = T(r,r_a)$ in the space is an algebraic sum of the partial potentials caused by the anode and the cathode charges since the potential is scalar value. It is defined by the following equation in the bi-radial coordinates /4/:

$$U(r,r_\alpha)=\frac{Q}{4\cdot\pi\cdot\varepsilon}\left(-\frac{1}{r}+\frac{1}{r_\alpha}\right) \tag{1}$$

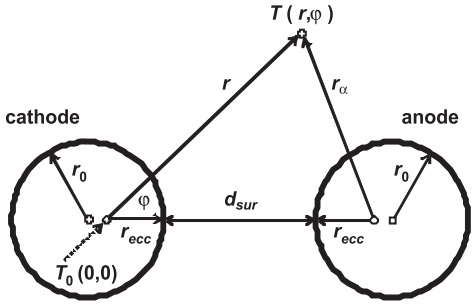

Fig. 2: The geometrical drawing of the cathode, the anode and the distances between them in r-φ *coordinate system.*

Further on,

$$U(r,\varphi)=\frac{Q}{4\cdot\pi\cdot\varepsilon}\cdot\left(-\frac{1}{r}+\frac{1}{\sqrt{(2\cdot r_{ecc}+d_{sur})^2+r^2-2\cdot(2\cdot r_{ecc}+d_{sur})\cdot r\cdot\cos\varphi}}+\frac{1}{r_{ecc}}-\frac{1}{r_{ecc}+d_{sur}}\right) \tag{2}$$

since the cathode is earthed, its surface potential is defined as zero:

$$r=r_{ecc}\ \wedge\ \varphi=0\ \Rightarrow\ U=0 \tag{3}$$

Between the anode and the cathode a certain voltage is applied, therefore the anode-cathode voltage is introduced instead of the anode and the cathode charges by using Eq. (2) under the following condition:

$$r=r_{ecc}+d_{sur}\ \wedge\ \varphi=0\ \Rightarrow$$

$$\Rightarrow\ U_{\alpha\kappa}=\frac{Q}{2\cdot\pi\cdot\varepsilon\cdot r_{ecc}\cdot\left(1+\frac{r_{ecc}}{d_{sur}}\right)} \tag{4}$$

Hence, the voltage of any point in the space is:

$$U(r,\varphi)=U_{\alpha\kappa}\cdot\frac{r_{ecc}}{2}\cdot\left(1+\frac{r_{ecc}}{d_{sur}}\right)\cdot\left(-\frac{1}{r}+\frac{1}{\sqrt{(2\cdot r_{ecc}+d_{sur})^2+r^2-2\cdot(2\cdot r_{ecc}+d_{sur})\cdot r\cdot\cos\varphi}}+\frac{1}{r_{ecc}}-\frac{1}{r_{ecc}+d_{sur}}\right) \tag{5}$$

The electric field intensity is:

$$\vec{E} = -\operatorname{grad}\left(U(r,\varphi)\right) = -\left(\vec{1}_r \cdot \frac{dU(r,\varphi)}{dr} + \vec{1}_\varphi \cdot \frac{dU(r,\varphi)}{r \cdot d\varphi}\right) \quad (6)$$

The radial component of the vector of the electric field intensity is:

$$\vec{E}_r = -\vec{1}_r \cdot \frac{dU(r,\varphi)}{dr} = \vec{1}_r \cdot U_{\alpha\kappa} \cdot \frac{r_{ecc}}{2} \cdot \left(1 + \frac{r_{ecc}}{d_{sur}}\right) \cdot \left(-\frac{1}{r^2} + \frac{r - (2 \cdot r_{ecc} + d_{sur}) \cdot \cos\varphi}{\left((2 \cdot r_{ecc} + d_{sur})^2 + r^2 - 2 \cdot (2 \cdot r_{ecc} + d_{sur}) \cdot r \cdot \cos\varphi\right)^{\frac{3}{2}}}\right) \quad (7)$$

and its angular component is:

$$\vec{E}_\varphi = -\vec{1}_\varphi \cdot \frac{dU(r,\varphi)}{dr} = \vec{1}_\varphi \cdot U_{\alpha\kappa} \cdot \frac{r_{ecc}}{2} \cdot \left(1 + \frac{r_{ecc}}{d_{sur}}\right) \cdot \frac{r \cdot (2 \cdot r_{ecc} + d_{sur}) \cdot \sin\varphi}{\left((2 \cdot r_{ecc} + d_{sur})^2 + r^2 - 2 \cdot (2 \cdot r_{ecc} + d_{sur}) \cdot r \cdot \cos\varphi\right)^{\frac{3}{2}}} \quad (8)$$

To establish the eccentric radius r_{ecc} as it is defined in Fig. 2, the mathematic inversion on the sphere with the radius of r_0 (known as Kelvin's transformation also) is used and the following result is obtained:

$$r_{ecc} = \frac{d_{sur}}{2} \cdot \left(\sqrt{1 + 4 \cdot \frac{r_0}{d_{sur}}} - 1\right) \quad (9)$$

The shortest field line between the spherical electrodes of the opposite charges is the shortest surface-to-surface distance between the spheres. In this case the angle φ is zero. The vector of electric field intensity has only radial component since the angular component is zero. Hereafter the mathematical model deals with the electric field and the phenomena associated with it in this particular direction. Therefore, the radial coordinate in this direction is named as r_x – radius in the *x*-direction. Hence the vector of the electric field intensity between the cathode and the anode is:

$$\vec{E} = \vec{E}(r_x) = -\vec{1}_x \cdot E(r_x) \quad (10)$$

where $E(r_x)$ is its absolute value:

$$E(r_x) = U_{\alpha\kappa} \cdot \frac{r_{ecc}}{2} \cdot \left(1 + \frac{r_{ecc}}{d_{sur}}\right) \cdot \left(\frac{1}{r_x^2} + \frac{1}{(2 \cdot r_{ecc} + d_{sur} - r_x)^2}\right) \quad (11)$$

The average velocity of an electron is according to Eq. (8) in literature /1/ as follows:

$$v_{e\_avg} = \sqrt{\left(\frac{m_e}{W_{ek}} + \frac{1}{c^2}\right)^{-1}} \quad (12)$$

According to the same equation the average velocity of an air gas molecule (O_2 or N_2) is established by substitution of the electron kinetic energy and mass by the molecule kinetic energy and mass in Eq. (12), so that the molecule velocity is:

$$v_{m\_avg} = \sqrt{\left(\frac{m_m}{W_{mk}} + \frac{1}{c^2}\right)^{-1}} \quad (13)$$

where the kinetic energy of the gas molecule is /6/:

$$W_{mk} = \frac{3}{2} \cdot k \cdot T \quad (14)$$

The mean free path of the electron up to collision with the gas molecule is derived from /5/:

$$\lambda = \frac{R \cdot T}{\sqrt{1 + \frac{v_{m\_avg}^2}{v_{e\_avg}^2}} \cdot \pi \cdot d^2 \cdot N_A \cdot p} \quad (15)$$

where the quantity *d* is:

$$d = r_e + r_m \quad (16)$$

The average kinetic energy of the electron travelling along the mean free path is:

$$W_{ek} = e \cdot E(r_x) \cdot \lambda \quad (17)$$

because the electric field intensity and the mean free path are co-linear vectors.

When the electron collided with the gas molecule, its kinetic energy is transferred to the molecule by impact as excitation energy of the molecule:

$$W_{exm} = W_{ek} \quad (18)$$

Following the direction of the cathode-anode gap towards the centre of the gap, these phenomena can occur: the ionization and the recombination of the gas molecules, the dissociation of the gas molecules, and further on, simply no effects on the gas molecules occur by their collision with the electrons. From the gap centre towards the anode these phenomena occur in reverse order. Which phenomenon takes place, and which do not, depends on the kinetic energy of the electrons, which means it depends on the excitation energy of the molecule, as it is defined by Eq. (18).

Due to the decreasing function of the electric field intensity depending on the radius in the range from the cathode to the gap centre, it is established, that there are four possible kinds of collisions with respect to the excitation energy of the molecules along the path between the cathode and the anode as follows:

1. Adjoining the ionization of the gas molecules, the inverse process also takes place. The probability of the ionization is P_i = 50 % and the probability of the recombination is (1 - P_i) = 50 %. The excitation energy of the molecule is:

   $$W_{exm} \geq W_{ion} \quad (19)$$

   When this electron collides with the gas particle, there are two possible reactions:

   a. If the gas particle is the molecule, ***the ionization*** of it takes place. The collision is partly inelastic, and it consumes the ionization energy and the additional electron is emitted from the mole-

cule. After the collision, the average kinetic energy per electron of these two electrons, that is of the one colliding and the one emitted, is:

$$W_{ek\_on} = \frac{W_{exm} - W_{ion}}{2} \cdot P_i \qquad (20)$$

and it is carried on by each electron to the next collision. After each of them has passed the next mean free path it gets the additional kinetic energy defined by Eq. (17).

b. If the gas particle is the ion in the neighbourhood of the cathode and the anode, ***the recombination*** occurs. The collision is totally inelastic, and it consumes the whole kinetic energy of the electron. The excitation energy of the recombined molecule is thermal energy and causes the molecule tem-perature rise above the ambient temperature for the increment:

$$\Delta T = \frac{2 \cdot W_{exm}}{3 \cdot k} \cdot (1 - P_i) \cdot (1 - K) \qquad (21)$$

So far the average temperature of the gas in the neighbourhood of the cathode and the anode rises and the temperature of the each electrode increases too, when the molecules bump at it. The parameter K=99.8% in Eq. (21) defines the percentage of the excitation energy, conveyed and conducted to the cathode and the anode, and further on, to the ambient as a natural or a forced cooling of both electrodes. Due to the temperature increment of Eq. (21), the average kinetic energy of the gas molecules increases according to Eq. (14), and so the average molecule velocity does according to Eq. (13). The recalculation process is convergent.

2. With the increasing radius, the electric field intensity decreases – Eq. (11), and the excitation energy of the molecule also decreases to such extend that:

$$W_{ion} > W_{exm} \geq W_{diss} \qquad (22)$$

In this case, the excitation energy of the gas molecule causes ***the dissociation*** of the two-atom molecule into two gas at-oms. This collision is partly inelastic and it consumes the dissociation energy. The remaining kinetic energy of the colliding electron is carried on by the same electron:

$$W_{ek\_on} = W_{exm} - W_{diss} \qquad (23)$$

and further on, it increases because the electron passes the next mean free path before the next collision – Eq. (17).

3. If the excitation energy of the molecule is lower than the dissociation energy of the gas molecule:

$$W_{diss} > W_{exm} \qquad (24)$$

the colliding electron has ***no effect*** on the gas molecule. The kinetic energy of the electron is carried on to the next collision because the collision is elastic:

$$W_{ek\_on} = W_{ek} \qquad (25)$$

The ionization-recombination collisions take place near the cathode, ***the dissociation collisions*** are next to them in the direction of increasing radius towards the gap centre and further on, there are ***the no-effect collisions***, and follows in the reverse order towards the anode.

Although there is a sequence of these phenomena, we could not consider there are any pure ranges such as an ionization-recombination range, a dissociation range and a no-effect range. But very near to the each electrode there is ***a highly ionized range*** because the electrons in this range have very high kinetic energy and nearly every collision causes such excitation energy in the molecule that its ionization occurs. Next to this range is ***a partly ionized range*** up to the point where no ionization occurs. At this point ***a non-ionized range*** begins and lies around the gap centre – Fig. 3.

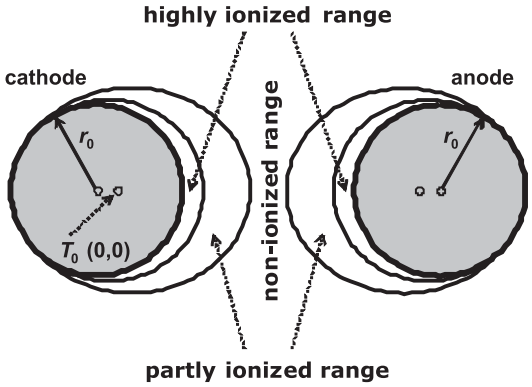

Fig. 3: The ranges of the arising discharge due to switch off manoeuvre in the electric circuit in Fig. 4 at the input-output quantities in Tab. 1 for oxygen molecules as simulated by the model.

In the highly ionized range, the ionization-recombination collisions take place mainly. In the partly ionized range, both the ionization-recombination and the dissociation collisions occur. Further on, in the non-ionized range, there are no ionization collisions, but the dissociation collisions and the no-effect collisions take action. This is the most general situation in the cathode-anode gap and in this case there is no electric breakdown through the cathode-anode gap. If the non-ionized range is not present in this gap along the shortest field line due to the high values of the electric field intensity (caused by the high anode-cathode voltage) and at least the partly ionized ranges come together from the cathode and the anode side, the electric breakdown occurs and electric discharge takes action through a stable or unstable arc, or as a glow discharge with a self-maintaining current.

There were some simplifications made during this modelling process:

1. When deriving Eqs (12) and (13), the following relations were presumed:

$$0 < \frac{v_{e\_avg}}{c} << 1$$
$$0 < \frac{v_{m\_avg}}{c} << 1 \qquad (26)$$

2. The rest and the actual masses of the electron and the gas molecule correspond to:

$$m_e << m_m$$
$$m_e(v_e) << m_m(v_m) \quad (27)$$

3. The ionizations and the recombinations take place in the same range that is in the highly ionized and in the partly ionized range, which lies by the both electrodes.

Knowing the electric field intensity at the cathode surface at $\varphi = 0$ and its temperature, the following conductive current densities are calculated: the current density of the field emission and the current density of the thermionic emission. Both of them are the active current densities.

The current density of the field emission is calculated by the Fowler - Nordheim equation /1/:

$$j_E = \frac{e^2}{8\cdot\pi\cdot h\cdot\frac{m_e^*}{m_e}}\cdot\frac{E^{*2}}{V_{\phi\kappa}^*}\cdot e^{-\frac{8\cdot\pi\cdot\sqrt{2\cdot m_e^*}\cdot e}{3\cdot h}\cdot\frac{V_{\phi\kappa}^{*3/2}}{E^*}+\frac{\sqrt{8\cdot m_e^*\cdot e^3}}{3\cdot h\cdot\varepsilon_0}\cdot V_{\phi\kappa}^{*-1/2}} \quad (28)$$

Possible thin insulation of the cathode and the roughness of the cathode surface effect the electric field intensity, the work function and the effective electron mass /1/. Therefore the following substitutions must be considered in Eq. (28) to describe exploatation condition of the cathode:

$$E^* = \beta\cdot E \quad \Leftarrow \quad \beta = 5$$
$$V_{\phi\kappa}^* = \frac{V_{\phi\kappa}}{\upsilon} \quad \Leftarrow \quad \upsilon = 5 \quad (29)$$
$$m_e^* = \frac{m_e}{\mu} \quad \Leftarrow \quad \mu = 5$$

but the values of these coefficients were presumed in the model.

The current density of the thermionic emission is defined according to /5/ as:

$$j_T = \frac{4\cdot\pi\cdot m_e\cdot e\cdot k^2}{h^3}\cdot T_\kappa{}^2\cdot e^{\frac{e}{k\cdot T_\kappa}\left(-\frac{V_{\phi\kappa}}{\upsilon}+\sqrt{\frac{e\cdot\beta\cdot E}{4\cdot\pi\cdot\varepsilon_0}}\right)} \quad (30)$$

The direct electric field was dealt with up to this point. If an alternating electric field is applied, a displacement current occurs, which has the following properties essential to establish the mathematical model of electric discharge:

- The displacement current could be measured inside the gas gap between the cathode and the anode.
- There are no current carriers (electrons and ions) in the gap due to this phenomenon.
- There is no rise in electric field intensity due to this phenomenon, so the field emission of the electrons is unchanged.
- This current causes no heat dissipation on the cathode surface, therefore there is no rise in temperature, and further on, there is no rise in the thermionic emission of electrons due to this phenomenon.
- The active component of this current causes the excitation of the two-atom gas molecules and further on the ionization and the dissociation of these molecules.
- The reactive component of this current causes that the electric energy is stored in the capacitance.
- Consequently to the ionization of the gas molecules, the recombination of the gas ions occurs, the thermal energy of the recombined gas molecules increases, but this rise is the effect of the recombination process, and not the effect of the displacement current.

The displacement current is defined in general by its density /4/ as:

$$\hat{j}_D = \breve{\varepsilon}_r\cdot\varepsilon_0\cdot\frac{d\hat{E}(r_x,t)}{dt} \quad (31)$$

The displacement current is complex current density (represented by a phasor) through the capacitance between the cathode and the anode. The relative permittivity $\breve{\varepsilon}_r$ is complex scalar quantity defined by its absolute value e_r and by losses angle d as follows:

$$\breve{\varepsilon}_r = \varepsilon_r\cdot e^{-i\cdot\delta} \quad (32)$$

Further on, the absolute value of the active displacement current is:

$$j_{Dact} = \varepsilon_r\cdot\varepsilon_0\cdot\frac{dE(r_x,t)}{dt}\cdot\sin\delta \quad (33),$$

and it is the one that causes the excitation of the molecules and the phasor of this current density is co-linear with the phasor of the electric field intensity – Fig. 5, so as the phasors of the field and the thermionic emission current densities.

The reactive displacement current is capacitive current and its absolute value is as follows:

$$j_{Dreac} = \varepsilon_r\cdot\varepsilon_0\cdot\frac{dE(r_x,t)}{dt}\cdot\cos\delta \quad (34)$$

Therefore the absolute value of the apparent displacement current density is:

$$j_{Dapp} = \varepsilon_r\cdot\varepsilon_0\cdot\frac{dE(r_x,t)}{dt} \quad (35)$$

The damping sinusoidal anode-cathode voltage /7/, which is the response of the circuit in Fig. 4 on the switch off manoeuvre, is applied, and hereby the electric field intensity has the same shape and frequency as the anode-cathode voltage:

$$\hat{u}_{\alpha\kappa}(t) = -1\cdot U_C\cdot e^{-\alpha\cdot t}\cdot e^{1\cdot(\omega_0\cdot t-\zeta-\xi)}+U_g \quad (36)$$

A phase angle ζ due to $U_C(0)$ and $I_L(0)$ and a phase angle ξ due to α and ω are equal because the inductance and the capacitance in Fig. 4 have no losses, otherwise the angle ζ is smaller then the angle ξ.

The electric field intensity is according to Eq. (11) equal:

$$E(r_x,t) = \mathrm{Re}\left(\hat{u}_{\alpha\kappa}(t)\right)\cdot\frac{r_{ecc}}{2}\cdot\left(1+\frac{r_{ecc}}{d_{sur}}\right)\cdot$$
$$\cdot\left(\frac{1}{r_x^2}+\frac{1}{(2\cdot r_{ecc}+d_{sur}-r_x)^2}\right) \quad (37)$$

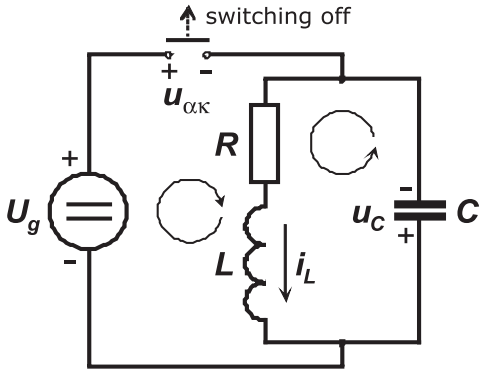

Fig. 4: The electric circuit switched off by the breaking contact.

The time derivative of the anode-cathode voltage is:

$$\frac{d\hat{u}_{\alpha\kappa}(t)}{dt} = U_C \cdot \sqrt{\alpha^2 + \omega_0^2} \cdot e^{-\alpha \cdot t} \cdot e^{\iota \cdot (\omega_0 \cdot t - \zeta)} \tag{38}$$

Using Eqs (32), (37) and (38) the phasor of the displacement current density is obtained:

$$\hat{j}_D(t) = J_D \cdot e^{-\alpha \cdot t} \cdot e^{\iota \cdot (\omega_0 \cdot t - \zeta - \delta)} \tag{39}$$

and further on, its apparent value is:

$$j_{Dapp}(r_x, t) = \varepsilon_r \cdot \varepsilon_0 \cdot \mathrm{Re}\left(\frac{d\hat{u}_{\alpha\kappa}(t)}{dt}\right) \cdot \frac{r_{ecc}}{2} \cdot \left(1 + \frac{r_{ecc}}{d_{sur}}\right) \cdot \left(\frac{1}{r_x^2} + \frac{1}{(2 \cdot r_{ecc} + d_{sur} - r_x)^2}\right) \tag{40}$$

Hereafter the shorter format of the following functions is used:

$$E = E(r_x, t)$$
$$\frac{dE}{dt} = \frac{dE(r_x, t)}{dt} \tag{41}$$

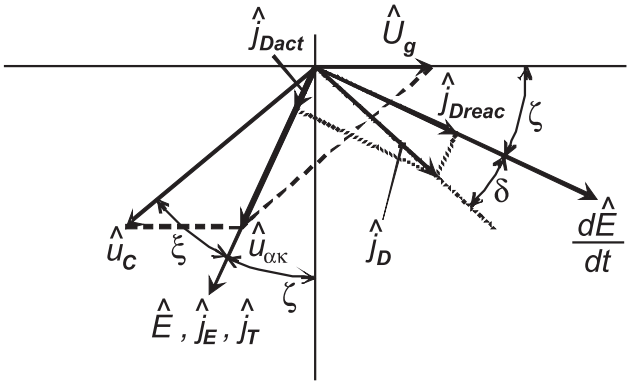

Fig. 5: The principle phasor diagram at t *= 0 and* φ *= 0; not in the scale, because the angles are very small:* ζ *=* ξ *= 0.0055 and* δ *= 0.00016 radians.*

Because the active displacement current causes the excitation of the molecule in the volume between the cathode and the anode, the active displacement energy is the integral of the scalar product of the phasors of the active displacement current and the electric field intensity throughout the volume. Hence, the cosine function of the angle between two phasors is applied, and it is equal to sine function of the complementary angle. So the excitation energy of one molecule in the volume, containing N_m gas molecules, due to the displacement current density is:

$$\begin{aligned} W_{Dact} &= \frac{1}{N_m} \cdot \int_0^t \iiint_{V(N_m)} \hat{j}_D \cdot \hat{E} \cdot dV \cdot dt = \\ &= \frac{1}{N_m} \cdot \int_0^t \iiint_{V(N_m)} j_{Dapp} \cdot E \cdot \sin\delta \cdot dV \cdot dt = \\ &= \frac{1}{N_m} \cdot \int_0^t \iiint_{V(N_m)} \varepsilon_r \cdot \varepsilon_0 \cdot \frac{dE}{dt} \cdot E \cdot \sin\delta \cdot dV \cdot dt \end{aligned} \tag{42}$$

Supposing the electric field is homogeneous in the volume V, which contains N_m gas molecules. The displacement energy in this volume is homogeneous also, which means that its density is equal in the gas molecules themselves and in the hollow volume around them. The displacement energy in the gas molecules causes the excitation of the molecules, so this part of the displacement energy is active. The displacement energy in the hollow volume is reactive. To obtain the homogeneous electric field, the smallest volume $V = V(1)$ has to be taken, and this is such one that contains only one gas molecule under the constant thermodynamic conditions of the gas. Hence, this volume must be the greatest one to be equally distributed among all N_m gas molecules. Further on, the active displacement energy of one molecule is defined under the following condition $V_m << V(1)$ by:

$$\begin{aligned} W_{Dact} &= \lim_{V(N_m) \to V(1)} \left(\frac{1}{N_m} \cdot \int_0^t \iiint_{V(N_m)} \varepsilon_r \cdot \varepsilon_0 \cdot \frac{dE}{dt} \cdot E \cdot \sin\delta \cdot dV \cdot dt \right) = \\ &= \int_0^t \iiint_{V(1)} \varepsilon_r \cdot \varepsilon_0 \cdot \frac{dE}{dt} \cdot E \cdot \sin\delta \cdot dV \cdot dt \approx \\ &\approx \int_0^t \iiint_{V_m} \varepsilon_r \cdot \varepsilon_0 \cdot \frac{dE}{dt} \cdot E \cdot dV \cdot dt \approx \int_0^t j_{Dapp} \cdot E \cdot V_m \cdot dt \end{aligned} \tag{43}$$

Taking into account Eqs (17), (20), (23) and (25), the electron kinetic energy just before the collision with the gas molecule is:

$$W_{ek} = e \cdot E \cdot \lambda + W_{ek\_on} \tag{44}$$

This equation forms the calculation loop with Eq. (12), but the mathematical process converges, and the result uniformly exists.

The mathematical model of the electric discharge in gases has to take into account both, the kinetic energy of the electrons and the energy of the displacement current. The electron kinetic energy is partly transferred to the gas molecule by the electron impact, and causes the ionization or the dissociation, discussed heretofore. In this case, the ionization is considered as the impact ionization although it is more probable that the ionization is done through the excitation of the gas molecule on its higher energy level /5/. The dissociation of the two-atom molecule just cannot be carried out directly by the electron impact due to

the large difference of the electron mass and the dissociated atom mass – Eq. (27). The dissociation is completed by the excitation energy of the two-atoms molecule due to the impact energy when raised in such extend that the dissociation energy level is achieved. This is the dissociation due to the conductive current. The displacement current energy also affects the gas molecules, and also causes their ionization and their dissociation. Because it has no carriers, the ionization and the dissociation are caused by the excitation of the gas molecule with no impact, but only due to the displacement current. All these processes: the impact ionization, the dissociation due to the conductive current, the ionization and the dissociation due to the displacement current have the same mechanism of being completed – the excitation of the molecule on its higher energy level, and afterwards the accomplishment of the process. Therefore the kinetic energy Eq. (44) and the displacement energy Eq. (43) are summarized in the excitation energy of the gas molecule, which is the active energy:

$$W_{exm}(r_x,t,T,W_{ion},W_{diss}) = e\cdot E(r_x,t)\cdot\lambda(T) + \\ + W_{ek\_on}(W_{ion},W_{diss}) + \\ + \int_0^t \varepsilon_r\cdot\varepsilon_0\cdot\frac{dE(r_x,t)}{dt}\cdot E(r_x,t)\cdot V_m\cdot dt \qquad (45)$$

This equation is in the calculation loop with Eq. (18) but the calculation converges.

The excitation energy is calculated by Eq. (45), and the minimal value of the excitation energy is graphically represented by the diagram in Fig. 6. The minimal value of the excitation energy is the one without the carry-on kinetic energy of the colliding electron. The gas used in this calculation is oxygen. The highly ionized range begins closely to the electrode and ends where the minimal value of the excitation energy decrease under the value of the ionization energy. The number of the ionized molecules is constant due to the radius and its level is hundred percent of molecules. This range comes out as corona. Closely to it, the partly ionized range begins where the minimal value of the excitation energy is lower than the ionization energy and higher than the dissociation energy, but the carried-on kinetic energy raises the excitation energy on a higher energy level than the ionization energy. It ends where the minimal value of the excitation energy decreases under the dissociation energy because the carried-on kinetic energy is not sufficient to raise the excitation energy on the ionization energy level. The number of the ionized molecules decreases to zero. The number of dissociated two-atom molecules increases up to hundred percent level. In the non-ionized range, where the minimal value of the excitation energy is under the value of the dissociation energy and the carried-on kinetic energy raises the excitation energy up to the dissociation energy level. The number of the dissociated molecules decreases, but the number of the unaffected molecules increases with the radius near centre of the cathode-anode gap.

If the anode-cathode voltage increases, the non-ionized range in Fig. 3 narrows, and the partly ionized range from the cathode side touches the partly ionized range from the anode side, and the ionized path between the electrodes arises, the electric breakdown occurs and the electric discharge arc takes place. Consequently the definition range of the percentage of unaffected molecules, which is on the abscise of the diagram in Fig. 6, limits to zero, and the percentage of the ionized molecules is above zero throughout the whole abscise range. This change in the mathematic functions of the percentage of the ionized and of the unaffected molecules means the establishment of the ionized path between the electrodes.

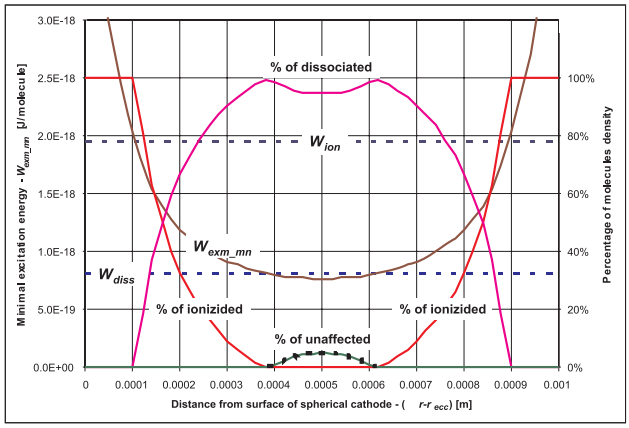

Fig. 6: The minimal excitation energy of the oxygen molecule versus the distance from surface of the cathode to any point at φ = 0 towards the anode, and the percentage of the oxygen molecules density at the input-output quantities in Tab. 1.

The simulation was carried out with the spherical cathode and anode with the radii of 0.5 mm, and with the surface-to-surface distance of 1 mm between them. The excitation energy in comparison with the first ionization, and with the dissociation energy of the oxygen molecule, and further on, the density of the ionized, the dissociated and the unaffected oxygen molecules are shown in Fig. 6. The input and output quantities of the spark gap discharge model are numerically stated in Tab. 1.

When discussing the electrical breaking contact, its contact members are the electrodes. The distance between them increases from zero, when the breaking contact still holds the closed position, up to the maximum value. In the model, the distance of 1 mm is used because the Paschen law minimum is being avoided. The Paschen law is described by the family of functions of the breakdown voltage of the spark gap depending on the product of the gap length and the gas pressure, but the functions differ by the chemical composition of the gas medium in the gap. These functions have minima: 450 V at 9.2 μm with oxygen, 251 V at 8.8 μm with nitrogen, and 327 at 7.5 μm with air at the same pressure 101.325 kPa in all three cases /8/. At the distances lower than the ones of the minima, the break-

Tab. 1: The input-output table of the spark gap discharge model of oxygen and nitrogen molecules at the same environmental conditions; the variables of the functions are (r, φ, t).

medium	O_2	N_2	
cathode	Ag	Ag	
W_{ion}	1.955	2.464	aJ/ particle
W_{diss}	0.816	1.266	aJ/ particle
r_0	0.500	←	[mm]
d_{sur}	1.000	←	[mm]
T_{amb}	293.15	←	[K]
p	101.325	←	[kPa]
U_g	220	←	[V]
R	3.75	←	[kΩ]
L	11.0	←	[H]
C	94.0	←	[pF]
t_0	17.0	←	[μs]
$U_{\alpha\kappa}(t_0)$	10.126	←	[kV]
$j_{Dact}(r_{ecc}, 0, t_0)$	1.49	1.21	[mA/m^2]
$j_{Dreac}(r_{ecc}, 0, t_0)$	9.55	←	[A/m^2]
$(j_E + j_T)@(r_{ecc}, 0, t_0)$	6.78	←	[A/m^2]
$dE/dt(r_{ecc}, 0, t_0)$	1.08	←	[TV/m/s]
$E(r_{ecc}, 0, t_0)$	20.3	←	[MV/m]
$E(r_{ecc}+ d_{sur}/2, 0, t_0)$	6.75	←	[MV/m]
T	467	531	[K]
d_{diss_B}	0.11	0.07	[mm]
d_{ion_E}	0.39	0.17	[mm]
non-ionizied gap	0.22	0.66	[mm]
voltage of non-ionizied gap	1.51	5.16	[kV]
ionized	38%	21%	
dissociated	61%	63%	
unaffected	1%	16%	

down voltages are higher than minimal voltages, and with the distances above, the breakdown voltage increases nearly linearly; greater the distance is, more linear the function of the breakdown voltage is. Hence the cathode-anode distance of 1 mm is used in modelling the spark gap phenomena. The Paschen law is also explained by this model: there is a cathode-anode distance at which the majority of the electrons do not achieve enough kinetic energy by moving along the electric field lines to ionize the gas molecules by their impact; and when this cathode-anode distance shortens, it is comparable with the mean free path of the electron, and therefore there is a very small number of impacts; further on the electric field intensity has to be increased, and hence the anode-cathode voltage, to obtain such electron kinetic energy to excite the gas molecules up to ionized state. The increased anode-cathode voltage is needed with the cathode-anode distance decreased under the certain value, which defines the minimum of Paschen's voltage function. But, this phenomenon is not incorporated in the model because it is no need to be included with the spherical electrodes. The electric field lines between two opposite charged spherical electrodes arise from the anode and sink at the cathode, virtually as their eccentric points are charged. The length of the electric field lines vary from the value of the electrodes surface-to-surface distance to the infinite value and depends on the angular coordinate φ, as it is defined in Fig. 2.

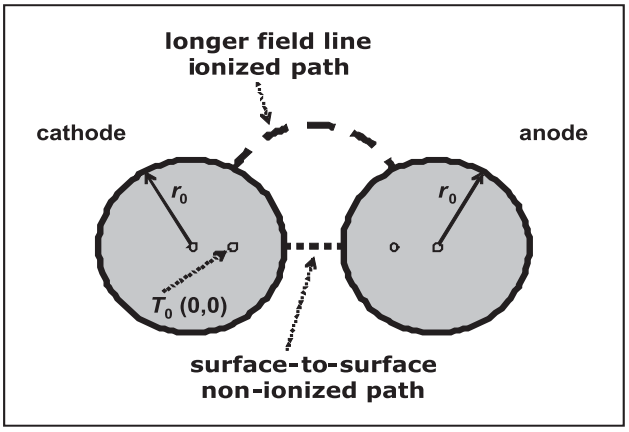

Fig. 7: The formation of the ionized path at the very narrow electrodes surface-to-surface distance.

If the electrodes surface-to-surface distance is too small to establish the electric breakdown, the ionized path is formed along the other longer electric field line – Fig. 7. Hence, dealing with the spherical electrodes, the breakdown voltage and its corresponding path length are always equal or greater then their respective values of the Paschen voltage minimum.

3. The electric arc measurements

The measurement of the discharging arc was carried out, when the air coil, represented by the equivalent electric circuit of the conceptual concentrated electric elements in Fig. 4, was switched off by the breaking contacts of silver. The infimum arc voltage of silver is 12 V and its infimum arc current is 400 mA /9/. The load current was 60 mA, so the drawn arc was unable to be established /1/. The discharging arc began at the instant of 2.4 ms as shown in Figs 8 and 9 when the current dropped towards zero as seen on the oscilogram in Fig. 9.

The time derivative of the current induced the overvoltage, which caused the electric breakdown and the discharging arc was ignited. The arc voltage was 270 V at the beginning and 440 V at the end. Its duration was 2.4 ms.

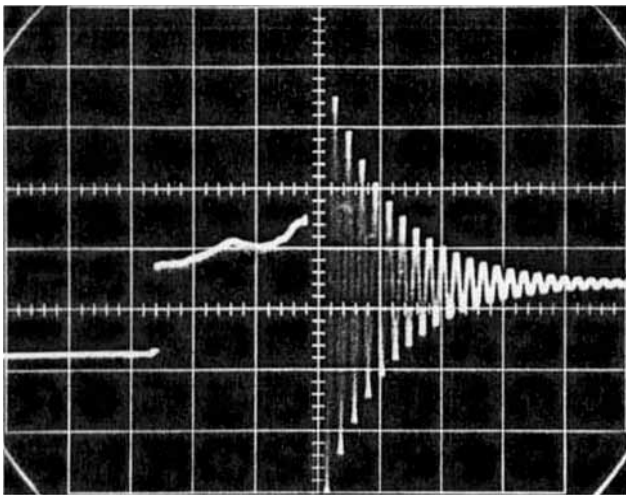

Fig. 8: The discharging arc voltage breaking the inductive load represented by RLC circuit in Fig. 4 and Tab. 1 at the voltage scale 200 V/div. and at time scale 1 ms/div.

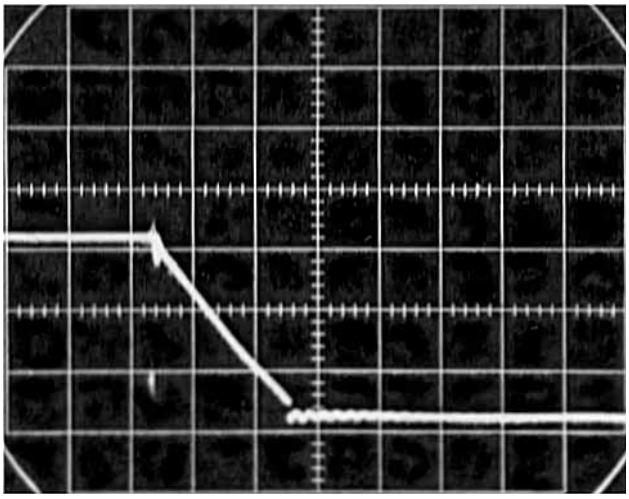

Fig. 9: The discharging arc current breaking the inductive load represented by RLC circuit in Fig. 4 and Tab. 1 at the current scale 20 mA/div. and at time scale 1 ms/div.

To compare the discharging arc with the drawn arc, the latter one was measured too.

The electric contact under the measurement was the commutator sliding contact with the brush of carbon and the commutator bar of copper. In this combination, the carbon infimum arc voltage prevails over the copper one, but the contrary is with the infimum arc current /1/. The infimum arc voltage of carbon is 20 V and its infimum arc current is 30 mA, and 13 V and 430 mA respectively for copper /9/. The drawn arc ignited at the instant of 24 µs as shown in Fig. 10. The arc voltage was around 20 V throughout the arc duration, and the current was continuous at the instant of ignition. The load was inductive since it was a dc commutator motor. The sliding contact was moving from holding to breaking operation during the arc, which is seen at the end of the drawn arc as a slight overvoltage.

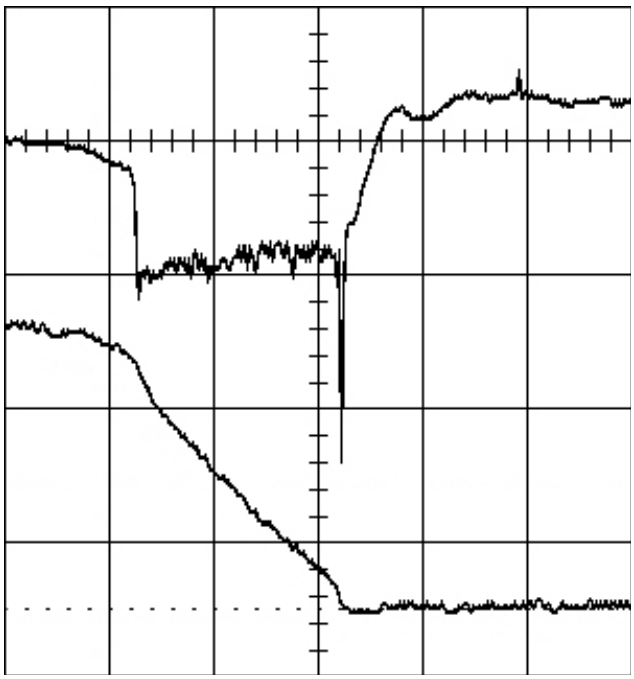

Fig. 10: The drawn arc voltage (upper diagram) and current (lower diagram) of a sliding contact of a commutator with an inductive load at the voltage scale 20 V/div. and the current scale 0.5 A/div. and at time scale 20 µs/div.

The differences between the discharging and the drawn arcs are clearly seen by the comparison of the oscilograms and the data of both arcs including the contact material properties concerning arcs.

4. Conclusions

Understanding the process of the discharging arc ignition and of the drawn arc also /1/, the arc avoiding and the arc extinguishing methods are established and same old methods are proved to be effective. Some of them are following:

- avoiding the discharging arcs by electric contacts in vacuum because there are no medium to be ionized;
- avoiding the discharging arcs and the drawn arcs also by the wetted electric contacts, which enable wider initial contacts gaps than solid contacts;
- avoiding the discharging and the drawn arcs by capacitance parallel to inductive loads to minimize the displacement current and the peak value of the overvoltage;
- avoiding the discharging and the drawn arcs by capacitance parallel to the electric contacts to bypass the contact current;
- extinguishing the discharging and the drawn arcs by the application of magnetic field perpendicular to the electric field lines in the contact gap to lengthen the path of the electron flow.

There is also the principle of avoiding the drawn arcs, which works effectively just with this kind of arcs, and it is based on the right selection of contact materials /1/, /2/.

5. Used symbols

The symbols used with complex scalars, phasors and vectors of appropriate quantities:

$\breve{a}, \breve{A}$ ... complex scalar a, A

$\hat{a}, \hat{A}$ ... phasor a, A

$\vec{a}, \vec{A}$ ... vector a, A

a, A ... absolute value a, A – dc or peak; small letter is instantaneous value

The symbols used with quantities:

$\vec{1}_\varphi$ ... angular unit vector

$\vec{1}_r$ ... radial unit vector

$\vec{1}_x$ ... radial unit vector at $\varphi = 0$

α ... damping factor of series RLC circuit

β ... enhancement factor of electric field intensity

δ ... losses angle

ε ... permittivity of the dielectric substance

ε_0 ... permittivity of vacuum

ε_r ... dielectric constant

ζ ... phase angle due to $U_C(0)$ and $I_L(0)$

ι ... square root of (-1)

λ ... electron mean free path

μ ... factor between rest and effective electron mass

ξ ... phase angle due to α and ω_0

υ ... decreasing factor of work function

φ angular coordinate

ω_0 ... natural resonant frequency of series RLC circuit

c ... light velocity in vacuum

C ... capacitance

d_{diss_B} ... electrode surface to begining pointof dissociation

d_{ion_E} ... electrode surface to ending point of ionization

d_{sur} ... electrodes surface-to-surface distance

e ... elementary charge

E ... electric field intensity (also instantaneous value)

E_φ ... angular component of electric field intensity

E_r ... radial component of electric field intensity

E^* ... enhanced electric field intensity

e^x ... exponential function

h ... Planck constant

$I_L(0)$ ... inductance current at $t = 0$

j_D ... displacement current density (instantaneous value)

j_{Dact} ... active displacement current density (instantaneous value)

j_{Dapp} ... apparent displacement current density (instantaneous value)

j_{Dreac} ... reactive displacement current density (instantaneous value)

j_E ... current density due to cold emission (instantaneous value, conductive current)

j_T ... current density due to thermionic emission (instantaneous value, conductive current)

J_D ... displacement current density (peak value)

k ... Boltzmann constant

K ... coefficient of conveyed and conducted thermal energy

L ... inductance

m_e ... rest electron mass

m_e^* ... effective electron mass

m_m ... rest molecule mass

N_A ... Avogadro number

N_m ... number of molecule

p ... gas pressure

P_i ... ionization probability

Q ... electric point charge

r ... radial coordinate

r_α ... radial coordinate from anode eccentric point

r_0 ... electrode radius

r_{ecc} ... eccentric electrode radius

r_x ... radial coordinate at $\varphi = 0$

R ... resistance

R ... general gaseous constant in Eq. (15)

Re() ... real component of compex scalar or phasor

t ... time

t_0 ... time of observation in Tab. 1

T ... gas temperature

T_κ ... cathode temperatrure

T_{amb} ... ambient temperature

$u_{\alpha\kappa}$ ... anode-cathode voltage (ac, instantaneous value)

u_C ... capacitance voltage (ac, instantaneous value)

U ... voltage, potential (dc)

$U_{\alpha\kappa}$ ... anode-cathode voltage (dc or peak value)

U_C ... capacitance voltage(dc or peak value)
$U_C(0)$ ... capacitance voltage at $t = 0$
U_g ... dc generator voltage
v_e ... instant electron velocity
v_m ... instant molecule velocity
v_{e_avg} ... average electron velocity
v_{m_avg} ... average molecule velocity
V ... volume
$V_{\phi\kappa}$ ... work function voltage
$V_{\phi\kappa}^*$ ... decreaced work function voltage
V_m ... molecule volume
$V(N_m)$ ... volume of N_m molecules under the same thermodynamic conditions
W_{diss} ... dissociation energy per molecule
W_{ek} ... electron kinetic energy
W_{ek_on} ... electron carried-on kinetic energy
W_{exm} ... molecule excitation energy
W_{ion} ... energy of 1st ionization per molecule
W_{mk} ... molecule kinetic energy

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MOBILE PAYMENTS – DESIGN OF NEW TERMINAL

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Key words: Mobile payment, GSM, Voice, Terminal

Abstract: Mobile phones and mobile access to internet are creating new space for challenges and ideas in companies business. And today's electronic revolution in electronic payments is promising even more mobile involvements in money. Mobile phones are far from just a device for communication with other people. They are overtaking functionalities of camera, personal computers, media players and others devices. But most of all mobile phones are also used for mobile payments. Because of great inquiry for mobile payments, different technologies were developed. Company named Ultra d.o.o. has developed new mobile transaction system. Data transmission is transmitted over the speech channel of different mobile communication systems such as GSM, CDMA and UMTS. Ultra d.o.o. has already obtained two international patents for this type of transmission. The basis of this mobile transaction system is voice-coded data transmission between the transaction authorization processing centre and the terminal.

The system is generally designed for two types of terminals; the mPOS and aPOS, which are meant for different applications. The terminal is a device which works similarly like a POS terminals.

In today's world there are increasing demands for mobile transaction systems that would enable a palette of services, portable, light, small, ergonomically designed and enabling different transaction technologies, all in one device. Demands like that have brought to new terminal concept, which we describe in this article. The main aim of the article is to present the transfer procedure form idea to practical realization and inside of this the technical evolution of electronic device-terminal which is a crucial part of the invented transaction system.

Mobilno plačevanje – razvoj sodobnega terminala

Kjučne besede: Mobilno plačevanje, GSM, POS, terminal

Izvleček: Mobilni telefon postaja nepogrešljiv del vsakdanjih opravil. V povezavi z drugimi tehnologijami prevzema tudi funkcionalnosti drugih naprav, na primer fotoaparata, dlančnika, mp3 predvajalnika… Vse močnejši trend mobilnih telefonov postaja uporaba mobilnega telefona za plačevanje. S porastom zanimanja za mobilna plačevanja so se in se še vedno razvijajo najrazličnejše tehnologije, ki omogočajo hitro, enostavno in prijazno mobilno plačevanje.

Podjetje Ultra d.o.o. je razvila lastno tehnologijo mobilnega plačevanja, ki temelji na osnovi prenosa zvokovno moduliranih podatkov po govornem kanalu različnih mobilnih omrežij. Glede na različne plačilne storitve in uporabo, sta se razvila dva tipa terminalov in sicer aPOS ter mPOS.

V sodobnem času se kažejo čedalje večje zahteve po POS napravah, ki bi omogočale široko paleto najrazličnejših servisnih storitev. Zraven tega morajo biti še prenosne, lahke, majhne, čim dalj časa avtonomne, ergonomsko oblikovane, hkrati pa bi omogočale uporabo različnih tehnologij plačevanja. Takšne zahteve so pripeljale do novega razvoja terminala, ki ga opisujemo v tem članku.

1. Introduction

Mobile businesses and mobile internet access are creating new challenges for business operations in all lines of business. The present-day electronic revolution in electronic payments is promising an enhanced role of electronic money in modern life. Mobile phones have long ago stopped being a mere communication device, but are now also assuming functions of cameras, computers, palms, media players etc. For an increasing number of users they also represent a mean of payment. Due to an increasing interest in mobile payments different technologies (SMS, GPRS, RFID etc.) providing such services have been developed.

The company Ultra d.o.o. has developed its own technology based on data transmission through a speech channel of different mobile networks, such as GSM, CDMA and UMTS /1/, /2/, /3/. The abovementioned mean of data transmission is enabled by a system with two international patents.

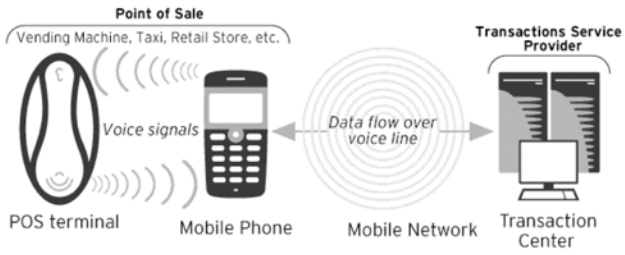

Fig 1: The basic principle of system operation.

The advantages of the mentioned payment-technology system against others make further developing sensible. These advantages are the following:

- Passive communication terminal: all transmitted and received data travels through a speech channel of the user's mobile phone.
- The use of technology is independent of the mobile phone standard or mobile network. All mobile phones include the primary function of transmitting and receiving speech.

Contemporaneity shows an increasing demand for POS devices that would enable a wide range of different services, such as payments, deposits into pre-subscriber accounts, bonus-points program etc. In addition they should be portable, light, small, autonomous for as long as possible and ergonomically designed. Support of other payment technologies is also needed to compete with existing terminals, so that a single terminal would enable different payment technologies, which is friendlier for the users as well as merchants, who already have too many different terminals at the pay points, which causes a certain degree of confusion. Such demands resulted in an advanced terminal, described in this article.

The article first presents the development of an advanced terminal, and development of terminal's external design, development of printed circuit and development of testing technologies are presented respectively. In the following chapter the overall functionality and the structure of the terminal are described. Applied wireless communication devices are presented next. Special chapters are devoted to terminal protection as well as data transmission through mobile network's speech channel. As final comes a chapter on the concept of the software part, which unites the aforementioned parts of the terminal.

2. Development of the terminal

2.1 The development of the external design

External design was developed gradually in CAD (computer-aided design) software environment /5/, /6/. The terminal has to be small, portable and ergonomically designed. It also has to take into consideration many other factors. The basic functionality of the terminal are mobile phone payments. Because of that the acoustic set has to be as adapted as possible for best data transmission between individual microphones and speakers. The design is also defined by different card slots, connectors for outside world connections and the size of the screen, keyboard, printer, speaker, microphones and other major components of printed circuit. Fig. 2 shows successive modifications of the external design with regard to the mentioned demands.

Further development of the terminal's design takes into consideration additional modifications that appear after the first tests of the acoustic set of the new terminal. Acoustics test is done on the casing, made with stereolitography technology. Extra deviations due to different plastic matter and accordingly different acoustic characteristic are taken into consideration. At the same time an additional layer of soft rubber is applied on the top casing, to prevent mobile phones from sliding of the terminal. The development of printed circuit was parallel to the development of the external design of the terminal. Because of that the external design was modified simultaneously according to smaller or larger modifications of the printed circuit. Fig. 3 shows the final external design of the terminal on a dock station, which is often used with the terminal.

2.2 Development of printed circuit

The development of printed circuit was parallel to the development of the external design of the terminal. Planning of printed circuit was done in three software environments. Planning of the circuit scheme was done in one software environment, planning of PCB (Printed Circuit Board) in another, and three-dimensional planning of the circuit and all electronic components was done in the third CAD software environment /5/, /6/, /7/. All three software environments are interconnected, so that for example a change of position of one of the electronic components in software environment for PCB composition reflects in the change of position in CAD software environment. This way the entire development is done in software environments and there is no need to create intermediary printed circuits to examine compatibility with the terminal's casing.

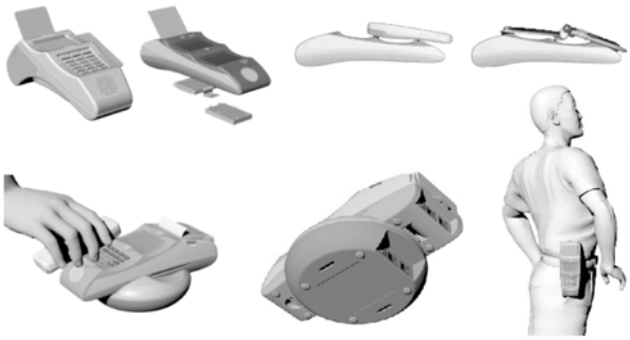

Fig 2: Gradual development of the external design of the terminal.

Fig. 3: The final design of the terminal with dock station

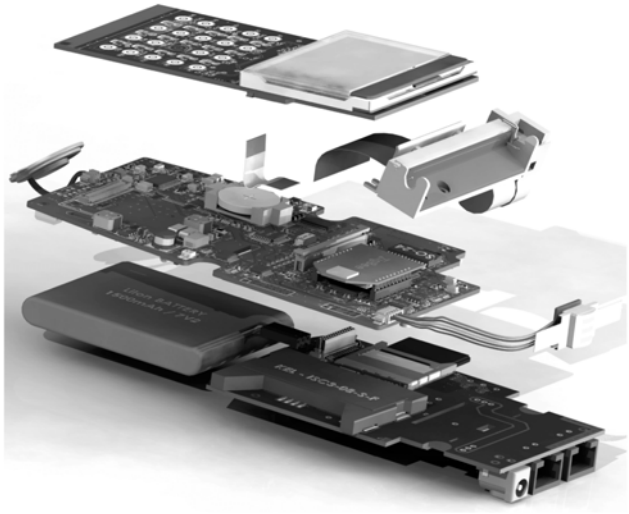

Fig. 4: The electronic part and the printed circuit of the terminal.

The electronic part of the terminal is roughly divided into 6 separate parts as follows (Fig. 4):

- Primary printed circuit includes:
  - central processing unit,
  - external memory units,
  - power management circuit.
- Secondary printed circuit includes:
  - screen and a keyboard
  - an antenna and RFID communication circuit,
  - a codec for collecting and producing sound.
- Lower printed circuit includes:
  - power connector
  - RJ45 connectors
  - SD connector
  - smart card connector, etc.
- Magnetic head for cards with a magnetic record,
- Printer
- Battery
- Speaker and microphones

With three-dimensional planning of printed circuit every used component needs to be transferred into CAD software environment. For some components manufacturers provide three-dimensional information, for the rest we provided them ourselves.

A part of creating printed circuit is testing PCB /4/. Considering that all printed circuits were planned also in CAD software environment we could also use the latter for easier planning of the testing device for PCB test. The mentioned choice of planning includes several advantages against standard methods of planning. One of them is also simpler preparing of test needles holes. With such planning a testing device can be created even before the first prototype of the printed circuit is made. By projecting printed circuits or marked testing points onto the lower testing board documentation on exact measures of the drilled openings as well as on other important information, such as end-height of individual components and suchlike can be sent to the manufacturer of testing devices.

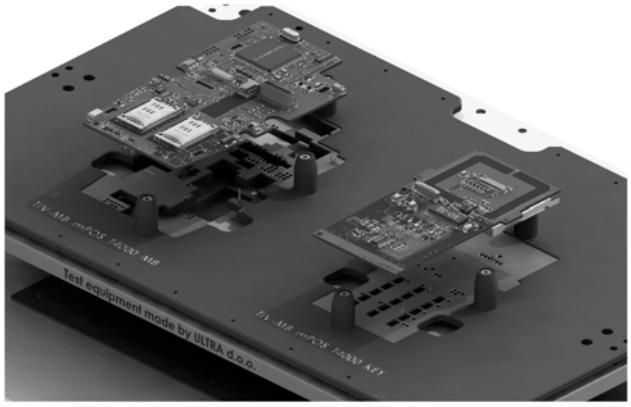

Fig. 5: A testing device for terminal printed circuits

3. Functionality and the structure of the terminal

The basic functionality of the terminal is performing different types of transactions. These can be carried out in different ways, since the terminal supports different technologies of user-identification (RFID tag, magnetic-stripe card, smart card and mobile phone's MSISDN) as well as different ways of communication with the centre like data transmission through a speech channel of a mobile network, GPRS, Ethernet wire technology, ZigBee. The choice of individual communication channel depends on the price of data transmission, the speed of data transmission and the location of the use of the terminal.

Besides the basic functionality, the terminal also provides others. We will only mention a few more important ones. The terminal enables distance maintenance or replacement of the software part of the terminal, display of different transaction extracts (reports, account, duplicate) on the screen and on paper via printer, portability of the terminal – battery and recharging option, corresponding display and a simple user-interface, transmitting or producing voice instructions, protection of the terminal against unwanted intrusion. For the sake of all the mentioned functionalities the terminal is constructed in several parts/sets:

- digital signal processor (FLASH and RAM)
- memory components (EEPROM, SD card etc.)
- circuit for protection against unwanted invasion
- power management circuit,
- battery
- connectors,
- keyboard,
- screen,
- printer,
- wireless technologies (RFID, GPRS, ZigBee),

- RTC (real time clock),
- smart card for ECC cryptography.

Fig. 6 and fig. 7 show individual sets and the basic structure of the terminal.

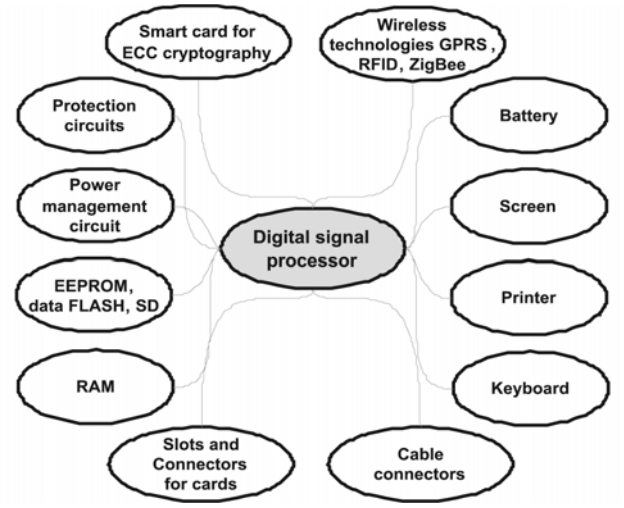

Fig. 6: The important sets of the terminal.

3.1 Central processing and external memory units

The central processor of the terminal is a 32-bit DSP (digital signal processor) TMS320F2812 made by company Texas Instruments, which has integrated peripheral buses. These directly support SPI, SCI, AD, PWM, QEP, McBSP CAN etc. The mentioned DSP supports 16x16 and 32x32 MAC (Multiply and Accumulate) operations and 16x16 double MAC operations. The core of the DSP runs with a frequency of 150 MHz and achieves the capacity of 150 MIPS (Million Instructions per Second). All the abovementioned characteristics are necessary for real-time processing of different operations performed by the terminal:

- FFT (Fast Fourier Transformation) and IFFT (Inverse FFT),
- filtering of individual carrier frequencies,
- encryption and decryption of data,
- BEC (Backward Error Correction),
- FEC (Forward Error Correction),
- GUI,
- ….

TMS320F2812 digital signal processor has an integrated internal FLASH and RAM for storing and processing program code and data. The following memory units that serve different purposes are connected directly to DSP: external static RAM, serial FLASH, EEPROM, additional alternative SD card and an interface for smart cards.

A version of PCB is saved in EEPROM, which enables easier service as well as proper functioning of one program code on different PCBs. Parameters which determine the functioning of the program code as well as storage of data needed by the terminal when restarted are also saved in EEPROM.

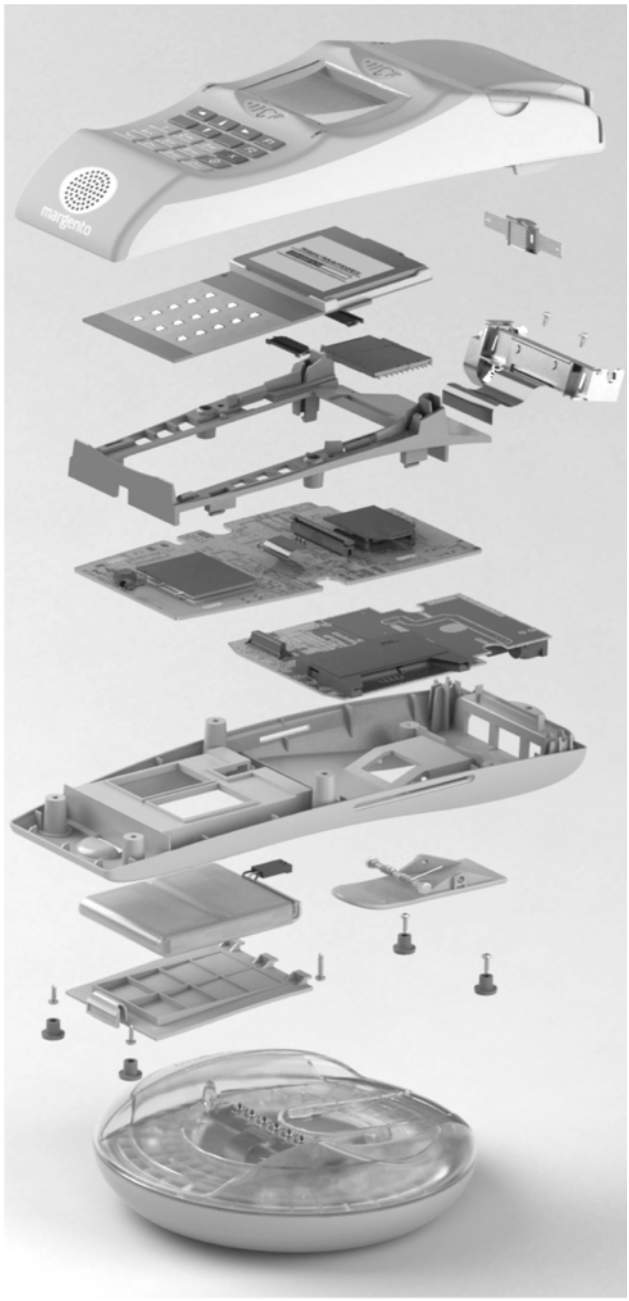

Fig. 7: The structure of the terminal.

Internal and external RAM are used for debugging in the development environment, as well as for storing data and performing individual program algorithms that have to be performed faster (FFT, correlations, filtering etc. using faster internal RAM).

Graphic data records, used for animations, text extracts, screen logotypes and thermal printer logotypes; as well as sound data records for proper signalization are stored in external serial FLASH. The latter is also used for storing transaction data and partial storing of the program code etc.

SD cards are used for storing additional advertising data such as logotypes, animations and larger sound records. At the same time the same input slot is also used for upgrading the terminal with a program card that holds the program code.

Smart card interface has four different functionalities. The first functionality is supporting credit cards for user identification and performing payment transactions. The second functionality is the use of merchant-identification cards. The third functionality is saving sensitive data onto protected cards. The fourth functionality is performed on a separate parallel port intended for alternative use of smart cards for storing cryptographic keys and performing corresponding cryptographic algorithms.

4. Wireless communication

Nowadays many devices use wireless communication, which primarily provides portability of the device. The following wireless communications are used with the terminal:

- ZIGBEE,
- RFID (Radio Frequency Identification),
- GPRS (General Packet Radio Service) and
- transmission of data through a speech channel of a mobile network.

The terminal uses ZigBee for wireless communication between the terminal and the dock station. The mentioned functionality is used only when the dock station is connected to ethernet network or the cash point directly. In this case ZigBee becomes a bridge, that enables indirect connection of the terminal to Ethernet network or the cash point.

RFID wireless communication is used for two different functionalities. Primarily it enables registration before the use of the terminal, which limits access to the terminal only to authorized persons or cards. At the same time the terminal and RFID also enable mobile payments through NFC (Near Field Communication) standard. With this the terminal enables 4 different means of payments, that is:

- smart cards,
- cards with a magnetic record,
- NFC and
- mobile payments with transmission of data through a speech channel of a mobile network.

In individual countries transmission of data through GPRS channel is relatively inexpensive. Apart from GPRS modem the terminal only needs a valid SIM card of a mobile operator. In this case mobile payments are done so that user identification is sent through a voice channel to the terminal, and all other data is sent through GPRS channel. Such transactions are faster and more robust, and the terminal also has the possibility to upgrade larger parts of software, which consequently means easier maintenance of the terminal.

4.1 Communication through a voice channel of a mobile network.

Transmission of data through the voice channel of a mobile network is the most important wireless communication of the terminal. Advantages against others have already been listed in the introductory chapter. Several different problems that prevent high speed of data transmission arise with this method of data transmission. Because of this the terminal includes different systems for correcting and detecting data as well as modified modulations for more robust data transmissions. Fig. 8 shows individual systems in charge of data transmission between the terminal and the centre. Among them is also encrypting and decrypting of data, based on ECC cryptography.

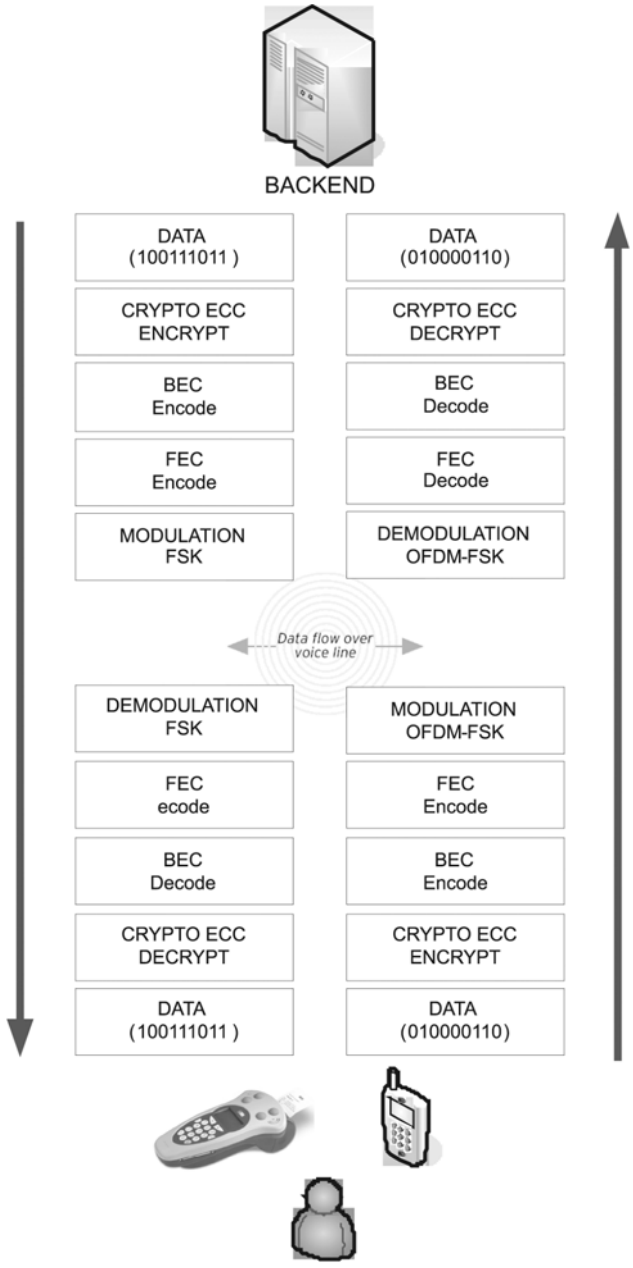

Fig. 8: Provision of robustness of data transmission with different systems or algorithms.

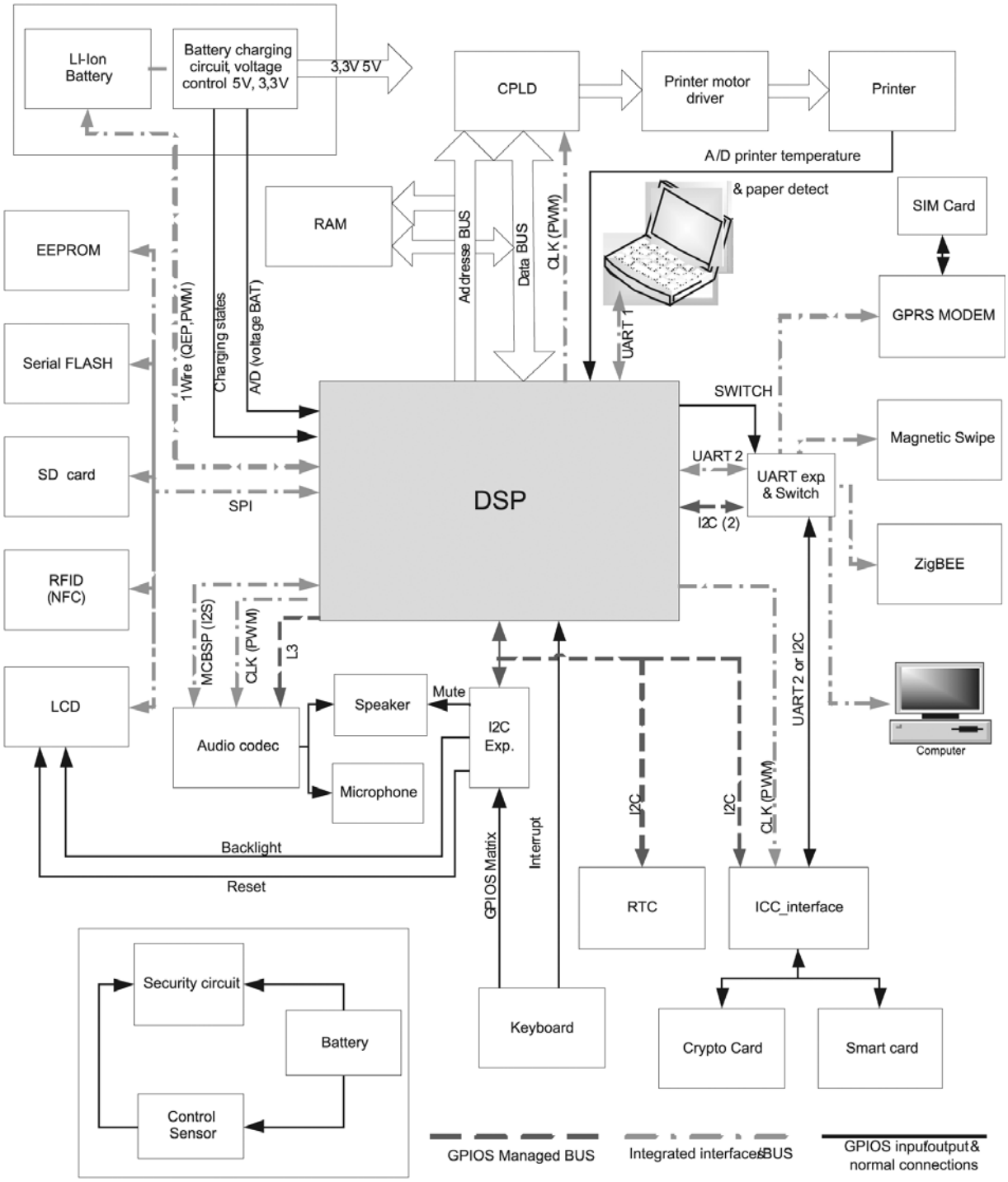

Fig. 9: Block diagram of the printed circuit of the terminal

Center and terminal are communicating in full-duplex mode. Terminal has to simultaneously in real-time perform demodulation and modulation, FEC (forward error correction) decoding and coding, BEC (backward error correction) decoding and coding and ECC encrypting and decrypting of data. For modulations and demodulations adaptive and robust techniques have been developed especially designed for voice coded transmission over speech channels in mobile networks. Those are based on modified OFDM techniques, pilot signals, chirp signals and different advanced channel analysis.

5. Terminal protection

The primary function of the terminal is performing money transactions. Because of this a high level of protection is necessary. Besides the protection of data transmission, protection against unauthorized physical intrusion to the terminal is needed. Protection circuit runs in connection to separate power supply and protection sensors. The mentioned protection must ensure that:

- it is not possible to intercept data running between the keyboard and the processor,

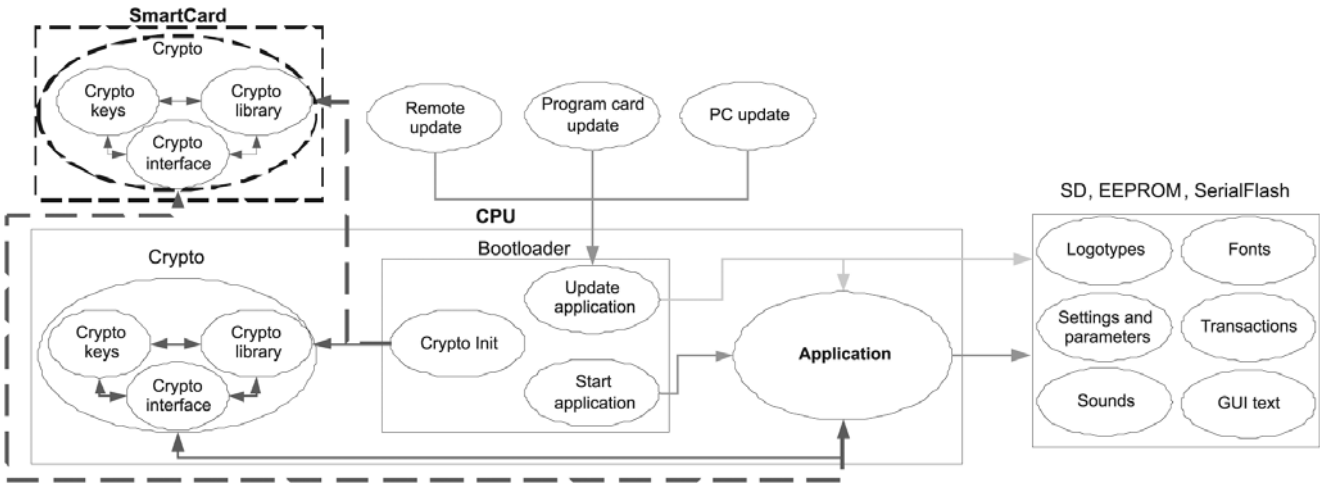

Fig. 10: Block diagram of the software part of the terminal

- it is not possible to intercept data running between the cards and the processor, and
- it detects and promptly reacts in case an unauthorized person tries to open the terminal.

Additional protection of data is provided with a 128-bit key that locks the processor, and at the same time especially sensitive data is saved onto an extra crypto smart card.

6. Software part

Fig. 10 shows a block diagram of the software part of the terminal, which is roughly divided into 4 parts: Bootloader, cryptography, main application and additional data.

Bootloader performs several tasks. At startup it first checks if a program card containing a new application is inserted into the terminal. In this case it updates the application and data in external memory units. In a similar way the terminal can be updated through a maintenance call or directly via PC.

Maintenance call enables distance updating of the application, which means that individual parts or the whole application is sent from the centre to the terminal through a channel that is used by the terminal for communication with the centre at the time. The next task of the bootloader is initialization of cryptography and afterwards startup of the main application. The terminal uses cryptography of elliptic curves ECC that is based on public and private keys / 8/. The cryptography is made up of crypto keys, crypto library and a crypto interface. It can all be done on a locked DSP or on a smart card. The latter has more advantages, among others also easier service of the terminal and disburdening of the DSP.

The main application is the core of the terminal and the largest software part since it connects all the presented components and performs different algorithms in charge of GUI, drivers, protocol and communication level of transactions, reports, wireless communication, saving and reading the data and several other important tasks. All these algorithms are communicating via well known services for synchronization (semaphores, mailboxes, queues etc.), scheduling (multitasking, periodical functions, interrupt manager) and other system services. s communication, storinted components safter that startup of the main application.g cryptgraphig algoritms

7. Conclusion

The presented article describes the development and the implementation of a modern terminal. The terminal provides a wide range of different services, enabling different methods of mobile payments as well as other functionalities that distinguish the terminal in many aspects. The terminal has a unique design that corresponds to the primary functionality, i.e. mobile payments with transmission of data through a speech channel of a mobile network. At the same time the presented terminal is an autonomous and small device that includes a high level of protection against intrusion to the terminal. Communication between the terminal and the centre runs through different wireless and wire technologies, which additionally enables easier integration of the terminal into the existing systems or environments. The terminal is constructed so that printed circuit can be added or modified without changing the external design of the terminal. For further development of the terminal a replacement of the core processing unit with a stronger one is foreseen, and at the same time the development will be in line with compatibility with the existing wire technologies (integration of Ethernet module etc.).

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TELEMETRY AND TELECONTROL OVER TETRA NETWORK

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Key words: Telemetry, Telecontrol, Data Logging, TETRA, PIC microcontroller

Abstract: Geographically distributed systems performing different functions in diverse operational conditions call for interconnection of their components and efficient and reliable remote management using telemetry and telecontrol functionalities in which data and control messages are exchanged. In this paper we present a generic architecture of telemetry and telecontrol systems consisting of a control centre and remote units. We have developed a representative test application comprising telemetry and telecontrol functionalities, making use of the TETRA (TErrestrial Trunked RAdio) network as a communication and interconnection platform. In particular the test application enables temperature at the microcontroller based remote unit to be monitored from the control centre and triggering of a remote alarm. A modular approach enables the remote unit to be connected to various types of sensors and appliances, thus satisfying the diverse needs of applications. The designed platform and the representative test application have been validated using a pilot TETRA network for remote temperature monitoring and public alarm triggering.

Daljinsko merjenje in upravljanje preko omrežja TETRA

Kjučne besede: daljinsko merjenje (telemetrija), daljinsko upravljanje, beleženje podatkov, TETRA, PIC mikrokrmilnik

Izvleček: Prostorsko porazdeljeni sistemi, ki v raznovrstnih pogojih izvajajo različne funkcije, zahtevajo medsebojno povezavo posameznih komponent ter učinkovito in zanesljivo upravljanje s pomočjo funkcionalnosti daljinskega merjenja in upravljanja za izmenjavo podatkovnih in nadzornih sporočil. V tem prispevku je predstavljena splošna arhitektura sistema za daljinsko merjenje in upravljanje, ki vsebuje nadzorni center in oddaljene enote. Prikazana je reprezentativna testna aplikacija, ki združuje funkcionalnosti daljinskega merjenja in upravljanja z omrežjem TETRA (TErrestrial Trunked Radio - prizemni snopovni radio) kot komunikacijsko platformo za medsebojno povezovanje. Testna aplikacija omogoča nadzor temperature na oddaljeni enoti iz nadzornega centra ter proženje oddaljenega alarma. Modularna zgradba oddaljene enote zagotovlja možnost povezovanja z različnimi tipi senzorjev in naprav, s čimer je omogočena uporaba v vrsti različnih aplikacij. Zasnovana platforma in reprezentativna testna aplikacija sta bili potrjeni z uporabo pilotskega omrežja TETRA za oddaljen nadzor temperature in proženje javnega alarma.

1. Introduction

Many applications in consumer and industrial sectors are becoming extensively distributed over a wide geographical region with the need to be monitored and/or controlled from a centrally located supervision point. Some examples include remote monitoring and metering in gas, electric or water billing systems; remote control in building access allowance systems, security and alarm systems, and a variety of healthcare applications. Increasingly important applications, considered in this paper, are systems used in nation-wide protection against natural and man-made disasters, crisis management and disaster relief. Such systems are geographically wide-spread and require extensive infrastructure. Traditionally, the interconnection of remote units has been established using leased lines or other dedicated communication channels, which leads to expensive solutions that are difficult if not impossible to implement in geographically isolated regions. Such systems need to withstand the consequences of various large-scale disasters such as earthquakes or floods, yet in such circumstances wired communication links can easily be broken down. Wireless solutions therefore appear to have a clear advantage for interconnecting a distributed system's components. Different wireless infrastructures have traditionally been used in this context for different services (voice and data), all aimed at assuring reliable and long-range communications. A typical example is depicted in Figure 1, with two different analog radio systems used for voice communication, a specialised radio network used to control and supervise the public sound alarm system, and another radio network used for the paging system.

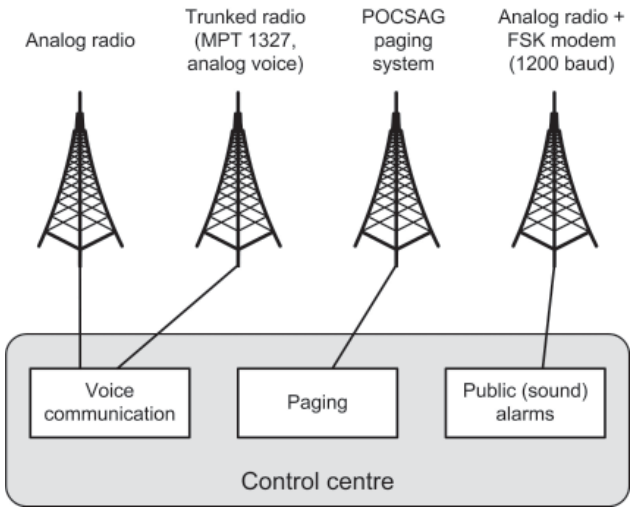

Fig. 1: Traditional wireless infrastructure

With the introduction of Professional Mobile Radio (PMR) systems, which are wireless communication systems designed for dedicated groups of users in specific organizations (e.g. police, army, fire brigades), it has become possible to use a single communication infrastructure for a range of data and voice services. Besides some proprie-

tary solutions, there are two prevailing digital PMR systems: the ETSI standard TETRA (TErrestrial Trunked RAdio) /1/ and the APCO Project 25 /2/. They all offer unified, reliable and secure voice and data communications, simplifying communication infrastructure, its management and maintenance, thus providing a reliable and robust wireless infrastructure for telemetry and telecontrol applications required in crisis management and disaster relief situations.

In general, telemetry and telecontrol systems comprise a set of remote units connected to a control centre using wired or wireless communication links. This paper is focused on telemetry and telecontrol systems based on a wireless network, with the emphasis on their design phase. As an example we have developed a test application for measuring and monitoring temperature at a remote unit and for triggering public alarms. It consists of a purposely designed control centre application and of a microcontroller-based remote unit. The latter has been designed with the idea of developing a modular hardware system whose components could be reused in a host of telemetry and/or telecontrol applications with the minimum number of modifications to the original design, although it is in general impossible to implement a generic platform for all applications.

2. Telemetry and Telecontrol

Telemetry and telecontrol are communication processes that can be defined as follows:

- Telemetry is a process by which automatic measurements and/or other data are collected and processed at a remote object and transmitted to a receiving station for monitoring, analysis and recording.
- Telecontrol is the process of remotely controlling the operation of a distant object's appliances from a control station.

The use of telemetry and telecontrol functionalities has proved useful for a variety of monitoring and control applications in systems distributed over wide geographical areas. They are used to couple remote site sensors (e.g. sensing devices for temperature, pressure, humidity, sound, light intensity, current, voltage, etc.) and remote site appliances (e.g. relays, motors, valves, pumps, lights, alarms) with the equipment controlling the operation of a process. A control centre and remote units are thus the basic components of any telemetry or telecontrol system. Their interconnection can be done using wired or wireless communication links. In either case a typical telemetry or telecontrol system /3/ includes three basic procedures:

- Remote site data acquisition – a process in a telemetry system where a data stream is sampled and the required parameters are measured, and a process in a telecontrol system where an action on a remote site appliance is executed.
- Data transmission – deals with data packaging and transmission in a communication process between the control centre and a remote unit.
- Control centre data analysis – deals with the analysis of data received from remote units in telemetry systems, and with the generation of control commands to be sent to remote units in telecontrol systems.

The telemetry and telecontrol concepts both assume the existence of two way communication in which the systems are trying to communicate using the shortest possible messages, with the interval between them being as long as possible. By this the power consumption of typically battery powered remote units is minimized. Data processing is typically handled by a dedicated application in the control centre, which leads to less complicated and consequently cheaper remote units.

The requirements regarding the importance and the volume of transmitted information in telemetry and telecontrol systems are opposite. In the case of telemetry messages carrying meaningful information are travelling from remote units to the control centre, while messages travelling in the opposite direction are required just for the proper operation of a communication protocol (e.g. request and confirmation messages). In the case of telecontrol, the inverse is the case, i.e. meaningful messages are sent from control centre to the remote units with acknowledgements flowing in the opposite direction. Considering these complementary requirements of telemetry and telecontrol systems it is advantageous to combine both functionalities in a complete distributed automation system, which would offer the monitoring and control capabilities of a remote unit, both from a control centre.

Regardless of wired or wireless communication infrastructure, telemetry and telecontrol systems require autonomous operating scenarios in case the communication link between a control centre and a particular remote unit is broken. This causes the remote units having to be more complex in terms of additional hardware and/or signal processing capabilities. Typically the system's autonomous operation exploits data logging techniques. Data logging is a process of gathering data values generated by a particular system for the purposes of later analysis and/or archiving. The data logger may be described as a device recording a time-sequence of events. In the case of upgrading the telemetry remote units by a data-logging capability, the operation of remote units can be extended to enable a reciprocal state restoration within a control centre, after the communication link is re-established. For the remote unit to offer data-logging functionalities it must additionally contain at least a non-volatile memory bank as a data storage device, with a real-time clock source used to time-stamp the recorded data, thus keeping the track of time and calendar date. Data loggers typically operate in one of two basic modes. The prevalent one is the time-based mode, where in which a data-logger is scheduled to obtain data readings at a given time interval. The other operating mode

is the event-driven mode, in which data-logging is triggered by an external event. Different modes combining these two basic principles are also widely used.

2.1 Applications

Considering the range of sensors that can be used in telemetry systems and the range of appliances suitable to be remotely controlled in telecontrol systems, there is a vast range of applications in which telemetry and/or telecontrol functionalities could be exploited. Currently emerging applications can be classified under consumer, industrial, environmental, and health-care areas.

Typical consumer and industrial applications include burglar alarms, door gate openers, heating, ventilation and air conditioning systems, automated meter reading systems used in consumer billing to take periodic measurements of utility meters, traffic measurement and control systems, etc. Applications of environmental care include weather and seismic monitoring, remote fire supervision, flood prevention, and irrigation control. Recently, telemetry and telecontrol systems are being introduced extensively in healthcare applications, allowing patients that require continuous monitoring to go about their daily business rather than being confined in bed. Heart related requirements, such as electrocardiograms, or blood glucose monitoring in diabetic individuals fall into this category. The limitations of a particular system usually arise from the limitations of the available telecommunication infrastructure, which determine constraints such as the amount of data transmitted per time unit, transmission delay, service interruptions, etc. /4/.

A range of telemetry and telecontrol applications also exploit the data-logging functionalities. The latter are employed in many industrial and environmental applications to enable real-time logging of critical or representative parameters (e.g. temperature, wind speed, barometric pressure). In the field of health-care, data loggers are used to monitor a patient's physiological condition which is then periodically communicated to the medical stuff.

2.2 Test Application

The representative test application described in this paper exploits both the telemetry and telecontrol capabilities with the wireless infrastructure used for the transmission of measurement and control data between a control centre and remote units equipped with external sensors. The remote units also offer an autonomous operation for periods lacking wireless network connection. In such cases a default operation scenario comes into play, with events being time-stamped and logged to a Compact Flash (CF) storage device for later transmission to the control centre. The general system architecture, consisting of control centre, TETRA wireless network and remote units, is depicted in Figure 2.

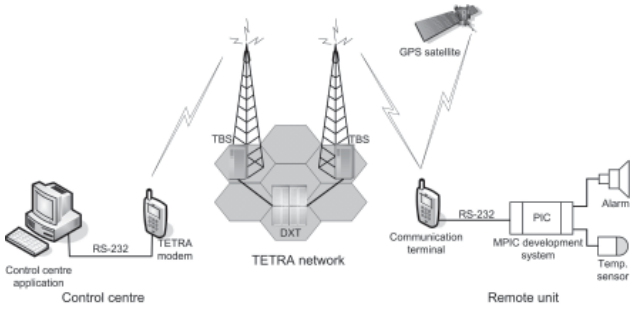

Fig. 2: The wireless telemetry and telecontrol system

The intention of the test application was to demonstrate and validate the following functionalities:

- Transmission of temperature measurement data from a remote unit over a wireless network to the control centre where this data is analysed and stored.
- Sending warning messages from the control centre to remote units where a public alarm system is activated or deactivated.
- Autonomous operation of remote units when remote unit has no network connectivity; the scheduled temperature measurements are stored to a CF storage device for later restoration at the control centre, and public alarms are triggered using the default operation scenario threshold temperature values.

In our system the remote unit application has been structured into two parts, each covering one of the operating modes. The normal operating mode is used whenever the remote unit's TETRA modem is connected to the network, while the autonomous operating mode is used to assure proper operation of the remote unit's basic functions in the absence of connection and to log actions taken for subsequent restoration by the control centre application.

3. Wireless interconnection infrastructure based on the TETRA system

In order to validate the operation of a test application in a robust networking environment suitable for disaster relief conditions, we selected a TETRA network /1, 5, 6/ for the wireless interconnection of the distributed elements. TETRA is an open ETSI standard for digital trunked mobile radio for professional use, featuring fast call setup, group calls, call priorities, direct mode operation, etc. It was developed to meet the needs of the most demanding professional radio users like police forces, fire brigades and rescue teams, army, as well as commercial organizations (power distribution systems, transport systems, etc.)

PMR systems in Europe based on the TETRA standard use RF channels 25 kHz wide, with carrier frequencies around 400 MHz. Although TETRA supports direct communication between mobile stations (as an emergency mode, when no base station is available), normal communication

runs between a base station and a mobile station. TETRA provides duplex communication using FDD (Frequency Division Duplex), with adjacent upstream and downstream transmission bands. By using TDMA (Time Division Multiple Access) with four time slots, each RF carrier provides four communication channels for secure digital voice or data transmission. One communication channel on each base station is reserved for system use as a TETRA control channel.

For data transmission, TETRA provides three different data transmission services:

- Short Data Service (SDS)
- Circuit Mode Data
- Packet Mode Data

SDS provides point-to-point and point to multi-point connectivity for sending short data messages, using the TETRA control channel. Messages can be either status messages with predefined meanings, or user data messages carrying arbitrary user-defined data. They can be of four different types: types 1, 2 and 3 are 2, 4 and 8 bytes long messages respectively, while type 4 are variable-length messages up to 256 bytes long, typically used for text messages. Short Data Service - Transport Layer (SDS-TL) is an extension of SDS type 4, which ensures a reliable transport using connection-oriented communication with handshaking. SDS is suitable for various low data rate applications including telemetry and telecontrol. Its advantage is simplicity of use without the need to implement a complicated communication protocol (e.g. IP protocol).

The Circuit Mode Data service establishes a fixed dedicated data communication channel between a mobile unit and a base station, while the Packet Mode Data service constitutes a fully featured packet data service, which is normally used for IP traffic. It supports packet data transmission in either connection-oriented or connection-less modes. The data transfer rate depends on the selected level of error protection as shown in Table I.

Table1: Data communication speed in TETRA system (one time slot)

Error protection level	Transmission speed [kb/s]
No protection	7,2
Standard protection	4,8
High protection	2,4

Taking into account the communication protocol overhead, the achievable net (application level) bit rate is about 3 kbit/s for the standard protection level. The communication speed can be increased by combining up to four time slots.

To connect data equipment to TETRA terminal (mobile radio stations), TETRA defines a standard interface PEI (Peripheral Equipment Interface), which uses standard asynchronous serial data communication (RS-232) and AT commands.

The pilot TETRA network used in our test application consisted of a digital exchange (DXT), two base stations (TBS), and two mobile radio stations, one in the control centre and the other in remote unit (see Figure 2). The communication terminal at the remote unit served as a TETRA modem to establish a link between the TETRA network and the remote unit, as well as a GPS (Global Positioning System) receiver. Using TETRA PEI interface it was connected to a microcontroller via a serial RS-232 line. Microcontroller received commands from the control centre over the TETRA network, and transmitted measurement data from the sensor to the control centre. SDS type 4 data service, being simple to use and providing sufficient transmission capacity for our test application, was used for the transmission of control and data messages.

4. Control Centre Application

The control centre application is designed to define and control remote units operation, to collect, store and analyze measured data, and to send additional settings and requests to remote units which are dynamically allocated to the control centre active set.

The control centre is composed of a TETRA modem which is connected on one side to the TETRA wireless network and on the other via a wired RS-232 interface to a personal computer running a dedicated telemetry control centre application. As it can be seen in Figure 3, the control centre application is divided into two main parts, the Remote Unit Control and the Data Analysis part.

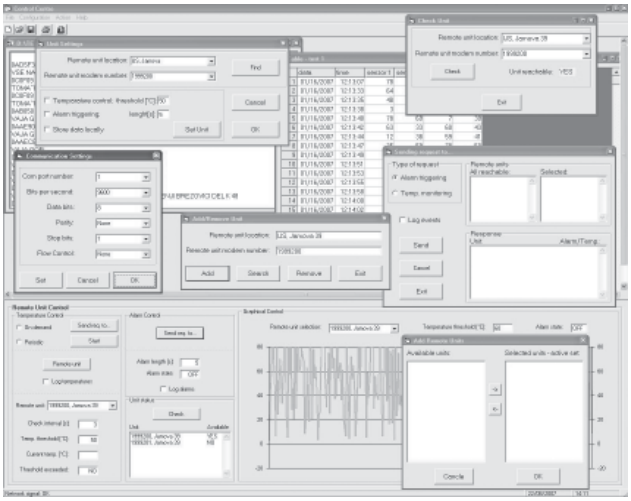

Fig. 3: User interface of the control centre application

When the application is started, the username and password must be entered, restricting the access to the application and consequently to the remote units' settings. Before using the application, the MS Access database of the remote units must be populated. This can be done directly via the MS Access program or using the 'Add/Remove' control in the 'Communication' menu of the control centre application.

In order to communicate with remote units the control centre computer must be connected to the TETRA network via the TETRA modem. The communication settings accessible through the 'Communication' menu must be defined according to the TETRA modem set up, and the RS-232 connection between the modem and the computer must be established. If the control centre is connected to the network (shown in the status bar) and the selected remote unit is accessible, its settings can be modified in terms of control/action type and local storage enabling. In order to check the availability of any remote unit found in the MS Access database the menu bar also provides a command 'Check unit'.

4.1 Data Analysis

The upper part of the application user interface is designed for analysing the measured data and triggered events. It enables tabular representation of the stored measured temperatures and actions with the belonging time stamps. Temperature variation of the selected sensor, stored in the table, can be also presented graphically. Charted graphs can be stored independently or they can be included in the reports designed in the same application.

The application also enables acquiring data from the remote unit which, in the absence of network connectivity, switches to autonomous operation mode. In this case the measured data are stored locally and analyzed by control centre application after establishing TETRA connectivity and restoring data from local storage on the remote unit.

4.2 Remote Unit Control

The 'Remote Unit Control' part of the application is composed of four sections. It helps the user to easily and clearly control and manage implemented test applications, namely temperature monitoring and alarm triggering.

The temperature monitoring is divided into periodic and on-demand execution. In both cases the alarm can be triggered for the predefined time if the temperature threshold defined in the 'Unit Settings' window is exceeded. In the case of periodic temperature measurements the remote units must be added to the active set. This can be done using the 'Remote units' button which opens an 'Add Remote Units' window with the list of the available units. For each selected remote unit the predefined parameters can be shown. The measured data and triggered events can be saved in a predefined text file.

On-demand temperature measurement and alarm control can be triggered using 'Send req. to…' button. It opens an additional window where the type of request is selected (alarm triggering or temperature monitoring), reachable remote units are shown, and the user selected remote units and their responses are noted. All the actions can be written to the user defined log file. The graphical control part is designed for real time graphical representation of the temperature variation on the selected sensor. To be able to present this kind of data the periodic temperature monitoring must be started. The available sensors are members of the remote unit active set.

5. Remote Unit

The core of the remote unit is built around a microcontroller providing sufficient processing capability for the autonomous operation, as well as various communication and adapter interfaces for the connection of communication, sensor, actuator and storage peripherals.

In the design of the electronic system representing the core of each remote unit, the driving idea was to implement a generic modular hardware platform consisting of reusable components that would form the basis for the development of telemetry and/or telecontrol systems. The core has to be simple, relatively small in size, and economical in cost and energy consumption. At the same time it also has to be powerful enough to form the basis of an autonomous system, and highly flexible in terms of being able to adapt to a great variety of applications by making minimal modifications. The success of the platform is thus determined by its flexibility, capacity and overall price.

5.1 Hardware Part

For the remote unit's core to be an open system, offering reconfiguration at a software level, the electronic circuit is based on a microcontroller, with the MPIC development system /7/ being used to develop and verify the test application in our case. However, in the design of an end-market product it would make sense to implement the hardware in such a way that its final function would be defined by attaching application specific add-on modules to the core unit. Together with the proper software configuration the system as a whole would then offer adaptability to a variety of environments being monitored and/or controlled.

The hardware part of the remote unit, depicted in Figure 4, consists of the core and the test application specific hardware. The core hardware comprises only the minimum requisites forming a working system, yet undetermined for a specific application. The basic components forming the core are power supply, a basic microcontroller circuit, and a communication terminal. The power supply in our case was a standard 5 V voltage regulator built around an LM7805 chip. A Microchip PIC16F877A microcontroller /8/ has been used as the heart of the core unit. It is an 8-bit RISC (Reduced Instruction Set Computer) architecture microcontroller operating at a clock input of up to 20 MHz with 8 K of 14-bit FLASH program memory, 368 bytes of RAM data memory and 256 bytes of EEPROM data memory. The package is 40-pin with three 8-bit, one 6-bit, and one 3-bit input/output (I/O) ports. The external peripherals available on these ports include: three timers (8- and 16-bit), two 16-bit capture/compare/PWM (Pulse Width Modulation) modules, 8-channel 10-bit AD (Analog-to-Dig-

ital) converter, analog comparator module, I^2C (Inter-Integrated Circuit), SPI (Serial Peripheral Interface), and USART (Universal Synchronous Asynchronous Receiver Transmitter) communication interfaces. The large number of I/O peripherals makes this microcontroller suitable for a great number of applications, which is especially important due to the fact that we are designing a unified core. Otherwise a more appropriate microcontroller, best fulfilling the performance/price ratio, could be selected for a specific application.

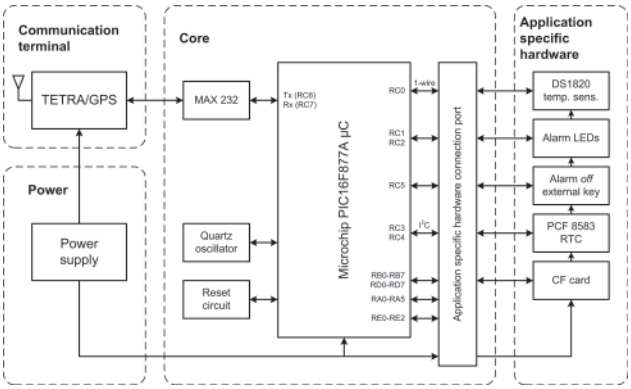

Fig. 4: Block scheme of the implemented remote unit's hardware

A EADS THR880i /9/ communication terminal, comprising TETRA modem and GPS receiver, has been used for the purposes of test application. It communicates with the microcontroller at a speed of 9600 bps using a standard RS-232 protocol. A MAX232 chip has been used to adapt the voltage levels of the RS-232 interface to the TTL levels. The communication interface occupies only two of the microcontroller's pins, i.e. the Tx and Rx of the USART interface available through port C. In our test application a standard 8 MHz crystal oscillator was used, while a reset circuit was driven by pushing a reset key.

To this end the core hardware has been described that is invariable in all remote units. Besides being the main data processing component it is also used to exchange AT messages with the communication terminal, and to set or read basic telemetry/telecontrol remote unit signals, i.e. converting analog input signals by built-in AD converters or managing each port's TTL digital signals (0 and 5 V levels). In the case of more complex signals, an application specific circuit has to be used, with the core circuit providing the proper communication interface. In our test application, shown in Figure 5, the following circuits have been designed:

- Temperature sensing circuit based on a Dallas DS1820 /10/ temperature sensor.
- Alarming device to visualize triggered alarms.
- Real-time clock (RTC) module for time-stamping measurement records.
- Compact Flash (CF) data storage device interface.

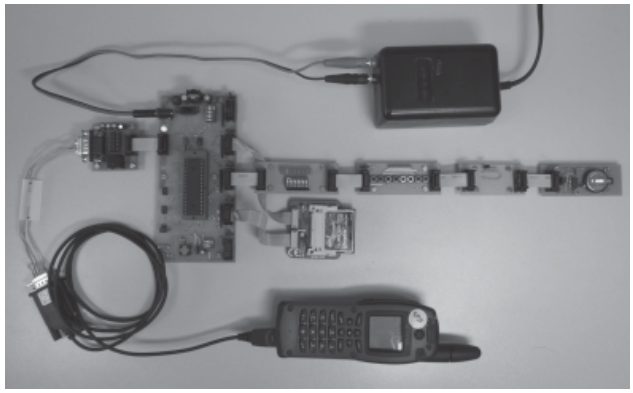

Fig. 5: Photo of the designed remote unit test application

The temperature sensor performs periodic or on-demand temperature measurements which are either reported to the control centre or stored in a log file. Based on these measurements alarms are triggered when a defined temperature threshold value is exceeded. The temperature sensor used measures temperatures in the range from -55 °C to +125 °C, where measurements between -10 °C and +85 °C are precise to a 0.5 °C. Communication is carried out using a 1-wire protocol, thus occupying only one of the microcontroller's pins. In our case the RC0 at the port C was used.

Alarming signals were in our test application represented simply by turning on and off the LEDs on pins RC1 and RC2 of port C. The key connected to the RC5 was used to manually turn the remote unit's alarm off and reset the process to a new iteration of temperature measurement and alarm triggering.

The real-time clock module is one of two components included in the system for the purpose of autonomous operation. It is based on a Philips PCF8583 integrated circuit /11/, which is the clock/calendar circuit that was used to time-stamp temperature measurements and alarm logs stored in a log file during the autonomous operation mode, i.e. operation in the period without TETRA network connectivity. The circuit uses a two-line bidirectional I^2C bus as a communication interface and is therefore connected to the microcontroller using the pins SCL (Serial CLock) and SDA (Serial DAta), located at RC3 and RC4 of the port C. The circuit additionally comprises a local oscillator and a battery backup.

The CF storage device is the second component included for the support of the autonomous operation, used to store logs of taken activities. It is connected to the microcontroller occupying two of its ports, with the control lines connected to port B and the data lines connected to port D.

5.2 Software Part

The software for the remote unit's microcontroller is of particular importance for the overall system performance, as the microcontroller has to utilize both the computation and

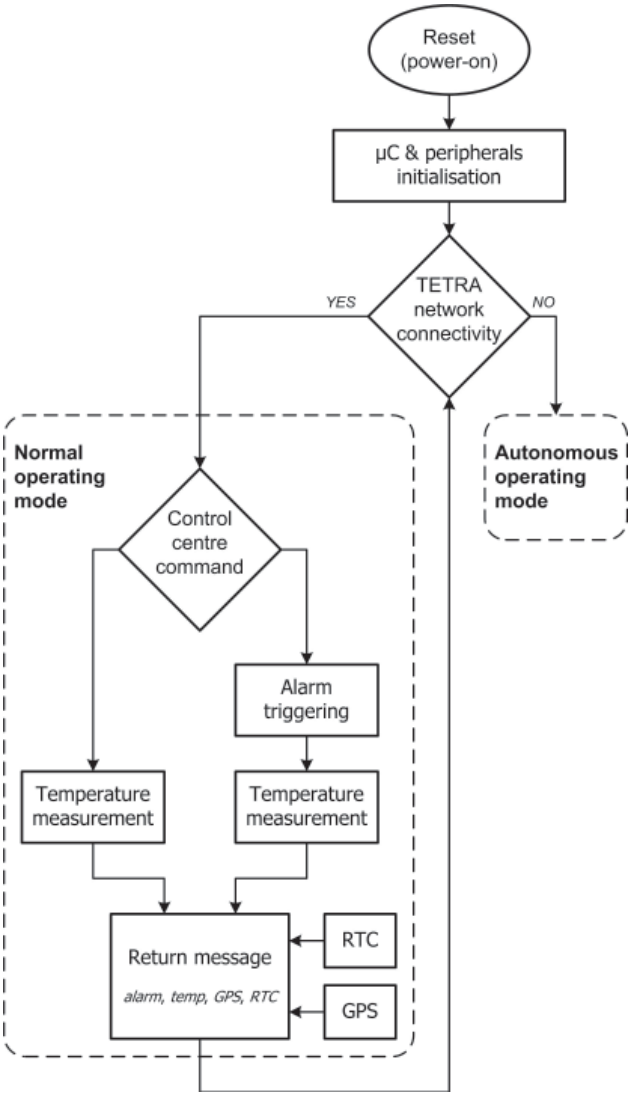

Fig. 6: Flow chart of the initialisation and normal operation mode

coordination functions efficiently /12/. Computation here refers to the code required to execute a particular command, while coordination refers to the code required for reliable communication of a remote unit with control centre, and the communication of a remote unit's core hardware with the application specific hardware.

Communication between the microcontroller and the communication terminal is based on exchanging AT command messages through the RS-232 serial port. Only a subset of the terminal AT commands defined by the manufacturer /13/ were supported in our test application, viz.

- commands used to set the proper terminal operation (e.g. how the RS-232 communication is handled),
- commands to check the TETRA network connectivity and signal strength,
- commands for handling the SDS messages, and
- commands used to manage the GPS receiver built in the terminal.

The execution flow chart of the microcontroller's program has been split into two parts, each describing one of the operating modes. They are depicted in Figures 6 and 7, for the normal and autonomous operation mode respectively. The normal operation mode flow chart also depicts the initialisation routine.

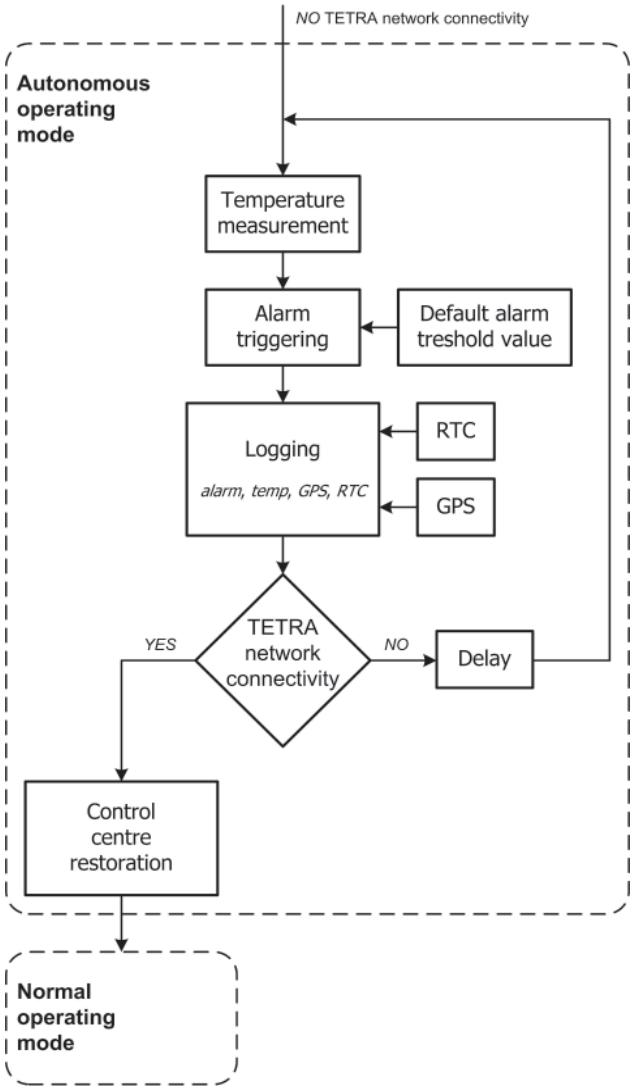

Fig. 7: Flow chart of the autonomous operation mode

The program for the initialisation and normal operation mode is executed as follows. After the reset the start-up procedure takes place, with the microcontroller, its peripherals and the associated communication protocols being initialised. The decision on the operation mode is then taken, based on the information about TETRA network connectivity. If the signal strength is appropriate, the program enters the normal operation mode, where it acts as a slave unit, executing commands received from the control centre. Alternatively, in the absence of TETRA network connectivity, the autonomous operation mode is selected.

In the normal operating mode, the remote unit receives SDS messages through the serial port, decodes them (i.e.

extracts the command information) and takes the appropriate actions. The program thus executes an infinite loop of making temperature measurements and triggering alarm signals. After each action taken (successful or unsuccessful command execution) the remote unit informs the control centre of its current status. This is done by sending back to the control centre a unified report SDS message containing the information about current measured temperature, alarm state, geographical location and time. This situation lasts as long as the TETRA modem has TETRA network connectivity.

The autonomous operation mode is entered when the TETRA modem loses TETRA network connectivity. In this mode the temperature is measured periodically and the alarm is triggered when the temperature exceeds the default threshold temperature. All this operating information, together with the time and current location, is in each iteration saved to the local storage device (CF card). When the remote unit regains TETRA network connectivity, all the locally stored operation information is transferred to the control centre, by which the control centre is restored and becomes ready to again take control of the remote unit, which consequently enters the normal operating mode.

Information like control centre TETRA modem number and threshold temperature value for alarm triggering in autonomous operation mode are saved in the microcontroller's EEPROM memory.

6. Conclusion

In this paper we presented the design and basic functionality of a telemetry and telecontrol system based on the TETRA network as a communication and interconnection platform. Test application with a dedicated control centre application and a microcontroller based remote unit was developed to demonstrate and validate the feasibility of the approach. In particular, the test application consists of remote temperature measurement and public alarming with the utilisation of Short Data Service for transmission of control commands and measurement data.

The modular design of the hardware platform provides the system with a great versatility, allowing it to be adapted to a host of telemetry and/or telecontrol applications from consumer, industrial, environmental, and health-care areas. The use of an appropriate microcontroller in a particular application would also provide the system with sufficient data processing capability and would adequately fulfil the performance/price ratio of the design.

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1977	Informacije SSESD (Strokovna sekcija za elektronske sestavne dele in materiale pri Jugoslovanski zvezi ETAN)
1986	Informacije MIDEM
1988	Iztok Šorli postane glavni in odgovorni urednik
1989	Revija je uradno registrirana, dobi UDK in ISSN; članki so pripravljeni v skladu z bibliografskimi standardi
1993	Revijo zajemata INSPEC in Iskra SAIDC-el Zaprosimo za zajem v podatkovno bazo ISI in začnemo s proceduro kvalifikacije
1995	ISI začne z zajemom v SciSearch, Research Alert in Materials Science Citation Index
1998	Revijo zajemajo INSPEC, Iskra SAIDC-el in ISI JCR IF: 0.088; SE, x: 0.549 (174/208), engineering, electrical & electronic, y: 0.698 (129/143), materials science
1999	Revijo zajemajo INSPEC, COBISS in ISI JCR IF: 0.019; SE, x: 0.702 (196/205), engineering, electrical & electronic, y: 0.78 (155/159), materials science
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2008	Revijo zajemajo INSPEC, COBISS in ISI JCR IF: 0,066; x: 0,942 (196/206), engineering, electrical & electronic, y: 1,659 (171/175), materials science

Informacije MIDEM (ISSN 0352-9045) v številkah 1987-2008

Tipologija	**št. čl.**
1.01 - Izvirni znanstveni članek	291
1.02 - Pregledni znanstveni članek	11
1.04 - Strokovni članek	88
1.05 - Poljudni članek	5
1.06 - Objavljeni znanstveni prispevek na konferenci, vabljeno predavanje	69
1.08 - Objavljeni znanstveni prispevek na konferenci	7
1.09 - Objavljeni strokovni prispevek na konferenci	1
1.12 - Objavljeni povzetek znanstvenega prispevka na konferenci	2
1.25 - Drugi članki ali sestavki	19
Nerazporejeno	63
Skupaj	556

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JCR IF = Journal Scientific Report Impact factor
SEx = Science Edition, engineering, electrical&electronic
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leto	JCR IF	SEx	mesto x	SEy	mesto y
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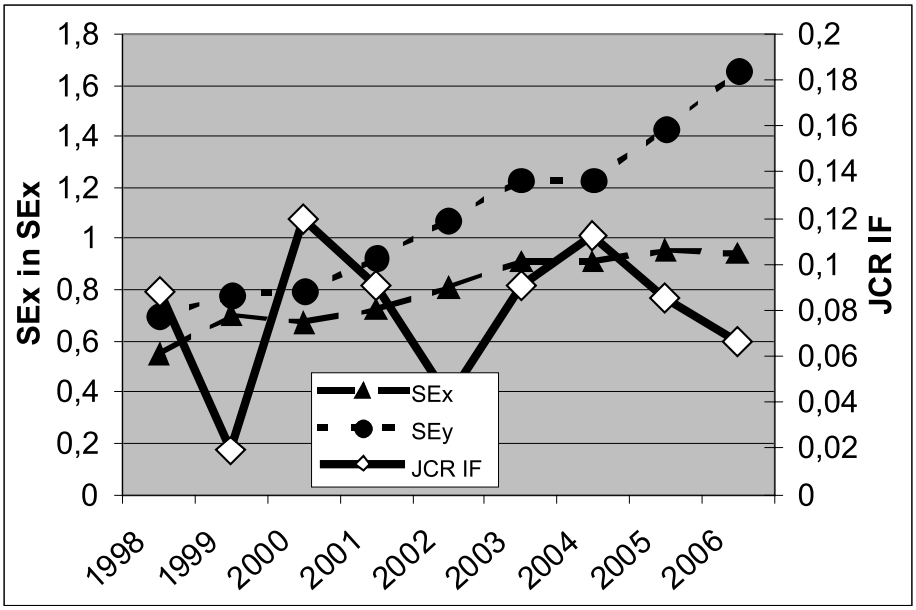
1999	0,019	0,702	196/205	0,78	155/159
2000	0,12	0,673	173/204	0,796	155/168
2001	0,091	0,724	175/200	0,923	162/170
2002	0,042	0,808	190/203	1,073	171/173
2003	0,091	0,912	190/205	1,229	170/177
2004	0,112	0,912	189/209	1,229	171/177
2005	0,085	0,954	190/208	1,429	172/178
2006	0,066	0,942	192/206	1,659	171/175



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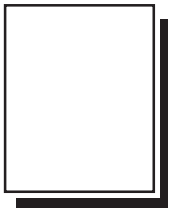

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