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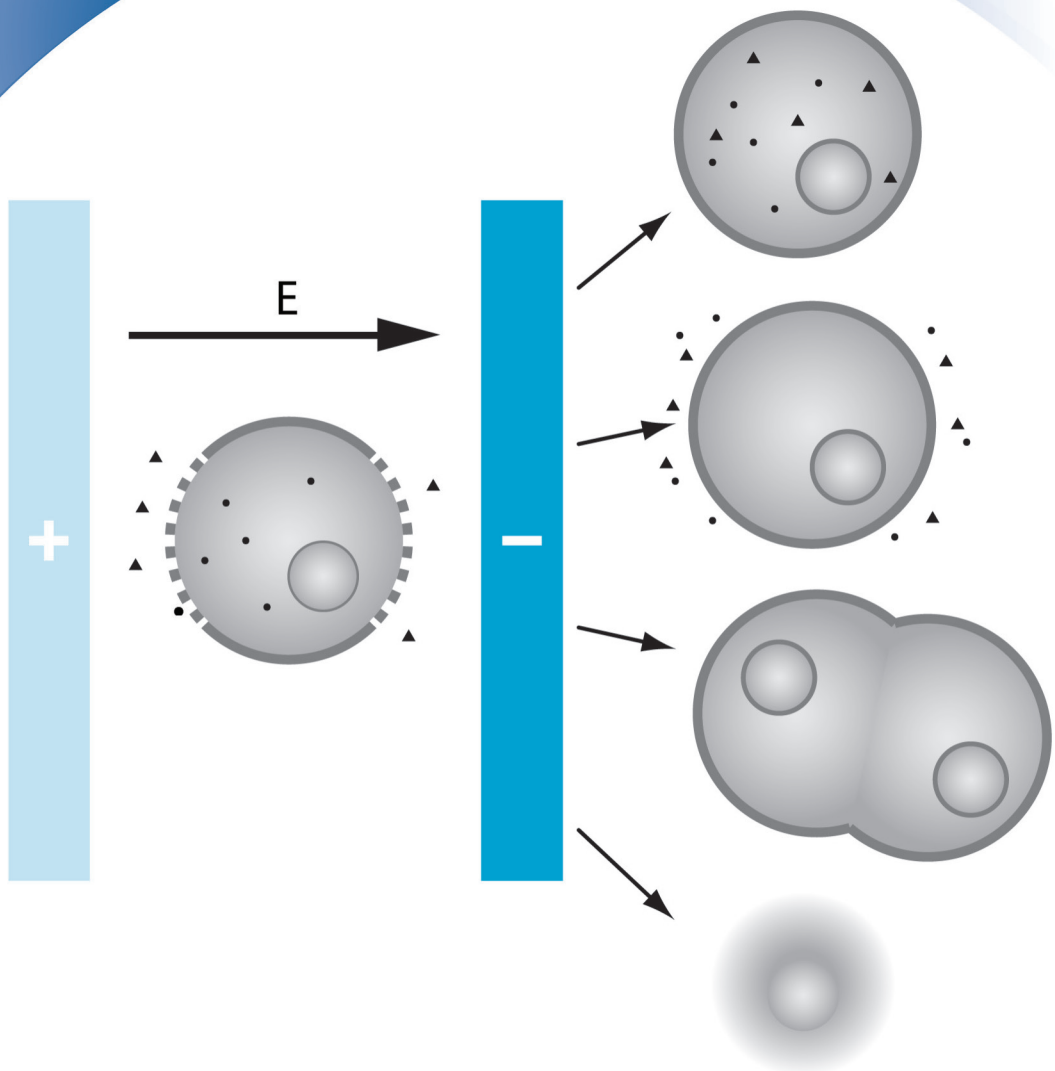

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Microfluidic devices for manipulation, modification and characterization of biological cells in electric fields – a review

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Abstract: This article presents use of electric field for manipulation of biological cells and modification of their physical properties in microfluidic chambers. Some fabrication procedures of electrodes and microfluidic chambers are presented, from thin film metal electrodes to three-dimensional structures. Strong electric field pulses induce formation of pores in cell membrane (electroporation), which allow for transport of physiologically membrane-impermeant molecules into the cell. Even stronger electric fields cause nonthermal cell lysis, which is useful in the extraction and analysis of intracellular components. Dielectrophoresis in an inhomogeneous electric field is used for manipulation of cells (e.g. guiding and patterning), characterization of their electrical properties, detection of rare cells, as well as for separation of different cells. Electroporation and dielectrophoresis can be used together on a single chip, where dielectrophoresis is used for positioning of cells where they are electroporated, which is often used for electrofusion of cells.

Keywords: microfluidic devices, electric field, dielectrophoresis, electroporation, cell separation, cell fractionation, cell fusion

Mikropretočne komore za ločevanje bioloških celic in spreminjanje njihovih lastnosti v električnem polju – zasnove, izdelava in aplikacije

Izvleček: Članek opisuje uporabo električnih polj za ločevanje bioloških celic in spreminjanje njihovih fizikalnih lastnosti v mikropretočnih napravah. Predstavljeni so različni načini izdelave elektrod in mikropretočnih naprav, od planarnih kovinskih elektrod do tridimenzionalnih struktur. V dovolj močnem električnem polju se v celični membrani pojavijo pore (elektroporacija), ki omogočijo transport molekul skozi sicer neprepustno membrano, v primeru še višjega polja pa se celica netermično lizira. Dielektroforeza omogoča premikanje in ločevanje različnih celic v nehomogenem električnem polju brez uporabe markerjev. Elektroporacijo in dielektroforezo lahko kombiniramo na čipih, ki omogočajo dielektroforetsko pozicioniranje celic in nato elektroporacijo, kar se najpogosteje uporablja za elektrofuzijo celic.

Ključne besede: mikropretočne komore, električno polje, dielektroforeza, elektroporacija, ločevanje celic, fuzija celic

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1 Introduction

Electric fields can be used for manipulation of biological cells, and at sufficiently high field strengths also for modification of their physical properties.

Cells can be manipulated by *electrophoresis* (movement of charged particles in an electric field), *electroosmosis* (movement of a liquid that contains a net charge, typically close to a charged solid surface), or *dielectrophoresis* (motion of polarizable particles in an inhomogeneous electric field). Strong electric field pulses can also induce formation of aqueous pores in the cell membrane – the phenomenon termed *electroporation*, and used for transmembrane transport of molecules for which the membrane is physiologically impermeant. In addition, such pulses can also cause fusion of adjacent

cells (*electrofusion*) and non-thermal cell lysis. If the exposure and the resulting damage is sufficiently limited, the exposed cells recover and remain viable (*reversible electroporation*), while excessive damage can lead to cell death (*nonthermal irreversible electroporation*) and lysis. The electric current caused by the field can also result in Joule heating, thus exerting a thermal effect on the cells, and excessive heating leads to irreversible thermal damage.

All these effects of electric fields can also be achieved in microfluidic chambers. Small dimensions of the channels and electrodes are more suitable for working with small volumes of cell suspensions, including single cells. Microfluidic chambers for exposure of cells to electric fields are sometimes qualified among Bio-MEMS – Micro-electro-mechanical systems for biological applications. In the last years Bio-MEMS sistem were developed for many different applications for cell biology, for example cell sorting [1]–[3], formation of tissue like structures [4], [5], analysis of intracellular content [6], [7], and efects of drugs on cells [8]–[10].

In microfluidic devices due to the short distance between the microelectrodes or the electric field constriction, a low voltage is sufficient to achieve required electric field, and thus can reduce the cost of high-voltage power generators as well as the negative effect of Joule heating present in traditional systems.

In this article, we review the designs, methods of fabrication and applications of microfluidic devices for manipulation and modification of biological cells using electric fields.

2 Effects of electric fields in biological cells

2.1 Electrophoresis and electroosmosis

Electrophoresis is the motion of charged particles, relative to the liquid medium in which they are suspended, under the action of an external electric field (Figure 1a). Electrophoretic force depends on surface charge of the particle and the strength of the acting electric field. Electrophoresis is a widely used technique for separation of charged molecules and intracellular components, while for separation of cells and other methods of their manipulation it is less efficient, and thus used much less than dielectrophoresis [11].

Electroosmotic flow is the motion of a liquid that contains a net charge, typically as a result of proximity of a solid surface and formation of a double electric layer at the interface, of which the layer of one polarity is bound to the surface, while the layer of the opposite polarity is in the liquid and thus highly mobile, so its charges are brought into motion by the field (Figure 1b). Because of the viscosity of the liquid in which the charges are dissolved, the whole liquid starts to move in the same direction. This phenomenon can be used for pumping the cell suspension into and through microfluidic devices, but generally not for finer manipulation or modification of the suspended cells [12], [13].

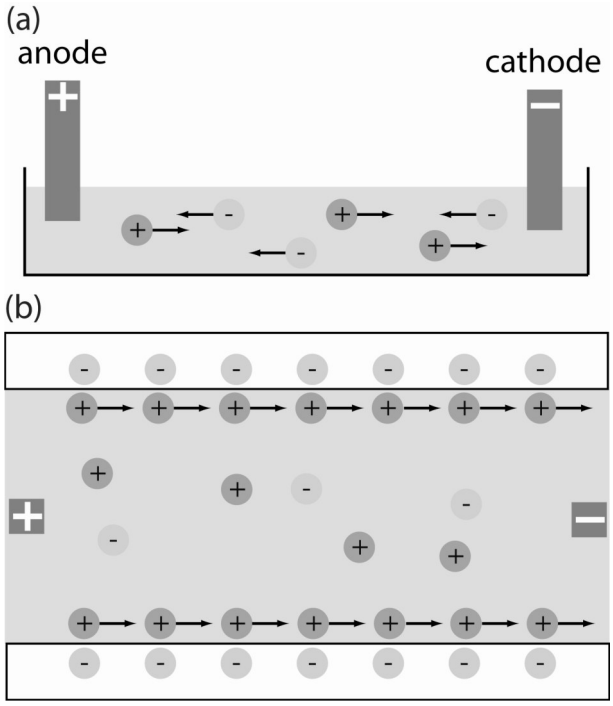

Figure 1: (a) electrophoresis, (b) electroosmosis.

2.1 Dielectrophoresis

Dielectrophoresis (DEP) is the motion of uncharged polarizable particles in a nonhomogeneous electric field [14]. An electric field induces a dipole moment of the particles, and its nonhomogeneity results in a net force on each particle (Figure 2). The size of the dielectrophoretic force (F_{DEP}) depends on the electric properties of the particles and the surrounding medium, while its direction is either towards higher field (if the particle is more polarizable than the medium – positive DEP), or towards lower field (if the particle is less polarizable – negative DEP).

Common uses of dielectrophoresis when applied to biological cells are in selective manipulation (e.g., focusing, guiding, and/or patterning) [15], [16], in separation of two or fractionation of several different cell groups [17], and in characterization of their properties [18]. Electrically, the cell plasma membrane represents a thin insulating sheet surrounded on both sides by

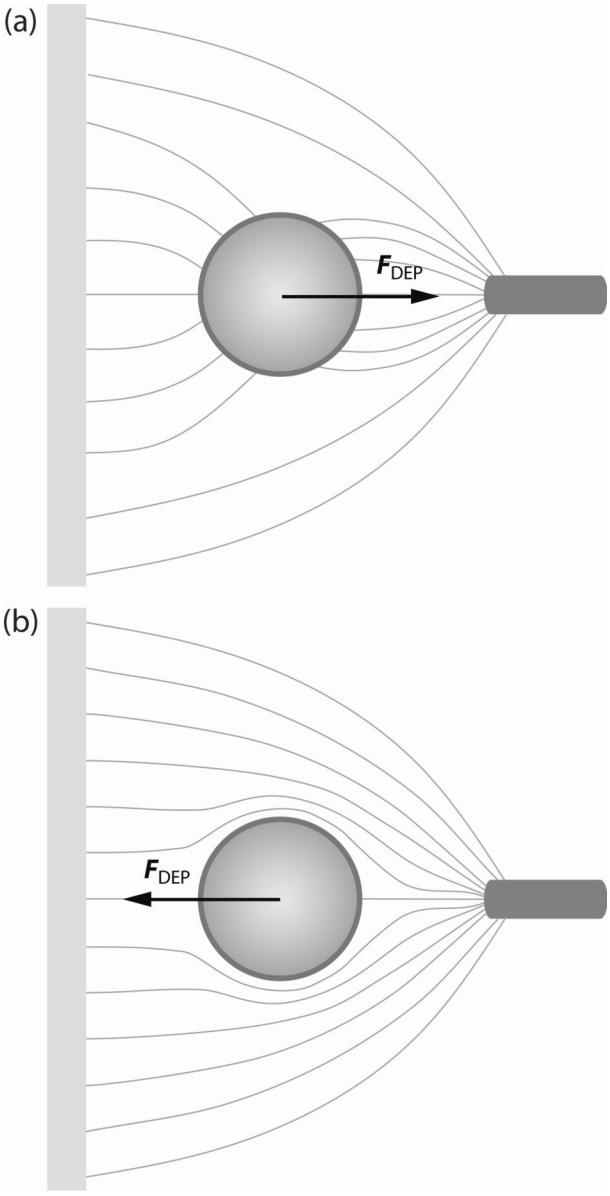

Figure 2: Dielectrophoresis: (a) positive, (b) negative.

aqueous electrolyte solutions. Time average of dielectrophoretic force acting on a spherical cell enveloped by a single membrane (i.e., a single-shell model of a cell) in an alternating electric field with amplitude E and angular frequency ω is given by [19]

$$F_{DEP} = \pi\varepsilon_0\varepsilon_e r^3 (\mathrm{Re}[f_{CM}(\omega)]\nabla|E^2| + 2\,\mathrm{Im}[f_{CM}(\omega)](E_x^2\nabla\varphi_x + E_y^2\nabla\varphi_y + E_Z^2\nabla\varphi_Z))' \quad (1)$$

with f_{CM} denoting the Clausius-Mossotti factor expressed as

$$f_{CM} = \frac{\varepsilon_c^{'} - \varepsilon_e^{'}}{\varepsilon_c^{'} + 2\varepsilon_e^{'}} \quad (2)$$

and with

$$\varepsilon_c^{'} = \varepsilon_m^{'} \frac{\left(\frac{r}{r-d}\right)^3 + 2\frac{\varepsilon_i^{'} - \varepsilon_m^{'}}{\varepsilon_i^{'} + 2\varepsilon_m^{'}}}{\left(\frac{r}{r-d}\right)^3 - \frac{\varepsilon_i^{'} - \varepsilon_m^{'}}{\varepsilon_i^{'} + 2\varepsilon_m^{'}}} \quad (3)$$

where r is the cell radius, d is the membrane thickness, φ is the phase delay between the components of the field, and ε_e', ε_m', and ε_i', are the complex dielectric permittivities of the external medium, membrane, and the cell interior (cytoplasm), respectively, each given by $\varepsilon' = \varepsilon - i\sigma/\omega$, with ε and σ the dielectric permittivity and the electric conductivity of the region, and ω again the angular frequency of the field.

The second term (summand) in Eq. (1) is non-zero only if a system of multiple electrodes is used and there is a phase delay between the field-generating signals delivered to them; this type of cell manipulation is termed *travelling-wave dielectrophoresis* [20]. If such electrodes are positioned in a radially symmetrical manner, and the signals are delivered as to generate a rotating electric field, this results in circular motion of the cells in the region between the electrodes, termed *electrorotation* [19].

But more typically, only one pair of electrodes is used, so that Eq. (1) simplifies into

$$F_{DEP} = \pi\varepsilon_0\varepsilon_e r^3\,\mathrm{Re}[f_{CM}\omega]\nabla|E^2| \quad (4)$$

with Eqns. (2) and (3) still valid. These equations show that at a given electric field, F_{DEP} is proportional to the real part of f_{CM}, which itself is a function of the field frequency, and this function will henceforth be referred to as the *dielectrophoretic spectrum* (*DEP spectrum*).

Separation of cells by dielectrophoresis is therefore possible if the cells in the mixture belong to two (or more) populations, each with either a different geometry, or different electric conductivity and/or dielectric permittivity [20]. Different geometrical and electrical properties result in different dielectrophoretic force acting on the cells of each population. Separation is the most successful if the two populations of cells to be separated differ in their crossover frequency (frequency of transition between negative and positive dielectrophoresis), and the applied field frequency is chosen in the manner that one population is subject to negative, and the other to positive dielectrophoresis, so that the dielectrophoretic force acts on them in opposite directions.

2.2 Electroporation

An exposure of a cell to a sufficiently high external electric field results in electroporation – formation of nanoscale aqueous pores in the lipid bilayer of the cell plasma membrane [21]–[24]. These permeable structures provide a pathway for diffusive transport of otherwise membrane-impermeant molecules into and out of the cells. If the exposure is sufficiently short and the membrane recovers sufficiently rapidly for the cell to remain viable, electroporation is reversible, otherwise it is irreversible.

Reversible electroporation is already an established method for introduction of membrane-impermeant chemotherapeutics into tumor cells – *electrochemotherapy* [25], and a promising technique for gene therapy devoid of the risks caused by viral vectors – *gene electrotransfer* [26]. In medicine, irreversible electroporation is a method for tissue ablation – *nonthermal electroablation* [27], while in biotechnology it is used for *electroextraction* of biomolecules [28] and microbial deactivation, particularly in food preservation [29] (Figure 3).

The voltage on the membranes of the exposed cells, termed the *induced transmembrane voltage* (*ITV*), represents a part of the voltage delivered to the electrodes and is position dependent; thus in spherical cells, it varies proportionally to the cosine of the angle θ measured from the center of the cell between the position on the membrane and the applied field direction [30]

$$\mathrm{ITV} = \frac{3}{2} ER\cos\theta \tag{5}$$

The ITV thus has extremal values at the points where the field is perpendicular to the membrane, i.e., at θ = 0° and θ = 180° (the "poles" of the cell), and is zero at 90° (the "equator"). Thus, if the peak transmembrane voltage of 0.3 V is to be achieved on a cell with a 10 μm radius, the cell has to be exposed to a field of about 200 V/cm.

2.3 Electrofusion

Cell fusion is a method for achieving nucleus transfer, hybridoma and epigenetic reprograming of somatic cells. Fusion of two different types of cells generates a third, polynuclear type that displays hybrid characteristics of the two parental cells (Figure 3). Although chemical (polyethyleneglycol treatment) or viral methods can be used for cell fusion, electrofusion is safer, more controllable and it can provide high yield of fused cells [32], [33].

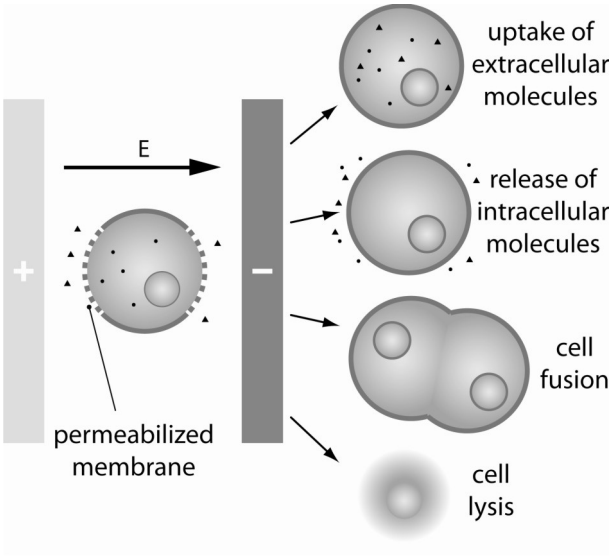

Figure 3: Use of electroporation: transport of molecules across the membrane, cell fusion and cell lysis. Adapted from [31].

For fusion, cells must be brought into a close contact, which can be achieved by chemical methods, sedimentation, in microstructures or by dielectrophoresis [34]. Traditional bulk pairing methods are mostly nonspecific, so that from a mixture of type A and type B cells one gets hybrids of AA, BB, and AB types, while generally only the latter are desired. Specific pairing methods, which are best achieved in microfluidic chambers, can increase the yield of the desired hybrid type.

Once the contact is achieved, electric pulses can be used to bring the membranes in contact into a fusogenic state, and thus facilitating the fusion of the two cells into a single hybrid cell [34].

3 Fabrication of microfluidic devices

Fabrication of microfluidic devices is often based on processes developed and used in semiconductor industry. The most frequently used materials are silicon, glass and gold. However, the cells suspended in fluid media introduce specific requirements that have lately led to an increasing use of plastics. Chambers are typically transparent, which allows for observation under the microscope, they have inlets and outlets for fluid flow. The electrodes are most often in direct contact with the cell suspension, and thus for every new experiment, the chamber must either be thoroughly cleaned, or replaced by a new one.

In the design of microfluidic devices, the designer must simultaneously consider the specifics of the fluid flow, electric field distribution, electrode fabrication, and

encapsulation. Modeling of such devices therefore requires knowledge of several different areas of physics, and verification of such models can be difficult, particularly as the electric field strength and its distribution within the chamber cannot be measured directly. Standardization of dimensions, which would allow for interconnection of several devices into a more complex system, is currently poor, as some chamber dimensions are adopted from semiconductor industry (e.g., silicon or glass wafers), and others from cell laboratory equipment (e.g., microscope slides and microtiter plates).

In the last years, a trend of standalone *lab-on-a-chip* or *μTAS* (micro total analysis) devices has started to emerge. The goal is to make small portable devices into which a sample of cells can be loaded, and all of the requested information extracted. However, current systems mostly still require connection of these small devices to external pumps, large electrical signal (function) generators, centrifuges, and often also manual pre- and post-handling of liquids and cells.

For analysis, small size is a great advantage, because very small amounts of stains or other expensive chemicals are required. In contrast, for production of cells with desired properties (for example production of cell hybrids by means of fusion), small volumes and thus small yields are a disadvantage. As microdevices often cannot be scaled up in all dimensions, particularly due to the loss of control of individual cells and the impact on the surface-to-volume ratios, designers must in such cases rely on parallelization.

3.1 Bio-MEMS materials

Desired Bio-MEMS materials are biocompatible, chemically modifiable, easy to fabricate, economic, soft and flexible. The most often used materials are borosilicate glass, silicon, gold, indium-tin oxide (ITO), titanium, chrome, silicon dioxide, silicon nitride, silicon carbide and polymers poly dimethyl siloxane (PDMS), poly methyl methacrylate (PMMA), SU-8 epoxy photoresist, and polyimide [35], [36].

Generaly used materials and fabrication processes of microfluidic devices were revieved elsewhere [5], [6], [37], here we describe fabrication of typical microfluidic device prototypes for cell manipulation and modification by elecric field.

Borosilicate glass is widely used as a base plate for microfuidic devices. It is chemically resistant to liquids used for suspending cells, it is highly transparent for broad range light wavelengths (~300-2200 nm), it is suitable for deposition of metallic and polymeric layers, and it can withstand high temperatures during metal deposition process. It can be anodically bonded to silicon, and fluidic channels can be made by etching. Thickness of the glass wafer is typically less than 1 mm, due to which large microchambers are brittle. Polymers are more flexible, for example polyimide can be used as the bottom plate for large electrode deposition [38]. PDMS is most often used as a cover or part of the chamber. It can be easily molded and cured and it is optically transparent, flexible, it has very low electric conductivity and it is biocompatible. It is also inexpensive and therefore a new chamber can be made for every experiment if required. Molds for PDMS chambers are typically made from silicon wafers by patterning SU-8 [39] or by etching in silicon by deep reactive ion etching (DRIE), which is more durable, useful for high aspect ratio structures, but more expensive [2].

Stainless steel is sometimes used for larger parts of microfluidic chambers, but not for smaller structures, as these are difficult to fabricate, and it is also preferable to avoid it in electrodes used for delivery of strong electric pulses, as electrolytic release of Fe^{2+} and Fe^{3+} ions can contaminate the cell suspension [40], [41]. Aluminum is sometimes used as an alternative; this similarly results in release of Al^{3+} ions, but the release was reported to be lower when using short pulses (≤ 100 μs) [41], [42]. The most expensive solution, but least problematic from the aspect of electrolytic contamination, is to construct electrodes from platinum.

Silicon is mechanically strong, and many techniques for fabrication of silicon microelectronic structures have been developed, making it a common material in microchamber fabrication. Silicon derivatives such as SiO_2, Si_3N_4 and SiC are insulators, which allows for construction of multilayer structures. The electrical conductivity of pure silicon is low (~10^{-4} S/m), but it can be increased by many orders of magnitude (up to 10^5 S/m) by doping the silicon substrate with conductive atoms [43]. Gold offers an even higher electrical conductivity, and higher chemical inertness than doped silicon, but it is typically only depositable in thin layers (up to 250 μm), while thicker layers are difficult to fabricate.

ITO is a conducting material, which is optically transparent in thin layers. Polymers can also be made conductive my mixing them with small conductive particles of silver or carbon. When concentration of these particles reaches the percolation threshold, electric current can flow through a mesh of these particles and electrical conductivity is increased by several orders of magnitude. As the volume of silver particles in PDMS reaches 19%, conductivity increases almost stepwise from $2.5 \cdot 10^{-14}$ S/m to $6.2 \cdot 10^3$ S/m [44], while addition of carbon black powder to PDMS can increase its conductivity up to 15 S/m [45]. Mechanical properties of

polymers with added particles are not altered as much as electric conductivity. A disadvantage of using non-metal electrodes is the need to use higher voltages to generate the same strength of electric field in comparison to metal electrodes. For dielectrophoresis and electroosmosis between the electrodes not more than 100 μm apart, the voltage of ±5 V is often sufficient, and common function generators can be used for this purpose. For higher voltages, amplifiers or custom built generators are required.

Cells tend to form clusters, and also bind to some surfaces, especially to metal electrodes. To prevent such binding, the internal surfaces of the chamber can be coated with antifouling molecules, such as Bovine serum albumin or polyethylene glycol [46].

3.2 Assembly, fluidic and electric connections

Assembling Bio-MEMS devices requires not only electrical, but also fluidic connections, and designing the shape of the channels and their assembly is as important as designing the appropriate shape of the electrodes [35]. Fluidic connections to flexible PDMS chambers can be made by punching PDMS device before bonding and inserting appropriate size tubing into holes. For rigid materials such as glass and silicon fluidic connectors holes must be drilled or etched and commercially available fittings can be used to connect tubing [47], [48]. For electrical connections part of metal layer must be uncovered or holes must be drilled to cover plate [47], [49]. Chamber components must be sealed in a watertight manner to prevent leakage, but if they are not for single use, they must at the same time allow for cleaning and/or replacing parts. Thus, parts of single-use chambers can be permanently glued or bonded together (glass-glass or glass-silicon bonds), while reusable chambers must allow for disassembly either by pressing the parts together with an external frame and sealing the contacts temporarily with a soft material (rubber, wax), or by weak bonding (plasma activation of PDMS and bonding to glass).

3.3 Fabrication techniques

For fabrication of large number of devices, plastic is the material of choice, while for prototypes and devices made in low production quantities, fabricated glass with thin metal film is often chosen due to precision and reproducibility of fabrication, as well as of the electrical and chemical properties of the materials (Figure 4a). Pyrex glass is thus used as a basis for the electrodes onto which a layer of metal (chromium, titanium or gold) is deposited by chemical or physical (sputtering) vapor deposition. Thickness of the metal film is typically several hundred nm. Then, the photoresist layer is spun-on onto metal-covered substrate surface. The chosen pattern of the electrodes is transferred onto photoresist by illuminating through the mask (photolithography). This process is followed by wet or dry etching of thin metal layers on the part of the surface not protected by photoresist, and concluded by cleaning the remaining photoresist. For three-dimensional structures deposition of photoresist, photolithography and etching can be repeated. Thick layer of metal can be deposited over thin film by electroplating; however, photolithography of thick photoresist is done before electroplating, and fluidic channels are formed by removing the remaining photoresist [35].

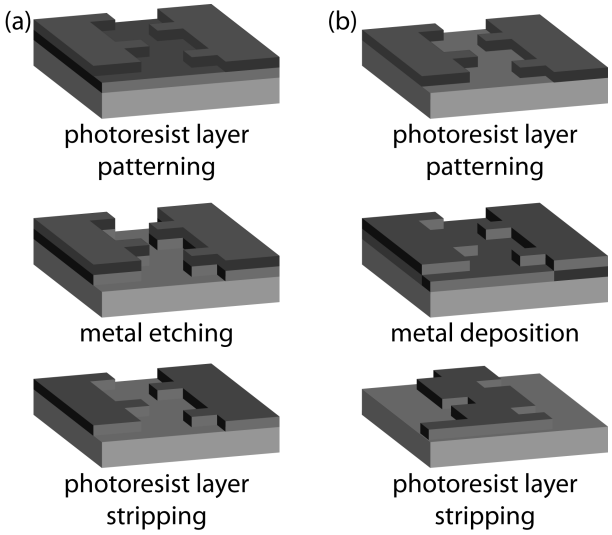

Figure 4: Fabrication of thin film electrodes. a) etching into metal layer, b) lift-off process. Adapted from [36].

Electrodes for MEMS can also be made by a lift-off process (Figure 4b). Photoresist is deposited on glass wafer, patterned by photolithography, and then a layer of metal is deposited, for example with electron beam evaporation. Finally, the photoresist is chemically removed and metal layer remains only on the part of the surface that was not covered by photoresist.

Laser ablation is another technique used to make electrodes from thin metal film. A thin metal film is deposited on a glass substrate. A laser beam heats a small volume of the metal, causing evaporation. By guiding the laser over the substrate, the required pattern is formed. The advantage of this process is in the absence of mask and etching, while its disadvantage is in the rougher surfaces and edges, and it is mainly used for fabrication of prototype devices.

Chambers with three-dimensional electrodes are typically made of insulating materials, which can easily be deposited in layers with thicknesses over 10 μm (thus exceeding the dimensions of biological cells), and with the deposition followed by electroplating of metal.

Fabrication of three-dimensional structures from silicon is well-established, but for electrodes, silicon must be heavily doped to attain sufficient electrical conductivity (at least 1 S/m [47]). The chamber can be made transparent if the electrodes are made from silicon on glass wafer and anodically bonded to the glass plate on top of the channel. The holes for fluid connections are drilled or etched into the glass. Channels more than 100 µm deep can be formed by deep reactive ion etching (DRIE). By exchanging etching and passivation (Bosch process), vertical sidewalls are formed, with very high reproducibility of the process [47].

The LIGA process (from German: Lithographie, Galvanoformung, Abformung) is used for fabrication of thick three-dimensional structures. A thick layer of photoresist is deposited on a conductive plate, and a pattern of electrodes is transferred to this layer by illumination through a mask (photolithography). Then a layer of metal is deposited in the gaps in photoresist, and the remaining photoresist material is cleaned. The result are thick metal electrodes that can also be used as a mold for injection molding of plastics. The disadvantage of this process is the required use of a high-power beam source of parallel X-rays when illuminating through the mask, and a synchrotron is generally required to generate this beam [36].

Inhomogeneous electric field for dielectrophoresis can be generated also by placing insulating structures into an otherwise homogeneous field – *insulator dielectrophoresis* (iDEP). Electric field is still generated by metal electrodes, but the electrode shape can be much simpler. Thin-layer metal electrodes positioned along the channel, or even a pair of wires can be used. To achieve the field nonhomogeneity, insulating structures such as constrictions or pillars are formed between the electrodes, e.g. by isotropic etching in glass [25]. A layer of chromium is deposited on the glass mask, serving as hard mask. Then a layer of photoresist is deposited, patterned and developed. Exposed chromium is etched and subsequently, the exposed glass is etched with a solution of hydrofluoric acid. The plate with the channel is bonded to the cover plate, forming a chamber. Another option is creating a mold and then using an injection molding process to create a channel from polymer material [50].

An alternative way of creating electrodes for dielectrophoretic separation are optoelectric tweezers [51]. A photosensitive layer consisting of n+ a-Si:H, intrinsic a-Si:H, and SiC_x films is deposited over a layer of indium-tin oxide (ITO) on glass. The photosensitive layer becomes electrically conductive when illuminated. By selectively illuminating this layer through a mask or by an adequate projector, virtual electrodes are generated that only remain conductive for the time of illumination. By applying AC voltage onto these electrodes, the cells can be manipulated or separated by means of dielectrophoresis. The advantage of such electrodes is their easily changeable shape, and a much lower density of the light current in comparison to optical tweezers. Their weakness is considerably lower electrical conductivity of virtual electrodes in comparison to metallic ones, due to which dielectrophoresis only functions with cells suspended in a medium with a very low electrical conductivity.

4 Applications of microfluidic devices

4.1 Electroporation

In traditional electroporation devices, hundreds of µl of a cell suspension (typically corresponding to millions of cells) are exposed to electric pulses simultaneously. To achieve electroporation, voltage in hundreds or even thousands of volts must be delivered to the electrodes, and special safety precautions are thus required. The large exposed volume can also contain local nonhomogeneities of the field, and consequently variable rates of porated and surviving cells, as well as variations in the local pH. Aluminum and stainless steel typically used for electrodes in such devices are sources of electrolytic contamination of the suspension with metal ions [41], with possible unpredictable effects on cells.

Microfluidic electroporation devices overcome many of the abovementioned shortcomings of conventional (bulk) electroporation, and add several other advantages [52]–[57]. Since electroporation in such devices is performed with a much narrower gap between the electrodes, several volts suffice for electroporation, and safety precautions can be avoided, lowering considerably also the power consumption and heat generation. At the same time, the small gap relative to the area of the electrodes also assures a high homogeneity of the field, and also largely reduces the electrolytic contamination, as well as the variations in the local pH [53]. In microscale devices, the larger surface-to-volume ratio also leads to the faster heat dissipation, making it possible to distinguish between the heating effects and the electric field effects, which is yet another advantage of microfluidic electroporation devices.

While the limited processing volume can be viewed as a shortcoming of microfluidic electroporation, this can largely be overcome by performing electroporation in a continuous flow [58]. Microfluidic electroporation also offers the possibility of real-time monitoring and visualization of cellular and intracellular response to

the electric pulses (using fluorescent probes for example), including molecular uptake.

The ability to perform single-cell electroporation is another advantage of the microfluidic electroporation, particularly from the aspect of basic research. Namely, it is possible to trap a single cell in a specific location within the microfluidic chamber, and then study effects of electric pulses under a high-magnification microscope, which is almost impossible to achieve in volumes used with conventional electroporation equipment. Microfluidic electroporation devices also offer high potential for integration with other microfluidic components to form a multifunctional lab-on-a-chip system, which would greatly facilitate biochemical experiments consisting of several stages.

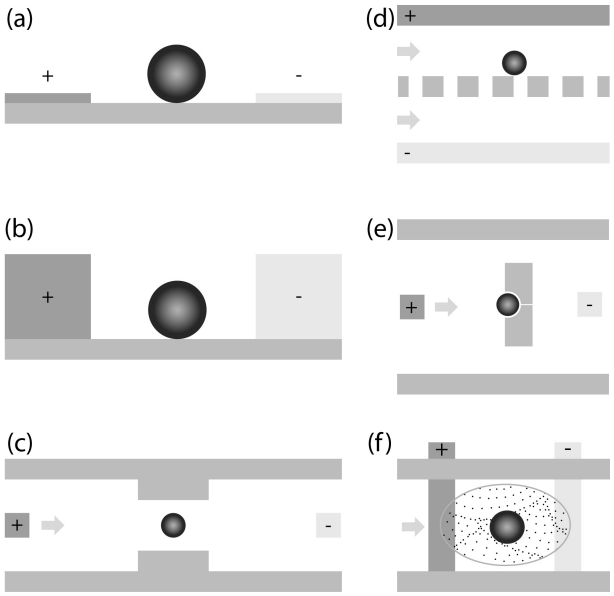

Figure 5: (a) thin film metal electrodes, (b) thick metal electrodes, (c) electroporation in a channel with constriction, (d) electroporation on an insulating mesh/ between pillars, (e) electroporation of cells trapped on insulating structures, (f) electroporation in aqueous droplet in oil. Panels (c-f) adapted from [59].

4.2 Gene electrotransfer

For cell transfection (transfer of genetic material into the cell and subsequent gene expression), electroporation must be well controlled to ensure cells are sufficiently electroporated, yet they remain viable. Microfluidic chambers allow for exposure of a single cell or a bulk of cells to electroporative pulses. Cells can flow though the chamber where they are electroporated either sequentially, or simultaneously in several designated positions. Electroporation is preferably performed in a homogeneous electric field using rectangular electric field pulses, but if cell positioning is well controlled, an overall nonhomogeneous field can also be suitable for the task.

For transfection of molecules into single cells, Valero et al. [60] used a microfluidic device with two channels etched into silicon by reactive ion etching. For positioning of single cells between the electrodes, a hole in the wall between two channels was etched. This allowed the fluid to flow through the holes, but not the cells for which the holes were too small. Channels were covered with glass on which platinum electrodes were sputtered prior to anodic bonding to the silicon wafer. When cells were trapped, DNA plasmid was released into the medium surrounding the cells, and the cells were individually electroporated. Transfection rate of 75% was achieved, which is quite high compared to typical yields with electrotransfer performed in bulk suspensions.

Vassaneli et al. [61] used an array of 60 cell-sized microelectrodes that enabled single-cell electroporation of attached cells. This silicon microchip was fabricated using the backend of a CMOS (complementary metal–oxide–semiconductor) process. The active area of the electrodes was made of a gold layer, and its diameter ranged between 15 and 50 μm to match different sizes of different cell types. The chip was encased with a plastic culture chamber, and the electrodes were individually addressable by the switching system.

Many cells can be electroporated and transfected in a simple microfluidic PDMS channel between two reservoirs with two platinum wires as electrodes. Traditionally, the direction of electric field is perpendicular to the flow direction, but orienting the electric field along the channel allows for much easier fabrication, as the channel can be made from a single insulating material, and the electrodes can be simple wires. Moreover, the ratio between electrodes surface and suspension volume is much smaller than in the case of metal electrodes positioned along the channel. Voltage drop on the electrode-liquid interface is relatively small due to the large distance between electrodes. Two reservoirs can be connected with many channels, which allows for simultaneous electroporation of cells in all the channels. Such channels can have different lengths, making the electric field in each channel different, which is particularly useful for determining e.g. the threshold electric field strength for electroporation [62].

The electric field between two reservoirs can be concentrated (focused) by positioning an insulating constriction into the channel (Figure 5c). By adjusting the frequency of electric pulses and flow rate, the operator determines the number of pulses to which each cell is exposed. Only one cell at a time can be inside the constriction, as other-

wise the cells would be exposed under different conditions. If the time spent by a cell inside constriction is very small (a few ms), a continuous DC voltage can also be used for electroporation. Wang et al. [63] made a channel 7 mm long, 213 µm wide, and ~33 µm high in PDMS, containing in its middle a narrower channel 2 mm long and 33 µm wide. Electric field inside the constriction was thus 5 times stronger than outside it. A mold for this chamber was fabricated using soft lithography on a layer of SU-8, and then PDMS was poured on it and cured. After removing the mold, the surface of PDMS was oxidized and bonded together with the glass slide. Platinum wires were used as electrodes.

Zhan et al. [64] used a similar channel, but with four constrictions (the equivalent of exposure of cells to four pulses), obtaining electroporation of CHO cells with transfection rate of 30 %. This type of devices allows for high-throughput controlled electroporation and transfection of cells flowing through the channel. Required voltage between electrodes was a few hundred volts and the cells had to be suspended in low-conductivity buffer to avoid thermal damage to the cells. Fabrication of such devices is relatively simple, but the chambers are for single use.

Electroporation in a channel with small electrode surfaces can be performed on a chip with a salt bridge. Kim et al. [53] developed such an electroporation chip made of PDMS channels on a glass. The mold for PDMS casting was made of SU-8 on a silicon wafer. Cells flowed through the main channel, while two side channels were filled with hypertonic hydrogel with conductivity of 16 S/m. Side channels were connected with the main channel through small openings, and the hydrogel delivered most of the applied voltage to the main channel, with the electric field focused in the low-conductivity cell suspension. The advantage of a salt bridge is absence of bubble generation and of electrolytic decomposition present on metal electrodes, since Ag-Ag/Cl electrodes are in direct contact only with the salt bridge. With a 10 V DC input voltage delivered to the chip, electric field in the main channel reached 900 V/cm.

The most straightforward method for decreasing required voltage for electroporation is to reduce the distance between the electrodes. Channels made in a single thin film layer cannot provide homogeneous electric field, since cells are larger than the layer thickness, but bonding together two plates, each with its own thin metal layer, so that they face each other, forms a channel with homogeneous electric field suitable for continuous electroporation. Lin et al. [65] fabricated such a chip using thin film evaporation, photolithography, lift-off process and fusion-bonding methods. A PMMA plate (Poly methyl methacrylate known as acrylic glass) was used for the top and the bottom plate, each with a layer of Au/Ti electrodes. A groove was precisely cut on a piece of PMMA substrate using an excimer laser and all pieces were fused together. The channel was 0.2 mm high, 5 mm wide and 25 mm long. With 10 ms rectangular pulses of 10 Hz frequency and 10 V amplitude, 500 V/cm electric field was generated. The authors obtained electrotransfer of the GFP gene, but did not report the transfection rate.

Zhan et al. [66] developed a microfluidic device that encapsulates cells into aqueous droplets and then electroporates the encapsulated cells. The device was fabricated based on PDMS using the standard soft lithography method. Thin film Au electrodes were fabricated on glass and PDMS was bonded with glass to form a chamber. A simple T-junction channel was used to produce droplets of monodispersity. For electroporation, a constant voltage was established across a pair of microelectrodes on the glass substrate in the downstream. The droplets with cells flowed continuously through the microelectrode pair, and because the oil phase is nonconductive, each flowing buffer droplet experienced a field intensity variation equivalent to a pulse with duration equal to the time during which the two electrodes were connected by the droplet. The microfluidic electroporation approach based on droplets could reduce the volume of dyes or reagents used for analysis, although the mixing of droplets with oil decreased the viability of cells by about 11%, which is significant but not critical for most of the applications.

Macqueen at al. [67] proposed electroporation in a nonhomogeneous electric field in combination with dielectrophoretic positioning. Thin Ti/Pt electrodes were fabricated on glass slide using standard lift-off processes. Surface of the electrodes was covered with a thin 50 nm layer of coatings using plasma-enhanced chemical vapor deposition. Electrically insulating (SiN_x:H) barriers prevented electrolysis of the suspension medium. A function generator provided both the AC field for dielectrophoretic positioning, and the pulses for electroporation. Such a device is very versatile, and can in principle be used for applications ranging from observation of dielectrophoretic separation of cells, measurement of crossover frequency, electrorotation, dielectrophoretic deformation, to transfection or cell lysis. As a disadvantage, such a chamber is suboptimal for any of these procedures from the aspect of achievable efficiency.

4.3 Cell lysis

Large devices for cell inactivation are typically used in industry for food preservation or deactivation of microor-

ganisms in water. They are most often made from stainless steel pipes (tubes). However, for studying the process of cell lysis, much smaller and transparent chambers are required, so that the effects can be monitored under the microscope. The advantage of cell lysis achieved with electric field pulses, in comparison to chemical lysis, is that only the outer cell membrane is damaged, while the organelle membranes remain intact.

Huang and Rubinsky [68] fabricated the first microfluidic devices capable of electroporating single cells. It had a multiple-layer chamber, consisting of three chips glued together placed on acrylic substrate with fluidic connections. Materials used for chamber fabrication were n-type silicon, silicon nitride, silicon dioxide and aluminum. For fabrication, standard silicon microfabrication technology (photolithography, etching) was used. Electrodes were in the top and the bottom layer, and in the isolation layer between them a 2 μm diameter hole was drilled. The cell was positioned on the hole, where the electric field was the strongest. The cells could be electroporated either reversibly or irreversibly with this device. By monitoring the electric current it was possible to detect the presence of the cell on the hole and deliver the electroporating pulse accordingly.

A chip with thick electrodes for cell lysis was fabricated by Lu et al. [69]. Glass substrate was covered with thin layer of gold. A thick layer of SU-8 was deposited, patterned and then additional thick layer of gold was electroplated. Then SU-8 was removed and deposited again with the pattern of a microfluidic channel. On the top of the channel cover slip was glued with epoxy. The device was used for lysis of human carcinoma cells. At 10 V of AC voltage delivered to the electrodes, a nonhomogeneous field in the range of kV/cm was generated. Nonhomogeneous fields formed around such electrodes generates positive dielectrophoresis, so that the dielectrophoretic force pulls the cells into the region of the highest electric field, where they are irreversibly electroporated [70], [71].

4.4 Measuring cell properties by dielectrophoresis and electrororation

Microelectrodes can be made in various shapes on a single chip, allowing for studying multiple effects of the electric field [16], [72]–[76]. For example, Müller et al. [72] constructed a three-dimensional microelectrode system for handling of single cells. It was designed to focus, trap and separate cells using negative dielectrophoresis, and they used two different systems. The first was fabricated by laser ablation of thin platinum layer on glass, with a polymer sheet used as spacer and two glass surfaces with electrodes assembled together face-to-face. The second system was fabricated with standard photolithography and lift-off process on glass with thin platinum layer and also assembled in a microfluidic chamber. When the cells entered the chamber, they were dielectrophoretically aligned in the middle of the channel, then individually measured by electrorotation and finally sorted in two channels by dielectrophoretic force. Such systems can operate continuously, but the throughput is low.

Cen et al. [73] combined dielectrophoresis, traveling-wave dielectrophoresis and electrorotation on a single chip. Planar microelectrode array was manufactured using CMOS process technology. It had two metal layers, one layer are electrodes and one layer for electric connections of bonding pads and electrodes. Conductive ITO glass was used as cover forming a microfluidic channel. Concentric circles were used for levitation, and the dielectrophoretic force was adjusted to provide equilibrium with sedimentation force. Electrodes for traveling-wave dielectrophoresis were concentric circles with phase-shifted sine voltage delivered to them, so that the cells were moving radially between these electrodes. Electrodes for electrorotation consisted of four sets of electrodes with phase-shifted signals forming a rotating field. Measurement on Daudi and NCI-H929 cells showed that viable and nonviable cells have different capacitance of the cell membrane.

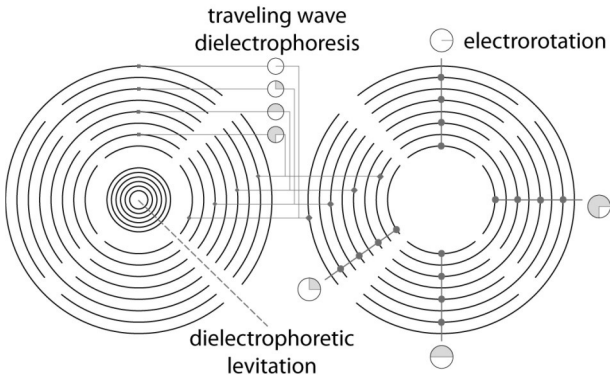

Figure 6: Electrodes for measuring cell properties by dielectrophoretic levitation, traveling wave dielectrophoresis and electrorotation. Adapted from [73].

4.5 Separation and fractionation of cells

For dielectrophoretic separation into two or fractionation into several subpopulations of cells, nonhomogeneous electric field is required. It can be generated using two different approaches – either by suitably shaping the electrodes, or by placing insulating structures into an otherwise homogeneous field generated by plate electrodes. In this section we present a concise overview of such devices and their use for dielectrophoretic separation and fractionation, while many fur-

ther details can be found in several comprehensive reviews that have been published recently [16], [77]–[82].

Typical shapes of planar thin-film electrodes are shown in Figure 7. They can be interdigitated [74], [83]–[85], castellated [86], curved [87], quadrupolar [15], or forming microwells [79]. These electrodes produce electric filed gradient both in the plane of the electrodes and perpendicularly to this plane.

Three-dimensional electrodes, some of which are shown in Figure 7, provide a better definition and control of the electric field and its gradient, but are generally more difficult to fabricate. In such designs, the chamber can be constructed from electrodes deposited both on the top and the bottom plate [88], or metallic posts can be extruded [89], or deposited in a thick layer by electroplating, thus forming vertical sidewalls [90]. The electrodes for generation of dielectrophoretic force can also be simple wires in reservoirs (similar to those in some electroporation chambers), with insulating pillars in the channel between the electrodes [91].

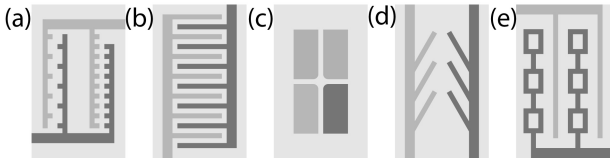

Figure 7: Classification of planar electrodes: (a) castellated, (b) interdigitated, (c) quadrupolar, (d) oblique, (e) microwells. Adapted from [79].

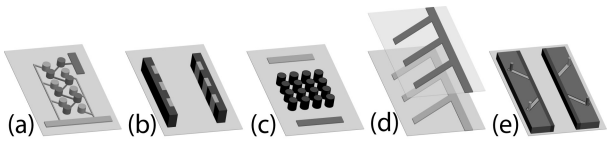

Figure 8: Classification of three-dimensional electrodes: (a) extruded, (b) sidewall patterned, (c) insulator-based, (d) top-bottom patterned and (e) contactless. Adapted from [79].

Many different strategies for cell separation can be used. Voldman et al. [89] describe a cell trapping method in a chamber with extruded metal electrodes, as shown in Figure 8a. For this method, a batch of cell suspension is injected in the chamber, and if two types of cells differ in their properties sufficiently, and an adequate field frequency is chosen, one type of cells from a mixture is trapped on the electrodes by positive dielectrophoresis, while the other type is repelled from them, flowing through the chamber. As the electric field is switched off, the trapped cells are released and also start flowing towards the output of the chamber.

Trapping of cells is also possible by negative dielectrophoresis on thin microwell electrodes, as shown in Figure 7e [92]. Here, one type of cells is immobilized in the center of the microwell, while other cells flow through the chamber. In contrast to trapping by positive dielectrophoresis, the cells are not exposed to high electric field, but the throughput is rather low.

Higher throughputs are achievable in chambers in which the dielectrophoretic force is used to change the trajectory of cells flowing through the channel. Han and Frazier [93] designed electrodes for lateral separation oriented at oblique angle according to fluid flow (Figure 7d), so that the dielectrophoretic force pushes the cells laterally either towards the center, or towards the sides of the channel. Their chamber has three output channels through which the separated cells leave the chamber and can be collected into three separate containers. Golden electrodes were deposited on glass with standard photolithography and the channel was made of PDMS bonded to glass. The device was used for separation of white and red blood cells, yielding samples of 92 % and 87 % purity, respectively.

Lewpiriyawong et al. [94] fabricated PDMS-based microfluidic device with sidewall AgPDMS electrodes. Along one side wall of the main channel 200 μm wide and 40 μm deep, there are four 100 μm wide AgPDMS electrodes, spaced 100 μm apart. This chamber was fabricated by patterning SU-8 on silicon wafer to create cavities for housing AgPDMS. Conducting paste (AgPDMS) with an electrical conductivity of ~2 $\times 10^4$ S/m was made by mixing 1 μm silver (Ag) particles with PDMS gel at a ratio of 85% w/w is filled into cavities. Channels were formed by molding PDMS and device was bonded to glass. This chamber, illustrated in Figure 9, has two inlets and two outlets. The cell suspension thus enters the chamber from one channel, while the other input channel is used for hydrodynamic focusing of cells. When the cells flow near the electrodes, they are either attracted to them or repelled from them, depending on the sign of the dielectrophoretic force. Separated cells are leaving the chamber continuously through two channels. This device was found useful for determining the cells' crossover frequency, as well as for separation of living and dead yeast cells, with efficiency of 97 % [94].

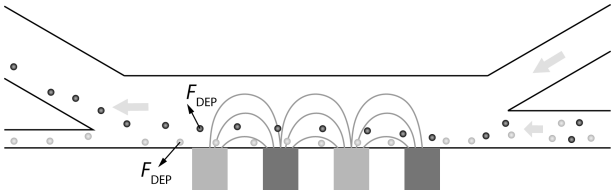

Figure 9: Dielectrophoretic separation with lateral "shift" of trajectories of cells. Adapted form [94].

Typically, the cells are separated by the sign of dielectrophoretic force, whereas separation by the magni-

tude of this force leads to separation by cell size due to its very strong dependence on cell size (proportional to r^3). Separation by other parameters is difficult, but the influence of cell size is decreased in dielectrophoretic field-flow fractionation (DEP-FFF) chambers, where separation is based on the balance between dielectrophoretic and gravitational force, which are both proportional to r^3 [95], [96]. Such chambers contain a long shallow channel with thin interdigitated electrodes at the bottom which create an electric field nonhomogeneous mainly in the vertical direction. At a properly selected frequency, the dielectrophoretic force pushes cells up, while sedimentation force pulls cell down. As the dielectrophoretic force decreases with the increasing distance from the electrodes, each cell reaches its steady-state position at a specific vertical position where the two forces are in equilibrium. The fluid flow in the shallow channels is laminar and has a parabolic velocity profile in vertical direction, so that the cells flowing at the bottom and the top of the channel flow through the chamber at the slowest rate, and the cells at the middle height flow the fastest. Due to different flow rates, vertical separation leads to horizontal separation along the channel, and allows for continuous separation if the chamber has two outputs at different vertical positions, and for batch separation if there is a single output, and the cells are collected into different containers at different times elapsed after the cells are injected at the channel's input. In this manner, DEP-FFF was found to be efficient in separation of tumor cells from healthy blood cells [38], and for separation of electroporated cells from non-porated ones [97].

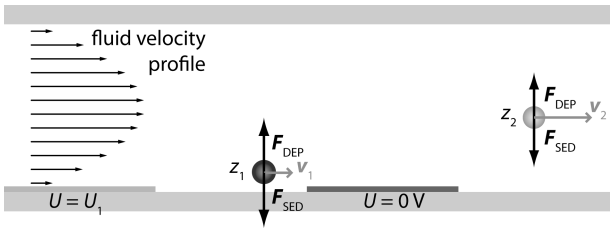

Figure 10: Dielectrophoretic field-flow fractionation

An alternative to metal microelectrodes is to use arrays of insulator structures to locally distort an otherwise homogeneous electrical field. In this technique, known as insulator dielectrophoresis (iDEP), metal macroelectrodes such as wire rods or machined metal plates are used to create a homogeneous electric field across an array of insulator structures. The insulator structures distort the field, creating its gradient. Glass, polymers or carbon can be used as insulator structures. The advantages are lower cost of fabrication and reduced metal-liquid interface effects, but as interelectode distances are in the range of millimeters, a rather higher voltage is required for efficient separation [82].

Macroelectrodes can also be positioned outside the channel, at its sides, or dipped into the channel at its inlet and outlet, with glass beads used as insulating structures. Channels with etched structures in glass, or structures from polymers provide better conditions for fluid flow. Thus Lapizco-Encinas et al. [98] fabricated an iDEP chamber with a channel 10 μm deep and etched in glass using standard photolithography, wet etching, and bonding techniques. Glass pillars as shown on Figure 8e distort the electric field generated between two platinum wires in channel inlet and outlet, distanced at 1 cm. In this design, the PDMS cover was reversibly bonded to the glass by vacuum. DC electric field with average amplitude up to 200 V/cm was used for trapping living bacteria, while dead bacteria passed through the channel untrapped.

iDEP devices have small surface of metal electrodes comparing to classical electrodes. Further modification of iDEP is contactless DEP (cDEP), where electrodes are insulated from cell suspension by a thin layer of PDMS [2], [99]. Channels filled with high conductive phosphate buffer saline form the electrodes (Figure 8e). Advantage of insulated electrodes are no contamination with metal ions, no bubble formation, and inexpensive fabrication suitable for disposable devices. These devices were used for characterisation of mouse ovaian cancer cells in different stages of cancere progression [76] and separation of tumor initiating cells from a population of human prostate cancer cells (PC3) [100].

Detection and separation of tumor initiating cells raised attention in the last years, since many people are diagnosed with cancer in late stages. Detection of tumor initiating cells using surface biomarkers is not reliable and too expensive for screening of large population of patients [101], howerer DEP is one of the methods thst allow for identification or/and separation of tumor initiating cells just by electrical properties without using any fluorescent markers [38], [100], [102], [103].

4.6 Cell patterning

DEP can be used for controlable patterning of biomaterials and bioactive structures for the formation of tissues and tissue-like structures [16].

It can be used for formation of cells to form artificial skin Yusvana at al. [104] fabricated interdigitated and castellated electrodes on ITO-covered glass to pattern skin cells to form artificial skin. Cells are collected between the electrodes and held for 10 min to adhere to each other. Fibrinogen and thrombin solution is added to atherent cells for further immobilisation. Xu et al. [105] designed a chip for dielectrophoretic patterning cells in micro-wells where they can be electroporated. Chamber

is constructed of bottom glass with gold electrodes and top cover glass with ITO electrode. For heterotypic cell positioning, different types of cells are separately introduced into the device, and the electrodes are selectively energized to trap different cells. Trapped cells can be electroporated and transfected with different plasmids.

4.7 Cell fusion

Both in conventional and microfluidic applications, cell fusion is a two-steps procedure. First, the cells are brought into close contact, typically achieved by dielectrophoretic force (generated either by shaping of the electrodes, or by placement of insulating structures into the channel). Second, strong electric pulses are delivered, causing the cells to electroporate and thus reach a fusogenic state. The use of the same electrodes for the two purposes simplifies the design, yet hampers the efficiency, as for dielectrophoretic alignment the field must be nonhomogeneous, while for electrofusion a homogeneous field is preferable, as to avoid both the irreversible electroporation of the cells that are exposed to a field too strong, and the lack of fusogenic state inducement in the cells that are exposed to a field that is too weak.

The first microfluidic chamber for cell electrofusion had two wire electrodes on a glass 0.1 to 0.2 mm apart, using positive dielectrophoresis to bring the cells into close contact before applying strong electric pulses that induced fusion [32]. Many adaptations of this design were published since [106].

The most typical shape of electrodes is castellated. Ju et al. [107] fabricated a chamber with thin Ti-Au electrodes, which are fabricated with standard soft lithography. Channels with fluidic ports are fabricated of PDMS. Cover can be opened, allowing for removal of fused cells with a pipette. Alignment of various plant cells was successful and yield of fused cells was 3-5 %, which is relatively low.

Electrodes thicker than the cell diameter offer highly controlled exposure of cells to electric field. Cao et al. [108] thus fabricated castellated gold electrodes 20 µm thick on silicon, with fabrication steps shown in Figure 11. Channels were etched in silicon wafer, followed by oxidation, titanium sputtering and etching, and gold sputtering and etching. Distance between two counter-electrodes in different chambers varied from 50 to 100 µm. For cell alignment, they used 1-4 MHz sine AC voltage, followed by electroporative DC pulses with electric field amplitudes ranging from 1 to 10 kV/cm, and a damped sine voltage delivered after the pulses to retain the contact between adjacent cells. For plant protoplasts, fusion efficiency of up to 44 % was obtained.

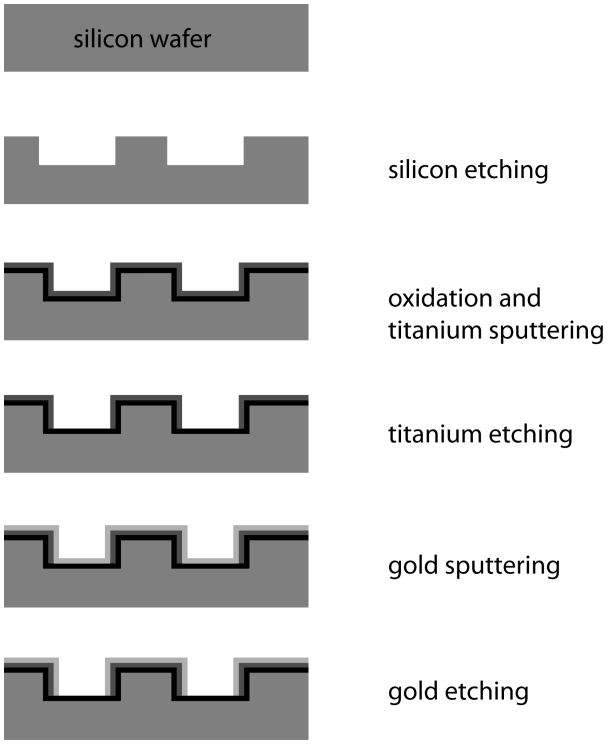

Figure 11: Fabrication steps of thick electrodes. Adapted from [108].

Hu at al. developed two types of thick castellated electrodes [48], [109]. Their first device was fabricated on silicon on an insulating substrate. A layer of highly doped silicon 40 µm thick served as vertical sidewalls of the microfluidic channel. On top of this layer, a thin aluminum film was deposited, patterned and etched by inductively coupled plasma etching. A film of SiO_2 was deposited on the fabricated surface using plasma-enhanced chemical vapor deposition, the unwanted SiO_2 was etched away, and then after another photolithography, channels were etched into the silicon. A PDMS cover with fluidic ports was bonded on the top to form a microfluidic channel. The shortest distance between electrodes was 60 µm, and 2-5 V at 1 MHz was used for dielectrophoretic cell alignment of HEK-293 cells and tobacco leaf protoplasts. The fusion efficiency of 40 % was obtained with a throughput of about 400 fused cells per hour in one channel.

Their second electrofusion chip consisted of a serpentine-shaped microchannel integrated with three-dimensional, thin-film microelectrode arrays fabricated on quartz glass substrate, and with a PDMS cover. The height of the channel was 25 µm and the distance between electrodes 80 µm. A thin film layers of titanium and gold were deposited on glass and patterned with standard lithography technology. A 40 µm thick Durimide 7510 layer was stacked onto the pattern obtained from the previous step, and the pattern of the microchannel was formed by standard lithography. The wafer

was then cured at a high temperature. During the curing procedure, the thickness of Durimide was reduced to 25 µm and the sidewalls reached a 65° inclination. A layer of resist was then deposited and patterned to protect the bottom of the channel, and finally a 300 nm film of gold was sputtered by a magnetron, and the unwanted gold was washed with acetone. In this manner, the three-dimensional microelectrode structure wrapping around the microchannel wall was formed. The chip was tested with K562 cells, which were dielectrophoretically aligned and then electroporated in the same manner as described above, yielding an average fusion efficiency of 43 %.

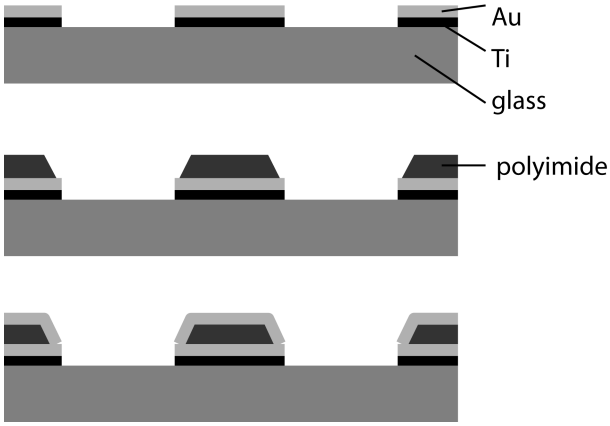

Figure 12: Basic schematics of fabrication steps of thick electrodes with gold layer over patterned polyimide Durimide 7510. Adapted from [48].

For most applications of cell fusion, the cells have to fuse pairwise, since multinucleate cells are typically not viable, and the two cells forming the fusing pair have to belong to two different types, so that the fused hybrid acquires the properties of both these types. In contrast, clustering of cells on simple microelectrodes is largely random, with fusion yielding many multi-cell and single-type hybrids. To improve the yield of the paired two-types hybrids, special structures are introduced into the microfluidic channels, and special protocols are developed.

Skeley et al. [110] thus fabricated a microfluidic device with thousands of single-cell traps formed as cup-shaped indentations in structures made of PDMS. The master for PDMS molding was made of SU-8, the electrodes were fabricated on glass slides from a thin film of chromium and then bonded with PDMS. The pairing of cells of two different types was achieved in three steps as shown on Figure 13. First, the cells were pumped through the chamber, getting trapped in the shallow cup-shaped traps. Second, the direction of flow was reversed, forcing the trapped cells to move directly into the deeper cup-shaped traps located on the opposite side of each trapping structure. Finally, another population of cells was loaded as to fill the remaining place in deeper cups, so that the formed cell pairs consisted of the two different types of cells. The cells were then electroporated by 50 µs pulses with amplitudes between 0.5 and 2 kV/cm. The pairing efficiency was about 70 %, and more than 50 % of all the cells were paired properly and fused.

Kemna et al. [111] used a similar approach and fabrication technique. With NS-1 and CD19+ B-cells, they obtained a fusion efficiency of about 50%, with a 1 % yield of functional hybridoma, which was considerably higher than the yield of the same hybridoma they were able to achieve by bulk electrofusion.

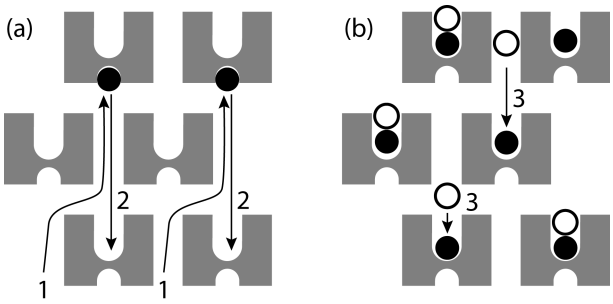

Figure 13: Cell electrofusion; (a) trapping of cells in small cups, reversing fluid flow and moving/shifting cells to large cups, (b) adding second type of cells, electroporation and cell fusion. Adapted from [110].

Another possibility for attaining a dielectrophoretic alignment of cells are insulating structures that concentrate the electric field. Masuda et al. [112] developed a microfluidic chip with two channels separated by a dielectric structure that allowed them to bring together a pair of cells of two different types, and then to electroporate and fuse them (Figure 14).
Mottet et al. [113] modified this design by enlarging the holes so that the fused cells could freely float through the channel, with the chip fabricated on a glass substrate. The dielectric structure separating the two channels had a thickness of 30 µm and a width of either 20 or 30 µm. One hole was about 30 µm wide and allowed for the focusing of the electric field. Thin gold electrodes were fabricated using a lift-off technique, and a thick SU-8 mold was formed on these thin electrodes as to form thick electrodes by electrodeposition (copper electroplating from sulfuric acid solution). SU-8 was then removed and a new layer of SU-8 deposited to form the walls of a channel. The channel was closed by bonding a dry SU-8 film and finally sealed by bonding a glass cover with fluid connectors. The glass cover of the chip allowed to monitor the cells being electrofused under a microscope.

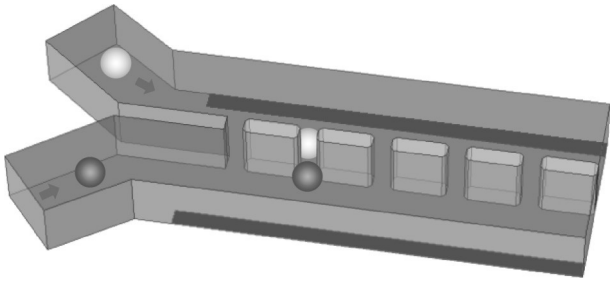

Figure 14: Electrofusion in a chamber with two channels separated by dielectric structures. Adapted from [113].

5 Conclusions

During the last two decades, many microfluidic devices for exposure of cells to electric field have been developed. They are typically made either on glass wafers with standard soft lithography, or out of inexpensive plastics such as PDMS, which can be replaced for every experiment. Among the advantages of small microfluidic devices, as opposed to larger bulk devices, are the highly controllable electric field, lower voltage on the electrodes, faster heat dissipation, small volume of reagents used, and *in situ* observation of the cell response. Still, current chambers are generally difficult to use and require external devices for operation. Compatibilization among these devices and their integration into purely microfluidic setups is expected to add considerable further value to the concept of an integrated *lab-on-a-chip*.

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References

1. J. Chen, J. Li, and Y. Sun, "Microfluidic approaches for cancer cell detection, characterization, and separation," Lab on a Chip, vol. 12, no. 10, p. 1753, 2012.
2. H. Shafiee, J. Caldwell, M. Sano, and R. Davalos, "Contactless dielectrophoresis: a new technique for cell manipulation," Biomed. Microdevices, vol. 11, no. 5, pp. 997–1006, 2009.
3. C. Liu, T. Stakenborg, S. Peeters, and L. Lagae, "Cell manipulation with magnetic particles toward microfluidic cytometry," Journal of Applied Physics, vol. 105, no. 10, p. 102014, 2009.
4. D.-H. Kim, P. K. Wong, J. Park, A. Levchenko, and Y. Sun, "Microengineered Platforms for Cell Mechanobiology," Annual Review of Biomedical Engineering, vol. 11, pp. 203–233, 2009.
5. M. Ni, W. H. Tong, D. Choudhury, N. A. A. Rahim, C. Iliescu, and H. Yu, "Cell Culture on MEMS Platforms: A Review," International Journal of Molecular Sciences, vol. 10, no. 12, pp. 5411–5441, 2009.
6. D. Mark, S. Haeberle, G. Roth, F. von Stetten, and R. Zengerle, "Microfluidic lab-on-a-chip platforms: requirements, characteristics and applications," Chem. Soc. Rev., vol. 39, no. 3, pp. 1153–1182, 2010.
7. E. Brouzes, M. Medkova, N. Savenelli, D. Marran, M. Twardowski, J. B. Hutchison, J. M. Rothberg, D. R. Link, N. Perrimon, and M. L. Samuels, "Droplet microfluidic technology for single-cell high-throughput screening," Proc. Natl. Acad. Sci. U. S. A., vol. 106, no. 34, pp. 14195–14200, 2009.
8. B. Eker, R. Meissner, A. Bertsch, K. Mehta, and P. Renaud, "Label-Free Recognition of Drug Resistance via Impedimetric Screening of Breast Cancer Cells," PLoS ONE, vol. 8, no. 3, p. e57423, 2013.
9. J. Hong, J. B. Edel, and A. J. deMello, "Micro- and nanofluidic systems for high-throughput biological screening," Drug Discovery Today, vol. 14, no. 3–4, pp. 134–146, 2009.
10. M.-H. Wu, S.-B. Huang, and G.-B. Lee, "Microfluidic cell culture systems for drug research," Lab Chip, vol. 10, no. 8, pp. 939–956, 2010.
11. R. N. Zare and S. Kim, "Microfluidic platforms for single-cell analysis," Annu. Rev. Biomed. Eng., vol. 12, pp. 187–201, 2010.
12. P. Tathireddy, Y.-H. Choi, and M. Skliar, "Particle AC electrokinetics in planar interdigitated microelectrode geometry," J. Electrostat., vol. 66, no. 11–12, pp. 609–619, 2008.
13. Q. Guan, S. D. Noblitt, and C. S. Henry, "Electrophoretic separations in poly(dimethylsiloxane) microchips using a mixture of ionic and zwitterionic surfactants," Electrophoresis, vol. 33, no. 2, pp. 379–387, 2012.
14. H. A. Pohl and J. S. Crane, "Dielectrophoresis of cells," Biophys. J., vol. 11, no. 9, pp. 711–727, 1971.
15. L.-S. Jang, P.-H. Huang, and K.-C. Lan, "Single-cell trapping utilizing negative dielectrophoretic quadrupole and microwell electrodes," Biosensors and Bioelectronics, vol. 24, no. 12, pp. 3637–3644, 2009.

16. Z. R. Gagnon, "Cellular dielectrophoresis: Applications to the characterization, manipulation, separation and patterning of cells," Electrophoresis, vol. 32, no. 18, pp. 2466–2487, 2011.
17. M. M. Meighan, S. J. R. Staton, and M. A. Hayes, "Bioanalytical separations using electric field gradient techniques," Electrophoresis, vol. 30, no. 5, pp. 852–865, 2009.
18. P. Patel and G. H. Markx, "Dielectric measurement of cell death," Enzyme Microb. Technol., vol. 43, no. 7, pp. 463–470, 2008.
19. T. B. Jones, "Basic theory of dielectrophoresis and electrorotation," IEEE Eng. Med. Biol. Mag., vol. 22, no. 6, pp. 33–42, 2003.
20. J. Voldman, "Electrical forces for microscale cell manipulation," Annu. Rev. Biomed. Eng., vol. 8, pp. 425–454, 2006.
21. E. Neumann and K. Rosenheck, "Permeability changes induced by electric impulses in vesicular membranes," J. Membrane Biol., vol. 10, pp. 279–290, 1972.
22. J. Weaver and Y. Chizmadzhev, "Theory of electroporation: A review," Bioelectrochem. Bioenerg., vol. 41, no. 2, pp. 135–160, 1996.
23. J. C. Weaver, "Electroporation of biological membranes from multicellular to nano scales," IEEE Trans. Dielect. Electr. Insul., vol. 10, no. 5, pp. 754–768, 2003.
24. T. Kotnik, P. Kramar, G. Pucihar, D. Miklavčič, and M. Tarek, "Cell membrane electroporation- Part 1: The phenomenon," IEEE Electrical Insulation Magazine, vol. 28, no. 5, pp. 14–23, 2012.
25. G. Serša, D. Miklavčič, M. Čemažar, Z. Rudolf, G. Pucihar, and M. Snoj, "Electrochemotherapy in treatment of tumours," Eur. J. Surg. Oncol., vol. 34, no. 2, pp. 232–240, 2008.
26. A. Gothelf and J. Gehl, "Gene Electrotransfer to Skin; Review of Existing Literature and Clinical Perspectives," Curr. Gene Ther., vol. 10, no. 4, pp. 287–299, 2010.
27. E. W. Lee, S. Thai, and S. T. Kee, "Irreversible electroporation: a novel image-guided cancer therapy," Gut Liver, vol. 4 Suppl 1, pp. 99–104, 2010.
28. M. Sack, J. Sigler, S. Frenzel, C. Eing, J. Arnold, T. Michelberger, W. Frey, F. Attmann, L. Stukenbrock, and G. Müller, "Research on Industrial-Scale Electroporation Devices Fostering the Extraction of Substances from Biological Tissue," Food Eng. Rev., vol. 2, no. 2, pp. 147–156, 2010.
29. M. Morales-de la Peña, P. Elez-Martínez, and O. Martín-Belloso, "Food preservation by pulsed electric fields: an engineering perspective," Food Eng. Rev., vol. 3, pp. 94–107, 2011.
30. T. Kotnik, F. Bobanović, and D. Miklavčič, "Sensitivity of transmembrane voltage induced by applied electric fields - a theoretical analysis," Bioelectrochem Bioenerg, vol. 43, no. 2, pp. 285–291, 1997.
31. D. Miklavčič and M. Puc, "Electroporation," in Wiley encyclopedia of biomedical engineering, M. Akay, Ed. Hoboken: Wiley-Interscience, 2006.
32. U. Zimmermann, "Electric field-mediated fusion and related electrical phenomena," Biochimica et Biophysica Acta (BBA) - Reviews on Biomembranes, vol. 694, no. 3, pp. 227–277, 1982.
33. M. Ušaj, K. Trontelj, R. Hudej, M. Kandušer, and D. Miklavčič, "Cell size dynamics and viability of cells exposed to hypotonic treatment and electroporation for electrofusion optimization," Radiol. Oncol., vol. 43, no. 2, pp. 108–119, 2009.
34. M. Ušaj, K. Trontelj, D. Miklavčič, and M. Kandušer, "Cell–cell electrofusion: optimization of electric field amplitude and hypotonic treatment for Mouse melanoma (B16-F1) and Chinese hamster ovary (CHO) cells," J. Membrane Biol., vol. 236, no. 1, pp. 107–116, 2010.
35. T. R. Hsu, MEMS and microsystems : design, manufacture, and nanoscale engineering, 2nd ed. John Wiley & Sons, 2008.
36. F. Chollet and H. Liu, A (not so) short introduction to Micro Electro Mechanical Systems, 3.0 ed. Singapore, 2009.
37. H. Becker and C. Gärtner, "Polymer microfabrication technologies for microfluidic systems," Analytical and Bioanalytical Chemistry, vol. 390, no. 1, pp. 89–111, 2007.
38. P. R. C. Gascoyne, J. Noshari, T. J. Anderson, and F. F. Becker, "Isolation of rare cells from cell mixtures by dielectrophoresis," Electrophoresis, vol. 30, no. 8, pp. 1388–1398, 2009.
39. B.-H. Jo, L. M. Van Lerberghe, K. M. Motsegood, and D. J. Beebe, "Three-dimensional micro-channel fabrication in polydimethylsiloxane (PDMS) elastomer," Journal of Microelectromechanical Systems, vol. 9, no. 1, pp. 76–81, 2000.
40. T. Tomov and I. Tsoneva, "Are the stainless steel electrodes inert?," Bioelectrochemistry, vol. 51, no. 2, pp. 207–209, 2000.
41. T. Kotnik, D. Miklavčič, and L. M. Mir, "Cell membrane electropermeabilization by symmetrical bipolar rectangular pulses - Part II. Reduced electrolytic contamination," Bioelectrochemistry, vol. 54, no. 1, pp. 91–95, 2001.
42. U. Friedrich, N. Stachowicz, A. Simm, G. Fuhr, K. Lucas, and U. Zimmermann, "High efficiency electrotransfection with aluminum electrodes using microsecond controlled pulses," Bioelectrochemistry and Bioenergetics, vol. 47, no. 1, pp. 103–111, 1998.
43. F. E. H. Tay, L. M. Yu, A. J. Pang, and C. Iliescu, "Electrical and thermal characterization of a dielectrophoretic chip with 3D electrodes for cells ma-

nipulation," Electrochim. Acta, vol. 52, no. 8, pp. 2862–2868, 2007.
44. H. Cong and T. Pan, "Microfabrication of conductive PDMS on flexible substrates for biomedical applications," in Nano/Micro Engineered and Molecular Systems, 2009. NEMS 2009. 4th IEEE International Conference on, 2009, pp. 731 –734.
45. X. Z. Niu, S. L. Peng, L. Y. Liu, W. J. Wen, and P. Sheng, "Characterizing and Patterning of PDMS-Based Conducting Composites," Adv. Mater., vol. 19, no. 18, pp. 2682–2686, 2007.
46. A. N. K. Lau, A. T. Ohta, H. L. Phan, H.-Y. Hsu, A. Jamshidi, P.-Y. Chiou, and M. C. Wu, "Antifouling coatings for optoelectronic tweezers," Lab Chip, vol. 9, no. 20, p. 2952, 2009.
47. C. Iliescu, L. M. Yu, G. L. Xu, and F. E. H. Tay, "A dielectrophoretic chip with a 3-D electric field gradient," J. Microelectromech. Syst., vol. 15, no. 6, pp. 1506–1513, 2006.
48. N. Hu, J. Yang, S. Qian, S. W. Joo, and X. Zheng, "A cell electrofusion microfluidic device integrated with 3D thin-film microelectrode arrays," Biomicrofluidics, vol. 5, no. 3, pp. 034121–034121–12, 2011.
49. C.-P. Jen and H.-H. Chang, "A handheld preconcentrator for the rapid collection of cancerous cells using dielectrophoresis generated by circular microelectrodes in stepping electric fields," Biomicrofluidics, vol. 5, p. 034101, 2011.
50. P. Sabounchi, A. M. Morales, P. Ponce, L. P. Lee, B. A. Simmons, and R. V. Davalos, "Sample concentration and impedance detection on a microfluidic polymer chip," Biomed Microdevices, vol. 10, no. 5, pp. 661–670, 2008.
51. A. T. Ohta, P. Y. Chiou, H. L. Phan, S. W. Sherwood, J. M. Yang, A. N. K. Lau, H. Y. Hsu, A. Jamshidi, and M. C. Wu, "Optically controlled cell discrimination and trapping using optoelectronic tweezers," IEEE J. Sel. Top. Quantum Electron., vol. 13, no. 2, pp. 235–243, 2007.
52. M. B. Fox, D. C. Esveld, A. Valero, R. Luttge, H. C. Mastwijk, P. V. Bartels, A. van den Berg, and R. M. Boom, "Electroporation of cells in microfluidic devices: a review," Anal. Bioanal.Chem., vol. 385, no. 3, pp. 474–485, 2006.
53. S. K. Kim, J. H. Kim, K. P. Kim, and T. D. Chung, "Continuous Low-Voltage dc Electroporation on a Microfluidic Chip with Polyelectrolytic Salt Bridges," Anal. Chem., vol. 79, no. 20, pp. 7761–7766, 2007.
54. W. G. Lee, U. Demirci, and A. Khademhosseini, "Microscale electroporation: challenges and perspectives for clinical applications," Integr. Biol., vol. 1, no. 3, pp. 242–251, 2009.
55. W. Longsine-Parker, H. Wang, C. Koo, J. Kim, B. Kim, A. Jayaraman, and A. Han, "Microfluidic electro-sonoporation: a multi-modal cell poration methodology through simultaneous application of electric field and ultrasonic wave," Lab Chip, vol. 13, no. 11, pp. 2144–2152, 2013.
56. M. Shahini and J. T. W. Yeow, "Cell electroporation by CNT-featured microfluidic chip," Lab Chip, vol. 13, no. 13, pp. 2585–2590, 2013.
57. A. Adamo, A. Arione, A. Sharei, and K. F. Jensen, "Flow-Through Comb Electroporation Device for Delivery of Macromolecules," Anal. Chem., vol. 85, no. 3, pp. 1637–1641, 2013.
58. D. Selmeczi, T. S. Hansen, Ö. Met, I. M. Svane, and N. B. Larsen, "Efficient large volume electroporation of dendritic cells through micrometer scale manipulation of flow in a disposable polymer chip," Biomedical Microdevices, vol. 13, no. 2, pp. 383–392, 2011.
59. J. Kim, I. Hwang, D. Britain, T. D. Chung, Y. Sun, and D.-H. Kim, "Microfluidic approaches for gene delivery and gene therapy," Lab Chip, vol. 11, no. 23, pp. 3941–3948, 2011.
60. A. Valero, J. N. Post, J. W. van Nieuwkasteele, P. M. ter Braak, W. Kruijer, and A. van den Berg, "Gene transfer and protein dynamics in stem cells using single cell electroporation in a microfluidic device," Lab Chip, vol. 8, no. 1, pp. 62–67, 2008.
61. S. Vassanelli, L. Bandiera, M. Borgo, G. Cellere, L. Santoni, C. Bersani, M. Salamon, M. Zaccolo, L. Lorenzelli, S. Girardi, M. Maschietto, M. Dal Maschio, and A. Paccagnella, "Space and time-resolved gene expression experiments on cultured mammalian cells by a single-cell electroporation microarray," N Biotechnol, vol. 25, no. 1, pp. 55–67, 2008.
62. J. A. Kim, K. Cho, Y. S. Shin, N. Jung, C. Chung, and J. K. Chang, "A multi-channel electroporation microchip for gene transfection in mammalian cells," Biosens. Bioelectron., vol. 22, no. 12, pp. 3273–3277, 2007.
63. H. Y. Wang and C. Lu, "Electroporation of mammalian cells in a microfluidic channel with geometric variation," Anal. Chem., vol. 78, no. 14, pp. 5158–5164, 2006.
64. Y. Zhan, Z. Cao, N. Bao, J. Li, J. Wang, T. Geng, H. Lin, and C. Lu, "Low-frequency ac electroporation shows strong frequency dependence and yields comparable transfection results to dc electroporation," J. Control. Release, vol. 160, no. 3, pp. 570–576, 2012.
65. Y.-C. Lin, C.-M. Jen, M.-Y. Huang, C.-Y. Wu, and X.-Z. Lin, "Electroporation microchips for continuous gene transfection," Sensors and Actuators B: Chemical, vol. 79, no. 2–3, pp. 137–143, 2001.
66. Y. Zhan, J. Wang, N. Bao, and C. Lu, "Electroporation of Cells in Microfluidic Droplets," Analytical Chemistry, vol. 81, no. 5, pp. 2027–2031, 2009.

67. L. A. MacQueen, M. D. Buschmann, and M. R. Wertheimer, "Gene delivery by electroporation after dielectrophoretic positioning of cells in a non-uniform electric field," Bioelectrochemistry, vol. 72, no. 2, pp. 141–148, 2008.
68. Y. Huang and B. Rubinsky, "Microfabricated electroporation chip for single cell membrane permeabilization," Sens. Actuators A Phys, vol. 89, no. 3, pp. 242–249, 2001.
69. H. Lu, M. A. Schmidt, and K. F. Jensen, "A microfluidic electroporation device for cell lysis," Lab Chip, vol. 5, no. 1, pp. 23–29, 2005.
70. H. Sedgwick, F. Caron, P. B. Monaghan, W. Kolch, and J. M. Cooper, "Lab-on-a-chip technologies for proteomic analysis from isolated cells," J. R. Soc. Interface, vol. 5, pp. S123–S130, 2008.
71. C. de la Rosa, P. A. Tilley, J. D. Fox, and K. V. I. Kaler, "Microfluidic Device for Dielectrophoresis Manipulation and Electrodisruption of Respiratory Pathogen Bordetella pertussis," IEEE Transactions on Biomedical Engineering, vol. 55, no. 10, pp. 2426 –2432, 2008.
72. T. Müller, G. Gradl, S. Howitz, S. Shirley, T. Schnelle, and G. Fuhr, "A 3-D microelectrode system for handling and caging single cells and particles," Biosens. Bioelectron., vol. 14, no. 3, pp. 247–256, 1999.
73. E. G. Cen, C. Dalton, Y. Li, S. Adamia, L. M. Pilarski, and K. V. I. S. Kaler, "A combined dielectrophoresis, traveling wave dielectrophoresis and electrorotation microchip for the manipulation and characterization of human malignant cells," J. Microbiol. Methods, vol. 58, no. 3, pp. 387–401, 2004.
74. B. G. Hawkins, C. Huang, S. Arasanipalai, and B. J. Kirby, "Automated dielectrophoretic characterization of Mycobacterium smegmatis," Anal. Chem., vol. 83, no. 9, pp. 3507–3515, 2011.
75. P. R. C. Gascoyne, S. Shim, J. Noshari, F. F. Becker, and K. Stemke-Hale, "Correlations between the dielectric properties and exterior morphology of cells revealed by dielectrophoretic field-flow fractionation," Electrophoresis, vol. 34, no. 7, pp. 1042–1050, 2013.
76. A. Salmanzadeh, M. B. Sano, R. C. Gallo-Villanueva, P. C. Roberts, E. M. Schmelz, and R. V. Davalos, "Investigating dielectric properties of different stages of syngeneic murine ovarian cancer cells," Biomicrofluidics, vol. 7, no. 1, 2013.
77. D. R. Gossett, W. M. Weaver, A. J. Mach, S. C. Hur, H. T. K. Tse, W. Lee, H. Amini, and D. Di Carlo, "Label-free cell separation and sorting in microfluidic systems," Anal Bioanal Chem, vol. 397, no. 8, pp. 3249–3267, 2010.
78. G. Xu, F. E. H. Tay, G. Tresset, F. S. Iliescu, A. Avram, and C. Iliescu, "Recent trends in dielectrophoresis," Inform. Midem, vol. 40, no. 4, pp. 253–262, 2010.
79. K. Khoshmanesh, S. Nahavandi, S. Baratchi, A. Mitchell, and K. Kalantar-zadeh, "Dielectrophoretic platforms for bio-microfluidic systems," Biosens. Bioelectron., vol. 26, no. 5, pp. 1800–1814, 2011.
80. L. Yang, "A review of multifunctions of dielectrophoresis in biosensors and biochips for bacteria detection," Anal. Lett., vol. 45, no. 2–3, pp. 187–201, 2012.
81. L. A. Macqueen, M. Thibault, M. D. Buschmann, and M. R. Wertheimer, "Electro-manipulation of biological cells in microdevices," IEEE Transactions on Dielectrics and Electrical Insulation, vol. 19, no. 4, pp. 1261 –1268, 2012.
82. R. Martinez-Duarte, "Microfabrication technologies in dielectrophoresis applications—A review," Electrophoresis, vol. 33, no. 21, pp. 3110–3132, 2012.
83. P. R. C. Gascoyne, X. B. Wang, Y. Huang, and F. F. Becker, "Dielectrophoretic separation of cancer cells from blood," IEEE Trans. Ind. Appl., vol. 33, no. 3, pp. 670–678, 1997.
84. G. H. Markx, R. Pethig, and J. Rousselet, "The dielectrophoretic levitation of latex beads, with reference to field-flow fractionation," J. Phys. D: Appl. Phys., vol. 30, no. 17, p. 2470, 1997.
85. D. Holmes, N. G. Green, and H. Morgan, "Microdevices for dielectrophoretic flow-through cell separation," IEEE Eng. Med. Biol. Mag., vol. 22, no. 6, pp. 85–90, 2003.
86. J. Oblak, D. Križaj, S. Amon, A. Maček-Lebar, and D. Miklavčič, "Feasibility study for cell electroporation detection and separation by means of dielectrophoresis," Bioelectrochemistry, vol. 71, no. 2, pp. 164–171, 2007.
87. K. Khoshmanesh, C. Zhang, F. Tovar-Lopez, S. Nahavandi, S. Baratchi, A. Mitchell, and K. Kalantar-Zadeh, "Dielectrophoretic-activated cell sorter based on curved microelectrodes," Microfluid. Nanofluid., vol. 9, pp. 411–426, 2010.
88. Aldaeus, Y. Lin, J. Roeraade, and G. Amberg, "Superpositioned dielectrophoresis for enhanced trapping efficiency," Electrophoresis, vol. 26, no. 22, pp. 4252–4259, 2005.
89. J. Voldman, M. Toner, M. L. Gray, and M. A. Schmidt, "Design and analysis of extruded quadrupolar dielectrophoretic traps," J. Electrostat., vol. 57, no. 1, pp. 69–90, 2003.
90. L. S. Wang, L. Flanagan, and A. P. Lee, "Side-wall vertical electrodes for lateral field microfluidic applications," J. Microelectromech. Syst., vol. 16, no. 2, pp. 454–461, 2007.
91. E. B. Cummings and A. K. Singh, "Dielectrophoresis in microchips containing arrays of insulating posts: Theoretical and experimental results," Anal. Chem., vol. 75, no. 18, pp. 4724–4731, 2003.

92. R. S. W. Thomas, P. D. Mitchell, R. O. C. Oreffo, and H. Morgan, "Trapping single human osteoblast-like cells from a heterogeneous population using a dielectrophoretic microfluidic device," Biomicrofluidics, vol. 4, no. 2, p. 022806, 2010.
93. K.-H. Han and A. B. Frazier, "Lateral-driven continuous dielectrophoretic microseparators for blood cells suspended in a highly conductive medium," Lab Chip, vol. 8, no. 7, p. 1079, 2008.
94. N. Lewpiriyawong, K. Kandaswamy, C. Yang, V. Ivanov, and R. Stocker, "Microfluidic characterization and continuous separation of cells and particles using conducting poly(dimethyl siloxane) electrode induced alternating current-dielectrophoresis," Anal. Chem., vol. 83, no. 24, pp. 9579–9585, 2011.
95. Y. Huang, X. B. Wang, F. F. Becker, and P. R. C. Gascoyne, "Introducing dielectrophoresis as a new force field for field-flow fractionation," Biophys. J., vol. 73, no. 2, pp. 1118–1129, 1997.
96. J. Čemažar, D. Vrtačnik, S. Amon, and T. Kotnik, "Dielectrophoretic field-flow microchamber for separation of biological cells based on their electrical properties," IEEE Trans. Nanobiosci., vol. 10, no. 1, pp. 36–43, 2011.
97. J. Čemažar and T. Kotnik, "Dielectrophoretic field-flow fractionation of electroporated cells," Electrophoresis, vol. 33, no. 18, pp. 2867–2874, 2012.
98. B. H. Lapizco-Encinas, R. V. Davalos, B. A. Simmons, E. B. Cummings, and Y. Fintschenko, "An insulator-based (electrodeless) dielectrophoretic concentrator for microbes in water," J. Microbiol. Methods, vol. 62, no. 3, pp. 317–326, 2005.
99. M. B. Sano, J. L. Caldwell, and R. V. Davalos, "Modeling and development of a low frequency contactless dielectrophoresis (cDEP) platform to sort cancer cells from dilute whole blood samples," Biosens. Bioelectron., vol. 30, no. 1, pp. 13–20, 2011.
100. A. Salmanzadeh, L. Romero, H. Shafiee, R. C. Gallo-Villanueva, M. A. Stremler, S. D. Cramer, and R. V. Davalos, "Isolation of prostate tumor initiating cells (TICs) through their dielectrophoretic signature," Lab on a Chip, vol. 12, no. 1, pp. 182–189, 2012.
101. C. Yu, Z. Yao, J. Dai, H. Zhang, J. Escara-Wilke, X. Zhang, and E. T. Keller, "ALDH Activity Indicates Increased Tumorigenic Cells, But Not Cancer Stem Cells, in Prostate Cancer Cell Lines," In Vivo, vol. 25, no. 1, pp. 69–76, 2011.
102. S. Shim, K. Stemke-Hale, A. M. Tsimberidou, J. Noshari, T. E. Anderson, and P. R. C. Gascoyne, "Antibody-independent isolation of circulating tumor cells by continuous-flow dielectrophoresis," Biomicrofluidics, vol. 7, no. 1, pp. 011807–011807–12, 2013.
103. V. Tirino, V. Desiderio, F. Paino, A. D. Rosa, F. Papaccio, M. L. Noce, L. Laino, F. D. Francesco, and G. Papaccio, "Cancer stem cells in solid tumors: an overview and new approaches for their isolation and characterization," FASEB J, vol. 27, no. 1, pp. 13–24, 2013.
104. R. Yusvana, D. J. Headon, and G. H. Markx, "Creation of arrays of cell aggregates in defined patterns for developmental biology studies using dielectrophoresis," Biotechnology and Bioengineering, vol. 105, no. 5, pp. 945–954, 2010.
105. Y. Xu, H. Yao, L. Wang, W. Xing, and J. Cheng, "The construction of an individually addressable cell array for selective patterning and electroporation," Lab on a Chip, vol. 11, no. 14, p. 2417, 2011.
106. N. Hu, J. Yang, S. W. Joo, A. N. Banerjee, and S. Qian, "Cell electrofusion in microfluidic devices: A review," Sensors and Actuators B: Chemical, vol. 178, pp. 63–85, 2013.
107. J. Ju, J.-M. Ko, H.-C. Cha, J. Y. Park, C.-H. Im, and S.-H. Lee, "An electrofusion chip with a cell delivery system driven by surface tension," J. Micromech. Microeng., vol. 19, no. 1, p. 015004, Jan. 2009.
108. Y. Cao, J. Yang, Z. Q. Yin, H. Y. Luo, M. Yang, N. Hu, D. Q. Huo, C. J. Hou, Z. Z. Jiang, R. Q. Zhang, R. Xu, and X. L. Zheng, "Study of high-throughput cell electrofusion in a microelectrode-array chip," Microfluid. Nanofluid., vol. 5, no. 5, pp. 669–675, 2008.
109. N. Hu, J. Yang, Z.-Q. Yin, Y. Ai, S. Qian, I. B. Svir, B. Xia, J.-W. Yan, W.-S. Hou, and X.-L. Zheng, "A high-throughput dielectrophoresis-based cell electrofusion microfluidic device," Electrophoresis, vol. 32, pp. 2488–2495, 2011.
110. A. M. Skelley, O. Kirak, H. Suh, R. Jaenisch, and J. Voldman, "Microfluidic control of cell pairing and fusion," Nat. Meth., vol. 6, no. 2, pp. 147–152, 2009.
111. E. W. M. Kemna, F. Wolbers, I. Vermes, and A. van den Berg, "On chip electrofusion of single human B cells and mouse myeloma cells for efficient hybridoma generation," Electrophoresis, vol. 32, no. 22, pp. 3138–3146, 2011.
112. S. Masuda, M. Washizu, and T. Nanba, "Novel method of cell fusion in field constriction area in fluid integration circuit," IEEE Transactions on Industry Applications, vol. 25, no. 4, pp. 732 –737, 1989.
113. G. Mottet, B. Le Pioufle, and L. M. Mir, "High-resolution analyses of cell fusion dynamics in a biochip," Electrophoresis, vol. 33, no. 16, pp. 2508–2515, 2012.

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A fast simulation emulation engine

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Abstract: Due to the number of functionalities built on the system development, a mixed hardware software systems has increased. To solve the problem of the cost, the flexibility, the time-to-market and the resulting behaviors, many verification methods are used in the literature. This paper describes a new hardware/software co-verification method for System-On–a-Chip, based on the integration of a SystemC simulator and an FPGA accelerator. Between the SystemC simulator [1,2] and the FPGA hardware platform, a simulation / emulation engine based on different synchronization scheme was established to accelerate the verification and to control the context switch. This work presents an extension for CODIS tool and it enables not only an easy and a high verification speed, with a low cost, but also it presents the real behavior of hardware / software.

Keywords: Simulation; Emulation; SystemC ; Transaction Level Modeling; FPGA; Synchronization.

Hitro simulacijsko emulacijsko orodje

Izvleček: Z rastjo števila vgrajenih uporabnosti v sisteme naraščajo sistemi z mešano programsko in strojno opremo. Številne verifikacijske metode so uporabljene v literaturi za reševanje problemov stroškov, fleksibilnosti, časa do predstavitvena trgu in rezultirajočega obnašanja. V članku je predstavljena nova programsko/strojna metoda za verifikacijo sistema na čipu, ki temelji na integraciji SystemC simulatorja in FPGA pospeševalnika. Med simulatorjem SystemC [1,2] in FPGA platformo je postavljeno simulacijsko/emulacijsko orodje, ki temelji na različnih sinhronizacijskih shemah in pospešuje verifikacijo in nadzor nad vsebinskim stikalom. Delo predstavlja razširitev CODIS orodja in ne predstavlja le enostavno in zelo hitro verifikacijo temveč dejansko obnašanje strojne in programske opreme.

Ključne besede: simulacija, emulacija, SystemC, nivojsko modeliranje, FPGA, sinhronizacija

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1 Introduction

Embedded systems are mostly heterogeneous devices. Their design is based on hardware and software components. These parts cannot be developed independently, since their interaction is a key point of the system behavior. Each part needs to be aware of the characteristics of the other parts, in order to provide optimized components. The best strategy adopted is co-design, since it allows us to develop HW/SW component concurrently [3].

Co-simulation is a key methodology in co-design that allows verification of the hardware, the software, and their interaction. The essential aim of the co-simulation is to validate and to cover the performance as well as the functionality. The main problem appears when the system complexity grows and the validation becomes more and more time consuming. To overcome this challenge, and speed up HW/SW co-simulation, many synchronization schemes are used.

As mentioned bellow, this paper presents an addition work for CODIS platform. CODIS (COntinuous DIscrete Simulation) [18] is a tool which can automatically produces co-simulation instances for continuous/discrete systems simulation using SystemC and Simulink simulators. This is done by generating and providing co-simulation interfaces and the co-simulation bus. To evaluate the performances of simulation models generated in CODIS, they measured the overhead given by the simulation interfaces.

This paper is organized as follows. Section 2 summarizes existing work on HW/SW co-simulation. Section 3 explains the proposed solution to accelerate the co-simulation. Section 4 presents the Simulation Emulation engine and his architecture. Finally, experimental results are discussed in section 5, and concluding remarks in section 6.

2 Related work

Several co-simulation frameworks have been proposed in the literature. They can be classified into two main categories: homogenous and heterogeneous.

Homogenous frameworks [22] [23] use a single simulator for the simulation of both HW/SW components. The main advantage of this category is the simplification of the design modeling and the good simulation performance. However, homogenous frameworks suffer from the huge time consummation and they are suitable only in a very initial phase of the design, prior to HW/SW partitioning.

Inversely, heterogeneous frameworks [19] [24] [25] warrant a more accurate tuning between HW/SW components and save much time in simulation. The major problem in this category is the communication and synchronization.

Several frameworks [4] [5] [6] are mainly focused on Multilanguage system description, that is, an HDL for hardware and a programming language for software.

All these heterogeneous co-simulations are based on solving the problems of controlling and synchronization several simulation engines. These frameworks are adopted because of the best simulation performance and the easiest integration but it was the only possible choice when VHDL or Verilog simulation was the highest possible level of abstraction for simulating hardware. To surmount this challenge, SystemC is more adopted in hardware description. The advantage of design with SystemC [7] [8] [9] is the use of the bus as different abstraction layer to obtain more efficient co-simulation and the HW/SW process are described on C. This approach simplifies the implementation of the initial model as well as the HW / SW partitioning. In fact, HW components are simulated by using the SystemC simulation kernel, while SW programs run on an Instruction Set Simulator (ISS) [20] [21].

These frameworks are based on two essential steps. The first is the Inter Process Communication (IPC) [26] [27]. It is used to make the communication between the ISS and the SystemC simulator. The second is the Bus Wrapper. It ensures synchronization between SystemC simulator and the ISS.

But these frameworks still suffer from some performance bottlenecks, caused by the use of the ISS. However, ISS gives the best simulation accuracy. To accelerate the simulation, in spite of the accuracy, the native SW simulation is adopted using SystemC and time annotations. Some works try to improve the performance estimation accuracy in native simulation by modeling and simulating the OS behavior essentially the interruptions and preemption mechanism [10] [11].

Other works like [17] are based on multi-ISS to accelerate the simulation. But these frameworks suffer not only from a complex synchronization scheme that increases the overhead but also from the grandiose simulation time.

3 Conventional approaches

To increase the verification speed while maintaining clock accuracy, an FPGA (Field Programmable Gate Array) such as ALTERA DE2-70 is used. The FPGA presents an easy and a fast environment for the target architecture implementation. As known, if all modeled blocks are implemented in hardware emulation, the system cost, as well as the running and debugging cost, will become expensive. Therefore, a combined method using an emulator and a simulator is the most adopted to model SOCs (System On Chip).

One method is based on an abstraction approach [12]. This approach uses only few FPGAs operating at about 1 MHZ. This method is similar to an accelerated C/C++ simulation. So it suffers from lack of performance estimation and no debugging.

Another method uses a transaction level C/C++ simulator to model the application program [13], and the FPGA to emulate the HW component.

A verification system that uses SystemC simulator to simulate the HW component and FPGA board based on target kernel architecture to simulate the SW application is proposed. The key contribution of this work is in the interoperability between the SystemC scheduler, and the target kernel architecture deployed on the FPGA.

The main advantages of our solution are:

- Increase the speed of SW validation without any lost of accuracy since SW will be executed by the target microprocessor.
- The base architecture (processor, bus and memory) is implemented in FPGA and the specific hardware components are described and simulated using SystemC.
- This framework represents a very useful platform for software engineers to validate their code before the hardware components become available
- The replacement of the ISS by a real target processor accelerates the simulation.

– A synchronization schemes between HW and SW are described in this paper with respect of the synchronization schemes between continuous and discrete design used in CODIS tool.
– The target base architecture is implemented in FPGA board at earlier stage. This fact conserves the time to market and informs the software engineers early about many characteristics as well as the time execution of the SW components, energy consumption, etc.
– The *interface* module provides the communication and the synchronization without modifying the SystemC kernel.

Figure 1 shows the verification environment. Two steps are essential to make the environment verification: communication and synchronization model. A Simulation Emulation engine is described in the next section.

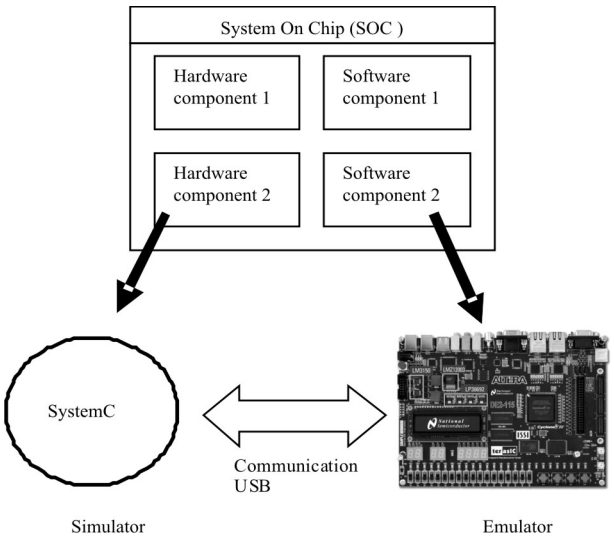


Figure 1: Combined simulator and emulator approach

4 Simulation emulation engine

Simulation engine presents the main problem of the majority of co-simulations environments. It ensures not only the communication between simulators and emulators but also the synchronization and the control. Figure 2 shows the Simulation/Emulation engine architecture. This section describes the communication and the synchronization layers with the implementation adopted.

4.1 Communication

This under section gives a brief introduction to the communication model and the associated library. A USB (Universal Serial Bus) link is used in the communication between PC and FPGA because this kind of communication has better speed than PCI which it adopted in emulation [14]. The model is divided into receiving / transmitting drivers models. Figure 3 shows the different steps of the communication.

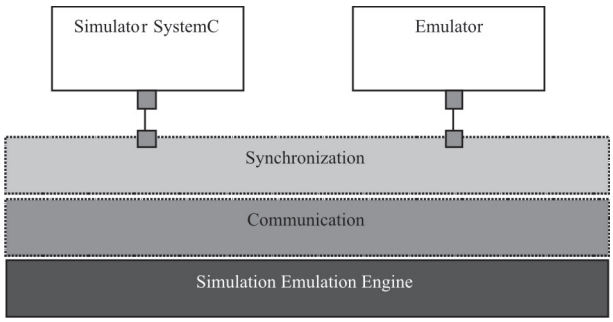


Figure 2: Simulation/Emulation engine architecture

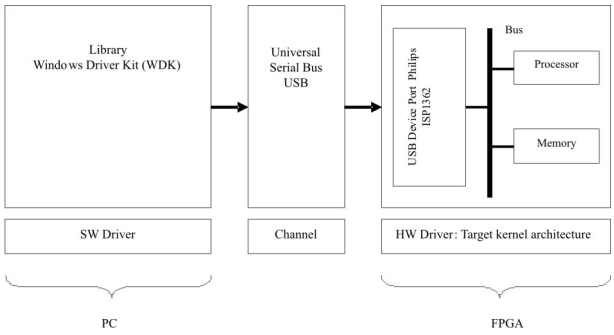


Figure 3: Communication model

- SW driver is made by Windows Driver Kit (WDK). This driver is responsible for the data transmission to and from the USB device. An operating system driver, running on the host system, responsible for receiving data from the high level application, forming the information packets as defined by the USB standard protocol, and also in charge for transmission of the data packet to the USB device. This driver will also be in charge of receiving data form the USB core (ISP1362), and deliver the received data to the high level application.

This driver contains essentially two main functions Read and Write. To achieve these two functions, four Win32 functions are used:
– CreateFile: required to connect application and USB core.
– WriteFile: required for data transfer into USB core.
– ReadFile: required for data transfer from the USB core into the application.
– ControlIODevice: requested for driver configuration.

- Channel: after the comparison research between the different kinds of communication channels, a USB communication is adopted not only because the portability but also because the speed of transaction is 480 Mbits/s; however, the speed of PCI is only 133 Mbits/s.

- **HW driver** is based on Philips ISP1362 device core that is integrated in emulation architecture with a processor, bus and memory, as shown in the Figure 3. The ISP1362 will manage the complete USB protocol from the device side, and which will also be in charge of leaving the received data in a buffer for resending when required. Note that the ISP1362 controller is used only in emulation environment and not be considered in the target architecture.

The ISP1362 provides the PIO (Programmed Input/Output) mode for the processor to access its internal control registers and buffer memory. An interruption mode is adopted to simulate the real behavior.

When an interrupt is activated, the processor halts normal operation and jump to the Interrupt Vector Table, which is a region of memory. There is one interrupt vector for each type of interrupt that can occur, and each interrupt vector is located at a unique memory address in the table. Each interrupt vector contains the address of the start of the Interrupt Service Routine (ISR) that will run for that interrupt. The ISR retrieves data from the ISP1362 Device Controller's internal FIFO (First In First Out) to NIOS II memory and sets up proper event flags to execute the program [15].

The ISR is like a subroutine and contains code that is executed once the ISR is entered. Once the code in the ISR is completed, control is passed back to the main program. If an interrupt event were to occur during this period, the processor halt the last interrupt program and jump to next interrupt program. When, it finished the processor go back to first interrupt program. This model is adopted to avoid the lost of data.

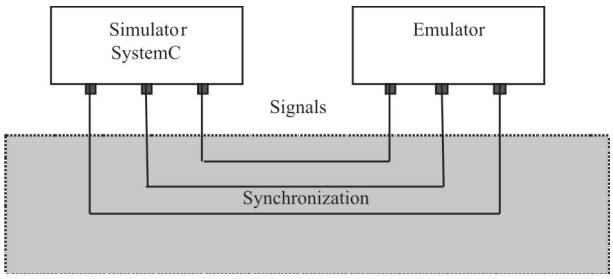
4.2 Synchronization schemes

A key part of the proposed verification is at first the synchronization schemes between the SystemC simulator and the target base architecture on FPGA board. Secondly, the model of synchronization between the different component of the Device Under Test (DUT). Note that the synchronization schemes ignored the communication overhead and focus in the process simulation.

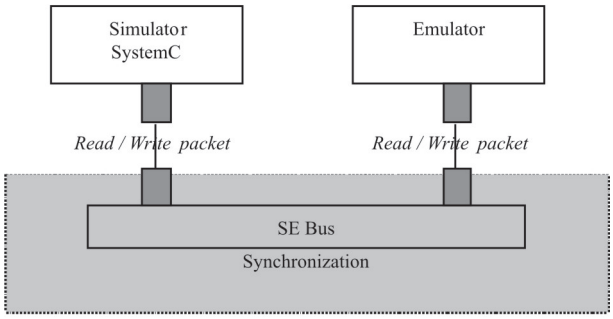
4.2.1 Simulator/Emulator Synchronization

We focus in this first part into the synchronization model between simulator and emulator. The SystemC simulator is fixed as the master of environment verification and the emulator based on target base architecture as slave.

The synchronization models are different form layer to layer. In RTL (Register Transfer Layer) layer the simulator and the emulator are interconnected with signals. While, the simulation/emulation bus ensures the transfer of data packet, in the TLM (Transaction Level Modeling) layer. Figure 4 a) shows the synchronization scheme for the RTL layer. Context switch presents the main function of the Simulation/Emulation (SE) bus. It assures the change of the control between simulator and emulator. Figure 4 b) describes the functionality of the Simulation/Emulation (SE) bus.



a) Simulation/Emulation bus in RTL



b) Simulation/Emulation bus in TLM

Figure 4: Simulation/Emulation Bus

The TLM layer is the most adopted in verification language because it is easier and faster than RTL layer.

The communication so described in the last section ensures packets forms which are constructed as interface between simulator and emulator (board).

Two forms of exchanged packets are used to perform the synchronization scheme between the simulator and the emulator, Figure 5.

Interruption packet shown in Figure 5 a) is the first form. It consists of two parts: a header and a body. The last one contains the routine number and the interruption time stamp. The header of this form presents the type of synchronization and the routine number indicates the routine Task to be executed. The time stamp represents a synchronization point [31] and it is used to execute the interrupt routine at the appropriate instant.

Data packet shown in Figure 5 b) is the second form. It comprises a header and the data. The header in this case contains the synchronization type, the size of data to send and the time stamp to synchronize when it is necessary.

Note that any packet received by the target processor side generates an USB interruption that can be exploit in the implementation phase to interrupt the target processor each time a packet is received.

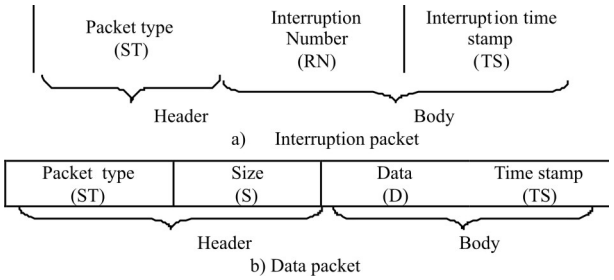


Figure 5: Synchronization forms

The verification method is based on the following synchronization schemes which respect the interaction style that can be involved between HW and SW components and the interaction style between continuous and discrete model used in CODIS tool. Note that, in the same design, HW and SW components may use different synchronization schemes. The execution time of SW applications in the target base architecture is considered as simulation time.

- Scheme 1: The SW Task receives data periodically from the hardware Task.

This scheme is based on FIFO memory between SW Task and HW Task. The main idea consists on fixed synchronization time between simulator and emulator (see Figure 6). Because of the difference of speed, the HW imposes a synchronization Time (T_{sync}). This T_{sync} must be more than HW or SW Tasks time.

- Scheme 2: The SW Task waits the end of the hardware Task.

When a hardware component is simulated by SystemC, the SW Task uses a waiting loop for data (see Figure 7). Once the hardware Task (Task1) is finished, the simulator sends data to the SW Task and a context witch from SystemC to board is taken. At this time, the SW Task receives data and resumes the execution. Here, the execution time of Task1 is modeled by the SystemC wait() function. The amount of time used by the wait function is sent to the SW part to inform it about the duration of the waiting loop (see Figure 7). The SystemC and the

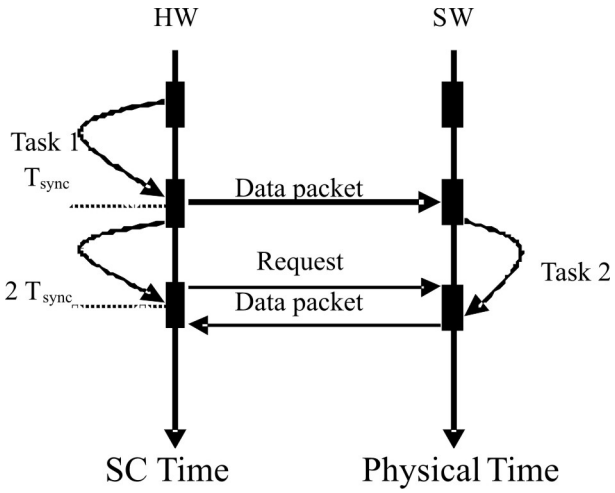


Figure 6: Synchronization model: scheme 1

emulator need to exchange the time stamp every context switch.

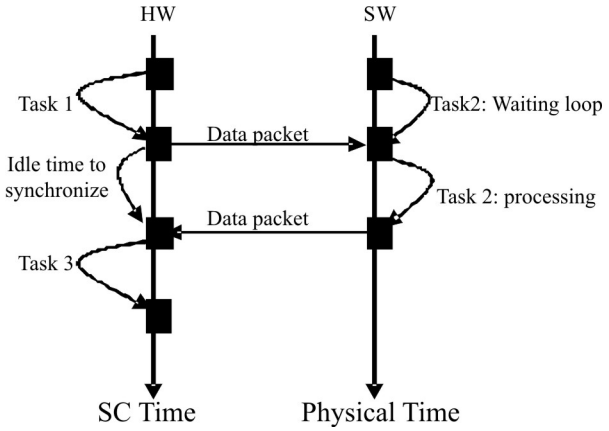


Figure 7: Synchronization model: scheme 2

- Scheme 3: The SW Task receives an interruption to indicate the end of the hardware Task

This scheme is illustrated by the Figure 8. In this case, the software does not use a waiting loop but the end of the Task is indicated by interruption, so the software can execute the Task instead of waiting. The Simulation scheduler (see Figure 14), running on the target processor, sends data to the simulation interfaces (arrow 0), which activates the hardware Task1. At the end of Task 1 process, and before sending data to SW Task, the *wait_for_interrupt(sc_time)* function is called (see Figure 9), so the simulator advances its time (arrow 1) and sends an interrupt packet to inform emulator for the next time stamp (arrow 2). At this time, the simulation scheduler activates a timer with a period that coincides with the received interruption time stamp and begins the execution of an intermediate Task (an eventual user background Task). When the timer is reached, it interrupts the background Task. Thus the simulation sched-

uler activates the Task 2 (the number of the interruption is received with the interrupt packet). The last one may request data, thus the Task 1 resumes execution and sends data packet (arrow 4), which activates Task 2. Figure 10 shows the template of the code.

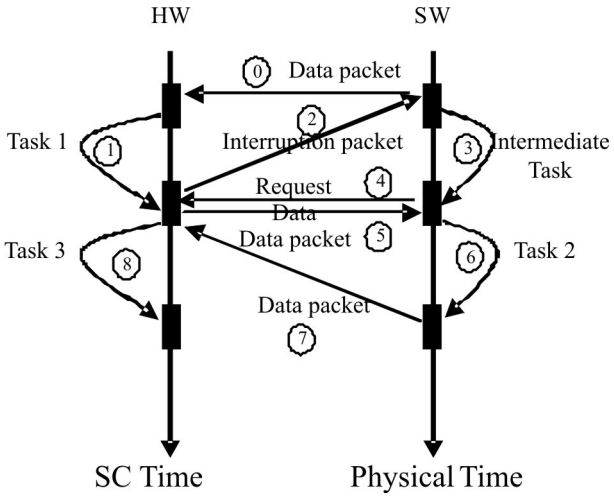


Figure 8: Synchronization model: scheme 3

```
void wait_for_interrupt(sc_time t)
{
wait(t);
send_interruption_packet(…..);
}
```

Figure 9: Wait_for_interrupt code

Where *t* is an estimation of the Task 1 duration

```
            /* Task1 code */
Instructions
….
….
Wait_for_interrupt (t);
Switch_context();/* context switch to SystemC */
```

Figure 10: Template of synchronization code

- Scheme 4: The SW Task may receive a random interruption resulting from externally data reception

This scheme is illustrated by the Figure 11. The SystemC begins the execution of the Task 1 and, when finished, sends a data packet to the SW Task. The Task 2 starts and the SystemC executes the *Hardware_Input_Interface* : a process that models the input interfaces of the hardware subsystem (its execution do not advances the SystemC local time). The process may generate a random interrupt packet which informs of the reception of a new data. The sent packet via USB generates an USB interruption which will interrupt the Task 2. Thus, the USB interruption plays the same role as the hardware interruption. Once the interruption is occurred, we need only to know, thanks to the received interrupt packet, the interruption routine to execute (here is Task 3).

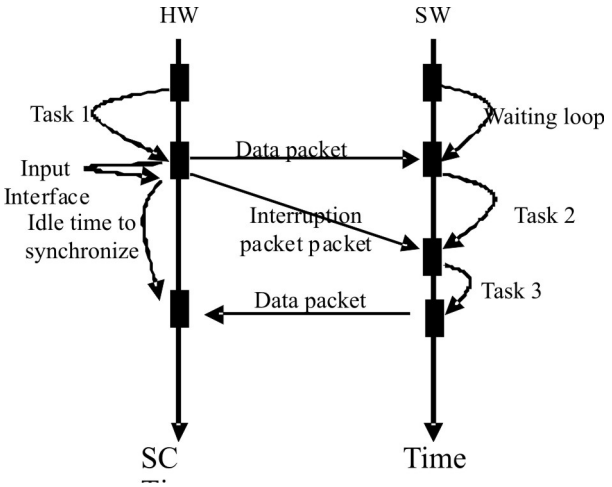


Figure 11: Synchronization model: scheme 4

To ensure communication and to save synchronization context, an array of shared registers is used. We fixed that the HW / SW partitioning is static. Also, the scheduler is at the same time static and based on data dependence. The last is used as a shared connection bus. Although this register based on bus modeling is not the same as the actual chip bus modeling, it is easy to set up. The register array is implemented on the FPGA board and can be accessed or Read / Write from the simulator using interruption services routines.

The S/E Engine ensures the verification of sequential and parallel applications. Two cases of sample are presented. The first is based on sequential Tasks and the second is based on parallel and sequential Tasks.

The Figure 12 describes the two samples based on data flow diagram and their synchronization model is shown in Figure 13.

Task 1, Task 3 and Task 5 are hardware components. Task 2 and Task 4 are software application.

For the sequential sample, the simulator begins the execution of the first Task. When Task 1 finished, the simulator sends an interrupt packet and data packet to the emulator to begin Task 2 and the simulator is blocked until he receives data packet from the emulator. At this moment, the simulator executes Task 3 and the emulator is blocked. When Task 3 finished, the simulator sends an interrupt packet to the emulator. The last runs Task 4 and returns data packet to Task 5 in the simulator.

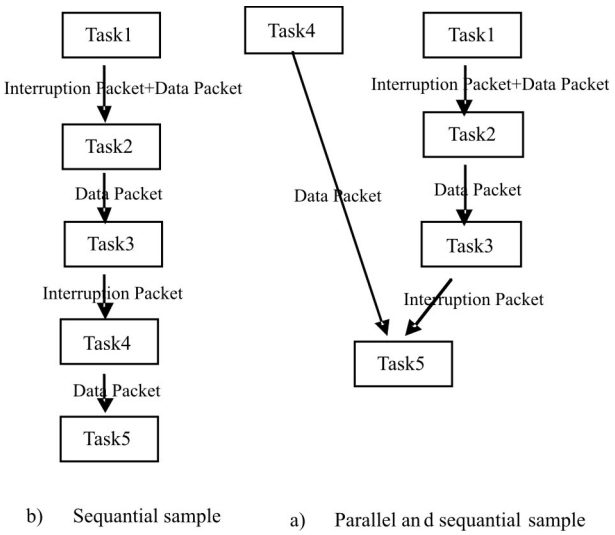


Figure 12: Data flow diagrams

For the parallel sample, the simulator begins Task1 and the emulator begins Task 4. When the simulator finished Task 1 he sends an interrupt packet to the emulator. The last stops the execution of the Task 4 and save the context then he receives the data packet and runs Task 2. The simulator is blocked. When Task 2 is finished, the emulator sends a data packet to the simulator and return to the execution of Task 4. At this moment, the simulator executes Task 3. When they finished, the simulator sends an interrupt packet. When the Task 4 is finished and the interrupt packet is sent, the emulator sends a data packet and the simulator runs Task 5.

4.2.2 Hardware/Software Synchronization interface

In this part, the hardware / software of the DUT is presented.

The SystemC is constructed using a modular approach to provide partitioning between the different functional elements of the overall controller. This facilitates the movement of functionality between different models, which proved useful during the control model design. It also simplifies the addition and/or removal of models from the system.

The hardware modules in SystemC are modeled in TLM layer and the adopted channel is FIFO. An Interface module is built to ensure the transaction between HW/SW. When a module wants to read or write data to the board, it makes connection with the TLM channel that implements a high level description of bus. The TLM channel assures the communication and the synchronization. Figure 14 describes the synchronization scheme for DUT.

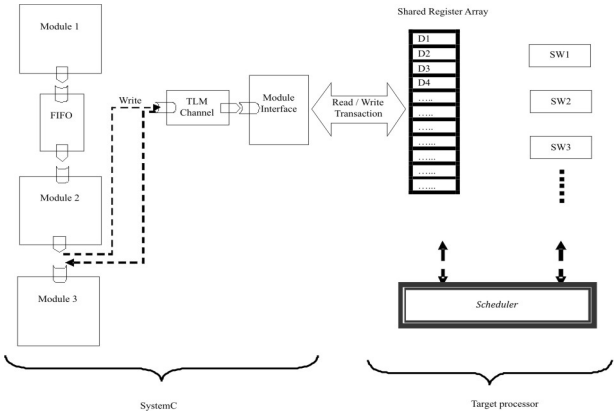


Figure 14: Synchronization interface for DUT

5 Experimental results

Three steps are essential for the Simulation/Emulation implementation and validation.

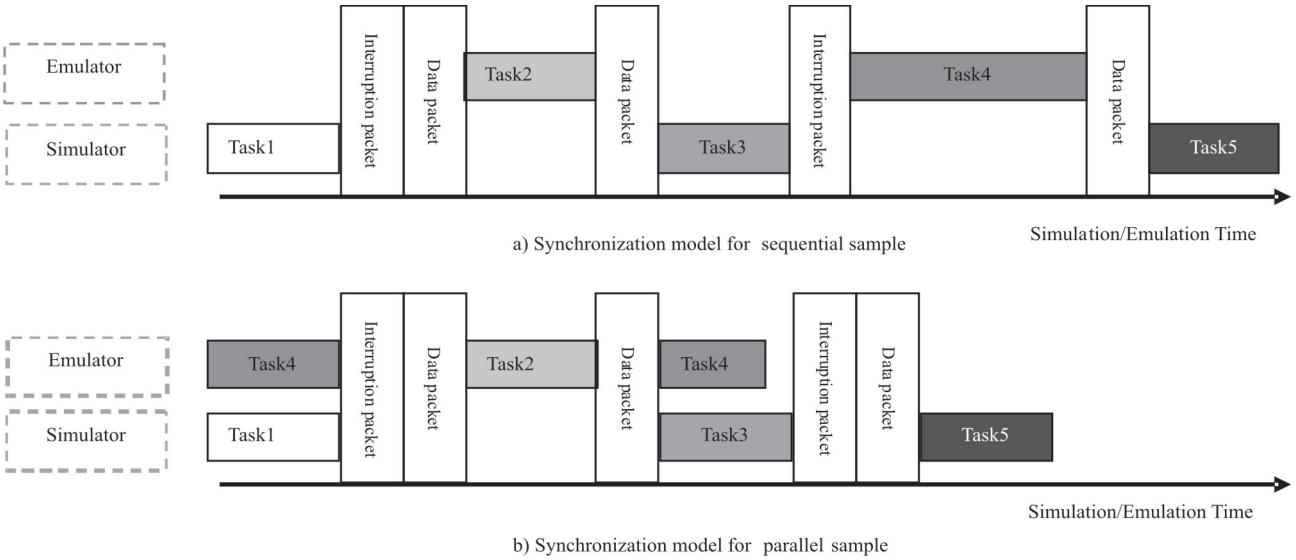


Figure 13: Synchronization model for each sample

Step 1: Target base architecture
The verification idea is based on combined tools to satisfy the HW/SW design. For the target base architecture an FPGA type ALTERA DE2-70 is used as a board and QuartusII, NIOSII IDE as tools. The first step is to set the architecture model. Figure 15 shows the architecture chosen. It contains the NIOSII processor [28], Avalon bus, memory and the ISP1362 USB controller [29].

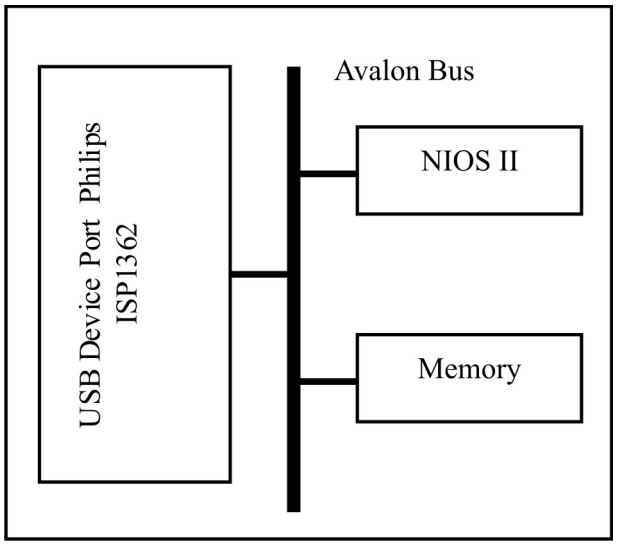


Figure 15: Target base architecture used

Step 2: Interfacing between HW/SW
This step concerns the addition of the *interface* module in SystemC. The last module is the responsible of the communication and the synchronization. When a context switch to the board is required, the *interface* module is called. The proposed interface can be added to any design described on SystemC without modify the kernel of SystemC like the work [30].

Step 3: Simulation results
In this section, two applications are proposed to validate the Simulation / Emulation environment.

*** Fingerprint recognition:**
Paper [16] presents a novel technique for fingerprint recognition based on DECOC classifier. Six steps are required for identification:
- Read the fingerprint: this phase reads the image of finger from sensor.
- Filter: A Gabor filter is used to ameliorate the contrast of ridge in the image.
- Binarization: This step converts the image from grayscale to binary system.
- Skeletonization: The neighborhood method is used.
- Minutia extraction: This step extracts the characteristics point in finger (Minutia) using the DECOC classifier.
- Matching: The final step makes correspondence between the input finger and the saved fingerprint.

Then, Based on the native execution of the fingerprint recognition on a 2 GB RAM, 1.66 GHz Intel Core 2 Duo processor with Windows XP operating system, we notice that the time execution of the minutia extraction is the minimum. We divided our system on hardware components and software applications with respect of the rule "the processes that has the more time expensive will be HW components".

The overall HW/SW configuration consists of the following entities:
– HW model of the read.
– HW model of the filter.
– HW model of the binarization.
– HW model of the matching.
– SW application of the skeletonization.
– SW application of the Minutia extraction.

Table 1 shows the simulation / emulation time of each process.

Table 1: simulation/emulation time of fingerprint

	Module	Time (s)
HW Components	Read of fingerprint	0.03
	Filter	
	Binarization	
	Matching	
Interface	Interface	0.5
SW Applications	Skeletonization	0.01
	Minutia extraction	
All Modules		0.54

To validate our simulation/emulation environment a comparison with simulation based on MIPS32 as ISS is made. Table 2 proves that the replacement of the ISS decrease by thirteen times less the time of simulation.

Table 2: Comparison Simulation Time

	Simulation (MIPS32)	Our environment
Simulation time (s)	18	0.54

*** 4 port router:**
A small 4-port router is described in SystemC, an extension of the Multicast Helix Packet Switch example distributed with SystemC 2.0.1.

This router receives data packets on its input ports and forwards them to the proper output port according to

a routing table embedded into the router. Whenever a new packet arrives on one of the input ports, it is stored into an internal buffer. If the buffer is full, the packet is dropped. Each packet is then read from the buffer by the main process of the router, and checked for errors by a checksum algorithm.

If the checksum is correct the destination address stored in the packet is used to find the right output port using the routing table; otherwise the packet is dropped. The packets consist of the following fields:
– Source address: the address of the producer.
– Destination address: the address of the consumer to which the packet must be sent.
– Packet identifier: an integer value used for debugging purposes only.
– Data field.
– Checksum: a 16 bit field used for error detection.

The overall HW/SW configuration consists of the following entities:
- HW model of the router.
- HW model of the packet generator (producer), which is attached to an input port of the router, and generates packets with a random destination address.
- HW model of the packet destination (consumer), which is attached to an output port of the router, and analyzes the integrity of the received packet.
- SW application computing the checksum, executing on NIOS II processor.

Table 3 shows the simulation / emulation time with 10 exchanged packets.

Table 3: Simulation/Emulation Time of 4-port router

	Module	Time (s)
HW Components	Router	0.03
	Packet generator	
	Packet destination	
Interface	Interface	0.12
SW Applications	Checksum	0.006
All Modules		0.156

To validate our simulation/emulation environment a comparison with simulation based on MIPS32 as ISS is made. Table 4 proves that the replacement of the ISS decrease by fifty times less the time of simulation.

Table 4: Comparison Simulation Time

	Simulation (MIPS32)	Our environment
Simulation time (s)	8	0.156

Discussion

These two samples highlight the performance of our environment with comparison with MIPS32 simulator. The simulation time is decreased by averaging 38 times.
The difference of the interface time between the fingerprint application and the 4-port router application is justified by the quantity of data transferred in each context switch. For the first sample, the interface consumes much time because the totality of the image must be transferred from/to the board.

6 Conclusion

The co-verification environment is based on synchronization between SystemC simulator and FPGA board emulator. The essential aim is to accelerate the simulation with the replacement of an ISS with target base architecture implemented in the board. The main features of the proposed synchronization schemes are the adaptation with CODIS tool. Experiments with real-life examples proved the effectiveness of the proposed system.

The resulting simulation/emulation time allows fast functional validation of HW devices before actually designing them and including onto a board, and, in particular, without changing the software executed on the board. The results shows that the simulation/emulation environment decreases the time simulation forty times less than the simulation environment based on ISS.

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References

1. OSCI; "Functional Specification for SystemC 2.0", available at www.systemc.org
2. T. Grotker, S Liao, G. Martin, S Swan, "System Design with SystemC", book published by Kluer Academic Publishers.
3. De Micheli, D., Ernst, R., and Wolf, W. Eds. Readings in Hardware/Software Co-design, Morgan Kaufmann, 2001.
4. Liem, C., Nacabal, F., Valderrama, C., Paulin, P., and Jerraya, A. 1997. System-on-chip cosimulation

and compilation. *IEEE Design and Test of Comput. 14,* 2, 16–25.
5. Valderrama, C.,Nacabal, F., Paulin, P., and Jerraya, A. 1998. Automatic VHDL-C interface generation for distributed cosimulation: Application to large design examples. *Design Autom. Embed. Syst. 3,* 2/3, 199–217.
6. Coste, P., Hessel, F., Marrec, P. l., Sugar, Z., Romdhani, M., Suescun, R., Zergainoh, N., and Jerraya, A. 1999. Multilanguage design of heterogeneous systems. In Proceedings of IEEE International Workshop on Hardware-Software Codesign. 54–58.
7. Liu, J., Lajolo, M., and Sangiovanni-Vincentelli, A. 1998. Software timing analysis using HW/SW cosimulation and instruction set simulator. In Proceedings of the IEEE International Workshop on Hardware/Software Co-design. 65–69.
8. Fummi, F., Martini, S., Perbellini, G., and Poncino, M. 2004. Native ISS-SystemC integration for the cosimulation of multi-processors SoC. In Proceedings of the IEEE Conference on Design Automation and Test in Europe. 564–569.
9. Moussa, I., Grellier, T., and Nguyen, G. 2003. Exploring SW performance using SoC transactionlevel modelling. In Proceedings of the IEEE Conference on Design Automation and Test in Europe. 120–125.
10. Bouchhima, A. Yoo, S. Jarraya A., "Fast and accurate timed execution of high level embedded software using HW/SW interface simulation model", Design Automation Conference: ASP-DAC, pp. 469 – 474, 2004.
11. Ziyi Jin, "A remote controlled embedded system implemented in FPGA", Master of Science Thesis in the Programme of Integrated Electronic System Design, Department of Computer Science and Engineering CHALMERS UNIVERSITY OF TECHNOLOGY UNIVERSITY OF GOTHENBURG Göteborg, Sweden ,2009.
12. N. Kim, H. Choi, S. Lee, S. Lee, I-C. Park, C-M. Kyung, „Virtual chip: making functional models work on real target systems", Proceedings of ACM/IEEE Design Automation Conference (DAC 98), pp.170-173, 1998.
13. Soha Hassoun*, Senior Member, IEEE*, Murali Kudlugi, Duaine Pryor, and Charles Selvidge "A Transaction-Based Unified Architecture for Simulation and Emulation" IEEE transactions on very large scale integration (vlsi) systems, vol. 13, no. 2, february 2005.
14. Jan Exalson, "USB COMPLETE Everything You Need to Develop Custom USB Peripherals" book, third edition, 2005.
15. ISP1362 Embedded Programming Guide Version 9 June 2002.
16. Mossaad Ben Ayed, Faouzi Bouchhima and Mohamed Abid, "Automated Fingerprint Recognition Using the DECOC Classifier", International Journal of Computer Information Systems and Industrial Management Applications. Volume 4 (2012) pp. 546-553
17. S. Cordibella, F. Fummi, G. Perbellini, D. Quaglia, "A HW/SW Co-Simulation Framework for the Verification of Multi-CPU systems", IEEE transactions, 2008
18. F. Bouchhima, M. Brière, G. Nicolescu, M. Abid, E. M. Aboulhamid, "A SystemC/Simulink Co-Simulation Framework for Continuous/Discrete-Events Simulation", Behavioral Modeling and Simulation Workshop, Proceedings of the 2006 IEEE International.
19. Primož Puhar, Andrej Žemva, "Hybrid functional verification of a USB host controller", Informacije MIDEM – Journal of Microelectronics, Electronic components and materials, Vol. 38, Iss. 2 (2008), p94-102.
20. Xunying Zhang, Fei Hui, Qiang Wang, Xubang Shen, "Integrated ISS and FPGA SoC HW/SW Coverification Environment Design", 12th International Conference on Computer Supported Cooperative Work in Design , 2008, p 1071-1075.
21. Mehrdad Reshadi, Nikil Dutt, "Hybrid-Compiled Simulation: An Efficient Technique for Instruction-Set Architecture Simulation", ACM Transactions on Embedded Computing Systems, Vol. 8, No. 3, Article 20, April 2009.
22. Wei Qin, Joseph D'Errico, Xinping Zhu, "A Multiprocessing Approach to Accelerate Retargetable and Portable Dynamic-compiled Instruction-set Simulation", The International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS'06, 2006.
23. Carsten Gremzow, « Compiled Low-Level Virtual Instruction Set Simulation and Profiling for Code Partitioning and ASIP-Synthesis in Hardware/ Software Co-Design", Proceedings of the 2007 Summer Computer Simulation Conference, SCSC 2007.
24. Hoeseok Yang, Youngmin Yi, Soonhoi Ha, "A Timed HW/SW Coemulation Technique for Fast Yet Accurate System Verification", Proceedings of the 9th international conference on Systems, architectures, modeling and simulation,2009, Pages 74-81.
25. Y.B. Liao, P. Li, A.W. Ruan, Y.W. Wang, W.C. Li, W. Li, "Hierarchy Communication Channel in Transaction-Level Hardware/Software Co-Emulation System", Ninth International Workshop on Microprocessor Test and Verification, 2008.
26. Franco Fummi, Giovanni Perbellini, Mirko Loghi, Massimo Poncino, « ISS-Centric Modular HW/SW

Co-Simulation », Proceedings of the 2006 ACM Great Lakes Symposium on VLSI GLSVLSI'06, April 30–May 2, 2006.
27. Luca Formaggio, Franco Fummi, Graziano Pravadelli, « A TimingAccurate HW/SW Cosimulation of an ISS with SystemC", The International Conference on Hardware/Software Codesign and System Synthesis CODES+ISSS'04, September 8–10, 2004.
28. NIOS II Processor Reference. (2013) [Online]. Available: http://www.altera.com
29. ISP1362 Single-chip Universal Serial Bus On-The-Go controller. (2013) [Online]. Available: http://www.cs.columbia.edu
30. Franco Fummi, Mirko Loghi, Stefano Martini, Marco Monguzzi, Giovanni Perbellini, Massimo Poncino, «Virtual Hardware Prototyping through Timed Hardware-Software Co-simulation », Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (DATE'05), 2005.
31. J. Tratnik, P. Lemut, M. Vidmar, "Time-transfer and synchronization equipment for high-performance particle accelerators", Informacije MIDEM – Journal of Microelectronics, Electronic Components and Materials, Vol 42, No 2 (2012), p115-122.

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Low-Voltage FGMOS Based Voltage-to-Current Converter

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Abstract: This paper proposes a novel floating-gate MOSFET (FGMOS) based voltage-to-current (VTC) converter. The proposed VTC converter has rail-to-rail input dynamic range, low THD (total harmonic distortion) and low power dissipation. The VTC converter has been simulated using SPICE in 0.25-μm CMOS technology with the supply voltages of ±0.75V. The simulation results of the VTC converter demonstrate THD of less than 1%, 3-dB frequency of 1.63GHz and maximum power dissipation of 0.84mW.

Keywords: Floating gate MOSFETs, low-voltage, mobility degradation, SPICE, VTC converter.

Nizkonapetostni napetostno-tokovni pretvornik na osnovi FGMOS

Izvleček: Članek predlaga nov napetostno-tokovni pretvornik (VTC) na osnovi MOSFET (FGMOS) s plavajočimi vrati. Predlagan VTC pretvornik ima polni vhodni napetostni obseg, nizko THD (dinamično harmonično distorzijo) in nizko disipacijo moči. VTC pretvornik je bil simuliran s SPICE v 0.25-μm CMOS tehnologiji z napajalno napetostjo ±0.75V. Simulacije VTC pretvornika izkazujejo THD manjši od 1 %, 3 dB pri 1.63 GHz in največjo disipacijo moči 0.84 mW.

Ključne besede: MOSFET s plavajočimi vrati, nizka napetost, degradacija mobilnosti, SPICE, VTC pretvornik

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1 Introduction

Low-voltage operation has become a major design issue for the analog signal processing applications. This is because a low-voltage power supply reduces the power dissipation which increases the battery lifetime and the reliability of the portable systems. Some of the low-voltage techniques used to reduce supply voltages are level shifters, self-cascode MOSFETs, sub-threshold MOSFETs, bulk-driven MOSFETs and floating-gate MOSFETs (FGMOS) [1-2]. Out of these, FGMOS presents a unique advantage of programmability of the threshold voltage. The other advantage of FGMOS is its compatibility with standard double-poly CMOS process technology. The FGMOS transistors have found many applications in electronic programming [3], digital-to-analog (D/A) and analog-to-digital converters [4], neural networks [5], voltage-controlled resistors [6]-[9], operational transconductance amplifier [10], multipliers [11], squarers [11]-[12], etc.

The voltage-to-current (VTC) converter is extensively used in the design of mixers/ modulators, voltage-to-frequency converters and interface units between circuits employing voltage-mode signal processing and those using current-mode processing. In addition, VTC converters are used as basic building blocks to perform various computational functions, such as square-rooting, squaring, multiplying, sum of squares and difference of squares, etc. [13]-[14]. The linearity and bandwidth are the usually concerned specifications of VTC converter which dominate whether its performance is adequate. The nonlinear effects of VTC mainly including nonlinear second-order V-I characteristic, body effect, mobility degradation, temperature variation and so on [15-19]. Recently, many researchers have been developed a fixed gain V-I converter input stage with programmable gain current mirrors [20]-[23]. However, these structures increase

complexity and power dissipation. In this paper, we have proposed a wide band linear VTC converter with mobility degradation and channel length modulation compensation.

The paper is organized as follows. The operation of the FGMOS is described in section 2. In section 3, the FGMOS based VTC converter is proposed. The detailed analysis of second-order effects on the performance of the proposed VTC converter is discussed in section 4. In section 5, SPICE simulation results are presented to verify the theoretical analysis and to demonstrate the effectiveness of the proposed circuit. The paper is concluded in section 6.

2 Operation of FGMOS

The basic structure of n-type, N-input FGMOS is shown in Figure 1. The first poly-silicon layer over the channel forms the floating gate and the second poly-silicon layer forms N-input gates that are located over the floating gate. The symbol and equivalent circuit model for an N-input FGMOS are shown in Figures. 2 (a) and (b), respectively. In both the figures, V_i (for i = 1, 2,…, N) are the control input voltages and D, S and B are the drain, source and substrate, respectively.

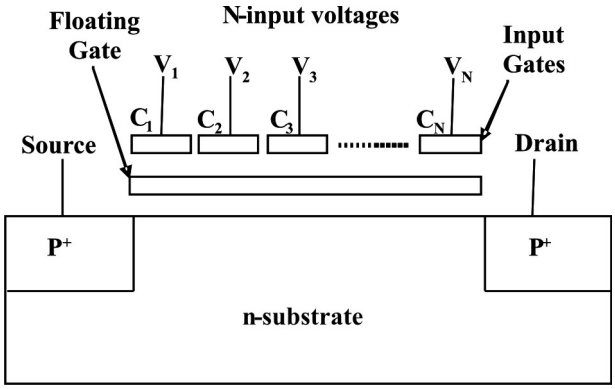

Figure 1: N-input FGMOS

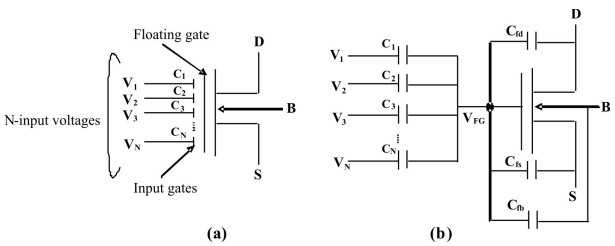

Figure 2: FGMOS (a) Symbol (b) Equivalent circuit

The N-input control gates are capacitively coupled to the floating gate. Hence, the voltage on the floating gate (V_{FG}) can be determined using the charge conservation law as [24]:

$$\sum_{i=1}^{N} C_i (V_i - V_{FG}) + C_{fd} (V_{DS} - V_{FG}) + C_{fs} (V_{SS} - V_{FG}) + C_{fb} (V_{BS} - V_{FG}) + Q_{FG} = 0 \quad (1)$$

Where C_1, C_2, C_3, …, C_N are the input capacitances between control gates and floating gate, $\sum_{i=1}^{N} C_i$ is the sum of N-input capacitances, C_{fd} is the parasitic capacitance between floating-gate and drain, C_{fs} is the parasitic capacitance between floating-gate and source, C_{fb} is the capacitance between floating gate and substrate, V_i is the input voltage of i^{th} input gate, V_{DS} is the drain-to-source voltage, V_{SS} is the source voltage, V_{BS} is the substrate-to-source voltage (usually, the value of V_{BS} is chosen as zero volt to avoid body effect), and Q_{FG} is the residual charge.

The residual charge Q_{FG} is trapped in the oxide-silicon interface during the fabrication process. The trapped residual charge gives rise to large variations in the threshold voltage of the FGMOS. The removal of the trapped charge in the FGMOS is possible by using the method suggested in [25-26], in which the first poly-silicon layer is connected to the metal-k (where k represents the top most metal layer, which is deposited and etched last) layer. By this contact, the floating gate is not connected to any other part of the circuit, so it will not affect the operation of the FGMOS. Therefore, Eq. (1) reduces to

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{fd} V_{DS} + C_{fs} V_{SS}}{C_T} \quad (2)$$

where C_T is the total capacitance and is given as

$$C_T = \sum_{i=1}^{N} C_i + C_{fd} + C_{fs} + C_{fb} \quad (3)$$

If $\sum_{i=1}^{N} C_i >> C_{fd}, C_{fs}$, Eqs. (2) and (3) are modified as:

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i}{C_T} \quad (4)$$

$$C_T = \sum_{i=1}^{N} C_i \quad (5)$$

The current equation of N-input FGMOS has been obtained by modifying the current equation of conventional MOSFET. The current I_p in the saturation region is expressed as follows:

$$I_p = \frac{K_p}{2} \left\{ V_{DD} - \left(\frac{\sum_{i=1}^{N} C_i V_i}{C_T} \right) - |V_{Tp}| \right\}^2 \quad (6)$$

where $K_p = \mu_p C_{ox}$ (W/L) is the transconductance parameter, μ_p is the mobility of holes, C_{ox} is the gate-oxide capacitance per unit area, (W/L) is the aspect ratio and V_{Tp} is the threshold voltage.

3 FGMOS based voltage-to-current converter

The proposed FGMOS based voltage-to-current (VTC) converter is shown in Figure 3. In this figure, the FGMOS transistors M_1, M_2, M_3 and M_4 are used to develop voltage-to-current conversion whereas the conventional MOS transistors M_5, M_6, M_7 and M_8 are used to provide proper biasing condition. All these transistors are biased in the saturation region. The transistors M_1, M_2, M_3 and M_4 are perfectly matched i.e. $K_{pi} = K_p$, $V_{Tpi} = V_{Tp}$ and $k_{i1} = k_{i2} = k_1$, where i = 1,2,3,4. The applied bias & input gate voltages of transistors M_1, M_2, M_3 and M_4 are V_b &V_{IN1}, V_b &-V_{IN2}, V_b &-V_{IN1} and V_b &V_{IN2}, respectively.

The transistors M_5 and M_6 form the current mirror and transistors M_7 and M_8 set the bias current. From Figure 3, it is evident that there is no body effect in the proposed circuit. The output current I_o is given as

$$I_o = I_1 - I_2 = \left(I_{p1} + I_{p2}\right) - \left(I_{p3} + I_{p4}\right) \quad (7)$$

Where I_{p1}, I_{p2}, I_{p3}, and I_{p4}, are the currents of transistors M_1, M_2, M_3 and M_4, respectively.

Using Eq. (6), the currents I_{p1}, I_{p2}, I_{p3}, and I_{p4} are given as

$$I_{p1} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN1}\right) - \left|V_{Tp}\right|\right)^2 \quad (8)$$

$$I_{p2} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN2}\right) - \left|V_{Tp}\right|\right)^2 \quad (9)$$

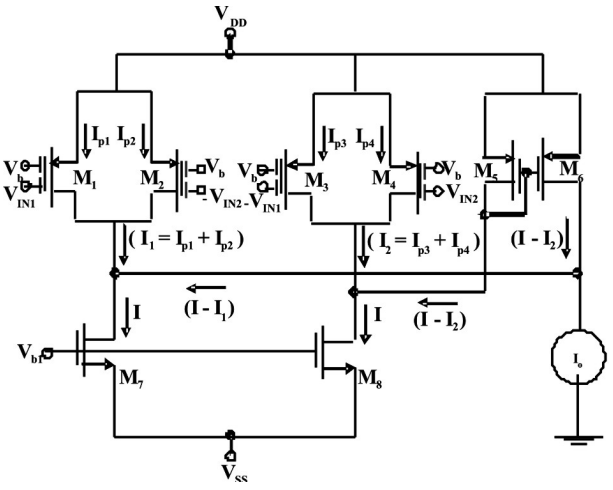

Figure 3: Proposed FGMOS based VTC converter

$$I_{p3} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN1}\right) - \left|V_{Tp}\right|\right)^2 \quad (10)$$

$$I_{p4} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN2}\right) - \left|V_{Tp}\right|\right)^2 \quad (11)$$

Where $k_1 = C_1/C_T$ is capacitive coupling ratio, V_{IN1} & V_{IN2} are input voltages, V_b is the bias voltage and V_{DD} is the supply voltage.

Substituting Eqs. (8) - (11) in Eq. (7), the output current I_o is given as

$$I_o = A\left(V_{IN2} - V_{IN1}\right) \quad (12)$$

where $A = 2K_p\ k_1\left(V_{DD} - k_1 V_b - \left|V_{Tp}\right|\right)$.

Equation (12) gives the linear relationship between the output current (I_o) and the differential input voltage (V_{IN2} - V_{IN1}). Hence, Figure 3 behaves as VTC converter.

4 Second order effects

In this section, the effects of channel length modulation and mobility degradation on the proposed VTC converter are discussed.

4.1 Channel Length Modulation Effect

The current I_p of 2-input FGMOS including channel length modulation effect is given as

$$I_p = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - \left|V_{Tp}\right|\right)^2\left(1 + \lambda V_{DS}\right) \quad (13)$$

where λ is the channel length modulation parameter.

Considering this effect, Eqs. (8)- (11) are modified as

$$I_{p1} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN1}\right) - \left|V_{Tp}\right|\right)^2\left(1 + \lambda V_{DS1}\right) \quad (14)$$

$$I_{p2} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN2}\right) - \left|V_{Tp}\right|\right)^2\left(1 + \lambda V_{DS2}\right) \quad (15)$$

$$I_{p3} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN1}\right) - \left|V_{Tp}\right|\right)^2\left(1 + \lambda V_{DS3}\right) \quad (16)$$

$$I_{p4} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN2}\right) - \left|V_{Tp}\right|\right)^2\left(1 + \lambda V_{DS4}\right) \quad (17)$$

From Figure 3, it can be seen that $V_{DS1} = V_{DS2}$ and $V_{DS3} = V_{DS4}$. Substituting the values of I_{p1}, I_{p2}, I_{p3}, and I_{p4}, from Eqs. (14)-(17) and $V_{DS1} = V_{DS2}$ & $V_{DS3} = V_{DS4}$ in Eq. (7), the output current I_o is given as

$$I_o = A\left(V_{IN2} - V_{IN1}\right) + B + C + D \quad (18)$$

where $A = 2K_p\ k_1\left(V_{DD} - k_1V_b - |V_{Tp}|\right)$;

$B = \lambda K_p\left(V_{DD} - k_1V_b - |V_{Tp}|\right)^2 (V_{DS1} - V_{DS3})$;

$C = \frac{\lambda}{2}k_1^2K_p\left(V_{IN1}^2 + V_{IN2}^2\right)(V_{DS1} - V_{DS3})$ and

$D = \lambda k_1 K_p\left(V_{DD} - k_1V_b - |V_{Tp}|\right)(V_{DS1} + V_{DS3})(V_{IN2} - V_{IN1})$.

For smaller values of (V_{DS1} - V_{DS3}) and (V_{IN2} - V_{IN1}), the effect of channel length modulation in Eq. (18) can be neglected.

4.2 Mobility Degradation Effect

The current I_p of 2-input FGMOS including mobility degradation effect is given as

$$I_p = \frac{K_p}{2}\left[\frac{\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - |V_{Tp}|\right)^2}{1 + \theta\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - |V_{Tp}|\right)}\right] \quad (19)$$

In Eq. (19), $\theta\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - |V_{Tp}|\right) << 1$, where Θ is the mobility degradation parameter. Using Binomial theorem expansion and neglecting the higher order terms, Eq. (19) is approximated as

$$I_p = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - |V_{Tp}|\right)^2 \cdot \left(1 - \theta\left(V_{DD} - k_1\left(V_b + V_{IN}\right) - |V_{Tp}|\right)\right) \quad (20)$$

Including this effect, Eqs. (8)- (11) are modified as

$$I_{p1} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN1}\right) - |V_{Tp}|\right)^2 \left(1 - \theta\left(V_{DD} - k_1\left(V_b + V_{IN1}\right) - |V_{Tp}|\right)\right) \quad (21)$$

$$I_{p2} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN2}\right) - |V_{Tp}|\right)^2 \left(1 - \theta\left(V_{DD} - k_1\left(V_b - V_{IN2}\right) - |V_{Tp}|\right)\right) \quad (22)$$

$$I_{p3} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b - V_{IN1}\right) - |V_{Tp}|\right)^2 \left(1 - \theta\left(V_{DD} - k_1\left(V_b - V_{IN1}\right) - |V_{Tp}|\right)\right) \quad (23)$$

$$I_{p4} = \frac{K_p}{2}\left(V_{DD} - k_1\left(V_b + V_{IN2}\right) - |V_{Tp}|\right)^2 \left(1 - \theta\left(V_{DD} - k_1\left(V_b + V_{IN2}\right) - |V_{Tp}|\right)\right) \quad (24)$$

Using Eqs. (21)-(24) in Eq. (7), the output current I_o is given as

$$I_o = 2K_p\ k_1\left(V_{DD} - k_1V_b - |V_{Tp}|\right)(V_{IN2} - V_{IN1}) - 3\theta k_1K_p\left(V_{DD} - k_1V_b - |V_{Tp}|\right)^2(V_{IN2} - V_{IN1}) - \theta K_p k_1^3\left(V_{IN2}^3 - V_{IN1}^3\right) \quad (25)$$

or

$$I_o = A\left(V_{IN2} - V_{IN1}\right)\left(1 - \frac{3\theta}{2}\left(V_{DD} - k_1V_b - |V_{Tp}|\right) - \frac{\theta}{2}k_1^2\frac{\left(V_{IN2}^2 + V_{IN1}^2 + V_{IN2}V_{IN1}\right)}{\left(V_{DD} - k_1V_b - |V_{Tp}|\right)}\right) \quad (26)$$

From equation (26), it can be seen that the second and third terms are very smaller than the unity, causes only the gain error. Since output current (I_o) is varied with the differential input voltage ($V_{IN2} - V_{IN1}$), mobility degradation effect can be neglected.

5 Results and Discussion

The proposed VTC converter has been simulated using SPICE in $0.25\mu m$ CMOS technology. The VTC converter operates with the supply voltages of $\pm 0.75V$. The various parameters of the designed VTC converter are listed in Table 1.

Table 1: Various circuit parameters

Circuit parameters	Values
CMOS Technology	0.25µm
Vb	0.75V
VTp	-0.55
λ	9.6X10-3
θ	0.05

Figure 4 shows the I-V characteristic of VTC converter and plots the output current I_o versus differential input voltage V_{IN2} - V_{IN1}. In this figure, blue and red lines denote the current/voltage characteristic for V_{IN2} while V_{IN1} = 0 and for V_{IN1} while V_{IN2} = 0 respectively. Figure 5 shows the THD obtained in the output waveform as a function of the peak-to-peak differential input voltage. From this figure, it is observed that for differential input voltage swings as large as 1.5V, distortion is still low (< 0.9%).

The total power dissipation of this circuit is .84mW. Figure 6 shows the frequency response of VTC converter and it is observed that the response remains constant till 1.63GHz.

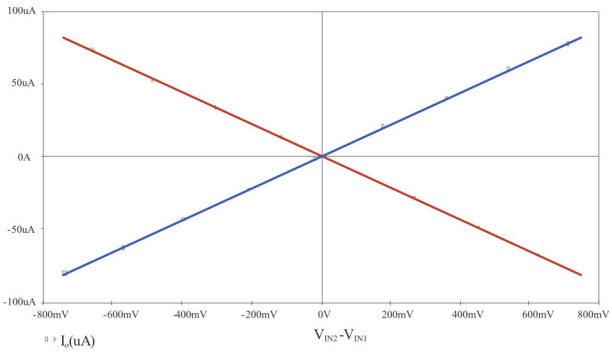

Figure 4: I-V characteristic of the proposed VTC converter

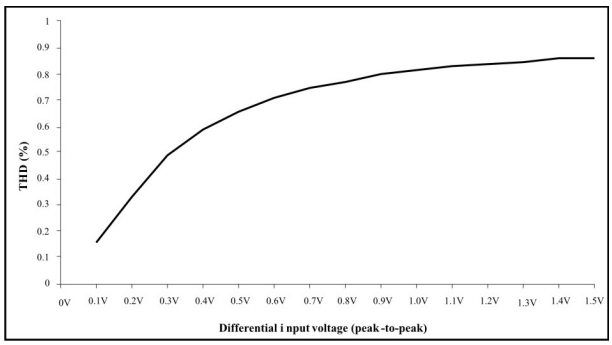

Figure 5: THD vs. differential input voltage amplitude

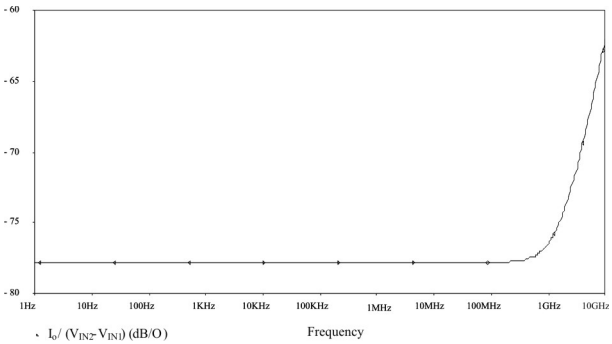

Figure 6: Transconductance ($I_o/(V_{IN2}-V_{IN1})$) curve for Figure 3

Table 2 compares the proposed FGMOS based voltage-to-current converter and the voltage-to-current converter reported by Srinivasan et al. in [27]. It is observed that FGMOS based voltage-to-current converter proposed in this manuscript has lower supply voltage requirement, lower power dissipation and wider input voltage range as compared to the existing circuit.

Table 2: Comparison of FGMOS based voltage-to-current converter with the voltage-to-current converter reported in [27]

Circuit parameters	Voltage-to-current converter [27]	Proposed FGMOS based voltage-to-current converter
Supply voltage	Not available	± 0.75V
CMOS technology	0.25 µm	0.25 µm
Input voltage range	± 500 mV	± 750 mV
Power dissipation	Not available	840 µW
-3dB frequency	200 MHz	1.63 GHz
THD	Not available	Less than 0.9%

Conclusion

In this paper, a new low-voltage FGMOS based VTC converter operates with the supply voltages of ± 0.75V has been presented. The inherent advantages of this circuit are wide input range, low power dissipation, low THD and wide frequency range which make it suitable for low-voltage signal processing applications. The analysis of the channel length modulation and mobility degradation effects show that they have little influence on the proposed circuit.

References

1. Sanchez-Sinencio, E., Andreou, A.G. Low Voltage/ Low Power Integrated Circuits and Systems. IEEE Press, New York, 1999.
2. Yan, S., Sanchez-Sinencio, E. Low Voltage Analog Circuit Design Techniques: A Tutorial. IEICE Trans. Analog Integrated Circuits and Systems, 2000, Vol. E00–A, no. 2, p. 1-17.
3. Berg, Y., Lande, T. S. Programmable floating gate MOS logic for low-power operation. In Proceedings of IEEE Int. Symp. Circuits Systems-ISCAS-97, Hong Kong, 1997, p. 1792-1795.
4. Liming, Y., Embadi, S.H.K., Sanchez-Sinencio, E. A floating gate MOSFET D/A converter. In Proceedings of IEEE Int. Symp. Circuits Systems, Hong Kong, 1997, p. 409-412.
5. Lee, B. W., Sheu, B. J., Yang, H. Analog floating gate-synapses for general purpose VLSI neural computation. IEEE Trans. Circuits Syst., 1991, vol. 38, p. 654-657.
6. Gupta, M., Pandey, R. Fgmos Based Low-Voltage Tunable Floating Resistor. Journal of Active and Passive Electronic Devices, 2011, vol. 6, no. 1-2, p. 119-128.
7. Gupta, M., Pandey, R. Fgmos Based Voltage-Controlled Resistor and Its Applications. Microelectronics Journal, 2010, vol. 41, no. 1, p. 25-32.
8. Pandey, R., Gupta, M. Fgmos based tunable grounded resistor. Analog Integrated Circuits and Signal Processing, 2010, vol. 65, no. 3, p. 437-443.
9. Pandey, R., Gupta, M. Fgmos Based Voltage-Controlled Grounded Resistor. Radioengineering journal, 2010, vol. 19, no. 3, p. 455-459.
10. Ramirez-Angulo, J., Choi, S.C., Altamirano, G.G. Low voltage circuits building blocks using multiple input floating gate transistors. IEEE Trans. Circuits Syst. –I, 1995, 42, no. 11, p. 971-974.
11. Vlassis, S., Siskos, S. Design of voltage-mode and current-mode computational circuits. IEEE

Transactions on Circuits and Systems-I, 2004, vol. 51, no. 2, p. 329–341.
12. Pandey, R., Gupta, M. Low Voltage Squarer Using Floating Gate MOSFETs. International Journal of Electronics, Circuits and Systems, 2009, vol. 3, no. 1, p. 53-56.
13. Hung, C. C., Ismail, M., Halonen, K., Porra, V. A low-voltage rail-to-rail CMOS V-I converter. IEEE Transactions on Circuits and Systems-II, 1999, vol. 46, no.6, p.816-820.
14. Chen, R. Y., Hung, T. S. A Linear CMOS Voltage-to-Current Converter. International Symposium on Signals, Circuits and Systems, 2005, Vol. 2, p. 677-680.
15. Wen, Y.C., Lee, K.J. A current-mode BIST structure of DACs. Journal of the International Measurement Confederation, 2002, vol. 31, no. 3, p. 147-163.
16. Mansuri, M., Ken Yang, C.K. A low-power adaptive bandwidth PLL and clock buffer with supply-noise compensation. IEEE J. of Solid -State Circ., 2003, vol. 38, no. 11, p. 1804-1812.
17. Fayed, A.A., Ismail, M. A low-voltage, highly linear voltage-controlled trans-conductor. IEEE Trans. on Circ. and Syst.-II, 2005, vol. 52, no. 12, p. 831-835.
18. Han, I.S. A novel tunable transconductance amplifier based on voltage-controlled resistance by MOS transistors. IEEE Trans. on Circ. And Syst.-II, 2006, vol. 53, no. 8, p. 662-666.
19. Lin, C. Wei, Lin, S. F., Wang, C. F. Wide Band Linear Voltage-to-Current Converter Design. IEEE International Symposium on Electronic Design, Test & Applications, 2010, p.115-120.
20. Lopez-Martin, A. J., Ramirez-Angulo, J., Durbha, C., Carvajal, R. G. A Cmos Transconductor with multidecade tuning using balanced current scaling in moderate inversion. IEEE J. Solid- State Circuits, 2005, vol. 40, no. 5, p. 1078-1083.
21. Ramirez-Angulo, J., Grau, I. Wide gm adjustment range, highly linear OTA with linear programmable current mirrors. IEEE International Symposium on Circuits and Systems, 1992, p. 1372-1375.
22. Adams, W. J., Ramirez-Angulo, J. Ota Extended gm Adjustment Range via Electronically Programmable Current Mirrors. IEEE International Symposium on Circuits and Systems, 1991, p. 2553-2556.
23. Klumperink, E. A. M., Seevinck, E. Mos current gain cells with electronically variable gain and constant bandwidth. IEEE J. Solid-State Circuits, 1989, vol. 24, no. 5, p. 1465-1467.
24. Inoue, T., Nakane, H., Fukuju, Y., Sinencio, E.S. A Design of a Low-voltage Current-Mode Fully-Differential Analog CMOS Integrator Using FG-MOSFETs and Its Implementation. Analog Integrated Circuits and Signal Processing, 2002, vol. 32, p. 249–256.
25. Rodriguez-Villegas, E., Barnes, H. Solution to trapped charge in FGMOS transistors. Electronics Letters, 2003, Vol. 39, no. 19, p.1416 – 1417.
26. Rodriguez-Villegas, E., Jimenez, M., Carvajal, R. G. On Dealing with the Charge Trapped in Floating-Gate MOS (FGMOS) Transistors. IEEE Transactions on Circuits and Systems-II: Express Briefs, 2007, Vol. 54, no. 2, p. 156-160.
27. Srinivasan, V., Chawla, R. Hasler P. Linear Current-to-Voltage and Voltage-to-Current Converters. 48th Midwest Symposium on Circuits and Systems, vol. 1, 2005, p. 675-678.

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A Low-Complexity and Energy-Efficient IR-UWB Pulse Generator in 0.18μm technology

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Abstract: A low-power and low-complexity impulse radio ultra-wideband (IR-UWB) pulse generator is presented in the paper. The tunable architecture is composed of a data and clock synchronization block, a controlled glitch generator, an adjustable two-stage buffer, and a pulse shaping filter. The generator has ability of the power spectral density (PSD) peak and central frequency adjustment. This is accomplished by varying the duration of the very short pulse produced by the glitch generator and changing the slope of the signal edges when passing through the buffer. This allows control in the output signal duration and amplitude (proportional to the slope of the signal at the pulse shaping filter input) determining the PSD value and -10 dB bandwidth. The pulse generator is designed and simulated in low-cost 0.18 μm UMC CMOS technology. The simulation results show 403 mV peak-to-peak amplitude and the pulse width of 0.6 ns. The PSD occupies bandwidth from 3 GHz to 7.8 GHz and fully complies with the corresponding FCC spectral mask. The IR-UWB generator supports OOK modulation with an area of 0.63 mm2. It has low power consumption of 1.3 mW corresponding to energy consumption of 13 pJ per pulse for 100 MHz pulse repetition frequency (PRF).

Keywords: analog RF design, CMOS integrated circuits, impulse radio ultra wideband (IR-UWB), pulse generator, transmitter.

Enostaven in energijsko učinkovit IR-UWB pulzni generator v 0.18μm tehnologiji

Izvleček: Članek predstavlja enostaven impulzni radio ultra širokopasoven pulzni generator (IR-UWB) nizkih moči. Spremenljiva arhitektura je sestavljena iz podatkovnega in časovnega sinhronizacijskega bloka, kontroliranega izvora kratkih pulzov, nastavljivega dvostopenjskega ločilnega ojačevalnika in pulzno oblikovnega filtra. Generator ima možnost spreminjanja spektralne gostote vršne in centralne frekvence. To je izvedeno s spreminjanjem trajanja zelo ozkega pulza generatorja in spreminjanja naklona robov signala pri prehajanju skozi ločilni ojačevalnik, kar omogoča kontroliranje trajanja in amplitude izhodnega signala (sorazmerno s strmino signala pri vhodu filtra oblikovanja pulza) z določitvijo PSD vrednosti in -10 dB pasovne širine. Pulzni generator je načrtovan in simuliran v ceneni 0.18 μm UMC CMOS tehnologiji. Rezultat simulacije je pulz z 403 mW amplitudo vrh-vrh in širino 0.6 ns. PSD zaseda pasovno širino od 3 do 7.8 GHz in polno ustreza pripadajoči FCC spektralni maski. IR-UWB generator podpira OOK modulacijo s površino 0.63 mm2. Ima nizko porabo moči 1.3 mW s pripadajočo porabo energija 13 pJ na pulz pri 100 MHz frekvenci ponavljanja (PRF).

Ključne besede: analogni RF dizajn, CMOS integrirano vezje, impulzni radio ultra širokopasovni (IR-UWB), pulzni generator, oddajnik.

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1 Introduction

Ultra-wideband (UWB), with allocated frequency range from 3.1 GHz to 10.6 GHz, is one of the most promising technologies for wireless communication applications [1] – [3]. There are several approaches within the UWB developed to satisfy very strict market requirements (multiband orthogonal frequency division multiplexing – MB-OFDM [4], direct-sequence – DS [5], the impulse radio ultra wideband – IR-UWB [6]). Besides of high data and wide bandwidth, low power consumption, or in other words high power efficiency becomes increasingly critical in wireless communications because of the popularity of battery-powered wireless devices. The IR-UWB technique has precedence in applications demanding energy efficient, low-cost and modest (without noisy and power-hungry blocks such as mixers and power amplifiers) UWB transmitter realizations allowing simple modulation scheme (e.g. on-off keying – OOK) [6]. These advantages are provided

by not so complicated type of transmission since the technology, as carrier-free approach, uses extremely short pulses (duration less than 1 ns) yielding a few GHz spectrum bandwidth. In addition, the protocol offers a great resistance to multipath fading that usually plagues for narrow-band systems, high time and range resolution (with a potential for centimeter accuracy in indoor environments), multiple access and robustness to interference, and low probability of undesired detection and interception [6]. The IR-UWB transceivers are highly used in very high data rate short-range communication, low data rate communication related to localization or/and positioning systems [6], biomedical applications such as wireless personal area networks [7], inter-chip communications [8], [9], and UWB biotelemetry [10], [11].

A pulse generator is one of the most essential parts of an IR-UWB transceiver as its signal shape determines the spectrum characteristics and effectively dictates specific system requirements. In addition to wideband spectrum satisfying all the FCC demands, it should provide low power and low complexity to enable low-cost UWB systems. Moreover, ability to control and tune the pulse generator spectrum and time domain signals represents very desirable advantage because it provides compensation due to process, voltage and temperature (PVT) variations, regulatory differences, and changes in the channel or antenna characteristics. A special attention must to be paid to this part of an UWB transceiver, as it is highly challenging to design the PG fulfilling all abovementioned demands.

The FCC rules define only allowed frequency bands and radiated power spectral density (PSD) but there are no requirements on the time-domain shapes. Therefore, different PG topologies can be found in the literature. Historically, the first IR-UWB pulse generators have used some specific components such as step recovery diode. They demonstrated limited tunability and very difficult integration in standard CMOS process [12]. Recently reported UWB pulse generators use diverse method to produce appropriately shaped signal, usually 5th derivative of the Gaussian pulse. Authors in [13], create a baseband impulse and then up-convert it to desired frequency using mixer (and local oscillator). These are quite complex and power hungry solutions due to use of continuously operating local oscillators and/or mixers. Although having decreased circuit complexity and power consumption, switched or gated local oscillator-based pulse generators suffer from restricted control over the star-up and turn-off transients and the output pulse shape [14]. PGs using digital-to-analog converter principle offer good resolution and controllability, but require high sampling rates, resulting in high power and system complexity [15]. Distributed waveform generators using transmission lines demand quite large area and complex combination of separately generated pulses [16].

A new energy-efficient, simple pulse generator designed in low cost 0.18 μm UMC CMOS technology is addressed in the paper. The tunable generator based on pulse shaping approach has very simply architecture leading to the power consumption and occupied area savings. Additionally, it provides control of the generated signal duration and amplitude enabling compensation due to the PVT variations and ensuring FCC compliance.

2 Pulse generator architecture and design

The output spectrum central frequency of an oscillator-based pulse generator is defined by the ring oscillator frequency [14]. In our previously published paper, the pulse generator architecture consisting of the ring oscillator uses different approach [17]. Since the maximal ring oscillator frequency obtained in the 0.18 μm UMC CMOS technology is 3.95 GHz (schematic-level simulation result) [18]-[20], the technique of increase in the spectrum frequency by doubling the high-pass filter frequency in comparison with the oscillator frequency was used in the aforesaid paper. To obtain 5th derivative of the Gaussian pulse at the output, only one or two pulses at the ring oscillator output are generated and then shaped by the output filter. The main cause of the frequency restriction is the limited set of transistor sizes available in the used process [18]-[20]. As the full potential of the oscillator-based approach could not be achieved in the 0.18 μm UMC technology, a new method is addressed in this paper. The pulse generator architecture is simplified by leaving the ring oscillator out and shaping a very short pulse produced by an advanced glitch generator topology. This allows UWB mask to be efficiently utilized and at the same time provides decrease in the circuit complexity.

The block diagram and architecture of the proposed pulse generator is shown in Fig. 1. It mainly consists of a Data and clock synchronization block, a glitch generator, a buffer, and a pulse shaping filter.

Buffers (inverter chains composed of transistors M_1–M_8) sharp the rising and falling edge of the clock (*clk*) and data (*Data*) signals. Then, the input signals are synchronized using transmission gate with the *clk* signal as the input, and the *Data* and inverted data (*D*) signal as the control signals. The *clk* signal passes through the transmission gate when the *Data* is high. The inverter stage

(transistors M_{11}–M_{12}) isolates the synchronization block (the transmission gate) from the glitch generator and sharps the rising and falling edge of the forwarded signal.

The tunable glitch generator is based on a three-transistor glitch module with a controlled delay element, implemented by a current starved inverter (transistors M_{16}-M_{18}) [21]. The method can produce Gaussian glitch shorter than techniques the most commonly used in glitch generator design (requiring NAND or NOR gate) due to parasitic reduction. When the *Data* signal is low, the transistor M_{13} is turned on connecting the node *A* to V_{DD}. At rising edge of the *Data*, the transistor M_{14} turns on and toggles the two inverters to charge the output node and the transistor M_{15} gate, turning it on. The M_{15} transistor activation causes the node *A* voltage to decrease sufficiently to toggle the inverters and discharge the output completing the glitch signal. The produced pulse duration is controlled by varying the V_1 voltage. This value determines the current of the M_{16}-M_{17} inverter stage and thus the feedback delay to the gate of M_{15}.

The role of the controlled two-stage buffer (consisting of two current-starved inverters, transistors M_{21}-M_{23} and M_{24}-M_{26}) is multiple. It provides good isolation between the glitch generator and the subsequent transmitter stage. Furthermore, not only does it amplify the glitch signal (G_{out}) but also determines slope of the rising and falling edge of the signal at the filter input. Varying the control voltages V_2 and V_3 changes the buffer stages currents that define the rate of charging and discharging their output parasitic capacitances, and thus allows control of the rising/falling edge of the filter input signal. Since the filter is used as a differentiator in the time domain to form appropriate signal waveform, the amplitude and shape of the generated signal depend on the slope of the filter input signal edges. As a consequence, the amplitude and shape of the output signal are adjusted by varying V_2 and V_3 control voltages.

Since the output spectrum central frequency (depending on the time domain behavior) is determined by the slope/shape of the filter input signal and its characteristics, the pulse shaping filter frequency is set to value approximately equal to the center of the UWB bandwidth by choosing suitable components values: C_1=240 fF, L=1.6 nH and C_2=220 nH.

The ability to tune the output spectrum characteristics in means of the bandwidth and spectrum central frequency by varying the control voltages V_1, V_2 and V_3 enables compensation due to PVT variations and additional spectrum fitting within the FCC spectral mask.

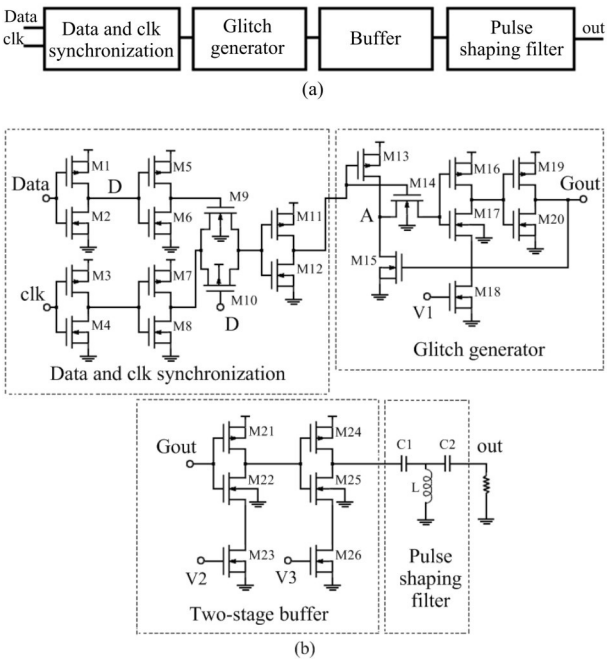

Figure 1: The proposed pulse generator: (a) block diagram and (b) circuit schematic.

3 Post-layout simulation results and comparison

The presented IR-UWB pulse generator is designed in a mixed mode/RF 0.18 µm UMC CMOS process and simulated using SpectreRF Simulator from Cadence Design System. The Assura (Cadence) and Calibre (Mentor Graphics) parasitic extraction tools have been used in post-layout simulations and obtained results were compared with each other. As those tools are the most commonly used in RF IC design, the presented results are very reliable.

The technology has supply voltage of 1.8 V. The generator supports on-off keying (OOK) modulation. This modulation type is adopted due to its simplicity as it allows the simplest transmitter realization, and consequently low power dissipation and the smallest chip area. It is well known that the energy efficiency and low transceiver cost represent the main advantages of the IR-UWB technology.

The proposed pulse generator is supposed to drive a 50 Ω load (the output resistor shown in Fig. 1(b)) representing the antenna characteristic impedance. Even though the UWB antenna impedance is not restricted to 50 Ω, this value is used for most of the models based on miniature commercial antennas. The pulse generator operates in burst mode with low duty cycle and pulse repetition frequency (PRF) of 100 MHz. This value of PRF marks the boundary between the low data

and high data rate applications, and it is considered as the lowest value for high data rate communications. The impulse regime with low duty cycle allows very low power dissipation of PGs. In general, the nature of the IR communication enables saving power between each pulses and consuming power just at the moment when the pulse is produced. The presented topology was optimized with the main goal to cover the lower UWB band with spectrum bandwidth as wider as possible, while still efficiently satisfying the FCC spectrum requirements. Additional aim was to minimize the power consumption and keep acceptable values for remaining Figures of Merits (FOMs). The main reason why the operation range is restricted to the lower UWB bandwidth is availability of measurement equipments. Our institute still has no required instrument but it is in a process of purchasing an oscilloscope that can measure time domain signals till 6 GHz. The proposed design is sent to fabrication and it is expected to be measured by the end of the year.

The pulse generator layout is shown in Fig. 2. The integrated circuit (IC) occupies a die area of 720 x 886 μm^2 including bonding pads, and the active circuit area is only 421 x 508 μm^2. The NMOS and PMOS transistor parameters values are given in Table 1. The transistors are made as multi-finger devices with the fixed channel length of 0.18 μm and variable gate width. The total transistors gate width is calculated by $W = ng \cdot 5$ μm, where 5 μm represents the gate finger width, and parameter *ng* the gate finger number which is in the range from 5 to 21 (the manufacturing process limitation). Additional technology recommendation is to use only odd values for the *ng* parameter. Since the 0.18 μm UMC CMOS is a twin-well process (without additional deep N-well layer), the bulks of all NMOS/PMOS transistors are connected to adequate reference voltages (GND in case of NMOS, and V_{DD} in case of PMOS transistors), shown in Fig 1(b).

The generated waveform and its spectrum are shown in Figs. 3 and 4, respectively. The pulse has peak-to-peak voltage amplitude (V_{pp}) of about 403 mV, and the duration about 0.6 ns. The 10 dB bandwidth of power spectral density (PSD) is from 3 GHz to 7.8 GHz. In fact the spectrum has wider bandwidth because the lower cut-off frequency is below 3 GHz (2.7 GHz). However, this is not taken into account since frequencies lower than 3 GHz are not considered in this kind of application. It can be noticed that the obtained PSD fully meets the FCC spectral mask except in the GPS band.

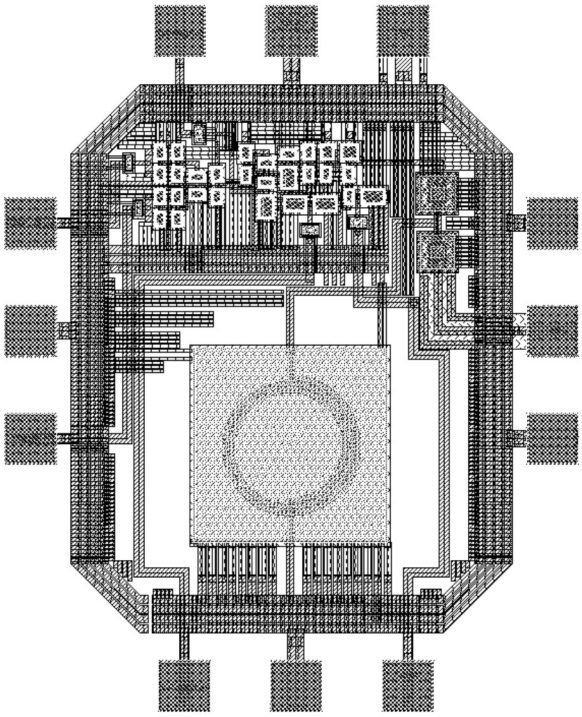

Figure 2: The IR-UWB pulse generator layout.

The PSD has maximum value of-43.78 dBm/MHz at 4.8 GHz, and a quite sharp roll off with more than 25 dB of out-of-band rejection relative to the peak power level. It is worth noticing that the peak value is very close to the maximal value regulated by the FCC alliance. The value could be increased to the FCC limit by choosing the appropriate set of control signals, but the corresponding spectral mask would be violated at frequencies around/below 3.1 GHz.

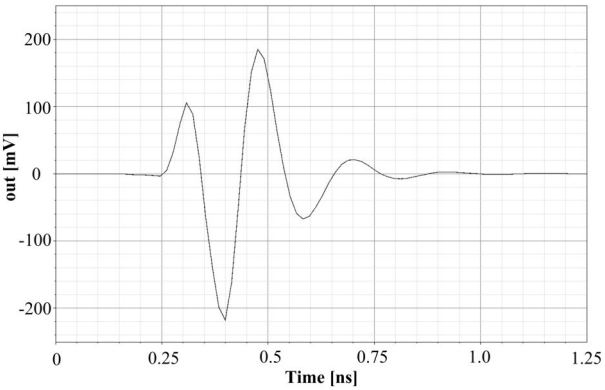

Figure 3: Pulse generator output waveform.

It should be emphasized that PG spectrum characteristics can be tuned in case of difference in post-layout

Table 1: The NMOS and PMOS transistors sizes.

Transistor	M1-12	M13	M14-16	M17	M18-20	M21	M22	M23	M24	M25,26
Width [μm]	25	35	25	105	25	45	25	105	75	25

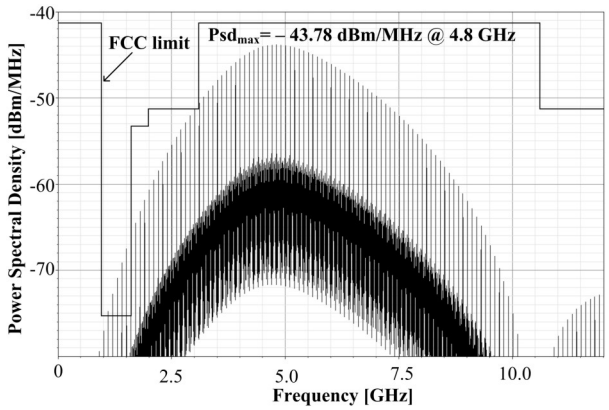

Figure 4: Pulse generator output power spectral density.

and measured results usually caused by the PVT variations. The pulse generator dissipates average power of only 1.3 mW corresponding to 13 pJ energy consumption per pulse for PRF of 100 MHz.

Table 2 summarizes the obtained post-layout simulation results of the proposed IR-UWB pulse generator and comparison to performance of the recently published PG designs. Although, it can be difficult to make fair comparisons when different specifications and technologies are used, it is clear that the proposed circuit has by far the highest peak-to-peak amplitude, the widest 10 dB bandwidth and the lowest power consumption. Moreover, other FOM are comparable to the results presented by the authors. The occupied area in Ref [25] is a little bit smaller comparing to layout dimensions presented here. However, it is expected since the chip is designed in scaled technology. The proposed pulse generator is suitable for ultra-low power wireless communication applications covering the 3 – 7.8 GHz frequency range.

4 Conclusion

A new energy-efficient tunable pulse generator is designed in 0.18 µm CMOS UMC technology for high date rate 3 – 7.8 GHz UWB applications. The time and spectrum domain signal adjustment is provided by varying the control voltage of tunable glitch generator and two-stage buffer composed of current starved inverted topologies. The power spectrum density of the output signal is tunable in order to provide compensation due to PVT variations and satisfies the FCC UWB mask requirements under different transmit conditions. The post-layout simulation results demonstrate that the proposed architecture has significantly lower power consumption and higher peak-to-peak amplitude compared to the previously reported UWB pulse generators covering the approximately the same frequency range.

Acknowledgments

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References

1. First report and order: revision of part 15 of the Commission's rules regarding ultra-wideband transmission systems Federal Communications Commission (FCC), ET Docket 98-153, adopted February 14, 2002, released Apr. 22, 2002.
2. M. Ghavami, L. B. Michael, and R. Kohno, "Ultra wideband signals and systems in communications engineering", John Wiley&Sons Ltd, 2004.
3. K. Siwiak and D. McKeown, "Ultra-wideband radio technology", John Wiley&Sons Ltd, 2004.
4. Multi-band OFDM physical layer proposal for IEEE 802.15 task group 3a, IEEE P802.15-03/268r2, Sep. 14, 2004.
5. DS-UWB physical layer submission to 802.15 task group 3a, IEEE P802.15, Mar. 2004.
6. R. Fernandes and D. Wentzloff, "Recent advances in IR-UWB transceivers: an overview", Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 3284–3287, 2010.
7. A. Medi, W. Namgoong, "A high data-rate energy-efficient interference-tolerant fully integrated CMOS frequency channelized UWB transceiver for impulse radio", IEEE Journal of Solid-State Circuits, vol. 43, no. 4, pp 974–980, 2008.

Table 2: Performance comparison of the IR-UWB pulse generators.

Reference	Power cons. [mW]	BW (-10 dB) [GHz]	Vpp [mV]	Pulse width [ns]	Die area [mm2]	PRF [MHz]	Technology
/24/	4.2	3.5 – 7.5	150	1	N/A	200	0.13 µm CMOS
/25/	3.8	3.0 – 6.0	230	0.5 – 0.9	0.44	910	0.13 µm CMOS
/26/	23.0	N/A	200	0.82	0.50	50	0.18 µm CMOS
This work	1.3	3 – 7.8	403	0.60	0.63	100	0.18 µm CMOS

8. N. Sasaki, K. Kimoto, W. Moriyama, T. Kikkawa, "A single-chip ultra-wideband receiver with silicon integrated antennas for inter-chip wireless interconnection", IEEE Journal of Solid-State Circuits, vol. 44, no. 2, pp. 382–393, 2009.
9. Y. Wang, A. Niknejad, V. Gaudet, K. Iniewski, "A CMOS IR-UWB transceiver design for contact-less chip testing applications", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 55, no. 4, pp. 334–338, 2008.
10. MS. Chae, Z. Yang, M. Yuce, L. Hoang, W. Liu, "A 128-channel 6mW wireless neural recording IC with spike feature extraction and UWB transmitter", IEEE Transactions on Neural Systems and Rehabilitation Engineering, vol. 17, no. 4, pp. 312–321, 2009.
11. C. Kim, S. Nooshabadi, "Design of a tunable all-digital UWB pulse generator CMOS chip for wireless endoscope", IEEE Transactions on Biomedical Circuits and Systems, vol. 4, no 2, pp. 118–124, 2010.
12. J. Lee, C. Nguyen, "Uniplanar picosecond pulse generator using step-recovery diode", Electronics Letters, vol. 37, no. 8, pp. 504–506, 2001.
13. J. Ryckaert et al., "Ultra-wide-band transmitter for low-power wireless body area networks: design and evaluation", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 52, no. 12, pp. 2515–2525, 2005.
14. O. Novak, C. Charles, R.B. Brown, "A fully integrated 19 pJ/pulse UWB transmitter for biomedical applications implemented in 65 nm CMOS technology", Proceedings of the IEEE International Conference on Ultra-Wideband (ICUWB), pp. 72–75, 2011.
15. J.Ch. Li, S. Jung, Y. Joo, P. Gui, "A current-steering DAC-based CMOS ultra-wideband transmitter with bi-phase modulation", Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), pp. 245–248, 2012.
16. Y. Zhu, J.D. Zuegel, J.R. Marciante, H. Wu, "Distributed Waveform Generator: A New Circuit Technique for Ultra-Wideband Pulse Generation, Shaping and Modulation", IEEE Journal of Solid-State Circuits, vol. 44, no. 3, pp. 808–823, March. 2009.
17. L. Nagy, J. Radic, A. Djugova, M. Videnovic-Misic, "Ultra Low-Power Low-Complexity Tunable 3-10 GHz IR-UWB Pulse Generator", Informacije MIDEM – Journal of Microelectronics, Electronic Components and Materials, vol. 42, no. 3, pp. 185–191, 2012.
18. J. Radic, A. Djugova, L. Nagy, M. Videnovic–Misic, "Body Effect Influence on 0.18μm CMOS Ring Oscillator Performance for IR-UWB Pulse Generator Applications", Proceedings of the IEEE Mediterranean Conference on Embedded Computing – MECO, pp. 170–173, 2012.
19. J. Radic, A. Djugova, L. Nadj, M. Videnovic–Misic, "Feedback Influence on Performance of Ring Oscillator for IR-UWB Pulse Generator in 0.18μm CMOS technology", Proceedings of the IEEE 28th International Conference on Microelectronics–MIEL, pp. 357 – 360, 2012.
20. J. Radic, A. Djugova, L. Nagy, M. Videnovic-Misic, Lj. Zivanov, "Comparison of Feedback Influence on Ring Oscillator Performance for IR-UWB Pulse Generator in 0.13μm and 0.18μm CMOS technologies", Proceedings of the 4th IFIP WG 5.5/SOCOLNET Doctoral Conference on Computing, Electrical and Industrial Systems – DoCEIS'13, pp. 603 – 610, 2013.
21. R. Hamdi, K. Elkhenissi, D. Deslandes, F. Nabki, "A Low-Power OOK Ultra-Wideband Transmitter with Power Cycling and Spectral Flexibility", Proceedings of the IEEE International NEWCAS Conference, pp. 197–200, 2010.
22. Y. Shamsa, W. A. Serdijn, "A 21pJ/pulse FCC Compliant UWB Pulse Generator", Proceedings of the IEEE International Conference on Circuits and Systems, pp. 497–500, 2010.
23. A.M. El-Gabaly, C.E. Saavedra, "A 5-GHz energy-efficient tunable pulse generator for ultra-wideband applications using a variable attenuator for pulse shaping", International Journal of Circuit Theory and Applications, doi: 10.1002/cta.792, pp. 150–167, 2011.
24. J. He, Y.P. Zhang, W.M. Lim, Y.Z. Xiong, "A fully integrated differential impulse radio transmitter", International Journal on Analog Integrated Circuits and Signal Processing, pp. 47–56, 2011.

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Amplitude Stabilization in Quadrature Oscilator for Low Harmonic Distortion

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Abstract: A simple non-linear network for amplitude stabilization in harmonic quadrature oscillator (QO) is analyzed. The oscillation startup conditions for QO topology with two operational amplifiers are used for amplitude adjustment by element values. A closed form expression for the amplitude setting resistance is derived. Total harmonic distortion (THD) is expressed as closed form function of the established amplitude. The derived expressions as well as the oscillator performance are verified by computer simulations and measurements.

Keywords: quadrature oscillator, harmonic distortion, integrator, steady state, sine wave

Stabilizacija amplitude v kvadraturnem oscilatorju za nizko harmonično popačenje

Izvleček: V prispevku je analizirano delovanje preprostega nelinearnega vezja za stabilizacijo amplitude kvadraturnega oscilatorja (QO). Nastavitev amplitude v QO z dvema operacijskima ojačevalnikoma je izvedena z vrednostmi elementov, ki vplivajo na zagonske pogoje. Vrednost upornosti za nastavljanje amplitude je določena z izpeljanim analitičnim izrazom. Harmonično popačenje (THD), ki ga vnaša vezje za amplitudno stabilizacijo, je podano kot funkcija amplitude in vrednosti elementov. Delovanje vezja za stabilizacijo amplitude in ustreznost izpeljanih izrazov je preverjeno z računalniško simulacijo in laboratorijskimi meritvami.

Ključne besede: kvadraturni oscilator, harmonično popačenje, integrator, sinusni signal

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1 Introduction

Oscillators represent an important electronic circuit that is included in almost every electronic device. The majority of them are used for clocking digital circuits that operate in sequential mode. The output signal of such time keeping oscillators is usually a square waveform - digital clock. Stable frequency and steep edges of the rising and falling edge are important properties that have to be assured by adequate design of the circuit. In common, such oscillators are realized as relaxation oscillator [1] (astable multivibrator) utilizing one or two capacitors which in combination with resistors determine the oscillating frequency and its temperature coefficient. For higher accuracy and stability of the frequency crystal and ceramic resonators are used. In the later case the core oscillator actually produces a sinusoidal signal [2] that is then amplified and clipped to become a square wave at the output.

Harmonic oscillators represent an important kind of circuits that operate in a quite different way. Ideally the frequency spectrum of the output signal should consist only of a single spectral line. In reality, there is no such thing as an ideal sine wave generator, but there is a variety of technical solutions approaching to this goal by minimizing certain imperfections. Numerous circuit topologies are used in order to meet the operating frequency band and the tolerated total harmonic distortion (THD).

For the audio frequency band extended up to several 100 kHz RC oscillators with operational amplifiers are an attractive solution. LC oscillators are known to have stable frequency and low distortion, but the physical size of inductances that would be used at the lower part of this frequency band becomes unacceptably big. In this frequency band spectrally pure sinusoidal

signal sources with residual distortion less than -66 dB (0.05 %) or -90 dB are required for testing low-distortion devices, such as audio amplifiers or line transformers for digital subscriber lines (xDSL), respectively.

Wien bridge oscillator is a good source of low THD sinusoidal signals if amplitude stabilization is achieved without challenging its low harmonic distortion. This can be achieved with rather complex networks [3]. Amplitude stabilizing solutions that include resistive device with negative temperature coefficient, like NTC or incandescent light bulb, are not suitable for oscillators operating at low voltages. The output signal amplitude is strongly influenced by the temperature of the ambient. In addition, the frequency is not very stable due to the low phase slope $d\varphi/d\omega$ of the feedback network, so relatively big changes of the oscillating frequency are caused by changes of the amplifier's phase response [4].

In this low to moderate frequency range quadrature oscillator (QO) is a better solution for a low distortion sine wave source then the formerly mentioned Wien bridge oscillator. The name quadrature oscillator is used for autonomous linear circuits that generate a pair of orthogonal or quadrature sinusoidal signals that are also maintaining sustained steady state oscilation. The quadrature signals are of the same amplitude with a phase lag $\pi/2$. If only one output signal is required, e.g., previously mentioned distortion measurements, then the signal with lower distortion can be selected.

QO outperform Wien bridge oscillators in the aspects of frequency stability and simple non inertial amplitude stabilization network. The output signal frequency is determined almost exclusively by time keeping passive elements, namely, capacitors and resistors. The oscillating frequency is virtually insensitive to characteristics of active devices, i.e., operational amplifiers. If temperature coefficients of capacitances and resistances of the elements in the QO are of the same magnitude but of opposite sign, then the frequency temperature coefficient is reduced at least for an order of magnitude.

QO in papers published in scientific and technical journals are mostly treated without considering the necessity of amplitude stabilization [5]. Low distortion of the QO signal can be achieved by a simple non-linear resistive circuitry. In other types of oscillator circuits this is often realized by lowering the gain of the amplifying non-linear device [6].

Analytical relations for the output signal amplitude and THD for the selected QO topology and amplitude stabilizing network are derived in the paper. At first, a detailed analysis of the circuit is performed with the aim to determine the conditions at which self oscillating can evolve. The results are used in the design of the non-linear resistive circuit that is then analyzed for its effects on the output. The obtained results are verified by SPICE simulations and experimental measurements.

2 Operation of quadrature oscillator

2.1 Ideal oscillator

In Fig. 1, the basic circuit concept of QO is shown. The elements in this simplified circuit are considered to be ideal, i.e., the voltage gain of operational amplifiers is infinite and frequency independent.

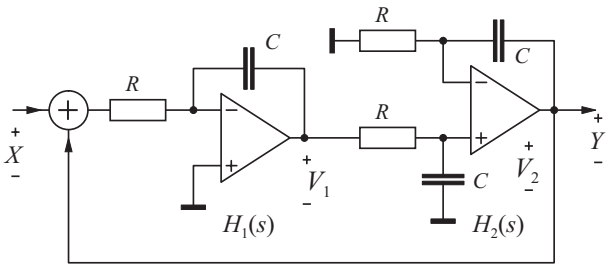

Figure 1: Explanatory scheme of QO based on two operational amplifiers

The circuit contains two integrators and an adding element that is actually just a wire. If the amplifiers are ideal, the system functions are

$$H_1(s) = -\frac{1}{RCs}, \quad H_2(s) = \frac{1}{RCs} \tag{1}$$

The system function $H(s)$ of the QO is then given as

$$H(s) = \frac{Y(s)}{X(s)} = \frac{T(s)}{1-T(s)} = -\frac{\omega_0^2}{s^2+\omega_0^2} \tag{2}$$

where $T(s) = H_1(s)H_2(s)$ and $\omega_0 = 1/(RC)$. The system function Eq. (2) has a pair of complex poles on the imaginary axis at $\pm j\omega_0$, that means the impulse response of the circuit is an undamped sine wave $V_m \cdot \sin(\omega_0 t)$. The amplitude V_m depends on the input stimulus or on initial conditions, whereas the frequency is set by the time constant RC. In reality it is necessary to obtain oscillating output of defined amplitude and without any starting signal. The system function must include a complex pair of poles lying initially on the right side of the s-plane, i.e., the real part has to be positive in order to obtain an increasing oscillating response. Ubiquitous thermal noise is sufficient to start the oscillatory process [7]. Exponential growth of the amplitude is unlimited as long as the elements remain linear. In order to obtain pure sine wave without any higher harmonic components, the pole pair has to be moved exactly on

the imaginary axis when the oscillation reaches the desired amplitude within the linear output range of real amplifiers. This start up process is depicted in Fig.2 by the position of the pair of complex poles.

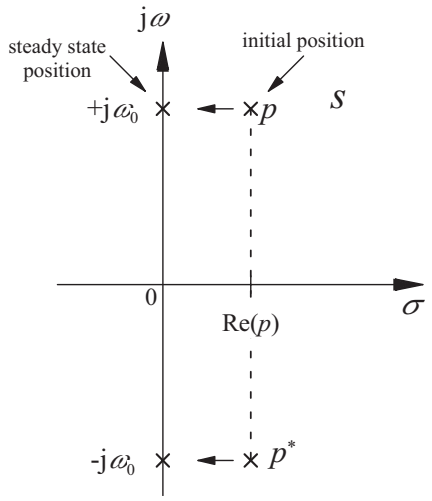

Figure 2: Oscillation determining pole pair during startup

2.2 System function of real QO

In order to find out the necessary starting conditions the most important parameters of real operating amplifiers must be considered. DC parameters like input offset voltage and input bias current have no effect on the operation of QO and are neglected. The most important parameters are open loop voltage gain A and the dominant pole frequency f_{op} that combine in the well known gain bandwidth product $GBW = A \cdot f_{op}$ (unity-gain bandwidth). For the sake of brevity, circular frequency ω_{op} is used in the system function of both operational amplifiers

$$A(s) = \frac{V_{out}}{V_{in}} = -\frac{A}{1+\frac{s}{\omega_{op}}} = -\frac{A\omega_{op}}{s+\omega_{op}} \tag{3}$$

The inverting integrator shown in Fig. 3 is slightly changed by the added resistance R_i to provide a means for altering the system function.

Using Eq. (3) the system function of the modified integrator is obtained

$$H_1(s) = \frac{V_1}{V_x} = \\ = \frac{-A\omega_{op}\omega_0}{s^2 + \left[\omega_0(1+\frac{R}{R_i}) + (A+1)\omega_{op}\right]s + \left[1+\frac{R}{R_i}(A+1)\right]\omega_{op}\omega_0} \tag{4}$$

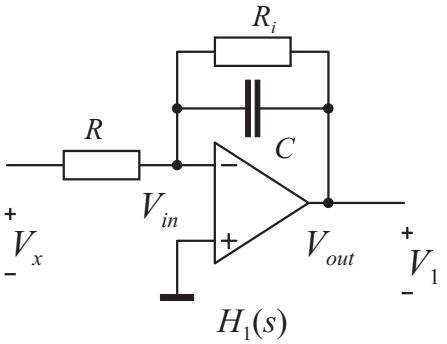

Figure 3: Inverting integrator with resistance R_i. Voltages V_{in} and V_{out} are indicated to clear up the designations used in Eq.

where $\omega_0 = 1/(RC)$. Eq. (4) is simplified by noting $A >> 1$ and $R/R_i << 1$ to obtain

$$H_1(s) = -\frac{A\omega_{op}\omega_0}{s^2 + (A\omega_{op} + \omega_0)s + A\omega_{op}\omega_0\frac{R}{R_i}} \tag{5}$$

without any loss of accuracy, because the exact value of DC open loop gain is not known. The poles of $H_1(s)$ can be determined if the values of gain bandwidth product $A \cdot f_{op}$ of usual amplifiers and the desired frequency f_0 are considered. Values of $A \cdot f_{op}$ are in the range 2 MHz to 10 MHz and thus bigger then the desired frequency f_0 <1 MHz. The denominator of $H_1(s)$ Eq. (5) can be factorized

$$H_1(s) = -\frac{\omega_0\omega_{op}A}{(s+A\omega_{op})(s+\frac{R}{R_i}\omega_0)} \tag{6}$$

yielding two real poles

$$p_1 = -\frac{R}{R_i}\omega_0 \ , \ p_2 = -A\omega_{op} \tag{7}$$

The lower pole p_1 depends on the oscillating frequency, whereas p_2 lies at the unity gain bandwidth of the amplifier. The same procedure is carried out for the system function $H_2(s)$ of the noninverting integrator

$$H_2(s) = \frac{A\omega_{op}\omega_0}{s^2 + (A\omega_{op} + \omega_0)s + \omega_{op}\omega_0} \approx \\ \approx \frac{A\omega_{op}\omega_0}{(s+A\omega_{op})(s+\frac{\omega_0}{A})} \tag{8}$$

The system function $H(s)$ of the oscillator is obtained from Eq. (2) by applying the derived results in Eqs. (6) and (8).

$$H(s) = -\frac{(A\omega_{op}\omega_0)^2}{\left(s^2 + (A\omega_{op} + \omega_0)s + \omega_0\omega_{op}\right)\left(s^2 + (A\omega_{op} + \omega_0)s + A\omega_{op}\omega_0\frac{R}{R_i}\right) + (A\omega_{op}\omega_0)^2} \tag{9}$$

Poles of $H(s)$ are can be estimated from the denominator $D(s)$ in and taking into account the approximate values of polynomial coefficients by omitting negligible terms.

$$D(s) = s^4 + 2A\omega_{op}s^3 + (A\omega_{op})^2 s^2 + (A\omega_{op})^2\omega_0\frac{R}{R_i}s + (A\omega_{op}\omega_0)^2 = \\ = \left(s^2 + 2A\omega_{op}s + (A\omega_{op})^2\right)\left(s^2 + bs + {\omega_0}^2\right) \tag{10}$$

The oscillator's system function has two real poles at $A\omega_{op}$ and a pair of complex poles whose real part depends on the coefficient b. By matching both sides of Eq. (10) the estimate for b is obtained as well as the position of the complex pair

$$b = \left(\frac{R}{R_i} - 2\frac{\omega_0}{A\omega_{op}}\right)\omega_0 \tag{11}$$

$$p_{1,2} = -\frac{b}{2} \pm j\omega_0 \tag{12}$$

The real part of the pole pair must be positive during start up and zero at steady state. The critical value of R_i is obtained from Eq. (11) respecting $b \leq 0$

$$R_i \geq \frac{R}{2}\frac{A\omega_{op}}{\omega_0} = \frac{R}{2}\frac{Af_{op}}{f_0} = R_0 \tag{13}$$

The amplitude of oscillation increases as long as $R_i > R_0$. The critical value depends on f_0 and the unity gain frequency of the used operational amplifier. The result obtained for the critical resistance in Eq. (13) is not always accurate because several approximations are involved in its derivation. The extent of inaccuracy of R_0 depends on the impact of the involved approximations. If a neglected term is two or more orders of magnitude smaller than the sum then such approximation has virtually no impact.

3 Amplitude stabilization

3.1 Non-linear circuit for amplitude stabilization

The circuit diagram of the oscillator shown in Fig. 4. includes the amplitude stabilizing network, which is made of two *pn* diodes and three resistors, is intended for amplitudes in the range 0.7 V to 2.5 V. Diodes D_1 and D_2 provide the required voltage threshold above which the stabilization process starts. Resistor R_3 improves the sharpness of the voltage threshold V_F by loading the diodes with a current that is several orders of magnitude greater than the current through R_2. Furthermore, resistor R_3 provides a path for the capacitive current of the diodes, so this current is shunted to the ground, thus the phase difference between the output voltage and the current of R_2 and is minimized.

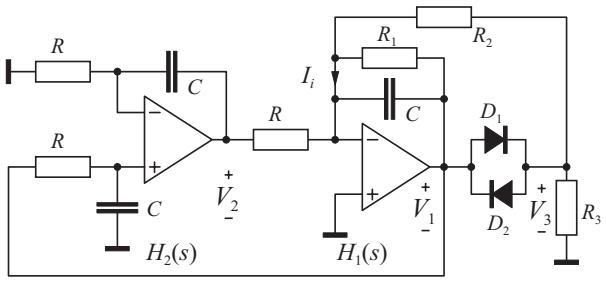

Figure 4: Two amplifier QO with amplitude stabilizing network

The amplitude V_m that is established at steady state can be determined from the plot shown in Fig. 4, that shows the relation between instantaneous values of voltage V_1 and current I_i as denoted in Fig. 3. For voltages $|v_1(t)| < V_F$ the current $i_i(t)$ is proportional to the voltage $i_i(t) = v_1(t) / R_1$. When $|v_1(t)|$ exceeds V_F the current $i_i(t)$ is increased by the contribution that flows through resistor R_2 causing that the apparent resistance felt by the integrator is decreased. Steady state amplitude V_m is obtained at the intersection point where currents are equal

$$I_i(V_m) = \frac{V_m}{R_0} \tag{14}$$

This description is not quite exact, because the wave shape of $i_i(t)$ is not sinusoidal. Only the fundamental harmonic component of current $i_i(t)$ must be respected. The output signal becomes distorted by higher harmonic components that are generated by this nonlinear network. These components should be kept as low as possible in order to minimize *THD* of the generated signal.

In spite of the fact that the piecewise-linear function shown in Fig. 5 is not suitable for accurate determination of the amplitude V_m, this function is useful to understand the influence of circuit parameters on amplitude stability and distortion. The impact of critical resistance's uncertainty ΔR_0 on the amplitude uncertainty ΔV_m increases as the angle of intersection between transfer function $I_i(V_1)$ and straight line V_i/R_0 is being decreased. Stable and well defined amplitude V_m is obtained if the value R_1 is high and R_2 is small, since this

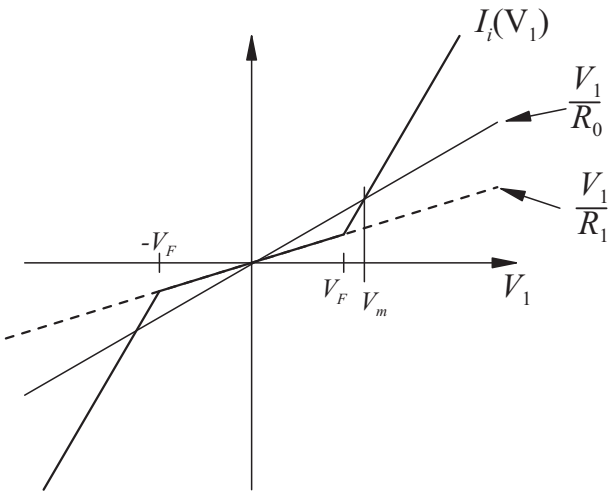

Figure 5: Plot of piecewise-linear transfer function $I_i(V_1)$

gives the largest angle of intersection, and as a consequence lowest sensitivity $\Delta V_m / \Delta R_0$. On the other hand, lower distortion can be obtained if larger tolerance of the amplitude is acceptable. In this case the elements are selected so that the lines intersect at smaller angle. In the next section this trade-off between stability and distortion is clarified by derived analytical expressions for harmonic distortion of the stabilized signal.

3.2 Harmonic analysis

As it is mentioned in the previous section, the plot in Fig. 5. is not adequate for the determination of sustainable amplitude. The effect of amplitude dependant resistance is achieved by the fundamental harmonic component of the current through R_2 that increases for voltages that are above or below V_F or $-V_F$, respectively.

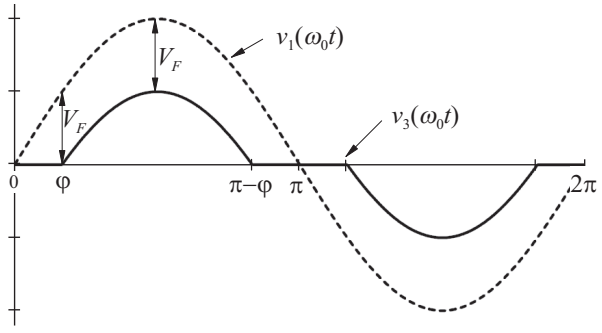

Figure 6: Idealized waveforms of the stabilizing network

For the purpose of harmonic analysis the diodes in the stabilizing network are replaced by piecewise linear relation that can be modeled as serial connection of ideal diode and a voltage source V_F. The obtained idealized waveform is shown in Fig. 6. For brevity, the harmonic components of the periodic voltage V_3 are denoted with C_k.

$$C_k = \frac{2}{T}\int_0^T v_3(t)\sin(k\omega_0 t)dt = \frac{2}{\pi}\int_{\varphi}^{\pi-\varphi}(V_m\sin(\alpha)-V_F)\sin(k\alpha)d\alpha \tag{15}$$

The calculation is simplified since the analyzed signal is odd and so all cosine terms are zero. The integration is preformed by substituting time with phase angle $\alpha = \omega_0 t$. The fundamental component is given by

$$C_1 = V_m\left[\left(1-\frac{2\varphi}{\pi}\right)+\frac{\sin(2\varphi)}{\pi}\right]-V_F\frac{4}{\pi}\cos\varphi \tag{16}$$

$$\varphi = \arcsin\frac{V_F}{V_m} \tag{17}$$

Higher odd components are given by

$$C_k = V_m\frac{2}{\pi}\left[-\frac{\sin((k-1)\varphi)}{k-1}+\frac{\sin((k+1)\varphi)}{k+1}\right]-V_F\frac{4}{\pi}\frac{\cos(k\varphi)}{k} \tag{18}$$

all even components are zero.

The expression for C_1 in Eq. (16) can be simplified by replacing Eq. (17) with equality.

$$C_{1ap} = V_m\left[\left(1-\frac{2}{\pi}\frac{V_F}{V_m}\right)+\frac{\sin(2\frac{V_F}{V_m})}{\pi}\right]-V_F\frac{4}{\pi}\cos\left(\frac{V_F}{V_m}\right) \tag{19}$$

First harmonic component of the distorted voltage V_3 is calculated using the both expressions. The results are plotted in Fig. 7 for values V_m above the threshold.

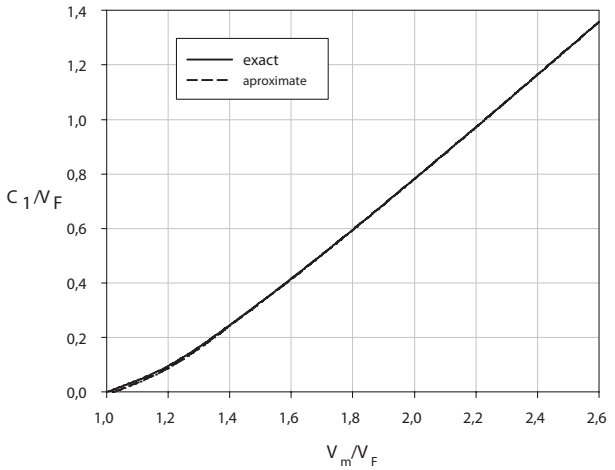

Figure 7: First harmonic component of the voltage V_3 vs. normalized amplitude V_m/V_F

The diagram in Fig. 7 shows that the difference between plots is negligible, so the simpler expression C_{1ap} is used for calculation of the resistances.

At first, R_1 is selected from the range $R_1 > R$, though it is advisable to choose at least $1.5 \times R_0$ to ensure a reliable startup. The selection of R_1 offers the possibility to control the distortion to certain extent. The value of R_2 is obtained as the solution of

$$\frac{V_m}{R_0} = \frac{V_m}{R_1} + \frac{C_{1ap}(V_m, V_F)}{R_2} \tag{20}$$

For the desired amplitude V_m, the value R_2 is then given by

$$R_2 = \left[1 - \frac{1}{\pi}\left(\frac{2}{a} - \sin\left(\frac{2}{a}\right) + \frac{4}{a}\cos\left(\frac{1}{a}\right)\right)\right]\left(\frac{1}{R_0} - \frac{1}{R_1}\right)^{-1} \tag{21}$$

whera a is the amplitude V_m normalized by V_F

$$a = \frac{V_m}{V_F} \tag{22}$$

3.3 Harmonic distortion

Harmonic distortion is caused by the higher harmonic components of the current flowing through R_2. This current flows through the integrating capacitor. The amplitude of harmonic components at the output is given by

$$V_k = \frac{|C_k|}{R_2}\left|Z_C(k\omega_0)\right| = \frac{|C_k|}{R_2}\frac{1}{k\omega_0 C} = \frac{|C_k|}{k}\frac{R}{R_2} \tag{23}$$

$$\frac{V_k}{V_m} = \frac{R}{k\,R_2}\frac{2}{\pi} \cdot \left|-\frac{\sin((k-1)a^{-1})}{k-1} + \frac{\sin((k+1)a^{-1})}{k+1} - \frac{2}{a}\frac{\cos(ka^{-1})}{k}\right| \tag{24}$$

The relative distortion in Eq. (24) is valid for normalized amplitudes $a > 1.2$. If the amplitude is closer to the threshold voltage, i.e., $a < 1.2$, then Eqs. (18) and (17) should be inserted in Eq. (23). The calculation of total harmonic distortion is simplified by considering only the third harmonic, because the contribution of higher frequency components to the RMS total distortion voltage is negligible. The distortion expressed in dB is obtained from Eq. (24)

$$THD[\text{dB}] = 10\log\frac{V_{D\,RMS}^2}{V_{1\,RMS}^2} \cong 20\log\frac{V_3}{V_m} \tag{25}$$

The curves of THD shown in Fig.7 can be used for the assessment of achievable performance of generated signal. Distortion of the output voltage depends on the critical value R_0 (Eq. (13)) and the resistance R. Plots in Fig. 8 are obtained for $R_0 = 150$ kΩ and $R = 3.9$ kΩ.

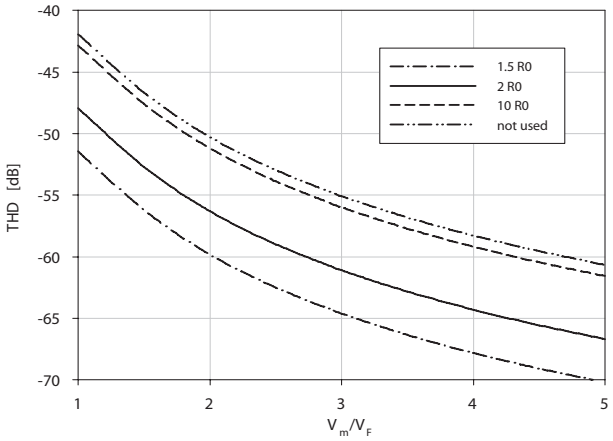

Figure 8: THD of QO with the proposed stabilizing network for typical values of R_1 against normalized amplitude

QO with larger normalized amplitude are featured with lower THD but the actual amplitude can substantially differ from the expected value. If R_1 is selected very close to the critical value R_0 then the maximal value from the worst case analysis must be used.

4 Results

4.1 SPICE simulations

The derived expressions for the amplitude V_m and *THD* were verified by simulations with SPICE and measurements of the realized circuit. Operational amplifiers TL071 with unity gain bandwidth 3 MHz have been used in the QO for 40 kHz. Ideal and real pn diodes have been used in the stabilizing network. The *I*(*V*) characteristic of real diodes has actually no pronounced voltage threshold therefore is V_F selected rather arbitrary. The threshold voltage of the diodes has become more pronounced by the load $R_3 = 1$ kΩ, which is low when compared to R_1 and R_2. The element values have been calculated with the assumption $V_F = 0.65$V. The ideal diode has been modeled by *b*-voltage source connected in parallel with R_3 and controlled by the output voltage V_2.The implemented threshold voltage has been the same as the assumed voltage for real diodes, i.e., 0.65V.

For the desired amplitude V_m, resistance R_2 has been obtained using Eq. (21). Steady state waveform for the defined circuit has been generated by transient analysis. Harmonic distortion has been determined from the spectrum. Flat top window has been applied on the generated signal. This window is suitable for determining discrete harmonic components of periodic signals. The broad and flat frequency response of this window has low spectral resolution, but has the important advantage that discrete spectral lines of periodic signals can-

not miss the flat part, so the spectral peak exactly corresponds to the amplitude of the harmonic component.

Table 1: Simulation results for $R_1 = 2 \cdot R_0 = 300\ k\Omega$

Input			Ideal diode		1N4148	
V_m/V_F	V_m [V]	R_2 [kΩ]	V_m [V]	THD [dB]	V_m [V]	THD [dB]
2	1.3	98	1.11	-53.0	0.9	-60.0
3	1.95	175	1.76	-59.5	1.7	-70.2
5	3.25	225	2.7	-63.0	3.4	-76.0

Table 2: Simulation results for circuit without R_1

Input			Ideal diode		1N4148	
V_m/V_F	V_m [V]	R_2 [kΩ]	V_m [V]	THD [dB]	V_m [V]	THD [dB]
2	1.3	58	1.25	-49.0	1.04	-53.3
3	1.95	87	1.8	-53.1	1.68	-59.1
5	3.25	112	2.8	-58.3	3.13	-66.1

Simulated THD for real pn diode in the limiting network is roughly 6 dB lower than for ideal diodes, which is a logical consequence of a smoother waveform $v_3(t)$. But these values are also too low when compared with theory, especially in the case when R_1 is missing.

4.2 Experimental results

The oscillator shown in Fig.3 has been used for experimental measurements to verify the possibility to build simple sinusoidal signal source for very low harmonic distortion. The same operational amplifier has been used as in simulations, namely TL071. It has turned out that the performance of the actual integrated circuit performed better than the spice subcircuit model provided by the manufacturer. The unity-gain bandwidth has proved to be higher, hence higher critical resistance has been used for the calculation of circuit elements in the amplitude stabilizing network. Harmonic components of the generated signal have been measured with spectrum analyzer HP 3589A.

The results are summarized in Table 3.

Table 3: Measured results

Expected value		$R_1 = 2 \times R_0 = 440\ k\Omega$			R_1 is not used		
V_m/V_F	V_m [V]	R_2 [kΩ]	V_m [V]	THD [dB]	R_2 [kΩ]	V_m [V]	THD [dB]
2	1.3	160	0.78	-61.1	86	0.87	-56.6
3	1.95	270	1.15	-60.0	130	1.22	-58.4
5	3.25	330	1.6	-61.7	180	1.72	-60.8

There is quite a substantial difference between expected amplitude and measured values for the circuit that includes resistance R_1. The voltage threshold of real diodes is not well pronounced but a better estimate can be acquired from the results for the circuit without resistor R_1, specifically $V_F = 0.4$ V seems to be a better choice for this purpose. The derived theoretical results concerning the relationship between R_2 and V_m are in sufficiently good agreement in simulations in which ideal diodes have been used. This is not a surprise as the relations are derived by the same approximation.

Measured THD for QO without resistor R_1 is in Fig.8 compared with analytical results for the usual range of normalized amplitudes. This range is featured with good amplitude stability and fair THD. A good match between the THD in Eqs. (25) and (24) and measured distortion can be noted.

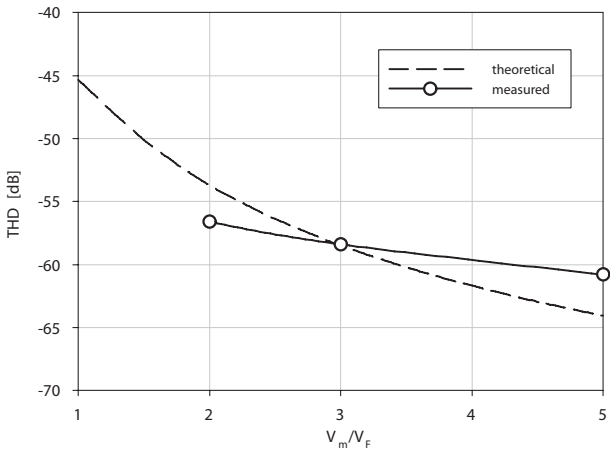

Figure 9: THD vs. normalized amplitude for QO without R_1

5 Conclusion

In this paper the performance of amplitude stabilizing network for QO has been analyzed. The derived relations offer a possibility to improve the performance of the circuit. The investigated oscillator is intended for low voltage operation, therefore only diodes are used for the non-linear network. Supply voltages and resistive dividers are usually used if stable larger amplitude is desired. In this case good stability of supply voltages is required. QO is a good and cheap source for sinusoidal voltages with moderate to low distortion for stand alone applications where digital solutions are not desired. The attained THD -61 dB has been measured at the output of the inverting integrator. THD of the quadrature signal V_2 is roughly 10 dB lower, because the third and higher harmonic components that are contained in V_1 are additionally attenuated. Low cost simple QO

with THD = -70 dB or 0.03 % can be achieved with proper circuit design based on the presented work.

References

1. J. R. Fernandes, M. H. L. Kouwenhoven, C. van den Bos, L. B. Oliveira, C.J. M. Verhoven, The effects of mismatches and delay on the quadrature error of a cross-coupled relaxation oscillator, IEEE Trans. on circuits and systems, Vol. 22, No.12, pp. 2592-2598, Dec 2007
2. R. J. Matthys, Crystal oscillator circuits, John Willey & Sons, 1983
3. C. W. Pei, Low distortion sine wave oscillator with precise RMS amplitude stability, Linear Technology magazine, March 2005, pp. 36
4. R. G. Irvine, Operational amplifier, Prentice-Hall, 1987
5. J. Bajer, J. Vavra, D. Biolek, K. Hajek, Low-distortion current-mode quadrature oscillator for low-voltage low-power applications with non-linear non-inertial automatic gain control, in European Conference on circuit theory and design, 2011, pp. 441-444.
6. S. M. A. Motakabber, M. I. Ibrahimy, Crystal controlled CMOS oscillator for 13.56 MHz RFID reader, Informacije MIDEM - Journal of Microelectronics, Electronic Components and Materials, 2013, 43(2), pp. 119-123
7. D. Ghosh, R. Gharpurey, Evolution of oscillation in a quadrature oscillator, in 24th Annual conference on VLSI design, 2011, pp. 36-40

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The influence of power supply voltage on exploitive parameters of the selected lamps

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Abstract: In the paper some results of measurements of the selected properties of the selected types of lamps are presented and discussed. Investigations were performed for the classical incandescent bulb, the energy-saving fluorescent lamp and the LED lamp. All the considered lamps are characterised by the luminous flux of the same value. The influence of the supply voltage on such exploitive parameters as: supply current, luminance of the lighted surface, case temperature, coefficient of total harmonic distortion of the supply current and power factor is taken into account. On the basis of the obtained results of investigations, some suggestions connected with the power supply built-in in the considered lamps are formulated.

Keywords: Lighting sources, power LEDs, measurements

Vpliv napajalne napetosti na izkoriščene parametre izbranih svetil

Izvleček: V članku so predstavljeni rezultati nekaterih meritev izbranih parametrov določenih tipov svetil. Raziskave so narejene na klasičnih žarnicah, energijsko varčnih fluorescentnih sijalkah in LED sijalkah. Vsa svetila so karakterizirana pri enakih vrednostih svetlobnega toka. Obravnavani so vplivi napajalne napetosti na izbrane parametre kot so: napajalni tok, svetilnost osvetlene površine, temperatura ohišja, koeficient totalne harmonične distorzije napajalnega toka in močnostni faktor. Na osnovi pridobljenih reultatov so podane posamezni predlogi v povezavi z napajanjem vgrajenim v svetila.

Ključne besede: svetila, močnostne LED, meritve

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1 Introduction

Nowadays, many kinds of electric light sources such: incandescent bulbs, compact fluorescent lamps (CFL), sodium lamps, halogenous bulbs or LED lamps are available in the market. The values of exploitive parameters of the mentioned light sources differ from one other considerably, for instance in their prices [1, 2]. The incandescent bulbs are currently the most popular and are the cheapest. However, according to the legal regulations obligatory in the European Union and in Australia, classical bulbs should disappear from the market by the year 2016 [3, 4]. The similar legal regulations are obligatory in China and in the USA [3].

A basic defect of bulbs is low value of luminous efficiency. It causes that only several percent of the electrical energy received by the bulb from the line is exchanged into light. Furthermore, the life time of these light sources typically does not exceed 1000 h [5, 6]. On the other hand, equivalents of bulbs in the CFL form are considerably more expensive and contain mercury, which is harmful for health. They also need long time indispensable to obtain full light. Additionally, in practice it is not possible to control brightness of these lamps [7]. In turn, sodium lamps, because of the spectrum of the emitted light, differing indeed from the spectrum of the sun light are mostly used in street lighting [8].

The economical and ecological aspects decided that after the elaboration of white light emitting diodes (LEDs) in the last decade of 20th century, the ideas to use them for lighting appeared [9]. After a dozen or so years LED lamps constituting equivalents of popular bulbs are available in the market [2, 4, 5]. Additionally, the available LED lamps designed for street lighting are offered together with suitable casings [3, 10].

In many papers devoted to power LEDs, eg. [3, 11-17], the problems connected with the use of these semiconductor devices for lighting are described. To these problems belong: remove of heat generated in the considered devices (over 80% of the energy received from the power source is exchanged into heat [3, 7]), the fall of the luminous flux at the temperature increase [17, 18, 19] and during the exploitation, necessity to use special power supplies for LEDs [3, 4, 7, 20, 21] and the exponential decrease of life time with temperature [6, 12, 22]. On the other hand, solid-state light sources are not sensitive to the network voltage fluctuations and make possible the easy control of brightness [5]. Moreover, they have very rapid growth of the value of luminous efficiency of these devices, which attain at present already 100 lm/W [3] and also have long life time (theoretically to 100000 hours, in practice - 25000 hours) [12, 22].

In the paper [4], the results of measurements of low-wattage LED lamps within the range of their influence on the supply line and temperatures of their cases are shown. The results of measurement of temperature distribution on the surface of the investigated lamps and and time courses of the supplied current are presented. The cited paper drawsour attention to the fact that the power factor of the investigated lamps can be less even then 0.5, and the case temperature of the LED lamp can exceed 70°C.

In turn, the paper [2] presents the results of measurements of electric, photometric and colorimetric parameters of the selected LED lamps being equivalents of classical bulbs. It is clear from the presented results of investigations that the declared by distributors of LED lamps values of their emitted luminous flux are smaller then of their classical equivalents. Additionally, it must be emphasised that LED lamps of the identical value of the nominal power can indeed differ from one other with regard to the value of the emitted luminous flux.

In the paper [5] exploitive proprieties of the selected types of LEDs are compared taking into account the influence of the supply voltage on the case temperature of the investigated lamps and the coefficient of the total harmonic distortion (THD) of the supply current. The results of measurements presented in the cited work showed that LED lamps offered by different producers indeed differed with regard to the value of the power factor (PF).

The investigation results presented in the cited papers refer to the light sources of different values of the exploitive parameters. In this paper the comparative results of measurements of characteristics of bulbs, CFLs and LED lamps are presented. The investigations were performed for lamps of different types of the close value of the emitted luminous flux.

2 Investigated lamps

Three lamps of the emitting luminous flux value equal to about 400 lm were arbitrarily selected: the LED lamp (OSRAM type PARATHOM CLASSIC A40 Warm White E27), the CFL (PHILIPS Eco Ambiance A A55 8W) and the classical bulb (OSRAM type CLAS A CL 40). The basic exploitive parameters of these lamps are collected in Table 1.

Table 1: Exploitive parameters of the investigated lamps [23, 24, 25]

Parameters	classical bulb	CFL	LED lamp
nominal power	40 W	8 W	8 W
nominal supply voltage	220-240 V	220-240 V	100-240 V
power factor	1	0.6	0.8
life time	1000 h	8000 h	25000 h
color rendering index	100	82	80
nominal luminous flux	415 lm	370 lm	345 lm
correlated color temperature	2700 K	2700 K	3000 K

As it is visible in Table 1, all the considered lamps can be used with the power supply from the line and they emit light of warm white colour. The essential differences refer to their life time (the longest for the LED lamp), the power factor (the biggest for the bulb) and luminous efficiency equal to the quotient of the emitted luminous flux through the nominal power (the best for the CFL).

3 Results

The proprieties of the lamps described in the previous section were examined in the measuring-set shown in Fig. 1. In this measuring-set the investigated lamp is supplied from the autotransformer. The RMS values of the supply voltage and current are measured by means of the voltmeter and the ampmeter. The current probe Tektronix TCPA300 together with the oscilloscope make possible determination of time courses and the spectrum of the supply current. The pyrometer Optex PT-3S measures the temperature in the warmest point of the casing of the lamp, while the illuminometer Sonopan L-100 equipped with the set to measure lumi-

nance allows measuring luminance of the lighted up area being found in the axis of the lamp within 75 cm below the stem of this lamp.

Using the presented measuring-set, the characteristics of the examined lamps illustrating the influence of the supply voltage on the supply current, the case temperature, the luminance of the lighted up area and the THD of the supply current were measured. The results of these measurements are shown in Figs.2-8.

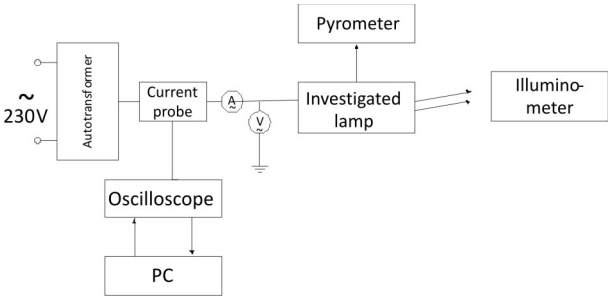

Figure 1: The block diagram of the measuring-set

Analyzing Figs. 2 and 3 one can see that the bulb begins to shine at the supply voltage equal to about 80 V and with an increase of this voltage the luminance of the lighted up area and the supply current increase visibly. In turn, the supply current of the CFL practically does not depend on the supply voltage, unless it exceeds the value 120 V. On the other hand, the luminance of the lighted up area by the CFL grows in the function of the supply voltage. The LED lamp is a light source the luminance of which practically does not depend on the supply voltage. In turn, the supply current of this lamp is a strongly decrescent function of this voltage. It is worth noticing that the luminance of the area lighted up by the bulb is the smallest, in spite of the greatest value of the luminous flux (see Table 1), of all the considered lamps. This is the result of the fact that the bulb emits radiation in the perigon, whereas the angle of emission of the remaining lamps is narrower.

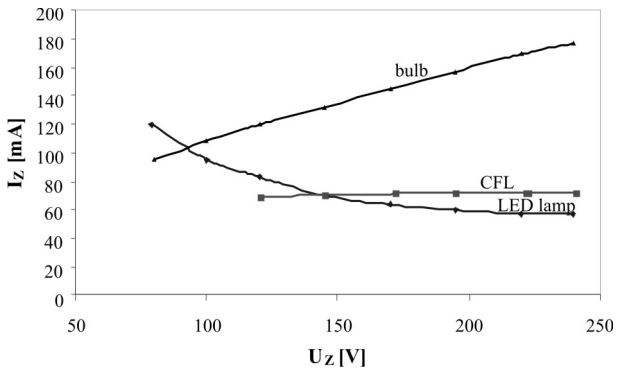

Figure 2: Measured dependences of the supply current on the supply voltage

The inequality of the area lighting obtained with the use of the considered lamps was analyzed. It turned out that for all the considered lamps the inequality of luminance distribution in the middle and on the circle of the ray of 10 cm did not exceed a dozen or so percent.

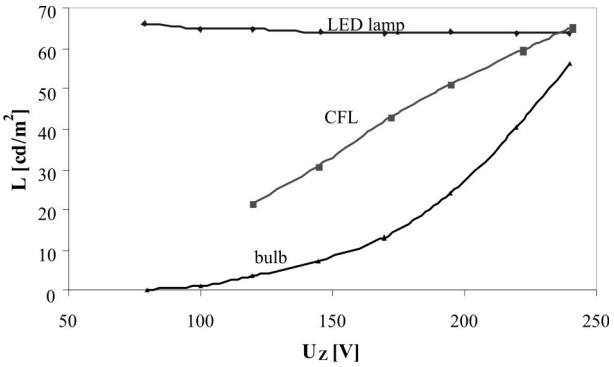

Figure 3: Measured dependences of the luminance on the supply voltage

The presented in Fig. 4, the dependences of the temperature of the lamp on the supply voltage show that all the investigated lamps strongly self-heat during the operation, even to over 130°C. The temperature of the bulb and the CFL is an increasing function of the supply voltage, while the temperature of the LED lamp is practically independent of this voltage.

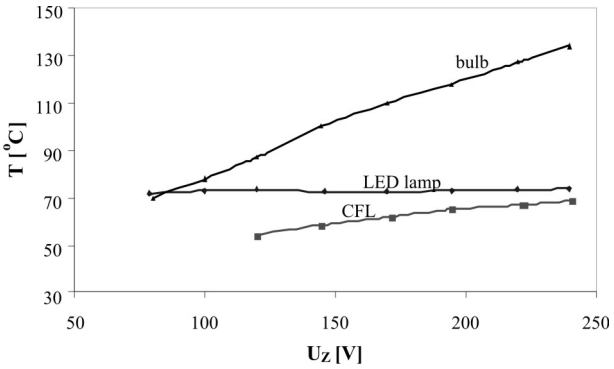

Figure 4: Measured dependences of the lamps temperatures on the supply voltage

The temperature of the case of the LED lamp is considerably lower and it does not exceed 72°C. The dependence of this temperature on the supply voltage shows the weak increasing tendency, which results from the fact that practically no changes of luminance of the area lighted up by these elements with the changes of the supply voltage are observed. Now then, the increase of their temperature is due mostly to an increase of power losses in the power supply system of the shining elements of the lamp.

From the point of view of the quality of electrical energy in the line, it is important that the supply current

of each device, e.g. lamps, should have the sinusoidal time course. In Fig. 5 the time courses of the supply current of the examined lamps measured at the supply voltage U_Z = 220 V are shown.

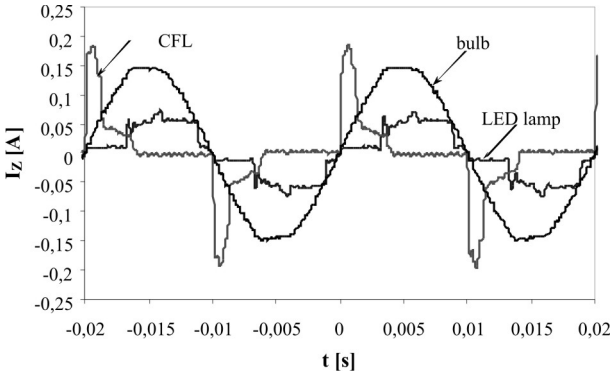

Figure 5: Measured time courses of the supply current of the lamps at the supply voltage U_Z = 220 V

From the point of view of the electric energy-network, the shape of the supply current of the investigated devices is of essential significance. Usually, the influence of the devices of the great power, e.g. industrial electric installations or large electric machines on the electric energy-network is considered [26]. Yet, a large number of diffuse low-power devices can also influence the quality of electrical energy significantly. Taking into account the fact that up to 30% of the used up electrical energy is used for lighting [6], the influence of lamps on the electric energy-network seems to be essential.

As one can observe, only the supply current of bulbs has the shape close to the sinusoid, and the remaining lamps receive the deformed current. To evaluate the degree of deformation of the supply current, the spectrum of the measured courses with the use of the fast Fourier transformation (FFT) is used. This spectrum, for all the examined lamps, is shown in Fig.6.

From Fig. 6 it is visible that for each of the considered lamps only the odd spectral stripes are visible. In the spectrum of the bulb current, practically only the stripe of the frequency about 50 Hz is visible. In turn, for the lamp LED the essential level of stripes are the stripes up to the ninth inclusively. The most strongly distorted is the supply current of the CFL, in which the spectrum harmonics up to 47th are visible.

Of course, the level of distorsions of the supply current of the lamp is relative to the supply voltage. In Fig.7 the dependence of the THD of this current of the examined lamps on the supply voltage is illustrated. As one can observe, the THD value is the least for the bulb, while the greatest for the CFL. The dependence THD(U_Z) for the CFL is a monotonically growing function, and the maximum value of this parameter exceeds 0.76. The LED lamp to a much smaller degree worsens the quality of the electrical energy, because for it the THD value does not exceed 0.4. For the LED lamp the THD attains the minimum at the supply voltage equal 120 V. This means that these lamps would influence less harmfully the electric energy-network, if there were supplied by the step-down transformer.

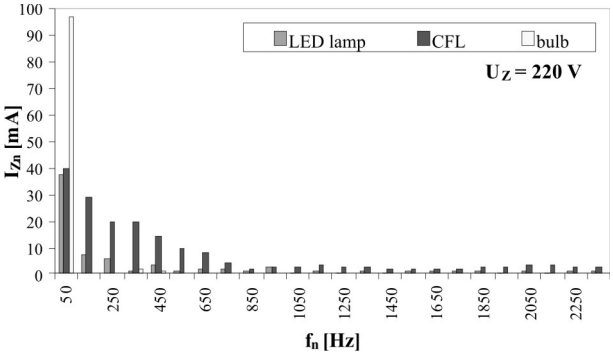

Figure 6: Measured spectrum of the supply current of the lamps at the supply voltage U_Z = 220 V

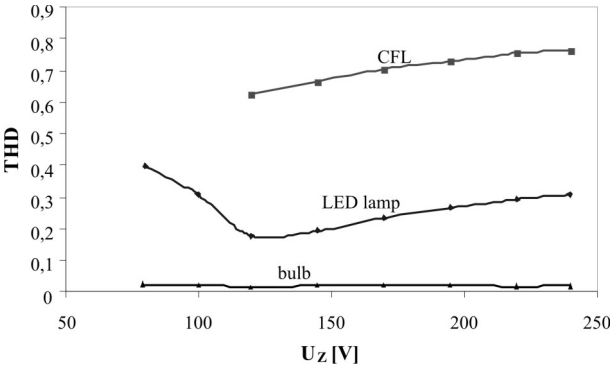

Figure 7: Measured dependences of the THD on the supply voltage

The considered lamps are dedicated to the operation at the nominal voltage of the electric energy-network. In such conditions the measurements of the active and apparent powers consumed by these devices and the power factor PF (equal to the quotient of the active and apparent powers) with the use of the instrument Voltcraft Energy Logger 4000F were performed. The obtained values of the power factor for the considered lamps are shown in Fig.8 in the form of the bar chart. Additionally, in this figure the values of the PF obtained from the equation, being the transformation of the dependence from the paper [26] were presented. This equation is of the form

$$PF = \frac{1}{\sqrt{1+THD^2}} \cdot \cos\varphi \qquad (1)$$

where φ denotes the phase shift between the supply current and the line voltage.

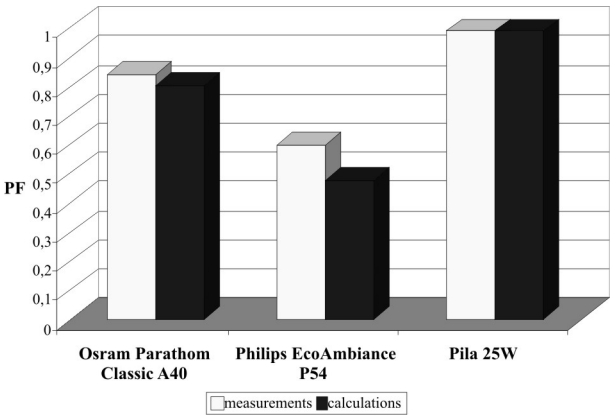

Figure 8: Measured and calculated values of the power factor of investigated lamps

The values of the power factor obtained from the measurements and values calculated from the equation (1) as well as the value of the THD calculated with the spectral stripes of the supply current are in agreement only for the bulb, whereas for the LED lamp and the CFL the essential differences between these values are observed. These differences result probably from the simplified manner of the measurements of the power factor in the device Voltcraft Energy Logger 4000F, which is based on the measurements of the phase shift between time courses of the supply current and the line voltage. This manner is correct only for lineal circuits [26]. Such a manner assures the reliable results, when these signals are not strongly deformed, which is not the case in the considered situation. It is worth noticing that the value of the power factor of the investigated LED lamp is comparatively high and negligibly exceeds 0.8, while for the CFL, the PF amounts to only 0.55. This means that the examined lamps unfavourably influence the quality of the electrical energy.

4 Conclusions

In the paper, the results of measurements of characteristics of the selected lamps were presented. From the presented results of the investigations one can draw the conclusion that at the nominal value of the supply voltage, the LED lamp consumes from the line the current of the least value. Because of the built-in swiching converter, the LED lamp assures the nominal luminous flux already at the supply voltage equal to 80 V. The power supplies built-in into the LED lamp and the CFL cause that the current consumed from the line by these lamps has not the sinusoidal course characteristic, like for the bulb. From among the examined lamps, the most negative influence on the electric energy-network has the CFL for which the THD exceeds even 0.76. As the result of heat generation in electronic circuits built-in in the CFLs and LED lamps the case temperature of these devices is high - it exceeds even 70°C.

Analyzing the spectrum of the supply current of the examined lamps, one can state that the reliable estimation of the value of the power factor of the examined lamps requires taking into account even 50 harmonics of the line frequency. Therefore, simple instruments used to measure the power factor can give the excessive value of this parameter. The high value of the THD of CFLs and the content of harmful mercury in these lamps should soon cause elimination of these lamps from the market. The LED lamps are already more and more spread and take their place. The use of LED lamps on mass-scale should bring down the inprice and make it possible to introduce, the power factor correction circuits (PFC) in the power supplies used in these lamps. The integrated circuits dedicated for this end are already offered by many producers.

It is worth noticing that luminous efficiency of LED lamps depends not only on luminous efficiency of the used LEDs, but also on watt-hour efficiency of the power supply applied in the lamp. For example, the luminous efficiency of the LED lamp examined in this paper amounts to only 43 lm/W, while the luminous efficiency of power LEDs already some years ago exceeded 100 lm/W [3].

References

1. *Craford M.G.: "Current State of the Art in High Brithness LEDs". CTO American Physical Society, Solid State Lighting Session, 6 March 2007.*
2. Czyżewski D.: "LED substitutes of conventional incandescent lamps". Przegląd Elektrotechniczny, Vol. 88, No. 11a, 2012, pp.123-127.
3. Weir B.: "*Driving the 21st Century's Lights*". IEEE Spectrum, Vol. 49, No. 3, 2012, pp. 42-47.
4. Uddin S., Shareef H., Mohamed A., Hannan M. A.: „*Harmonics and thermal characteristics of low wattage LED lamps*". Przegląd Elektrotechniczny, Vol. 88, No. 11a, 2012, pp. 266-271.
5. Górecki K., Górecka K., Górecki P.: „*Porównanie właściwości eksploatacyjnych wybranych typów lamp LED*". Przegląd Elektrotechniczny, Vol. 88, No. 11a, 2012, pp. 111-114.
6. Krames M.: "*Progress and Future Direction of LED Technology*". 2003, www.netl.doe.gov/ssl/PDFs/Krames.pdf.
7. Cheng Y.K., Cheng K.W.E.: "*General Study for using LED to replace traditional lighting devices*". 2nd International Conference on Power Electronics

Systems and Applications ICPESA '06, Hong Kong, 2006, pp. 173 - 177.
8. *"LEDs: Coming soon to a street light near you". Lumileds, White Paper WP14, 2010.*
9. Mroziewicz B.: *„Biało-świecące diody LED rewolucjonizują technikę oświetleniową"*. Elektronika, No. 9, 2010, pp 145-154.
10. Zalewski S.: "*Application of LEDs in road lighting*". Przegląd Elektrotechniczny, Vol. 85, No. 11, 2009, pp. 280-282.
11. Wiśniewski A.: *„Diody elektroluminescencyjne (LED) - analiza obecnych konstrukcji i możliwości zastosowania w oświetleniu"*. Przegląd Elektrotechniczny, Vol. 85, No. 11, 2009, pp. 300-303.
12. Górecki K., Zarębski J.: *„Wpływ wybranych czynników na właściwości półprzewodnikowych źródeł światła"*. Elektronika, No. 10, 2008, pp. 73-77.
13. Krejcar O., Frischer R.: "Smart intelligent control of current source for high power LED diodes". Microelectronics Journal, Vol. 44, 2013, pp.307-314.
14. Bianco A. M., Parra E. E.: "Effects of high peneteration of CFLs and LEDs on the distribution networks". 14th International Conference on Harmonics and Quality of Power (ICHQP), 2010, pp.1-5.
15. Qu X., Wong S.C., Tse C.K.: "Resonance assisted buck converter for offline driving of power LED replacement lamps". IEEE Transactions on Power Electronics, Vol. 26, 2011, No. 2, pp. 532-540.
16. Chen N., Chung H.S.N.: "Adriving technology for retrofit LED lamp for fluorescent lighting fixtures with electronic ballasts". IEEE Transactions on Power Electronics, Vol. 26, 2011, No. 1, pp. 588-601.
17. Qin Y., Lin D., Hui S.Y.: "A simple method for comparative study on the thermal performance of LEDs and fluorescent lamps". IEEE Transactions on Power Electronics, Vol. 24, 2009, No. 7, pp. 1811-1818.
18. Górecki K., Górecka K.: *„Wpływ zjawisk cieplnych na właściwości diody LED mocy"*. Przegląd Elektrotechniczny, Vol. 87, No. 7, 2011, pp. 144-147.
19. Górecki K.: "*Electrothermal model of a power LED for SPICE*". International Journal of Numerical Modelling Electronic Network, Devices and Fields, Vol. 25, No. 1, 2012, pp. 39-45.
20. Schubert E.F.: "*Light-Emitting Diodes. Second Edition*". Cambridge University Press. New York, 2008.
21. Wojtkowski W.: "Step-up converters for power LED power supply". Przegląd Elektrotechniczny, Vol. 87, 2011, No. 4, pp. 71-72.
22. Narendran N., Gu Y.: "*Life of LED-based white light sources*". Journal of Display Technology, Vol. 1, No. 1, 2005, pp. 167- 171.
23. PARATHOM CLASSIC A40 Warm White E27. Catalogue data, Osram 2012.
24. Product description: Economy Ambiance. Philips, 2011.
25. CLAS A CL 40. Catalogue data. Osram, 2012.
26. Rashid M. H., "Power Electronic Handbook", Academic Press, Elsevier, 2007.

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PATTERN GENERATOR 1979-2012

Ni preminil, le upokojil se je. Srečate ga lahko v avli Fakultete za elektrotehniko Univerze v Ljubljani.

Slikovni generator (angl. Pattern Generator) je ključna naprava polprevodniške tehnologije, ki omogoča izdelavo osnovnih orodij tehnologij, fotomask. Na primer: za izdelavo polprevodniškega integriranega vezja (čipa) potrebujemo set do 18 mask.

Slikovni generator je računalniško podprt optični sistem velike natančnosti, zgrajen na 1,5 t težkem granitu, izoliran od okolice in montiran v lastni brezprašni komori. Točnost naprave sloni na strogo kontroliranem okolju, elektroniki in laserskem interferometru.

Zgrajen je bil leta 1979 in predstavlja vrhunec tehnologije osemdesetih. Leta 1980 je bil instaliran v prostorih Laboratorija za mikroelektroniko na Fakulteti za elektrotehniko Univerze v Ljubljani, LM-FE. Fakulteta je bila namreč vključena v Iskrin projekt prenosa tehnologije. Tako je tudi raziskovalna skupina LM-FE dobila priložnost izpopolniti svoje znanje v »silicijevi dolini« v ZDA. Še več, bila je polno vključena tudi v Iskrine mednarodne projekte.

Slikovni generator je bil jedro oddelka za fotomaske skupine LM-FE in v tistem času edina naprava te vrste v tem delu Evrope. Ekipa oddelka je takrat delovala 24 ur na dan in 365 dni v letu, da je lahko zadostila potrebam ne samo Iskre ampak tudi industrije tedanje Jugoslavije in celo tujine! Moto te zelo intenzivne dejavnosti je bil: ostati v konici s svetovne tehnologije in vključiti v to sredino tudi čim večji del znanstveno raziskovalne dejavnost Univerze v Ljubljani. Tako smo lahko v mikroelektronske tehnologije vložili tudi veliko lastnega znanja in prispevali svoj kameček v mozaiku svetovnega napredka. Slikovni generator je bil naše prepotrebno osnovno orodje. Tudi to napravo smo izpopolnjevali po lastnih zamislih. Posodobili smo komunikacijo, razvili lastna orodja in omogočili prenos podatkovnih baz tudi preko osebnega računalnika. V svojem več kot tridesetletnem delovanju je naprava več kot opravičila svoj obstoj. Skupini LM-FE je odprla ne samo okno, temveč tudi vrata v svet miniarurizacije elektronike.To je v svet majhnih dimenzij, kjer so tranzistorji manjši od bacilov in mikrobov! Najzahtevnejši projekti so tako postali uresničjivi.

Dvaintrideset let je dolga doba za napravo visoke tehnologije. V letu 2012 je ta naprava tehnološko zastarela. Optika in mehanika sta sicer še vedno v najboljšem stanju, pač pa sta elektronika in spremljajoči računalniški sistem ne samo zastarela temveč tudi energetsko potratna. Zadnji set polprevodnikih mask smo naredili v letu 2011.

Naprava je odigrala pomembno vlogo v razvoju slovenske (in svetovne) mikroelektronike. Nedvomno predstavlja zgodovinsko dediščino in je kot muzejski eksponat razstavljena v avli Fakultete za elektrotehniko v Ljubljani.

Dr. Ivan Jan Lokovšek v imenu raziskovalne skupine LM-FE

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