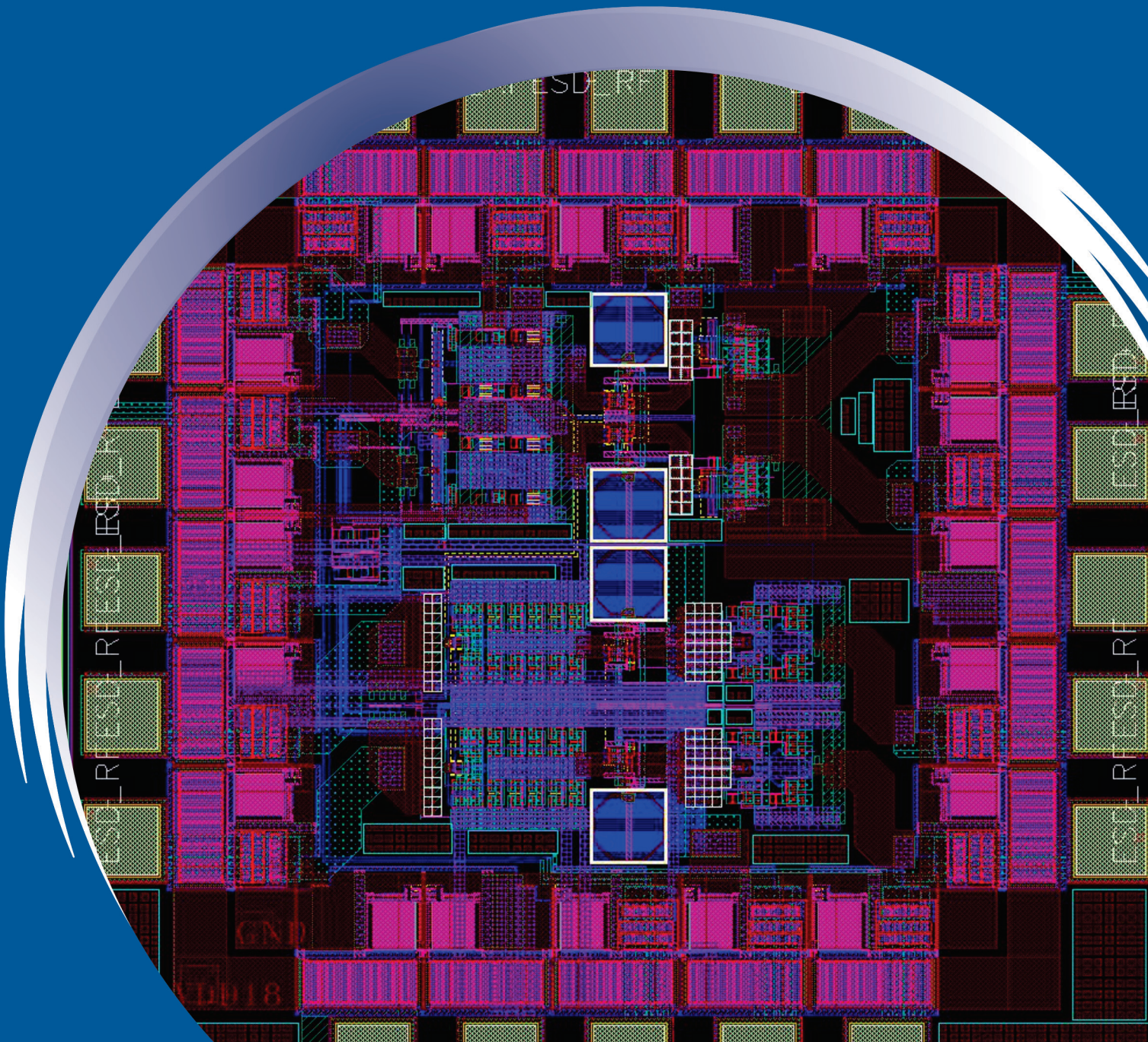
ISSN 0352-9045

Informacije MIDEM

Journal of Microelectronics, Electronic Components and Materials
Vol. 46, No. 2(2016), June 2016

Revija za mikroelektroniko, elektronske sestavne dele in materiale
letnik 46, številka 2(2016), Junij 2016



UDK 621.3:(53+54+621+66)(05)(497.1)=00 ISSN 0352-9045

Informacije MIDEM *2-2016*

Journal of Microelectronics, Electronic Components and Materials

VOLUME 46, NO. 2(158), LJUBLJANA, JUNE 2016 | LETNIK 46, NO. 2(158), LJUBLJANA, JUNIJ 2016

Published quarterly (March, June, September, December) by Society for Microelectronics, Electronic Components and Materials - MIDEM.

Headquarters | Naslov uredništva
Uredništvo Informacije MIDEM
MIDEM pri MIKROIKS
Stegne 11, 1521 Ljubljana, Slovenia
T. +386 (0)1 513 37 68
F. + 386 (0)1 513 37 71
E. info@midem-drustvo.si
www.midem-drustvo.si

Annual subscription rate is 160 EUR, separate issue is 40 EUR. MIDEM members and Society sponsors receive current issues for free. Scientific Council for Technical Sciences of Slovenian Research Agency has recognized Informacije MIDEM as scientific Journal for microelectronics, electronic components and materials. Publishing of the Journal is cofinanced by Slovenian Research Agency and by Society sponsors. Scientific and professional papers published in the journal are indexed and abstracted in COBISS and INSPEC databases. The Journal is indexed by ISI® for Sci Search®, Research Alert® and Material Science Citation Index™. |
Letna naročnina je 160 EUR, cena posamezne številke pa 40 EUR. Člani in sponzorji MIDEM prejemajo posamezne številke brezplačno. Znanstveni svet za tehnične vede je podal pozitivno mnenje o reviji kot znanstveno-strokovni reviji za mikroelektroniko, elektronske sestavne dele in materiale. Izdajo revije sofinancirajo ARRS in sponzorji društva. Znanstveno-strokovne prispevke objavljene v Informacijah MIDEM zajemamo v podatkovne baze COBISS in INSPEC. Prispevke iz revije zajema ISI® v naslednje svoje produkte: Sci Search®, Research Alert® in Materials Science Citation Index™.

Design | Oblikovanje: Snežana Madić Lešnik; Printed by | tisk: Biro M, Ljubljana; Circulation | Naklada: 1000 issues | izvodov; Slovenia Taxe Percue | Poštnina plačana pri pošti 1102 Ljubljana

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
vol. 46, No. 2(2016)

Content | Vsebina

Editorial | Uvodnik

Dear Reader,

This issue brings six original scientific papers. It also introduces a new category of news. PhD theses successfully defended at universities and graduate schools in Slovenia in 2015 that are related to the fields of microelectronics, electron components and materials are listed at the end of the issue. And we will repeat it in the second issue every year.

We look forward to receiving your next manuscript(s) in our on-line submission platform:
http://ojs.midem-drustvo.si/index.php/InfMIDEM

Enjoy reading the Issue 2/2016!

Prof. Marko Topič
Editor-in-Chief

P.S.
All papers published in *Informacije MIDEM* –Journal of Microelectronics, Electronics Components and Materials (since 1986) can be access electronically for free at http://midem-drustvo.si/journal/home.aspx. A search engine is provided to use it as a valuable resource for referencing previous published work and to give credit to the results achieved from other groups.

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 2(2016), 57 – 64

Population Ranking Based Differential evolution with Simulated Annealing for Circuit Optimization

Jernej Olenšek, Árpád Bűrmen

University of Ljubljana, Faculty of Electrical Engineering, Ljubljana, Slovenia

Abstract: Finding the values of circuit parameters for which the resulting circuit satisfies the design requirements can be formulated as an optimization problem. This problem is often solved using global optimization algorithms that provide some guarantee the resulting solution is the best possible one provided that the algorithm is given sufficient time. Unfortunately, these algorithms are slow and require many circuit evaluations. One of the algorithms proposed in our past research is PSADE that combines the favorable properties of simulated annealing and differential evolution and was shown to be a fast and reliable tool for solving circuit optimization problems. To make PSADE faster we replace the Metropolis criterion for accepting a trial point with one that is based on population ranking. The proposed algorithm retains its highly parallel nature. We tested the algorithm on a set of mathematical test functions and on a real-world circuit optimization problem. The results on the analog circuit sizing case show that the modified algorithm is more efficient and reliable than PSADE and some other global optimization methods.

Keywords: differential evolution; simulated annealing; population ranking; global optimization;, circuit design

Optimizacija vezij z diferencialno evolucijo in simuliranim ohlajanjem na osnovi rangiranja populacije

Izvleček: Iskanje vrednosti parametrov, pri katerih vezje zadosti načrtovalskim zahtevam, lahko predstavimo kot optimizacijski problem, ki ga pogosto rešujemo z globalnimi optimizacijskimi postopki. Ti nam zagotavljajo, da bomo našli najboljšo možno rešitev pod pogojem, da ima postopek na razpolago dovolj časa. Na žalost tovrstni postopki zahtevajo veliko simulacij vezja. Eden od postopkov, ki smo jih razvili, je postopek PSADE, ki združuje ugodne lastnosti diferencialne evolucije in simuliranega ohlajanja in se je izkazal kot hiter in zanesljiv pri optimizaciji vezij. Da bi postopek pospešili, smo zamenjali Metropolisov kriterij za sprejem točk s kriterijem, ki temelji na rangu točke znotraj populacije. Dobljeni postopek lahko zelo učinkovito paraleliziramo, saj obdrži vse ugodne lastnosti postopka PSADE. Preizkusili smo ga na naboru matematičnih funkcij in na praktičnem primeru iz načrtovalske prakse. Rezultati kažejo, da je pri načrtovanju vezij predlagani postopek bolj učinkovit in zanesljiv kot nekatere druge znane globalne optimizacijske metode

Ključne besede: diferencialna evolucija; simulirano ohlajanje; rangiranje populacije; globalna optimizacija; načrtovanje vezij

** Corresponding Author's e-mail: jernej.olensek@fe.uni-lj.si*

1 Introduction

Choosing the values (parameters) of circuit components (also referred to as circuit sizing) with the goal of satisfying the design requirements can be formulated as an optimization problem by introducing a cost function (CF) that reflects the quality of the circuit in a real number. Finding the best performing circuit reduces to finding the minimum of a CF. Unfortunately real-world CFs have many local minima. Finding the best local minimum is a computationally hard problem that is addressed with global optimization algorithms.

Many global optimization algorithms were devised in the past. Some of the most successful mimic the evolution (e.g. [1, 2]) and behavior (e.g. [3, 4]) of living beings and physical processes (e.g. [5, 6]). Simulated anneal-

ing (SA) ([7, 8]) was one of the first global optimization algorithms drawing its inspiration from the process of cooling a metal. Due to its nature this algorithm is capable of finding a global minimum, albeit with a large number of CF evaluations.

Due to the so-called "no free lunch" theorems [9] the research in the area of global optimization started to focus on hybrid algorithms (e.g. [10, 11]). In our past research we hybridized SA with differential evolution (DE) [12] which resulted in the parallel simulated annealing and differential evolution algorithm (PSADE) [14] that exhibited good performance on mathematical test functions, as well as, real world circuit design problems. Due to the SA component of PSADE it can mathematically be proven that the algorithm converges to a global minimizer given a sufficiently large number of CF evaluations. PSADE is highly parallelizable which makes it possible to significantly speed up the optimization when multiple processors are available.

PSADE has the same drawbacks as other heuristic optimization algorithms. Most notable is the possibility of premature convergence to a local minimizer. The main cause of this drawback is the Metropolis acceptance criterion of SA which often rejects trial points that would otherwise lead the algorithm away from a local minimizer. Furthermore, the Metropolis acceptance criterion is based on an artificial parameter (temperature) that is based on the CF value. Because the CF value can differ to a great extent between similar optimization problems the acceptance criterion can be misguided into rejecting promising points.

To counter this drawback and simplify the algorithm we propose a different approach for accepting points based on the solution ranking within the population. The rank of the point is determined by sorting the points according to their CF value. We also assign every individual in the population a separate position. In turn, every position is assigned a set of parameters for SA and DE. Parameters corresponding to higher positions have a greater probability to be used in the process of constructing and evaluating a trial point. The algorithm tries to align the positions of individuals within the population with their ranks. This alignment is occasionally broken to increase the probability of accepting an inferior solution which may lead the algorithm away from a local minimum. We deem the proposed algorithm DESAPR (DE and SA with Population Ranking).

The paper is divided as follows. Section 2 outlines the proposed approach. The asynchronous parallel version of the algorithm is the subject of section 3. The optimization results for mathematical test function are given in section 4 while section 5 presents the results obtained on a real-world circuit optimization problem. Section 6 concludes the paper.

Notation. Vectors are denoted by bold lowercase letters. The *i*–th component of vector $\boldsymbol{a}$ is denoted by a_i. Inequalities are applied to vectors component-wise. The realization of a uniformly distributed random number from interval (0,1) is denoted by $U(0,1)$.

2 The proposed method

The problem subject to optimization can mathematically be formulated as

$$\begin{aligned} &\boldsymbol{x}^* = \operatorname{argmin}_{\boldsymbol{x}\in S} f(\boldsymbol{x}) \\ &f : S \to \mathbb{R} \\ &S = \left\{ \boldsymbol{x} : \boldsymbol{x} \in \mathbb{R}^N, \boldsymbol{L} \le \boldsymbol{x} \le \boldsymbol{U} \right\} \end{aligned} \tag{1}$$

where f is the CF, N is the number of optimization variables, and $\boldsymbol{L}$ and $\boldsymbol{U}$ are vectors of lower and upper bounds imposed on these variables. The outline of the DESAPR is given by Algorithm 1.

Algorithm 1: DESAPR outline.
1. Initialization.
2. Competition.
3. Selection of parameters.
4. Trial point generation.
5. Trial point evaluation.
6. Replacement of a point in the population.
7. Local search.
8. If termination condition is not met, go back to step 2.

The population consists of M individuals. It is initialized by dividing each of the N parameter ranges given by vectors $\boldsymbol{L}$ and $\boldsymbol{U}$ uniformly into M subintervals. For every variable the M subintervals are assigned randomly to M individuals. The value of a variable for an individual is then chosen by randomly selecting a point in the assigned subinterval.

We denote the available positions with $i = 0,1, \ldots, M-1$. The behavior of the algorithm is determined by the weight factor W, crossover probability P_X, and random step probability distribution width parameter η. A set of parameter values is assigned to every one of the M available positions. The values of parameters assigned to *i*-th position are

$$W_i = W_0 e^{-c_W i}$$
$$P_{X,i} = P_{X,0} e^{-c_{P_X} i}, \quad (2)$$
$$\eta_i = e^i - 1$$

Coefficients c_W and c_{P_X} are computed from the weight factors and crossover probabilities of positions 0 and *M*-1 which are user defined parameters of the algorithm.

$$c_W = (M-1)^{-1} \ln \frac{W_0}{W_{M-1}}$$
$$c_{P_X} = (M-1)^{-1} \ln \frac{P_{X,0}}{P_{X,M-1}} \quad (3)$$

Every individual $\boldsymbol{x}_i$ is assigned to one of the *M* available positions. Let p_i and r_i denote the position and the rank of *i*-th individual. The rank of an individual is determined by ordering the individuals according to the CF value $f_i = f(x_i)$ and assigning ranks from M-1 (for the lowest CF value) to *0* (for the highest CF value). The goal of the competition in step 2 of Algorithm 1 is to align the rank of the individuals in the population with their positions. For this purpose two individuals are randomly selected from the population. Let *i* and *j* denote their indices. They exchange positions if $r_j > r_i$ and $p_j < p_i$. This forces individuals with high rank (low CF value) to move to high positions.

In step 3 of Algorithm 1 an individual is selected randomly with probability $P_{S,i}$.

$$P_{S,i} = \frac{e^{r_i}}{\sum_{i=0}^{M-1} e^{r_i}} \quad (4)$$

Let *k* denote the position of the selected individual. The weight factor (W_k), the crossover probability ($P_{X,k}$), and the range parameter (η_k) values assigned to this position are used in steps 4-7 of Algorithm 1. Individuals with high rank are selected with higher probability. Because higher ranking individuals tend to occupy higher positions, parameter values corresponding to higher positions are often used (but not always).

To simplify the notation the search space is transformed so that the components of vectors (i.e. individuals) lie within [0,1], where 0 and 1 correspond to the lower and the upper bound, respectively.

In step 4 of Algorithm 1 a trial point is generated using a modified DE operator [12] and polynomial mutation [13]. First a parent (***x***) and three additional distinct individuals (***u***, ***v***, and ***w***) are selected. The DE operator is applied component wise with probability $P_{X,k}$ resulting in point ***y***' with components

$$y_i' = \begin{cases} u_i + W_k (v_i - w_i) & U(0,1) \le P_{X,k} \\ x_i & \text{otherwise} \end{cases}. \quad (5)$$

If ***y***' violates the bounds the components that are outside the bounds (i.e. $y_1' \notin [0,1]$) are corrected resulting in point ***y*** with components defined as

$$y_i = \begin{cases} y_i' & 0 \le y_i' \le 1 \\ x_i + U(0,1) \cdot (1 - x_i) & y_i' > 1 \\ x_i - U(0,1) \cdot x_i & y_i' < 0 \end{cases}. \quad (6)$$

Finally, polynomial mutation is applied to ***y*** component wise. For every component a random number $\alpha_i = U(0,1)$ is generated. The trial point ***z*** is then computed as

$$z_i = y_i + \begin{cases} 1 - \left[2 - 2\alpha_i + (2\alpha_i - 1) y_i^{\eta_k + 1}\right]^{1/(\eta_k+1)} & \alpha_i > 0.5 \\ \left[2\alpha_i + (1 - 2\alpha_i)(1 - y_i)^{\eta_k + 1}\right]^{1/(\eta_k+1)} - 1 & \text{otherwise} \end{cases} \quad (7)$$

Let f_z denote the CF value corresponding to the trial point ***z***. The population along with the trial point is ordered according to the CF value. Rank 0 is assigned to the point with the highest CF value. Let r_z and r_x denote the ranks of the trial point and the parent, respectively. The trial point is accepted into the population (i.e. replaces the parent point ***x*** in step 6 of Algorithm 1) with probability

$$P = \min\left(1, e^{\frac{(r_z - r_x)k}{M-k}}\right) \quad (8)$$

The acceptance criterion resembles the original Metropolis criterion [7] in the sense that higher ranking trial points are accepted with higher probability. A trial point ranking higher than the parent point is always accepted.

Finally, in step 7 of Algorithm 1 a simple local search strategy is performed if the trial point is accepted, the parent point is the best point in the population, or with some small probability P_L (set to 0.05). Local search uses one of the points in the population as the origin and two additional points for computing a search direction (***d***). All three points are chosen randomly. Two additional points are evaluated along direction ***d*** and a quadratic model of the CF is computed. This model is minimized and the resulting point evaluated. The evaluated point with the lowest cost function value is the result of

the local search. The resulting point replaces the parent point if its CF value is lower. The complete details of the local search can be found in [14].

3 Parallel implementation

Suppose one has *m* parallel processors available. Assuming most of the computational time is spent for evaluating the trial point and for local search, these two tasks are outsourced to parallel processors in an asynchronous manner. The main process (master) runs the following algorithm:

Algorithm 2: asynchronous parallel optimization
1. Initialization.
2. If no processor is idle go to step 5.
3. Perform steps 2-4 of Algorithm 1 (generate a trial point).
   Send it to an idle processor (*p*) for evaluation.
   Remember the parent point (*x*) and the selected parameters position (*k*) for that processor.
4. If there are idle processors left return to step3.
5. Wait until one of the processors (*p*) finishes its task. Collect the results.
6. If *p* was performing global search point evaluation.
   Perform step 6 of Algorithm 1 (point replacement) using the parameters corresponding to position *k* that was stored for *p*.
   If required, start a local search (step 7 of Algorithm 1) on processor *p*.
   If *p* was performing local search.
   Replace the parent point of *p* if local search found a better point.
7. If termination condition is not met, go back to step 2.

Algorithm 2 performs multiple passes of Algorithm 1 in parallel and in this way accelerates the evolution of the population.

4 Performance on mathematical test functions

DESAPR was implemented within the framework of the PyOPUS library [15]. The performance of DESAPR was compared to that of PSADE, DE, SA, and JADE [18] on 13 test functions from [14]. For the sake of comparison, 30 optimization runs were performed for every function. We will later use the presented method for analog circuit sizing, where CF evaluations can take several seconds. Therefore we impose a CF evaluation budget of 100000 function evaluations per run to maintain reasonable optimization run times.

For DESAPR we used fixed parameter values in all experiments: $M=20$, $W_0=0.9$, $W_{M-1}=0.9$, $PX_0=0.9$, $PX_{M-1}=0.1$. We made no attempt to fine tune the parameter values to any specific problem. It is very time consuming especially for real world problems, where every CF evaluation can take considerable amount of time. The values were chosen based on our experience with evolutionary algorithms. High weight factor for DE and low crossover probability tend to maintain population diversity longer, which is desirable since DESAPR uses very small population. Fine tuning the parameters and introducing parameter adaptation or evolution could lead to even better performance for our method and is also subject of our future research.

For the compared methods, the parameters were selected according to guidelines from the authors of the methods. For DE we used DE/rand/bin strategy with population size 100, weight factor 0.5 and crossover probability 0.9. SA used in our experiments uses only two parameters. We set the final temperature and random step range parameter to T_{min}=1e-10, R_{min}=1e-10. For PSADE we set population size to 20, T_{min}=1e-10, R_{min} =1e-10, τ_1 = 0.01 (local step), τ_2 =0.1 (parameter adaptation). For JADE we also followed the author suggestions. We used the version without the archive, as suggested by the authors for problems with low dimensionality (< 30). We used the population size of 100, the learning parameter c=0.1 and the percentage of points considered as the best in population p=5%.

The results are given in Table 1.

For every function we chose a target CF value f_{target}, that lies in the basin of attraction of the global minimum. Finding this solution means that global search was successful, and any local search procedure can be used to quickly find the exact minimum. Not all runs succeed in reaching f_{target}. We report the success rate and the average number (over successful runs) of CF evaluations (#CF) needed to reach f_{target}. The average final CF error (with respect to the true global minimum) after 100 000 CF evaluations is listed in the *error* column. The best value of #CF and *error* are written in boldface if there exist a statistically significant difference between the best and second best method.

No method was able to reach f_{target} for all functions in all runs. JADE and DESAPR outperformed the other methods so we will focus on them. Considering final CF value, JADE outperformed DESAPR on 8 functions, while DESAPR was better only on 2 functions. On 3 functions there was no statistically significant difference. When

Table 1: Performance comparison results for 30D mathematical test functions. The function value at the global minimum is denoted by *f**. The results of the best performing algorithm are written in boldface if there exist a statistically significant difference to the second best method.

Function	*f**	f_{target}	#CF	Success rate [%]	*error*	Algorithm
f_1 Sphere	0	10-10	39388	100	$9.74 * 10^{-17}$	DESAPR
			62347	100	$5.32 * 10^{-12}$	PSADE
			NA	0	$5.20 * 10^{-7}$	DE
			NA	0	$7.09 * 10^{-6}$	SA
			34000	100	**0.0**	JADE
f_2 Schwefel 2.22	0	0.1	**14477**	100	$5.19 * 10^{-7}$	DESAPR
			47562	100	$4.91 * 10^{-2}$	PSADE
			58954	100	$1.73 * 10^{-4}$	DE
			78691	76	$4.30 * 10^{-3}$	SA
			16020	100	**0.0**	JADE
f_3 Schwefel 1.2	0	15	37693	100	$7.11 * 10^{-3}$	DESAPR
			67121	100	0.811	PSADE
			NA	0	29.01	DE
			61051	100	$7.38 * 10^{-4}$	SA
			26334	100	$\mathbf{4.81 * 10^{-9}}$	JADE
f_4 Schwefel 2.21	0	0.1	**35228**	100	$\mathbf{4.07 * 10^{-5}}$	DESAPR
			71209	100	0.073	PSADE
			94510	36	$2.94 * 10^{-1}$	DE
			73522	100	$1.18 * 10^{-3}$	SA
			88247	63	$9.22 * 10^{-2}$	JADE
f_5 Rosenbrock	0	30	18919	100	16.52	DESAPR
			36599	100	21.46	PSADE
			57851	100	21.11	DE
			63210	70	92.07	SA
			17418	100	**4.28**	JADE
f_6 Step	0	0	11149	100	0	DESAPR
			16151	100	0	PSADE
			42566	100	0	DE
			61547	100	0	SA
			10862	100	0	JADE
f_7 Noisy quartic	0	0.02	30999	100	$7.84 * 10^{-13}$	DESAPR
			36211	100	$2.31 * 10^{-3}$	PSADE
			79544	57	$2.58 * 10^{-2}$	DE
			58044	73	$1.41 * 10^{-2}$	SA
			16225	100	$\mathbf{1.96 * 10^{-3}}$	JADE
f_8 Schwefel 2.26	-418.982887*30 = -12569.486618	-12569.45	**22049**	97	3.95	DESAPR
			36955	93	7.90	PSADE
			NA	0	$7.59 * 10^{3}$	DE
			NA	0	$7.11 * 10^{2}$	SA
			77722	97	3.95	JADE
f_9 Rastrigin	0	0.1	**30697**	100	$\mathbf{6.83 * 10^{-13}}$	DESAPR
			81588	100	$8.19 * 10^{-3}$	PSADE
			NA	0	144.23	DE
			NA	0	6.31	SA
			77644	100	$1.60 * 10^{-4}$	JADE
f_{10} Ackley	0	10^{-4}	31255	100	$2.27 * 10^{-7}$	DESAPR
			55982	100	$1.93 * 10^{-5}$	PSADE
			96542	83	$8.14 * 10^{-4}$	DE
			NA	0	0.71	SA
			27122	100	$\mathbf{4.44 * 10^{-16}}$	JADE
f_{11} Griewank	0	10^{-9}	42281	100	$1.37 * 10^{-13}$	DESAPR
			77545	100	$7.88 * 10^{-9}$	PSADE
			NA	0	$4.13 * 10^{-8}$	DE
			NA	0	$2.10 * 10^{-2}$	SA
			35385	100	$\mathbf{5.55 * 10^{-17}}$	JADE

f_{12} Penalty 1	0	10^{-10}	39953	100	$4.70 * 10^{-16}$	DESAPR
			52650	100	$3.31 * 10^{-16}$	PSADE
			NA	7	$1.71 * 10^{-9}$	DE
			NA	0	$4.94 * 10^{-8}$	SA
			32804	100	$\mathbf{3.77 * 10^{-32}}$	JADE
f_{13} Penalty 2	0	10^{-10}	43895	100	$1.65 * 10^{-14}$	DESAPR
			54261	100	$5.74 * 10^{-15}$	PSADE
			NA	0	$3.59 * 10^{-7}$	DE
			NA	0	$1.01 * 10^{-6}$	SA
			34960	100	$4.39 * 10^{-30}$	JADE

comparing the speed, JADE was faster on 7 functions, while DESAPR was better on 4. JADE displays a good fine tuning capabilities and fast convergence on unimodal and well behaved functions. However on the most difficult f_8 and f_9, that have many local minima, DESAPR was significantly better than JADE, regarding both the speed and the final solution quality. JADE and DESAPR also exhibit similar success rate.

5 Performance on a real-world design problem

We tested DESAPR by sizing a Miller operational trans conductance amplifier (OTA) (Figure 1)[16] across a large number of corner points. The bias current was set to 100µ*A*. The performance measures and the design requirements are listed in Table 2.

Every corner point is a combination of temperature (0°C, 25 °C, and 100 °C), operating voltage (1.7V, 1.8V, and 2.0V), and CMOS corner model (average, worst power, worst speed, worst one, and worst zero). Let $\mathcal{C}$ denote the set of 45 corner points obtained in this manner. Every design requirement must be met for all 45 corner points from set $\mathcal{C}$. The CF is a function of the design parameters ($\boldsymbol{x}_D$). It is constructed as a sum of contributions (CF_i) corresponding to individual performance measures.

$$CF(\boldsymbol{x}_D) = \sum CF_i(\boldsymbol{x}_D) \tag{9}$$

Let $p_i(\boldsymbol{x}_D)$, g_i, and n_i denote the worst value of a performance measure across corners from set $\mathcal{C}_i \subseteq \mathcal{C}$, the corresponding goal, and the corresponding norm, respectively. A contribution of a performance measure to the CF for which an upper bound is imposed (design requirement of the form $p_i(\boldsymbol{x}_D) \leq g_i$) is computed as [17]

$$CF_i(\boldsymbol{x}_D) = \begin{cases} \dfrac{p_i(\boldsymbol{x}_D) - g_i}{n_i} & p_i(\boldsymbol{x}_D) \geq g_i \text{(the design requirement is not met)} \\ 10^{-6} \cdot \dfrac{p_i(\boldsymbol{x}_D) - g_i}{n_i} & \text{otherwise} \end{cases} \tag{10}$$

For performance measures with design requirements of the form $p_i(\boldsymbol{x}_D) \geq g_i$ the roles of $p_i(\boldsymbol{x}_D)$ and g_i in equation (10) are exchanged. By default the norm is equal to the goal. If the goal is 0, the norm is set to 1. An exception is the circuit area for which the norm is set to 100µm^2. Constructing the cost function in this manner penalizes designs that fail to satisfy the design requirements with a positive CF contribution while rewarding designs that exceed the design requirements with a small negative CF contribution.

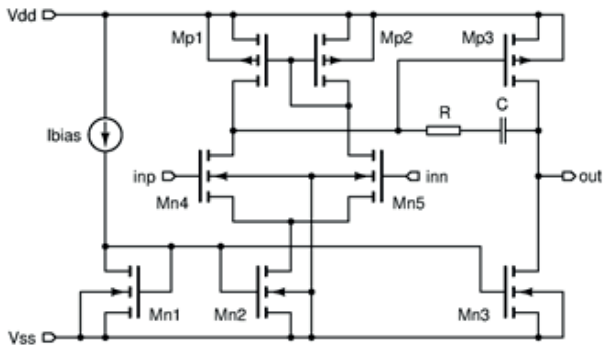


Figure 1: Miller OTA.

The optimizer tries to find the minimum of the CF by tuning the 13 design parameters (11 transistor channel widths and lengths, the resistance of R and the capacitance of C). The optimizer stops as soon as all design requirements are satisfied.

Table 2: Design requirements and circuit analyses from which the performance of the Miller OTA is evaluated.

Performance measure	Goal	Required analyses
Supply current [µA]	≤ 200	op
Vgs overdrive [V]	≥ 0.0	op
Vds overdrive [V]	≥ 0.1	op
Output swing [V]	≥ 1.2	dc
Gain [dB]	≥ 60	ac
UGBW [MHz]	≥ 30	ac
Phase margin [o]	≥ 50	ac
PSRR Vdd [dB]	≥ 65	ac, acvdd

PSRR Vss [dB]	≥ 65	ac, acvss
CMRR [dB]	≥ 90	ac, accom
Settling time (up) [ns]	≤ 100	tran
Settling time (down) [ns]	≤ 100	tran
Overshoot (up) [%]	≤ 10	tran
Overshoot (down) [%]	≤ 10	tran
Slew rate (up) [V/µs]	≥ 10	translew
Slew rate (down) [V/µs]	≥ 10	translew
Circuit area [µm^2]	≤ 1000	-

Because evaluating one point in the design space requires the circuit to be evaluated across all corner points from $\mathcal{C}$ a strategy for reducing the number of circuit evaluations was used. The circuit was optimized in multiple passes where the solution of *k*–th pass ($\boldsymbol{x}_{D,k}$) was used as the initial point for pass *k* +1. In the beginning of *k*–th pass all performance measures were evaluated across all corners from $\mathcal{C}$ at the initial point $\boldsymbol{x}_{D,k-1}$. Let $c_i \in \mathcal{C}$ denote the corner point where the *i*–th performance measure reached its worst value. If this worst performance did not satisfy the corresponding design requirement corner point c_i was added to $\mathcal{C}_i$. If no corner was added to any of the corner point subsets, no further passes were performed. If the resulting circuit satisfied all design requirements the run was deemed as successful. If, however, a corner point was added to any of the corner point subsets, the CF was minimized using an optimization algorithm starting from $\boldsymbol{x}_{D,k-1}$ which resulted in point $\boldsymbol{x}_{D,k}$. In most cases the final corner subsets contained only a handful of corners where the circuit exhibited its worst performance. Therefore the number of circuit evaluations was much lower compared to the brute force approach where every point in the design space is evaluated across all 45 corners.

Population based algorithms were started from a given initial point $\boldsymbol{x}_{D,k}$ by replacing one member of the initial population with $\boldsymbol{x}_{D,k}$. Optimization was stopped as soon as all design requirements were satisfied across the corresponding corner point sets $\mathcal{C}_i$ or if the number of evaluated circuits exceeded 50000. Four optimization algorithms were tested: differential evolution (DE), PSADE [14], DESAPR and JADE. SA was not included in this test because its performance on mathematical test functions considering the average final CF value was significantly worse than the performance of DE. Due to the stochastic nature of the tested algorithms the circuit was optimized 10 times on a cluster of 100 processors. For every algorithm the final CF value, the run time, and the number of performed circuit analyses was recorded. The minimal, the maximal, and the average results are listed in Table 3.

In terms of the final CF value DE and JADE failed to find a circuit satisfying all design requirements, despite many more CF evaluations. DESAPR and PSADE both succeeded in finding such a circuit in all 10 optimizations. The final CF value found by PSADE was slightly better, although this is not relevant because the optimization was stopped as soon as a circuit satisfying all design requirements was found and there was no real competition between the algorithms in terms of finding the best possible circuit. In terms of computational time DESAPR was on average two times faster than PSADE. The same can be said about the number of circuit analyses.

6 Conclusion

Finding the values of the circuit's design parameters is an important task in analog design automation. Global optimization algorithms are often selected for this task due to their ability to find the best possible circuit. Un-

Table 3: Performance comparison results for the Miller OTA. The best results (CF value and time) are written in boldface.

		CF	Time [s]	# op	# dc	# ac	# acvss	# acvdd	# accom	# tran	# translew
DE	Min	1.76e-02	7.42e+03	597390	132382	999350	221375	241473	261571	528424	264396
	Max	4.97e-01	2.95e+04	2358660	381896	5036254	2105616	2280094	2396099	2029708	1133701
	Avg	8.66e-02	1.96e+04	1453050.4	271884.2	3049903.2	1004943.8	1080426.9	1134624.7	1247288.0	670108.5
PSADE	Min	-3.99e-05	6.59e+02	34722	9180	45739	9180	12955	14976	39943	21951
	Max	-3.50e-05	3.59e+03	180440	42717	365833	112328	95558	119591	259453	124762
	Avg	-3.77e-05	1.92e+03	107708.4	24171.2	172718.2	48279.7	46172.2	55005.7	136731.1	66726.0
DESAPR	Min	-3.96e-05	4.08e+02	19222	5750	31718	6225	8090	8090	24758	13626
	Max	-3.47e-05	1.24e+03	69940	15284	117381	29909	35803	39533	75463	54541
	Avg	-3.70e-05	9.24e+02	46279.4	10833.1	71826.0	19131.2	20380.1	23858.7	53771.4	32792.2
JADE	Min	8.67E-03	2.55E+05	3806920	688720	10603220	5299470	5299470	5299470	5989420	3018020
	Max	5.74E-02	4.08E+05	8380226	1280426	27604226	11204410	11204410	11062510	11054026	5803526
	Avg	2.78E-02	3.06E+05	5.70e+06	9.55e+05	1.77e+07	7.56e+06	7.59e+06	7.51e+06	8.00e+06	4.23e+06

fortunately these algorithms are quite slow. We propose a modification of the PSADE global optimization algorithm that replaces the original Metropolis criterion of simulated annealing with a ranking based criterion. By replacing the acceptance criterion we hope to avoid situations where the algorithm gets caught in the neighborhood of a local minimum. The proposed algorithm (DESAPR) is highly parallelizable. We tested the algorithm on a set of mathematical test functions and on a real-world circuit design problem. The results confirmed, that DESAPR is an efficient and reliable optimizer for analog circuit sizing problem.

7 Acknowledgements

The research was co-funded by the Ministry of Education, Science, and Sport (Ministrstvo za Šolstvo, Znanost in Šport) of the Republic of Slovenia through the programme P2-0246 Algorithms and optimization methods in telecommunications.

8 References

1. JY Sun, QF Zhang, and EPK Tsang. DE/EDA: A new evolutionary algorithm for global optimization. Information Sciences, 169(3-4):249–262, 2005.
2. R Chelouah and P Siarry. A continuous genetic algorithm designed for the global optimization of multimodal functions. Journal of Heuristics, 6(2): 191–213, 2000.
3. Chuen Tse Kuah, Kuan Yew Wong, and Manoj Kumar Tiwari. Knowledge sharing assessment: An Ant Colony System based Data Envelopment Analysis approach. Expert Systems with Applications, 40(8):3137–3144, 2013.
4. Bolun Chen, Ling Chen, and Yixin Chen. Efficient ant colony optimization for image feature selection. Signal Processing, 93(6, SI):1566–1576, 2013.
5. J Kennedy and R Eberhart. Particle swarm optimization. IEEE International Conference on Neural Networks Proceedings, 1-6: 1942–1948, 1995.
6. JJ Liang, AK Qin, PN Suganthan, and S Baskar. Comprehensive learning particle swarm optimizer for global optimization of multimodal functions. IEEE Transactions on Evolutionary Computation, 10(3):281–295, 2006.
7. S Kirkpatrick, CD Gelatt, and MP Vecchi. Optimization by simulated annealing. Science, 220(4598):671–680, 1983.
8. D. R. Thompson and G. L. Bilbro. Sample-sort simulated annealing. IEEE Transactions on System, Man, and Cybernetics (B), 35(3):625–632, 2005.
9. David H. Wolpert and William G. Macready. No free lunch theorems for optimization. IEEE Transactions on Evolutionary Computation, 1(1):67–82, 1997.
10. A. Kaveh and S. Talatahari. Particle swarm optimizer, ant colony strategy and harmony search scheme hybridized for optimization of truss structures. Computers & Structures, 87(5-6):267–283, 2009.
11. Ali Riza Yildiz. A novel hybrid immune algorithm for global optimization in design and manufacturing. Robotics and Computer-Integrated Manufacturing, 25(2):261–270, 2009.
12. R Storn and K Price. Differential evolution - A simple and efficient heuristic for global optimization over continuous spaces. Journal of Global Optimization, 11(4):341–359, 1997.
13. M Hamdan. A dynamic polynomial mutation for evolutionary multi-objective optimization algorithms. International Journal on Artificial Intelligence Tools, 20(1):209–219, 2011.
14. Jernej Olenšek, Tadej Tuma, Janez Puhan, and Árpád Bűrmen. A new asynchronous parallel global optimization method based on simulated annealing and differential evolution. Applied Soft Computing, 11(1):1481–1489, 2011.
15. "PyOPUS - Circuit Simulation and Optimization", available at http://fides.fe.uni-lj.si/pyopus/, 2015.
16. R.J. Baker, CMOS Circuit Design, Layout, and Simulation, Wiley-IEEE Press, Hoboken (NJ), 2007.
17. Á Bűrmen, D Strle, F Bratkovič, J Puhan, I Fajfar, T Tuma. Automated robust design and optimization of integrated circuits by means of penalty functions. AEU-International journal of electronics and communications 57 (1), 47-56, 2003.
18. Jingqiao Zhang and Arthur C. Sanderson. JADE: Adaptive Differential Evolution with Optional External Archive. IEEE Transactions on evolutionary computation, 13 (5), 945-958, october 2009.

Arrived: 18. 12. 2015
Accepted: 13. 06. 2016

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 2(2016), 65 – 73

Real Time Implementation of PI and PID Controlled Cascaded H-Bridge Eleven Level Inverter using SPWM

M. S. Sivagamasundari, P. Melba Mary

V V College of Engineering, Department of EEE, Tisaiyanvilai, Tamil Nadu, India

Abstract: Multilevel inverters are nowadays widely used in high-power and high-voltage applications. A multilevel inverter synthesizes a large number of levels to get the desired output voltage levels and they have lot of merits such as improved output waveform, smaller passive filter size, lower Electro Magnetic Interference and reduced harmonics. However, multilevel inverters also have some disadvantages such as increased number of components, voltage-balancing problem and higher switching losses. This paper presents a PI and PID Controlled Cascaded H-bridge eleven level inverter based sinusoidal pulse width modulation control technique suitable for improved power quality applications. The main objective of reducing the THD of output of the chosen eleven level cascaded inverter under set point tracking as well as steady-state with fast transient response are proposed from control point of view. Simulation results have been discussed that the cascaded H-bridge eleven level inverter performs perfectly in connection with PI or PID. A comparative analysis of these two different controllers is revealed. Harmonic spectrum and output voltage and current waveforms have been obtained to validate the role of controllers. Experimental results are presented to confirm the simulation results.

Keywords: Multilevel inverter; Cascaded H-Bridge multilevel inverter; Total Harmonic Distortion; Sinusoidal pulse width modulation; PI Controller; PID Controller

Implementacija PI in PID kaskadnega H-mostičnega enajstopenjskega inverterja v realnem času z uporabo SPWM

Izvleček: Večstopenjski inverterji so danes široko uporabljeni v močnostnih in visoko napetostnih izdelkih. Za doseganje visokih napetosti združujejo veliko število napetostnih izhodov. Odlikujejo jih številne lastnosti, kot so izboljšan izhodni signal, manjši pasivni filter, nizka elektromagnetna interferenca in zmanjšanje harmonikov. Imajo pa tudi slabosti, kot so: veliko število elementov, uravnavanje napetosti in višje preklopne izgube. Članek predstavlja PI in PID krmiljen kaskadni H mostič enajstopenjskega inverterja na osnovi sinusne pasovno širinske modulacije. S stališča kontrolne so predstavljeni glavni vidiki znižanja THD izhoda pri sledenju točk, kakor tudi v stacionarnem stanju. Prikazana je primerjalna analiza dveh inverterjev, rezultati po so potrjeni tudi eksperimentalno.

Ključne besede: večstopenjski inverter; kaskadni H mostič; harmonsko popačenje; sinusna pulzni-širinska modulacija; PI kontroler; PID kontroler

* *Corresponding Author's e-mail: mssivagamasundari@gmail.com*

1 Introduction

Numerous industrial applications require electrical power in large quantities and of high quality and the demands are fast growing in recent years [1]. For various industrial drives applications, power-electronic inverters are becoming more popular [2]. A multilevel inverter is a power electronic device having several levels of dc voltages as inputs and produces a desired output voltage. Recently, multilevel power conversion technology has been developing very fast in the area of power electronics with good potential for future developments. As a result, the medium to high voltage range is the most attractive application of this technology [3]. A multilevel inverter not only enables the use of renewable energy sources, but also achieves high power ratings. A multilevel inverter system can be easily interfaced to renew-

able energy sources such as photovoltaic, wind, and fuel cells for high power applications.

The advantages of multilevel inverters is their smaller stepped output voltage, which results in lower switching losses, lower harmonic components, better electromagnetic compatibility, high voltage capability and high power quality [4]. For both low switching frequency and high switching frequency PWM, multilevel inverters are available with configurations. It must be noted that high switching frequency PWM means lower efficiency and higher switching loss and low switching frequency PWM means higher efficiency and lower switching loss [5].

The patent result search shown that multilevel inverter circuits have been around for more than 25 years. Today, in medium voltage levels with high-power applications, multilevel inverters are widely used [6]. The main field applications are in laminators, pumps, conveyors, compressors, fans, blowers, and mills. Later, there are several topologies have been developed for multilevel converters [7]. There are three different topologies proposed for multilevel inverters are as follows cascaded multi cell with separate dc sources, diode clamped (neutral-clamped) and capacitor-clamped (flying capacitors). These topologies have a different mechanism for providing the voltage level. The series H-bridge was the first topology introduced and more configurations have been developed for this topology [7]. Since this topology consists of series power conversion cells, the power and voltage levels may be scaled easily. The Series H-bridge topology was followed by the diode-clamped converter that utilized a bank of series capacitors [8]. After few years, flying capacitor topology followed diode-clamped topology. This topology uses floating capacitors to clamp the voltage levels, instead of series connected capacitors [9]. H-bridge inverters do not require either flying capacitor or clamping diode inverters because they have isolation transformers to isolate the voltage source.

Moreover, more than enough modulation techniques and control models have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others [10], [11]. In this paper, in order to generate the switching signals of the power converter a special sinusoidal pulse-width modulation (SPWM) technique was implemented. Some requirements must be satisfied when shoot through states are generated, for instance, shoot-through states have to be uniformly distributed during the whole output voltage period with constant width and the average output voltage should remain unaffected. These features result in several merits, such as low ripple input current, low value of the passive elements, reduction in output voltage THD, and gaining of the desired boost factor[12].In addition, many multilevel converter focused on applications such as industrial medium-voltage motor drives [13], utility interface for renewable energy systems [14], flexible AC transmission system (FACTS) and traction drive systems [15], [16]. To improve the power quality in the distribution network , Shunt Active Power Filters using PI, PID and Fuzzy Logic Controller (FLC) for power line conditioners (PLC) have been proposed [17]. In order to maintain the output load voltage at the desired value to supply the power for a variety of loads with a minimum THD , a deadbeat-based proportional-integral (PI) controller using a battery cell as the primary energy source for a stand-alone single-phase voltage source inverter has been proposed [18].

In paper [19], in order to eliminate the Total Harmonic Distortion (THD) and improve the power factor, DSTATCOM drawn from a Non-Linear Diode Rectifier Load has been proposed. In this paper [20] , a nine stepped multilevel power inverter has been designed, which chooses a multi-PWM optimized using genetic algorithms (GA), and minimizing Total Harmonic Distortion (THD) of the first 50 harmonics to about 0% has been presented. In addition,[21] a 43-level asymmetric uniform step cascaded multilevel inverter (CMLI) has been introduced which consists of four H-bridges per phase, with different dc sources of values E, 2E, 7E and 11E and a mixed integer linear programming (MILP) optimization model was employed to determine the switching angles of the CMLI power switches which can minimize the values of any undesired harmonics.

A typical single-phase nine-level inverter chooses full-bridge configuration by using suitable sinusoidal modulation technique as the power circuits. The output voltage has nine levels: zero, positive (+Vdc,+2Vdc,+3Vdc,+4Vdc), and negative(–Vdc,-2Vdc,-3Vdc,-4Vdc) supply dc voltage (assuming that Vdc is the supply voltage). By using the carrier frequency and switching functions, the harmonic components of the output voltage are determined. Therefore, their reduction of harmonics is just restricted to a certain degree.

To overcome this drawback, this paper presents an eleven-level inverter whose output voltage can be obtained in eleven levels. The harmonic content can be reduced, as the number of output levels increases. THD reduction [22] can be considered from three different views namely: by considering new switching strategies, by designing alternative circuit topological structures and by proposing suitable control techniques. The third view, i.e. proposition of suitable control technique is an alternate solution for THD reduction is

discussed in this paper. In view of the inherent merits, Cascaded H-bridge inverter and SPWM control strategy are used in this work. This H-bridge inverter topology uses five reference signals to generate PWM signals for the switches.

In this paper, the performance of both PI and PID controllers are compared and analyzed to minimize total harmonic distortion in cascaded H-bridge eleven level inverter. Results confirm the effectiveness of the proposed controller. The experimental results are presented to confirm the simulation results and thus the proposed idea.

This paper has been arranged as follows. After the introduction in section 1, Section 2 gives an outline of cascaded h-bridge multilevel inverter topology. Then, the Cascaded H-bridge eleven level inverter with PI and PID controllers are explained in Section 3. The two sections 4 and 5 show the simulation and experimental results that validate the proper operation of the inverter. Conclusion and final remarks are made in Section 6.

2 Cascaded H-bridge eleven level Inverter topology

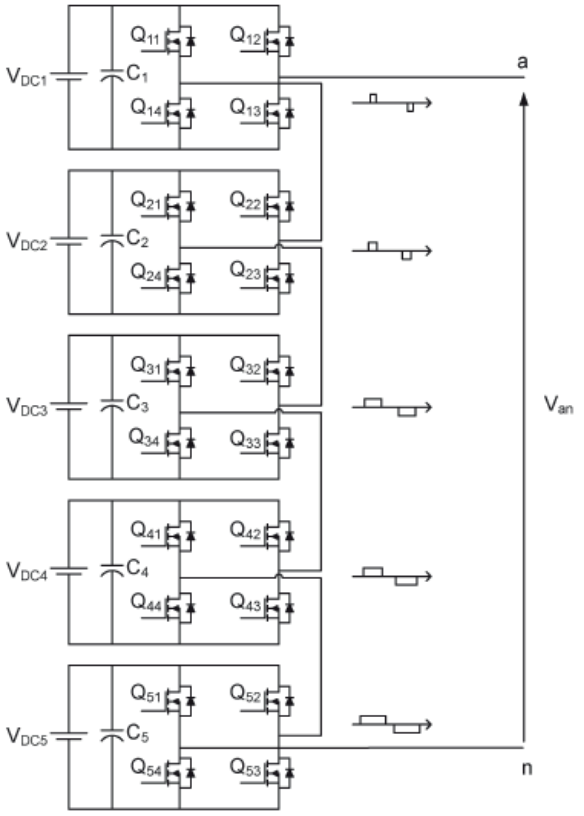


Figure 1: Schematic of a single-phase cascaded h-bridge eleven level inverter

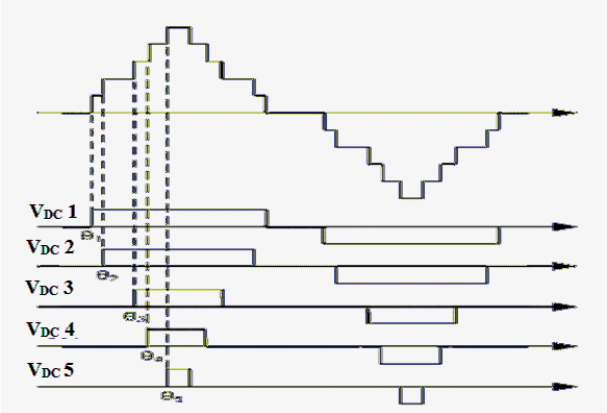


Figure 2: Output voltage waveform of a single-phase cascaded eleven level inverter

Fig. 1 and 2 show the Schematic diagram and Output voltage waveform of a single-phase cascaded h-bridge eleven level inverter. A single-phase 11-level inverter is formed by connecting five identical inverter modules in series. All five identical inverter modules having the same magnitude are fed by DC voltage sources. During the positive half cycle, the power electronic switches (Q11, Q13) are in the on-state, and the power electronic switches (Q12, Q14) are in the off-state. Likewise, during the negative half cycle the power electronic switches (Q11, Q13) are in the off-state, and the power electronic switches (Q12, Q14) are in the on-state and vice versa. The output voltage of the inverter has eleven voltage levels from -5 Vdc. to +5 Vdc. Each of the different full-bridge inverter ac output levels are connected in series such that the total voltage waveform is the sum of the inverter outputs.

The number of phase output voltage levels m in a cascaded h-bridge inverter is given by

$$m = 2n+1 \quad (1)$$

where n is the number of separate dc sources.

Each H-bridge unit produces a quasi-square waveform by phase-shifting the switching timings of its positive and negative phase legs.

3 Cascaded Multilevel Inverter(MLI) with PI and PID Controllers

A PI controller is built for MLI to examine the system behavior, The Cascaded H-Bridge Multilevel inverter with PI controller is shown in Fig. 3. The gate signals are generated using SPWM strategy. The isolated dc power sources are connected to the Cascaded H-bridge in-

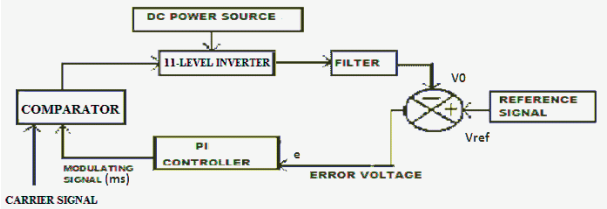


Figure 3: Cascaded MLI with PI Controller

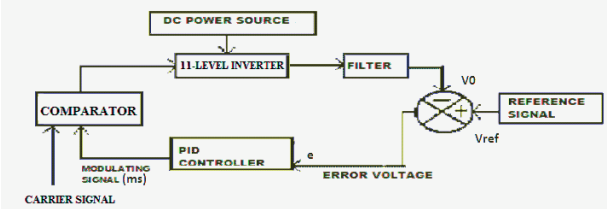


Figure 4: Cascaded MLI with PID Controller

verter. The eleven level output of the cascaded inverter is given to the load through LC filter to obtain sinusoidal output (Vo) and is compared with the reference voltage (Vref) to produce the error signal (e). The input to the PI controller is e. The output of the PI controller i.e the modulating signal (ms) is compared with carrier signal which is used to generate the gating pulses. Thus to get the required sinusoidal output voltage a voltage feedback loop is established. Hence, when the distortion in the output is more, the load is non linear. Using Ziegler – Nichols tuning technique PI controller settings Kp and Ki are designed in this work and the designed values of Kp and Ki are 0.1 and 0.01 respectively.

The Cascaded H-bridge Multilevel inverter with PID controller is shown in Fig. 4.The PID-controller is a linear combination of the P, I and D contributions carried out on the error. Sinusoidal pulse width modulation strategy generated the gate signals. The five isolated dc power sources are connected to the Cascaded H-bridge eleven level inverter. The output of the cascaded h-bridge eleven level inverter is given to the load through LC filter to obtain sinusoidal output (Vo) and is compared with the reference voltage (Vref) to produce the error signal (e). The input of the PID controller is error e. The output of the PID controller is multiplied with the unit reference signal to provide the required modulating signal (ms) and is used to produce the gating pulses in association with a carrier. Using Ziegler – Nichols tuning technique , PID controller settings Kp, Ki and Kd are designed in this work. The designed values of Kp, Ki and Kd are 0.1,0.01 and 0.001 respectively. The

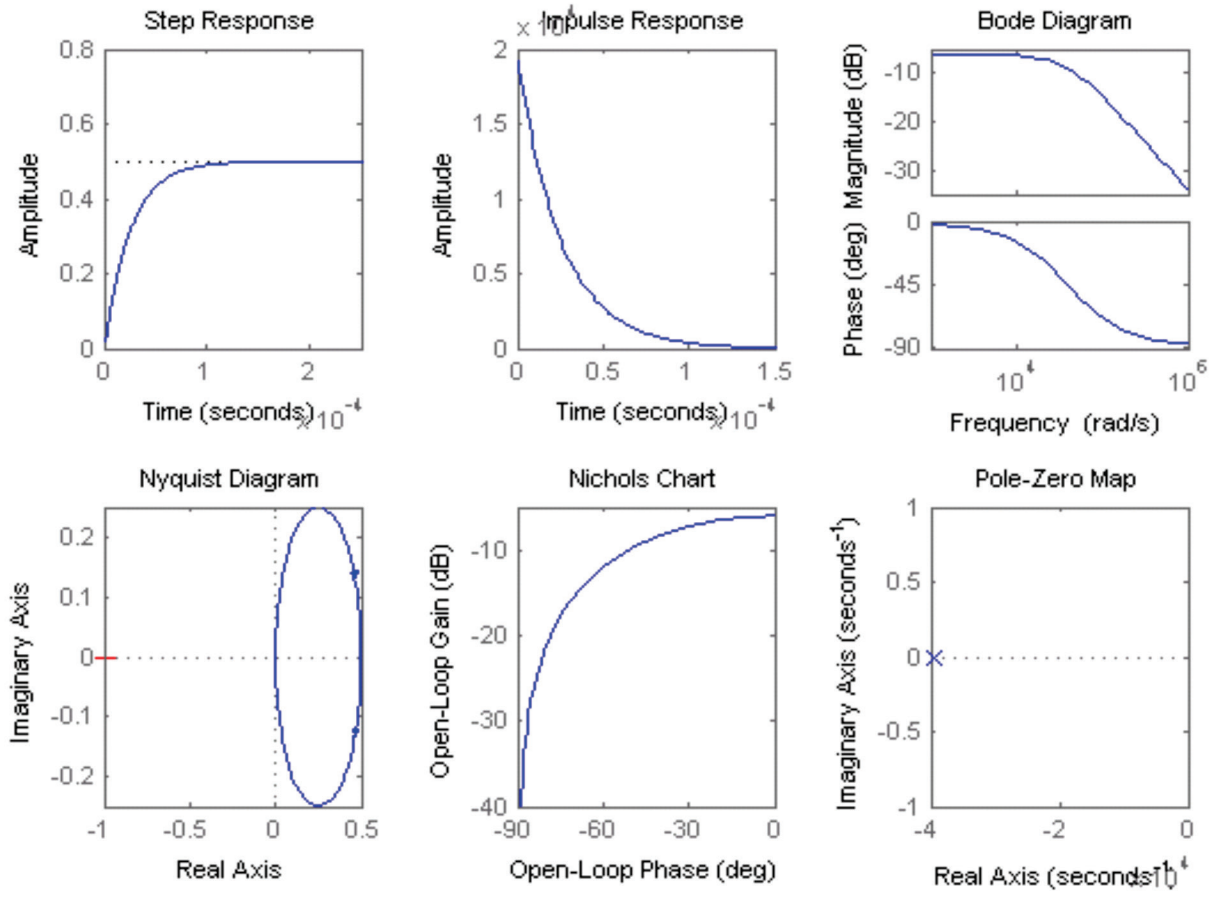


Figure 5: PID stability plots

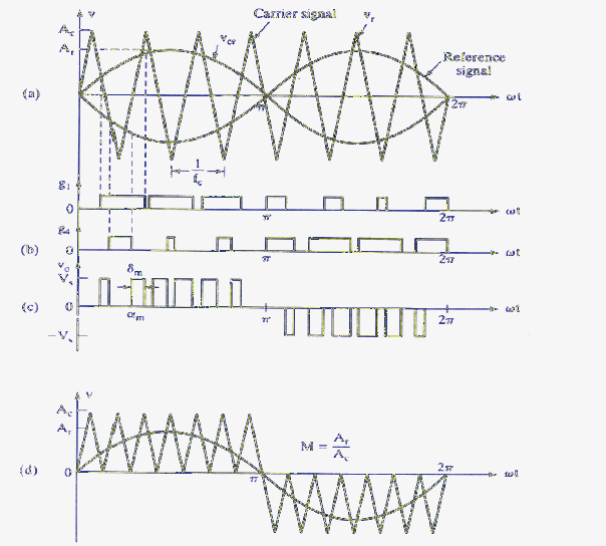


Figure 6: Sinusoidal Pulse width modulation a) Carrier and reference for bipolar modulation; b) pulses for bipolar modulation c) pulses for unipolar modulation d) carrier and reference for unipolar modulation

step response, bode plot, Nichols chart, nyquist, impulse response and pole-zero mapping are presented by carrying out the corresponding stability analysis shown in figure 5.

There are several switching control strategies have been proposed for Cascaded H-Bridge (CHB) inverters. High switching frequency PWM technique is widely used for eliminating harmful lower order harmonics in inverters. Several times the inverter switches are turned ON and OFF during every half cycle and by varying the pulse width output voltage is controlled in PWM control. This paper chooses the sinusoidal PWM control strategy because instead of maintaining the width of all pulses the same as in the case of multiple PWM, each pulse width is varied in proportion to the sine wave amplitude determined at the same pulse. The distortion is reduced importantly compared to multiple PWM. The gating pulses are shown in figure 6.

4 Simulation results

The performance of the proposed PI and PID controllers based cascaded H-bridge eleven level inverter with isolated dc sources is determined through MATLAB/ SIMULINK software. The elements and the parameters considered for simulation are presented in Table 1.

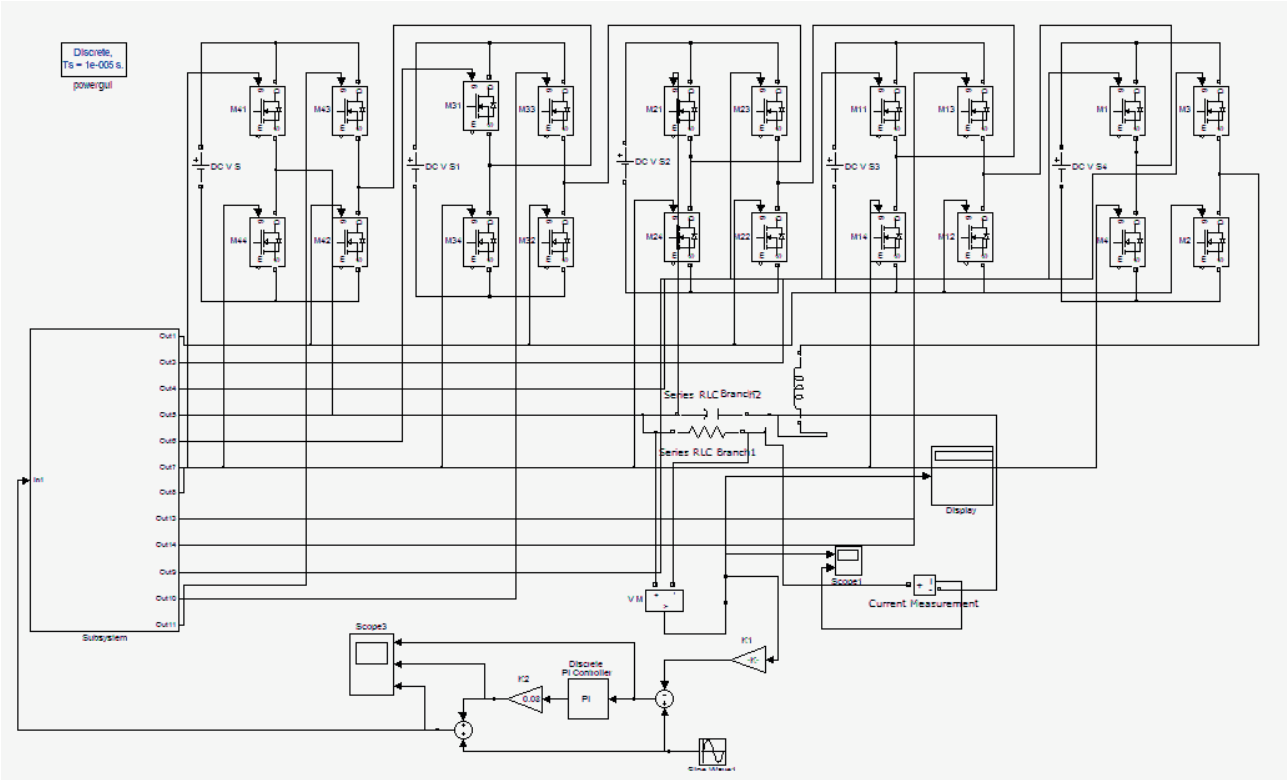


Figure 7: Simulink model of the Cascaded MLI with PI Controller

Table 1: Parameters of the Cascaded H-Bridge Inverter

Parameters	Values
No. of H-Bridge levels	5
No. of Switches	20
DC source voltage for individual H- bridge	34.8V
Fundamental frequency	50Hz
Load resistor	100 Ohm
Load Inductor	40mH

Case 1 : PI controller

The simulation model of cascaded h-bridge eleven level inverter topology using PI controller is shown in fig.7. The main power circuit consists of five H-bridges whose dc voltage is considered to be 34.8 V and the eleven level stepped output voltages are obtained and the harmonics are reduced. It also consists of PWM block and has parameters as amplitude, pulse width period and phase delay which is used to determine the shape of the output .Therefore the inverter efficiency is increased. The inverter must perform reliably and

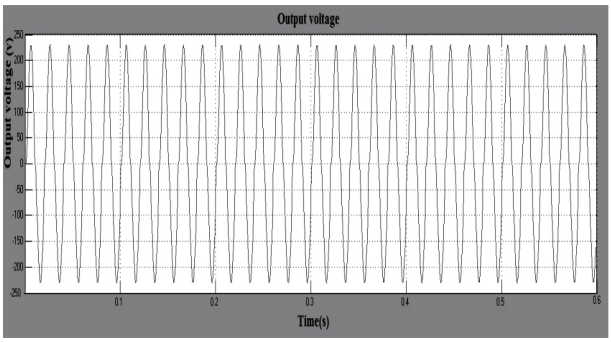


Figure 8: Load voltage waveform(PI Controller)

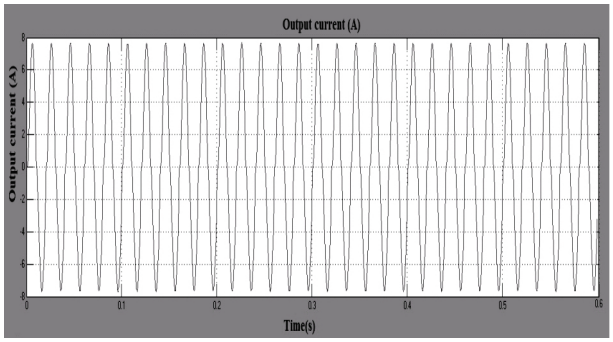


Figure9: Load current waveform(PI Controller)

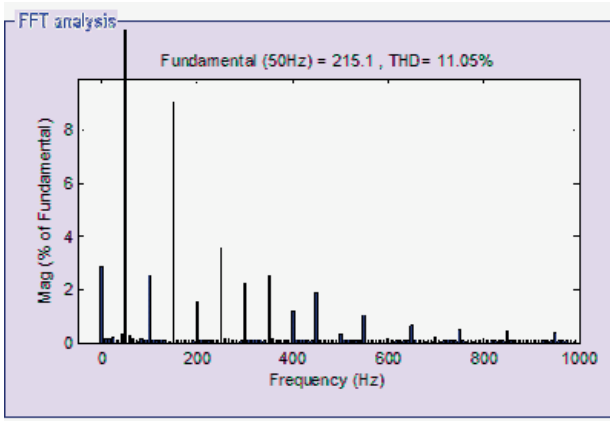


Figure10: Voltage THD

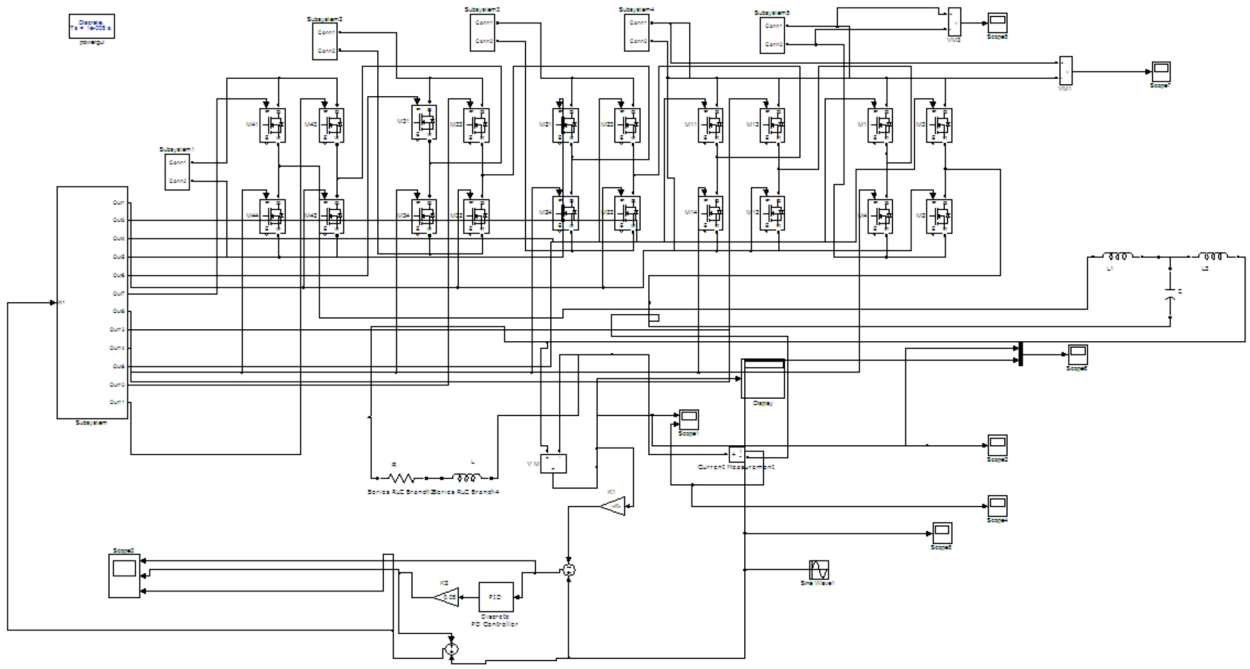


Figure 11: Simulink model of the Cascaded MLI with PID Controller

efficiently to supply a wide range of ac loads with the voltage and required power quality necessary for reliable and efficient load and system performance. The advantages of the proposed topology are high power high voltage handling capability, lower harmonics and lower switching loss. The output voltage and output current of cascaded h-bridge eleven level inverter has eleven levels. The inverter fundamental frequency is 50 Hz. The loads are connected across the cascaded H-bridge eleven level inverter.

The response of the MLI with PI controller is satisfactory and the load voltage and load current is shown in figure 8 and 9. The Total Harmonic Distortion waveform is shown in figure 10. It is observed from the results that the peak overshoot in the output voltage is 5.4 % and the total harmonic distortion is 11.05 %.

Case 2 : PID controller

The Simulink model of the Cascaded MLI with PID Controller is shown in figure 11. The response of the MLI with PID controller is also satisfactory and the load voltage and load current is shown in figure 12 and 13. The Total Harmonic Distortion waveform is shown in figure 14.

It is observed from the results that the peak overshoot in the output voltage is 4.4 % and the total harmonic distortion is 9.70 %. The performance of the controllers is tabulated in Table 2. Hence it is observed from the simulation results that the peak overshoot, settling time , THD are reduced in the output voltage and higher fundamental rms voltage using PID controller.

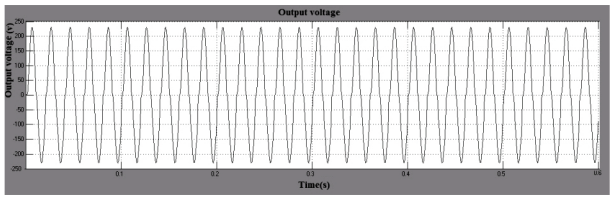


Figure 12: Load voltage waveform(PID Controller)

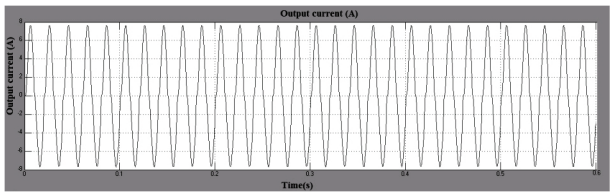


Figure 13: Load current waveform(PID Controller)

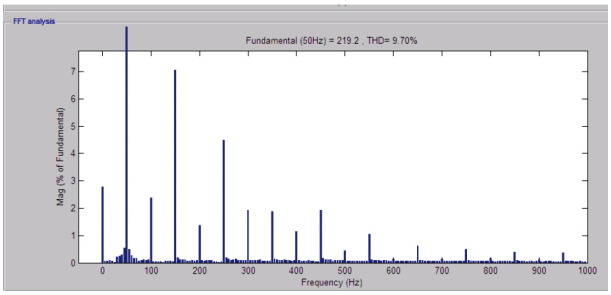


Figure 14: Voltage THD

Table 2: Comparison of Controller Performance

Controllers	Peak Overshoot	Settling Time	RMS fundamental voltage	THD%
PI	5.4	0.04	215.1	11.05
PID	4.4	0.01	219.2	9.70

5 Experimental results

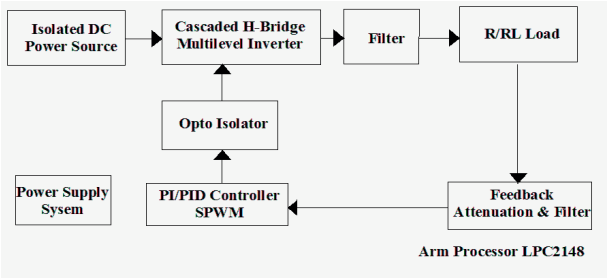


Figure 15: Experimental block diagram

The experimental block diagram of proposed Cascaded H-bridge inverter topology is shown in Fig. 15. This proposed block diagram consists of a multilevel DC/AC power inverter, Optocoupler, Arm processor, filter and a load. The isolated dc power sources are connected to the Cascaded H-bridge inverter. The output of the eleven level inverter is ac voltage which is connected to the load through filter and the load is considered as resistive and an inductive. PI and PID controllers are employed to minimize total harmonic distortion in cascaded H-bridge eleven level inverter.

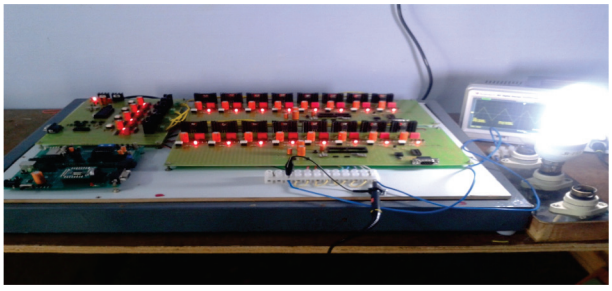


Figure 16: Structure of the experimental prototype

A single phase 0.3kW hardware prototype 11-level inverter as shown in Fig. 16 is developed. It consists of five full-bridge inverters and are connected in a series manner. The inverter uses 8-A, 500-V MOSFETs as the switching devices and the DC source voltage of each H-bridge inverter is selected to be 34.8V and is constant . The output frequency is assumed to be 50 Hz. Five transformers (0-24V, 2A) are used to power up the individual H- bridge inverters. Three transformers (6V-0-6V, 500mA) are used to power up the opto couplers.

The real time implementation of PI and PID controllers for eleven level inverter using LPC2148 Arm Processor is carried out in this work. Sinusoidal PWM strategy for the eleven level inverter is developed using MATLAB software. The PI and PID controllers generate the compensating signal to provide the required modulating signal for regulating the output voltage of this inverter.

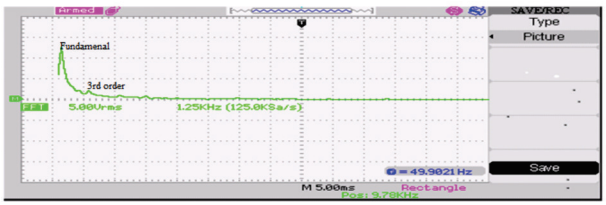


Figure 17: Harmonic spectrum of the inverter output voltage

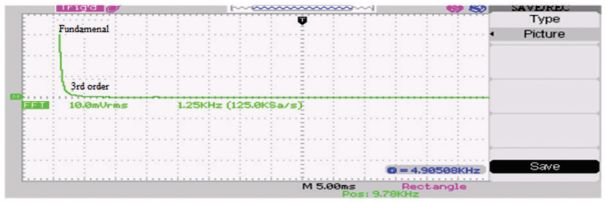


Figure 18: Harmonic spectrum of the inverter output current

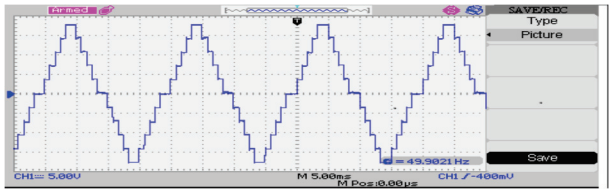


Figure 19: Output voltage waveform

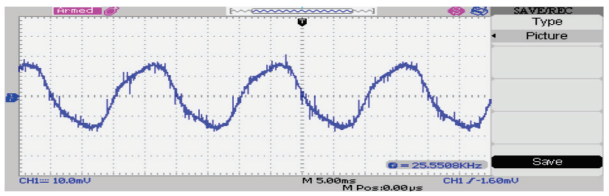


Figure 20: Output current waveform

Fig. 17 and 18 shows the harmonic spectrum of the inverter output voltage and output current . Fig. 19 shows the output voltage waveform. Fig. 20 shows the output current waveform. The elements and the parameters considered for implementation are presented in Table 3 for the cascaded h-bridge eleven level inverter topology.

Table 3: Experimental Parameters of the Cascaded H-Bridge Inverter

Parameters	Values
No. of H-Bridge levels	5
No. of Switches MOSFET IRF840 – 20Nos.	500V,8A
DC source voltage for individual H- bridge	34.8V/2A
Fundamental frequency	50Hz
R Load	47 Ohm
RL Load	47 Ohm,10mH
Opto Couplers MCT2E (20 Nos.)	30V,3A
Filter Capacitor	1000µF
Transformers(5 Nos.)	0-24V,2A
Transformers (3 Nos. for individual H- bridge)	6V-0-6V,500mA

With reference to table 4 a comparison of THD of the output voltage have been done. It is clearly shown that the results of simulation are closer to the experimental values.

Table 4: Comparison of THD of the output voltage

THD (%)		
Controllers	Experimental	Simulation
PI	11.01	11.05
PID	9.2	9.70

6 Conclusion

The real time implementation of PI and PID control strategies for single phase cascaded h-bridge eleven level inverter have been carried out and the results are compared and analyzed. From the obtained simulation results, it is found that PID performs better than PI controller since it provides output with relatively low harmonic distortion and higher fundamental rms output voltage. The PID controller yields a smaller overshoot in the output voltage, quick settling time, good dynamic response and lower total harmonic distortion than the PI controller for power quality applications. The measured value of total harmonic distortion of the inverter output voltage satisfies the IEEE-519 constraints.

7 References

1. J. Rodriguez, J. S. Lai and F. Z. Peng, "Multilevel inverters: Survey of topologies, controls, and applications," IEEE Trans. Ind. Elect., vol. 49, no. 4, pp. 724-738, Aug. 2002.
2. Beser, E.; Camur, S.; Arifoglu, B.; Beser, E.K. , " Design and application of a novel structure and topology for multilevel inverter," in Proc. IEEE SPEEDAM, Tenerife, Spain, 2008, pp. 969 – 974.
3. R.H. Baker, "High-Voltage Converter Circuit," U.S. Patent Number 4,203,151, May 1980.
4. S. Mekhilef and M. N. Abdul Kadir "Voltage control of three-stage hybrid multilevel inverter using vector transformation" IEEE Trans. Power Electron.,vol.25,no.10,pp 2599-2606, Oct. 2010.
5. L.M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel PWM Methods at Low Modulation Indices," IEEE Trans. Power Electron.,vol. 15, no. 4, pp. 719-725, July 2000.
6. M. N. A. Kadir S. Mekhilef, and H. W. Ping "Voltage vector control of a hybrid three-stage eighteen-level inverter by vector decomposition" IET Trans. Power Electron.,vol.3,no. 4, pp.601- 611, 2010.
7. E. Babaei, M. T. Haque, and S. H. Hosseini, "A novel structure for multilevel converters," in Proc. ICEMS, 2005, vol. 2, pp. 1278–1283.
8. A.Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Applicat., vol. IA-17, no. 5, pp. 518– 523, Sep./Oct 1981 .
9. T. A. Meynard and H. Foch, "Multilevel conversion: High voltage choppers and voltage-source inverters," in Proc. IEEE PESC, Toledo , Spain 1992, pp. 397– 403.
10. S. Mekhilef and M. N. Abdul Kadir "Novel vector control method for three-stage hybrid cascaded multilevel inverter" IEEE Trans. Ind. Elect., vol. 58, no. 4, pp. 1339-1449, May 2010.
11. S. Mekhilef, A. M. Omar and N. A. Rahim, "Modeling of three-phase uniform symmetrical sampling digital PWM for power converter" IEEE Trans. Ind. Electron.,vol. 54, no. 1, pp.427-432, Feb. 2007.
12. Carlos Roncero-Clemente, Oleksandr Husev, V. Miñambres-Marcos, Enrique Romero-Cadaval, Serhii Stepenko, Dmitri Vinnikov, "Tracking of MPP for three-level neutral-point-clamped qZ-source off-grid inverter in solar applications". Informacije MIDEM. Journal of Microelectronics, Electronics Components and Materials. ISSN 0352-9045, Vol.43, No. 4, 2013, pp. 212-221. December 2013.
13. M. F. Aiello, P. W. Hammond, and M. Rastogi, "Modular Multilevel Adjustable Supply with Parallel Connected Active Inputs," U.S. Patent 6301 130,Oct. 2001.
14. L. M. Tolbert, F. Z. Peng, "Multilevel converters as a utility interface for renewable energy systems," in Proc. IEEE Power Eng. Soc. Summer Meeting 2000 ,vol. 2 , pp. 1271-1274.
15. L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel Inverters for Electric Vehicle Applications," IEEE Workshop on Power Electronics in Transportation, Dearborn, Michigan, 1998, , pp. 1424-1431.
16. M. N. Abdul Kadir S. Mekhilef and H. W. Ping, "Dual vector control strategy for a three –stage hybrid cascaded multilevel inverter," Journal of power Electronic, vol.10, no.2,pp.155-164,2010.
17. P. Karuppanan and Kamalakanta mahapatra, '' PI ,PID and Fuzzy logic controlled cascaded voltage source inverter based active filter for phone line conditioners", Wseas transactions on power systems,vol.6 ,no.4 ,pp 100-109, Oct 2011.
18. Towleong Tiang and Dahamen Ishak, ''Modelling and simulation of dead beat based PI controller in a single phase H-bridge inverter for standalone applications",Turkish journal of electrical engineering and computer sciences , 22, pp 43-56,2014.
19. B. Suryajitt, G. Sudhakar," Power Quality Improvement Using Cascaded H-Bridge Multilevel Inverter Based Dstatcom" Int. Journal of Engineering Research and Applications, ISSN : 2248-9622, Vol. 4, Issue 11(Version 3), pp. 31-37, November 2014.
20. Jorge Luis Diaz Rodriguez, Luis David Pabon, Aldo Pardo Garcia," THD improvement of a PWM cascade multilevel power inverters using genetic algorithms as optimization method" WSEAS TRANSACTIONS on POWER SYSTEMS, Volume 10, pp 46-54, 2015.
21. Mahmoud El-Bakry," A 43-level filterless CMLI with very low harmonics values" Journal of Electrical Systems and Information Technology, Volume 1, Issue 3, 2015.
22. B. Shanthi and S.P. Natarajan, ''FPGA based fuzzy logic control for single phase multilevel inverter ,"International Journal of Computer Applications , vol.9 ,no.3 ,pp 10-18, Nov 2010.

8 Acknowledgement

The authors are thankful to the Institution of Engineers (India), Kolkata for the financial grant for carrying out the research work in real time application.

Arrived: 09. 08. 2015
Accepted: 10. 06. 2016

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 2(2016), 74 – 79

0.18 µm CMOS power amplifier architecture comparison for a wideband Doherty configuration

Aleksandr Vasjanov, Vaidotas Barzdenas

Department of Computer Engineering, Vilnius Gediminas Technical University, Vilnius, Lithuania

Abstract: This paper presents a comparison between a classical and a self-biased two stage CMOS power amplifier (PA) suitable for a wideband Doherty (DPA) configuration. Both PAs are fully differential and have been implemented in IBM 7RF 0.18 µm CMOS process and are supplied from 1.8 V. Classical PA input impedance is shown to be matched from 1.6 GHz to 2.7 GHz @ S_{11} = -10 dB with external matching components. Self-biased PA his matched from 800 MHz to 1.75 GHz without any additional matching components and the bandwidth can be further increased to 2.15 GHz. Self-biased PA average PAE is 25.3 % which is 4.2 % higher than that of the classic PA. Both power amplifiers have an average output power of 10.5 dBm. The latter results show, that a self-biased PA architecture has more potential to be implemented in a wideband DPA configuration, compared to the classic PA arrangement. The active area for both on-chip PAs is 800 µm^2, whereas the full IC chip size is 1.5 mm^2. The dual PA ASIC has been designed to be enclosed in a 20-pin QFN package.

Keywords: CMOS; Power amplifier; Self-biased; Doherty; Wideband

Primerjava 0.18 µm CMOS arhitektur močnostnih ojačevalnikov za širokopasovno Doherty konfiguracijo

Izvleček: Članek predstavlja primerjavo med klasičnim in samonastavljivim dvostopenjskim CMOS močnostnim ojačevalnikom (PA) za širokopasovno Doherty (DPA) konfiguracijo. Oba sta popolnoma diferencialna in izvedena v 0.18 µm IBM 7RF CMOS tehnologiji. Napajana sta z 1.8 V. Vhodna impedanca klasičnega ojačevalnika se ujema od 1.6 GHz do 2.7 GHz @S_{11} = -10 dB z zunanjimi ujemalnimi komponentami. Samonastavljivi ojačevalnik je ustrezen od 800 MHz do 1.7 GHz brez dodatnih zunanjih komponent. Njegovna pasovna širina se lahko razširi do 2.15 GHz. Povprečen PAE je 25.3%, kar je 4.2% več kot pri klasičnem ojačevalniku. Oba ojačevalnika imata izhodno moč 10 dBm, kar nakazuje, da je samonastavljivi ojačevalnik bolj primeren za širokopasovne DPA konfiguracije. Površina obeh je 800 µm^2, pri velikosti čipa 1.5 mm^2. Dvojni PA ASIC je bil dimenzioniran, da ustreza 20 pinskem QFN ohišju.

Ključne besede: CMOS; močnostni ojačevalnik; samonastavljiv; Doherty; široki pas

** Corresponding Author's e-mail: aleksandr.vasjanov@vgtu.lt*

1 Introduction

Over the past decade, the number of papers published on power amplifier (PA) research has been increasing exponentially. Since then different PA efficiency enhancement techniques and architectures have been proposed and the Doherty power amplifier (DPA) arrangement is one of the most promising [1]. The vast majority of published papers present single-ended or differential Doherty power amplifiers designed using a classical PA topology. Only classical, cascode PAs with either common inductors, slab inductors or baluns implemented in a DPA have been researched [3-14]. This article presents a comparison between a classical two stage power amplifier and a self-biased PA approach both suitable to be implemented in a wideband DPA. This paper is arranged as follows: DPA design challenges and a performance comparison between the published DPAs are presented in the second chapter. The proposed classical and self-biased PA architectures are presented and thoroughly analyzed in the next chapter. Simulation results and full ASIC layout are presented in the following chapter. Finally conclusions are made and references are given.

2 Doherty power amplifier design challenges

Multiple power amplifier architectures have been published in research papers over the last decade, including classic, cascode, self-biased PA configurations employing different parameter improvement techniques such as feedback, feedforward or/and linearization circuits. One of the most promising advanced PA architecture – Doherty power amplifier (DPA) presented in Figure 1 – provides a combination of high linearity and sufficient PAE at input powers ranging from back-off power to P1dB. Although DPAs prove to be very efficient at a certain frequency, there are several drawbacks in the architecture which restrict performance over wide bandwidth. The first drawback is the bandwidth of the classical output impedance inverter, which enhances the DPA to utilize loadpull in order to achieve high efficiency. This has been addressed in [2] and it has been proven, that the proposed impedance inverter can be designed in such a way that has more than 83 % of fractional bandwidth. Another DPA drawback is the inevitable result nonlinear nature of the peak amplifier. The peak amplifier is typically biased in class *C* [15] and requires harmonic termination. A harmonic termination circuit is essentially a series *LC* circuit (resonator) connected as a shunt to the output of the peak amplifier. Consequently for a larger DPA bandwidth several switchable harmonic terminations may be used.

Table 1 summarizes published CMOS DPA parameters. The latter table reveals, that the scaling of CMOS process does not improve the main design criterion for the always power hungry PA – power added efficiency (PAE). According to Table 1 CMOS processes in the range from 0.18 µm to 0.13 µm provide the largest DPA efficiency. Moreover, the latter processes are have been around since 1999-2001, therefore the relation between the performance and price per chip area can be very attractive for DPA designers and researchers.

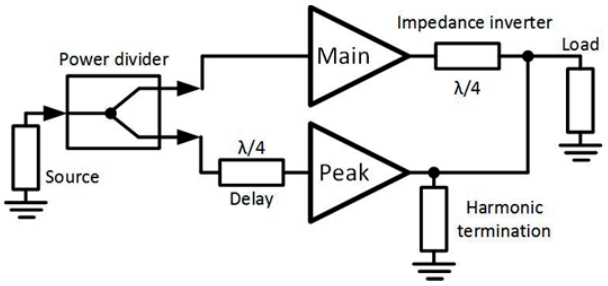


Figure 1: Classic Doherty power amplifier block diagram

3 Power amplifier architectures for wideband Doherty configuration

The simplified single-ended classic two-stage cascode PA is presented in Figure 2. The latter PA input and output stages are biased from internal sources for AB class operation. Cascoding in both stages has been chosen in order to reduce the influence of Miller effect and improve both isolation and stability. Gain control has been implemented to toggle the cascode transistors in both stages through on-chip buffers.

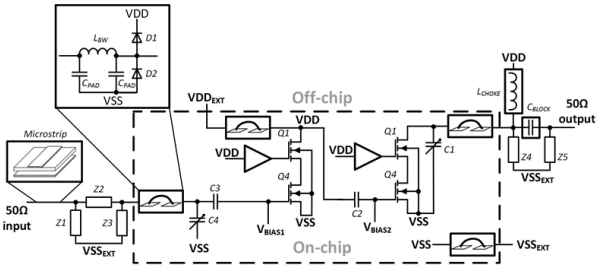


Figure 2: Classic two stage single ended power amplifier simplified schematic

Table 1: CMOS Doherty power amplifier performance comparison

Ref.	Process	VDD, V	Frequency, GHz	P1dB, dBm	Overall PAE, %	Power back-off, dB
3	0.18 µm CMOS	3.7	3.5	24.4	36.1	6.0
4	0.18 µm CMOS	3.3	2.4	29.5	22.0	5.0
5	0.18 µm CMOS	3.0	2.4	22.6	31.0	7.0
6	0.18 µm CMOS	-	0.89	25.0	43.6	5.0
7	0.13 µm CMOS	3.3	2.4	31.9	30.1	5.0
8	0.13 µm CMOS	3.3	1.7	31.7	33.0	5.0
9	0.13 µm CMOS	3.0	2.4	22.0	45.0	7.0
10	90 nm CMOS	3.3	2.4	30.0	24.0	5.0
11	90 nm CMOS	2.4	2.4	24.8	26.0	5.0
12	65 nm CMOS	5.5	2.535	23.4	25.0	8.5
13	65 nm CMOS	3.3	2.4	33.5	20.0	5.0
14	65 nm CMOS	2.5	2.4	23.4	24.7	7.0

The simplified single-ended self-biased two stage PA is presented in Figure 3. The main difference between the latter PA and the classic architecture is the type and the biasing of the first stage. The first stage is inverter based and is biased at *VDD*/2 via diodes Q_2 and Q_5. In order to widen input S_{11} response, R_1 and C_2 components should be designed with caution. One of the main drawbacks of an inverter based input stage is that the input saturates at 5 dB to 10 dB lower input powers than the classic input stage. The output stage is biased for an *AB* class operation from an internal source.

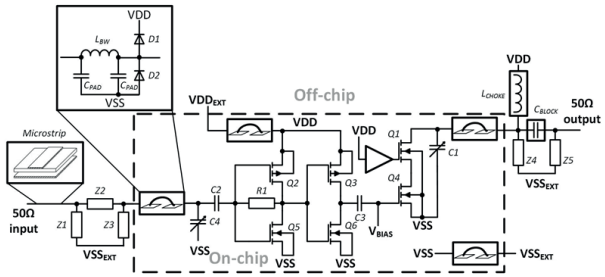


Figure 3: Self-biased two stage single-ended power amplifier simplified schematic

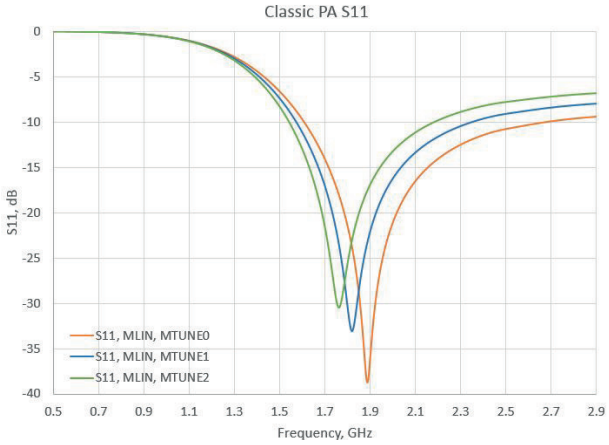
In both PA architectures, capacitors C_4 and C_2 act as DC blocks and also influence the overall PA stability. Digital varactors C_1 and C_4 are used to tune input and output impedances in order to achieve optimal power and gain matching respectively. In order to get more accurate impedance matching results, bondwire models with ESD protection diodes and microstrip feed lines (as *S*-parameter *nPort* elements) are also introduced. Both input (Z_1, Z_2, Z_3) and output (Z_4, Z_5, C_{BLOCK} and L_{CHOKE}) impedance matching networks are placed off-chip due to the lack of chip area. External component package parasitics were also taken into account during calculations.

4 Simulation results

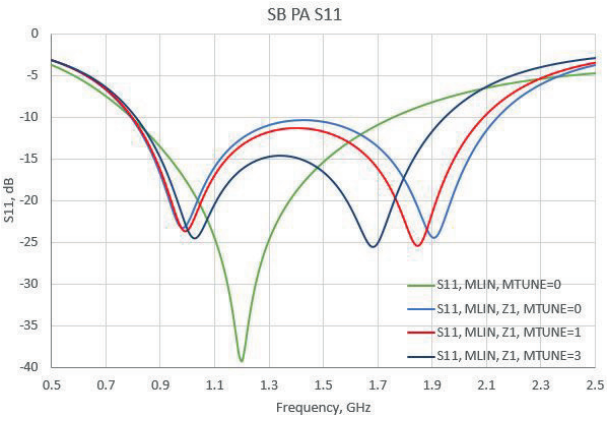
This chapter presents simulation results for the proposed PAs. It should be noticed, that the presented results correspond to the fully differential power amplifier configurations, whereas Figure 2 and Figure 3 present only the simplified single-ended schematics. Both PAs operate at 1.8 V supply voltage and were designed to provide a power gain of 20 dB and output power of 11 dBm to a 50 Ω load.

Input impedance matching results for both PA architectures are presented in Figure 4. Figure 4 (a) presents S_{11} response for the classic PA configuration with an external impedance matching network Z_2 and Z_3. External matching component Z_2 has been designed to be a 1.5 pF capacitor and Z_3 – a 4.2 nH shunt inductor. The matched frequency can be altered either by changing internal C_4 capacitor control *MTUNE* value or by varying the off-chip shunt inductor Z_3. In both cases the S_{11} notch response bandwidth does not top 1.1 GHz at S_{11} = -10 dB.

In comparison, Figure 4 (b) presents input impedance matching results for the self-biased PA architecture. Taking into account package parasitics and a cautious R_1 (ref. Figure 3) resistor value tuning leads a naturally matched bandwidth of 1 GHz without any additional matching components ("S11, MLIN, MTUNE = 0" plot in Figure 4 (b)). The matching bandwidth can be further increased by introducing a series (Z_2 in Figure 3) 6.2 nH inductor and altering *MTUNE* value.



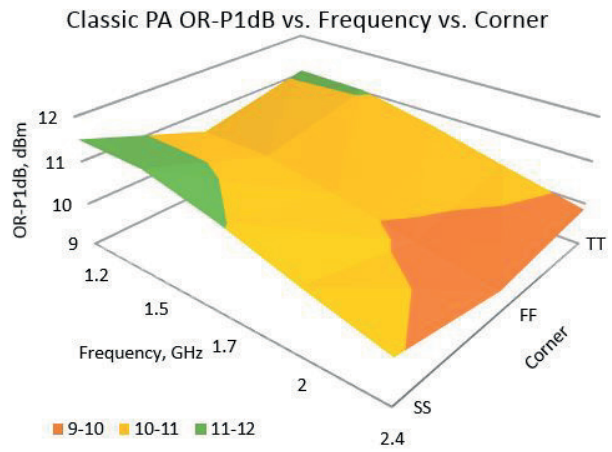
a



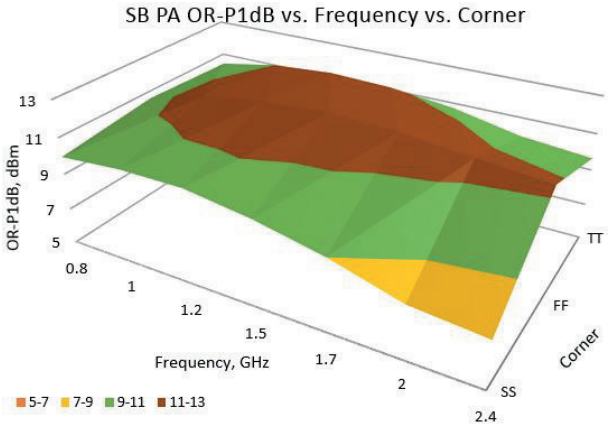
b

Figure 4: Classic PA (a) and self-biased PA (b) *S11* response control

Figure 5 presents output referred 1 dB compression point (P1dB) over frequencies and corners for both PA architectures. Both power amplifiers have been designed to output an average power of 10.5 dBm.



a

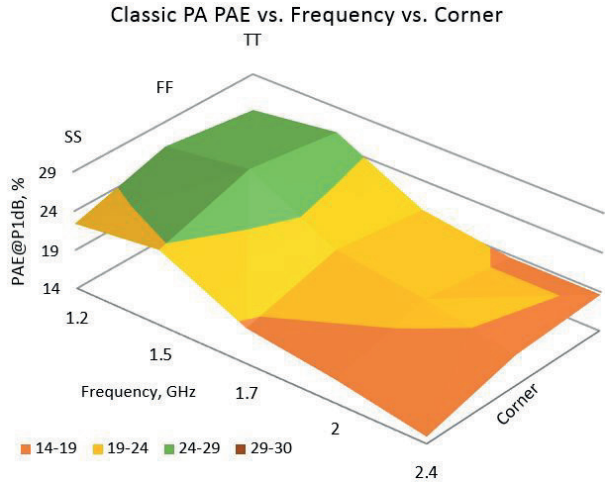


b

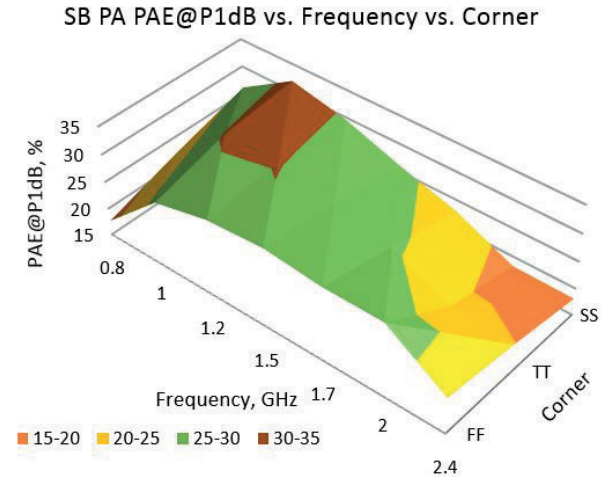
Figure 5: Classic PA (*a*) and self-biased PA (*b*) output referred 1 dB compression point at different frequencies and corners

Power added efficiency is presented in Figure 6. Self-biased PA average PAE is 25.3 % which is 4.2 % higher than PAE of the classic PA.

Table 2 presents the raw simulation data for surface plots in Figure 5 and Figure 6. The results presented in Table 2 depict that the self-biased PA architecture has a



a



b

Figure 6: Classic PA (*a*) and self-biased PA (*b*) power added efficiency at different frequencies and corners

25 % vantage in bandwidth and 1.4 % – 5.8 % efficiency at all corners and frequencies.

The layout of the designed dual differential power amplifier, implemented in IBM 7RF 0.18 µm CMOS process,

Table 2: Classic and self-biased CMOS power amplifier performance comparison at different frequencies and corners

SS		Classic PA OR-P1dB			SB PA OR-P1dB			Classic PA PAE@P1dB			SB PA PAE@P1dB		
		FF	TT	SS	FF	TT	SS	FF	TT	SS	FF	TT	
Frequency, GHz	0.8	-	-	-	9.9	10.6	10.4	-	-	-	26.0	17.6	22.1
	1.0	-	-	-	10.2	11.5	11.0	-	-	-	31.9	26.5	30.3
	1.2	11.5	10.5	11.1	10.3	12.0	11.3	22.4	25.8	24.3	29.6	28.8	30.1
	1.5	11.5	10.5	11.0	9.8	12.2	11.1	23.7	27.4	25.8	26.1	29.5	28.3
	1.7	11.1	10.2	10.7	9.0	12.1	10.7	18.5	21.7	20.2	23.0	28.5	25.8
	2.0	10.5	9.8	10.3	7.9	11.7	10.0	17.0	20.2	18.7	18.3	28.5	20.9
	2.4	10.0	9.5	9.9	7.6	11.4	9.6	14.9	17.9	18.7	18.1	21.7	20.1

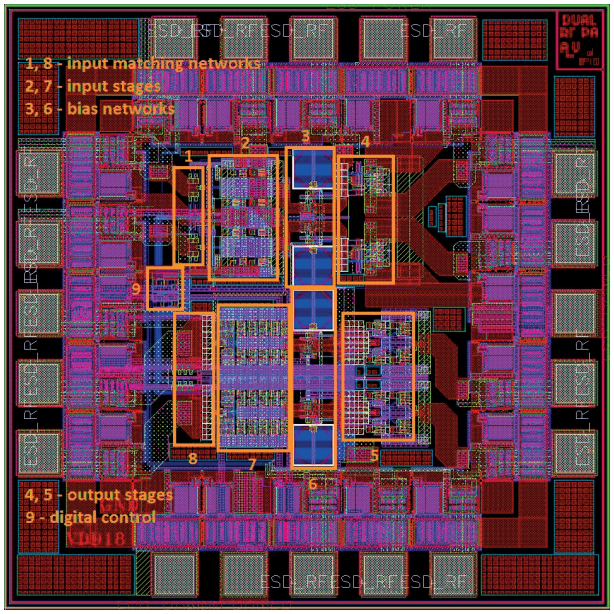


Figure 7: Dual differential power amplifier IC layout

IC is presented in Figure 7. PA implemented in classic architecture is presented on the top of the latter figure, and the self-biased PA – on the bottom. On-chip input matching network tuning circuits are marked 1 and 8. Active input stages are marked 2 and 7. Output stage bias networks are marked 3 and 6. Active output stages are marked 4 and 5 whereas digital control block is marked 9. The active area for both on-chip PAs is 800 μm^2, whereas the full IC chip size is 1.5 mm^2. The dual PA ASIC has been designed to be enclosed in a 20-pin QFN package and is prepared to be send to fabrication.

5 Conclusion

A comparison between a classical and a self-biased PA architectures was presented in this article both suitable for a wideband Doherty configuration. Both PAs are fully differential have been implement in IBM 7RF 0.18 μm CMOS process and are supplied from 1.8 V. Classical PA architecture has a notch type S_{11} response and a bandwidth up to 1.1 GHz (from 1.6 GHz to 2.7 GHz @ S_{11} = -10 dB) with external matching components. Self-biased PA his matched from 800 MHz to 1.75 GHz without any additional matching components and the bandwidth can be further increased to 2.15 GHz by introducing an external matching network and by tuning the on-chip capacitance. Self-biased PA average PAE is 25.3 % which is 4.2 % higher than that of the classic PA. Both power amplifiers have an average output power of 10.5 dBm. The latter results show, that a self-biased PA architecture has more potential to be implemented in a wideband DPA configuration, compared to the classic PA arrangement. The active area for both on-chip differential PAs is 800 μm^2, whereas the full IC chip size is 1.5 mm^2. The dual PA ASIC has been designed to be enclosed in a 20-pin QFN package and is prepared to be send to fabrication.

6 References

1. Qian-Fu Cheng et al. "Investigating the global trend of RF power amplifiers with the arrival of 5G". Wireless Symposium (IWS), 2015 IEEE International. March 30 2015-April 1 2015. pp. 1-4.
2. R. Giofre, L. Piazzon, et al. "A distributed matching/combining network suitable for Doherty power amplifiers covering more than an octave frequency band". 2014 IEEE MTT-S International Microwave Symposium (IMS2014). 1-6 June 2014. pp 1-3.
3. Xian Cui, et al. "A 3.5 GHz CMOS Doherty power amplifier with integrated diode linearizer targeted for WiMax applications". MWSCAS 2007. 50th Midwest Symposium on Circuits and Systems. 2007. 5-8 Aug. 2007. pp. 465 - 468.
4. N. Ryu, J. H. Jung, and Y. Jeong, "High-efficiency CMOS power amplifier using uneven bias for wireless LAN application". ETRI J., vol. 34, no. 6, Dec. 2012. pp. 885–891.
5. C. Y. Liu. "A 2.4 GHz CMOS Doherty Power Amplifier". IEEE MTT-S International Microwave Symposium Digest, 2006. 11-16 June 2006. pp. 885 - 888.
6. J. H. Kim, et. al. "Single-Ended CMOS Doherty Power Amplifier Using Current Boosting Technique". IEEE Microwave and Wireless Components Letters (Volume: 24, Issue: 5). 06 May 2014. pp. 342 - 344.
7. N. Ryu et al. "CMOS Doherty Amplifier With Variable Balun Transformer and Adaptive Bias Control for Wireless LAN Application". IEEE Journal of Solid-State Circuits, Vol. 49, issue 6. 10 April 2014. pp. 1356 - 1365.
8. N. Wongkomet, et al. "A 1.7GHz 1.5W CMOS RF Doherty Power Amplifier for Wireless Communications". Digest of Technical Papers. IEEE International Solid-State Circuits Conference, 2006. ISSCC 2006. 6-9 Feb. 2006. pp. 1962 - 1971.
9. J. Kang, et al. "A Ultra-High PAE Doherty Amplifier Basedon 0.13-um CMOS Process". IEEE Microwave and Wireless Components Letters (Volume: 16, Issue: 9). 28 August 2006. pp. 505-507.
10. H. H. Liao, H. Jiang, P. Shanjani and A. Behzad. "A fully integrated 2x2 power amplifier for dual band MIMO 802.11nWLAN applications using SiGe HBT technology", IEEE RFIC Symp. Dig. 2008. pp. 515–518.

11. W. M. Gaber, et al. "A CMOS IQ Digital Doherty Transmitter Using Modulated Tuning Capacitors", 2012 Proceedings of the ESSCIRC. 17-21 Sept. 2012. pp. 341 - 344.
12. M. L. Carneiro, et al. "A 2.535 GHz fully integrated Doherty power amplifier in CMOS 65nm with constant PAE in backoff". 2013 IEEE Fourth Latin American Symposium on Circuits and Systems (LASCAS), Feb. 27 2013-March 1 2013, pp. 1-4.
13. A. Afsahi, A. Behzad, and L. E. Larson "A 65 nm CMOS 2.4 GHz 31.5 dBm power amplifier with a distributed LC power-combining network and improved linearization for WLAN applications". IEEE ISSCC Dig. Tech. Dig., 2010, pp. 452–453.
14. N. Deltimple, et al. "Integrated Doherty RF CMOS Power Amplifier design for Average Efficiency Enhancement". 2015 IEEE International Wireless Symposium (IWS). March 30 2015 - April 1 2015. pp. 1-4.
15. P. Colantonio, F. Giannini et al. "Designing a Doherty power amplifier". Melecon 2010 - 2010 15th IEEE Mediterranean Electrotechnical Conference. 26-28 April 2010. pp. 543 - 548.

Arrived: 15. 06. 2016
Accepted: 01. 07. 2016

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 2(2016), 80 – 90

Performance of Ni-alloy MEMS-probes coated with PdCo films in semiconductor wafer test

Bahadir Tunaboylu

Istanbul Sehir University, Department of Industrial Engineering, Istanbul, Turkey
TUBITAK Marmara Research Center, Kocaeli, Turkey

Abstract: A novel electroplating system and approach for selectively coating of probe tips for wafer and package testing are presented. A Ni-alloy probe tip with an overcoat layer of 3.5um thick PdCo provided less tip wear and better electrical contact resistance performance in wafer testing. Microstructures of films resulting from different conditions of electroplating process were analyzed, most uniform films were obtained at 5 mA of plating current conditions. The probe tip wear throughout probe life testing was monitored which indicates PdCo film with Au underlayer establishes good electrical contacts.

Keywords: Wafer test; electroplating PdCo films; probes;, contact resistance

Lastnosti MEMS sond iz Ni litine in prevlečenih z PdCo filmom pri testiranju polprevodniških rezin

Izvleček: Predstavljen je nov sistem selektivnega nanašanja prevlek na konice sond za testiranje rezin. Konica sonde iz Ni litine, ki je prevlečena za 0,35 um debelo plastjo PdCo predstavlja boljši električen kontakt in manjši vpliv dotika pri testiranju rezin. Analizirane so mikrostrukture plasti, ki nastajajo pri različnem procesu nanašanja z elektriko. Najbolj homogene plasti so bile dosežene pri toku 5 mA. Spremljana je bila obraba konic sond, pri čemer smo ugotovili, da dober električen kontakt zagotavljajo konice z PdCo plastjo, ki je nanešena na plast Au.

Ključne besede: testiranje rezin; nanos PdCo plasti z elektriko; sonde; kontaktna upornost

** Corresponding Author's e-mail: btunaboylu@sehir.edu.tr*

1 Introduction

In wafer and package testing, spring connectors are utilized to transmit test signals from a testing system and the semiconductor device by an electrical contact on the device pads or bumps. The probes shown in the probe card structure in Fig. 1 or spring pins shown in Fig. 2 are used in wafer and package testing respectively. Spring pins are used in flip-chip bump testing in sockets and conventional probes are typically made of Pd-alloys or beryllium-copper (BeCu) [1-3], and can potentially have outer layers of overcoat, while more advanced style probes produced lithographically are made of Ni-alloys, or MEMS (Microelectromechanical systems) probes [4-7]. Outer layers coated on those probe types can be pure or alloys of nickel, gold, or rhodium and palladium, intended to increase the hardness and decrease wear of the probe or pin. In testing, it is required for probe tip to pierce the oxide layer on the pad or bump consistently to secure good electrical connection. A very hard probe tip, achieved with an overcoat, is needed for long probe life. This type of coating on the spring section of the probe is undesirable since it may peel off during cycling operation of a probe or lead to an unwanted change in the spring characteristics of a probe and also it is more expensive to coat the whole probe.

The spring section of the probes are typically electrodeposited from nanostructured Ni-alloys, NiMn or NiCo, utilized as structural spring members and contact tips may have various coatings for reliable electrical contacts needed in fine pitch Cu pillar and other test requirements [7-11]. These types of alloys were used for their strength, ductility and thermal stability as well as good electrical conductivity necessary for good electrical contacts. In addition, these two alloys are electroformable and lend themselves to MEMS processes allowing creation of small structures and probe geometries.

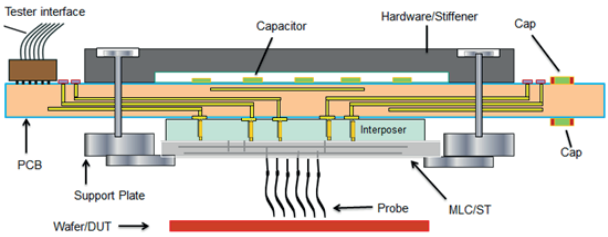
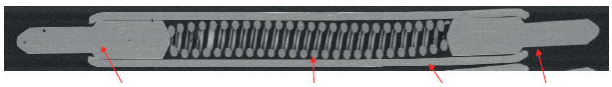


Figure 1: The probe card structure showing the test system, probes and the wafer. Cap refers to capacitor and MLC/ST refers to multilayer-ceramic and the space transformer.



a) Plunger Spring Shell Plating over plunger

b) Spring pin types

Figure 2: Spring pins in two different designs typically used in package testing. The spring in the middle is typically made of stainless steel and the other components are made of brass or BeCu.

A coating system for applying a coating to only a tip portion of a probe was developed and used in this study. The coating system includes a container for holding a coating material and a porous plate adjacent the container for receiving a portion of the coating material during a coating process. The system was described in detail elsewhere [12]. The plating solution used was a palladium cobalt solution with a targeted ratio of Pd to Co ranged from 60 wt.% Pd and 40 wt.% Co to 80 wt.% Pd to 20 wt.% Co. Some material properties and contact reliability of palladium cobalt and palladium nickel were previously reported [13,14]. PdCo may offer less porosity and superior finish on the probe surface compared to other coatings. Because it possesses a fine grain structure and a low coefficient of friction, it will prevent metal debris adhering from the contact pad. PdCo-tip plating offers better probing performance in repeated test cycles due to a reduction or elimination of debris buildup on the probe tips. Probes typically contact solder bumps such as PbSn, Cu or SnAgCu bumps and Al or Cu pads on wafers. Various Pd-alloys or films with nanocrystalline microstructures have been investigated using different physical and chemical approaches towards sensors or fuel cell catalyst applications in the past [15-17]. Nanostructured and nanoporous Pd materials were synthesized by electrochemical methods for various fuel cell studies and for its some magnetic properties [18-23].

In this work, different conditions of electroplating process of PdCo coating on NiMn probes were analyzed, and plated probe tip microstructures were studied. It must be stated that PdCo coatings applied on the plunger (contacting ends of pins) or shells of spring pins, manufactured by final machining processes, are produced in a lot immersed in plating solution, quite different than the present proposed process. In this process, MEMS probes are produced by lithographic electrodeposition of NiMn alloy first, subsequently the ends of probes which contact the bumps on wafer are overcoated with series of steps with PdCo. Selective plating of vertical style probes with PdCo overcoat with an underlayer of Au is presented here for the first time. The probe tip wear throughout life testing in test cards was monitored and presented.

2 Experimental

Probe sets as strips for the study were manufactured through lithographic methods. Probes are electroplated from NiMn alloy. The probe formation process begins with laminating the desired material, masking the laminated material to define the probe set and UV imaging this, remove the mask and then develop the imaged material. Subsequently probes are formed from this photoresist pattern defined shape in the plating process. The strip used in PdCo plating is illustrated in Fig. 3 a. One method of getting the PdCo plating applied only to the tips, a resist coating may also be applied to the probes. The resist coating such as NIT215 or NT250 dry films available from Morton Electronic Materials Chicago, Illinois or Intermountain Circuit Supply, Scottsdale, Arizona, were applied by a lamination process. The resist coating may have a thickness of between approximately 30 µm and 50 µm, other than the probe tip. A sketch showing a cross-section of probe tip section with the resist coating prior PdCo electroplating operation is shown in Fig 3 b.

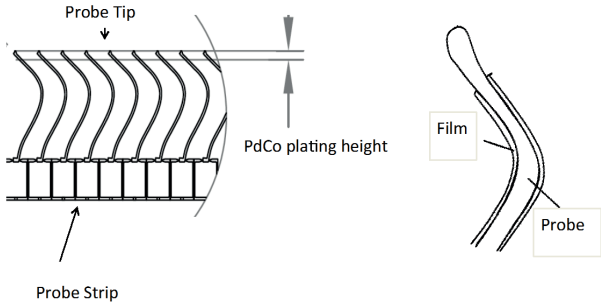
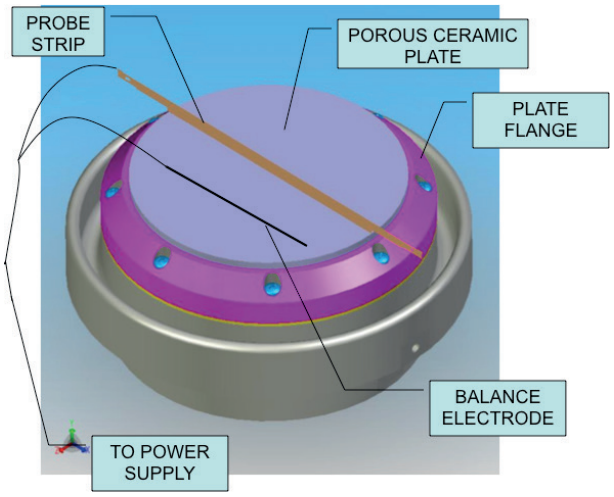
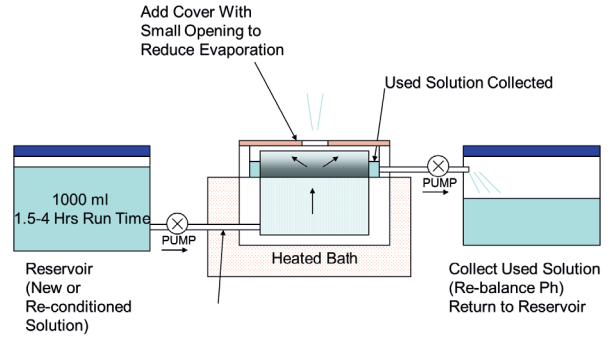


Figure 3: The probe strip used in PdCo plating is illustrated (A on the left) and the probe tip section and the resist coating (film) in (B on the right).



a



b

Figure 4: The plating system.

Figure 4 a shows the designed container with a plating solution. The container may be formed from insulator material and anode may be located within the plating solution. The electrodes and the probes are connected to a power source. The probe strip shown in Fig 3 a. comes into contact with the fiber sheets on top of the ceramic plate on the container. Once the probe tips contact the fiber sheets, the plating solution wets the tip of the probes. Fiber sheets may be cellulosic or other synthetic fibers (or nylon, polycarbonate and glass from Whatman International, Clifton, N.J.) similar to those used as filter papers. In order to minimize surface tension of the plating solution to prevent or minimize wicking of the plating solution between probes. It is desirable to plate only tips of the probes in the strip, and prevent plating over the full length. The plating solution is maintained at approximately 50 degrees °C, by using water bath held in glass bowl warmed by hotplate, while the electrical system is held at approximately 4 volts and the current density at approximately 10 asf (Amps/ft, where 1 ft. equals 30.48 cm). In order to plate the probe tips, the backing plate is lowered so as to submerge the probe tips in the plating solution. Current is supplied from the power source to cause the plating solution to adhere to the probe tips. Fig 4 b shows the system with reservoir connection showing a replenishing scheme for the plating solution. The pH of a solution should be maintained during the plating cycle. When used solution collected in the right reservoir deviates from the plating solution pH, then rebalancing meaning bringing the solution back to original pH is carried out before solution is fed back to main reservoir to keep the total volume.

After the plating has completed on the probe tips as planned, the probes are removed from the plating solution, and the resist coating can be removed using a variety of conventional techniques, for example, through the use of a stripper bath, such as ADC available from RBP Chemical Technology, Milwaukee. Alternatively, it may be removed using another material such as n-methylpyrolidinone (NMP). There may be sources of variations across PdCo plating process steps which will impact final probe plating quality and test results. Table 1 summarizes process steps used in this study and nearly forty steps which may contribute to variations in the manufacturing various strips with coatings and finally qualification testing.

In qualification of the PdCo plating process used for the probe tips, a wafer test card was used at real test conditions of wafers. Test vehicle consisted of a MLC (Multilayer ceramic space transformer) bonded with MEMS (Microelectromechanical systems) style probes. For life-testing, 200 probes with PdCo tips plated were used as electrical contacts touching wafers. Probe tips were coated with PdCo with an underlayer of Au to ensure good adhesion and good electrical contact. Probing recipe is as follows: 0.5 A/B ratio in probing chuck movement of Prober (TEL XL) at 70 µm of probe overtravel (OT) which defines the probe deflection amount. Probes are cycled on a prober touching on a wafer contacting bumps. The contact resistance (Cres) measurements at initial, 90K, 175K, 250K, 340K, 425K, 513K, 595K, 670K, 760K and 844K cycles. Cleaning recipe was applied on probe tips was as follows: Every 87 touchdowns, 25 insertions at 50 µm OT to maintain good contact resistance. Cleaning of debris from probe tips during the testing cycle was carried out using a 3M Tape 0.5 µm-grid Type A on a prober. The term 'Touchdown' used commonly in wafer testing industry is described as the probe making a physical and thus an electrical contact with a wafer pad or a bump and the signal passing through the circuit under testing. The probe, the probe card structure and the wafer were illustrated in Fig. 1.

3 Results

When NiMn probes had no tip coating, the contact resistance (Cres) results were not very stable since probe tip sizes grew as probe cycling on contact pads in-

Table 1: Plating process steps

Process Step	
1. SYSTEM PREP	
	Fill heating water bath
	Unplug external thermocouple. Turn hot plate and stirrer on (125 ºC / 200 rpm)
	Plug external thermocouple; set hot plate to 65 ºC
2. PREPLATE CLEANING	
1. Alconox solution	Pour DI (deionized) water into dish
	Add detergent powder (1%)
	Heat cleaning solution to 45 ºC
	Place probes in cleaner 15 min
2. DI Rinse	Prepare DI water rinse baths
	Rinse probes for 5 min
3. H2SO4	30 ml H2SO4, 270 ml DI water, (10% acid)
	Place probes for 5 seconds
4. DI Rinse	Prepare DI water rinse baths
	Rinse probes for 10 min
5. Dry bake	Load baking plate on the hot plate
	Heat to 70 º C
	Load strips and bake for 15 min
3. PLATING	
1.Mounting the probe strip	Clear Jig (strip holder) of remaining material
	Place strip in the center of jig (probe tip up + curvature left to right)
	Seat strip in bottom of track
	Tighten Set screws
	Place and secure Jig in "Gantry"
2. On sequence	Plug the power source wire to jig
	Turn the data logger on
	Lower the jig (probe tips) into plating fluid
	Adjust planarity if necessary using the level screws
	Make sure the strip is parallel to the Pt anode wire
	Turn on input pump
	Turn on output pump
	Remove the bridge (hydrophilic membrane to promote flow) using Q tips
3. Plating Process	Start the current source and time it for 5 min
	Stop current source
4. Off sequence	Turn off input pump
	Turn off output pump
	Put the bridge back on
	Unplug the power source from jig
5. Dismounting the probe strip	Raise the jig
	Remove the jig
	Remove strip from jig
4. POST PLATE CLEANING	
1. DI Rinse	Rinse probes for 10 min in DI water
2. Dry bake	Load strips and bake for 15 min

creased and the scrub on contact metal pads became smaller and irregular in shape, as shown in Figure 5. This led to higher average Cres values as the testing continued, from less 0.5 Ohms at initial cycling to more than 1 Ohms after 100K cycling and 5 Ohms after 200K cycle testing on pads. The average probe tip diameter

grew from 7.5 µm at initial conditions to 18 µm at 100K cycling and 22 µm after 200K cycling. This shows that bare NiMn probe tips do not provide stable Cres necessary for wafer testing, hard and conductive and smooth probe tip materials or coatings are necessary for reliable contact measurements for lifetesting of product wafers. In this study, a relatively inexpensive method of probe tip coating by PdCo is explained. It has only one-step for NiMn electroplating and subsequent single-step PdCo selective plating of just the probe tips. So this process used at this work is radically simpler and cheaper than most widely used existing processes for generating probe assemblies.

Common but more expensive methods for generating probe tips with PdCo or Rh in probe cards have been used in the test industry. Rh tips have been generated on multilayers of Ni-alloys using MEMS process on substrates where up to 25 layers were built up the beams and finally tips, a process also called EFAB [24-25]. In this method, as Ni-alloy beams are electroplated, a sacrificial metal structure made of Cu is also formed. After each layer, a planarization process is employed, then the following thin Ni-alloy layer is electroplated again. The tip made of different metallurgy is done as a final step. Another widely used MEMS-card in the industry involves manufacturing probe beams in many layers and producing PdCo probe tips separately and bonding them together, which is costly and a long process [26-30]. These electrical contacts can be cantilever beams or vertical beams which are also called microsprings. In this method vertical spring starts as a gold bond wire with a spring shape which gets electroplated with Ni-alloy to impart its spring characteristics. After molding and planarization steps, PdCo tips formed separately gets attached in a solder reflow process to wire spring assembly. PdCo tips are generated in an etched silicon wafer.

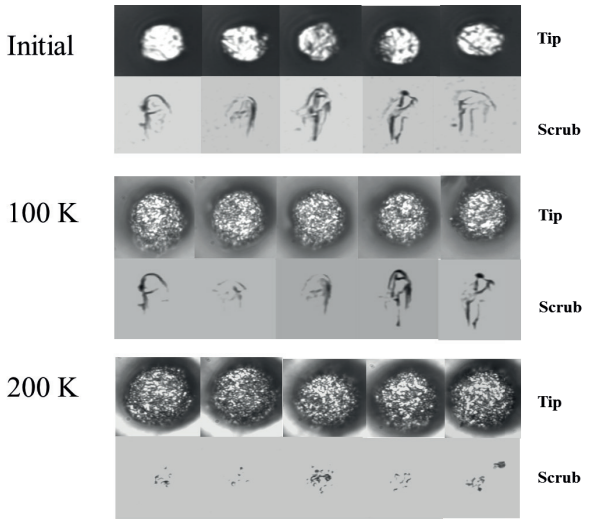


Figure 5: Probes and probe tips made of NiMn and resulting scrub marks are shown at initial touchdown, after 100K and 200K cycling on Al contact pads. As tip diameters grow after cycling, scrub marks start fading.

In this study, the measurements of Pd/Co ratio by weight on the probe strips and corresponding plating thickness readings were made. The palladium content varied from 60 to 78 wt.% in various strips measured by AAS (Atomic Absorption Spectroscopy). Some measurements were initially performed also by WDS (Wavelength Dispersive Spectroscopy). The plating ratios and compositions indicated a range where there is low stress in deposits and no cracking was observed. The plating current was varied to study microstructures and find appropriately uniform microstructures with no sign of cracking in the films. SEM images in Fig. 6-12 show submicron grain structures from different plating current conditions whose duration was approximately 6 minutes. A porous microstructure is observed in Fig. 6 at a low plating current of 3 mA. Most grains have ir-

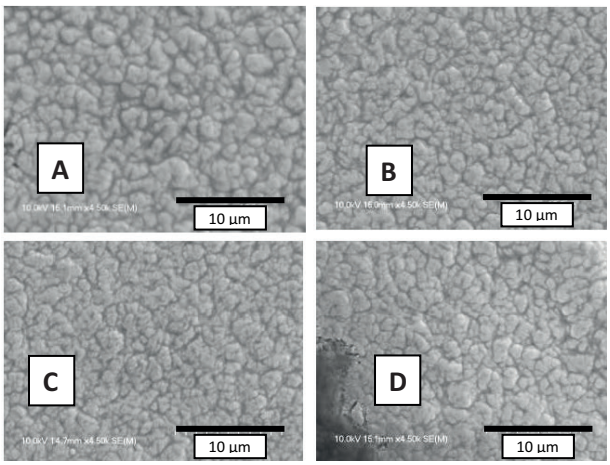


Figure 6: Microstructures produced at 3 mA current conditions.

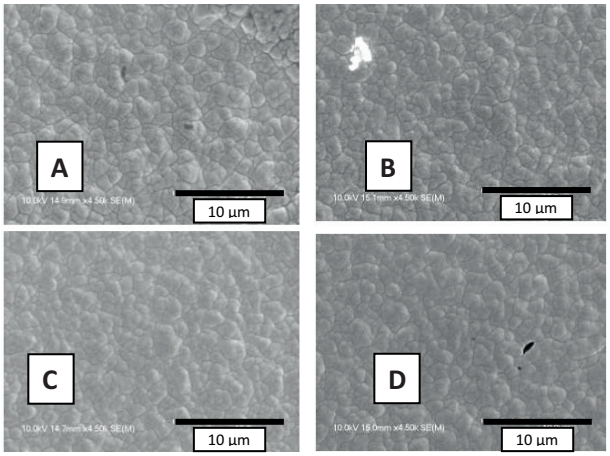


Figure 7: Microstructures produced at 4 mA current conditions.

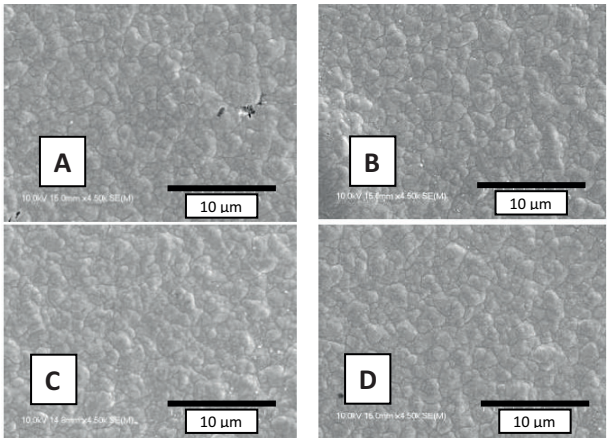


Figure 8: Microstructures produced at 5 mA current conditions.

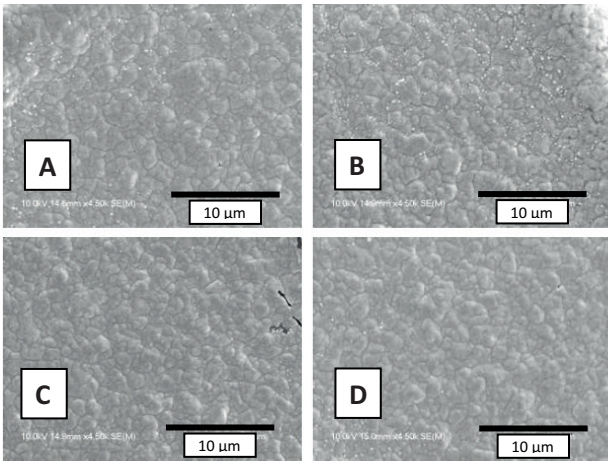


Figure 9: Microstructures produced at 6 mA current conditions.

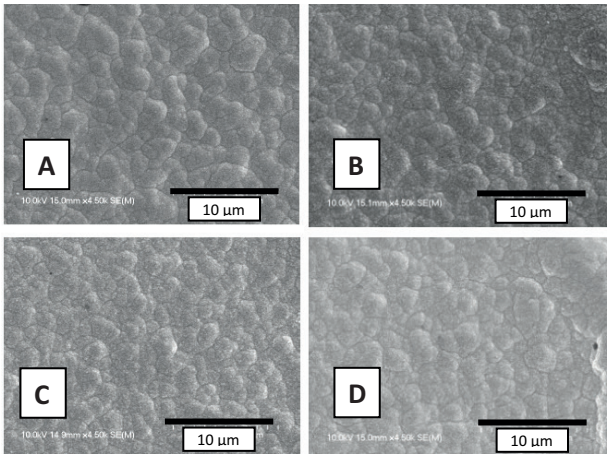


Figure 10: Microstructures produced at 7 mA current conditions.

regular shapes where two or three grains are conjoined together. It appears that grains become more uniform at 4 mA in Fig .7 and at 5 mA Fig. 8 in terms of uniformity of grains and quality of the overplate. Increasing plating current from 6 mA in Fig. 9 to 7 and 7.7 mA in Figs 10-11 changes a fairly uniform size distribution to a somewhat nonuniform or lower quality films. Lower quality films usually have pores or ruptures over the critical surface of probes near their tips. Porous films have typically less integrity and cause delamination of films during aggressive tip cleaning cycles in wafer test. It was noted that as the plating time exceeded 12 min and no stirring was used during the plating cycle, microcracking was observed on the plated surface sections of probe tips as shown in Fig 13. For longer plating time and nonoptimal stirring conditions, microcracking was observed regardless of existence of Au underlayer. Although it is more prevalent to see undesirable microcracking in of PdCo overcoat plated directly over Ni-alloy. It should be noted that the stirring conditions, especially stirring pump-direction was also key to stabilizing the plating quality and compositional uniformity. The compositional variation and grain size variations are less pronounced for stirring condition when operator-to-wall mode is employed. Such mode was used for all plating conditions microstructures are shown from Fig. 6 to Fig. 11. It was seen to produce more uniform microstructures and also compositions of probe beams across the probe strip. The variation of plating composition across a long strip is shown for non-optimal wall-to-operator side stirring direction, as shown in Fig 12, Pd/Co wt. % 60/ wt.% 40 to wt.% 78/ wt.% 22. The pump stirring was optimized to obtain low-stress, compositionally stable uniform grained structures with a uniform and smooth overcoat. In Fig 6-11, images A, B, C, D refer to different locations across a strip analyzed to understand microstructural characteristics. I appears that for these plating conditions, there are no dramatic grain structure or porosity changes within a plating set of conditions. For example, microstructural features in four images of Fig 6 (A, B, C, D) are similar in appearance

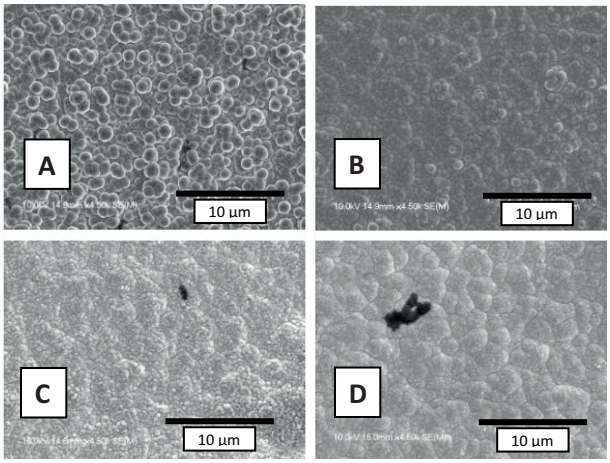


Figure 11: Microstructures produced at 7.7 mA current conditions.

and porosity. A similar correlation is observed for four images in Fig 7 (A, B, C, D).

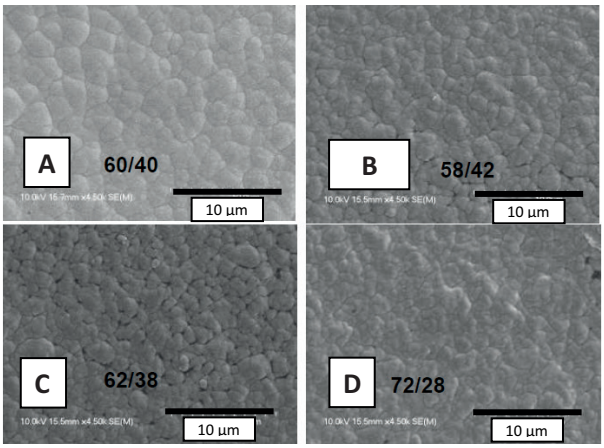


Figure 12: Pd/Co ratio (wt.% of Pd / wt.% of Co) variation for one condition was shown. 6 mA plating current was used. The stirring pump direction was a critical parameter in stabilizing the plating quality and compositional uniformity. Greater variation of plating composition across a long strip is shown for the case of stirring from the wall-side to the operator-side in this case. Pictures labelled as A, B, C, D refer to different locations along the strip.

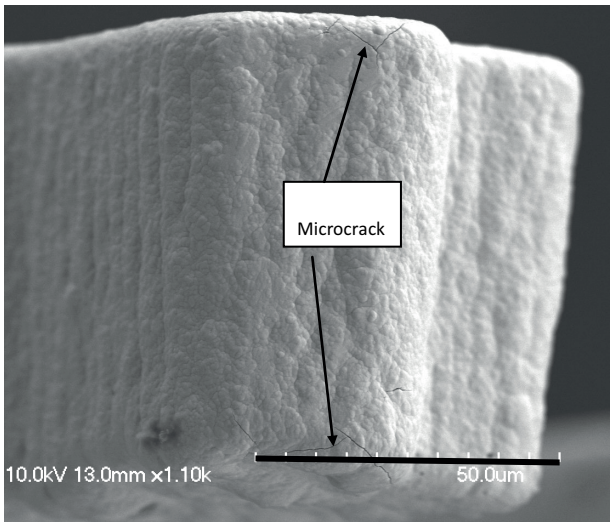


Figure 13: Probe tip microstructure showing microcracks on top and bottom sections.

Figure 14 shows the cross-section of a probe tip where the core is NiMn alloy with electroplated inner Au overcoat layer with an average thickness of 2.9 µm and a PdCo outerlayer with average thickness measured at 5.7µm. Strip 11 in Fig. 14 refers to a strip of probes characterized to exhibit an overcoat chemical composition of Pd/Co 78/22 wt% with a thickness on the high end measured as 5.7 µm on average. This strip was analyzed for Au as well as PdCo coating uniformity and compositions from a total of 14 strips plated in the experiments.

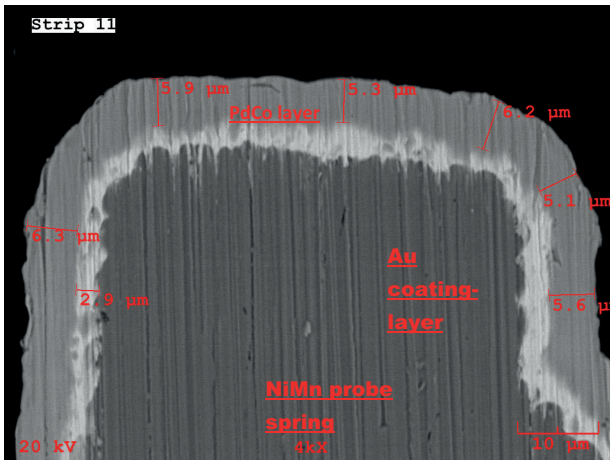


Figure 14: Cross-section of probe-tip is shown for a probe from one of the test strips. Average Pd-Co thickness is 5.7 µm and the average Au innerlayer thickness is 2.9 µm.

Strip probes from selected composition and uniform microstructure lots were used in constructing a test card for lifetest and Cres qualification test. The contact resistance (Cres) is measured using a test system which includes a probe card with contact probes and interface and a test wafer with Al or solder contacts as shown in Fig.1 and in earlier work [4-5]. Signal is sent through one channel which links the prober/probe card and interface which reaches the wafer finally by a probe contact. For some lifecycle and qualification studies, blank wafers coated with Cu or Al or solder materials were used. Bump contact studies were carried out with wafers with Cu pillars or solder-capped copper pillars placed at various pitches, typically daisy chained for contact resistance measurements. Trace resistance was measured for the test vehicle used as the probe card. It contained a probe head carrying probes attached to a space transformer structure including a MLC (multilayer ceramic) and a PCB (printed circuit board), as illustrated in [4]. The trace resistance is calculated as the sum of reistances, $R_{MLC}+R_{probe}+R_{cres}+(R_{probe}+R_{cres})/N$, where R is the resistance and N is the number of probes, i.e. links in the chain being tested. It is more accurate to test many probes due to a negligibly small second term in the equation. For the Cres test, the current is forced through a single probe and all other probes are shorted together and the last probe is sensed.

The average PdCo thickness for test strips was identified to be 3.5 µm. The stability of contact resistance is a very important parameter in wafer test. Probes made from NiMn probes without tip coating did not per-

form well in lifetest and Cres assessments as the tips wore quickly and Cres became unstable after 100K touchdowns. Therefore a stable, non-corroding, non-oxidizing and hard-tip contact material was needed to improve performance. Coating over the tip should not be adhering to the debris generated during scrub cycle of probe tip on the pad or bump on the wafer. Any accumulating debris on the probe tip must be removed by a cleaning cycle. A smooth, nonporous coating such as PdCo offers opportunities for good electrical contact in repetitive test cycles. Contact resistance and lifetesting on a test card indicated a fairly stable mean Cres of 0.2 Ohms up to 844000 touchdowns on test wafers, as seen in Fig. 15. Initial lifetest and stable Cres target was 500K touchdowns and tests indicated good results. In Fig. 15, each measurement interval represents 10 data points (25 data points at 513K). Each data point represents the average of all 120 Cres probes taken before and after cleaning was applied. Cres mean is well below 0.5 ohms (<0.2 ohms, 15,000 data points).

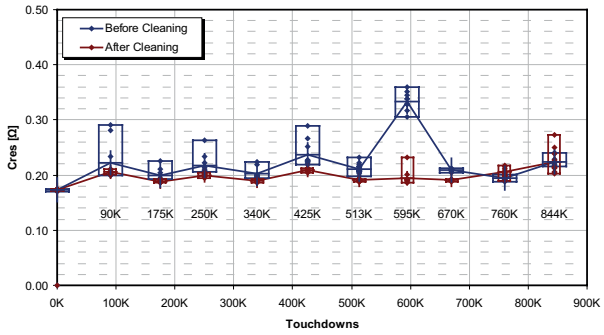


Figure 15: Each data point represents the average of all 120 Cres probes taken before and after cleaning was applied. Cres mean is well below 0.5 ohms.

Figure 16 shows SEM images of probe tips (wedge style) from initial contact on the test wafer all the way up to 854K touchdowns. There is slow progression of tip wear and 12 µm tip width grows to 22um at 250K touchdowns and PdCo and also Au plating on the contacting wedge wears out and NiMn core becomes visible. At 854K touchdowns, the tip width reaches to 33 µm as seen in image 6 in Fig. 16. Despite the tip wear observed, results indicate a good electrical contact based on electrical measurements of Cres as shown in Fig. 15. This was thought to be resulting from the combination of the probe tip composition. The contacting probe surface has both Au and PdCo contacting the bump along with NiMn core and it is possible that current mostly flows from Au plating surfaces in test cycle. Since the gold has the lowest resistivity and no corrosion by products, once the gold plating is exposed, the contact resistance is kept low due to lower resistivity of Au than nickel-alloy. Periodic probe tip cleaning and constant cycling of solder-metal wears out probe tips and breaks through the PdCo overplate, however, this does not seem to cause any significant rise in average contact resistance. Probe tip-pad contact appears to be gold-to-solder pad over lifecycling.

Figure 17 illustrates measurements of the tip width of probes based on SEM photos. The probe tip width reached 16um at 175K touchdowns and Au-underlayer broke through the PdCo overcoat, as the tip growth data shows. The baseline initial tip width was 12 µm. It remained fairly constant at 22 µm from 250K to 550K touchdowns and it grew to 28.6 µm at 760K and 33.3 µm at 854K touchdowns. The graph includes a polynomial which defines the tip wear versus number of touchdown cycles. Probe force stability at initial and final test conditions was also analyzed.

Measurements indicated a constant probe force readings of 8.8 +-0.2 g at 75 µm OT. This suggests that probes survive the test cycle up to 854K touchdown cycle.

It must be stated the PdCo coating can only be applied at tips where it helps good electrical contact between a probe and the bump. It should not be applied over deflecting section of a probe since it can peel off due to insufficient ductility of PdCo coatings over one million cycles necessary. However, underlayer of Au is useful but it is not by itself sufficient for reliable probe contacts over lifetesting. PdCo is harder than Au, leading to decreased wear, increased life and improved reliability in contacting surfaces. PdCo is more stable at higher temperature than the gold. The gold up is stable to 150 °C and the PdCo up to 395 °C under test conditions. During testing, even at high temps, the Cres stays consistent for PdCo plated contacts. Pd oxidizes at high temp ~ 380 °C. Co oxides are thin, self-limiting and conductive. Additionally surface oxides inhibit solder adherence. PdCo has smaller grain size than Au which may lead to lesser potential of diffusion and formation of intermetallic compounds. Intermetallic compound when formed at boundary layer of two dissimilar materials tend to be hard and not very conductive. Pd and Co have higher melting points, 1559 °C and 1425 °C respectively, which show reduced tendency for diffusion and formation of intermetallic compounds. The melting temperature of gold is 1064°C. It was suggested that higher melting point plating material will help inhibit diffusion and formation of intermetallics in earlier research [31]. Also, it was surmised that lower porosity in PdCo does not allow corrosion to penetrate plating and damage base metal. It was reported that PdCo has a lower coefficient of friction than the gold [32]. Solder particles will not adhere to the spring probe surface minimizing excessive contamination or build-up on the probe surface. This provides a consistent contact resistance, allowing for longer periods for testing. NiMn

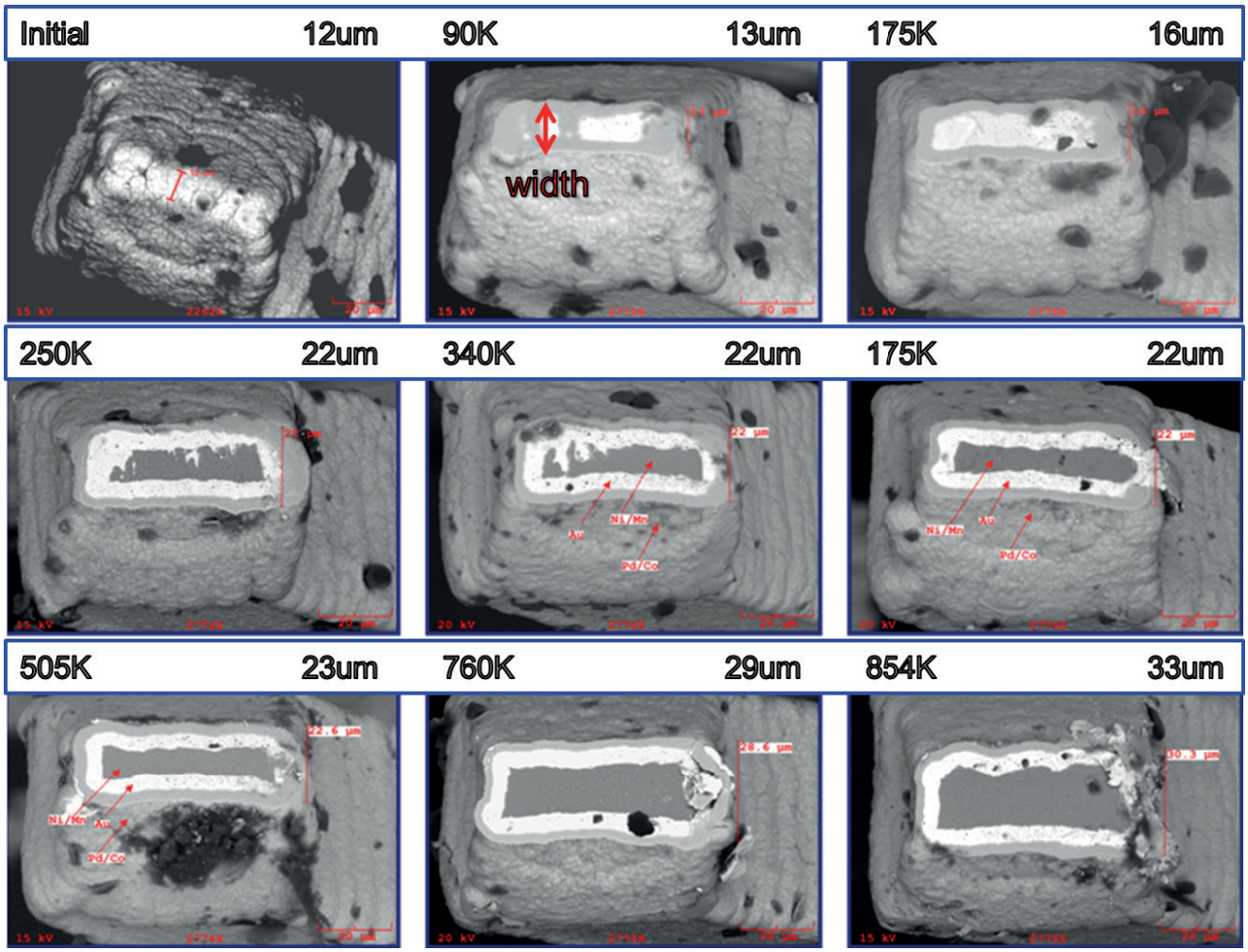


Figure 16: SEM photos showing progression of tip wear in lifetest. The bars above images show number of cycles (from initial to 854K) and measured probe tip with in µm.

alloy is susceptible to oxidation above 100 °C and if used without any coatings as probes, contact pressures need to be increased to achieve stable contact resistance. Also, PdCo (600 HV) [12, 33] is much harder than both NiMn-alloys (300 HV) [9] and BeCu (350 HV) [34]. HV refers to average Vickers hardness values for the electrodeposits. Therefore, probes of these alloys must be coated on the tips for reliable contact resistance.

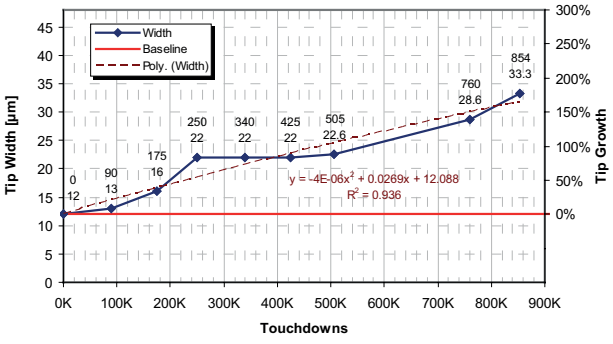


Figure 17: Measurements of the tip width of probes based on SEM photos.

4 Conclusion

A new plating process was developed to plate-up hard PdCo coating in the tip section of NiMn probes used in wafer testing. During testing, PdCo-plating at the probe tip kept Cres low and stable throughout the test even with the excessive wear rate caused by the aggressive cleaning recipe. PdCo thickness could be further optimized to minimize tip wear. Overall Cres performance after cleaning was very satisfactory. The results show the mean value of <0.2 ohms, and a standard deviation of <0.16 ohms. Average tip width grew 200% after 844K touchdowns. Contact force was consistent between initial and after 844K touchdowns.

5 Acknowledgements

This research was supported by a Marie Curie International Reintegration Grant within the 7th European Community Framework Program under grant # 271545.

We also thank SV Probe Inc. R&D members for the discussions and contributions in this study.

6 References

1. B. Prior, "Packaging and interconnect trends," Ed. by M. Jensen, V. treilbergs, O. Prillaman, R. Hussain, F. Taber, M. Noel, I. Feldman, M. Moessinger, J. Moore, I. Pal, *IEEE Burn-in Test Workshop*, Mesa, AZ, USA, 2014, S1.
2. E. Smith, J. Kumnick, B. Quimby, and A. Klein, "Next generation probe alloys," Ed. by J. Broz, R. Rincon, M. Harwood, J. Caldwell, D. James, J. Martens, P. Mui, F. Taber, G. Boehm, M. Huebner, T. Inoue, A. Leong, C. Liu, M. Ojeda and J. Wu, *IEEE Semiconductor Wafer Test Conference*, San Diego, CA, USA, 2013, S27.
3. R. Grimm, M. Hegazy, D. Linjianjun and R. Chen, "3D TSV Cu pillar probing challenges and experience," Ed. by J. Broz, R. Rincon, M. Harwood, J. Caldwell, D. James, J. Martens, P. Mui, F. Taber, K. Armendariz, G. Boehm, M. Huebner, T. Inoue, A. Leong, C. Liu, M. Ojeda J. Wu, and A. Wegleitner, *IEEE Semiconductor Wafer Test Conference*, San Diego, CA, USA, 2014, S20.
4. B. Tunaboylu, "Testing of copper pillar bumps for wafer sort," *IEEE Trans. on Comp. and Pack. Tech.,* 2012, 99(6), 985.
5. S. Theppakuttai, B. Tunaboylu and J. Hicklin, "Probing Assessment on Fine Pitch Copper Pillar Solder Bumps," Ed. by J. Broz, R. Rincon, M. Harwood, M. Griffith and K. Easterling, *IEEE Semiconductor Wafer Test Conference*, San Diego, CA, USA, 2010, S08.
6. S. Angles and R. Vallauri, "Addressing 80 µm pitch Cu Pillar Bump Wafer probing: Technoprobe TPEG™ MEMS solution," Ed. by J. Broz, R. Rincon, M. Harwood, J. Caldwell, D. James, J. Martens, P. Mui, F. Taber, K. Armendariz, G. Boehm, M. Huebner, T. Inoue, A. Leong, C. Liu, M. Ojeda J. Wu, and A. Wegleitner, *IEEE Semiconductor Wafer Test Conference*, San Diego, CA, USA, 2014, S19.
7. A. Wittig, A. Leong, T. Nguyen, T. Masi, J. Kister and M. Slessor, "Key considerations to probe Cu in high volume production," Ed. by J. Broz, R. Rincon, M. Harwood, J. Caldwell, D. James, J. Martens, P. Mui, F. Taber, K. Armendariz, G. Boehm, M. Huebner, T. Inoue, A. Leong, C. Liu, M. Ojeda J. Wu, and A. Wegleitner, *IEEE Semiconductor Wafer Test Conference*, San Diego, CA, USA, 2014, S18.
8. T. E. Buckheit, D. A. Lavan, J. R. Michael, T. R. Christenson, and S. Leith, "Microstructural, mechanical properties of electrodeposited and annealed LIGA nickel structures," *Metall. Mater. Trans.*, 2002, 33A, 539.
9. N. Y. C. Yang, T. J. Headley, J. J. Kelly and J. M. Hruby, "Metallurgy of high strength NiMn microsystems fabricated by electrodeposition," *Scr. Mater.,* 2004, 51, 761.
10. R. Fathi and S. Sanjabi, "Electrodeposition of nanostructured $Ni_{1-x}Mn_x$ alloy films from chloride bath," *Current App. Phys.,* 2012, 12/1, 89.
11. B. Eldridge, "Test parallelism trends," *Chip Scale Rev.,* 2009, 43.
12. B. Tunaboylu, E. L. Malantonio, D. T. Beatson, and A. Hmiel, Probe tip plating, US Patent 7638028, 2009.
13. J. A. Abys, E. J. Kudrak and C. Fan, "The Materials properties and contact reliability of palladium-cobalt," *Trans. IMF,* 1999, 77(4), 164.
14. I. Boguslavsky and V. E. Eckert, "Electroplating of PdCo Alloy for Connector Application," By Electronic Connector Study Group, International Institute of Connector and Interconnection Technology, *Proc. 29th HCIT Connector and Interconnection Symposium*, 1996, 219.
15. N. Alexeyeva, A. Sarapuu, K. Tammevski, F.J. Vidal-Iglesias, J. Solla-Gullón, J.M. Feliu, "Electroreduction of oxygen Vulcan carbon supported Pd particles and Pd-M nanoalloys in acid and alkaline solutions," *Electrochim. Acta,* 2011, 56, 6702.
16. G. V. Strukov, G. K. Strukova, I. E. Batov,M. K. Sakharov, E. A. Kudrenko, A. A. Mazilkin, "Nanocrystalline Pd alloy films coated by electroless deposition," *J. Nanosci. Nanotechnol.,* 2011, 11(10), 8986.
17. K. Lee, O. Savadogo, A. Ishihara, S. Mitsushimas, N. Kamiya, K. I. Ota, "Methanol-tolerant oxygen reduction electrocatalysts based on Pd-3D transition metal alloys for direct methanol fuel cell," *J. Electrochem. Soc.,* 200, 153 (1), A20.
18. R. D. Noce, N. Borelli, P. T. A. Sumodjo, D. R. Cornejo and A. V. Benedetti, "Effect of bath pH on the electrodeposition of nanocrystalline PdCo alloys and their magnetic properties," *J. Magnetism and Mag. Mater.,* 2006, 306, 199.
19. O. A. Petrii, "Electrosynthesis of nanostructures and nanomaterials," *Russian Chem. Rev.,* 84/2 (2013) 159.
20. K. Oishi and O. Savagado, "Electrochemical investigation of Pd–Co thin films binary alloy for the oxygen reduction reaction in acid medium," *J. Electroanal. Chem.,* 2013, 703, 108.
21. Z. Y. Zhou, N. Tian, Z. Z. Huang, D. J. Chen, S. G. Sun, "Nanoparticle catalysts with high energy surfaces and enhanced activity synthesized by electrochemical method," *Faraday Discuss.*, 2009, 140, 81.
22. S. Tominaka and T. Osaka, "Nanoporous PdCo catalyst for microfuel cells: Electrodeposition and dealloying," Adv. Phys. Chem., 2011, 2011, 1.

23. S. Tominaka and T. Hayashi, "Mesoporous PdCo sponge-like nanostructure synthesized by electrodeposition and dealloying for oxygen reduction reaction," J. Mater. Chem., 2010, 20, 7175.
24. C. Folk, "Mechanical design of MEMS probes for wafer test," Ed. by J. Broz, B. Crump, W. Mann, M. Harwood, M. M. Griffith, *IEEE Semiconductor Wafer Test Conference*, San Diego, CA, USA, 2008, S1.
25. K. Kieun. A. Cohen, W. A. Larsen, R. Chen, A. H. Kumar, J. J. Kruglick, V. Arat, G. Zhang, M. Lockard and C.Bang, Microprobe tips and methods of making, US Patent 7273812, 2007.
26. I. Khandros, Method of manufacturing electrical contacts using sacrificial member, US Patent 5476211, 1995.
27. B. Eldridge and G. L. Mathieu, Reassembly process for MEMS structures, US Patent 7010854, 2006.
28. R. Martens, S. Mitchell, "Electrical and mechanical characterization of bladerunner tips on reflowed eutectic bumps," Ed. by W. Mann, R. Rincon, J. Broz and F. Taber, *IEEE Semiconductor Wafer Test Conference*, San Diego, CA, USA, 2002, S1.
29. R. Martens, A. Abdelrahman, S. Martinez, "Microforce probing for devices with low-k ILD materials," Ed. by W. Mann, J. Broz and M. Harwood, *IEEE Semiconductor Wafer Test Conference*, Long Beach, CA, USA, 2003, S4.
30. F. Pietzschmann, "On the way to 30um pads-a new generation of kerf probe cards," Ed. by W. Mann, J. Broz and M. Harwood, *IEEE Semiconductor Wafer Test Conference*, Long Beach, CA, USA, 2003, S6.
31. T. Souza and L. Nelson, "Electroplated Palladium-Cobalt on Test-Probe Plungers," Ed. by F. Taber, J.Hartstein, C. carpenter, V. Treilbergs, J. Ambrosini, M. Harwood, B. Mann, R. Hussain, O. Prillaman, J. O'Sullivan, *IEEE Burn-in Test Workshop*, San Diego, CA, USA, 2003, S7.
32. J. A. Abys,C. O. Dullaghan, and C. Fan, Electrodeposited precious metal finishes having wear resistant particles therein, US Patent 6274254, 2001.
33. H. Groll, M. Celetano, and J. Finnerty, Biological testing system and connector therefor, US Patent 8398443, 2013.
34. BeCu and Paliney- The other probe materials, Advanced Probing Systems Technical Bulletin, Nov 1997, p1.

Arrived: 24. 02. 2016
Accepted: 27. 07. 2016

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 2(2016), 91 – 99

High-performance Current-Controlled Quadrature Oscillator Using an optimized CCII

Samir Ben Salem[1,4], Achwek Ben Saied[3,4] and Dorra Sellami Masmoudi[2,4]

[1]Development Group in Electronics and Communications (EleCom) Laboratory of Electronics and Information Technology (LETI), Sfax, Tunisia
[2]Computor Imaging and Electronic Systems Group (CIEL), Research Unit on Intelligent Design and Control of complex Systems (ICOS), Sfax, Tunisia
[3]Research Center for Computer Science & Multimedia of Sfax (CETIC), Sfax, Tunisia
[4]University of Sfax, National Engineering School of Sfax (ENIS), Sfax, Tunisia

Abstract: This paper proposes two structures of current-controlled quadrature Sinusoidal oscillator in CMOS technology (Voltage mode "VM" and Voltage/Current mode "VCM"). Thanks to its high degree of controllability, the translinear second-generation current conveyor is used as a basic block for our oscillator. The proposed circuit employs three optimized translinear second-generation current conveyors (CCII). The oscillation condition and the oscillation frequency are independently controllable by bias current. The proposed Quadrature Oscillator frequency can be tuned in the range of [285 MHz – 844 MHz] by a simple variation of a DC bias current. ADS (Advanced Design System) simulation results are performed using CMOS 0.18 µm process of TSMC.

Keywords: Voltage Mode Current-controlled Oscillators; Standard CMOS current conveyor; Voltage/Current Mode Current Controlled Oscillators; CMOS 0.18 µm process of TSMC; optimized CCII.

Visoko učinkovit tokovno krmiljen kvadrantni oscilator z optimiziranim CCII

Izvleček: Članek predlaga dve strukturi tokovno krmiljenega kvadrantnega sinusnega oscilatorja v CMOS tehnologiji (napetostni – VM in napetostno tokovni – VCM). Zaradi velike zmožnosti nadzorovanja je za osnovni blok oscilatorja uporabljen translinearen tokovni krmilnik druge generacije (CCII). Frekvenca oscilacije je neodvisno določljiva z enosmerno komponento toka v območju od 285 – 844 MHz. Simulacijski rezultati so narejeni v CMOS 0.18 µm tehnologiji TSMC

Ključne besede: napetostni tokovno krmiljen oscilator; standardni CMOS tokovni krmilnik; napetostno tokovni oscilator; CMOS; CCII.

** Corresponding Author's e-mail: samir.bensalem@isecs.rnu.tn*

1 Introduction

Variable-frequency quadrature Oscillators are basic signal-generating blocks frequently needed in communication systems. The LC or RC quadrature oscillator presents many problems in the literature such as problems of integration, limitations of Surface Acoustic Wave, impedance matching, tuning, linearity, phase noise, … etc. For this reason, the voltage and current-controlled resistors (VCR and ICR) are widely used to replace floating or grounding resistors. The literature abounds with approaches implementing VCR and ICR [2-3]. Some structures use the OTA (Operational Transconductance Amplifier) [1], circuit-based on MOS transistors operating in saturation region [4]. Nevertheless, these circuits suffer from their dependence to absolute temperature and their small input voltage range and complexity of control. Second-generation current-conveyor (CCII) based resistor blocs provide a working solution to solve these problems [5-6].

In order to enhance the performance, minimize the noise effect provoked by the floating and grounding resistor, get controllable characteristics for the proposed Quadrature oscillator, translinear second-generation, current-controlled conveyor based structures seem to be the most efficient [7-8]. These structures

present a higher degree of CCII characteristics control [9-10]. This family of CCII is first proposed in bipolar technology [9-11]. Recently, the translinear CCII family was extended to MOS submicron technologies going towards VLSI design. Reaching submicron technologies, the MOS transistor becomes able to achieve high transit frequencies [12-15]. These CCII's structures are used in different radio frequency (RF) controllable applications such as oscillators, quadrature oscillators and filters [10-15].

This paper is organized as follows: In section II, we present the characteristics of optimized translinear Second Generation Current Conveyors. Simulation results of an optimized translinear second generation current conveyor are highlighted in section III (implemented in 0.18µm CMOS technology). In section IV, we present the CCII based quadrature oscillator architecture. We introduce the proposed Controlled Quadrature Oscillator in section V. Finally, the proposed structure is designed and simulated using ADS (Advanced Design System) software.

2 The optimized transinear loop-based ccii configurations

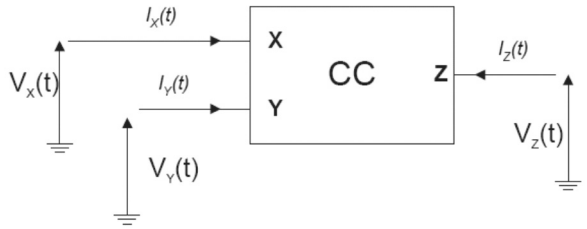


Figure1: General representation of a current conveyor

The CCII is a three-terminal active block. Its general representation is shown in Figure 1. The CCII ensures two functionalities between its terminals:
A Current follower between terminals X and Z.
A Voltage follower between terminals X and Y.

In order to get ideal transfers, a CCII should be characterized by low impedance on terminal X and high impedance on terminals Y and Z.

An implementation of the second-generation translinear loop-based current conveyor with a positive current transfer from X to Z terminal (CCII+) is shown in Figure 2 [10]. In this configuration, the relation between terminal voltages and currents can be expressed in the following matrix:

$$\begin{pmatrix} I_Y(s \\ V_X(s) \\ I_Z(s) \end{pmatrix} = \begin{pmatrix} \frac{1}{\mathrm{R_Y//C_Y}} & 0 & 0 \\ \beta(\mathrm{s}) & \mathrm{R_X} & 0 \\ 0 & \alpha(\mathrm{s}) & \frac{1}{\mathrm{Rz//Cz}} \end{pmatrix} \begin{pmatrix} V_Y(s) \\ I_X(s) \\ V_Z(s) \end{pmatrix} \quad (1)$$

Where R_Y , C_Y and R_Z, C_Z are respectively parasitic resistances and capacitances at port *Y* and *Z*. R_X is the series parasitic resistance at port *X*. α and β are the current and the voltage transfer gains of the CCII, respectively.

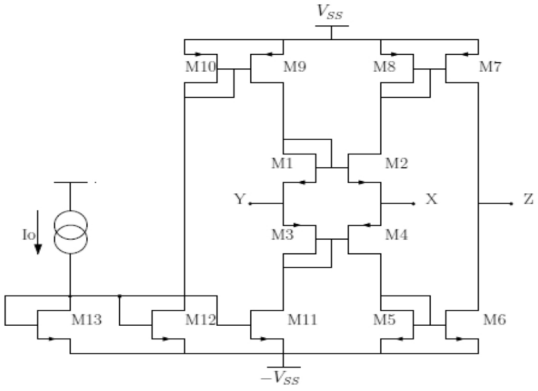


Figure2: Translinear loop MOS-based implementation of CCII

In this configuration, the voltage follower function between Y and X nodes is ensured by means of one mixed translinear loop formed by transistors M1, M2, M3 and M4. Transistors M9-M13 allows the mixed loop to be DC-biased. The output NMOS and PMOS current mirrors duplicate the current flowing from X to Z ports. For later optimization of this configuration, we should dispose of a process dependent explicit model of the different parasitic impedances on X, Y and Z ports. The parasitic effects in this CCII are to be modeled in a 0.18µm CMOS technology. Assuming the same static transconductance factors for the NMOS and PMOS transistors, a simple small signal analysis of the proposed circuits leads to the following expressions:

$$R_X \approx \frac{1}{g_{m2}+g_{m4}} = \left[\frac{1}{\sqrt{2k_P(\frac{W}{L})_P}+\sqrt{2k_N(\frac{W}{L})_N}}\right]\frac{1}{\sqrt{I_o}} = \frac{V_{xy}}{I_x} \quad (2)$$

$$R_z = \frac{1}{g_{ds6}+g_{ds7}} = \frac{1}{\lambda_{N6}Io+\lambda_{P7}Io} \quad (3)$$

$$R_Y \approx \frac{1}{g_{ds1}+g_{ds3}} = \frac{1}{\lambda_{N1}Io+\lambda_{P3}Io} \quad (4)$$

where λ_n and λ_p are channel length modulation factors for NMOS and PMOS transistors, μ_n and μ_p are electrons and hole mobility and g_{mi} and r_{oi} are transconductance

and output resistance of M_i transistor, respectively, with:

$$g_{mi} = \sqrt{2k_{NorP}(\frac{W}{L})_i(1+\lambda_i V_{DS})I_o} \approx \sqrt{2k_{NorP}(\frac{W}{L})_i I_o} \quad (5)$$

$$\frac{1}{r_{oi}} = g_{dsi} = \frac{\lambda_i I_o}{(1+\lambda_i V_{DS})} \approx \lambda_i I_o \quad (6)$$

We can see from the above equations that entire translinear loop-based CCII parasitic impedances can be controlled by means of I_o. Moreover, parasitic resistance on the X (R_X) port was used in many high-frequency tuning applications. Getting lower values of this resistance can lead to higher frequency operations. In this light, we try below to ameliorate the performance of the CCII by optimization approach. This strategy consists in minimizing the X port input resistance value, maximizing the resistance values of Y and Z ports, maximizing high cut-off current (F_{ci}) and voltage (F_{cv}) frequencies, minimizing noise effect ($\overline{i_{T,out}}^2$) and silicon area (S), minimizing the deviation between F_{ci} and F_{cv} and minimizing the deviation between α (current static gain) and β (voltage static gain). To obtain good performance we will maximize the objective function. The objective function can be expressed as follows:

$$F_o = a_1 * F_{ci} + a_2 * F_{cv} + \frac{a_3}{\overline{i_{T,out}}^2} + a_4 * (Ry + Rz) + \frac{a_5}{Rx} + \frac{a_6}{S} + \frac{a_7}{|F_{cv} - F_{ci}|} + \frac{a_8}{|\alpha - \beta|} \quad (7)$$

Where $a_1,...,a_8$ are positive coefficients used for normalization.

The static current and voltage gains are given by the following equations:

$$\beta = \left|\frac{V_X}{V_Y}\right| = \frac{E}{F+E} \quad (8)$$

$$\alpha = \left|\frac{I_Z}{I_X}\right| = \frac{G}{K} \quad (9)$$

Where:

$$E = g_{m8}g_{m5}(g_{m2} + g_{m4}) + g_{m8}g_{m2}(g_{ds4} + g_{ds5})$$

$$F \approx g_{m8}g_{m5}(g_{ds2} + g_{ds4})$$

$$G = g_{m4}g_{m6}(g_{m8} + g_{ds8} + g_{ds2}) + g_{m7}(g_{m2}g_{m5} + g_{ds2}g_{m5} + g_{m2}g_{ds4})$$

$$K = g_{m4}g_{m5}(g_{m8} + g_{ds8} + g_{ds2}) + g_{m8}(g_{m2}g_{m5} + g_{ds2}g_{m5} + g_{m2}g_{ds4} + g_{m5}g_{ds4} + g_{m2}g_{ds5}) + g_{m8}g_{m4}g_{ds5} + g_{m2}g_{m5}g_{ds8}$$

The current bandwidth is given by:

$$H_i(s) == \frac{A}{B * s^2 + C * s + D} \quad (10)$$

Where:

$$A = -(1 + g_{m4} \cdot r_{04})(1 + g_{m6} \cdot r_{06})/r_{06}$$

$$B = C_{gs4} \cdot r_{04}(C_{gd4} + C_{gs6} + C_{gs5})$$

$$D = g_{m4} \cdot r_{04} \cdot g_{m5} + g_{m5}$$

and

$$C = (((C_{gd4} + C_{gs6} + C_{gs5}) \cdot g_{m4} + C_{gs4} \cdot g_{m5}) \cdot r_{04} + C_{gd4} + + C_{gs4} + C_{gs5} + C_{gs6})$$

To optimize the CCII, we use a Heuristic methodology [15-16]. The Heuristic optimization approach follows the plot depicted in Figure 3. It starts with an initialization of the parameters vector which includes the sizing of the different transistors interfering in the above expressions. A random choice of the variables vector is then done followed by a verification of the preliminary conditions. These conditions are imposed to ensure that the different transistors are in the inversion mode of operations. If these conditions are fulfilled, the vector parameters are candidates for the following steps, otherwise we do another choice. Next, we compute the objective function. If it is decreasing, when compared to the previous iteration, the parameter vector is saved; otherwise, we keep this vector unchanged. After a series of trials with the randomly chosen parameters, the parameter vector corresponding to the minimal objective function is obtained. When the number of trials is important, this solution corresponds to an optimal solution. This method does not suffer from any divergence problems seen when applying gradient-

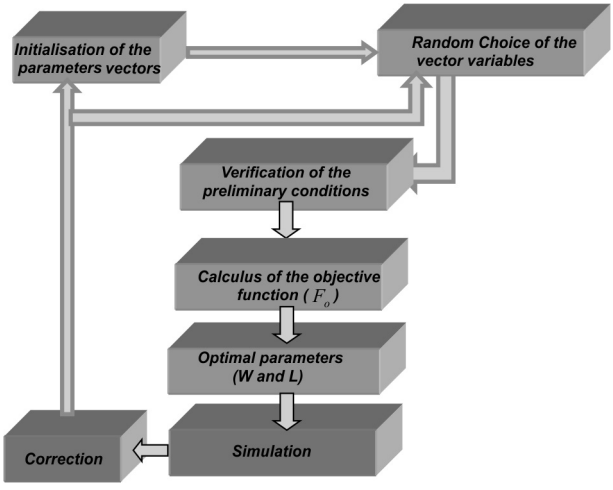


Figure 3: The optimization approach.

based methods, but its efficiency is closely related to the number of iterations. Indeed, with a high number of trials, we manage to explore in a simple random way all the proposed tuning range of the different parameters and good performances are ensured. Finally, we simulate the performances of the optimized CCII. If it is correct we take the optimal parameters else we go to the correction phase.

We notice that the optimization process can be done with a ±1.5V supply voltage and 100µA bias current (table 1). The obtained optimal transistor sizes are reported in table 2.

Table 1: Simulation conditions

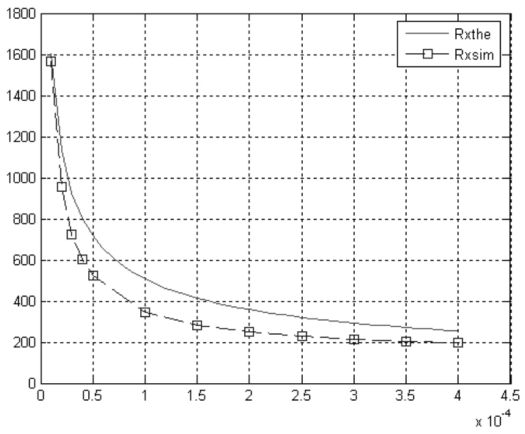
Technology	0.18 µm CMOS TSMC
Supply voltage	1.5 V
Bias current	100 µA

Table 2: Optimal device sizing

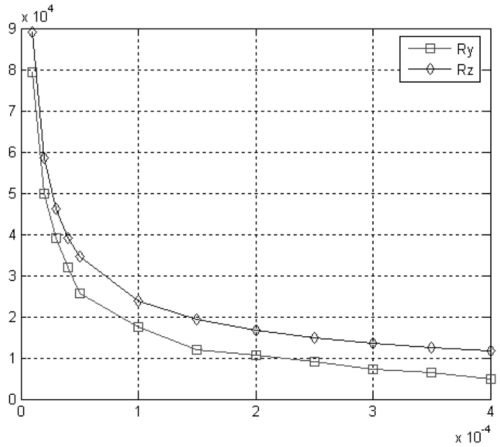
Device Name	Aspect ratio W/L (µm)
M1, M2	6.1/0.18
M3, M4	27.45/0.18
Mxx (in PMOS current mirrors)	13.725/0.18
Mxx (in NMOS current mirrors)	3.05/0.18

3 Simulation results

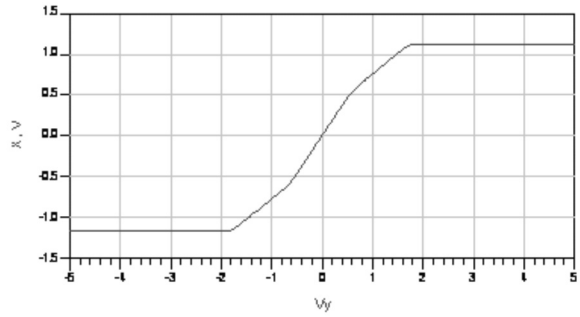
The optimized current conveyor was simulated with ADS software. The main results obtained are represented in Figure 4



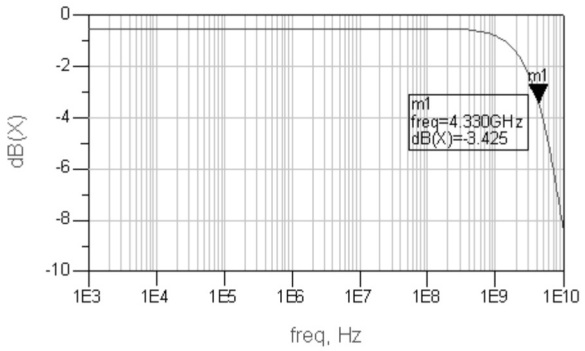
A. Parasitic resistance at x terminal (Rx(Ω)) relative to Io(A)



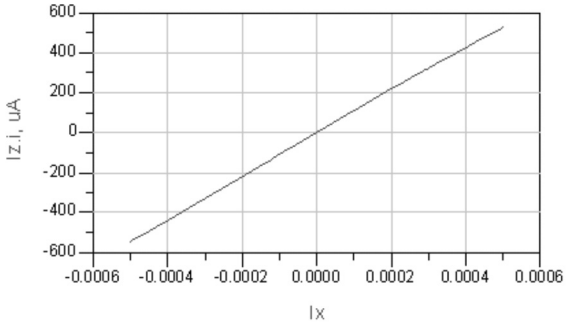
B. Parasitic resistance at Y and Z terminals (Ry(Ω) and Rz(Ω)) relative to Io (A)



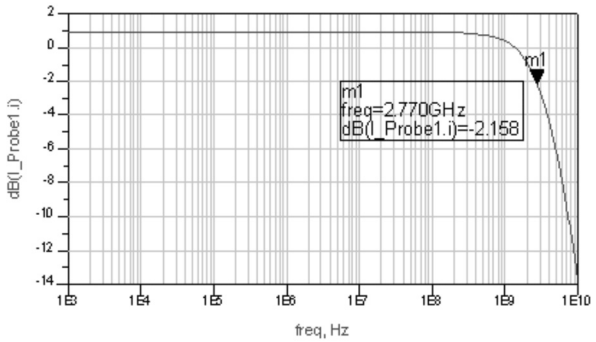
C. Voltage DC transfer characteristic of the CCII



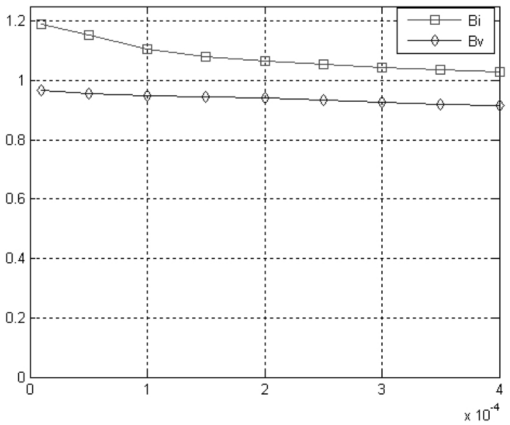
D. Frequency response of the voltage follower Vx/Vy



E. Current DC transfer characteristic of the CCII



F. Frequency response of the current follower Iz/Ix



G. current and voltage gains versus Io (Bi and Bv present respectively αand β)

Figure 4: Performance of the optimized CCII

ADS software simulations of the translinear loop based CCII in Figure 2 were conducted under the optimal parameters. The parasitic resistance at port X is represented in Figure 4.A versus I_o. It is obvious that R_X can be controlled in the range [200Ω, 1.6kΩ] by varying I_o in the range [1μA, 400μA]. The fact that should be underscored is that, even though this structure has a lower R_X when compared to the value given in [11, 15]. Figure 4.A depicts results obtained from both simulations (R_X) and MAPLE theoretical calculus of (R_{Xthe}). We notice a good agreement between both characteristics. Figure 4.B depicts the parasitic resistance values R_Z and R_Y versus the bias current I_o. Accordingly, tunable characteristics can be obtained while higher values of these parasitic resistances are preserved.

Figure 4.C and Figure 4.E display the DC transfer characteristics of the optimized CCII. The voltage transfer can be linear between -0.7V and 0.7V. Moreover, the bandwidths of output terminals are shown in Figure 4.D and Figure 4.F. The −3dB bandwidths of I_z/I_x and V_x/V_y are located at 4.33GHz and 2.77GHz, respectively. Figure 4.G indicates that α and β (current and voltage gains) are close to unity. The remaining other static and dynamic characteristics of the optimized translinear configuration are summarized in table 3.

Table 3: Performance characteristics of the optimized CCII with Io = 100μA and 1.5 supply voltage

Voltage gain β	0.943
Current gain α	1.1
Fci	2.7GHz
Fcv	4.33GHz
Relative current Error	0.15%
Relative Voltage Error	0.093%
Input Impedance(RY//CY)	18KΩ//87fF
Input Impedance(Rz // Cz)	24KΩ//25fF
Input Resistance Rx	380Ω
The offset current	-2.2μA
The offset voltage	13mV

It is noticeable that the optimized configuration yields a high current and voltage cut-off frequencies. This structure is a promising building block for the design of RF blocs such as the controlled quadrature oscillator.

4 Quadrature Oscillator based on the CCII

This architecture of the oscillation structure of Figure 5 [17-18] uses only three optimized CMOS CCIIs, one floating resistor along with the grounded resistors and capacitors. Taking into account these passive connections, we get the following characteristic equation of the oscillator:

$$s^2 C_1 C_5 + sC_5\left(\frac{1}{R_4} - \frac{1}{R2}\right) + \frac{1}{R_4 R_{X3}} = 0 \qquad (12)$$

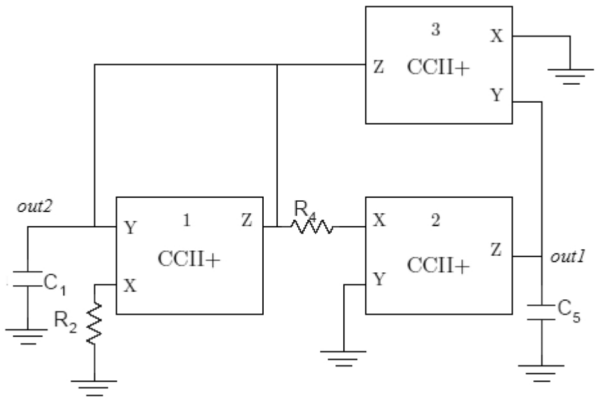


Figure 5: Variable Frequency Oscillator Implementation

This leads to the following oscillation condition and oscillation frequency, respectively:

$$R_4 \geq R_2 \tag{13}$$

$$f_0 = \frac{1}{2\pi\sqrt{C_1 C_5 R_{X3} R_4}} \tag{14}$$

In the reality R_2 and R_4 are respectively given by these relations: $(R_2 + R_{x1})$ and $(R_4 + R_{x2})$. If one of the values varies after implementation, we can recover the correct value by I_{o1} or I_{o2}.

From the above equations, a variable frequency oscillator is obtained. The oscillation frequency can be adjusted independently without modification of the oscillation condition by varying R_{X3}. In this case, the oscillator will be controlled by means of a current source I_{o3}. The confirmed performance of the oscillator is reported in Figure 6, showing the responses of the oscillator where $C_1=C_5=0,3pF$, $R_2=R_4=300\Omega$, $I_{03}=230\mu A$ and $I_{01}=I_{02}=400\mu A$. Figure 7 reveals that the phase and amplitude noise for 10MHz (offset frequency) are -115.5dBc and -145.2dBc, respectively.

A sensitivity analysis of the quadrature oscillator shows that:

$$S_{C_1}^{w_o} = S_{C_5}^{w_o} = S_{R_{x3}}^{w_o} = S_{R_4}^{w_o} = -\frac{1}{2}$$

Therefore, all of the passive-element sensitivities of the quadrature oscillator parameters are low.

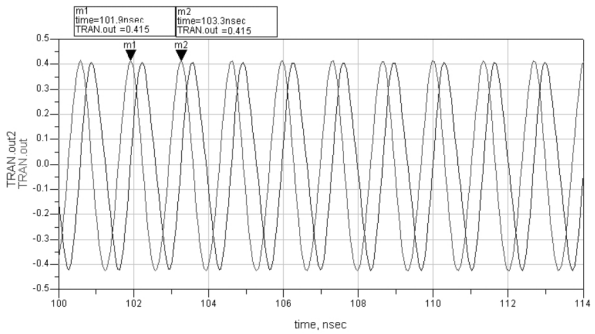


Figure 6: The simulation results of current waveforms of oscillator

The quadrature oscillator is simulated for different CCII bias currents. Simulation results are shown in Figure 8. When varying the current I_{o3} between 30 µA and 400 µA, the oscillation frequency is tuned in the range [285–844 MHz].

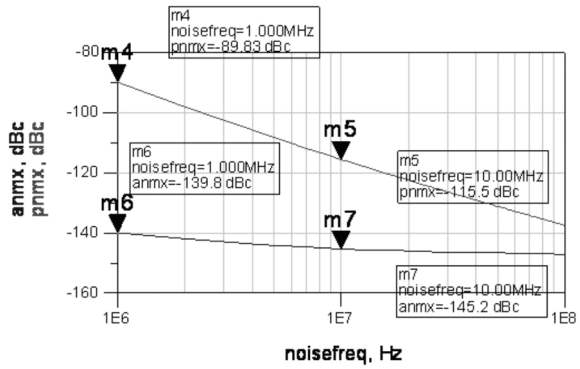


Figure 7: Phase and amplitude noise

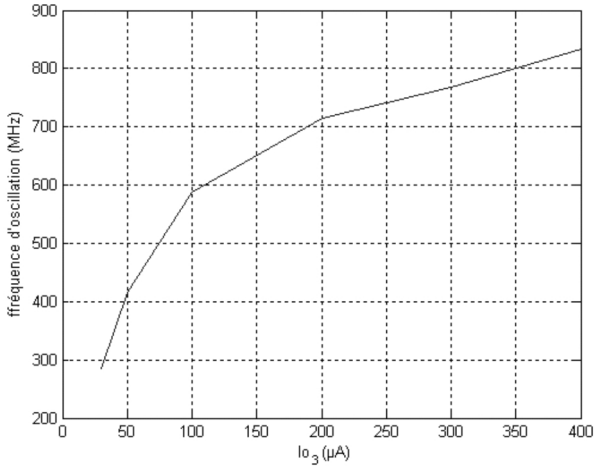


Figure 8: Oscillation Frequency versus Control Current (I_{o3})

The major drawback of this structure is the existence of floating resistance (R_4). The dispersion of manufacturing processes and the temperature variation contribute to the absolute error value of the resistance. In VLSI technology, a resistor is implemented on silicon wafer. However, resistors of practical values on silicon wafer suffer from limited values and high variability due to process variations. Moreover, its resistance values are not variable after integration. The same phenomenon can degrade the value of R_4 and R_2 after integration. Therefore, the basic idea is to replace these resistances

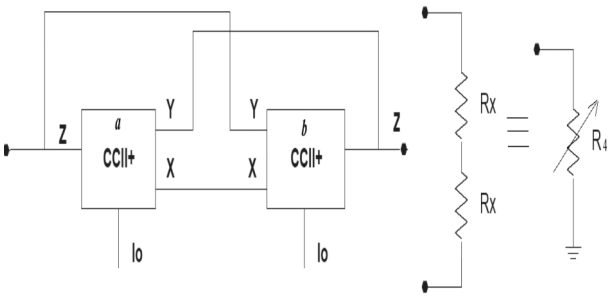


Figure 9: The active floating resistance Req=R_{Xa}+R_{Xb}=R_4

by active resistors bloc. To address this problem, we present in Figures 9 and 10 a solution to eliminate the use of floating resistance and replace the grounding resistor.

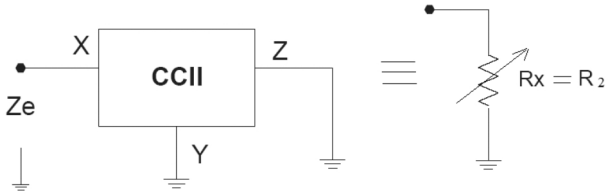


Figure 10: The active grounding resistance Req=R_X=R_2

5 The new Voltage Mode (VM) Current controlled quadrature Oscillator:

The basic idea in the proposed VM quadrature oscillator consists in replacing the resistance R_4 by the active floating resistance given in Figure 9 and the resistance R_2 by the parasitic resistance on port *X* (Figure 10). To realize these blocs, we use this implementation of optimized CCII. The new structure of the quadrature oscillator is shown in Figure 11.

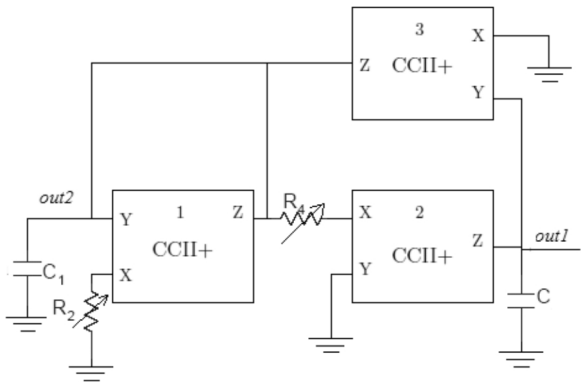


Figure 11: The proposed quadrature oscillator implementation

The advantages of this circuit are the following:

- The circuit enjoys simple controlled optimized structure which can be easily configured to realize quadrature oscillator using the minimum number of passive components.
- The circuit uses grounded capacitors with no externally connected resistors; this should be very convenient for integration.
- The circuit possesses independent controls of the oscillation frequency. Thus, the latter can be controlled by adjusting a bias current of $CCII_3$ without disturbing the condition of oscillation while this condition can be met without disturbing the frequency of oscillation by the bias current of $CCII_4$; this should pave the way for electronic tunability.

The proposed oscillator is simulated for different CCII polarisation currents. The responses of the quadrature oscillator where C_1=*0,3pF*, C_5=*0,3pF*, R_4=R_{Xa}+R_{Xb}=R_2=R_X=*600Ω* (I_{oa}=I_{ob}=*130μA* and I_{o4}=*40μA*), I_{o3}=*230μA* and I_{o1}=I_{o2}= *400μA* are given in Figure 12. The oscillation frequency is equal to 625MHz.

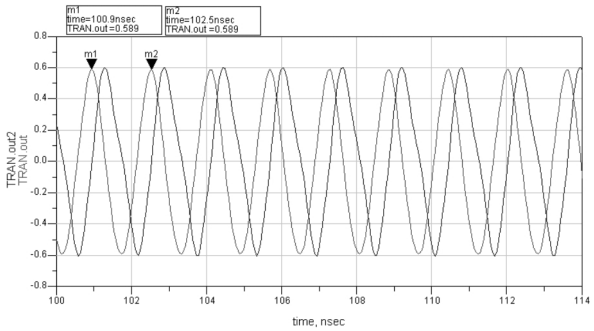


Figure 12: The simulation result of Voltage waveforms of oscillator

To verify and validate the good functionality of the proposed structure, we simulated the two structures (i.e. basic quadrature oscillator and proposed structures) under the same simulation conditions (R_2 = R_4 = 600Ω for the first structure and R_4=R_{Xa}+R_{Xb}=R_2=R_X=600Ω for the proposed structure). Figure 13 illustrates the oscillation frequency versus control bias current of $CCII_3$ (I_{o3}). The maximum relative difference between the frequencies determined for the two structures is less than 0.05%.

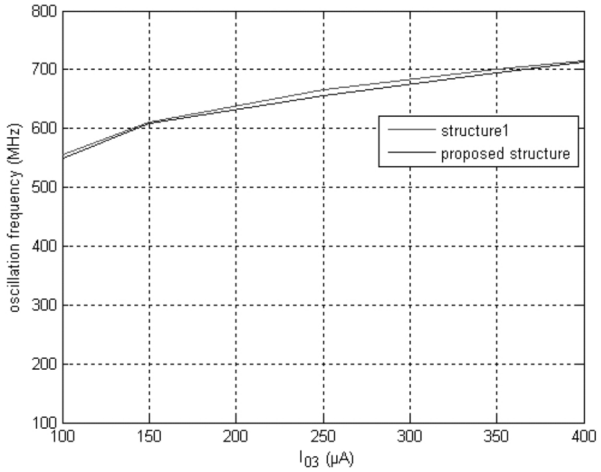


Figure 13: Oscillation Frequency versus control bias current (I_{03})

6 The new Voltage/Current Mode (VCM) current controlled quadrature Oscillator:

The evaluation of the high frequency circuits requires a voltage/current mode design. To transfer the Voltage-mode (VM) quadrature oscillator to a Voltage-Current-mode (VCM) quadrature oscillator, it is necessary to add two voltage/current conversion circuits shown in Figure 14 at the output stage. The voltage/current conversion uses one current conveyor (CCII). Figure 15 shows the ameliorated structure of the Voltage/Current mode quadrature oscillator.

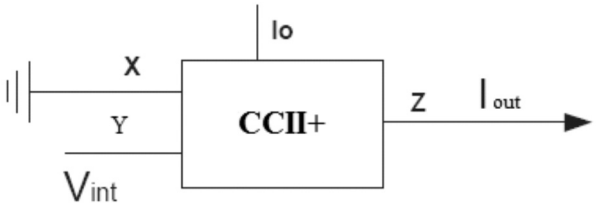


Figure 14: Voltage/current conversion

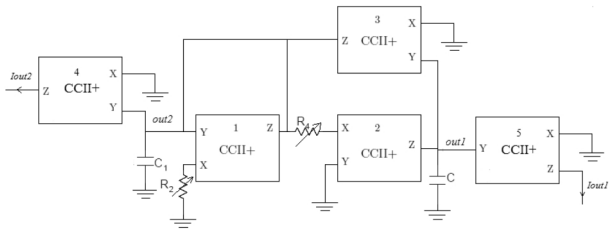


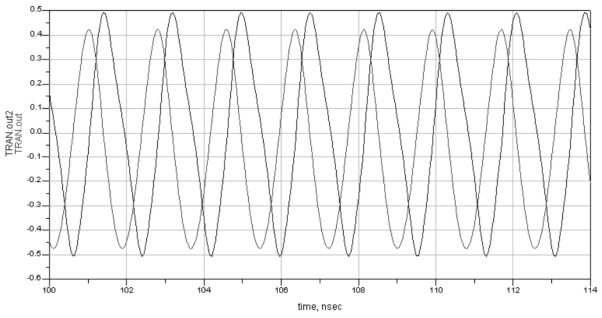
Figure 15: Proposed Voltage/Current mode Quadrature oscillator

The Voltage and Current responses of the VCM quadrature oscillator where $C_1 = C_5 = 0.3pF$, $R_4 = R_{xa} + R_{xb} = R_2 = Rx = 600\Omega$ ($I_{oa} = I_{ob} = 130\mu A$ and $I_{o4} = 40\mu A$), $I_{o3} = 230\mu A$ and $I_{o1} = I_{o2} = 400\mu A$ are given in Figure 16. The oscillation frequency is equal to 625MHz.

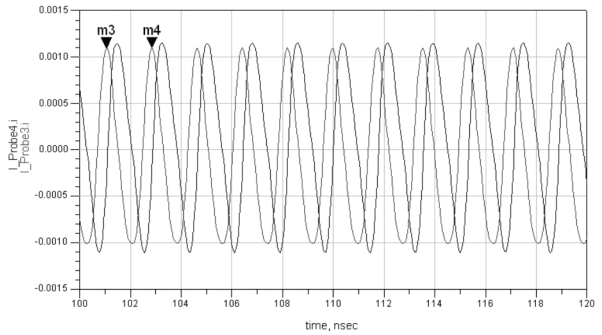
To verify and validate the good functionality, we simulated the VCM quadrature oscillator and the VM quadrature oscillator. Figure 17 illustrates the oscillation frequency versus control bias current of $CCII_3$ (I_{o3}). We notice a good agreement between both characteristics. From this Figure, we see that when varying the control current I_{o3} between 100µA and 400µA, the oscillation frequency is tuned in the range [555 MHz –714.2MHz].

7 Conclusion

In this paper, a new design of variable-frequency, current-controlled quadrature oscillator was proposed.



(a)



(b)

Figure 16: The simulation result of Voltage (a) and current (b) waveforms oscillator

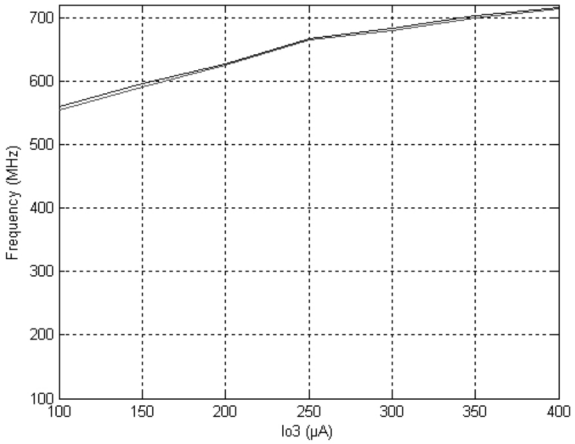


Figure 17: Oscillation Frequency versus control bias current (I_{03})

In order to get higher frequency performance of the quadrature oscillator, a translinear CCII structure is optimized in 0.18µm CMOS process of TSMC. Simulation results show that this oscillator provides an independent control of oscillation frequency and oscillation condition in the range [285MHz - 844MHz] by varying the control current in the range [30µ-400µA]. To validate these results, a comparison between both the proposed and the basic structures is performed. This study demonstrates that the maximum relative difference between the frequencies determined for the two

structures is less than 0.05%. Finally we have proposed a Voltage-Current mode quadrature oscillator. Simulation results show that the proposed VCM oscillator presents a control oscillation frequency between [555 MHz –714.2MHz] by varying the control current in the range of [100µ-400µA]

8 References

1. KHAN, A., AHMED, A. M. T. Realization of tunable floating resistors. *Electronics Letters*, 1986, vol. 22, p. 799–800.
2. SAAID, O., FABRE, A. Class AB current-controlled resistor for high performance current-mode applications. *Electronics Letters*, 1996, vol. 32, p. 4–5.
3. SENANI, R., SINGH, A. K., SINGH, V. K. A new floating current-controlled positive resistance using mixed translinear cells. *IEEE Transactions on Circuits and Systems-II*, 2004, vol. 51, p.374–377.
4. G. Wilson, P. Chan, Floating CMOS resistor, IEE Electronics Letters 28 (1993) 306–307.
5. RIEWRUJA, V., PETCHMANEELUMKA, W. Floating currentcontrolled resistance converters using OTAs. *International Journal of Electronics and Communications*, 2008, vol. 62, p. 725–731.
6. M. KUMNGERN, U. TORTEANCHAI, K. DEJHAN" Voltage-Controlled Floating Resistor Using DDCC " *Radioengineering, vol. 20, no. 1, april 2011*
7. P. Beg, I. A. Khan and M. T. Ahmed, "Tunable Four Phase Voltage Mode Quadrature Oscillator using Two CMOS MOCCIIs," *Multimedia*, *Signal Processing and Communication Technologies*, Aligarh, 14-16 March 2009, pp. 155-157. doi:10.1109/MSPCT.2009.5164198
8. S. Maheshwari, "Analogue Signal Processing Applica-tions Using a New Circuit Topology," *IET Circuits*, *De-vices & Systems*, Vol. 3, No. 3, 2008, pp. 106-115.
9. A. Fabre, F. Seguin. "New second generation current conveyor with reduced parasitic resistance and Band pass filter application" IEEE transaction on circuits and systems1: fundamental theory and applications, VOL.48, NO.6, June 2001.
10. S. B. Salem, D. S. Masmoudi and M. Loulou "A Novel CCII-Based Tunable Inductance and High Frequency Current Mode Band Pass Filter Application," *Journal of Circuits*, *Systems*, *and Computers* (JCSC), Vol. 15, No. 6, 2006, pp. 849-860.
11. Hassan O.Elwan and A. M. Soliman, "Low-Voltage Low-Power CMOS Current Conveyors" IEEE transaction on circuits and systems1: fundamental theory and applications, VOL.44, NO.9, SEPTEMBER 1997.
12. C. Thoumazou, F. J. Lidgey and D. Haigh, "Integrated Circuits: The Current Mode Approach," *IEEE Circuit and Systems Series* 2, Peter Ltd., London, 1993.
13. P. Beg, I. A. Khan and M. T. Ahmed, "Tunable Four Phase Voltage Mode Quadrature Oscillator using Two CMOS MOCCIIs," *Multimedia*, *Signal Processing and Communication Technologies*, Aligarh, 14-16 March 2009, pp. 155-157.
14. Achwek BENSAIED, Samir BEN SALEM and Dorra SELLAMI MASMOUDI "A new CMOS Current Controlled Quadrature Oscillator Based on a MCCII" in the Journal: Circuits and Systems ISSN2153-1285 Volume: 02; Issue: 04; Start page: 269; Date: 2011
15. S. B. Salem, M. Fakhfakh, D. S. Masmoudi, M. Loulou, P. Loumeau and N. Masmoudi, "A High Performances CMOS CCII and High Frequency Applications," *Journal of Analog Integrated Circuits and Signal Processing*, Vol. 49, No.1, 2006, pp. 71-78.
16. M. Fakhfakh, M. Loulou and N. Masmoudi, " An Improved Algorithm-Driven Methodology To Optimize Switched Current Memory Cells By Transistor Sizing " The IEEE Inter. Conf. on Electrical, Electronic and Computer Engineering (ICEEC'04). September, 2004. Cairo, Egypt.
17. D. Sellami Masmoudi, S. Ben Salem, M. Loulou and L. Kamoun " A Radio Frequency CMOS Current Controlled Oscillator Based on a New Low Parasitic Resistance CCII"2004 International Conference on Electrical, Electronic and Computer Engineering ICCEC'04 (0-7803-8575-6/04/$20.00 ©2004 IEEE)

[18 Ben Salem, S.; Sellami Masmoudi, D.; Fakhfakh, M.; Loulou, M.; Masmoudi, N " High frequency CCII based oscillators and multifunction filters" Design and Test of Integrated Systems in Nanoscale Technology, 2006. DTIS 2006. International Conference

19,. U. Torteanchai and M. Kumngern "Current-Tunable Current-Mode All-pass Section Using DDCC" International Conference on Electronic Devices, Systems and Applications (ICEDSA) 2011

Arrived: 12. 07. 2015
Accepted: 13. 03. 2016

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 2(2016), 100 – 105

Processing of steatite ceramic with a low dielectric constant and low dielectric losses

K. Makovšek[1], I. Ramšak[2], B. Malič[1], V. Bobnar[1], D. Kuščer[1]

[1]Jožef Stefan Institute, Ljubljana, Slovenija
[2]ETI Elektroelement d.d., Izlake, Slovenia

Abstract: Steatite ceramic was processed from natural raw materials talc, clay and dolomite. They were stabilised in water electrostatically and electrosterically with polyacrylic acid at pH 9. The suspensions were spray dried and the resulting powders contained granules with a mean size of 10 μm. The powders were dry-pressed and sintered at 1275 °C and 1300 °C for 2 hours. The effect of type of stabilisation and sintering temperature on the phase composition, microstructure and dielectric properties of the ceramic was studied. The X-ray powder diffraction analysis revealed that the orthorhombic protoenstatite and tetragonal cristobalite were present in all the ceramic samples. The microstructures of the samples investigated by scanning electron microscopy were homogenous with grains surrounded with a glass phase and some pores. By energy dispersive X-ray spectroscopy we identified Mg, Si, Al and O in the grains and Mg, Si, O and minor amount of Al, Ca and Fe in the glassy phase. The dielectric constant of the ceramic measured at room temperature and 1 MHz decreased from about 8 to about 5 with increasing sintering temperature from 1275 °C to 1300 °C, while the dielectric losses were between 0.001 and 0.003. The dielectric properties of the steatite ceramic were related to the chemical composition of the glassy phase. The results show that the chemical composition of the phases and the dielectric properties of the ceramic depend on the processing temperature while the type of stabilization of raw materials in water has only a minor influence on these parameters.

Keywords: steatite ceramic; microstructure; dielectric properties

Priprava steatitne keramike z nizko dielektrično konstanto in nizkimi dielektričnimi izgubami

Izvleček: Steatitno keramiko smo pripravili iz naravnih surovin talka, gline in dolomita, ki smo jih stabilizirali v vodi pri pH 9 elektrostatsko in elektrosterično s poliakrilno kislino. Z razprševanjem suspenzije v laboratorijskem razpršilnem sušilniku smo dobili granulat s povprečno velikostjo granul okoli 10 μm. Iz granulata smo z enoosnim stiskanjem pripravili surovce, ki smo jih sintrali pri 1275 °C in 1300 °C 2 uri. Študirali smo vpliv tipa stabilizacije in temperature sintranja na fazno sestavo, mikrostrukturo in dielektrične lastnosti keramike. Z rentgensko praškovno analizo smo ugotovili, da vsi keramični vzorci vsebujejo ortorombsko fazo protoenstatit in tetragonalno fazo kristoblit. Mikrostruktura keramike, ki smo jo preiskali z vrstičnim elektronskim mikroskopom, je bila homogena. Sestavljena je bila iz zrn, ki jih je obdajala steklasta faza, in por. Z energijsko disperzijsko spektroskopijo rentgenskih žarkov smo v zrnih dokazali prisotnost Mg, Si, Al in O, v steklasti fazi pa smo identificirali poleg Mg, Si in O tudi sledove Al, Ca in Fe. Dielektrično konstanto (ε) in dielektrične izgube (tan δ) keramike smo izmerili pri sobni temperature in 1 MHz. Po sintranju pri 1275 °C je imela keramika ε 8, medtem ko je bila vrednost ε po sintranju na 1300 °C nižja, t.j., 5. Vrednoti tan δ so bile med 0.001 in 0.003. Ugotovili smo, da so dielektrične lastnosti steatitne keramike odvisne od kemijske sestave steklaste faze. Rezultati so pokazali, da so dielektrične lastnosti steatitne keramike in kemijska sestava faz keramike odvisne od pogojev priprave keramike, medtem ko ima tip stabilizacije osnovnih surovin v vodi na te parametre le manjši vpliv.

Ključne besede: steatitna keramika; mikrostruktura; dielektrične lastnosti

** Corresponding Author's e-mail: danjela.kuscer@ijs.si*

1 Introduction

Steatite ceramic is alumosilicate that contains approximately 60 % of SiO_2, 30 % of MgO, 5 % of Al_2O_3 and low amounts of oxides such as K_2O, Na_2O, CaO, Fe_2O_3 and TiO_2 originated from impure raw materials. It is characterized by a flexural strength between 110 and 165 MPa, an electrical resistivity of about 10^{11} Ωm at room temperature, a dielectric constant between 5.5 and 7.5 and dielectric losses of about 0.001 [1]. These characteristics and the ability to fabricate final products in a

wide variety of forms, make steatite ceramic attractive in many applications such as high-frequency insulators, appliance insulators, resistor cores, casings for thermostats and fuses.

Steatite ceramic is usually fabricated from natural raw materials, namely talc and clay components, that are wet ground and patterned into a green body by ceramic technologies, examples being dry pressing of spray-dried powder and extrusion or casting of the suspension. After sintering at temperatures between 1250 and 1400 °C, the ceramic contains the grains of Mg-Al-Si-O that crystallise as protoensteatite and a glassy phase, whereas SiO_2 as crystoballite can also be present in small quantities [2,3]. Protoenstatite consists of tetrahedral chains usually of corner-shearing SiO_4 units that are separated by parallel chains of octahedral edge-sharing MO_6 units containing cations such as Mg and Al [4].

The high-temperature orthorhombic protoenstatite phase is prone to transform on cooling into clinoenstatite, a monoclinic phase [5]. The resulting unit volume change of 2.8 % may lead to formation of cracks and thus to deterioration of mechanical properties of the ceramic. The protoenstatite- clinoenstatite phase transformation is prevented when the protoenstatite grains are surrounded by the glassy phase and when the grains are in the micrometre range [1]. Thus, the microstructure of the steatite ceramic has to be homogeneous with micrometre-sized grains.

The microstructure and the phase composition of the steatite ceramic depend on the chemical composition and the morphology of the raw materials, as well as on the processing conditions, such as homogenisation of raw materials, consolidation, temperature and time of firing. The presence of agglomerates in the powder has a detrimental effect on the ceramic since agglomerates either persist during processing or even lead to the formation of new heterogeneities during densification [6]. Agglomerates can be eliminated from the powder by colloidal processing [7]. By controlling the interparticle forces using polyelectrolytes such as ammonium polyacrylate the talc was effectively dispersed in water [8]. After spray-drying and sintering the steatite ceramic was dense and homogeneous.

Electrical properties of steatite ceramics are mostly related to the amount and the composition of the glassy phase [1]. It was shown that the presence of alkalis in the glassy phase increases the electrical conductivity and dielectric losses, while the presence of alkaline earth oxides results in low-loss steatite ceramics [1,9].

In this work we processed the steatite ceramic from talc and clay components stabilized in water electrostatically and electrosterically by polyacrylic acid, respectively. The suspensions were spray-dried and the resulting powder was pressed into powder compacts. They were sintered at 1275 °C and 1300 °C, respectively. The aim of this work was to relate the dielectric permittivity and the dielectric losses of the resulting ceramic to the phase composition, the microstructure and the chemical composition of the phases.

2 Experimental

Talc, clay and dolomite were dispersed in water (Milli Q) without any additive and with polyacrylic acid (PAA, Aldrich) in the amount of 0.3 wt. % per g of the powder. The suspensions had the solid/water mass ratio 33/67. During the mixing of the suspensions with a magnetic stirrer for 2 hours, 0.2 wt. % of polyvinyl alcohol (PVA, Alfa Aesar) and 0.8 wt. % of polyethylene glycol (PEG, Aldrich) were added. Then the suspensions with pH 9 were homogenized in a planetary ball mill (Retsch) for 2 hours at 200 min^{-1}.

The suspensions were spray-dried in a laboratory spray drier (Buechi B-290) in air at 190 °C and 7.5 bar. Powder compacts were prepared from granulated powders. The powders were placed in a steel mold with a diameter of 12 mm and uniaxially pressed at 100 MPa. The samples were then sintered at 1275 °C and 1300 °C, respectively, for 2 h with heating and cooling rates of 5 °C/min. The ceramics prepared from the powder without PAA, sintered at 1275 °C and 1300 °C, were denoted S1275 and S1300, respectively. The ceramics prepared from the powder with PAA, sintered at 1275 °C and 1300 °C, were denoted SA1275 and SA1300, respectively.

The geometrical density of the ceramic samples was calculated from the mass and dimensions of the pellets.

The ceramics were analyzed by X-ray powder diffraction (XRD) at room temperature using a diffractometer (PANalytical, X'Pert PRO MPD, The Netherlands). The data were collected in the 2 θ range from 20 ° to 50 ° in steps of 0.034 °, with an integration time of 100 s. The phases were identified by software X-Pert High Score using the PDF-2 database [10].

The particle size distribution of the powders was measured using a static light-scattering particle size analyser (Microtrac S3500).

For the microstructural analysis the scanning electron microscope (SEM, JSM-5800 JEOL, Japan) equipped with energy dispersive spectroscopy (EDXS, Tracor-Northern) was used. For standardless analysis, the Tracor SQ standardless analysis program, using multiple least-squares analysis and a ZAF matrix correction procedure, was used. The samples were analyzed using an accelerating voltage of 20 kV and a spectra acquisition time of 100 s. The oxygen content in the samples was obtained by difference and is considered in the matrix correction calculations. The estimated error for EDXS analysis is up to 10 % for major elements and up to 30 % for minor elements.

For dielectric investigations, the gold paste (ESL 8884 G) was screen-printed on top- and bottom- surfaces of the samples having a diameter of 11 mm and a thickness of 3 mm. The paste was fired at 900 °C for 10 minutes. The dielectric constant (ε) and dielectric losses (tan δ) were measured at room temperature and frequency of 1 MHz with a Novocontrol Alpha High Resolution Dielectric Analyzer. The amplitude of the probing AC electric signal was 1 V.

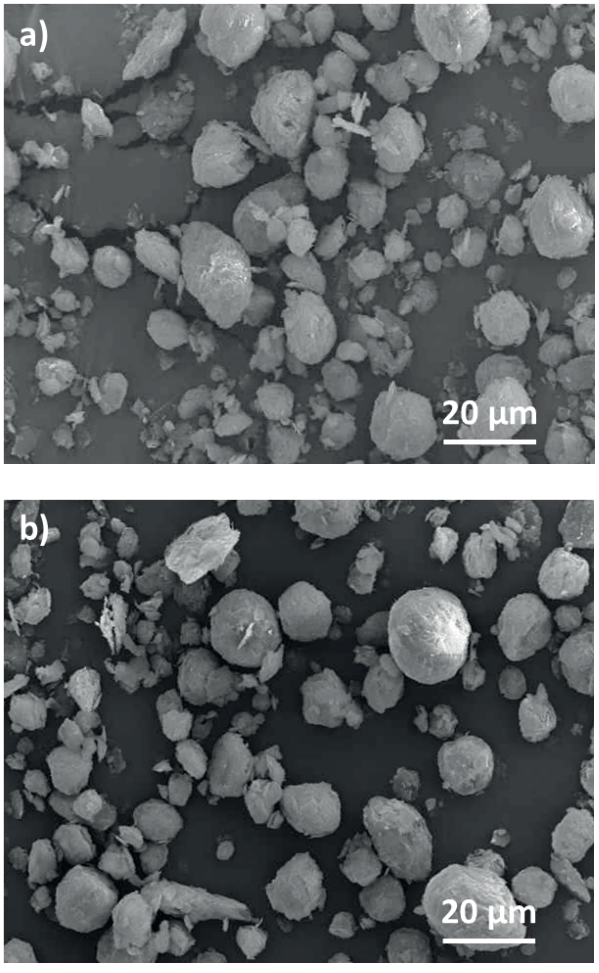


Figure 1: SEM image of the spray-dried powder prepared from the suspension a) without any PAA (G) and b) with PAA (G PAA)

3 Results and discussion

The morphology of the spray-dried powders prepared from suspension without any PAA (denoted G) and with PAA (denoted G PAA) is shown in Figure 1 a and b, respectively,

The morphology of both powders was similar. The granules were roughly spherically shaped with sizes between a few and about 20 µm. The mean granule size d_{v50} measured by the particle size analyzer was 10 µm and 9.9 µm for G and G PAA, respectively. The d_{v90} for both powders was 20 µm.

The XRD spectra of the SA1275, SA1300, S1275 and S1300 ceramic samples are shown in Figure 2.

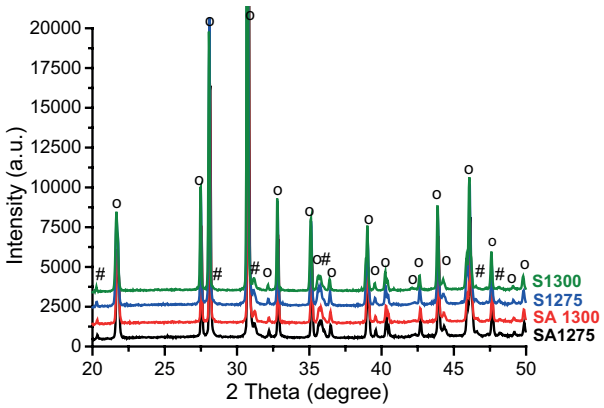


Figure 2: Diffraction spectra of S1275, S1300, SA1275 and SA1300 steatite ceramic. o-protoenstatite, #-cristobalite

All the spectra were similar with the diffraction peaks that corresponded to the orthorhombic protoenstatite phase (PDF 76-1806) and the tetragonal SiO_2 (cristobalite, PDF 76-0941). The main phase was protoenstatite, while the SiO_2 was present in a low quantity. The relatively high background of the spectra indicated that the ceramic contained also some amorphous phase. The intensity of the diffraction peaks and the background were comparable for all the samples, therefore we assume that the amounts of the phases in all the samples were similar.

The cell parameters of the protoenstatite in the S1275, S1300, SA1275 and SA1300 steatite ceramics are shown in Table 1.

Table 1: Cell parameters of protoenstatite $MgSiO_3$ in the S1275, S1300, SA1275 and SA1300 steatite ceramic

	a [nm]	b [nm]	c [nm]
SA 1275	0.9246(1)	0.8746(2)	0.5319(1)
SA 1300	0.9251(1)	0.8750(1)	0.5322(1)
S 1275	0.9247(1)	0.8745(2)	0.5319(1)
S 1300	0.9250(1)	0.8750(2)	0.5321(1)

The cell parameters of the protoenstatite phase in ceramics prepared from the granulated powder without PAA and with PAA depended on the processing temperature and were similar for the samples sintered at 1275 °C (compare S1275 and SA1275) and 1300 °C (compare S1300 and SA1300), respectively. They were in agreement with the protoenstatite unit cell reported in literature [11]. The cell parameters of the protoenstatite sintered at 1300 °C were larger than those of the sample sintered at 1275 °C.

The microstructures of the SA1275, SA1300, S1275, and S1300 ceramic samples are shown in Figure 3. The microstructure of all the samples contains a bright phase (denoted S) and a dark, glassy phase (denoted LP) in addition to pores (P) which is in agreement with the literature [1]. Pores with sizes up to about ten micrometers are homogeneously distributed in the microstructure. The geometrical density of the ceramic was similar for all the samples, 2.77 ± 0.01 g/cm^3.

It is evident that the grains of the bright phase (S) are distributed in the dark, glassy phase The size of the grains ranged from submicrometre to about 5 µm. In some grains we observed cracks. By SEM/EDXS analysis we confirmed that some of the grains with the cracks were SiO_2-rich. It is known that crystaoballite can transform during cooling to quartz with corresponding change in unit cell volume that leads to the formation of intragranular cracks [12]. With XRD analysis we confirmed the presence of cristobalite phase in all ceramic

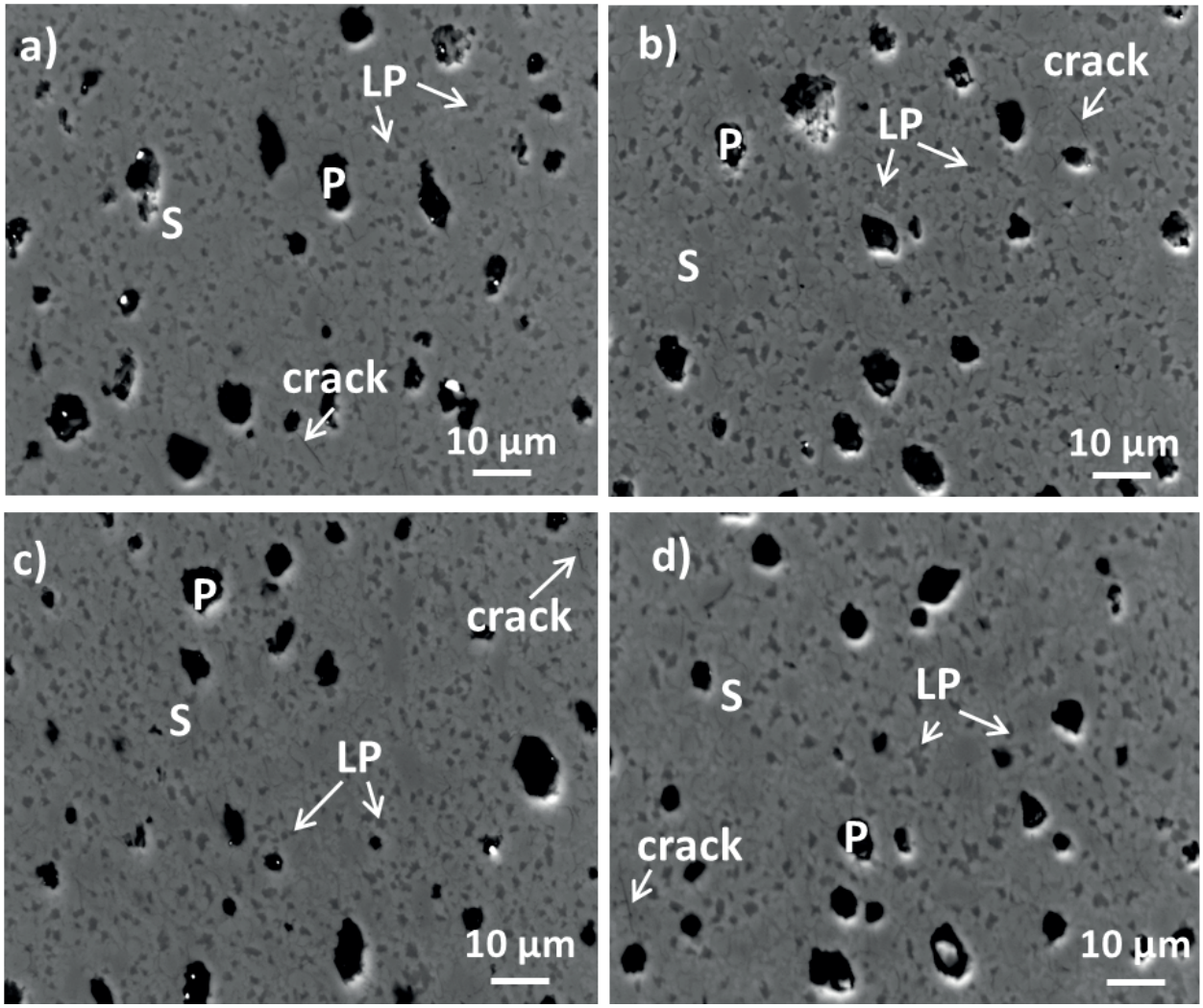


Figure 3: Microstructure of ceramic samples a) SA1275; b) SA 1300; c) S1275; d) S1300.
S = bright phase (steatite), LP = dark phase, P: pores.

samples. The characteristic quartz (101) diffraction peak with the highest intensity at 2 Theta of 26.2 ° was not detected in any of the samples. It is possible that the amount of quartz was below the detection limit of XRD analysis, which is about 2 wt. %. The formation of cracks could also be a consequence of protoenstatite to clinoenstatite phase transformation during cooling and corresponding difference in the unit cell volume [2,[13]]. However we have not detected any monoclinic clinoenstatite phase by XRD. The characteristic clinoenstatite (-2 2 1) diffraction peak with the highest intensity at 2 Theta of 29.75 ° (PDF 75-1406) was not detected in any of the samples (see Figure 2). It is possible that the amount to clinoenstatite was below the detection limit of XRD analysis.

We performed the EDXS analysis of the bright phase (S) and the dark phase (LP) in all the samples. We found out that the composition of the selected phase in the ceramic prepared from the granulated powder without PAA and with PAA was similar, but it varied with the processing temperature. The results of the analysis of the samples SA1275 and SA1300 are presented in Table 2.

Table 2: The composition of the dark (LP) and bright (S) phases in the samples SA1275 and SA1300.

	SA 1275		SA 1300	
	LP [wt. %]	S [wt. %]	LP [wt. %]	S [wt. %]
MgO	14.4 ± 0.7	29.6 ± 1.5	12.8 ± 0.6	31.1 ± 1.5
Al_2O_3	3.6 ± 0.3	3.6 ± 0.3	3.9 ± 0.6	2.8 ± 0.4
SiO_2	79.3 ± 4	64.4 ± 3	80.4 ± 4	63.9 ± 3
CaO	1.9 ± 0.3	1.3 ± 0.2	2.1 ± 0.3	1.3 ± 0.2
Fe_2O_3	0.80 ± 0.12	1.10 ± 0.16	0.80 ± 0.10	0.90 ± 0.13

In the dark and in the bright phases we identified the following elements: Mg, Al, Si, Ca, Fe and O. Concerning the sample sintered at 1275 °C, it is evident that the bright phase (S) contained about 65 % of SiO_2, about 30 % of MgO, 3.6 % of Al_2O_3, 1.3 % of CaO and about 1 % of Fe_2O_3 (all in wt. %). The ratio between SiO_2, MgO and Al_2O_3 corresponded well to that of steatite. On the basis of XRD and EDXS analyses we concluded that the bright phase crystallized in the orthorhombic structure and contained Si-Mg-Al-O protoensteatite phase with minor amounts of Ca and Fe. The presence of CaO and Fe_2O_3 is related to impurities originated from the natural raw materials.

The dark phase (LP) contained a higher amount of SiO_2, about 80 % and a lower amount of MgO, about 14 %, while the amounts of Al_2O_3, CaO and Fe_2O_3 were similar.

The chemical composition of the bright phase slightly changed after sintering at 1300 °C. The amount of MgO increased, while the amounts of Al_2O_3 and SiO_2 decreased. A higher amount of Mg^{2+} with ionic radius r = 0.072 nm [[14]] and a lower amount of Si^{4+} (r = 0.026 nm) [12] and Al^{3+} (r = 0.039 nm) [12] may result in larger unit cell at 1300 °C which is consistent with the calculated lattice parameters of the protoensteatite (Table 1).

The dark phase (LP) contained in a sample sintered at 1300 °C less MgO and more SiO_2, while the amounts of Al_2O_3, CaO and Fe_2O_3 were similar to that in sample sintered at 1275 °C.

The dielectric constant ε and the dielectric losses of the S1275, S1300, SA1275 and SA1300 samples measured at room temperature are presented in Table 3.

Table 3: Dielectric constant ε and the dielectric losses tan δ of the S1275, S1300, SA1275 and SA1300

	ε (1 MHz)	tan δ (1 MHz)
SA1275	8.42	0.002
SA1300	5.5	0.003
S1275	7.74	0.001
S1300	4.6	0.002

The dielectric constants of the samples sintered at 1275 °C were higher than of those sintered at 1300 °C. This could be related to the chemical composition of the steatite ceramic which depends on the processing temperature.

The dielectric constant of the steatite $MgSiO_3$ with the density of 93 % is 6.2 [[15]]. The dielectric constants of MgO and Al_2O_3 are similar, 9.8 and 10, respectively, while the dielectric constant of SiO_2 is 4. It was reported that the properties of the steatite ceramic depend mostly on the composition of the glassy phase [1]. From the results it is evident that at 1300 °C the liquid phase contained more SiO_2 and less MgO than at 1275 °C. A higher amount of SiO_2 with a low dielectric constant and a low amount of MgO with a high dielectric constant decreased the dielectric constant of the glassy phase. Consequently the dielectric constant of the steatite ceramic processed at 1300 °C was lower than that at 1275 °C.

4 Conclusions

Aqueous suspensions of talc/clay/dolomite mixtures stabilized electrostatically and electrosterically with polyacrylic acid at pH 9 have been prepared in a solid load of 33 wt. %. After spray-drying the powder contained spherically shaped granules with sizes between a few and about 20 μm. The powder compacts were

sintered at 1275 °C and 1300 °C. The microstructures of all the steatite ceramics were homogeneous and contained protoenstatite grains surrounded with a glassy phase together with a low amount of crystobalite and some pores.

The dielectric constant was about 5 and about 8 for the ceramics sintered at 1300 °C and 1275 °C, respectively, while the dielectric losses were between 0.001 and 0.003. The values of the dielectric constant were related to the chemical composition of the glassy phase that contained more SiO_2, less MgO and similar amounts of Al_2O_3, CaO and Fe_2O_3 after sintering at 1300 °C. A higher amount of SiO_2 with the dielectric constant of about 4 and a lower amount of MgO with the dielectric constant of about 10 contributed to a lower dielectric constant of the steatite ceramics.

5 Acknowledgments

Ministry of Education, Science and Sport of Slovenia is acknowledged for the financial support through the project Raziskovalci na začetku kariere-2013-IJS-726 (OP13.2.1.8.01.0014). This work was supported also by the Slovenian Research Agency (P2-0105).

The authors would like to thank to Jana Cilenšek and Silvo Drnovšek for technical assistance and dr. Mateja Podlogar for spray driying experiments.

6 References

1. W. D. Kingery, H. K. Bowen, D. R. Uhlmann, "Introduction to ceramic", John Wiley&Sons, 1976.
2. W. Mielcarek, D. Nowak-Wozny, K. Prociow, "Correlation between $MgSiO_3$ phases and mechanical durability of steatite ceramics", J. Eur. Ceram. Soc., vol. 24, pp. 7813-3821, 2004.
3. F.A.C. Oliveira A. Ferreira, J.R. Domingues, J. C. Fernandes, D Dias, "The role of talc in preparing steatite slurries suitable for spray-drying", J. Mat. Res., vol. 101, pp. 1272-1280, 2010.
4. R. T. Downs, "Topology of the pyroxenes as a function of temperature, pressure and compositions as determines from the procrystal electron density". Am. Minerologist., vol. 88, pp. 556-566, 2003.
5. H. Yang, S. Ghose, "High temperature single crystal X-ray diffraction studies of the ortho-proto phase transition in enstatite, $Mg_2Si_2O_6$ at 1360 K". Phys. Chem. Minerals., vol. 22, pp. 300-310, 1995.
6. F. F. Lange, "Powder processing science and technology of increasing reliability". J. Am. Ceram. Soc., vol. 72, no. 2, pp 3-15, 1989.
7. J. J. Lewis, "Colloidal Processing of Ceramics", J. Am. Ceram. Soc., vol. 83, no. 10, pp. 2341–2359, 2000.
8. F. A. C. Oliveira, A. Ferreira, J. R. Domingues, J. C. Fernandes, D. Dias, "The role of talc in preparing steatite slurries suitable for spray-drying". Int. J. Mat. Res., vol. 101, pp. 1272-1280, 2010.
9. H. F. G. Ueltz, "Crystallin and glassy phases of steatite dielectrics", J. Am. Ceram. Soc., vol. 27, no. 2, pp. 33-39, 1944.
10. International Centre for Diffraction Data. PDF-ICDD, PCPDFWin Version2.2. June 2001. 2002:Newtown Square, PA.
11. H. Yang, S. Ghose, "High temperature single crystal X-ray diffraction studies of the ortho-proto phase transformation of enstatite, $Mg_2Si_2O_6$ at 1360 K." Phys. Chem. Minerals, vol. 22, pp. 300-310, 1995.
12. E. Ringdalen, Changes in quartz during heating and the possible effects on Si production, JOM, Vol. 67, No. 2, pp. 484-492, 2015
13. J. R. Smyth, Experimental study on polymorphysm of enstatite, American Minerologyst, vol. 59, pp 345-352, 1974.
14. R. D. Shannon, C. T. Prewitt, »Effective Ionic Radii in Oxides and Fluorides«, Acta Cryst., B25, pp. 925-946, 1969.
15. M-E. Song, J-S. Kim, M-R Joung, S. Nahm, Y-S. Kim, J-H. Paik B-H. Choi, "Synthesis and microwave dielectric properties of $MgSiO_3$ ceramics", J. Am. Ceram Soc., vol. 91, no. 8, pp. 2747–2750, 2008.

Arrived: 12. 05. 2016
Accepted: 25. 07. 2016

Original scientific paper

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 2(2016), 106 – 108

Doktorske disertacije na področju mikroelektronike, elektronskih sestavnih delov in materialov v Sloveniji v letu 2015

Doctoral theses on Microelectronics, Electronic Components and Materials in Slovenia in 2015

Univerza v Ljubljani / University of Ljubljana

Fakulteta za elektrotehniko / Faculty of Electrical Engineering

1	Avtor Author	Iztok Bratuž
	Naslov	**Optimizacija protokolov samodejnih brezstičnih sistemov za identifikacijo oseb in predmetov**
	Title	Optimisation of protocols for automated contactless systems for person and object identification
	Mentor Supervisor	izr. prof. dr. Andrej Trost
2	Avtor Author	Jure Močnik
	Naslov	**Nizkonapetostna arhitektura za upravljanje pametnih omrežij**
	Title	Low voltage architecture for smart grid management
	Mentor Supervisor	prof. dr. Andrej Žemva
3	Avtor Author	Sebastjan Šlajpah
	Naslov	**Nosljivi senzorni sistem za merjenje in ocenjevanje vstajanja**
	Title	Wearable sensory system for measurement and evaluation of sit-to-stand movements
	Mentor Supervisor	prof. dr. Roman Kamnik
4	Avtor Author	Martin Sever
	Naslov	Optimizacija hrapavosti spojev v tankoplastnih silicijevih sončnih celicah s tridimenzionalnim optičnim modeliranjem in simulacijami
	Title	**Optimisation of interface textures in thin-film silicon solar cells aided by three-dimensional optical modelling and simulations**
	Mentor Supervisor	prof. dr. Janez Krč

5	Avtor / Author	Gašper Matič		
	Naslov	**Razvoj elektronskega sistema za upravljanje vsevrtečega brezpilotnega letala**		
	Title	Development of electronic control systems for all-rotating unmanned aerial vehicle		
	Mentor / Supervisor	doc. dr. Marko Jankovec		

6	Avtor / Author	Uroš Puc		
	Naslov	Spektroskopsko teraherčno slikanje		
	Title	**Spectroscopic terahertz imaging**		
	Mentor / Supervisor	prof. dr. Anton Jeglič	Somentor / Co-Supervisor	prof. dr. Gintaras Valušis

Univerza v Mariboru / University of Maribor

Fakulteta za elektrotehniko, računalništvo in informatiko / Faculty of Electrical Engineering and Computer Science

1	Avtor / Author	Tine Konjedic
	Naslov	**Soft switching for improving the efficiency and power density of a single-phase converter with power factor correction**
	Title	Uporaba tehnike mehkega preklapljanja za izboljšanje učinkovitosti in povečanje gostote moči enofaznega pretvornika s korekcijo faktorja moči
	Mentor / Supervisor	prof. dr. Miro Milanovič

2	Avtor / Author	Lucijan Korošec
	Naslov	**Pulzno gostotno moduliran mikrorazsmernik z aktivnim razklopitvenim tokokrogom**
	Title	Pulse density modulated microinverter with active decoupling circuit
	Mentor / Supervisor	prof. dr. Miro Milanovič

3	Avtor / Author	Lovro Belak		
	Naslov	**Strateško vzdrževanje prenosnih naprav s stališča zanesljivosti in tveganja**		
	Title	Strategic maintenance of high voltage equipment from the point of reliability and risk		
	Mentor / Supervisor	prof. dr. Jože Pihler	Somentor / Co-Supervisor	prof. dr. Josip Voršič

Mednarodna podiplomska šola Jožefa Stefana / Jožef Stefan International Postgraduate School

1	Avtor / Author	Gregor Filipič		
	Naslov	Plazemska sinteza kovinsko-oksidnih nanožic in njihova uporaba		
	Title	**Plasma synthesis of metal-oxide nanowires and their application**		
	Mentor / Supervisor	prof. dr. Uroš Cvelbar		
2	Avtor / Author	Andrej Kovič		
	Naslov	Sinteza in karakterizacija nanožic in nanocevk na osnovi molibdena		
	Title	**Synthesis and characterization of molybdenum based nanowires and nanotubes**		
	Mentor / Supervisor	dr. Aleš Mrzel		
3	Avtor / Author	Raluca-Camelia Frunza		
	Naslov	Tanke plasti dielektrikov na osnovi tantalovega oksida s sintezo iz raztopine in njihova uporaba v transparentni elektroniki		
	Title	**Solution-derived dielectric tantalum-oxide-based thin films and their applications in transparent electronics**		
	Mentor / Supervisor	prof. dr. Barbara Malič		
4	Avtor / Author	Jernej Pavlič		
	Naslov	Optimizacija pogojev priprave debelih plasti kalijevega natrijevega niobata ter njihov elektromehanski odziv		
	Title	**Optimization of the processing of potassium sodium niobate thick films and their electromechanical behavior**		
	Mentor / Supervisor	doc. dr. Tadej Rojac	Somentor / Co-Supervisor	prof. dr. Barbara Malič

Bold font is used for the original title of the thesis (and language in which the thesis is written), normal font for title translation.

Informacije MIDEM
Journal of Microelectronics,
Electronic Components and Materials
Vol. 46, No. 2(2016), 109 – 109

MIDEM 2016

52nd INTERNATIONAL CONFERENCE ON MICROELECTRONICS, DEVICES AND MATERIALS WITH THE WORKSHOP ON BIOSENSORS AND MICROFLUIDICS

MIDEM

Announcement and Call for Papers

September 28th – 30th, 2016
Ankaran, Slovenia

ORGANIZER: MIDEM Society - Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia

CONFERENCE SPONSORS: Slovenian Research Agency, Republic of Slovenia; IMAPS, Slovenia Chapter; IEEE, Slovenia Section; Zavod TC SEMTO, Ljubljana.

GENERAL INFORMATION
The 52nd International Conference on Microelectronics, Electronic Components and Devices with the Workshop on Biosensors and Microfluidics continues a successful tradition of the annual international conferences organised by the MIDEM Society, the Society for Microelectronics, Electronic Components and Materials. The conference will be held at **Hotel Convent, Ankaran, Slovenia**, well-known resort and conference centre, from **SEPTEMBER 28th – 30th, 2016**.

Topics of interest include but are not limited to:
- Workshop focus: Biosensors and Microfluidics
- Novel monolithic and hybrid circuit processing techniques,
- New device and circuit design,
- Process and device modelling,
- Semiconductor physics,
- Sensors and actuators,
- Electromechanical devices, Microsystems and nanosystems,
- Nanoelectronics
- Optoelectronics,
- Photonics,
- Photovoltaic devices,
- New electronic materials and applications,
- Electronic materials science and technology,
- Materials characterization techniques,
- Reliability and failure analysis,
- Education in microelectronics, devices and materials.

ABSTRACT AND PAPER SUBMISSION:
Prospective authors are cordially invited to submit up to 1 page abstract before **May 1st, 2016**. Please, identify the contact author with complete mailing address, phone and fax numbers and e-mail address.
After notification of acceptance (**June 15th, 2016**), the authors are asked to prepare a full paper version of six pages maximum. Papers should be in black and white. Full paper deadline in PDF and DOC electronic format is: **August 31st, 2016.**

IMPORTANT DATES:
Abstract deadline: **May 1st, 2016** (1 page abstract or full paper)
Notification of acceptance: **June 15th, 2016**
Deadline for final version of manuscript: **August 31st, 2016**

Invited and accepted papers will be published in the conference proceedings.

Deatailed and updated information about the MIDEM Conferences is available at
http://www.midem-drustvo.si/ under Conferences.

Boards of MIDEM *Society* | *Organi društva* MIDEM

MIDEM *Executive Board* | *Izvršilni odbor* MIDEM

Supervisory Board | Nadzorni odbor

Court of honour | Častno razsodišče

Informacije MIDEM
Journal of Microelectronics, Electronic Components and Materials
ISSN 0352-9045

Publisher / Založnik:
MIDEM Society / Društvo MIDEM
Society for Microelectronics, Electronic Components and Materials, Ljubljana, Slovenia
Strokovno društvo za mikroelektroniko, elektronske sestavne dele in materiale, Ljubljana, Slovenija

www.midem-drustvo.si