CHALLENGING ISSUES IN ELECTRONIC TESTING

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Key words: test, diagnosis, nano-scale systems, thermal-aware test, SiP test

Abstract: This editorial note summarizes the topics of the Workshop on Electronic Testing, Bled, Slovenia, September 13, 2007. The workshop gathered participants from seven European countries presenting papers on their current research in the areas of digital, sensor and mixed-signal test. Testing, debugging and diagnosing nano-scale systems, thermal-aware SoC testing and system-in-package test were hot topics covered by the invited papers.

Sodobni izzivi na področju testiranja elektronskih vezij in sistemov

Kjučne besede: testiranje, diagnostika, nano sistemi, testiranje ob upoštevanju energijske uporabe, testiranje sistemov integriranih na nivoju sestavov

Izvleček: V okviru 43. mednarodne konference MIDEM je bila 13.septembra 2007 na Bledu organizirana delavnica o testiranju elektronskih vezij in sistemov. Udeleženci iz sedmih evropskih držav so predstavili svoje raziskovalne rezultate s področja testiranja digitalnih vezij, senzorjev in mešanih analogno digitalnih vezij. Vabljena predavanja so osvetlila aktualne probleme testiranja in diagnosticiranja vezij izdelanih s sodobnimi nano-tehnološkimi postopki, testiranja ob upoštevanju energijske porabe ter testiranja sistemov integriranih na nivoju sestavov (angl. System-in-Package, SiP).

Nowadays, electronic testing is addressing challenging problems of providing high-quality cost-effective tests coping with ever-increasing design complexity of modern electronic devices. Increased interest in the above problems and the growing needs for practical solutions led to the decision of the programming committee of the International Conference on Microelectronics, Devices and Materials to host a workshop on this topic in the frame of the 43rd International Conference MIDEM 2007. According to the established practice, special issue of "Informacije MIDEM" is devoted to the key points of the event. This issue features, among others, invited papers from the resulting Workshop on Electronic Testing, Bled, Slovenia, September 13, 2007, The workshop gathered participants from seven European countries presenting papers on their current research in the areas of digital, sensor and mixed-signal test. Testing, debugging and diagnosing nano-scale systems, thermal-aware SoC testing and system-in-package test were hot topics covered by the invited papers.

In the nanometer domain, fabrication defects, variations in device parameters and coupling effects in the interconnect impact the device behavior and produce significant variability in timing, drive, leakage, and so forth. Instead of determinism and static analysis employed so far, the new design process is increasingly becoming subject of statistical variation, which consequently calls for a new paradigm in verification and test. As robust design becomes mandatory to ensure fail safe operation and acceptable yields, design robustness invalidates many traditional test approaches. The new test solutions should also incorporate verification of robustness properties. The RealTest Project presented by the first invited speaker Sybille Hellebrand addresses the problems of robust design and associated efficient test procedures. The need of new fault models comprising statistical profiles of circuit parameters and conditions for fault detection is demonstrated in the case study of single event transients in random logic. In contrast to the traditional transient current model a refined model (also referred to as UGC model) is proposed more closely focusing on the impact of a single event transient (SET) on a pn-junction. The analysis of the impact of UGC model based on the simulations of a set of finite state machine benchmarks with randomly injected SET in the combinational logic have shown that longer duration of glitches is likely to affect the behavior of the circuit and should therefore be considered in both system design and test.

Fault diagnosis of electronic systems has been a challenge for decades. From the early 70s marked by the fundamental reference Fault diagnosis of digital systems authored by H.Y.Chang, E.Manning and G.Metze, technology made tremendous progress while theoretic fault diagnosis principles remained basically unchanged. Emerging nano-scale systems on chip make debug and diagnosis a complicated and difficult task /1/. Establishing good quality control and improvement over the whole system life cycle necessitates alternative descriptions and treatment of er-

rors in individual steps of the life cycle, points out Hans-Joachim Wunderlich in his invited paper. New approaches are needed for description of effects originating from defects in nano-scale technologies. While in the past, fault detection and location were considered two distinct steps for achieving diagnosis, in very deep submicron technology their roles are indivisible and very demanding. Diagnostic resolution is determined by the test set, hence diagnostic ATPG focused on fault localization may lead to more precise localization of defects. Adaptive diagnosis approach described in the paper by an illustrative example gives encouraging results. Design for debug and diagnosis (DDD) is the next obvious step to increase diagnostic resolution in practice. Major problems to be overcome by DDD are highlighted in the paper with some more detailed discussion related to compaction techniques and trace buffers.

Full-scan methodology supported by Automatic Test Pattern Generation (ATPG) is a widely adopted test strategy for testing integrated circuits. In this approach, considerable peak power occurs periodically at the capture cycles during input application and result capturing. Excessive test power dissipation may permanently damage a circuit under test or reduce its reliability. High temperature has become a technological barrier to the testing of high performance SoC, especially when deep submicron technologies are employed. In his invited paper, Zebo Peng discusses several issues related to the thermal problem during SoC testing. In the following, he presents a thermal-aware SoC test scheduling technique to generate the shortest test schedule such that the temperature constraints of individual cores and the constraint on the test-bus bandwidth are satisfied. The idea is to partition the entire test set into a number of test sub-sequences and to introduce a cooling period between two consecutive test sub-sequences in order to avoid overheating. Since long cooling periods may substantially increase test time some additional test scheduling heuristics have been developed and are presented in the paper. Comparison of different strategies given in the experimental case study demonstrates the advantages of the developed test scheduling heuristics.

According to the definition given by the International Electronics Manufacturing Initiative (iNEMI) /2/ "System in Package (SiP) is characterized by any combination of more than one active electronic component of different functionality plus optionally passives and other devices like MEMS or optical components assembled preferred into a single standard package that provides multiple functions associated with a system or sub-system". (SiP) design is gaining importance because it can provide a number of advantages over SoC in specific areas such as high-performance consumer electronics or mobile phones. Its design inherently poses problems of testing due to a broad mix of process technologies, different types of interconnections and 3-D stacked IC. In presenting design and test issues of SiP, Michel Renovell first outlines quality concerns for achieving the required acceptable yield (e.g., known good die concept). Next, problems related to bare-die testing are addressed. New probing techniques developed due to the limitations of traditional cantilever probe card technology are summarized. Challenges in system test imposed by RF, analog and MEMS components are described in the last part of the paper. Since mixed-signal and RF test requires expensive test instrumentation alternative test solutions such as built-in self-test or signal transformations from analog to digital domain are often preferred. Initiative for setting up a SiP test standard similar to IEEE Std 1149.1 or IEEE Std 1500 is discussed.

The Workshop on Electronic Testing brought together participants from both industry and academia providing a forum for the exchange of ideas and dissemination of research results. Since this was the first workshop on testing organized in Slovenia it had also the goal of identifying local groups and individuals working on test and establishing close contacts among them. ETTTC (IEEE European Test Technology Technical Council) /3/ fosters national activities and encourages test society to joint collaboration. An example of successful joint collaboration has been the European IST project EuNICE-Test (European Network for Initial and Continuing Education in VLSI/SOC Testing using remote automatic test equipment (ATE)), /4/, addressing the shortage of skills in the microelectronics industry in the field of electronic test. In this project, 4 academic centres: Universitat Politčcnica de Catalunya, Spain, Politecnico di Torino, Italy, University Stuttgart, Germany and Jožef Stefan Institute Ljubljana, Slovenia, joined the existing network accessing remote test facilities (Agilent 83000 F330t ATE for testing digital and mixed-signal integrated circuits) located at CRTC in Montpellier. Established links offer opportunities for future collaboration including exchange of information, consulting, joint experimental work of Ph.D. thesis up to bilateral research projects and EC projects.

References

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