SiGe-HETEROJUNCTION BIPOLAR TRANSISTORS: KEY TECHNOLOGIES AND APPLICATIONS IN COMMUNICATION SYSTEMS

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Abstract: The SiGe HBT is attractive for future broadband and wireless communication ICs owing to its outstanding performance and from the fabrication point of view (fabrication costs ≈ 0.25 x GaAs and 1.3 x Si). Most processes of main-stream Si technology can be utilized for integration of the HBT on Si substrates. This is due to the similar chemical and physical behaviors of Si and SiGe with respect to reactive ion etching, low ohmic contact systems, isolation and passivation. Thus, several groups have integrated the SiGe-HBT in standard Bipolar and BiCMOS technologies using differential or selective Si/SiGe/Si-epitaxy. Others use blanket epitaxy of the Si/SiGe/Si layers to benefit from an easy technology to eliminate influences of the isolation oxide on the growth and doping, and to allow an easy characterization of the material including the doping profile with global physical diagnostic methods. In addition, there is a simple and low cost fabrication technology using blanket epitaxy and double mesa integration, which has led to several records of SiGe-HBTs in high-frequency (f_T=116 GHz, f_{max}=160 GHz) and noise data (F_{min} (at 2 GHz)<0.5 dB, F_{min} (at 10 GHz) <1 dB, F_C ≈ 100 - 2000 Hz).

SiGe heterospojni bipolarni tranzistorji: Ključne tehnologije in uporaba v komunikacijskih sistemih

Ključne besede: polprevodniki, naprave polprevodniške, Si-Ge HBT transistorji bipolarni heterospojni, tehnologije ključne, aplikacije praktične, sistemi komunikacijski, IC vezja integrirana, frekvence visoke f_{max} = 160 GHz, število šumno <0,5 dB (pri f = 2 GHz), upori električni, induktorji električni, induktorji električni spiralni, kondenzatorji električni, MMIC vezja integrirana monolitska mikrovalovna

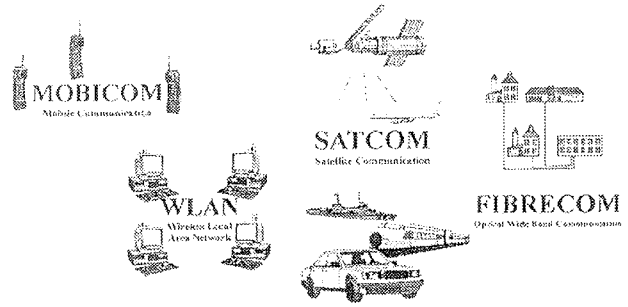
Povzetek: SiGe heterospojni bipolarni tranzistor (SiGe HBT) je privlačen element za bodoča integrirana vezja za brezžične in širokopasovne komunikacije predvsem zaradi izrednih lastnosti in kompatibilnosti z obstoječo proizvodnjo (cena izdelave ≈ 0.25 GaAs in 1.3 Si). Večino korakov glavne Si tehnologije lahko uporabimo za integracijo HBT na silicijeve substrate. To je možno predvsem zaradi podobnega kemičnega in fizikalnega obnašanja Si in SiGe glede na reaktivna ionska jedkanja, nizkoomske kontaktne sisteme ter glede na tehnike izolacije in pasivacije. Tako je že večim skupinam uspelo integrirati SiGe HBT v standardne bipolarne in BiCMOS tehnologije z uporabo diferencijalne ali selektivne Si/SiGe/Si epitaksije. Drugi zopet uporabljajo slepi nanos Si/SiGe/Si plasti, kar je enostavnejše, saj se ognemo vplivom izolacijskega oksida na rast in dopiranje in nam to hkrati omogoča lažje vrednotenje nanešenih plasti, vključujoč meritev koncentracijskega profila z globalnimi fizikalnimi diagnostičnimi metodami. Nadalje, obstaja dokaj enostavna in poceni tehnologija, ki uporablja slepi nanos epi plasti in dvojno mesa strukturo, s pomočjo katere je bilo do sedaj izdelano več visokofrekvenčnih SiGe HBT tranzistorjev (f_T = 116 GHz, f_{max} = 160 GHz) z ustreznimi šumnimi lastnostmi (F_{min} (pri 2 GHz) < 0.5 dB, F_{min} (pri 10 GHz) <1 dB, F_C ≈ 100 - 2000 Hz).

1. Introduction

For the steadily increasing communication market the acceptance of new communication services depends on the costs of the terminals. Low cost and high performance chip sets are needed. SiGe heterojunction bipolar transistors (SiGe-HBTs) meet these requirements since a few years. SiGe/Si offers high speed, low noise, high power, low power consumption and cost effective production in existing Si-lines. Consequently SiGe heterodevices are for the high volume market and should be produced by large chip manufacturers. Indeed, companies like IBM, Siemens, NEC, Philips and Temic (a company of Daimler-Benz) are active in SiGe. It was the early pioneering activities and results of IBM and AEG Telefunken (later belonging to Daimler-Benz) that have stirred up the interest of others. From year to year the SiGe community becomes larger.

The high volume market for these SiGe hetero-chips can be divided into four segments represented by their operation frequency (Fig. 1). The mobile communication (1-2 GHz), wireless local area network (2.4-5.8 GHz), satellite communication (10.7-14.5 GHz) and the wide-band communication via cable or optical fibre (3-40 Gbit/s) are united to communication networks offering numerous services such like private/business contacts, entertainment music/video, telecommuting,

telemedicine, distance learning, fabrication robot check, workforce training, Internet, interactive/multmedia video, disaster management, mailbox/messaging, interactive home banking/shopping, goverment services, wireless scientific backdone collaborative groupwork, etc.



MOBICOM	WLAN	SATCOM	FIBRECOM
1-2 GHz	2.4-5.8 GHz	10.7-14.5 GHz	3-40 Gbit/s

Fig.1: Scenario: SiGe-HBTs for communication markets.

1.1 SiGe-HBT integration into the Si standard technology

Since the discovering of the bipolar transistor by W. Shockley, J. Bardeen und W. Brattain in the year 1947 the technological evolution mainly concerned the following topics: the implantation and the base epitaxy improved the internal transistor, whereas the trench isolation reduced the parasitic collector-substrate-capacitance and increased the package density /1-3/. The novel double polysilicon technology was an innovative technique to optimize the lateral and vertical transistor. The emitter efficiency increased and the self-aligment of the emitter to the base contacts reduced the emitter-base and base-collector-capacitance. The lateral scaling of the bipolar transistor was supported by the shrinking of the minimum feature size driven by the mainstream technologies (DRAMs, CMOS-logic). The vertical optimization of the bipolar transistor was dominated by the reduction of the base width, because the transit time is one of the most important factors determining the speed of bipolar circuits and is in first-order calculation proportional to the square of the base width /6/.

When reducing the base width in bipolar transistors there are some physical constraints to be considered. Since punchthrough between emitter and collector must be avoided, a reduction of the base width must be accompanied by a corresponding increase in maximum base doping concentration N_A. However, a limit is set by trap-assisted forward tunnelling in the emitter-base-junction, which leads to strongly nonideal behaviour of the base current at large values of N_A, a reduction of the current gain, and an increase of the emitter transit time and the emitter-base-capacitance.

These drawbacks of a conventional silicon homojunction bipolar transistor (BJT) can be overcome by the HBT with an epitaxial silicon-germanium alloy narrow-gap base region. It offers the possibility of decoupling a reasonable current gain and a low base resistance leading to an independent adjustment of emitter and base doping /4,5/. The current gain itself is much higher due to the B/E heterojunction, which allows an increased base doping and a thinner base to get the same current gain β compared with Si. Because of the thin base SiGe-HBTs exhibit a very low transit time τ_F. In addition the optimization of the lateral structure is a very important issue for improving device performance for low power and low noise applications. This is because lateral scaling means the reduction of parasitic components of the extrinsic transistor, which slow down the intrinsic transistor and dissipate power.

The first SiGe-HBT was realized in the year 1987 by S.S. Iyer /7/, when III/V-HBTs were standard devices at this time. The main difficulties were related to the growth of pseudomorphic SiGe-layers, because of the lattice mismatch of SiGe and Si /8/. The mechanical stress in the pseudomorphic SiGe base increases with the Ge content and the SiGe layer thickness. The Ge content is limited and the thermal budget has to be low to prevent the relaxation and the boron outdiffusion of the SiGe base. In early years simple double mesa transistor structures were used for electrical characterisation of the Si/SiGe/Si layers /7,9-12/. These structures allowed a fast and simple processing at low temperatures.

Basically the SiGe-HBT is a new version of the Si-BJT now having an optimized vertical structure. From the fabrication point of view, one major advantage of an HBT on a Si substrate is the utilization of most processes of mainstream Si technology for the integration. This is due to the fact that Si and Ge have similar chemical and physical behaviour with respect to reactive ion etching, low ohmic contact systems, isolation and passivation, the precondition for a seamless transfer of this novel device into standard Si-production lines /14,16,17,22, 25,52-54/.

Si/SiGe/Si-epitaxy

Different to Si-BJTs the Si/SiGe/Si-epitaxy is a new central process step, which must fullfil the following points in correlation with the integration concept: (1) Reproducible control of the n- and p-doping and gradients and the Ge content, (2) good homogeneity of these parameters and sufficient throughput, (3) high interface and crystal quality at a low contamination level (e.g. metals, C, O, B,..), (4) low temperature epitaxy (<800°C) to minimize the boron outdiffusion and the SiGe relaxation and (5) the possibility for blanket, differential and selective epitaxy. Solid source MBE /7,9-15/, gas source MBE /16/ or CVD in different process windows (UHVCVD /17,18/, APCVD /19/, RTCVD /20,21,53/, LPCVD /22,23,52,54/ or LRP /24/) are used for the definition of the vertical SiGe-HBT profile. Because of its high flexibility MBE is used in research, whereas CVD is used in the production lines due to its higher throughput.

There are three basic Si/SiGe-HBT fabrication concepts which differ in the position of the SiGe-base epitaxial growth within the process flow (see Fig.2). The epitaxial growth within the field oxide windows and polycrystalline layer outside is called differential epitaxy. Selective epitaxy is a monocrystalline deposition only in the field oxide windows. The blanket epitaxy (homogenious epitaxial Si/SiGe/Si growth on the whole Si substrate) seems to have some advantages: There is no influence of the isolation oxide on growth and doping, and the material parameters can be characterized with global physical diagnostic methods (SIMS, SNMS, x-ray, optical methods). The differential epitaxy (**A2**) is used by most production lines (e.g. IBM /17/, NTT /16/, DBAG/TEMIC /14/, Motorola /22/, AT&T (Lucent Technology) /53/). While NEC /25/, Siemens /52/, Philips /54/ and HP /23/ focus on the selective epitaxy (**A3**). The research centers prefer the SiGe blanket epitaxy (e.g. /10-12,15,20, 26-29/). The integration of the SiGe-HBT into a Si BiCMOS technology was shown by IBM /30/ (**A2**) and NEC /31/.

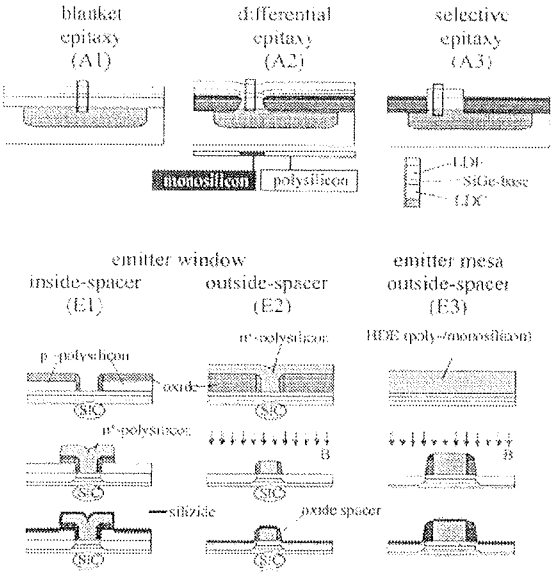


Fig.2: The different concepts for the integration of the Si/SiGe/Si-epitaxy and the emitter constructions.

Emitter definition

After the low-doped collector (LDC)/SiGe-base/low doped emitter (LDE) epitaxy, the emitter can be definied using inside- or outside-spacer- polysilicon technology (see **E1**, **E2** and **E3** in Fig. 2). The outside-spacer structure can be generated by a polysilicon deposition or monocrystalline high-doped emitter (HDE) epitaxy followed by a mesa etching (**E3**).On the other hand an oxide hole filled with polysilicon can be planarized (**E2**). For **E1** und **E2** the emitter width can even become smaller than the minimum feature size using an oxide inside-spacer. In addition the integration of the SIC (**S**elective **I**mplanted **C**ollector) can easily be realized by the self-aligned implantation through the emitter window. **E1** and **E2** dominate in the SiGe-IC technology (e.g. IBM /19/, NTT /16/, NEC /25/, Motorola /22/, DBAG/TEMIC /54/, AT&T (Lucent Technology) /53/, Siemens /52/, Philips /54/ and HP /23/).

Base contact

The three HBT versions A1-A3 have different contacts to the exstrinsic base (Fig. 3). In the differential SiGe-HBT **A2** the polycrystalline layer on the field oxide regions acts as a lateral base contact with the smallest contact resistance between the mono- and polycrystalline silicon. The selective SiGe-HBT **A3** utilizes the conventional double polysilicon technology with a negligible contact resistance between the monocrystalline extrinsic base and the deposited B-doped polysilicon. A further reduction of the external base resistance can be achieved either by an additional B implantation /17, 45/, a low ohmic salicide /53, 32/ or a selective deposited metal /16/.

For the blanket double mesa SiGe-HBT a significant reduction of parasitic resistances and capacitances can be achieved by using additional self-aligning processes like planarization for transistor contacts and outside-spacer-technology for micromasking /55, 56/. The size of the base-collector area depends strongly on the integration concept. For **A2** /14,16,17/ the area can be minimized owing to the sidewall contacted base. In **A1** and **A3** a defined parasitic base contact area remains /10,12,25,26,56/. Sophisticated concepts for self-aligned lateral base contact of Si-BJTs /50,51/ are not useable for the SiGe-HBT.

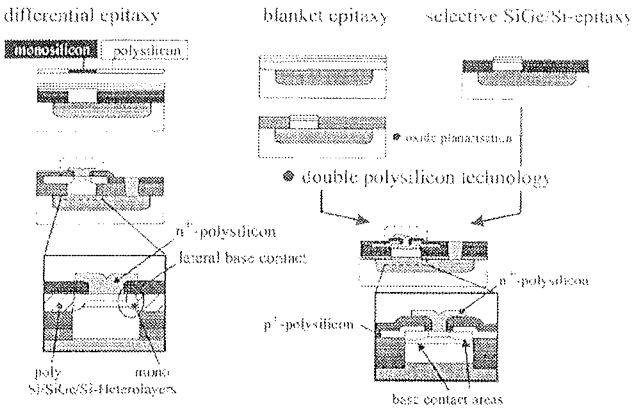


Fig.3: Optimization of the base contact and the parasitc base-collector-area in correlation with the integration of the SiGe epitaxy.

2. Experimental results

(a) SiGe-HBT

A non-passivated and non-implanted double mesa HBT can quickly be processed. The zero thermal budget processing prevents any outdiffusion of the boron doping profile and any SiGe layer relaxation. Therefore it is suited best to obtain optimum performance. The process flow for such a test transistor is shown in Fig. 4a. The 300nm thick PtAu metallisation defined in a lift off

process masks the wet chemical etching of the emitter in KOH solution, which stops at the SiGe base. The undercut of the emitter mask results in a self-aligned base metallisation also structured in a lift-off process. After the lift-off of the collector contact metal, air bridges are etched in an isotropic SF_6/O_2 plasma in order to reduce the parasitic elements. Using such a double mesa test transistor a high transit cutoff frequency f_T of 116 GHz /57/ has been obtained for a single emitter transistor. A multi emitter finger structure with an optimized vertical doping profile has increased the maximal oscillation frequency f_{max} up to 160 GHz /44/. Fig. 5 shows the remarkable improvement of the f_T and f_{max} values in the last years.

In order to integrate a SiGe-HBT, the device should be passivated and have all elements of a high integrability including contact implantation and self-aligned low ohmic contacts (see Fig. 4b). The process starts with the implanted buried layer formation into the 5-10 Ωcm p (100) 4" substrate. After the blanket epitaxy of the entire LDC/SiGe-base/LDE/ HDE layer structure the emitter mesa is defined by reactive ion etching masked by oxide.

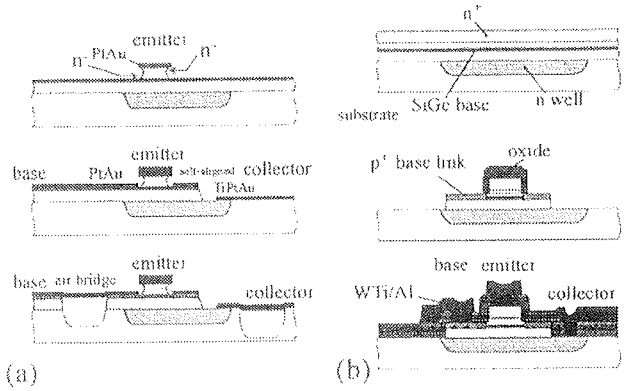


Fig.4 Process flow of (a) a non-passivated quick test SiGe-HBT and (b) a passivated double mesa SiGe-HBT

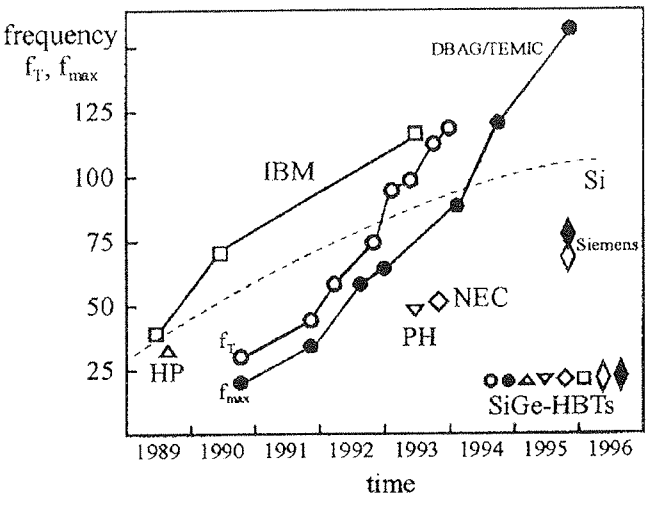


Fig 5: Development of the frequencies f_T and f_{max} of SiGe-HBTs

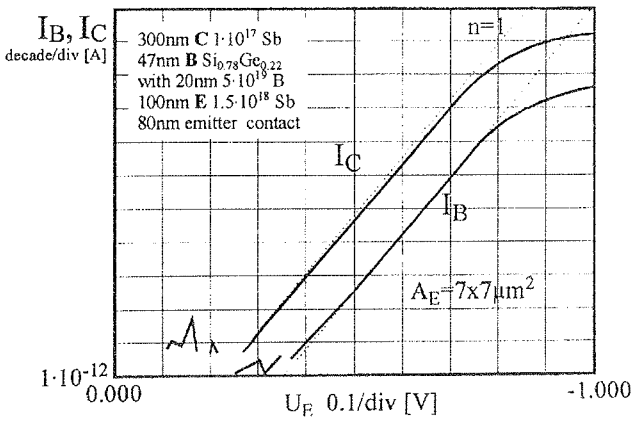


Fig.6: I-V characteristic of a passivated Si/SiGe-HBT

An outer base contact implantation is necessary to reduce the parasitic resistances. Low temperature passivation (LTO) by CVD SiH_4/O_2 at 300°C follows after etching of the BC-mesa and annealing of the contact implantation. Contact holes are defined and the WTi/Al-metallisation is wet chemically etched. Conventional silicon process technologies use high temperature oxidation and high temperature gettering processes to ensure a high quality surface passivation of the active and passive device areas and a low level of active metal contaminants. That is not acceptable for Si/SiGe-HBTs, because of the strong outdiffusion of the base and the SiGe layer relaxation. The Gummel plot in Fig. 6 shows a low temperature budget SiGe-HBT after a 450°C N_2/H_2-anneal. The passivation seems to be sufficient for Si/SiGe/Si double mesa transistors, according to the good ideality at low currents.

For the production of SiGe-HBTs TEMIC uses their Si-bipolar production line. The process, which was recently described in /58/, starts with a buried layer formation and a channel stop implantation in a 20 Ωcm substrate. The collector layers are formed by a 700 nm CVD silicon deposition and seperated by a recessed LOCOS process. The collector contact regions are implanted with phosphorus. Subsequently the differential CVD or MBE growth of the SiGe-base and the n-emitter follows. The 24-26% Ge and the $4\text{-}5\cdot10^{19}cm^{-3}$ boron are kept constant in the SiGe-base. The growth is monocrystalline in the oxide windows and poly-crystalline on the SiO_2. The CVD/MBE-poly-silicon, originally n-type, is converted to p by a BF_2 implantation. A selectively implanted collector offers the possibility to build transistors with high breakdown voltage and low collector-base capacitance and on the same wafer HBTs with higher current densities and higher f_T, but higher capacitance and lower breakdown voltage. In order to reduce the lead and the contact resistances titanium silicide is formed by a salicide process. The fabrication process ends with a two level Al metallization. Fig. 7 shows a top view of the transistor and Fig. 8 presents the transistor parameters.

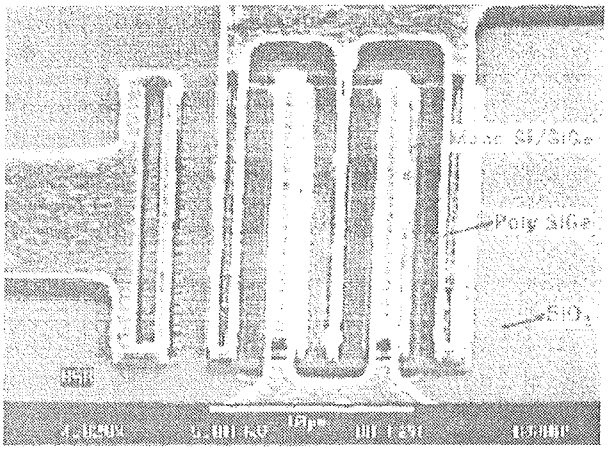


Fig.7: Top view of SiGe-HBT fabricated in a production line (TEMIC)

Parameter		no SIC	SIC
A_E	[μm^2]	1.2x2	1.2x2
N_C	[cm^{-3}]	3E16	1E17
BV_{CE0}	[V]	6.0	3.5
R_{sbi}	[Ω/]	1200	1200
h_{FE}	[ ]	150	150
V_A	[V]	50	40
f_T	[GHz]	30	50
f_{max}	[GHz]	50	50
F_{min}(2GHz)	[db]	1	1
R_B	[Ω]	140	140
C_{BC}	[fF]	10	15
C_{CS}	[fF]	22	22

Fig. 8: Transistor Parameter (TEMIC)

(b) passive components

High performance communication ICs need not only active but also passive devices. Fig. 9 gives an overview of the technological concept for resistors (R), inductors (L) and capacitors (C). After having processed the SiGe-HBT following layers are sputter-deposited: A 100 nm PECVD-oxide, the WSi_x-layer, the thin insulator IN_C of the integrated capacitors (SiO_2, Si_3N_4, AlN or TiO_2), the 50 nm WTi barrier and the 50 nm $Al_{(SiCu)}$ top layer. The MIM-structure for the capacitors is defined by the wet chemical etching of the $Al_{(SiCu)}$ and the WTi barrier.

An additional 300 nm PECVD-oxide insulates the upper electrode of the MIM-capacitor. After the contact hole etching and the wet chemical etching of the first metallization (WTi/$Al_{(SiCu)}$) the resistors and the capacitors are processed. A 3 μm thick polyimide is spun on and forms the IML (**I**nter **M**etal **L**ayer) for the isolation to the second metallization (100 nm WTi and 4 μm $Al_{(SiCu)}$). A second polyimide (1.5 μm) covers the second metallization and is opened only in the pad area.

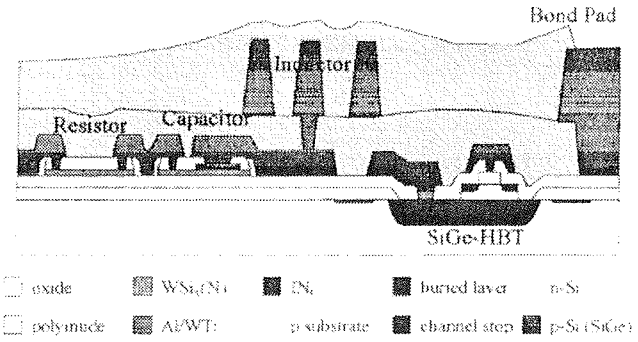


Fig. 9a: Schematic cross section of the two level metallization with the passive RLC-devices

L[nH]	n	D_a [μm] W/S=10/10	D_a [μm] W/S=10/5
1.25	2	190	175
	3	155	140
	4		130
3.00	2	330	315
	4	210	185
7.50	5	300	265
	7	280	240
15.0	6	385	
	8	350	340
	9		305

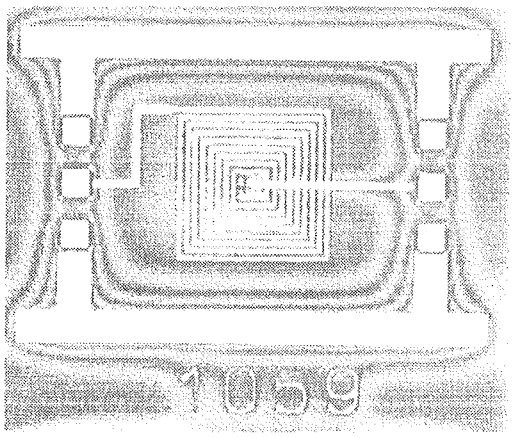


Fig. 9b: Table with the geometry of the spiral inductor (n=number of turns, L=inductivity, D_a=outer diameter, W=width of the Al-lines, S=distance between the lines) and a top view of a integrated inductor with polyimide between the to metallizations.

Resistors: For high performance analog and digital circuits there is a great interest for integration of thin film resistors (TFRs), because of the poor longterm stability of polysilicon resistors due to their polycrystalline structure. The materials of integrated TFR are WSi_x or WSi_yN_z /59/, $FeSi_x$ /60/, NiCr and $NiCr_xO_y$ /61,62/, Ta_2N /63/ or RuO_2 /64/. In contrast to VLSI integration, for most of these materials the lateral definition is done by lift off techniques or wet chemical etching. However sputtered $WSi_x(N_y)$ can be structured in F-based plasma or reactive ion etching and has a long term stability against temperature and current stress and has a sufficient resistance for most applications. The conductivity of the $WSi_x(N_y)$-TFRs is defined by the DC-power and the Ar/N_2 gas flow. Target values are R_S=100Ω (**WSi_x**: 30sccm Ar, 220W, 0.51Ωcm, d=52nm) and R_S=1000Ω (**WSi_xN_y**: 30sccm Ar, 4sccm N_2, 220W, 6.00Ωcm, d=58nm). The homogenity of the sheet resistance R_S across a 4 inch wafer is below 2% for R_S=100Ω and around 10% for R_S=1000Ω, with a high batch to batch reproducibility.

Capacitors: The integration concept for the capacitors has already been described above. The main advantage is the planar deposition of the bottom electrode (WSix), of the insulator IN_C and of the upper $WTi/Al_{(SiCu)}$ electrode e.g. in one multi target PVD machine. We use 20 nm PVD-SiO_2 and 45 nm AlN and receive capacitances of C*=6.0 fF/μm^2 and 2.3 fF/μm^2. In addition other materials with higher dielectric constants have to be tested to reduce the parasitic inductor.

Inductors: In monolithic microwave integrated circuits (MMICs) spiral inductors are used. They will be applied as reactive loads, for low-noise coupling purposes and in matching networks. From these applications inductors should have a high imaginary part and a high quality factor Q. The layout optimization of the spiral inductors for applications in the 2 (7.5 nH), 5 (3.0 nH) and 12 GHz (1.25 nH) range is shown in Fig. 9b. The inductivities are calculated using the Greenhouse Algorithmus /65/. Some of the measured inductivities and quality factors are plotted in Fig. 10. The difference between the measured and target inductivity values is due to the Ing contact lines. The quality factors increase with decreasing substrate loss and thicker second metallization and/or a thicker IML. The maximum of the quality factors is near the operating frequency.

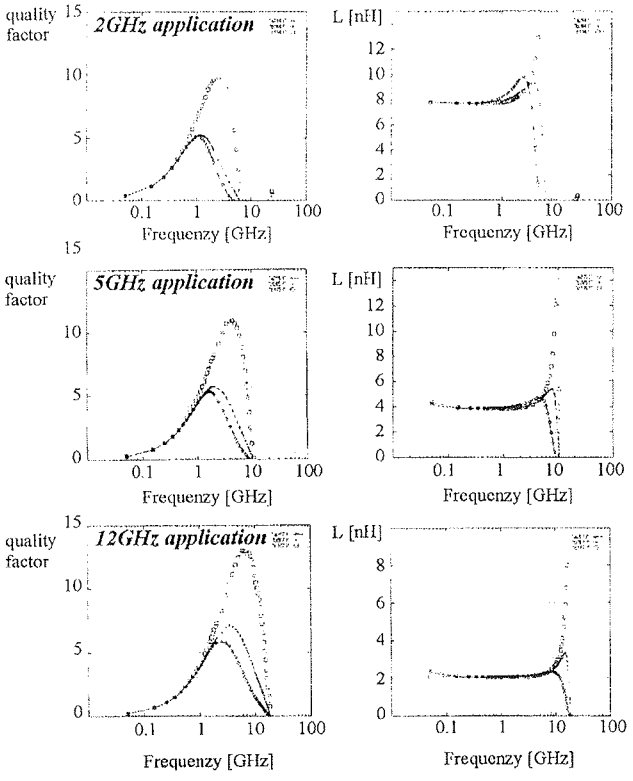


Fig. 10: Measured inductivity and quality factor for different frequency ranges.

3. SiGe-HBT circuits

Various HBT-ICs have been reported so far, some with outstanding, some at least with promising performances. Fig. 11 shows a chip with circuits for 5 to 40 GHz operation realized on semiinsulating Si-substrate. More production like are circuits on 20 Ωcm substrates (one example in Fig. 12), has under development at TEMIC/66/. ECL ring oscillators realized by Siemens, Philips, IBM, NEC, or Temic together with our house (DBAG) exhibit 11 to 20 ps /52,67-69/. A 12 bit DAC operating at 1 GHz has been demonstrated by IBM together with ADI /70/. NEC has reported on D-type flip-flop for 20 Gbit/s, a selector for 30 Gbit/s and 33 ps, a 2:1 multiplexer for 20 Gbit/s and a preamplifier with 19 GHz and 36 dB /71,72/. Multiplexer and demultiplexer

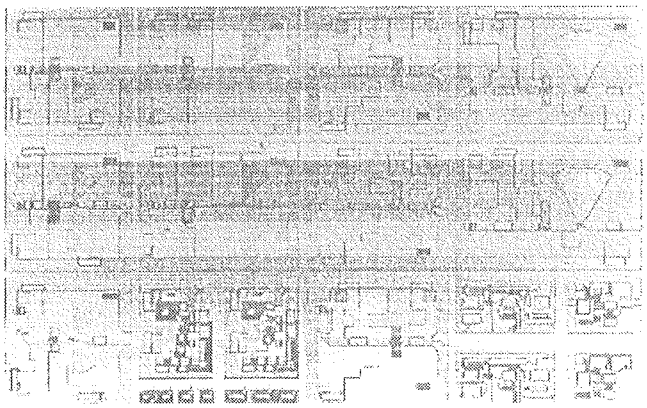


Fig.11: SiGe-HBT chip with circuits for 5-40 GHz.

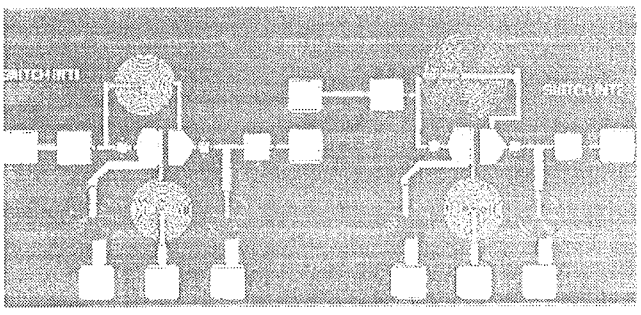


Fig.12: SiGe-HBT switches for 2 GHz with spiral inductors (Temic) /66/

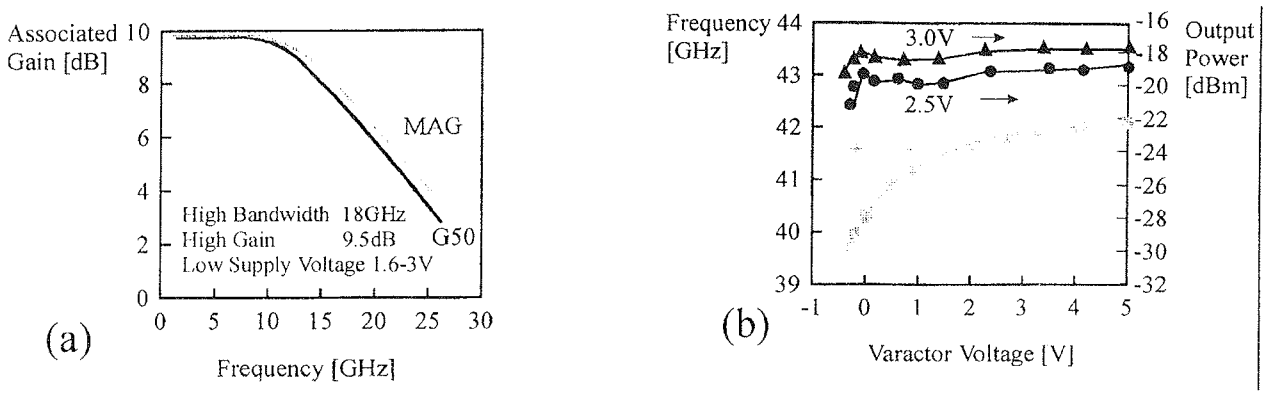


Fig.13: Low power consumption broad-band amplifier a) and varactor controlled oscillators with SiGe-HBTs /74,75/

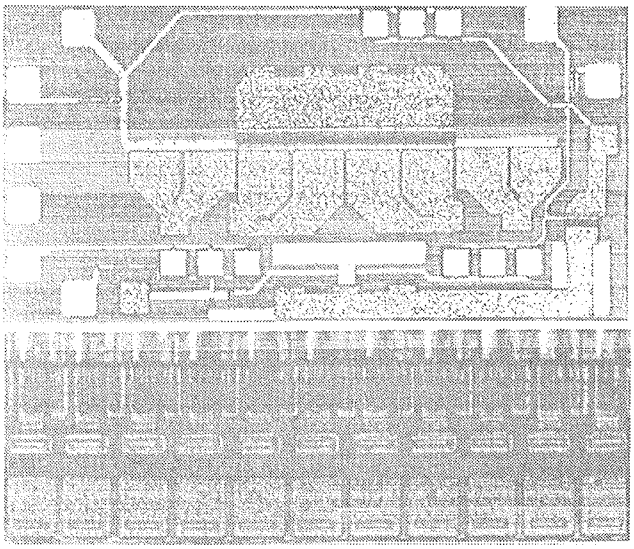


Fig. 14: SiGe-HBT power amplifier and enlarged emitter area

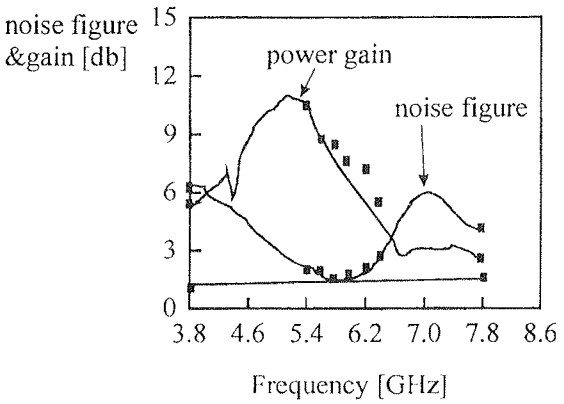


Fig. 16: Hybrid active antenna with a SiGe HBT yielding low noise at a receiving frequency of 5.8 GHz (Uni Ulm)

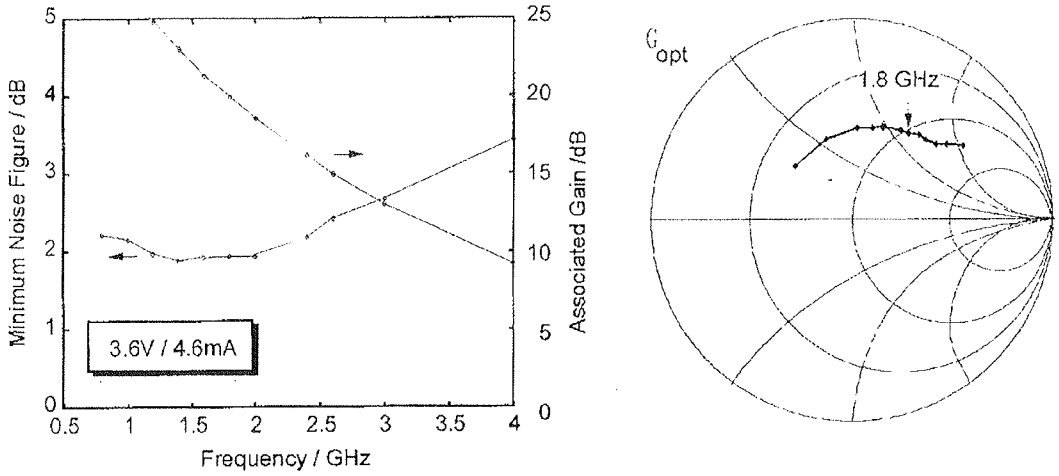


Fig. 15 Low-Noise Amplifier using SiGe HBTs for DECT Receivers (Uni Ulm) /76/.

with 28 Gbit/s have been realized by the Ruhr University Bochum using samples from DBAG /73/. A wideband amplifier capable of 9.5 dB gain with 18 GHz bandwidth while drawing only 50 mW from a 3 V supply and operating even at 1.6 V was realized (Fig. 13a) /74/. Varactor controlled oscillators for different frequency ranges of 1.8, 11, 26, 28, 40 GHz (e.g. see Fig. 13b) were presented by Nortel together with IBM, by TEMIC, by IBM and by DBAG /75, 76/. Power amplifiers for 0.9 to 2 GHz have been realized by Temic together with DBAG (Fig. 14) and by Philips /54, 77/. LNAs with F_{min} of 1.7 to 1.9 dB came from Temic together with DBAG and the University of Ulm (Fig. 15) A frequency devider of 42 Gbit/s was recently realized by Siemens /78/. We have used SiGe HBTs for hybrid intergration, too: A dielectric resonator oscillator (DRO) for 9.6 GHz and a 8-12 GHz VCO were reported by DBAG and Dornier /79/. Very recently an active antenna for receive at 5.8 GHz with the excellent noise Figure of 1.4 dB was reported by the University of Ulm using a device of DBAG (Fig. 16) /80/.

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