IEEE 1149.1 STANDARD: A WIDELY SUPPORTED DESIGN FOR TESTABILITY TECHNIQUE

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Key words: electronics, electronic circuits, PCB, Printed Circuit Boards, IC, Integrated Circuits, electronic systems, testing, debuggers, debugging, design for testability, in-circuit test, boundary-scan test, JTAG, Joint Test Action Group, IEEE 1149.4 standards, TAP, Test Access Port, mixed-signal test buses, EDA, Electronic Design Automation, ATPG, Automated Test Pattern Generation, IEEE 1532 standards, in-system configurations, IEEE 1500 standards, embedded core tests

Abstract: This paper is a short introduction to the implementation and application of IEEE 1149.1 boundary-scan test techniques, which are key to efficient design test and debug in increasingly complex electronic circuits. Following a short description of IEEE 1149.1 compliant devices, the paper focuses on the actual benefits of using boundary-scan test infrastructure on chip, board and system levels. Main features of currently available boundary-scan test design and application tools are briefly presented. A survey on IEEE 1149.1 standard extensions and recent developments of related standards is also included, which confirms the importance for designers to be familiar with boundary-scan techniques. The main goal of the paper is therefore to promote the use of IEEE 1149.1 and other standardized design for testability techniques amongst developers and designers in our national electronic industry.

IEEE 1149.1 standard: dobro podprta tehnika načrtovanja zmožnosti testiranja vezij

Ključne besede: elektronika, vezja elektronska, PCB plošče vezja tiskanega, IC vezja integrirana, sistemi elektronski, preskušanje, iskalniki in odstranjevalniki napak, iskanje in odstranjevanje napak, snovanje za preskusljivost, preskušanje v vezju, linija preskusna robna, JTAG skupina delovna za preskušanje spojev, IEEE 1149.4 standardi, TAP vrata dostopa preskusa, vodila preskusna s signali mešanimi, EDA avtomatizacija snovanja elektronike, ATPG generiranje vzorcev preskusnih avtomatizirano, IEEE 1532 standardi, konfiguracije v sistemu, IEEE 1500 standardi, preskušanje jeder vgrajenih

Izvleček: Članek predstavlja kratek uvod v načrtovanje in uporabo tehnike IEEE 1149.1 robne testne linije, ki je ključnega pomena za učinkovito testiranje in razhroščevanje čedalje bolj kompleksnih elektronskih vezij. Kratkemu opisu strukture IEEE 1149.1 združljivih komponent sledi predstavitev dejanskih koristi, ki sledijo iz vgradnje infrastrukture robne testne linije v integrirano ali tiskano vezje oziroma elektronski sistem. Na kratko so predstavljene poglavitne lastnosti trenutno razpoložljivih orodij za načrtovanje vezij in testnih postopkov z uporabo robne testne linije. Pregled razširitev standarda IEEE 1149.1 ter trenutnega razvoja sorodnih standardov dodatno potrjuje potrebo načrtovalcev vezij po poznavanju tehnik robne testne linije. Cilj prispevka je tako predvsem spodbujanje uporabe IEEE 1149.1 in drugih standardiziranih postopkov načrtovanja zmožnosti testiranja med razvijalci in načrtovalci v domači elektronski industriji.

1. Introduction

Miniaturization and increasing density of modern electronic devices has brought to increased problems in the production testing of loaded printed circuit boards (PCBs). The production test is essentially an attempt to detect possible defects, such as net-to-net shorts, solder opens or missing components in the assembly of integrated circuits (ICs) and other components on the board. In-circuit test (ICT) has been the industry leading technique for board level testing since mid-1970s due to a number of benefits compared to various functional ("edge connector") testing methods /1/. ICT relies on physical probing of internal PCB interconnections through a "bed-of-nails" fixture (Figure 1) in order to improve fault detection and simplify component level diagnosis.

As high density ICs with smaller pin-to-pin spacing evolved, distance between PCB interconnections has decreased and test lands, which are laid onto copper interconnections to allow ICT probe application, have shrinked as well. This made ICT bed-of-nails fixtures difficult and costly to build. Furthermore, use of multichip modules (MCMs), complex System-on-Chip (SoC) devices and multi-layer boards made physical access to internal nodes virtually impossible /2/.

During the 1980s several companies tackled the problem of limited access board testing, developing the so-called boundary-scan principle. They built their concept on ICT techniques, but with physical nails being substituted by an on-chip serial shift register placed around the IC core boundary i.e. a boundary-scan register. In 1985 representatives from several European and North American companies formed the Joint Test Action Group (JTAG), which converted the boundary-scan idea into an international standard. The IEEE 1149.1 standard was first published in 1990.

During the past decade boundary-scan became a mature Design for Testability (DfT) technique /3/, widely supported by both catalog IC manufacturers and by electronic design automation (EDA) tool vendors /4, 5, 6/. Nevertheless many electronics manufacturers still ignore the benefits of providing their PCB designs with IEEE 1149.1 infrastructure. This paper wants to briefly illustrate these ben-

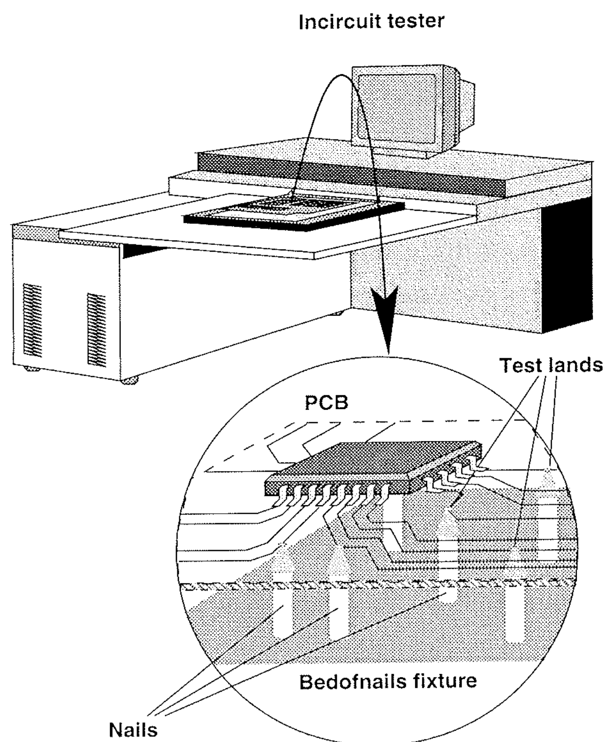

Figure 1: In-circuit test technique

efits and direct the interested reader to more detailed sources of information on boundary-scan infrastructure design, its use and the available tools.

2. The IEEE 1149.1 standard test access port and boundary-scan architecture

A boundary-scan device features multi-purpose memory elements called boundary-scan cells (BSCs), which are interposed between each primary input or output and the appropriate core logic terminal, and a minimal Test Access Port (TAP) interface (Figure 2). The BSCs are serially concatenated into a parallel-in parallel-out shift register, which is accessed through two TAP pins, namely Test Data Input (TDI) and Test Data Output (TDO). Control structures, which are required to select between normal and test operation modes, comprise a finite state machine (TAP controller) that operates synchronously to a Test Clock (TCK) and under the control of a Test Mode Select (TMS) signal. Additional test structures include a single instruction register that controls the test modes and any number of test data registers (including the boundary-scan register) that can be selected by specific instructions. An optional Test Reset (TRST) pin can be also included into the TAP.

The IEEE 1149.1 standard does not prescribe actual hardware implementation of the test infrastructure described above but only defines required components (4-port TAP, boundary, instruction and bypass registers) and their functional properties, as well as the minimum test instruction

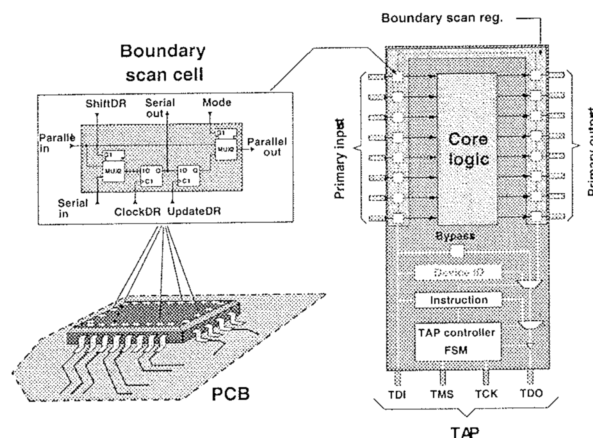

Figure 2: Structure of a boundary-scan device

set that any compliant device must support /7/. Furthermore, the standard allows for optional and proprietary test instructions, and for additional test data registers to be implemented on-chip. A later supplement to the standard defines the Boundary-Scan Description Language (BSDL) syntax. BSDL is used for describing the boundary-scan device pin-out and the specific implementation of its test infrastructure (such as boundary register, optional registers, instruction set and opcodes). BSDL files are readily available from manufacturers of IEEE 1149.1 compliant devices.

2.1 Use of boundary-scan at chip level

The on-chip boundary-scan test infrastructure does not contribute to the basic functionality of the device. Nevertheless it can provide substantial benefit at chip level with its provision for a standard test access method (TAP), which can be used to access chip-internal test facilities, such as internal scan path, built-in self-test (BIST) or built-in emulation and debug.

Internal scan paths are implemented by substituting normal storage elements (latches, flip-flops) within the core logic with scannable ones, which can be serially interconnected to form a shift register structure (Figure 3). The primary reason to adopt this technique is the inability of sequential automatic test pattern generation (ATPG) algorithms to provide adequate fault coverage for core logic test. By dividing core logic into smaller sequential blocks (partial-scan), or plain combinatorial blocks (full-scan) that are accessible from the internal scan path, better fault coverage can be achieved with existing ATPG algorithms /8/.

IEEE 1149.1 architecture allows the definition and use of proprietary instructions therefore the internal scan path register can be easily integrated with other 1149.1 test data registers. Consequently, static device test requirements can be reduced to the TAP interface, since both boundary and internal scan registers are accessible through TDI/TDO. Furthermore, internal scan path can be accessed through the same interface for chip debug and failure diagnosis.

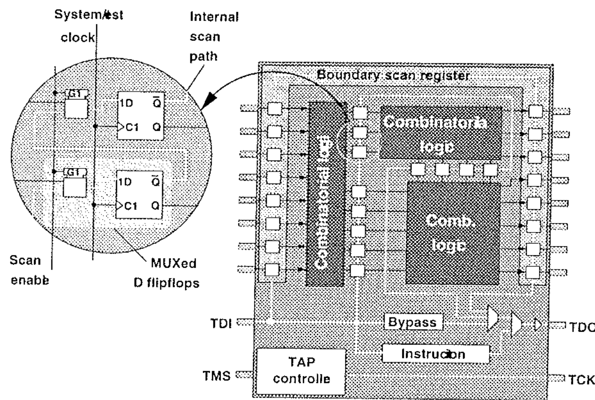

Figure 3: Device with internal scan path

The main benefit of BIST techniques is that test vectors are generated and test responses are monitored on-chip thus eliminating the need for external generation and application of large sets of test vectors via the chip primary inputs/outputs. This is usually achieved by means of pseudo-random pattern generators and signature analyzers implemented as linear-feedback shift registers (LFSRs). IEEE 1149.1 provides for easy integration with on-chip BIST through the implementation of the optional *runbist* test instruction. When implemented, *RUNBIST* can provide for quick functional testing of a PCB mounted device.

2.2 Use of boundary-scan at board level

Board-level test has been the primary concern of the IEEE 1149.1 standard developers. Boundary-scan cells replace ICT physical nails by providing electrical access to circuit-internal nodes through device primary inputs/outputs and are therefore often referred to as "virtual nails" or "silicon nails". At the board level, boundary-scan devices are usually daisy-chained (TDO to TDI, Figure 4) to form a single boundary-scan path.

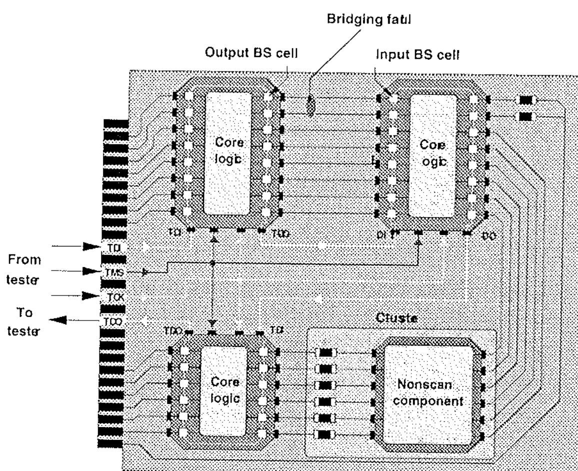

Figure 4: Board-level boundary-scan path implementation

For boards, which are entirely populated by IEEE 1149.1 compliant devices, opens/shorts tests with 100% fault coverage can be generated fully automatically by ATPG software and inexpensive four-wire boundary-scan testers can be used to perform the board test. Furthermore, faults can be automatically isolated to the interconnection (for shorts) or to the node (for opens). The task of generating board-level fault tests is greatly simplified. Since each device input pin can be sampled and each output pin can be driven from the appropriate BSC, no knowledge of the device core logic is required for fault testing the board. For a group of PCB interconnections between two boundary-scan devices, a single test vector is required to test all interconnections for stuck-at-one faults. To provide stimulus, an all-zeros test vector is shifted into output BSCs via TDI to drive the interconnections low. Interconnection values are then sampled into input BSCs and shifted out via TDO for comparison with the expected value. Similarly, stuck-at-zero faults test requires a single test vector of all-ones. Bridging faults can be isolated using a binary search algorithm: a group of 8 interconnections requires only 3 test vectors for a complete bridging fault test, as shown in Table 1.

	Interconnection							
	1	2	3	4	5	6	7	8
Vector 1	0	1	0	1	0	1	0	1
Vector 2	0	0	1	1	0	0	1	1
Vector 3	0	0	0	0	1	1	1	1

Table 1: Test vectors for 100% bridging fault coverage (number of interconnections = 8)

Altogether, a board with N interconnections between distinct BSCs, would require a total of (log N / log 2) + 2 test vectors for full bridging and stuck-at fault test (i.e. 5 test vectors for 8 nets). Consider now fault testing a non-IEEE 1149.1 board with ICT probes. In contrast with BSCs, bed-of-nails fixtures usually provide a single access point to any interconnection, therefore stimulus is applied to interconnections at device inputs and response is sampled on interconnections at device outputs. A plain combinatorial device would require 2^N test vectors for a full test (i.e. 256 vectors for 8 interconnections). Although the number might be significantly reduced by studying the device functionality, this requires adequate functional models and test development tools. In case of a sequential device the problem would become even more complex, since several set-up vectors might be required to condition a device to test an input and several vectors might be required to propagate the fault to an output for observation.

On the other hand, even if the board comprises only a few IEEE 1149.1 devices, the test development can be substantially simplified and fault coverage improved. When clusters of non-scan devices and other components are surrounded by boundary-scan devices, BSCs in surrounding devices can be used to stimulate the cluster and observe its responses. In this case a suitable test vector set targeting interconnection faults within the cluster must be prepared. When such approach is not sufficient in terms of fault coverage, the boundary-scan infrastructure can be

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combined with ICT physical nails to access cluster-internal interconnections.

2.3 Use of boundary-scan at system level

Chip and board-level IEEE 1149.1 based tests can be re-used at system level e.g. for system BIST, field service, remote diagnostics or hardware debug. The main benefit is that the physical test access can be limited to the simple TAP interface and use of complex test hardware can be avoided. Moreover, by implementing backplane bus interfaces on single PCB modules and on the backplane PCB with scannable devices, the backplane connectivity and integrity test can be performed and the system can be partitioned along modules boundaries for easier diagnostics.

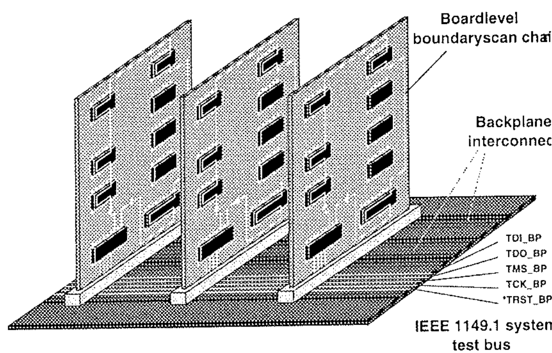

Figure 5: Multidrop system IEEE 1149.1 architecture

While a single boundary-scan chain is usually used to connect IEEE 1149.1 devices on a PCB (Figure 4), the same approach is not adequate for integrating boards into the backplane architecture (Figure 5). If the backplane is designed such that board-level scan chains are daisy-chained into a single system wide chain, then removing any board from the system will break the boundary-scan chain. Furthermore, boards must be located in specific slots in order to preserve a known test infrastructure and a fault in the chain of one board would leave the entire system untestable. To avoid such problems the standard proposes a multidrop star configuration in which the TDI and TDO pins are bussed. However to prevent simultaneous scanning of multiple boards onto the same TDI/TDO bus, multiple TMS signals are required (one for each slot) and the number of backplane channels increases proportionally. An alternative solution, which does not require multiple TMS lines, is a multidrop scheme using addressable IEEE 1149.1 devices.

3. Boundary-scan development tools and testers

In order to benefit from the IEEE 1149.1 standard, the designer should specify the use of boundary-scan infrastructure in custom ASICs and place scannable catalog devices on board wherever possible. Nowadays a number of IC vendors provide a variety of IEEE 1149.1 compliant devices, including standard components (bus interfaces, microprocessors, DSPs, memory ICs, ...), user field-programmable devices and ASICs (gate-arrays, standard cells, ...). Various support devices (test bus controllers, scan path bridges/linkers/selectors, multidrop addressable test ports) are readily available to facilitate the implementation of board or system level boundary-scan infrastructure.

Another very important issue for a designer is the availability of EDA tools supporting boundary-scan. Most major EDA vendors offer boundary-scan insertion tools as well as tools for boundary-scan ATPG.

Finally, some means of boundary-scan test application is also required, which can come either in the form of large production in-circuit or functional testers with integrated boundary-scan capabilities or as inexpensive, PC-based standalone boundary-scan testers.

3.1 Design of IEEE 1149.1 compliant devices

Boundary-scan insertion tools provide for a more or less automated design of IEEE 1149.1 compliant ASICs, which is often combined with insertion of other on-chip test structures, such as internal scan or BIST. These tools usually operate on RTL or gate-level descriptions of the ASIC design and on existing libraries of boundary-scan building blocks. Better tools provide for a more flexible configuration of the building blocks (e.g. implementation of proprietary test instructions, integration with internal scan / BIST) as well as for the generation of test patterns for use with on-chip test structures. The tool output usually consists of a device netlist and the appropriate BSDL device description (see Figure 6).

3.2 Boundary-scan test development

Boundary-scan ATPG tools automatically generate prototype or manufacturing tests to be applied to the circuit under test (CUT) using the board level TAP. ATPG tools usually consist of various software modules, which can be combined to suite the chosen test strategy. Modules include access analysis, boundary in-circuit test, virtual interconnects test, virtual component/cluster test, boundary functional test as well as test generators for BSDL validation and TAP/scan-path integrity testing. Access analysis tools are typically used before layout of mixed scan/non-scan circuits to identify interconnections, which do not require physical test access. Boundary in-circuit test generators combine physical probing and boundary-scan devices to reduce test complexity. Virtual interconnect test modules generate patterns to test interconnections using only the virtual access provided by the boundary-scan path while virtual component/cluster test modules use boundary-scan access to detect open and stuck-at faults on the leads of non-scan devices/clusters, eliminating the need for physical access. Some tools also support multiple boundary-scan paths on a single board. ATPG tools usually operate

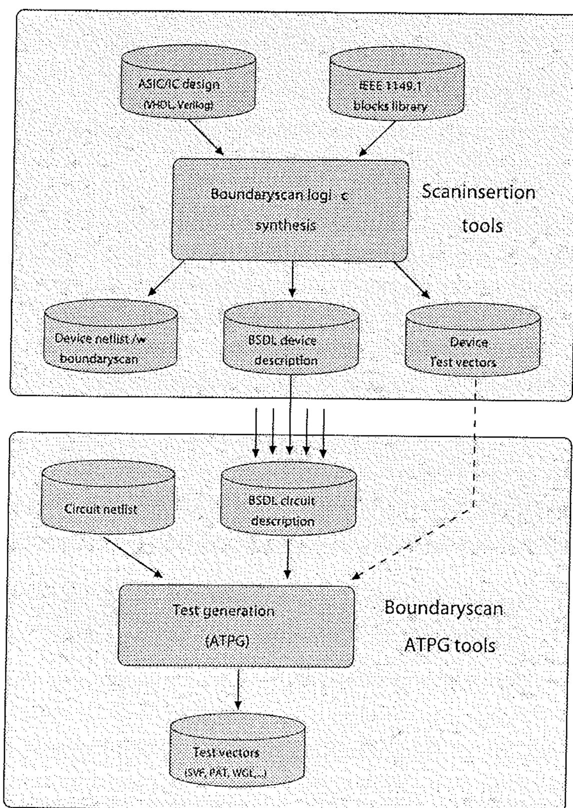

Figure 6: Boundary-scan development process

on given circuit netlist and BSDL description (see Figure 6), producing test patterns in standard automatic test equipment formats, such as the Serial Vector Format (SVF).

3.3 Boundary-scan testers

We can roughly divide commercially available boundary-scan testers into two groups. The first one includes large production in-circuit and functional testers with integrated boundary-scan support, which are designed to achieve the highest possible fault coverage within only one production step. This is reflected by high complexity and elevate costs of such testers. The second group includes so-called stand-alone boundary-scan testers. These usually consist of a host PC and a relatively inexpensive adapter, which controls the IEEE 1149.1 test bus and possibly features some additional parallel I/Os to control/observe CUT edge connectors. A variety of internal and external PC adapters are available on the market for many standard buses, such as ISA, PCI, VXI, PXI, PC-CARD, PIO, RS-232, USB or GPIB.

The minimum requirement for any boundary-scan tester is the ability to exercise the board-level TAPs under the control of a simple test description (e.g. a SVF file), however an interactive boundary-scan test and debug environment is preferred to simplify the use of the test system. Most boundary-scan testers provide software tools that allow interactive view and control of only those portions of the board (pin, register, bus, user-defined signal group) that

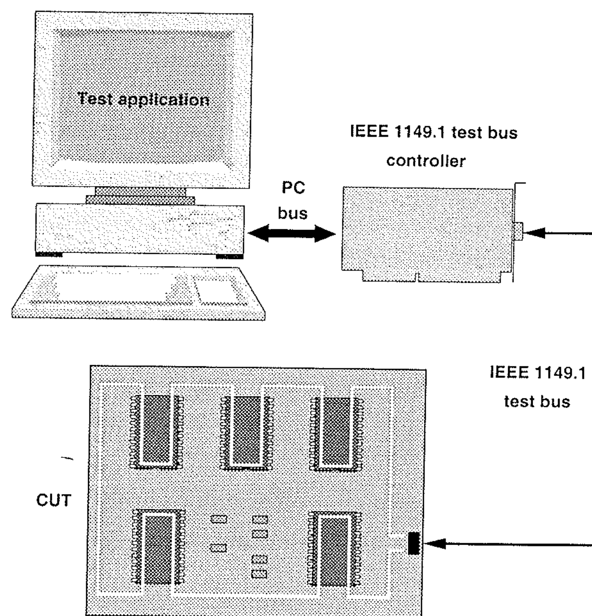

Figure 7: Stand-alone boundary-scan tester

are of interest. The benefit of such tools is that complexity of TAP protocol and boundary-scan chain are hidden from the user and test stimuli/responses are presented as waveform and state diagram displays. The tools usually support various test vector generation methods including interactive creation and EDA or boundary-scan ATPG generated test sets. They also allow the user to describe the boundary-scan test infrastructure using standard formats such as BSDL and EDIF (Electronic Design Interchange Format).

4. IEEE 1149.1 related standards

During the existence of IEEE 1149.1 several related standards have emerged, which extended the use of the boundary-scan techniques and its infrastructure to new areas such as testing of mixed-signal circuits or in-system configuration (ISC) of programmable devices, while a standard concerning testing of System-on-Chip (SoC) devices is currently in project phase. The original standard itself has seen two additional supplements: IEEE 1149.1a-1993 and IEEE 1149.1b-1994 (BSDL). The IEEE 1149.1-1993 supplement brought some clarifications and new optional boundary-scan test commands to the original standard. Furthermore it addressed the issue of integration of IEEE 1149.1 with other test access methods such as the Level Sensitive Scan Design (LSSD), which is frequently used to access internal scan paths. The supplement described a simple mechanism for converting a component from conformance to IEEE 1149.1 to conformance to a different standard. The three publications were finally merged into the latest standard publication - IEEE 1149.1-2001.

4.1 IEEE standard for a mixed-signal test bus (1149.4-1999)

The IEEE 1149.4 standard extended the boundary-scan principle into the domain of mixed analog-digital circuits with the introduction of new elements to the existing IEEE 1149.1 test infrastructure. The standard defines analog boundary modules (ABMs), which are interposed between primary analog functional pins and appropriate analog core terminals. The TAP is expanded with analog pins AT1 (Analog Test 1) and AT2, which are internally connected to each ABM via the Test Bus Interface Circuit (TBIC) and a two-wire on-chip analog bus AB1/AB2 (Figure 8). At the board level, all IEEE 1149.4 devices are connected to a two-wire analog bus through AT1 and AT2 pins /9/.

This additional infrastructure allows analog stimulus from external generators to be routed from AT1 pin to an output ABM and on to connected analog components. Analog responses arriving at an input ABM can be routed to AT2 pin and on to an external measurement unit. In this way, parametric measurements of on-board analog components can be performed.

Although IEEE 1149.4 compliant catalog devices are currently unavailable, first steps are being done by IC manufactures towards the implementation of such devices /10/ and feasibility studies on experimental ICs have already shown a number of possible benefits in designing mixed-signal ICs with IEEE 1149.4 infrastructure /11, 12, 13/.

4.2 IEEE standard for in-system configuration of programmable devices (1532-2000)

In-system configuration of programmable devices has become a major new application of the IEEE 1149.1 standard. Programmable logic imposes several problems (lack of device models, test preparation delays) to ICT board testing methods, therefore IEEE 1149.1 infrastructure is included in the majority of programmable devices. The manufacturers soon realized that they could also use the TAP interface and the boundary-scan serial protocol for ISC of the device. The result of a standardization effort between various manufacturers is the IEEE 1532 standard, which defines additional data registers to assist configuration programming, along with new mandatory and optional instructions compatible with the IEEE 1149.1 physical and logical protocols /14, 15/.

4.3 IEEE Standard Testability Method for Embedded Core-based Integrated circuits (P1500)

Test development currently represents a major problem in the design of complex SoC devices, which include embedded cores originating from different core providers. The P1500 working group was established in 1995 with the goal to develop a standard DfT method for such devices. The standard will define a test wrapper architecture and a language for the description of test related information for

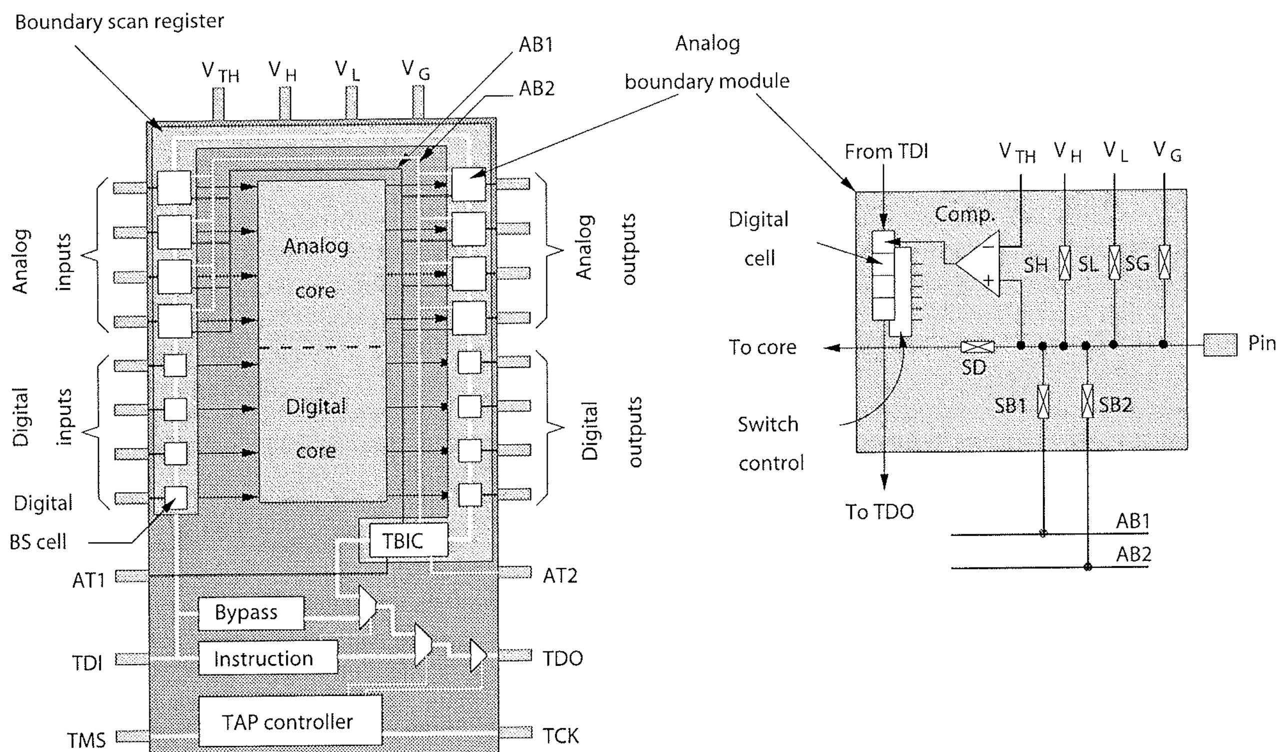

Figure 8: IEEE 1149.4 compliant mixed-signal device structure

the cores (e.g. processor cores, memory blocks, ...) embedded in the SoC /16/, /17/.

In practice, many embedded cores might already include IEEE 1149.1 or another test access mechanism. Hence we may expect the P1500 standard (or a related document) to present some solution for the integration of different test access standards with the proposed wrapper architecture. As mentioned above, similar issues concerning IEEE 1149.1 were addressed by a later supplement to the original standard.

5. Conclusion

In the early years from its publication, the IEEE 1149.1 standard was often criticized for elevating silicon costs and increasing design time. Many designers failed to see how the standard can benefit them, often being confused by the requirements for complex sequencing of the TAP signals. However the declining silicon costs, the growing list of IEEE 1149.1 compliant catalog devices, and the increasing availability of EDA tools that automate boundary-scan test insertion, generation and application have resulted in boundary-scan becoming a widely accepted DfT technique.

Although IEEE 1149.1 is a very efficient answer to the complex problem of testing boards and systems for various manufacturing defects and performing other design debug tasks, many designers still seem to lack basic knowledge about its potentials. In this paper we briefly introduced the reader to the standard, the main benefits of its use at chip, board or system level, and the most important features of available EDA tools. We presented some recent standardization efforts related to the IEEE 1149.1 standard, demonstrating the importance for designers to be familiar with boundary-scan techniques, which will keep an important role in the design of increasingly complex electronic devices. Readers looking for further details on boundary-scan are therefore encouraged to consult referenced literature.

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Prispelo (Arrived): 18.11.2001 Sprejeto (Accepted): 25.04.2002