CONSIDERATIONS OF IEEE 1149.4 STANDARD IN ANALOG DESIGN

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Abstract: The paper gives a brief introduction to the emerging Standard for Mixed-Signal Test Bus described by the P1149.4/D25 draft. The aim is to provide standardized approaches to interconnect test, parametric test and internal test of a printed circuit board including mixed-signal devices. In the paper, the main features of the proposed standard are described and the results of an experimental case study using the IEEE 1149.4 KLIC Test Chip are summarized.

Upoštevanje standarda IEEE 1149.4 pri načrtovanju analognih vezij

Ključne besede: IEEE standardi, IEEE 1149.4 standardi, preskusi robni, DFT snovanje na preskusljivost, vezja analogna, vezja digitalna, vezja mešana, preskusi parametrični, preskusi notranji, ATE oprema za preskuse avtomatska, JTAG skupina delovna za preskušanje spojev, TAP vrata dostopna preskusa, TCK ura preskusna, ABM moduli robni analogni, TBIC vezje vmesniško vodila preskusnega, ATAP vrata za preskus analogni

Povzetek: Članek podaja kratek uvod v nastajajoči Standard testnega vodila mešanih digitalno/analognih vezij predstavljenega v delovni dokumentaciji P1149.4/D25. Cilj predlaganega standarda je ponuditi standardiziran pristop k izvedbi testiranja povezav, parametričnega testa in notranjega testa tiskanine opremljene z digitalno/analognimi integriranimi vezji. Opisane so glavne značilnosti predlaganega standarda in povzeti rezultati eksperimentalne študije uporabe testnega integriranega vezja IEEE 1149.4 KLIC.

1. Introduction

Increasing complexity and greater miniaturization are rapidly reducing the ability to test printed circuit boards effectively. Traditional in-circuit test techniques utilize a bed-of-nails to make contact to each individual lead on a printed circuit board. With the introduction of surface mounted devices, small pitch packaging becomes prevalent which makes the access to the test points on the board either impossible or at least very costly. Furthermore, as device and board functionality grow, the test process is becoming more difficult.

The need for an alternative access approach gave the idea of somehow building the test probe directly into the silicon chip. In other words, the proposed solution was to build parts of the test equipment into the actual circuits. The effort of a group of ATE makers and EDA tool suppliers organized as the Joint Test Action Group (JTAG) resulted in a boundary-scan test technique for digital circuits and systems. In 1990 it was approved by the IEEE as standard 1149.1, /1/. The standard is now widely supported by major manufacturers of ICs and ASIC vendors.

Boundary scan was developed first for digital components and boards. This was due to the fact that the problem is more tractable in digital than analog or mixed-signal domain. In contrast to the digital circuits, analog components are specified by a continuous range of parameters rather than two discrete logical values 0 and 1. Besides, their interconnections may comprise networks of other analog components rather than simple wires. In order to tackle the problem, the development of analog boundary-scan has started in 1991. The work is coming to a close after the second ballot in March 1999. It is realistic to expect that the current Draft Standard for a Mixed-Signal Test Bus P1149.4/D25 /2/ will be approved by the IEEE as standard 1149.4 in the following months.

In this article we first briefly describe the main idea of the IEEE 1149.1 standard. Next, we summarize the basic features of P1149.4 Mixed-Signal Test Bus and point to some useful references related to this document. In the second part, experiments with IEEE 1149.4 KLIC Test Chip are reported. At the end, some concluding remarks are drawn.

2. IEEE 1149.1 Standard

The principle of the boundary-scan technique is to place a shift register boundary-scan cell adjacent to each component pin and to interconnect the boundary-scan cells in order to form a chain around the border of the chip logic design. During the test mode, boundary-scan cells are used to control the status or read the states of the pins, while during the normal mode the cells are transparent. Components of a board that are fitted with the test structure of the IEEE 1149.1 standard are interconnected by way of the standard interface with the 4-wire test bus providing serial input data, serial output data, clock and mode select line. Addition of the boundary-scan logic has the following principal tasks: it allows normal circuit operation, it allows data to be shifted in or test results to be shifted out, and it provides a number of circuit tests. The following test modes are normally supported:

- external test (i.e., test of interconnections of the board),
- sample test (i.e., a snapshot of the states of boundary-scan supported pins during the normal operation of the board),

- bypass (i.e., a shortcut of a boundary-scan path of the board),
- built-in self-test at the chip level.

In addition, IC manufacturers usually provide more testing facilities by offering the user a set of non-mandatory boundary-scan operations.

The IEEE 1149.1 Standard defines the following basic hardware elements:

- the Test Access Port (TAP),
- the TAP Controller,
- the Instruction Register,
- different Test Data Registers.

An IC compliant with IEEE Std 1149.1 must include TAP, TAP Controller, IR and the mandatory Test Data Registers: Boundary-Scan Register and Bypass Register, as shown in Figure 1.

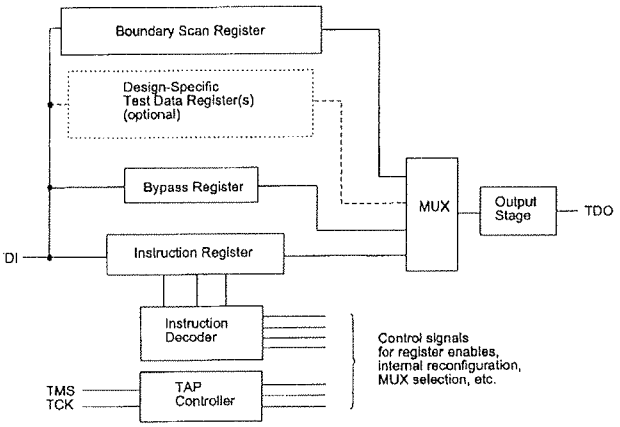

Figure 1: The standard boundary-scan architecture

The TAP Controller is a sequential circuit, its operation is controlled by the signals through the TAP. TAP consists of four mandatory connections (Test Clock Input, Test Mode Select Input, Test Data Input and Test Data Output) and one optional (Test Reset Input). Thus, any IC conforming with IEEE Std 1149.1 has at least four additional pins.

The TAP Controller generates clock and control signals required for the operation of the Instruction Register and the Test Data Registers in order to:

- provide signals for loading the instructions into the Instruction Register,
- provide signals for shifting data into and out of the Test Data Registers,
- perform test actions (i.e., capture data, shift data, update data).

The operation of the TAP Controller is given by the state diagram which defines the test protocol. IEEE Std 1149.1 prescribes three mandatory instructions: Bypass, Sample/Preload and Extest.

The purpose of the Bypass instruction is to shorten the scan path through the boundary-scan architecture when scan access of the test data registers is not required.

The Sample/Preload instruction is used to scan the Boundary-Scan Register during the normal circuit operation (i.e., not in the test mode!). Its execution does not interfere with circuit's normal operation, hence this option may be very useful for system debugging.

The Extest instruction allows test of board interconnections (i.e., test of opens, shorts or bridging faults).

In addition, a number of non-mandatory instructions may also be provided. Some typical representatives are: Runbist (which runs a built-in self-test of a circuit), Idcode (which allows reading of the circuit's identification code and thus permits blind interrogation of the assembled components on a board), Intest (which allows slow speed testing of the core of a circuit), etc.

Limited space prevents us to go further into details. The reader can find a good introduction to the boundary-scan test technique and the associated standard in /3/.

3. Emerging IEEE 1149.4 Standard

The aim of the proposed standard for a Mixed-Signal Test Bus described in the P1149.4 document is to provide standardized approaches to interconnect test, parametric test and internal test. For the first objective, the aim is to provide facilities that allow to detect opens in the interconnections between integrated circuits, and to detect and localize bridging faults. The test structure should allow interconnect testing in full compatibility with IEEE 1149.1 Std. The second objective refers to the problem of measuring the values of discrete components such as pull-up resistors, filter capacitors, etc., that are often interposed between integrated circuits on a board. The third objective relates to the ability to perform internal test of a component. An internal test of a complex component mounted on a board may result in a rather costly testing procedure, hence this option of the proposed standard is not mandatory.

As a whole, P1149.4 can be regarded as an extension of IEEE 1149.1 Std. The 1149.4 extensions are analog boundary modules (ABMs) on every analog functional pin and optionally on other functional pins. Functional pins with ABMs can be accessed via internal analog test bus consisting of 2 lines (AB1, AB2). The bus is connected to the Analog Test Access Port (AT1, AT2) through the Test Bus Interface Circuit (TBIC).

The boundary modules associated with the digital pins are identical to the boundary cells as specified in IEEE 1149.1 Std.

The test register structure is essentially identical to the one defined in IEEE 1149.1 Std. The only difference concerns the boundary-scan register which in the case of P1149.4 contains additional shift-register stages for the control of ABMs and TBIC.

The structure of a basic 1149.4 chip is shown in Fig. 2.

The functional schematic of the ABM module, connected to each analog function pin, is shown in Figure 3. The ABM module consists of six conceptual switches SB1, SB2, SH, SL, SG and SD. (A conceptual switch is defined as a circuit feature that allows two circuit nodes to be electrically connected or disconnected. The conceptual switch is controlled by a digital control signal.)

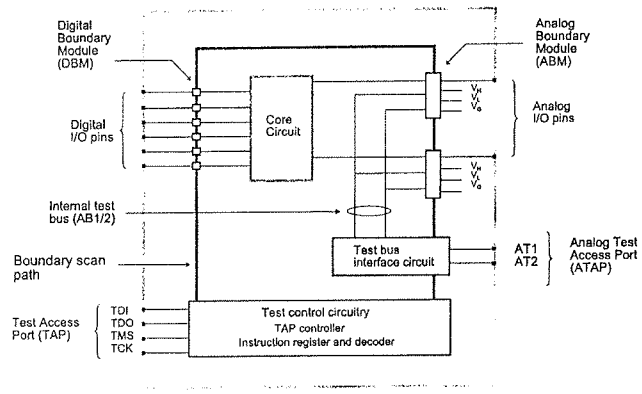

Figure 2: The structure of a basic 1149.4 chip

SB1 and SB2 are used to connect the pin to the internal analog test bus lines AB1 and AB2. In this way, Analog Test Access Port lines AT1 and/or AT2 can be connected to any component pin without the need of physical probing. (The above stated goal of somehow building the test probe directly into the silicon chip is thus achieved by the "virtual probe" feature provided by the ABM framework.) This structure is used to perform component measurements.

A digitizer with a threshold voltage VTH is included in the ABM. It is used to interpret voltages on the pin as digital ones and zeros. This feature can be used for the detection of bridging faults in the interconnect test.

SH and SL are used to set either of two voltage levels (VH or VL) on the pin. This feature allows simple interconnect testing on analog pins to take place at the same time, and using the same methods, as digital interconnect testing.

SG is provided to allow the pin to be connected to the reference quality voltage VG. This feature is used for measurements of board components connected between function pins supported by the AMS modules.

The fifth switch, labeled CD is the core disconnect facility. It provides a controllable mechanism for disconnecting the analog core from the analog function pin while external testing is taking place. From the implementation point of view, it is imperative that the additional series impedance due to the CD is still acceptable for the circuit normal operation.

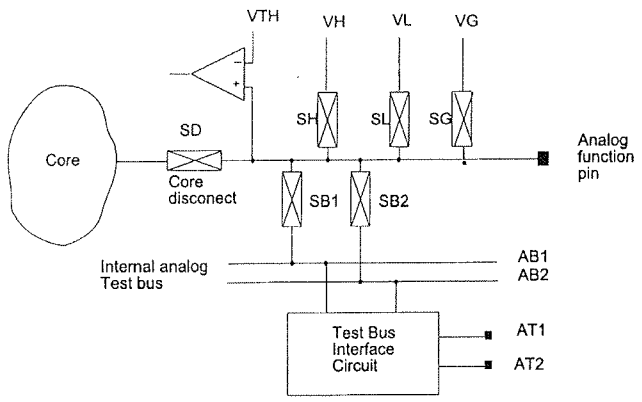

Figure 3: ABM switching structure

Each component conforming to P1149.4 must provide the mandatory instruction: Probe. This instruction allows analog pins to be monitored on AB2, and/or stimulated from AB1 during the normal operation. In order to provide the compatibility with IEEE 1149.1 Std, the mandatory instructions Bypass, Sample/Preload and Extest are also included. The proposed standard allows optional user-defined instructions as well as optional instructions defined in IEEE 1149.1 Std.

P1149.4 document also covers the aspects of measurement methodology. The principles of simple interconnect testing (i.e., testing of open circuits and bridging faults), extended interconnect testing (i.e., measurements of individual analog components) and simple network measurements (when more general networks are connected between the 1149.4 compliant components) are described. For more complicated cases, a special metrology has been developed by Parker et al /4/.

It should be mentioned that P1149.4 also defines differential analog boundary-modules for analog differential pins. However, detailed description of this subject and the associated testing principles are beyond the scope of the paper. Furthermore, analog parametric limits are discussed in the P1149.4 document, including switch limitations, problems associated with incorporation of electrostatic protection, measuring performance and calibration.

For experimental purposes, a series IEEE 1149.4 test chips have been manufactured and distributed by the working group to the interested parties. The samples granted to Jožef Stefan Institute were used for the experimental case study of the possible application of the emerging IEEE 1149.4 Std in the products of Hipot Hyb, /5/. In the following we summarize some experimental results.

4. Experiments with IEEE 1149.4 KLIC Test Chip

Experiments have been performed using the IEEE 1149.4 KLIC Test Chip /6/ in an active RC filter implemented in thick-film hybrid technology. The goal was to analyze the influence of IEEE 1149.4 ABMs on the circuit performance. For the case study we have chosen an active RC notch filter (as a part of a thick-film hybrid circuit for a telecommunication application) with quite exacting characteristics. The impact of non-ideal op-amp on pole and zero locations is considered in the early design phase and finally compensated by trimming the resistor(s) in the production process. The introduced ABMs have additional impact on filter characteristics. The question is, how much do they actually influence circuit performance, and if it is possible to compensate their impact in practice. In our case we inserted ABMs in the circuit as shown in Figure 4 and measured amplitude and phase characteristics. Since the characteristics depend on the amplitude of the input signal, we made measurements at two different input signals (Vin = 20 mV and 100 mV).

In the case when only ABM1 was inserted, the central frequency f0 shifted towards higher frequencies and the gain at f0 increased. For the input signal Vin = 100 mV,

the frequency shift of f0 was 0.3%, and the gain has increased for 2.12 dB. At the lower input signal Vin = 20 mV, the frequency shift was a little smaller (about 0.01%), and the gain at f0 changed for 2.37 dB. The changes are due to the capacitive effect of the inserted ABM1, while the serial resistance of the ABM1 module can be neglected.

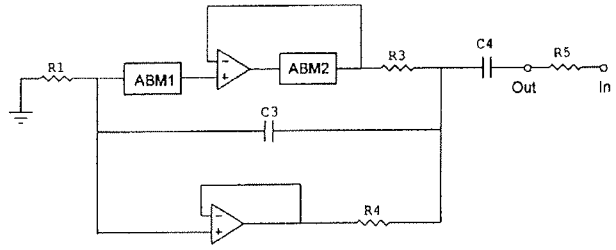

Figure 4: active RC notch filter with inserted ABMs

In the case when only ABM2 was inserted, the central frequency f0 slightly shifted towards higher frequencies and the gain at f0 decreased. The changes are due to the on-resistance of the ABM2, while its capacitive effect can be neglected.

Figure 5 depicts situation when both ABM1 and ABM2 were inserted and Vin = 20 mV. Note that the change of circuit characteristic was smaller than in the cases when only ABM1 or ABM2 were employed. This is due to the fact that the impact of ABM1 and ABM2 on the filter quality partially compensate.

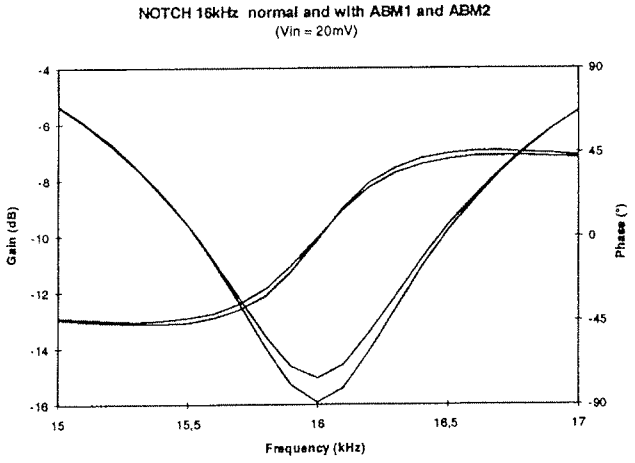

Figure 5: Measured frequency and gain when both ABM1 and ABM2 were inserted

In our case, the resulting changes of the central frequency f0 are not critical since they can be easily adjusted. Hence the application of IEEE 1149.4 in this particular case is feasible.More efforts would be needed to achieve the required quality in the case of high performance circuits (narrow tolerance ranges).

Conclusion

Boundary-Scan has proved to be an effective test technique for digital circuits and systems and its standard IEEE 1149.1 has been widely accepted in practice. Likewise, we can expect a similar success of the emerging IEEE 1149.4 in the area of mixed-signal circuits. The costs of implementing include 1149.1 TAP controller (resulting in area overhead), extra pins (at least 4 for compatibility with IEEE 1149.1 plus 2 for the analog test bus) and some inevitable performance degradation due to the additional capacitance and resistance of individual parts of ABMs, /7/. On the other hand, the benefits of increased testing facilities and diagnosability are likely to outweigh the costs and P1149.4 is likely to become essential solution for automatic test of mixed-signal circuits and systems. Let us conclude this brief introduction to P1149.4 with a daring idea stated at the International Test Conference 1997 by Steve Sunter, one of the members of the 1149.4 working group: "Just as the Internet evolved into the World Wide Web, and high performance sound, graphic, and programming were developed for the medium, we can expect to see dramatically better design and test solutions developed to fit into the P1149.4 framework. The Internet and 1149.4 might eventually link together!" /8/.

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