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A 4.1-bit, 20 GS/s Comparator for High Speed Flash ADC in 45 nm CMOS Technology

M.J. Taghizadeh. Marvast, H.Sanusi, M. A. Mohd. Ali*

Universiti Kebangsaan Malaysia, Bangi, Malaysia

Abstract: A 4.1-bit, high speed comparator for high-speed flash analog-to-digital converter and K-band applications that can work at a sampling rate of 20GS/s is presented in this paper. This fully differential comparator consists of three stages using a new structure to improve its performance. The offset voltage of the designed comparator has been reduced by means of an active positive feedback. The CMOS positive feedback and a new structure as output circuit are used to improve sampling rate and performance of comparator. The analyses and simulation results were obtained by using CMOS parameters. The comparator can operate with a 1 V peak to peak input range consuming 0.561 mW. The predicted performance is verified by analyses and simulations using HSPICE tool.

Keywords: Analog –to- Digital converter, Comparator, Preamplifier.

4.1-bitni 20 GS/s komparator za hitrobliskovni ADC v 45 nm CMOS tehnologiji

Izvleček: V članku je predstavljen 4.1-bitni hiter komparator za hitrobliskoven analogno-digitalen pretvornik in K-pasovne aplikacije, ki lahko delujejo pri vzorčni frekvenci 20 GS/s. Polno diferencialen komparatoru uporablja za izboljšanje učinkovitosti novo tristopenjsko strukturo. Ničelna napetost načrtovanega komparatorja je bila zmanjšana v smislu pozitivne povratne vezave. Pozitivna CMOS povratna vezava in nova struktura izhodnega vezja je bila uporabljena za izboljšanje vzorčenja in učinkovitosti komparatorja. Analize in rezultati simulacij so bile opravljene na osnovi CMOS parametrov. Komparator deluje pri napetosti 1 V (peak to peak)in porabi 0.564 mW. Predpostavljena učinkovitost je bila preverjena s simulacijskim orodjem HSPICE.

Ključne besede: anogno digitalni pretvornik, komparator, predojačevalec

** Corresponding Author's e-mail: taghiza@eng.ukm.my*

1. Introduction

Flash analog-to-digital converters (ADC) with X-band and K-band frequency sampling rates are critical components for applications such as radar, signal capture, satellite, digital oscilloscopes and waveform recorders [1]. Today researchers and the industry have extended the requirement for higher frequency and higher sample rate. Flash can generally achieve the higher sampling rates, with the comparator limiting the maximum achievable sampling speed. In addition, this comparator can be used for UWB, X-band and K-band technology that offer a lot of capability for the design of communications devices requiring very high performance and low power consumption. The comparators published in years [2][3][4] still have relatively high power consumption and operate with sampling rate lower than the expected future requirement. In this paper a new CMOS positive feedback is proposed to increase the speed of track and hold (T/H) of the comparator. A new structure is also proposed to achieve the overall high speed for the comparator. The comparator design incorporates various techniques to lower its power consumption and improve its overall performance. The comparator architecture is described in Sect. 2. The preamplifier design, T/H and output domino logic are presented in Sect. 3. Section 4 shows the simulation results, and finally Sect. 5 is the conclusion.

2. Architecture

Fig. 1 illustrates the comparator architecture that consists of preamplifier, track&hold (T/H) and output circuits. The comparator structure is fully differential and consists of three stages. The first stage is a low gain differential amplifier with resistive loads (RD), which is high range band with.

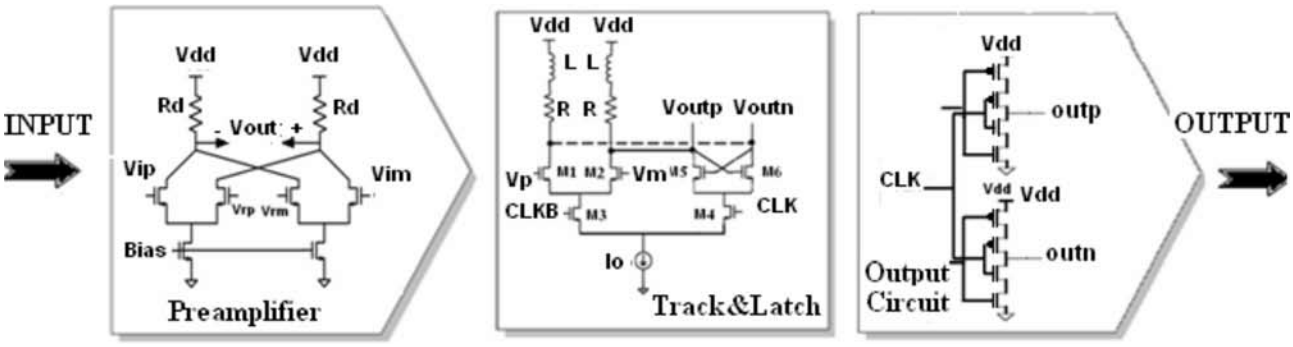

Figure 1: Schematic of comparator.

The comparator with resistive loads shows better linearity offset and gain response in comparison with comparators with active or diode loads. The first stage of comparator is used to reduce the input offset of comparator. The second stage is a CMOS track and hold with positive feedback and used of inductor and current source to reduce regenerative time. The domino output circuit that is new our suggestion circuit as shown in right block of Fig. 1is used instead of SR Latch to support the comparator in high sampling rate.

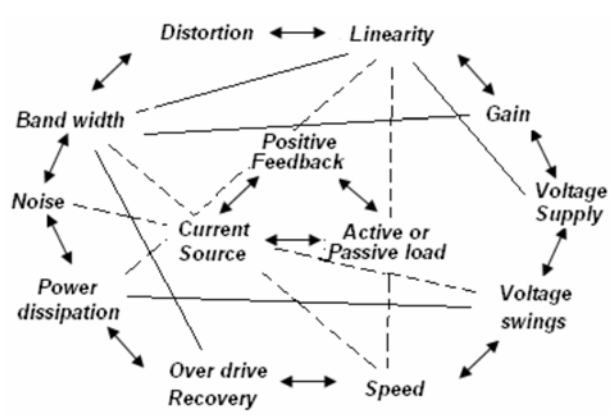

Figure 2: Relationship between comparator design parameters

In practical implementation, any random or systematic imbalance of the circuit creates an offset in the comparator. Offsets are classified as static or dynamic according to their origins. The fully differential comparator has many advantages to prevent supply and kickback noise and therefore, achieves a big dynamic range. The differential amplifier has better linearity.

It has to be clear, which aspect of comparators performance is important? In addition to power dissipation there are several items which may be important, such as supply voltage, gain, swing voltage, band width, distortion input offset, linearity and over drive recovery. In practice, most of these parameter trade with each other, making the design a multi-dimensional optimization problem. Illustrated in Fig. 2 such trade-off present many challenges in the design of high quality comparator for flash ADC, requiring intuition and experience to arrive at an acceptable compromise.

3. Comparator Design

3.1. Preamplifier

The low noise amplifier (LNA) is shown in Fig. 3. The main role of LNA is to reduce the input referred offset of the comparator. The preamplifier acts as an isolator between voltage reference and T/H to improve bandwidth and decrease input offset. The preamplifier has two inputs for differential analog signal and two inputs for voltage reference.

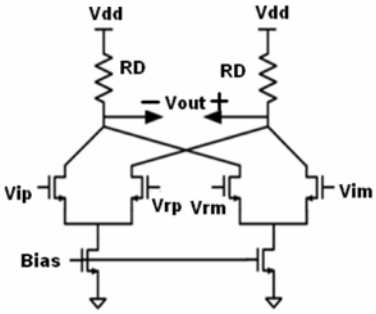

Figure 3: Preamplifier.

There is a relation between offset and W/L of the preamplifier that is equal to:

$$V_{offset} = \Delta Vt + \frac{1}{gm}\left(\frac{\Delta w_1}{w_1} + \frac{\Delta L_1}{L_1} + \frac{\Delta w_2}{w_2} + \frac{\Delta L_2}{L_2} + \ldots + \frac{\Delta w_n}{w_n} + \frac{\Delta L_n}{L_n}\right) \quad (1)$$

where *Vt* is threshold voltage and gm is transconductanc *w* and *L* are width and length respectively [5] [6].

Equation (1) indicates that with increase of transistor size (W) offset will be reduced, but this increase depends on the design. In addition, swing, bandwidth, output capacitance and linearity are important factors to choose the load of preamplifier. The linearity and frequency response of the preamplifier with passive load is better than preamplifier with active load. It is important to note that, with increasing LNA gain, the bandwidth is also decreased.

3.2. Comparator core (T/H) and Output circuit

The comparator core is shown in Fig. 4. The load is formed by the series combination of a resistor and an inductor. Vp and Vm are the differential analog inputs signal from the preamplifier. It has input differential pairs (MI and M2) that turn on when the clock is low and track the input from the previous stage. When the clock is high, the comparator goes into hold mode. In this paper CMOS positive feedback is applied to improve speed of comparator and decrease the regenerative time in latching mode. The passive inductor peaking technique is also employed in the T/H circuit to enhance the bandwidth [7] [8] [9]. The comparator core is designed using new structure. This type of design is the most efficient in terms of speed and very low swing signal operation. Therefore, it's reduced output swing and hence low-power dissipation. In other words, the domino output circuit as shown in Fig. 1 is used instead of SR Latch to support the comparator in high sampling rate operation. The combination of T/H and output circuit creates a fast structure for the comparator. Domino logic as output circuit operates in two phases, the precharge phase and the evaluation phase. In the precharge phase, output is precharged from low to high, while in the evaluation phase, output will either be discharged from high to low or remain high.

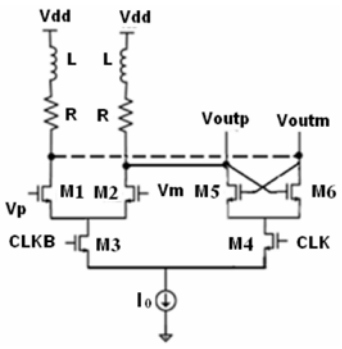

Figure 4: Comparator core (Track/Hold).

4. Simulation Results

The proposed comparator structure is designed using 45 nm CMOS technology. Simulation result was obtained by using HSPICE tool Table 1shows the summary of comparator performance, in comparison with the designs in [2] and [3].

The new comparator dissipates only 0.561 mW at 20 GS/s. Fig. 6shows the output wave of comparator with1 GHz analog input signal and clock frequency of 20 Gs/s. The FFT of the signal at input frequency of 6.5 GHz and sampling rate of 20 Gsample/s is shown in Fig. 5.

5. Conclusion

In this paper, a 45 nm CMOS K-band comparator for high speed low power flash ADC is proposed. CMOS positive feedback and a new structure as output circuit are used to improve sampling rate and performance of comparator. We have used new core structure and domino logic circuit to speed up, reduce crosstalk and save power consumption of comparator. The measured ENOB is 4.1 bits at 20 GS/s with a 6.5 GHz sine input signal.

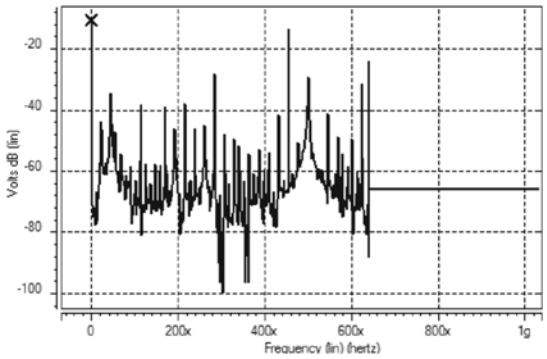

Figure 5: FFT at input frequency of 6.5 GHz and sampling rate of 20 Gsample/s.

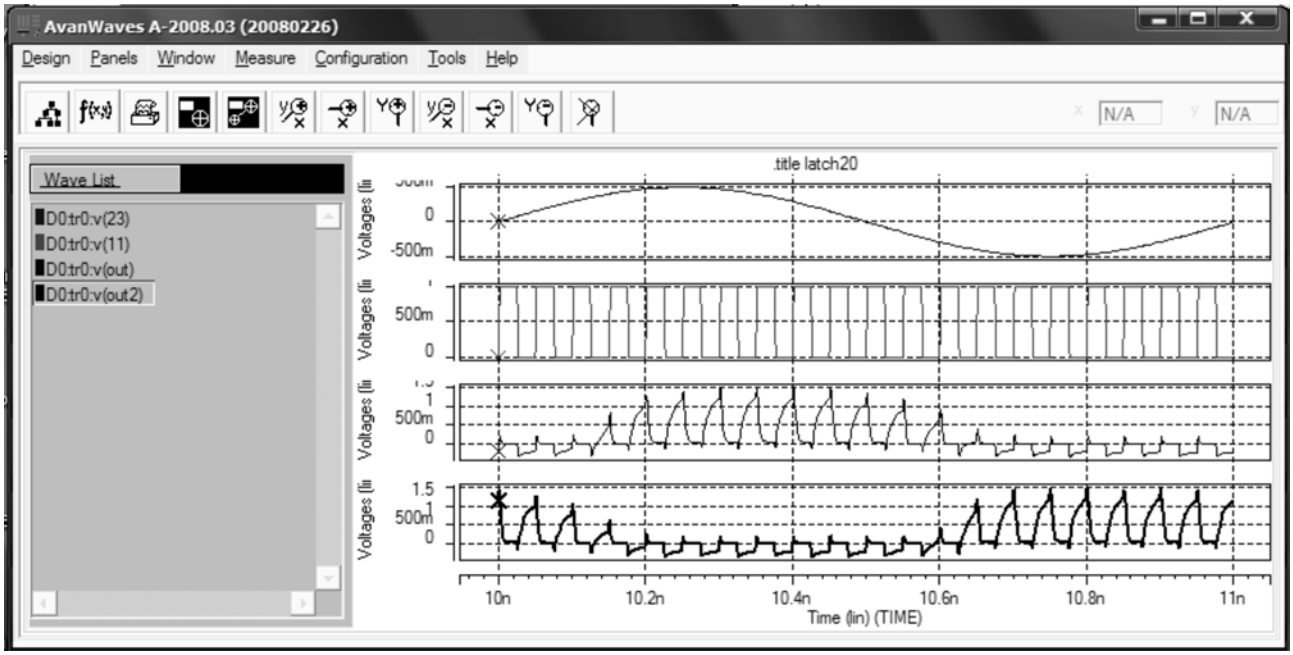

Figure 6: shows output wave of comparator at Fin=1GHz, Fclk=20Gs/s.

Table 1: Performance comparision

Aurhor	Supply voltage	Sampling frequency (fs)	ENOB Effective number of bits (ENOB)	Process	Power dissipation	Years
[3]	1 v	4 (GS/s)	4	90 nm CMOS	3.6 mW	2007
[4]	1.2 v	0.5 (GS/s)	3.5	130 nm CMOS	148 µW	2007
[2]	2.2 v	11 (GS/s)	3	120 nm CMOS	-	2008
This work	1.8 v	20 (GS/s)	4.1	45 nm CMOS	0.561 mW	2010

References

1 Federal Communications Commission. (2002). First Report and Order Revision of Part 15 of the commission's rules regarding ultra-wideband systems. ET Docket No. 98-153.

2 Yuan Yao, Foster Dai, J. David Irwin and Richard C. Jaeger. (2008). A 3-Bit 2.2V 3.08pJ / Conversion-Step 11GS/s Flash ADC in 0.12um SiGe BiCMOS Technology. IEEE Bipolar /BiCMOS Circuit and Technology. Meeting (BCTM), Monterey, California.

3 International A. Mohan, A. Zayegh, A. Stojcevski, R. Veljanovski. (2007). High Speed Ultra Wide Band Comparator in Deep Sub-Micron CMOS. IEEE International Symposium on Integrated Circuits. ISIC07, Singapore.

4 J. P. Oliveira, J. Goes, N. Paulino, J. Fernandes, (2007) low power low voltage CMOS comparator for 4-bit FLASH ADCS for UWB applications. 14th International Conference, MIXDES 07.

5 B. Razavi, Principles of Data Conversion System Design, IEEE Press, 1995.

6 A. Mohan, A. Zayegh, and A. Stojcevski.(2007) A High Speed Analog to Digital Converter for Ultra Wide Band Applications. IFIP International Federation for Information Processing, pp. 169-180.

7 S. Park and M. P. Flynn,.(2006) A regenerative comparator structure with integrated inductors. IEEE Trans. Circuits Syst. I, vol. 53, pp. 1704–1711.

8 B. Razavi, Principles of Data Conversion System Design. (1994). Hoboken, NJ: Wiley-IEEE Press, p. 183.

9 S. S. Mohan, M. D. M. Hershenson, S. P. Boyd and T. H. Lee. (2000). Bandwidth extension in CMOS with optimized on-chip Inductors. IEEE J. Solid-State Circuits, vol. 35, no. 3, pp. 346–355.

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