A CMOS MEMBERSHIP FUNCTION CIRCUIT EMPLOYING SINGLE CURRENT DIFFERENCING BUFFERED AMPLIFIER

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Key words: MFC, CDBA, PSPICE, CMOS

Abstract: The author proposes a new fully integrable Membership Function Circuit (MFC) using a Current Differencing Buffered Amplifier (CDBA) which employs two second generation current conveyor (CCII) and a voltage buffer. This MFC achieves basic membership functions such as trapezoidal, triangle, S-shape, and Z-shape. The characteristics (width, height, and position) of the implemented MFC are easily adjusted by varying left and right voltages and bias currents. Since the proposed MFC is implemented with a single CDBA block with simple structure, it can be capable of high-speed operation and integrated as a circuit to cover small area of a chip. The behaviour of the proposed MFC has been verified by PSPICE using the model parameters with 0.5 mm MIETEC CMOS process. The proposed MFC is voltage-input current-output and CMOS based structure with low supply voltages (± 1.5V). Therefore, it is suitable for both current-mode and low-voltage fuzzy and neural hardware.

Izvedba CMOS MFC vezja z uporabo enojnega tokovnega diferenčnega ojačevalnika

Kjučne besede: MFC, CDBA, PSPICE, CMOS

Izvleček: V prispevku predlagamo izvedbo popolnoma itegriranega MFC vezja (Membership Function Circuit) z uporabo CDBA, ki uporablja dva CCII druge generacije in napetostni vmesnik. S pomočjo tako izvedene MFC pridemo do osnovnih funkcij, kot so trapezoidalna, trikotna, S-oblike in Z-oblike. Karakteristike MFC zlahka prilagajamo s spreminjanjem napetosti in napajalnih tokov. Ker je MFC izveden z enim CDBA blokom z enostavno strukturo, je hiter in se da integrirati na majhno površino čipa. Vedenje MFC smo preverili s pomočjo programa PSPICE z uporabo modelnih parametrov procesa 0.5 µm MIETEC CMOS. MFC je izveden z napetostnim vhodom in tokovnim izhodom s tehnologijo CMOS pri nizki napajalni napetosti +-1.5V.

1. Introduction

The Membership Function Circuit (MFC) or fuzzifier is one of the most important units in the fuzzy logic controllers (FLC). The various MFC hardware have implemented in literature /1-10/. A high-speed digital MFC based on BiCMOS technology has been proposed in /1/ but the fabrication cost is high. The other MFC designs with current-mode analogue circuits were proposed in /2-3/. However the speed of these circuits is low. Then, the sub-threshold membership function circuit was proposed in /4/. Although this MFC has low power consumption, the output current linearity and accuracy of the circuit is low. Most of the membership function circuits in literature /5-6/ have been designed to provide two membership functions as triangle and trapezoidal shapes in general. In addition to these functions, for generating Z-shape and S-shape membership functions are required extra circuits in original membership function circuit /7-8/. A voltage-input/current-output programmable Gaussian function network with capacitors for the programmability is introduced in /9/. But, the capacitors in network can be refreshed to maintain an accurate programmed value. Also, the reference current needs to be adjusted to control the amplitudes of the output current in their design. The other MFC with good programmable features is presented in /10/. In this MFC, all using transistors are operated in weak inversion region and narrow input current range. The dynamic range of this circuit is small and speed is low for general applications because of the inherent limitations of transistors in weak inversion /11/.

In this study, a new MFC using CDBA is presented. The proposed MFC has capability of generating four standard membership functions without extra devices. Also, it can be operated high speed and implemented simple structures with easy design automation.

The outline of this paper is as follows. Section II briefly defines a basic Current Differencing Buffered Amplifier (CDBA) and proposed Membership Function Circuit (MFC) is theoretically described in detailed. Section III evaluates a current-mode MFC with PSPICE simulation experiments. In Section IV, the overall conclusions are given.

2. Circuit description

The fuzzification block maps the measured fuzzy input variable(s) of a fuzzy system into a suitable range that corresponds to the universe of discourse, and then converts the crisp input value into a fuzzy set. In many fuzzy and neuro-fuzzy applications, a Gaussian or triangular function is generally used in the fuzzification process of the Fuzzy Logic Controllers (FLCs).

In this study, we used a CDBA into our proposed MFC. The modified circuit structure of the CDBA in /12/ and circuit symbol is shown in Fig. 1. The characteristic equation of this element can be given as

$$V_p = V_n = 0, \quad I_z = I_p - I_n, \quad V_w = V_z \tag{1}$$

Here, current through z-terminal follows the difference of the current through p-terminal and n-terminal. Input terminals, p and n, are internally grounded. A possible CMOS realization of CDBA consisting of a differential current controlled current source (DCCCS) followed by a voltage buffer is shown in Fig. 1. The CDBA offers the well-known advantages of the CFA and CCII, such as high slew-rate, wide bandwidth and simple implementation. According to the above equations, this element converts the difference of the input currents I_p and I_n, into the output voltage V_w, through the impedance which will be connected to terminal 'z'. Therefore, the CDBA can be considered as a trans-impedance amplifier and, from this viewpoint, it is similar to the current feedback amplifier (CFA) /13/. Furthermore, since the CDBA can be considered as a collection of current-mode and voltage-mode unity gain cell, this element is free from many parasitic effects and is expected to be suitable for high-frequency operation /14-16/. It can be operated in both current-mode and voltage-mode in a wide frequency range and can also be implemented with CMOS technology.

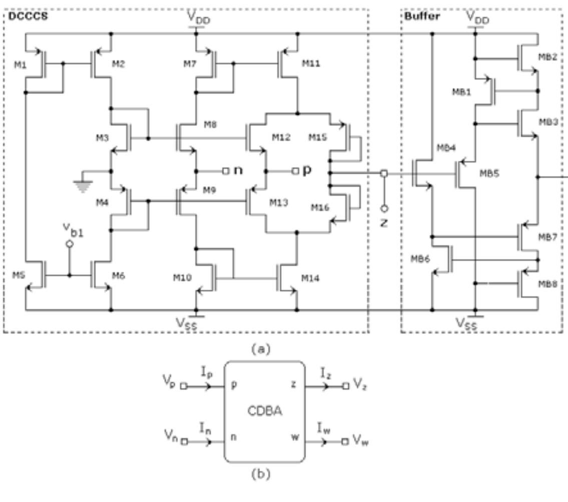

Fig. 1 (a) Simplified circuit of modified CDBA and (b) its symbol

The proposed MFC is shown in Fig. 2 which composed of two P channel MOS based cascode current mirrors, a single CDBA, two bias current sources (I_{BR}, I_{BL}), and four N channel MOS transistors. The PMOS current mirrors are carried out reversing right and left currents from input NMOS transistors. The CDBA is operated to take difference between right and left currents from PMOS cascode mirrors.

The MOSFETs, M1, M2, M3, and M4, are the identical transistors, working in saturation region. In condition that $V_{GS}>V_T$ and $V_{DS}>V_{GS}-V_T$, the expression of drain current for the simple MOS transistor operating in saturation region is

$$I_{ds} = \mu C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \tag{2}$$

$$I_{ds} = K(V_{GS} - V_T)^2 \tag{3}$$

where **K** is trans-conductance parameter. μ, C_{ox}, W, and L stand for carrier effective mobility, gate oxide capacitance per unit area, width, and length of the channel, respectively.

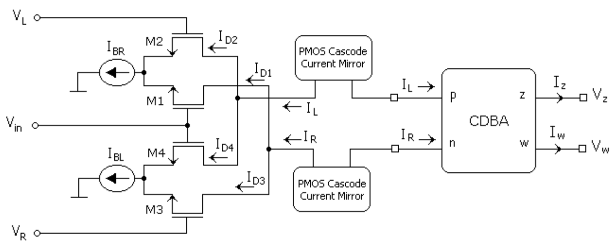

Fig. 2. The block representation of proposed CDBA-based MFC

In Fig.2, V_L and V_R can be adjusted to determine left and right side of membership function such as trapezoidal. The branch currents of proposed MFC are given as follows:

$$I_{D1} = \frac{I_{BR}}{2} + V_{D1}\frac{K_1}{2}\sqrt{\frac{2I_{BR}}{K_1} - V_{D1}^{\ 2}} \tag{4}$$

$$I_{D2} = \frac{I_{BR}}{2} - V_{D1}\frac{K_2}{2}\sqrt{\frac{2I_{BR}}{K_2} - V_{D1}^{\ 2}} \tag{5}$$

$$I_{D3} = \frac{I_{BL}}{2} + V_{D2}\frac{K_3}{2}\sqrt{\frac{2I_{BL}}{K_3} - V_{D2}^{\ 2}} \tag{6}$$

$$I_{D4} = \frac{I_{BL}}{2} - V_{D2}\frac{K_4}{2}\sqrt{\frac{2I_{BL}}{K_4} - V_{D2}^{\ 2}} \tag{7}$$

where difference voltages, V_{D1} and V_{D2}, are given by

$$V_{D1} = V_{in} - V_L \quad \text{and} \quad V_{D2} = V_{in} - V_R \tag{8}$$

Also, right and left currents of MFC, I_R and I_L, can be obtained with KCL as follows:

$$I_R = I_{D1} + I_{D3} \quad \text{and} \quad I_L = I_{D2} + I_{D4} \tag{9}$$

The output current, I_{out}, is equal to difference of left and right currents of MFC and it is obtained from z-terminal of CDBA.

$$I_{out} = I_L - I_R \tag{10}$$

In condition that $K_1=K_2=K_3=K_4=K$ and $I_{BR}=I_{BL}=I_B$, the output current of MFC can be given in Eq. (11).

$$I_{out} = K\left[(V_{in} - V_L)\sqrt{\frac{2I_B}{K} - (V_{in} - V_L)^2} + (V_{in} - V_R)\sqrt{\frac{2I_B}{K} - (V_{in} - V_R)^2}\right] \tag{11}$$

V_L must be greater than V_R in order to generate the Gaussian-type curve. The drain current equations of the MOSFETs are valid when voltage from gate-to-source, V_{GS}, is higher than V_T threshold voltage of related transistor. Hence, the following condition must be as follows:

$$\sqrt{\frac{2I_B}{K_i}} < V_{Di} < 2\sqrt{\frac{2I_B}{K_i}} \qquad i = 1,2 \tag{12}$$

3. Simulation results

In order to verify the above given theoretical analysis, a new MFC is designed using the proposed configuration of Fig.2. The behaviour of the implemented CDBA-based MFC was confirmed with 0.5 µm MIETEC CMOS process parameters by PSPICE simulation experiments. The device dimensions of the channel width (W) and the channel length (L) for M_1, M_2, M_3, and M_4 are 10 mm and 4 µm, respectively. For all transistors operated in saturation region, bias currents of differential pairs, I_{BR} and I_{BL}, are adjusted to 10 µA. The power supply is V_{DD}= -V_{SS}=1.5 V.

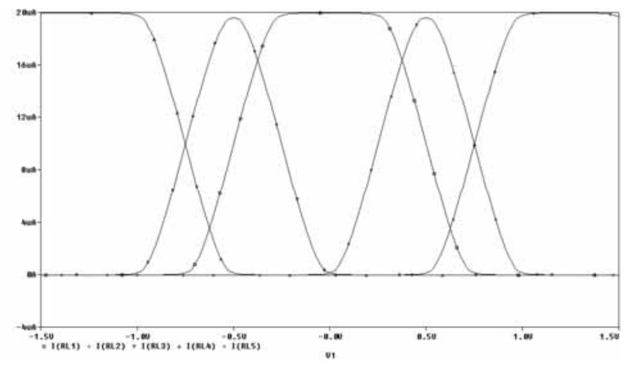

Fig. 3. The basic membership function output graphs of proposed MFC

The simulation result of basic four membership functions such as trapezoidal, S and Z shape obtained by proposed MFC is shown in Fig. 3. Here, right voltage V_R must be bigger than left voltage V_L. For example, in this study, triangular membership shape is obtained on condition that V_R-V_L=0.5 V.

Fig. 4 (a) and (b) show the width adjusting of MFC towards right and left, respectively. In this DC analysis result, the one of the adjusting voltages is fixed a constant value for extension to right or left direction of membership function. Also, the height of membership function (amplitude of output current) can be varied with adjusting bias currents, I_{BR} and I_{BL}, as shown in Fig. 5. Here, bias currents are varied between [10 µA; 50 µA] in 5 µA steps for V_R –V_L= 1V, i.e., trapezoidal membership shape centred 0 V. Also, the CDBA based MFC has capable of high-speed operations because of using CDBA structures in this design has got high frequency range. The frequency response of the MFC is shown in Fig. 6. The bandwidth of the MFC is about 266 MHz (for -20 dB) as shown in Fig. 6. Low power low voltage technology offers the possibility of connecting the bulk and the source of transistors. In this case, the input current swing increases but the bandwidth is reduced substantially, as it is expected

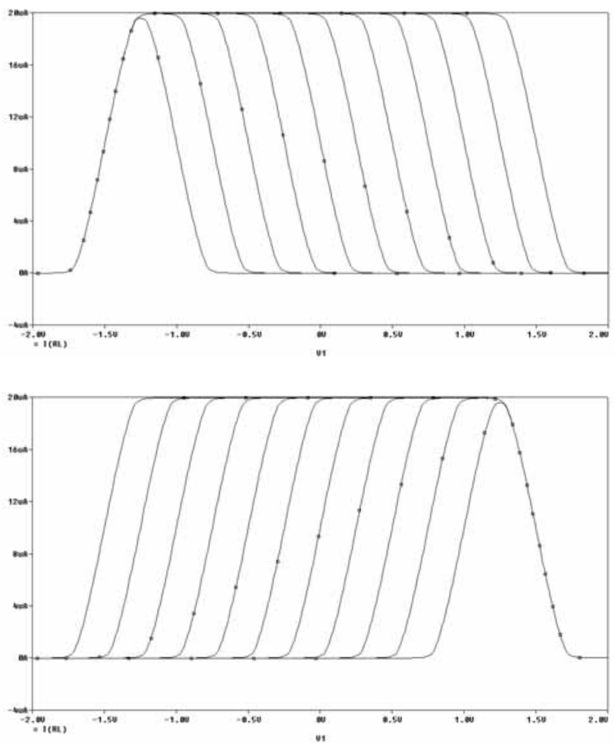

Fig. 4. Width adjusting of proposed MFC (a) Right directions, and (b) Left directions

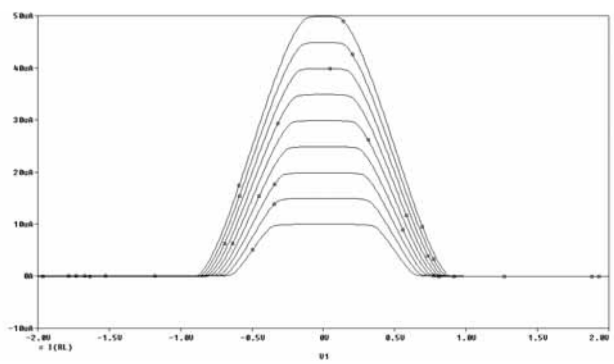

Fig. 5. Width adjusting of membership function with varied bias currents, I_{BR} and I_{BL}, for trapezoidal shape centered 0V. (I_{BR} = I_{BL} and between [10 µA; 50 µA] with 5 µA steps)

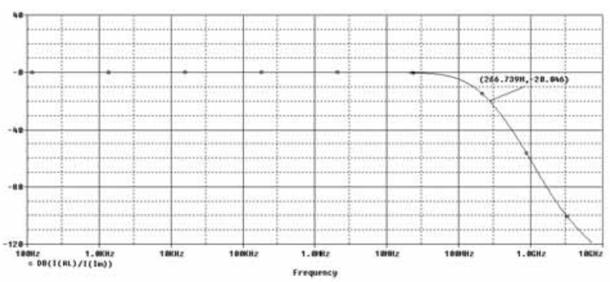

Fig. 6. Frequency response of the proposed CDBA based Membership Function Circuit (MFC)

4. Conclusion

A new and fully integrable membership function circuit (MFC) is proposed by using single CDBA. The performance of proposed MFC is analyzed based upon PSPICE simulation experiments. This MFC operates low supply voltages as ± 1.5 V. Also, the proposed MFC has got both wide input current range and high frequency response. The proposed circuit configuration consists of a single CDBA and four N channel MOS transistors operated in saturation region. This MFC is suitable for both current-mode and voltage-mode fuzzy hardware because of a voltage buffer is available in CDBA structure. Basic four membership functions can be implemented by this MFC. The characteristics such as width, height, and position of implemented membership functions are easily adjustable by varying left and right voltages, and bias currents.

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