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Measurement of NBTI Degradation in p-channel Power VDMOSFETs

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Abstract: In this paper we report on the use of a cost-effective stress and measurement setup for investigations of NBTI in commercial p-channel power VDMOS transistors IRF9520. The effects of stress voltage and temperature under both static and pulsed bias stress conditions are briefly discussed, and dynamic recovery effects are evaluated by varying the duty cycle and frequency of the pulsed stress voltage applied. Less significant degradation of threshold voltage found after pulsed bias stressing is ascribed to the dynamic recovery, and its tendency to further decrease with lowering the duty cycle and/or increasing the frequency of the pulsed voltage used for stressing is explained in terms of the enhanced dynamic recovery effects.

Keywords: Measurement, NBTI, VDMOSFET, Threshold voltage

Meritev NBTI degradacije v p-kanalu močnostnega VDMOSFETa

Izvleček: Članek opisuje stroškovno učinkovito uporabo merilne in testne opreme za preučevanje NBTI v komercialnih p-kanalnih VDMOS IRF9520 tranzistorjih. Opisani so vplivi bremenske napetosti in temperature na statične in pulzne razmere. Obravnavani so dinamični efekti okrevanja s spreminjanjem delovnega cikla in frekvence pri pulzni bremenski napetosti. Ugotovljena je bila manj pomembna degradacija pragovne napetosti pri pulznem vzbujanju je vzrok dinamičnega okrevanja. V okviru dinamičnega okrevanja je razložen je trend nadaljnje degradacije pri manjšem delovne ciklu i/ali višji frekvenci pulznega signala.

Ključne besede: Meritve, NBTI, VDMOSFET, pragovna napetost

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1 Introduction

Negative bias temperature instability (NBTI) has been found to occur mostly in p-channel MOSFETs operated at elevated temperatures (100 – 250 °C) under negative gate oxide fields in the range 2 – 6 MV/cm [1–8]. NBTI is manifested as the decrease in device transconductance (g_m) and absolute drain current (I_{Dsat}) and the increase in device threshold voltage (V_T) and absolute "off" current (I_{off}) [3]. The phenomenon had been known for many years, but has only recently been recognized as serious reliability issue in state-of-the-art MOS integrated circuits with ultra-thin gate oxide devices. Several factors associated with device scaling have contributed to bringing NBTI to the attention of device and circuit designers: first, operating voltages have not been reduced as rapidly as gate oxide thickness, resulting in higher fields and increased chip temperatures, which both enhance NBTI; second, threshold voltage scaling has not kept pace with operating voltage, which has resulted in larger percentage degradation of drain current for the same ΔV_T; and third, the addition of nitrogen into the thinned gate oxides for leakage reduction has had the side effect of increasing NBTI [2].

Regarding device electrical parameters, NBT stress-induced threshold voltage shifts are most critical and can put serious limit to a lifetime of p-channel devices with gate oxide thinner than 3.5 nm [5]. Several models of microscopic mechanisms responsible for the observed V_T shifts have been proposed [1–8], but these are beyond the scope of this paper and will not be discussed. However, it is important to offer a brief answers to a couple of basic questions that could arise so far, such as: (*i*) Why the NBTI is of greater concern in p-channel devices compared to n-channel ones? (*ii*) Why the negative bias causes more considerable degradation than positive bias? The bias temperature stress-induced V_T shifts are generally known to be the consequence

of underlying buildup of interface traps and oxide-trapped charge due to stress-initiated electrochemical processes involving oxide and interface defects, holes and/or electrons, and variety of species associated with presence of hydrogen as the most common impurity in MOS devices. An interface trap is a trivalent silicon atom with an unsaturated (unpaired) valence electron at the SiO_2/Si interface. Unsaturated Si atoms are additionally found in SiO_2 itself, along with other oxide defects, the most important being the oxygen vacancies. Both oxygen vacancies and unsaturated Si atoms in the oxide are concentrated mostly near the interface and they both act as the trapping centres responsible for buildup of oxide-trapped charge. Interface traps readily exchange charge (electrons or holes) with the substrate and they introduce either positive or negative net charge at interface, which depends on gate bias: the net charge in interface traps is negative in n-channel devices, which are normally biased with positive gate voltage, but is positive in p-channel devices as they require negative gate bias to be turned on. On the other hand, the charge found trapped in the centers in the oxide is generally positive in both n- and p- channel MOS transistors and cannot be quickly removed by altering the gate bias polarity [9]. Therefore, absolute values of V_T shifts due to stress-induced oxide-trapped charge and interface traps in n- and p-channel MOS transistors, respectively, can be expressed as [9–11]:

$$\Delta V_{Tn} = \frac{q\Delta N_{otn}}{C_{ox}} - \frac{q\Delta N_{itn}}{C_{ox}} \quad (1)$$

$$\Delta V_{Tp} = \frac{q\Delta N_{otp}}{C_{ox}} + \frac{q\Delta N_{itp}}{C_{ox}} \quad (2)$$

where q denotes elementary charge, C_{ox} is gate oxide capacitance per unit area, while ΔN_{ot} and ΔN_{it} are area densities of oxide-trapped charge and interface traps, respectively. Similar amounts of oxide-trapped charge and interface traps are generated in both n- and p-channel devices [2], but above consideration clearly shows that the net effect on threshold voltage, ΔV_T, must be greater for p-channel devices, because in this case the positive oxide charge and positive interface charge are additive. As for the question (*ii*), it seems well established that holes are necessary for BTI degradation [1–8], which provides a straight answer since only negative gate bias can provide holes at the SiO_2/Si interface. This is also an additional reason why the greatest impact of NBTI occurs in p-channel transistors since only those devices experience a uniform negative gate bias condition during typical CMOS circuit operation.

In spite of continuous tendency in nanometre scale technologies to have the gate oxide thinned down, the interest in ultra-thick oxides has remained owing to widespread use of MOS technologies for realisation of power devices. Vertical double-diffused MOSFET (VD-MOSFET) is an attractive power device for application in high-frequency switching power supplies owing to its superior switching characteristics, which enable operation in a megahertz frequency range [12, 13]. High-frequency operation allows the use of small passive components (transformers, coils, capacitors) and thus enables the reduction of overall weight and volume, making the power VDMOSFETs especially suited for application in power supply units for communication satellites. Also, power VDMOSFETs are widely used as the fast switching devices in home appliances and automotive, industrial and military electronics [14]. Degradation of power MOS devices under various stresses (irradiation, high field, temperature, and even hot carrier injection) has been subject of extensive research (see, for example, [15] and references listed therein), but only few research groups seem to have addressed the NBTI in these devices [14, 16–26]. However, increased electric fields and elevated chip temperatures are frequently approached during the routine operation of power devices in automotive and industrial applications [14], so the investigations of NBTI in power MOSFETs are of importance as well.

Several new measurement techniques have recently been developed in order to get better insight into the microscopic mechanisms of NBTI [27–31]. In this paper we will describe a measurement technique that is particularly suitable for NBTI measurements on power VDMOS transistors. Few experimental results for both static and pulsed NBT stress conditions of investigated devices will be discussed as well.

2 Stress and measurement setup

Threshold voltage shift in the NBTI tests is determined by using various measurement techniques [27–31], including the one based on current–voltage (*I–V*) characteristics. The stress voltage, either static (dc) or dynamic (ac) [32], is removed from the device to perform the measurement, and the threshold voltage is determined from the measured *I–V* characteristic. In order to minimize the dynamic recovery effects on threshold voltage value, the measurement must be completed as fast as possible. Once the measurement has been done, the stress voltage is switched back to the device. Recent developments in measurement technology have made possible fast and on-the-fly (when the stress is even not being interrupted) NBTI techniques with the measurement times reduced down to 1 μs [33–39] or even lower [28]. Measurements are spot, utilizing one or a few points on the transfer *I–V* characteristic [34], so a compromise between accuracy and speed is achieved.

This is fully applicable to thin gate oxide transistors in CMOS technology, where the stress voltage magnitudes are comparable to the operating gate voltage of the device. However, stress voltages required for NBTI investigations in VDMOS transistors, whose gate oxides are much thicker than those in CMOS devices, are several times larger than their typical operating voltage, so separate circuits for providing the stress voltage and performing the NBTI measurements are needed. The tests should be realized by switching back and forth between the circuits.

This paper is focused on the application of the recently developed measurement technique, which is based on cost-effective switching circuit and is suitable for NBTI measurements on VDMOS transistors [25]. Devices used in this study were commercial p-channel power VDMOSFETs IRF9520 with current/voltage ratings of 6.8 A/100 V, encapsulated in TO-220 plastic cases [40]. The devices were built in standard Si-gate technology with gate oxide thickness of 100 nm, and had the initial threshold voltage, V_{T0}, about −3.6 V. As already mentioned, owing to the thick gate oxide, accelerated NBT stressing of these devices requires negative gate voltage amplitudes even over 40 V, which exceed capabilities of commonly used signal voltage sources [41, 42]. Therefore, an external amplifier or a booster is required between the source unit providing the stress voltage and the device under test (DUT), as illustrated by a block diagram shown in Fig. 1. Full scheme and detailed explanation of the system developed for NBT stress and measurements on power VDMOSFETs are given in [25], and here we only provide short description. Reed relays S1 and S2 are used as switches to separate the high-voltage stress circuit from the low-voltage measurement circuit. In the stress mode, source and drain of DUT are tied to ground, whereas gate stress voltage is obtained by boosting a signal from Tektronix AFG3102 function generator to a required magnitude. The booster circuit is based on power VDMOS transistor in a simple switching configuration, which enables to perform either dc stress (function generator output is kept at 0 V) or ac stress (function generator output is used to provide pulses). The booster circuit includes the appropriate drain and gate resistors, which are required to maintain acceptable shape of the switching waveform [43] and prevent possible parasitic oscillations. In the measurement mode, two source-measure units from Agilent 4156C precision semiconductor parameter analyzer are used: one solely to provide sweeping gate voltage to the DUT and the

second one to provide constant drain voltage and to measure drain current of DUT. As already mentioned, switching between stress and measurement circuits is accomplished by using reed relays S1 and S2, but one more relay (not shown in Fig. 1) is additionally used to switch the drain voltage sense circuit of 4156C analyzer, so the voltage drop on the external leads is properly compensated.

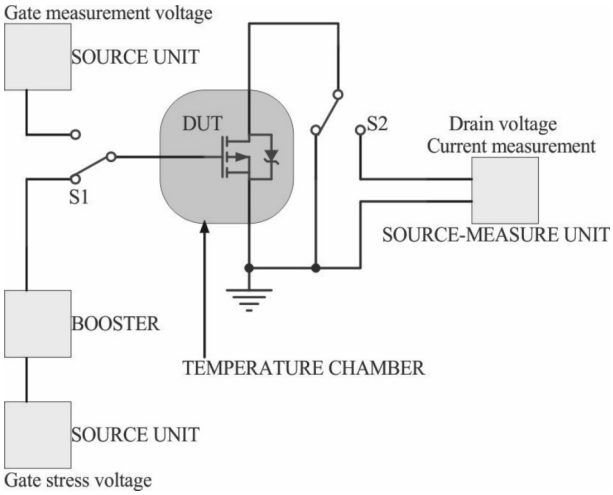

Figure 1: Block diagram of NBT stress and measurement setup for p-channel power VDMOSFETs [25].

All instruments shown in Fig. 1, and the temperature inside the chamber as well, are computer controlled over the IEEE-488 (GPIB) bus. Multithreading PC application software is developed using .NET technology to allow the NBTI test specification and control through the graphical user interface. Timeline for interim measurements is loaded from the external file. Within the graphical interface, which is shown in Fig. 2, user is allowed to specify gate stress voltage amplitude, frequency and duty cycle, stress type (dc, ac, or combined), measurement condition (linear or saturation), drain voltage, and nested timeline for multiple interim measurements after stress. If a combined stress is used, an arbitrary point on the loaded timeline may be chosen for changing the stress type. Measurements at room temperature before and after the test are also performed automatically. Results for each measurement are saved in a separate file during the test and merged upon the test completion. The overall time required to complete an interim measurement, which includes switching from the stress to measurement circuit, measurement of the full *I–V* characteristic while sweeping the gate voltage from −2 to −4.75 V with 50 mV steps, and switching back to the stress circuit, is found to be about 235 ms and cannot be further reduced due to the speed limitations of the reed relays and instrumentation used [25].

3 Results and discussion

The system has been verified by series of NBTI tests on several devices. As an example, Fig. 3 shows measured transfer *I–V* characteristics for one device subjected to

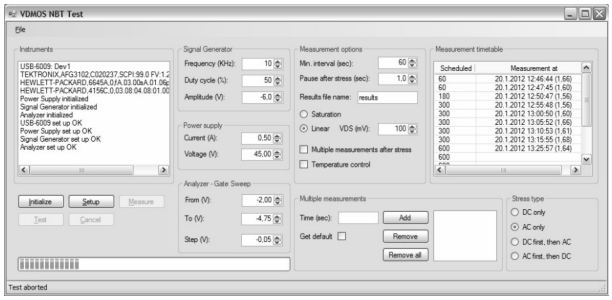

Figure 2: Graphical user interface of the software application for NBT stress and measurement.

12 hours of the pulsed bias stress followed by 24 hours of static stress under the specified conditions. During the 36 h test, the total of 48 interim measurements were performed according to the predefined timeline, but for simplicity, only the initial (before stress) and final (after stress) characteristics at room (27 °C) and stress (175 °C) temperatures are shown. As can be seen, the characteristics are shifted along the gate voltage axis toward the higher voltage values, while their slope slightly decreases, which all points to generation of oxide trapped charge and interface traps induced by NBT stress. The overall NBT stress-induced degradation is considered to include hole trapping in the oxide and creation of interface and oxide traps through the reactions involving hydrogen species and their subsequent diffusion away from the interface (reaction–diffusion component) [44]. The holes trapped near the interface are quickly released once the NBT stress is ceased, and thus make the 'fast' component of degradation, whereas the reaction–diffusion component, whose recovery depends on hydrogen back-diffusion, is the 'slow' component and may even be partially non-recoverable. It should be noted, however, that the time constants associated with hole trapping–detrapping increase about exponentially with distance from the interface [44], and in the case of ultra-thick oxides typical for VDMOS devices may span over many decades in time, which means that hole trapping in this case may contribute to both slow and fast degradation components. Moreover, some recent studies have strongly suggested that the hole trapping could give major contribution to the degradation in thin gate oxides as well [8, 45], and these findings have led to the development of the new charge-trapping models, which link the NBTI degradation with the creation of switching oxide traps and are more consistent with the post-stress recovery data showing dispersion over a wide range of time [45].

Due to the limitations in measurement speed of 4156C [27, 30, 35, 36], the fast component of NBT stress-induced degradation cannot be captured by the proposed setup. However, the setup was optimized to start the measurement immediately (within the instrument's limits) after completing the stress, and it was shown that an approximate evaluation of the dynamic recovery effects in power VDMOS devices still might be possible [25]. Actually, the setup may be of help to alleviate the dynamic recovery effect in NBTI characterization as it seems to offer measurements short enough to capture the faster part of the slow degradation component, which should be sufficient for rather reliable prediction of device lifetime considering the finding that even a 60 s long delay in measurements does not cause significant overestimation of NBTI lifetime [46]. In addition, this method provides the full range *I–V* characteristics that can be used to determine not only threshold voltage but also to extract and/or calculate some other important device parameters, such as transconductance and channel carrier mobility, which may provide better insight into the effects of NBTI.

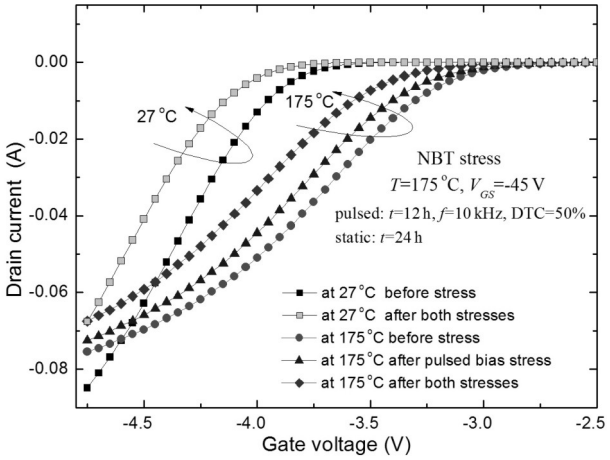

Figure 3: Measured transfer *I–V* characteristics before and after the NBTI test.

Herewith we will present and discuss in more details the results of the experiment in which the two sets of p-channel power VDMOS devices were stressed for 36 hours under the static and pulsed NBT stress conditions, respectively. For the static NBT stress, negative dc voltages in the range 35 – 45 V were applied to the gate, whereas the drain and source terminals were grounded. For the pulsed stress, negative gate voltage pulses (with frequency f = 10 kHz and duty cycle DTC = 50%) of the same magnitudes were used instead. Stressing under both static and pulsed conditions was performed at temperatures ranging from 125 to 175 °C. Threshold voltage values were calculated from the measured *I–V* characteristics by the second derivative method [47].

Two characteristic sets of data (for different stress voltages at 175 °C and for different temperatures at the stress voltage of –45 V) for the stress-induced threshold voltage shifts during the static and pulsed NBT stressing of IRF9520 p-channel VDMOSFETs are shown in Fig. 4. As can be seen, NBT stressing under both static and pulsed bias conditions was found to cause signifi-

cant threshold voltage shifts, which were more pronounced at higher voltages and/or temperatures. The threshold voltage shifts caused by pulsed NBT stress appeared with rather significant delay (30-60 minutes after the start of stressing), which was found to depend on stress temperature and pulse magnitude. In addition, the pulsed voltage stressing caused generally lower shifts as compared to static stressing performed at the same temperature with equal stress voltage magnitude.

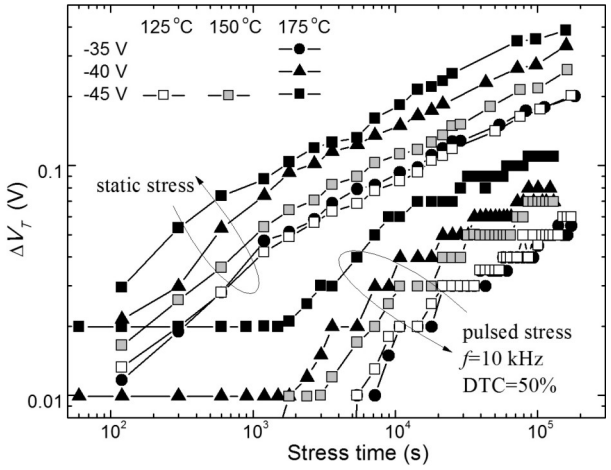

Figure 4: Threshold voltage shifts in p-channel VD-MOSFETs during the static and pulsed (f = 10 kHz, DTC = 50%) NBT stressing.

The reason for the observed delay and lower shifts in the case of the pulsed NBT stress can be explained by two factors associated with the nature of pulsed stressing itself. The first factor is assessed by taking into account that "stress time" in Fig. 4 refers to the total time, which includes fractions of the periods corresponding to both "high" and "low" levels of the pulsed gate voltage applied. However, the devices are stressed only during the fraction of period corresponding to the "high" voltage level (on-time), so the actual or net stress time is significantly shorter (and the resulting stress-induced threshold voltage shifts appear both slower and lower) in the cases of pulsed stress than in the case of static one. The other factor could be a partial recovery of threshold voltage during the period fractions corresponding to the "low" level of the pulsed stress voltage (off-time), which also contributes to the smaller shifts observed in the cases of pulsed bias stress. The partially recovered degradation is restored again on arrival of each new stress voltage pulse, so the phenomenon is referred to as dynamic recovery [48].

To evaluate dynamic recovery effects during the pulsed bias stressing it is necessary to alleviate the first factor mentioned above, which could be done by plotting the threshold voltage shift versus the net stress time rather than the total time. The results of stressing with three different duty cycle pulses (75%, 50%, and 25%) at 10 kHz and those of static stress are shown in Fig. 5, where the net stress time in the cases of pulsed stressing was calculated by multiplying the total stress time with corresponding duty cycle value for each specific case. The overall net stress time was 6 h in all cases, and all devices were stressed with the same gate voltage magnitude (–45 V) at 175 °C. As can be seen, the NBT stress-induced threshold voltage shifts are most significant in the case of the static stress and clearly decrease with lowering the duty cycle in the cases of the pulsed bias stress. This is clear indication that dynamic recovery effects become more pronounced with lowering the duty cycle of the gate voltage applied. However, it should be noted that frequency remains constant, so variations in duty cycle change the ratio between the pulse and no-pulse fractions of the period: the lower duty cycle actually means shorter pulses and longer breaks in between the pulses, which further means shorter stress time and longer recovery time during each period of pulsed stress voltage applied. Accordingly, there is less time to create degradation during a single period and more time for recovery, so the overall resulting degradation found after stressing for equal net stress times tends to decrease with lowering the duty cycle. Therefore, it can be speculated that overall degradation tends to decrease with duty cycle lowering because of two combined effects: one is creation of lesser degradation because the pulses are getting shorter, and the other is enhanced dynamic recovery because the period fractions between the two pulses are getting longer.

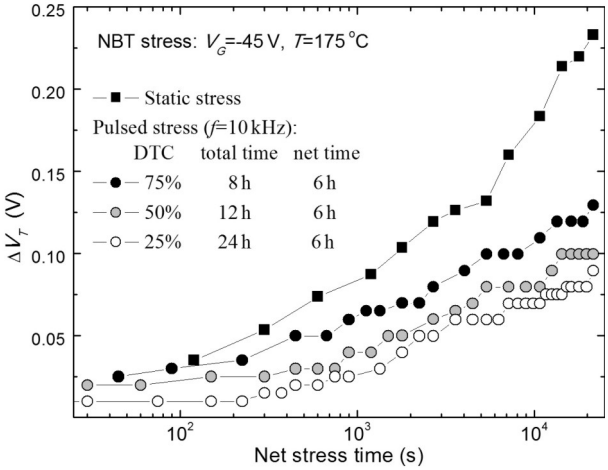

Figure 5: Threshold voltage shifts in p-channel VD-MOSFETs vs. net stress time at various duty cycles (NBT stress: V_G = –45 V, T = 175 °C, f = 10 kHz).

Threshold voltage shifts observed in devices stressed with three different frequency pulses (1, 10 and 100 kHz) in comparison with those obtained by static

stress are shown in Fig. 6. All devices were stressed with the same gate voltage magnitude (–45 V) at 175 °C, and the overall net stress time was 6 h in all cases again. A duty cycle was kept at 50% for the pulsed stressing at all frequencies, so the net stress time in these cases was equal to a half of the total stress time. Again, the stress-induced threshold voltage shifts are most significant in the case of the static stress, and it is interesting to note that they clearly decrease with increasing the frequency in the cases of the pulsed bias stress. So, the dynamic recovery effects seem to become more pronounced with increasing the frequency of the gate voltage applied even though the change of frequency at constant duty cycle practically does not affect the ratio between the pulse and no-pulse fractions of the period at all. However, the increase in frequency means that the pulses and fraction of period between the pulses become both shorter, which further means that there is less time to create degradation and less time for recovery during each period of the pulsed voltage applied. Accordingly, one may expect the resulting degradation would be nearly independent of frequency, as reported in [49, 50], but in our case degradation apparently decreases with increasing the frequency, as reported more recently in [32] (advanced measurement techniques mentioned in previous section have become available rather recently, which might be a reason for inconsistency of the data reported here and in [32] with those found in less recent publications [49, 50]).

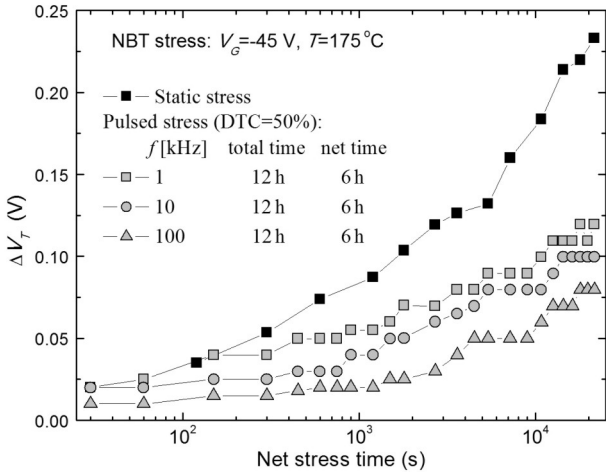

Figure 6: Threshold voltage shifts in p-channel VD-MOSFETs vs. net stress time at various frequencies (NBT stress: V_G=–45 V, T=175°C, DTC=50%).

A possible explanation for why the degradation decreases with increasing the frequency could be as follows. The pulses at low frequencies are long enough to allow for creation of rather significant amount of the slow and/or non-recoverable component of degradation, which is hardly removed in the fraction of period between the pulses. The amount of this component decreases at higher frequencies, while that of the fast component increases, and the latter is more easily removed even though the fraction of period between the pulses becomes shorter. As a result, the dynamic recovery effects become more pronounced and overall degradation tends to decrease with increasing the frequency.

4 Conclusions

A cost-effective stress and measurement setup was used to investigate dynamic recovery effects during the NBTI tests in commercial p-channel VDMOS transistors IRF9520. The effects of NBT stress voltage and temperature under both static and pulsed stress bias conditions were discussed, and dynamic recovery effects were evaluated by varying the duty cycle and frequency of the pulsed stress voltage applied. The stress induced threshold voltage shifts under both static and pulsed bias conditions were found to be larger at higher temperatures and/or stress voltage magnitudes. Less significant degradation of threshold voltage was observed under the pulsed stress bias conditions because of the dynamic recovery. The tendency of overall degradation to decrease with lowering the duty cycle and/or increasing the frequency of the pulsed voltage used for stressing was explained in terms of enhanced dynamic recovery effects.

Acknowledgments

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