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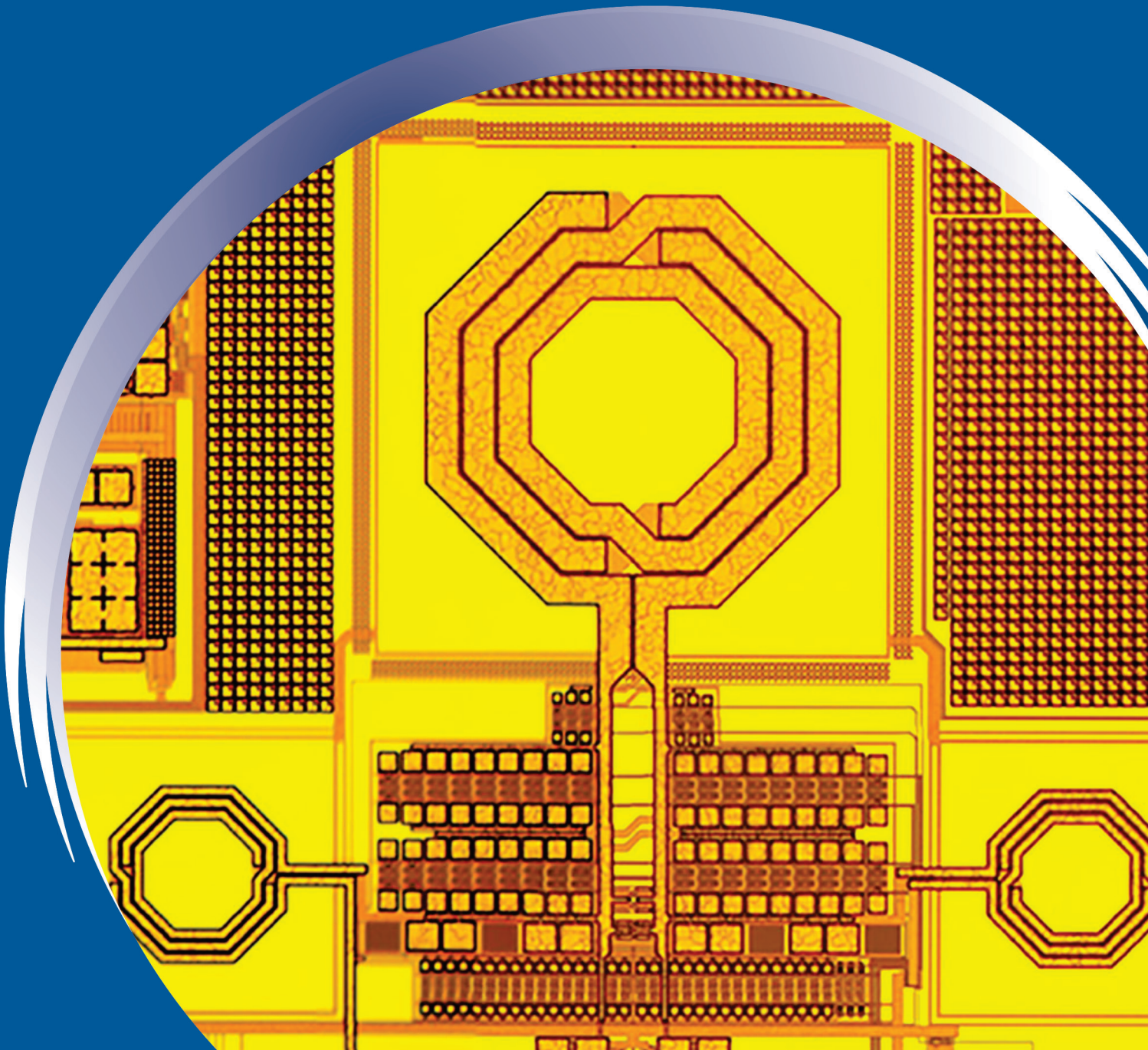

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Content | Vsebina

Editorial | Uvodnik

Dear reader,

This issue brings a review scientific paper in an exciting field of microelectronics that already proves but much more promises to contribute to further progress. It covers fascinating progress of spintronics that was presented as a planary talk at the MIDEM conference that we organize in late September every year. The 53rd MIDEM Conference under the Chairmanship of Asst. Prof. Slavko Bernik and Prof. Barbara Malič was a big success with the highlight on Materials for Energy Conversion and their Applications: Electrocalorics and Thermoelectrics as the Workshop.

Year 2017 almost ran out and this editorial brings up some statistics about manuscripts submitted. In 2017 we have received more than 180 manuscripts, out of which only 23 have been accepted for publication and more than 140 manuscript were rejected. Despite clearly defined title of our journal and on-line instructions for authors we continue to receive each year a dozen of manuscripts that are out of our journal's scope. In 2017 we published 1 review scientific paper and 25 original scientific papers. The success rate below 15% in 2017 reflects determination for quality that will path long-term quality growth. Increase in citation metrics (JCR IF-2016=0.478, SNIP-2016=0.482 and CiteScore-2016=0,60) is certainly a proof for that. I sincerely thank all reviewers and Editorial Board Members for their valuable contribution to the journal quality growth. Three associate editors, Prof. Vanja Ambrožič, Asst. Prof. Danjela Kuščer Hrovatin and Prof. Matjaž Vidmar received the Society MIDEM Editor Award for their valuable editorial contribution over the last 5 years.

Let the festive days bring joy and peace in each home, office or research laboratory. It is the time to look ahead and make plans for the coming year. This brings me to editorial wishes for 2018. As a part of your success we look forward to receiving your future manuscript(s) on our submission page (http://ojs.midem-drustvo.si/).

Merry Christmas and a Happy, Healthy and Prosperous New Year!

Prof. Marko Topič
Editor-in-Chief

P.S
We look forward to receiving your next manuscript(s) in our on-line submission platform:
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Review scientific paper

Informacije MIDEM
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Spintronics as a Non-Volatile Complement to Modern Microelectronics

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Abstract: Continuous miniaturization of semiconductor devices has been the main driver behind the outstanding increase of speed and performance of integrated circuits. In addition to a harmful active power penalty, small device dimensions result in rapidly rising leakages and fast growing stand-by power. The critical high power consumption becomes incompatible with the global demands to sustain and accelerate the vital industrial growth, and an introduction of new solutions for energy efficient computations becomes paramount.

A highly attractive option to reduce power consumption is to introduce non-volatility in integrated circuits. Preserving the data without power eliminates the need for refreshment cycles and related leakages as well as the necessity to initialize the data in temporarily unused parts of the circuit. Spin transistors are promising devices, with the charge-based functionality complemented by the electron spin. The non-volatility is introduced by making the source and drain ferromagnetic. Recent advances in resolving several fundamental problems including spin injection from a metal ferromagnet to a semiconductor, spin propagation and relaxation, as well as spin manipulation by the electric field, resulted in successful demonstrations of such devices. However, the small relative current ratio between parallel/anti-parallel source and drain alignment at room temperature remains a substantial challenge preventing these devices from entering the market in the near future.

In contrast, a magnetic tunnel junction is an excellent candidate for realizing power-reducing approaches, as it possesses a simple structure, long retention time, high endurance, fast operation speed, and yields high integration density. Magnetic tunnel junctions with large magnetoresistance ratio are perfectly suited as key elements of non-volatile magnetoresistive memory compatible with the complementary metal-oxide-semiconductor technology and capable to replace dynamic and potentially static random access memories. We review the present status of the technology, remaining challenges, as well as approaches to resolve the remaining problems. Regarding active power reduction, delegating data processing capabilities into the non-volatile segment and combining non-volatile elements with CMOS allows for efficient power gating. It also paves the way for a new low-power and high-performance in-memory processing paradigm-based on an intrinsic logic-in-memory architecture, where the same non-volatile elements are used to store and to process the information.

Spintronics kot trajno dopolnilo moderne mikroelektronike

Keywords: Spintronics; non-volatility; spin field-effect transistors; spin relaxation; magnetic tunnel junctions; magnetic random access memory (MRAM), spin-transfer torque MRAM, spin-orbit torque MRAM; voltage-controlled MRAM; logic-in-memory

Sestavljivi 2D Vernier TDC na osnovi obročnih oscilatorjev

Izvleček: Nenehno zmanjševanje polprevodniških naprav je bila glavna gonilna sila izjemnega povečanja hitrosti in zmogljivosti integriranih vezij. Poleg škodljivega povečevanja aktivne moči majhne dimenzije naprav vplivajo tudi na višje uhajalne tokove in večjo porabo v stanju mirovanja. Visoka poraba energije je postala nekompatibilna z zahtevami vzdržnosti rastoče industrije, zato so potrebne nove rešitve učinkovite rabe energije.

Zelo privlačna možnost zmanjšanja porabe energije je uvedba trajnosti v integriranih vezjih. Ohranjanje podatkov brez porabe energije odpravlja potrebo po osveževalnih ciklih in uhajanjih ter nujnosti inicializiranja podatkov v začasno neuporabljenih delih vezja. Spin tranzistorji so obetavni elementi, ki temeljijo na osnovi naboja z dopolnitvijo vrtilne količine elektrona (spin). Trajnost se ustvari tako, da sta vir in ponor feromagnetna. Nedavni napredek pri reševanju številnih temeljnih problemov, vključno s injektiranjem vrtilne količine iz kovinskega feromagnetika v polprevodnik, vzpostavitev in relaksacija vrtilne količine ter upravljanje vrtilne količine z električnim poljem,

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je bil ključen za uspešno demonstracijo takšnih naprav. Kljub temu ostaja relativno majhno razmerje tokov med vzporednim/nasprotnim položajem izvora in ponora pri sobni temperaturi ključen izziv, ki preprečuje vstop teh naprav na trg v bližnji prihodnosti.

V nasprotju s tem je magnetni tunelski spoj odličen kandidat za uresničevanje pristopov zmanjšanja moči, saj ima preprosto strukturo, dolg čas zadrževanja, visoko vzdržljivost, hitro obratovalno hitrost in visoko gostoto integracije. Magnetni tunelski spoji z visokim razmerjem magnetoresonance so idealni za uporabo v trajnih megnetorezistivnih spominih, ki so združljivi s komplementarno kovina-oksid-polprevodnik tehnologijo in sposobni zamenjati dinamičen in statičen spomin z naključnim dostopom. V članku je podan pregled tehnologije, izzivi in postopki, kako rešiti obstoječe probleme.

Zmanjševanje porabe energije se lahko doseže s prenosom obdelave podatkov v trajne segmente in kombinacijo trajnih elementov s CMOS. Prav tako se utira pot novi paradigmi procesiranja v pomnilniku z nizko porabo energije in visoko zmogljivostjo, ki temelji na arhitekturi logike v pomnilniku, kjer se za shranjevanje in obdelavo podatkov uporabljajo isti trajni elementi.

Ključne besede: Spintronika; trajnost; tranzistorji z vrtilnim poljem; relaksacija vrtilne količine; magnetni tunelski spoj; magnetni spomin z naključnim dostopom (MRAM); navor prenosa vrtilnosti MRAM; navor orbite vrtilnosti MRAM; napetostno krmiljen MRAM; spominska logika

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1 Introduction

The breathtaking increase in performance and speed of integrated circuits has been enabled by continuous miniaturization of complementary metal-oxide semiconductor (CMOS) devices. On this exciting path numerous outstanding technological challenges have been resolved. Among the most crucial technological changes recently adopted by the semiconductor industry to boost CMOS performance while maintaining gate control over the semiconductor channel are the introduction of strain [1], high-k gate dielectrics and metal gates [2], and a three-dimensional (3D) tri-gate transistor architecture [3-5]. The successes and innovative solutions developed for the microelectronics technology have been always supported by sophisticated simulation tools, which allow reducing the research and development costs by 35-40% [6].

Although transistor sizes are scaled down, the on-currents cannot be further decreased due to the need to charge/discharge the load capacitances and to maintain the clock, which is saturated at approximately 4.0 GHz. Increasing the clock frequency results in an active power penalty, while continuous transistor scaling results in growing leakages and stand-by power. Novel revolutionary approaches are desperately needed in the long run to sustain the vital societal and industrial progress in computing performance whilst simultaneously reducing power consumption.

The ultimate solution to one of the primary issues – the power reduction – is to introduce non-volatility into the circuits. Non-volatility is the ability to preserve data, when the supply power is turned off. It enables stand-by power-free integrated circuits as no information is lost and there is no need to recover the data, when the power is turned on. Non-volatility is crucial for eliminating the leakage power dissipation and data refreshment cycles. Apart from stand-alone applications, e.g., critical program and data storage devices in extreme environments employed in the air and space industry, it is particularly promising to use non-volatility in the main computer memory as a replacement of conventional volatile CMOS-based dynamic random-access memory (DRAM) [7], which will drastically reduce energy consumption. In modern multicore processors, much of the energy consumption appears in the hierarchical multi-level cache memory structure. To reduce this energy consumption, a viable approach is to replace the caches with a non-volatile memory technology which also offers a reduced memory cell size compared to static random-access memory (SRAM) [7]. This will help bridging the speed gap between the last-level cashes and main memory, since CMOS SRAM is much faster compared to CMOS DRAM.

To be competitive with the traditional volatile memory technologies and also with non-volatile flash memory, emerging non-volatile memories must offer a fast switching time, a high integration density supported with good scalability, a long retention time, a high endurance, and a low power consumption. At the same time, they must possess a simple structure to reduce fabrication costs and the new non-volatile circuit elements must be compatible with CMOS technology to benefit from advantages provided by the well-developed CMOS fabrication technology.

A spin field-effect transistor (SpinFET) is a promising future semiconductor device with a performance poten-

tially superior to that achieved in the present transistor technology. The non-volatility in SpinFETs is added by replacing the non-magnetic source and drain in a FET by its ferromagnetic counterparts. The two ferromagnetic contacts (source and drain) are linked by a non-magnetic semiconductor channel region. Metallic ferromagnetic contacts serve not only as an injector/detector of the spin-polarized electron charge current in the channel, but, because of their magnetization, the source and drain electrodes provide an additional current modulation due to their capabilities to inject/detect spins [8]. Indeed, the electron current gets enhanced in the case of parallel alignment between the source/drain electrodes as electrons are injected with spins parallel to the drain magnetization and can easily escape from the channel to the drain, while the current is suppressed for anti-parallel magnetization alignment [8]. As the magnetization of the source/drain can be manipulated by means of an external magnetic field and/or current (by means of the spin-transfer torque), the two on-current states for parallel/anti-parallel magnetization alignment potentially enable reprogrammable logic [9]. Importantly, the relative magnetization orientation between source and drain is preserved without external power, which makes reprogrammable logic partly non-volatile. Below we discuss recent advances and remaining challenges to realize SpinFET-based logic in detail. We only stress the most important, in our opinion, shortcoming to overcome, namely, a small relative difference between the on-currents in parallel and anti-parallel source/drain alignment.

Magnetoresistive random access memory (MRAM) and in particular spin transfer torque (STT) MRAM possesses many, if not all, of these advantages and is considered as a perfect candidate for future universal memory applications. MRAM is CMOS-integrable, which increases its potential to replace the typical processor-embedded SRAM and DRAM.

With STT MRAM currently emerging as a commercial product for stand-alone applications, it will be critically important to introduce STT MRAM in the main computer memory, i.e., to replace conventional DRAM and SRAM. This will create a new innovative multi-billion dollar industry and will sustain the breathtaking path of electronics by delivering cheaper, faster, and environmentally friendlier compact and mobile devices. Bringing STT MRAM into the vast computer memory market as embedded and stand-alone applications for traditional high-performance and low-power mobile platforms will result in an exponential growth of the non-volatile memory market share in the near future.

Regardless of the first commercial STT MRAM-based products for stand-alone applications being available, one critical aspect of the currently used STT MRAM technology is a relatively high switching current, which again is in sharp contrast to the overall demand for reduced energy consumption. This obviously prevents the MRAM from successfully entering the vast computer memory market. The problem of high switching current and large active writing energy jeopardizes the advantages provided by non-volatility, such as zero stand-by power, no data refreshment, and no data recovery. Several plausible approaches to address these issues are conceivable including the replacement of the in-plane magnetization orientation in magnetic tunnel junctions (MTJs) with perpendicular magnetization, the use of composite free recording layers, decoupling the write and read current paths, controlling magnetization by voltage, and employing new materials with improved properties and characteristics.

2 Spin transistor

In a SpinFET [8] schematically shown in Fig.1 the electrons with spin aligned to the drain magnetization direction can easily leave the channel to the drain thus contributing to the current. The total current through the device depends on the relative angle between the magnetization direction of the drain and the electron spin polarization at the end of the semiconductor channel. The electron spin orientation at the end of the channel is determined by the source magnetization and can be additionally manipulated by the modulation which is achieved by tuning the strength of the effective spin-orbit interaction in the channel induced by the gate voltage. As a non-equilibrium quantity, the injected spin relaxes to its equilibrium zero value while propagating through the channel. Spin relaxation is an important detrimental ingredient as it reduces the current modulation and affects the SpinFET functionality.

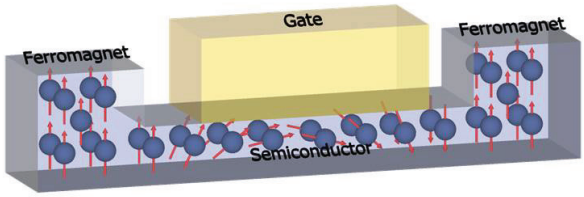

Figure 1: Datta-Das SpinFET [8]. Spin-polarized electrons are injected from a ferromagnetic source and absorbed by in a ferromagnetic drain. The electron spins in the channel are manipulated by means of the gate voltage-dependent spin-orbit interaction.

2.1 Spin-Orbit Interaction

The spin relaxation is governed by the spin-orbit interaction (SOI) and scattering, both spin-dependent and

spin-independent, and manifests itself differently in semiconductors with and without the inversion symmetry [10,11].

In crystals obeying the inversion symmetry (silicon, germanium) the spin relaxation is governed be the Elliott-Yafet mechanism [10,11]. The wave function with a fixed spin projection (defining the quantization axis) is not an eigenstate of the Hamiltonian due to the electron momentum-dependent SOI. In other words, the SOI forces the eigenstate wave function to possess a small but finite contribution with an opposite spin projection in the fixed basis. Therefore, the small but finite amplitude to flip the electron spin appears at every spin-independent scattering event – the Elliott process [12]. This is complemented by the Yafet spin-flip events due to SOI-dependent electron-phonon scattering. In silicon the electron spin relaxation is determined by the inter-valley transitions [12] and can be efficiently controlled by stress [13]. In silicon channels, uniaxial stress generating shear strain is particularly efficient to suppress the spin relaxation [14] as it lifts the degeneracy between the two unprimed subband ladders [15]. In addition, choosing the spin injection direction also boosts the spin lifetime by a factor of two [16], as shown in Fig.2.

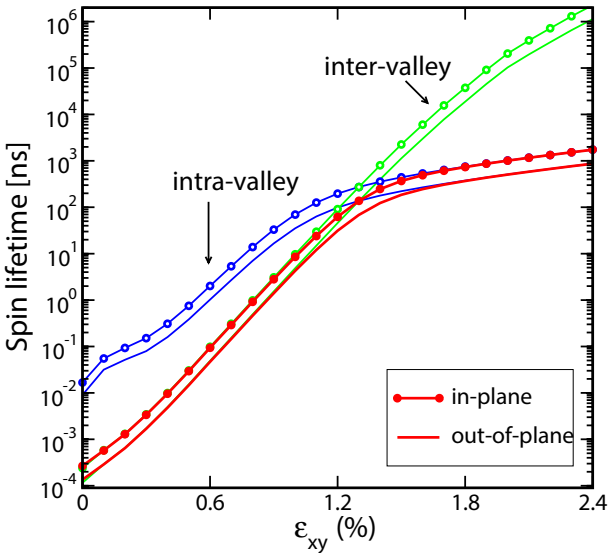

Figure 2: Spin lifetime in (001) thin Si film as a function of shear strain. The spin lifetime is a factor of two longer for spins injected in-plane as compared to the time for spins injected perpendicular to the film. The factor of two is preserved for both inter- and intra-valley scattering and is independent of the scattering mechanism (electron-phonon and surface roughness scattering).

In III-V materials without inversion symmetry the degeneracy between the up and down spin states with the same electron momentum is lifted, and the spin relaxation is governed by the Dyakonov-Perel mechanism [10,11]. However, the SOI does not always play a detrimental role. In semiconductor channels the SOI may also be used efficiently to manipulate the electron spins in the channel [8]. The inversion symmetry in the channel can additionally be violated by applying the gate voltage. In this case the strength of the effective SOI depends on the effective electric field perpendicular to the channel [17]. The strength of the gate voltage-dependent SOI can be used to modulate the current between the ferromagnetic source and drain by means of an additional spin modulation in the channel resulting in a different spin orientation relative to the drain as compared to the case without SOI [8]. Importantly, as the strength of the SOI in the channel depends on the effective electric field, the suggested method provides a purely electrical mean of manipulating the electron spins and thus the current in the channel.

The voltage-induced SOI in III-V materials can be used for an efficient spin injection in the channel from the point contacts [18]. Additional gates are used to create the point contacts to the two-dimensional (2D) electron gas by confining the 2D gas in the III-V channel under the gates. Application of different voltages to these gates generates the spin-orbit Rashba field perpendicular to the point contact. By properly tuning the chemical potential one can achieve that, due to this SOI, all electrons moving to the right are spin-polarized (while electrons moving to the left are polarized in the opposite direction). Thereby an efficient and purely electrical spin injection/detection is achieved. Using this injection scheme, the ever first reliable demonstration [18] of a working SpinFET [8] suggested in 1990 was achieved.

Not long ago, new 2D materials (graphene, transition metal dichalcogenides), become attractive for future microelectronics applications. Recently, a new concept for realizing a spin switch with a graphene channel was demonstrated [19]. Spin-polarized electrons are injected into the graphene, a good spin conductor due to low SOI, and reach the drain electrode, if the electrochemical potential in MoS_2 is tuned into the energy gap. In this case the electrons do not enter MoS_2. The situation is completely changed, if the electrochemical potential is tuned by the gate into the MoS_2 conduction band. In this case a parallel path for electrons through a material with high SOI is open, which results in strong spin relaxation, so that the current reaching the drain is not spin-polarized.

Regardless of the successful demonstration of the SpinFET, the conductance modulations were only resolved at temperatures far below 300K. The spin switch [19] discussed above was demonstrated to work at

temperatures below 200K and requires additional cooling, which modern microelectronics working at room temperature is striving to avoid. Recently, the first successful demonstration of a silicon spin metal-oxide-semiconductor field-effect transistor (SpinMOSFET) at room temperature [20] was presented. In silicon the strength of the Rashba SOI is much smaller compared to that in III-V semiconductors. Therefore, the SOI cannot be used for spin manipulation. Thus, the current modulation in the SpinMOSFET is achieved by altering the relative magnetization between the ferromagnetic source and drain. This way, a high difference between the on-currents in parallel and anti-parallel source/drain configuration was demonstrated. However, the relative ratio of the currents, a characteristic similar to the tunnel magnetoresistance (TMR) ratio, is still several orders of magnitude lower [20] than the TMR in MTJs. Fig.3 shows the TMR in a silicon SpinFET as a function of the SOI strength, for several channel lengths for an ideal case when the spin relaxation is neglected. In order to facilitate the spin injection and detection, delta function-like Schottky barriers between the source, drain, and the channel of the strength $U = \frac{h}{2\pi}\sqrt{\frac{E_F}{2m_F}}$ were h is the Plank constant, E_F and m_F are the Fermi energy and the electron mass in the ferromagnetic contacts, are assumed. Even in this ideal case the TMR is about 10%, much inferior to that in MTJs. A TMR less than 1% was experimentally observed at room temperature [20].

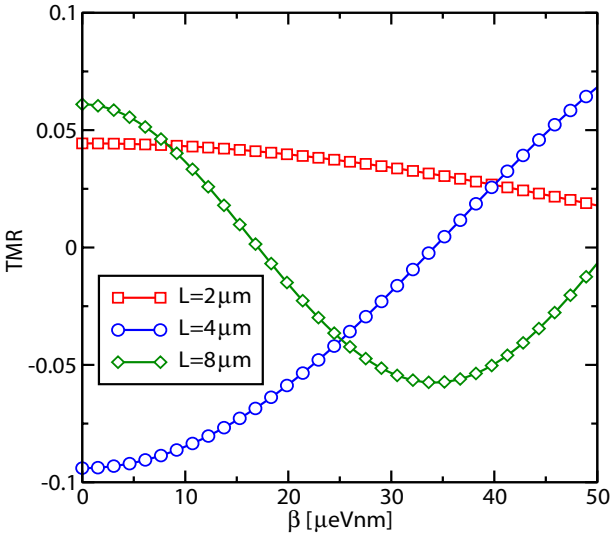

Figure 3: The ratio of the resistance difference in antiparallel and parallel configurations to the resistance in parallel configuration of the source and drain in Si-based SpinFETs as a function of the spin-orbit interaction strength, for several channel lengths.

2.2 Spin Injection and Spin-Dependent Tunneling

The device described above can function only if the electron spins are efficiently injected/extracted in/from the channel. As there are no semiconductor ferromagnets at room temperature, to achieve the efficient injection/detection from metal ferromagnets in the semiconductor channel and vice versa, a thin tunneling barrier must be placed between the electrodes and the channels [21] to mitigate the spin impedance mismatch. However, the signal attributed to the spin injection [22] appears to be much weaker as compared to the large effect [23] currently attributed to the spin-dependent resonant tunneling [24-26], and the development of efficient ways to electrically inject spins from a ferromagnetic metal in a semiconductor has become an area of active research.

To summarize, although many fundamental challenges have been resolved and both a SpinFET and a SpinMOSFET have been successfully demonstrated, an enhancement of the on-current ratio between the parallel and anti-parallel source/drain magnetization alignment at room temperature remains one of the main challenges. In addition, both SpinFET and SpinMOSFET still rely on the charge current to transfer the spin, which may set some limitations for the applicability of such devices in main-stream microelectronics in the future. Non-volatile devices based on MTJs possess the TMR suitable for practical applications and are reviewed below.

3 Magnetoresistive random access memory

Applications driven by magnetic moments and induced magnetic fields have a large share in typical information technology products. Coupling between magnetic fields and currents in coils was employed in the first electronic devices. However, the coupling is relatively weak, resulting in low efficiency and high energy supply costs. An efficient coupling between the electrical and the magnetic degree of freedom is possible on a quantum mechanical level and was discovered in 1986 as a phenomenon called the giant magnetoresistance (GMR) effect. This facilitated a reliable, purely electrical read operation of the information encoded in the magnetization orientation. Based on this principle hard drive storage devices with extremely high density appeared on the market. The enormous impact of this discovery on the development of information technology was recognized by awarding the inventors the Nobel Prize in 2007 [27,28].

The next generation of storage devices with higher density is based on the unique properties of the MTJ. It was discovered that, if the non-magnetic metal layer in a GMR memory element is substituted by a thin dielectric, the tunneling current through the structure strongly depends on the relative polarization of the ferromagnetic contacts (Fig.4). The difference in the MTJ resistivity can reach several hundred percent at room temperature [29]. Thanks to this technology a new generation of hard drives with even higher storage densities has been developed.

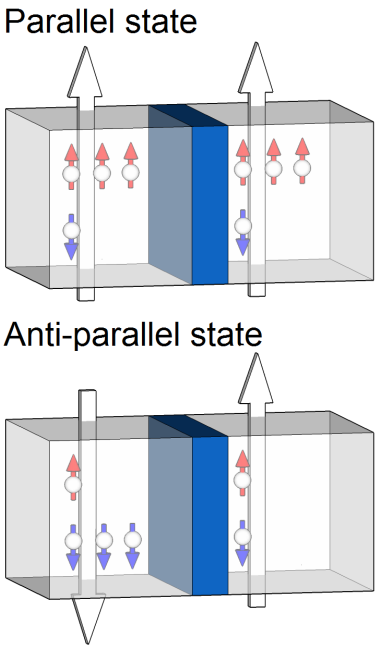

Figure 4: A magnetic tunnel junction possesses low (high) resistance for parallel (antiparallel) relative orientation between the ferromagnetic electrodes.

In order to be used in memories, MTJs must be complemented with the ability to efficiently convert charge information into magnetic moment orientation. Writing the state by the magnetic field is currently used in toggle switching commercial MRAM. This method, however, is not scalable as the magnetic field is generated by the current, which leads to a current increase with scaling [30].

3.1 Spin Transfer Torque Magnitoresistive Random Access Memory

The STT effect [31,32] has been proven to be a perfect alternative to the magnetic field for magnetization switching. The STT is used for purely electrical data writing by passing the current through the MTJ. The memory technology based on MTJs and the STT effect has resulted in the development of STT MRAM. STT MRAM is characterized by lower power-consumption and better scalability than conventional MRAM, where the switching is performed by the magnetic field [33] generated by an electric current passing through the write lines next to the cell. Several cells are arranged in a matrix connected with bit and world lines. A cell in this cross-point architecture is written by simultaneously selecting the cell with current pulses applied to the corresponding world and bit lines. The problem of half-selected cells [30] is solved by the application of a certain pulse sequence to the lines supplemented with a special design of the free layer arranged as a synthetic anti-ferromagnet [34]. This results in a deterministic, toggle-like fast switching of the free layer.

The magnetic field employed for switching prevents MRAM from scaling down beyond 90nm [35] as the current needed for the field generation rapidly increases with scaling. STT [31,32] opened a new way of manipulating magnetization dynamics by using spin-polarized currents instead of magnetic fields. The spin-polarized current allows writing the information into the memory cell by purely electrical means. When electrons pass through a fixed ferromagnetic layer, their spins become aligned with the magnetization. When these spin-polarized electrons enter the free layer, they become aligned with the magnetization of the free layer within a transition layer of a few angstroms. The electron spins change results in a torque exerted on the magnetization of the free layer. This torque causes magnetization switching, if it is large enough to overcome the damping. By altering the current polarity the magnetization of the free layer can be switched from the anti-parallel to the parallel state and back with respect to the reference layer.

The interest in STT MRAM has increased significantly after the observation of spin torque induced switching in AlO_x-based [36] and MgO-based [37] STT MRAM cells. Depending on the orientation of the layer magnetizations the magnetic pillars can be divided into two categories: (1) perpendicular with out-of-plane magnetization direction and (2) in-plane with the magnetization lying in the plane of the magnetic layer. The introduction of STT MRAM with in-plane magnetization orientation to the market has already begun with the first demonstration by Everspin Technologies [38] of a 64Mb chip. The size of the MTJ bits is 80–90nm with an aspect ratio of 2 and 3. An MgO barrier was used and MTJs with a TMR ratio above 110% were exploited. The chip is able to operate within a broad temperature range.

Switching the magnetization can occur spontaneously due to thermal fluctuations. This is an undesired event, which leads to the loss of the stored information. An important parameter of MRAM is the thermal stability

factor which is defined as the ratio of the thermal stability barrier to the operating temperature. For gigabit applications the thermal stability barrier should be at least 80kT to guarantee the required retention time of 10 years. Achieving large thermal stability and a low switching current for fast switching simultaneously represents one of the main challenges to engineer a good MRAM cell. Perpendicular MTJs (p-MTJs) with the thermal barrier equal to the switching barrier are preferred for applications, because they allow to reduce the switching current. In addition, p-MTJs are better suited for high-density memory [39].

Both field-induced and STT switching can be complemented with heat assisted switching [30]. This technology was routinely used in hard drives in order to facilitate writing. Presently methods using thermally assisted switching in MRAM have already been developed. In addition to assisting switching, heat can facilitate new unique functionalities, for instance, using an MRAM cell with a soft reference layer as a magnetic logic unit [40]. This extends the MRAM research and development area towards logic-in-memory architectures and non-volatile computing.

Regardless of the undisputable success of the first MRAM products on the market, several important challenges remain. The general requirements for any memory type including MRAM are:

- ability to write the data with low energy without damaging the device;
- data retention within a given long time interval;
- ability to read the recorded data without destroying the data.

Improving one or two aspects of its functionality usually leads to a degradation of the remaining functionality [30]. Therefore, a careful parameter optimization specific to a particular technology is the main subject which must be addressed in order to facilitate production of high density memory arrays suitable for replacing SRAM caches and DRAM-embedded main computer memory.

One of the main problems of STT MRAM is a relatively high critical current required for STT-induced magnetization switching. This fact has several implications. Firstly, due to the relatively high energy required for writing, the current generation of STT MRAM cannot be used in high-level processor caches due to the high activity factor in these elements and the high level of generated heat. The necessity to switch memory frequently negates the benefits of non-volatility provided by MRAM. Secondly, large switching currents are supplied via an access transistor. This potentially puts scaling limitations on the transistor dimensions of a one-transistor (1T)-1MTJ memory cell. However, a careful and innovative design yielded already a successful implementation of 8Mb 1T-1MTJ STT MRAM embedded in a 28nm CMOS logic platform [41]. Finally, a large switching current density can result in serious reliability issues like MTJ's resistance drift and eventually its dielectric breakdown. The critical current density depends on the switching pulse duration, with a substantial current increase for faster, sub 10ns switching. A plausible way to reduce the switching current density is to work with p-MTJs.

The problem of data retention is related to thermally agitated magnetization fluctuations. During these fluctuations the magnetization can switch spontaneously via a potential barrier separating the two states with opposite magnetization directions. As already noted, for about 10 years data retention the thermal stability barrier must be at least 80kT for gigabit MRAM arrays. However, increasing the barrier also results in an increase of the switching current density, which is proportional to the thermal barrier for p-MTJs. In order to reduce the switching current density and preserve the large thermal barrier at the same time one has to reduce the Gilbert damping and increase the spin current polarization. An interface-induced p-MTJ structure with a composite free layer CoFeB/Ta/CoFeB with two MgO interfaces [42] allows simultaneously boosting the thermal barriers and reducing damping.

For in-plane MTJs, the faster switching can also be achieved, when the composite free layer is made of two half-ellipses separated by a narrow gap. The peculiarities of the magnetization dynamics of the two parts of the composite free layer [43,44], which occur in opposite senses to each other, lead to the magnetization switching in-plane. This way the large demagnetization penalty of the magnetization getting out of plane is avoided, and the switching barrier becomes equal to the thermal barrier. Because the thermal barrier depends on the free layer volume, the required large thermal stability factors of ~80kT are easily achieved in this structure.

A large TMR ratio is needed for reliably reading the information in MRAM. Indeed, the middle reference resistance to which the low and high resistance MTJ states are compared must be well separated from either of them. However, since a bit-to-bit resistance variation within a memory array is increasingly difficult to control with device sizes scaling down, the dispersion increases and so must the TMR. Obtaining a large TMR is more difficult in interface-induced p-MTJs, because the layer width must be reduced in order to boost the magnetic anisotropy; however, a TMR ratio as large as 350% has been demonstrated [45].

With growing data services such as Big Data analysis the need for additional memory capacity and speed as well as in-memory computing has increased dramatically. The last-level cache memory must be increased [46-48] to bridge the memory-bandwidth gap between central processing units (CPUs) and the main memory. The CPU performance can be significantly boosted by using fast non-volatile memories in cache for data storing without the need to address the main memory.

In particular, the use of STT MRAM as the last-level cache memory helps bridging the memory-bandwidth gap between multi-core CPUs and the main memory. Ultra-large volatile DRAM devices are available; however, due to the high refresh rate and thus high power consumption their use as last-level caches has been limited. The introduction of non-volatility to reduce energy consumption in last-level cache memory can increase the CPU performance significantly by using this cache for data storing and processing without the need to address the main memory.

Advanced STT MRAM is characterized by high-speed access with less than 10ns. It is thus suitable for last-level cashes where it guarantees about ten times power reduction [49-51], while other types of non-volatile memories are much slower and cannot provide such a high speed access. 4Gbit density STT MRAM arrays with p-MTJs and compact memory cell were recently reported [39]. On May 26th, 2017, Samsung [52] reaffirmed the beginning of production of embedded STT MRAM based on the 28nm silicon-on-insulator technology node [41] in 2018. On September 15th, 2017, Globalfoundries announced the beginning of embedded STT MRAM production based on the 22nm fully-depleted silicon-on-insulator technology [53]. We are therefore witnessing the beginning of non-volatile STT MRAM entering the DRAM and potentially SRAM markets, traditionally dominated by CMOS-based volatile devices. If successful, it will result in an exponential expansion of the STT MRAM market with a momentous impact on information storage and processing in the near future.

3.2 Advanced MRAM

Although STT MRAM is competitive with DRAM for embedded memory applications and can also be used in level three caches in CPUs, increasing write currents for faster switching prevents it from being used in level one caches, where very fast switching is required. An ultimate swap to p-MTJs and Gilbert damping reduction are two common paths to reduce the switching current; however, these efforts are counteracted by the necessity to maintain high thermal stability which requires high perpendicular magnetic anisotropy [30].

There are indications that by downscaling the p-MTJ diameter the switching current decreases faster than the thermal stability factor, which has been shown to be as high as 120 in p-MTJs with a diameter of 30nm [54]. Nevertheless, it is preferred to have an alternative way to switch the free layer.

Interface-induced perpendicular magnetic anisotropy materials provide a sufficiently large thermal stability factor for free layers with diameters down to 12-14nm. Since the anisotropy is determined by the interface properties, it can be altered by applying an electric field. The electric field polarizes the charge densities of the interfacial atoms, thereby modifying overlap integrals and exchange interactions. This may soften the perpendicular magnetic anisotropy thus reducing the switching energy barrier and even changing it to in-plane. The magnetization can easily be pushed over the barrier by a small current and stabilized in the state with an opposite magnetization after the voltage is removed.

3.2.1 Voltage-controlled MRAM

An MRAM controlled by voltage [55-58] is a viable option for last-level cache applications. The voltage-controlled MRAM switching principle is based on voltage-mediated removal of the potential barrier separating the two stable magnetization orientation states. Without the barrier the magnetization precesses around the effective magnetic field and can be put into the alternative magnetization state, when the potential barrier is re-introduced at the end of the voltage pulse [59].

Because the voltage-induced switching is unipolar, the voltage controlled MRAM is free from the read disturb which is characteristic to STT MRAM. Although voltage controlled MRAM is a two-terminal device, the separation between read and write is performed by alternating the polarities during these two operations.

Voltage controlled MRAM has a few unsolved issues so far preventing it from being broadly used in applications. One of the problems originates in the precession at switching and thus depends on the initial state determined by the fluctuating thermal and unwanted variability. This variability results in write errors and must be suppressed.

The second problem is a larger resistance of the memory cell compared to STT MRAM, which results in smaller currents. Small currents lead to a longer delay while reading the state by a sense amplifier. As it was shown recently [60], both problems can be solved by carefully tailoring and optimizing the entire circuit.

Extending the ideas of voltage-controlled magnetic anisotropy, the voltage pulse can be applied not only to lower the potential barrier between the two magnetization states but also to boost it to make the switching harder [60]. The switching is mediated by a spin-orbit and/or spin Hall torque generated by the current flowing through a conductive line made of a heavy metal underneath the magnetic MTJ, ensuring the write operation without an external magnetic field [61]. If reading is performed by applying the voltage pulse with its polarity opposite to that used for writing, the potential barrier is increased, hardening the cell immunity against read disturb errors.

3.2.2 Spin-orbit torque MRAM

Among the newly discovered physical phenomena suitable for next-generation MRAM are the spin Hall effect and the spin-orbit torque (SOT) switching [62-66]. Current passing in a material with a high spin Hall angle/SOI results in spin-orbit torques capable to switch the free layer of an MTJ. This way the read and write currents are decoupled, which prevents the tunnel barrier from damage and improves device reliability.

The spin Hall effect and/or SOT alone do not provide switching in devices with perpendicular magnetization. To provide switching, it is required to apply an external magnetic field. In addition, innovative materials are required to increase the torques and to boost the switching efficiency. New materials with a strong SOI, e.g., topological insulators, allow the current to flow only at their interface states [67]. Due to the spin-momentum locking characteristic to these states the passing current results in a large spin accumulation at the interface [68,69] and the SOT aids the magnetization to switch.

A potential disadvantage of the write and read current paths' separation is that these devices appear in a three-terminal cell configuration [70]. Therefore, they can be used only for applications in which the density is not the top priority, but for high-speed reliable operation competing with SRAM.

There exists a different design of a three-terminal MRAM cell, where the switching is done by the current induced fast domain wall motion within a ferromagnetic material between the two ferromagnetic electrodes, while reading is done by means of an additional ferromagnetic contact grown on top of the ferromagnetic layer [70]. The domain wall is pushed by both STT and spin SOT, with the relative strength of each contribution tuned by proper engineering the magnetic layer structure. The domain walls can be moved very fast [71,72], which is attractive for high speed applications. However, the critical current densities obtained experimentally are still high. A reduction of the critical currents by minimizing the domain wall pinning in domain wall MRAM may compromise the data retention. Similar to SOT-based MRAM, the reduction of the current density, while maintaining the domain wall speed, remains a critical challenge for domain wall motion based MRAM.

The need to lower the critical current in advanced MRAM accelerates the search for new materials with large SOI. A promising candidate for such a material is a topological insulator, for which a large spin Hall angle has been demonstrated [67]. A general form of the relevant torque terms in the presence of spin-orbit interaction can be determined by symmetry considerations [73,74]. As SOTs appear at the interface between a material with high SOI and a ferromagnet, a description of these torques by means of boundary conditions was recently suggested [75,76]. The corresponding boundary conditions allow to relate the non-equilibrium spin accumulation at both sides of the interface in presence of the in-plane current and couple them to the magnetization dynamics.

4 Non-volatile logic

MRAM is CMOS compatible and attractive to use with CMOS-based logic applications. Fast non-volatile memory combined with non-volatile processing elements is a fertile ground for realizing the first microprocessors with reduced power consumption working on an entirely new principle. In addition, MRAM arrays are embedded directly on top of CMOS logic [77]. This allows reducing the length of interconnects and the corresponding delay time.

4.1 CMOS-MRAM hybrid logic

The computer architecture where non-volatile elements are located on a chip with CMOS devices is traditionally called logic-in-memory, although as of yet no information is processed in non-volatile elements. Power-efficient MRAM-based logic-in-memory concepts have already been demonstrated [78]. They include field-programmable gate arrays and ternary content addressable memory as well as other variants. These CMOS/spintronic hybrid solutions are already competitive in comparison to the conventional CMOS technology with respect to power consumption and speed.

The power consumption problem in modern integrated circuits with ultra-scaled CMOS devices is becoming critical, which prompts various power reduction technologies to be used for keeping the heat dissipation

under control. The techniques based on reduced voltage operation, clock gating, and power gating modes allow to address the problem to a certain extent, however, they also result in an increase of the time delay to get into or out from these modes. The use of non-volatile MRAM-based devices [79-81] with fast access to the stored data allows cutting out the penalty of stand-by power and eliminates the delays when using energy saving modes. The first microcontroller unit with zero standby power featuring non-volatile elements is operating at 8MHz [82]. In order to boost the operating frequency, spin-based non-volatile flip-flops were recently used to demonstrate a power-gating microcontroller unit [78] fabricated with standard 90nm CMOS technology with an additional MTJ process. The chip features a very short delay in entering/exiting power-on/power-off with the potential to be further reduced by optimizing parasitic capacitances.

Another new circuit example is a field programmable gate array built with non-volatile devices. Here, temporal data is quickly saved in magnetic tunnel junctions before the power is turned off. This has a great potential to reduce the power consumption, which becomes a critical issue in conventional SRAM-based gate arrays [83-85]. By using a logic-in-memory structure [86,87], replacing SRAM cells with non-volatile flip-flops [88] and smartly connected redundant MTJs to avoid resistance variations [89], the area of a six-input look-up table is shown to be reduced by about 50% [78].

Ternary content-addressable memory (TCAM) is able to perform a very high-speed search to match an input [90]. CMOS-based TCAM suffers from standby power losses and relatively high costs due to its complex structure [90]. Employing a 2T-2MTJ structure for the equality search logic part reduces the TCAM cell area [91,92]. A 1Mb non-volatile TCAM chip with a 6T-2MTJ cell structure fabricated in 90nm CMOS and perpendicular MTJ technologies has been demonstrated [93], with 9T-2MTJ [94], 7T-2MTJ [95], 4T-2MTJ [96], and 5T-4MTJ [97] modifications for high-speed accessibility and reduced variation effects have been also reported. Currently, the TCAM cell structure design as well as the word segmentation algorithm optimization is under intense investigation [78] in order to increase speed and reduce the area.

With the continued rapid development of smartphones and mobile video applications it becomes necessary to introduce non-volatile elements into important circuits responsible for performance acceleration. A motion-vector prediction circuit is critical for performing mobile video compression by finding motion vectors between two adjacent frames. It has been demonstrated that the introduction of non-volatile elements to implement a full adder helps making the circuit compact, fast, and stable [98-102]. The introduction of non-volatility and a logic-in-memory architecture helps reduce power consumption by 45% [103]. With the activation ratio of embedded clusters decreased a reduction of 97% is possible [78]. Another example of an application specific circuit currently under thorough investigation is a brain-inspired computing network with non-volatile elements, which also demonstrates a large, i.e., more than 90%, power reduction on average when compared to its CMOS based counterparts [78].

4.2 Intrinsic logic-in-memory

The current age of Big Data requires an unprecedented level of data storage capacity complemented with efficient processing capabilities. The data processing is typically confined in large data centers, which appears to customers as a cloud computing environment to enable resource flexibility. The scale of data centers (and their power consumption) is increasing exponentially. One of the limitations of current computing systems is the overhead of transferring data between memory and processors. As already mentioned, the problem can be solved by placing the main memory closer to processors. Another efficient solution will be to perform at least part of the data processing already in the storage by designing a memory architecture with enhanced functionalities capable to directly perform a set of Big Data-oriented, memory-centric operations. This methodology promises a dramatic reduction in the need for data transfers between memory and processor, eliminating the interconnection bottleneck, by creating a new high performance and low power efficient computing paradigm, where the data is not only stored but also analyzed by non-volatile stand-by-power free processing units.

Placing the actual computation into the magnetic domain reduces the need of converting magnetically stored information into currents and voltages for processing and helps not only to simplify the circuit layout but also increases the integration density. The idea is to use MTJs as elementary blocks for non-conventional logic-in-memory architectures. Our invention, which shows that on an MRAM array any two of the coupled 1T-1MTJ cells can serve simultaneously as non-volatile memory and computing units by performing a logical implication operation, has been granted a patent [104]. These structures inherently realize non-volatile logic-in-memory circuits with zero-standby power, where the same elements are used for storing and also processing information. They have a great potential for Big Data storing and computing, as they are also opening a path for developing computing architectures conceptually different from the still standard Von Neumann architecture. A new design of an implication-based full

adder involves six 1T-1MTJ cells with 27 subsequent FALSE and material implication operations [105].

The paradigm of employing memory for information processing is perfectly suited for the Big Data revolution we are experiencing now by providing computation capabilities within memory itself, thus eliminating the need for data communication between memory and the processor. However, precisely because of the absence of a clear division between memory and the computing unit this intrinsic logic-in-memory architecture is completely different from the Von Neumann architecture currently employed, and a development of a conceptually new calculation paradigm using this architecture is needed.

An alternative option is to follow a more conventional path with memory and computing units separated, where, however, both elements are non-volatile and implemented in a magnetic domain. Placing the actual computation into the magnetic domain reduces the need of converting magnetically stored information into the currents and voltages for processing. It also simplifies the circuit layout and boosts the integration density. The idea of combining MTJs with a common free layer enables the realization of an efficient nanooscillator [106] and a non-volatile magnetic flip-flop [107]. The computation unit is represented by the STT based non-volatile majority gate, with non-volatile magnetic flip-flops [107] used as memory registers. Because all the data processing elements are performed in the magnetization domain, the flip-flops could be put at the legs of the majority gates thus removing the need of data transfer and interconnects between the processing unit and memory. By using the non-volatile computation unit the realization of a 1-bit full adder in magnetic domain is demonstrated [108].

Finally, we mention a completely different neural network based approach to calculations. Non-volatile MTJs fit for neural network realizations as they can be considered as a current-driven programmable resistor – memristor – and they significantly advance programming and storage functions. MTJ based neural networks have been demonstrated featuring non-volatile synapses [109] for high-speed pattern recognition with about 70% reduction of gate count and 99% improvement in speed. Neuromorphic computing is becoming a reality, with the first self-learning chip revealed on September 25th, 2017 by Intel [110].

5 Conclusions

Spin transistors have been recently successfully demonstrated, however, an enhancement of the on-current ratio between the parallel and anti-parallel source/drain magnetization configuration at room temperature remains one of the main challenges. As both Spin-FET and SpinMOSFET still rely on the charge current to transfer the spin, it sets limitations for the applicability of such devices in main-stream microelectronics, and new ideas are needed for the future.

Non-volatile devices based on MTJs possess a TMR suitable for practical applications. Several companies announced embedded STT MRAM production in 2018. Although STT MRAM is positioned as a successor not only for flash, but also for CMOS-based main computer memory, the relatively high switching current and power may confine STT-MRAM to replacing flash memory in data-intensive and low-power mobile, automotive, or Internet of Things applications. Because of the large switching currents and insufficient speed, STT-MRAM is unlikely to replace SRAM in high-level core caches. Novel innovative non-volatile devices with improved switching characteristics and low power consumption are required for processor-embedded memories.

Finally, the successful adoption of non-volatility in microelectronic systems by developing various logic-in-memory architectures and in-memory processing will inevitably result in increasing disseminations of this technology for other applications such as ultra-low-power electronics, high-performance computing, the Internet of Things, and Big Data analysis.

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7 References

1. S.-E. Thompson, M. Armstrong, C. Auth *et al.,* A 90-nm Logic Technology Featuring Strained-Silicon, *IEEE Trans. Electron Dev.*, vol. 51, pp. 1790–1797, 2004. DOI: 10.1109/TED.2004. 836648
2. K. Mistry, C. Allen, C. Auth *et al.,* A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging, *IEDM Techn. Digest*, pp. 247–250, 2007. DOI: 10.1109/IEDM.2007.4418914

3. S. Natarajan, M. Armstrong, M. Bost *et al.,* A 32nm Logic Technology Featuring 2nd-Generation High-k + Metal-Gate Transistors, Enhanced Channel Strain and 0.171μm² SRAM Cell Size in a 291Mb Array, *IEDM Techn. Digest*, pp. 941–943, 2008. DOI: 10.1109/IEDM.2009.5424253
4. R. Xie, P. Montanini, K. Akarvardar *et al.,* A 7nm FinFET Technology Featuring EUV Patterning and Dual Strained High Mobility Channels, *IEDM Techn. Digest*, pp. 47–50, 2016. DOI: 10.1109/IEDM.2016.7838334
5. S.-Y. Wu, C. Y. Lin, M. C. Chiang *et al.,* 7nm CMOS Platform Technology Featuring 4th Generation FinFET Transistors with a 0.027um² High Density 6-T SRAM cell for Mobile SoC Applications, *IEDM Techn. Digest*, pp. 43–46, 2016. DOI: 10.1109/IEDM.2016.7838333
6. International Technology Roadmap for Semiconductors (2016). Available: http://www.itrs2.net/
7. H. Ohno, M. Stiles, B. Dieny, Spintronics, *Proc. of the IEEE*, vol.104, pp. 1782–1786, 2016. DOI: 109/JPROC.2016.260116301163
8. S. Datta, B. Das, Electronic Analog of the Electro-Optic Modulator, *Appl. Phys. Lett.*, vol. 56 (7), pp. 665–667, 1990. DOI: 10.1063/1. 102730
9. S. Sugahara, J. Nitta, Spin-Transistor Electronics: An Overview and Outlook, *Proc. of the IEEE*, vol. 98, pp. 2124–2154, 2010. DOI: 10.1109/JPROC.2010.2064272
10. I. Zutic, J. Fabian, S. Das Sarma, Spintronics: Fundamentals and Applications, *Rev. Mod. Phys*., vol. 76, pp. 323–410, 2004. DOI: 10.1103/RevModPhys.76.323
11. J. Fabian, A. Matos-Abiaguea, C. Ertler, P. Stano, I. Zutic, Semiconductor Spintronics, *Acta Phys. Slovaca*, vol. 5, pp. 565–907, 2007. http://www.physics.sk/aps/pubs/2007/aps-07-04/aps-07-04.pdf
12. P. Li, H. Dery, Spin-Orbit Symmetries of Conduction Electrons in Silicon, *Phys. Rev. Lett*. vol. 107, 107203, 2011. DOI: 10.1103/PhysRevLett.107.107203
13. O. Chalaev, Y. Song, H. Dery, Suppressing the Spin Relaxation of Electrons in Silicon, *Phys. Rev. B*, vol. 95, 035204, 2017. DOI: 10.1103/PhysRevB.95.035204
14. V. Sverdlov, S. Selberherr, Silicon Spintronics: Progress and Challenges, *Phys. Rep.*, vol. 585, pp. 1–40, 2015. DOI:10.1016/j.physrep.2015.05.002.
15. V. Sverdlov, Strain-induced Effects in Advanced MOSFETs, Springer, 2011.
16. V. Sverdlov, J. Ghosh, S. Selberherr, Universal Dependence of the Spin Lifetime in Silicon Films on the Spin Injection Direction, in *Abstracts Workshop on Innovative Devices and Systems (WINDS)*, p. 7, 2016.
17. Y. Bychkov, E. Rashba, Properties of a 2D Electron Gas with Lifted Spectral Degeneracy, *JETP Lett*. vol. 39, pp. 78–81, 1984. Available: http://www.jetpletters.ac.ru/ps/1264/article_19121.shtml
18. P. Chuang, S.-C. Ho, L.W. Smith *et al.*, All-electric All-semiconductor Spin Field-effect transistors, *Nature Nanotechnol*., vol. 10, pp. 35–39, 2015. DOI: 10.1038/nnano.2014.296
19. W. Yan, O. Txoperena, R. Llopis *et al.*, A Two-dimensional Spin Field-effect Switch, *Nature Communications*, vol. 7, 13372, 2016. DOI: 10.1038/ncomms13372
20. T. Tahara, H. Koike, M. Kameno, *et al*., Room-temperature Operation of Si Spin MOSFET with High on/off Spin Signal Ratio, *Appl. Phys. Express*, vol. 8**,** 11304 2015. DOI: 10.7567/APEX.8.113004
21. E. I. Rashba, Theory of Electrical Spin Injection: Tunnel Contacts as a Solution of the Conductivity Mismatch Problem, *Phys. Rev. B*, vol. 62, pp. R16267–R16270, 2000. DOI: 10.1103/PhysRevB.62.R16267
22. T. Tahara, Y. Ando, M. Kameno *et al.*, Observation of Large Spin Accumulation Voltages in Non-degenerate Si Spin Devices due to Spin Drift Effect: Experiments and Theory, *Phys. Rev. B*, vol. 93, 214406, 2016. DOI: 10.1103/PhysRevB.93.214406
23. R. Jansen, Silicon Spintronics, *Nature Materials*, vol. 11, pp. 400–408, 2012. DOI: 10.1038/nmat3293
24. Y. Song and H. Dery, Magnetic-Field-Modulated Resonant Tunneling in Ferromagnetic-Insulator-Nonmagnetic Junctions, *Phys. Rev. Let.* vol. 113, 047205, 2014. DOI: 10.1103/PhysRevLett.113.047205
25. Z. Yue, M. C. Prestgard, A. Tiwari, M. E. Raikh, Resonant Magnetotunneling between Normal and Ferromagnetic Electrodes in Relation to the Three-terminal Spin Transport, *Phys. Rev. B,* vol. 91, 195316 2015. DOI: 10.1103/PhysRevB.91.195316
26. V. Sverdlov, J. Weinbub, S. Selberherr, Spin-Dependent Trap-Assisted Tunneling in Magnetic Tunnel Junctions: A Monte Carlo Study, in *Abstract Book Intl. Workshop on Computational Nanotechnology (IWCN),* pp. 88 – 90, 2017.
27. A. Fert, Nobel Lecture: Origin, Development, and Future of Spintronics, *Rev. Modern Phys*., vol. 80, pp. 1517–1530, 2008. DOI: 10.1103/RevModPhys.80.1517
28. P. A. Grunberg, Nobel Lecture: From Spin Waves to Giant Magnetoresistance and Beyond, *Rev. Modern Phys*., vol. 80, pp. 1531–1540, 2008. DOI: 10.1103/RevModPhys.80.1531
29. S. Ikeda, J. Hayakawa, Y. Ashizawa *et al*., Tunnel Magnetoresistance of 604% at 300 K by Suppression of Ta Diffusion in CoFeB/MgO/CoFeB Pseudo-spin-valves Annealed at High Temperature, *Appl. Phys. Lett.*, vol. 93, 082508, 2008. DOI: 10.1063/1.2976435

30. D. Apalkov, B. Dieny, and J. M. Slaughter, Magnetoresistive Random Access Memory, *Proc. of the IEEE*, vol. 104, pp. 1796–1830, 2016. DOI: 10.1109/JPROC.2016.2590142
31. J. Slonczewski, Current-driven Excitation of Magnetic Multilayers, *J. Magn. Mater.*, vol. 159, pp. L1–L7, 1996. DOI: 10.1016/0304-8853(96)00062-5
32. L. Berger, Emission of Spin Waves by a Magnetic Multilayer Traversed by a Current, *Phys. Rev. B*, vol. 54, pp. 9353–9358, 1996. DOI: 10.1103/PhysRevB.54.9353
33. Electronicdesign.com, 4-Mbit Device is First Commercially Available MRAM, Electronic Design, 2006. Available: http://electronicdesign.com/dsps/4-mbit-device-first-commerciallyavailable-mram
34. L. Savtchenko, B. Engel, N. Rizzo, M. Deherrera, J. Janesky, Method of Writing to Scalable Magnetoresistance Random Access Memory Element, US Patent 6545906 B1, 2003. https://www.google.com/patents/US6545906
35. R. Sbiaa, H. Meng, and S. N. Piramanayagam, Materials with Perpendicular Magnetic Anisotropy for Magnetic Random Access Memory, *Phys. Stat. Solidi (RRL) – Rapid Research Letters,* vol. 5, pp. 413–419, 2011. DOI: 10.1002/pssr.201105420
36. Y. Huai, F. Albert, P. Nguyen *et al.,* Observation of Spin-transfer Switching in Deep Submicron-sized and Low-resistance Magnetic Tunnel Junctions, *Appl. Phys. Lett.,* vol. 84, pp. 3118–3120, 2004. DOI: 10.1063/1.1707228
37. Z. Diao, D. Apalkov, M. Pakala *et al*., Spin Transfer Switching and Spin Polarization in Magnetic Tunnel Junctions with MgO and AlO_x Barriers, *Appl. Phys. Lett.,* vol. 87, 232502, 2005. DOI: 10.1063/1.2139849
38. N. D. Rizzo, D. Houssameddine, J. Janesky *et al.,* A Fully Functional 64 Mb DDR3 ST-MRAM Built on 90 nm CMOS Technology, *IEEE Trans. Magn.*, vol. 49, pp. 4441–4446, 2013. DOI: 10.1109/TMAG.2013.2243133
39. S.-W. Chung, T. Kishi, J. W. Park *et al.,* 4Gbit Density STT-MRAM Using Perpendicular MTJ Realized with Compact Cell Structure, *IEDM Techn. Digest*, pp. 659–662, 2016. DOI: 10.1109/IEDM.2016.7838490
40. B. Dieny, R. Sousa, S. Bandiera *et al.,* Extended Scalability and Functionalities of MRAM Based on Thermally Assisted Writing, *IEDM Techn. Digest*, pp. 1.3.1–1.3.4, 2011. DOI: 10.1109/IEDM.2011.6131471
41. Y. J. Song, J. H. Lee, H. C. Shin *et al*., Highly Functional and Reliable 8Mb STT-MRAM Embedded in 28nm Logic, *IEDM Techn. Digest*, pp. 663–666, 2016. DOI: 10.1109/IEDM.2016.7838491
42. H. Sato, M. Yamanouchi, S. Ikeda *et al.*, MgO/CoFeB/Ta/CoFeB/MgO Recording Structure in Magnetic Tunnel Junctions with Perpendicular Easy Axis, *IEEE Trans. Magn.*, vol. 49, pp. 4437–4440, 2013. DOI: 10.1109/TMAG.2013.2251326
43. A. Makarov, V. Sverdlov, D. Osintsev, S. Selberherr, Reduction of Switching Time in Pentalayer Magnetic Tunnel Junctions with a Composite-Free Layer, *Phys. Stat. Solidi (RRL) – Rapid Research Letters*, vol. 5, pp. 420–422, 2011. DOI: 10.1002/pssr.201105376
44. A. Makarov, T. Windbacher, V. Sverdlov, S. Selberherr, CMOS-Compatible Spintronic Devices: A Review, *Semicond. Sci. and Tech.*, vol. *31*, 113006, 2016. DOI: 10.1088/0268-1242/31/11/113006
45. M. Krounbi, V. Nikitin, D. Apalkov *et al*., Status and Challenges in Spin-Transfer Torque MRAM Technology, in *Proc. of ECS Meeting*, 2015. Available: http://ecst.ecsdl.org/content/69/3/119.abstract
46. M. T. Chang, P. Rosenfeld, S. L. Lu B. Jacob, Technology Comparison for Large Last level Caches (L3 Cs): Low leakage SRAM, Low Write-energy STT-RAM, and Refresh-optimized eDRAM, *in Proc. 19th Intl. Symp. High Performance Computer Architecture (HPCA)*, pp. 143–154, 2013. DOI: 10.1109/HPCA.2013.6522314
47. T. Endoh, T. Ohsawa, H. Koike *et al.,* Restructuring of Memory Hierarchy in Computing System with Spintronics-based Technologies, in *Symp. VLSI Technol.*, pp. 89–90, 2012. DOI: 10.1109/VLSIT.2012.6242475
48. T. Endoh, Nonvolatile Logic and Memory Devices Based on Spintronics, in *Proc. of IEEE Intl. Symp. Circ. Syst*., pp. 13–16, 2015. DOI: 10.1109/ISCAS.2015.7168558
49. H. Noguchi, K. Ikegami, N. Shimomura *et al.,* Highly Reliable and Low-power Nonvolatile Cache Memory with Advanced Perpendicular STT-MRAM for High-performance CPU, *in Symp. VLSI Circuits*, pp. 97–98, 2014. DOI: 10.1109/VLSIC.2014.6858403
50. G. Jan, L. Thomas, S. Le *et al*., Achieving Sub-ns Switching of STT-MRAM for Future Embedded LLC Applications through Improvement of Nucleation and Propagation Switching Mechanisms*, in Symp. VLSI Technol.*, pp. 18–19, 2016. DOI: 10.1109/VLSIT.2016.7573362
51 H. Noguchi, K. Ikegami, S. Takaya *et al*., 7.2 4Mb STT-MRAM-based Cache with Memory-access-aware Power Optimization and Write-verify-write / Read-modify-write scheme, *in ISSCC Dig. Tech. Papers*, pp. 132–133, 2016. DOI: 10.1109/ISSCC.2016.7417942
52. https://www.mram-info.com/tags/companies/samsung

53. https://www.globalfoundries.com/news-events/press-releases/globalfoundries-launches-embedded-mram-22fdxr-platform
54. L. Thomas, G. Jan, J. Zhu *et al.,* Perpendicular Spin Transfer Torque Magnetic Random Access Memories with High Spin Torque Efficiency and Thermal Stability for Embedded Applications, *J. Appl. Phys.,* vol. 115, 172615, 2014. DOI: 10.1063/1.4870917
55. T. Nozaki, Y. Shiota, M. Shiraishi *et al*., Voltage-induced Perpendicular Magnetic Anisotropy Change in Magnetic Tunnel Junctions, *Appl. Phys. Lett*., vol. 96, 022506, 2010. DOI: 10.1063/1.3279157
56. Y. Shiota, T. Nozaki, F. Bonell *et al.,* Induction of Coherent Magnetization Switching in a Few Atomic Layers of FeCo Using Voltage Pulses, *Nature Materials*, vol. 11, pp. 39-43, 2012. DOI: 10.1038/nmat3172
57. Y. Shiota, T. Nozaki, S. Tamaru *et al.,* Evaluation of Write Error Rate for Voltage-driven Dynamic Magnetization Switching in Magnetic Tunnel Junctions with Perpendicular Magnetization, *Appl. Phys. Express*, vol. 9, 013001, 2015. DOI: 10.7567/APEX.9.013001
58. K. L. Wang, X. Kou, P. Upadhyaya *et al.*, Electric-Field Control of Spin-Orbit Interaction for Low-Power Spintronics, *Proc. of the IEEE*, vol. 104, pp. 1974-2008, 2016. DOI: 10.1109/JPROC.2016.2573836
59. M. K. Niranjan, CG. Duan, S. S. Jaswal, E. Tsymbal, Electric Field Eeffect on Magnetization at the Fe/MgO(001) Interface, *Appl. Phys. Lett*., vol. 96, 222504, 2010. DOI: 10.1063/1.3443658
60. H. Noguchi, K. Ikegami, K. Abe *et al*., Novel Voltage Controlled MRAM (VCM) with Fast Read/Write Circuits for Ultra Large Last Level Cache, in *IEDM Techn. Digest*, pp.675–678, 2016. DOI: 10.1109/IEDM.2016.7838494
61. H. Yoda, N. Shimomura, Y. Ohsawa *et al.,* Voltage-Control Spintronics Memory (VoCSM) Having Potentials of Ultra-Low Energy-Consumption and High-Density, *in IEDM Techn. Digest*, pp.679–682, 2016. DOI: 10.1109/IEDM.2016.7838495
62. I. M. Miron, G. Gaudin, S. Auffret *et al.,* Current-driven Spin Torque Induced by the Rashba Effect in a Ferromagnetic Metal Layer, *Nature Materials*, vol. 9, pp. 230–234, 2010. DOI: 10.1038/nmat2613
63. I. M. Miron, K. Garello, G. Gaudin *et al.,* Perpendicular Switching of a Single Ferromagnetic Layer Induced by In-plane Current Injection, *Nature*, vol. 476, pp. 189–193, 2011. DOI: 10.1038/nature10309
64. L. Liu, O. J. Lee, T. J. Gudmundsen *et al*., Current-induced Switching of Perpendicularly Magnetized Magnetic Layers Using Spin Torque from the Spin Hall Effect, *Phys. Rev. Lett*., vol. 109, 096602, 2012. DOI: 10.1103/PhysRevLett.109.096602
65. A. Brataas and K. M. D. Hals, Spin-orbit Torques in Action," *Nature Nanotechnol*., vol. 9, pp. 86–88, 2014. DOI: 10.1038/nnano.2014.8
66. M. Cubukcu, O. Boulle, M. Drouard *et al.,* Spin-orbit Torque Magnetization Switching of a Three-terminal Perpendicular Magnetic Tunnel Junction, *Appl. Phys. Lett*., vol. 104, 042406, 2014. DOI: 10.1063/1.4863407
67. Y. Fan, P. Upadhyaya, X. Kou *et al.,* Magnetization Switching through Giant Spin–orbit Torque in a Magnetically Doped Topological Insulator Heterostructure, *Nature Materials*, vol.13, pp. 699–704, 2014. DOI: 10.1038/nmat3973
68. C. H. Li, O. M. J. Van't Erve, J. T. Robinson *et al.,* Electrical Detection of Charge-current-induced Spin Polarization due to Spin-momentum Locking in Bi_2Se_3, *Nature Nanotechnol*., vol. 9, pp. 218–224, 2014. DOI: 10.1038/nnano.2014.16
69. C. H. Li, O. M. J. Van't Erve, S. Rajput *et al.,* Direct Comparison of Current-induced Spin Polarization in Topological Insulator Bi_2Se_3 and InAs Rashba States, *Nature Communications*, vol. 7, 13518, 2016. DOI: 10.1038/ncomms13518
70. S.-W. Lee, K.-J. Lee, Emerging Three-Terminal Magnetic Memory Devices, *Proc. of the IEEE*, vol. 104, pp. 1831–1843, 2016. DOI: 10.1109/JPROC.2016.2543782
71. L. Thomas, K.-S.Ryu, S.-H. Yang, and S. S. P. Parkin, Chiral Spin Torque at Magnetic Domain Walls, *Nature Nanotechnol*., vol. 8, pp. 527–533, 2013. DOI: 10.1038/nnano.2013.102
72. S. Emori, U. Bauer, S.-M. Ahn et al., Current-driven Dynamics of Chiral Ferromagnetic Domain Walls, *Nature Materials*, vol. 12, pp. 611–616, 2013. DOI: 10.1038/nmat3675
73. R. G. Elías, N. Vidal-Silva, and A. Manchon, Steady Motion of Skyrmions and Domains Walls under Diffusive Spin Torques, *Phys. Rev. B*, vol. 95, 104406, 2017. DOI: 10.1103/PhysRevB.95.104406
74. E. van der Bijl and R. A. Duine, Current-induced Torques in Textured Rashba Ferromagnets, *Phys. Rev. B*, vol. 86, 094406, 2012. DOI: 10.1103/PhysRevB.86.094406
75. V. P. Amin and M. D. Stiles, Spin Transport at Interfaces with Spin-orbit Coupling: Formalism, *Phys. Rev. B*, vol. 94, 104419, 2016. DOI: 10.1103/PhysRevB.94.104419
76. V. P. Amin and M. D. Stiles, Spin Transport at Interfaces with Spin-orbit Coupling: Phenomenology, *Phys. Rev. B*, vol. 94, 104420, 2016. DOI: 10.1103/PhysRevB.94.104420
77. J.-G. Zhu, Magnetoresistive Random Access Memory: The Path to Competitiveness and Scalability, *Proc. of the IEEE*, vol. 96, pp. 1786–1798, 2008. DOI: 10.1109/JPROC.2008.2004313

78. T. Hany, T. Endoh, D. Suzuki *et al.,* Standby-Power-Free Integrated Circuits Using MTJ-Based VLSI Computing, *Proc. of the IEEE*, vol. 104, pp. 1844-1863, 2016. DOI: 10.1109/JPROC.2016.2574939
79. T. Endoh, S. Togashi, F. Iga *et al.,* A 600 MHz MTJ-based Nonvolatile Latch Making Use of Incubation Time in MTJ Switching, *IEDM Techn. Digest*, pp.75–78, 2011. DOI: 10.1109/IEDM.2011.6131487
80. N. Sakimura, Y. Tsuji, R. Nebashi *et al.,* A 90 nm 20 MHz Fully Nonvolatile Microcontroller for Standby-Power-Critical Applications, in *Proc. of IEEE Intl. Solid-State Circuits Conf.,* p. p. 184–185, 2014. DOI: 10.1109/ISSCC.2014.6757392
81. H. Koike, T. Ohsawa, S. Ikeda *et al.,* A Power-gated MPU with 3-microsecond Entry/Exit Delay Using MTJ-based Nonvolatile Flip-Flop, in *Proc. of IEEE A-SSCC.*, pp. 317–320, 2013. DOI: 10.1109/ASSCC.2013.6691046
82. S. C. Bartling, S. Khanna, M. P. Clinto *et al.*, An 8 MHz 75 μA/MHz Zero-leakage Non-volatile Logic-based Cortex-M0 MCU SoC Exhibiting 100% Digital State Retention at V_{DD} = 0 V with < 400 ns Wakeup and Sleep Transition, in *Proc. IEEE Intl. Solid-State Circuits Conf.,* pp. 432–433, 2013. DOI: 10.1109/ISSCC.2013.6487802
83. Y. Guillemenet, L. Torres, G. Sassatelli *et al.*, A Nonvolatile Run-time FPGA Using Thermally Assisted Switching MRAMs, *in Proc. Intl. Conf. Field-Programmable Logic*, pp. 421–426, 2008. DOI: 10.1109/FPL.2008.4629974
84. Y. Y. Liauw, Z. Zhang, W. Kim *et al.,* Nonvolatile 3D-FPGA with Monolithically Stacked RRAM-based Configuration Memory, in *Proc. IEEE Intl. Solid-State Circuits Conf.*, pp. 406–408, 2012. DOI: 10.1109/ISSCC.2012.6177067
85. Z. Zhang, Y. Y. Liauw, C. Chen, S. S. Wong, Monolithic 3-D FPGAs, *Proc. of the IEEE*, vol. 103, pp. 1197–1210, 2015. DOI: 10.1109/JPROC.2015.24339543954
86. D. Suzuki, M. Natsui, S. Ikeda *et al.,* Fabrication of a Nonvolatile Lookup-table Circuit Chip Using Magneto/Semiconductor-hybrid Structure, for an Immediate-power-up Field Programmable Gate Array, *in Symp. VLSI Circuits*, pp. 80–81, 2009. Available: http://ieeexplore.ieee.org/document/5205282/
87. D. Suzuki, M. Natsui, T. Endoh *et al.,* Six-input Lookup Table Circuit with 62% Fewer Transistors Using Nonvolatile Logic-in-memory Architecture with Series/Parallel-connected Magnetic Tunnel Junctions, *J. Appl. Phys.*, vol. 111, 07E318, 2012. DOI: 10.1063/1.3672411
88. S. Yamamoto, Y. Shuto, and S. Sugahara, Nonvolatile Power-gating Field-programmable Gate Array Using Nonvolatile Static Random Access Memory and Nonvolatile Flip-flops Based on Pseudo-spin-transistor Architecture with Spin-transfer-torque Magnetic Tunnel Junctions, *Jpn. J. Appl. Phys.*, vol. 51, pp. 11PB021–11PB025, 2012. DOI: 10.1143/JJAP.51.11PB02
89. D. Suzuki, M. Natsui, A. Mochizuki *et al.,* Fabrication of a 3000-6-input-LUTs Embedded and Block-level Power-gated Nonvolatile FPGA Chip Using p-MTJ-based Logic-in-memory Structure, *in Symp. VLSI Circuits*, pp. 172–173, 2015. DOI: 10.1109/VLSIT.2015.7223644
90. K. Pagiamtzis and A. Sheikholeslami, Content-addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey, *IEEE J. Solid-State Circuits*, vol. 41, pp. 712–727, 2006. DOI: 10.1109/JSSC.2005.864128
91. S. Matsunaga, K. Hiyama, A. Matsumoto *et al.,* Standby-power-free Compact Ternary Content-addressable Memory Cell Chip Using Magnetic Tunnel Junction Devices, *Appl. Phys. Express*, vol. 2, pp. 0230041–0230043, 2009. DOI: 10.1143/APEX.2.023004
92. S. Matsunaga, M. Natsui, S. Ikeda *et al.,* Implementation of a Perpendicular MTJ-based Read-disturb-Tolerant 2T-2R Nonvolatile TCAM Based on a Reversed Current Reading Scheme, *in Proc. Asia South Pacific Design Autom. Conf.*, pp. 475–476, 2012. DOI: 10.1109/ASPDAC.2012.6164998
93. S. Matsunaga, A. Katsumata, M. Natsui *et al.,* Fabrication of a 99%-energy-less Nonvolatile Multi-functional CAM Chip Using Hierarchical Power Gating for a Massively-parallel Full-text-search Engine, *in Symp. VLSI Circuits*, pp. 106–107, 2013. Available: http://ieeexplore.ieee.org/document/6576611/
94. S. Matsunaga, A. Katsumata, M. Natsui *et al.,* Design of a Nine Transistor/Two-magnetic-tunnel Junction Cell- based Low-energy Nonvolatile Ternary Content-addressable Memory, *Jpn. J. Appl. Phys.*, vol. 51, pp. 02BM061–02BM066, 2012. DOI: 10.1143/JJAP.51.02BM06
95. S. Matsunaga, A. Katsumata, M. Natsui *et al.,* Design of a 270 ps-Access 7T-2MTJ-cell Nonvolatile Ternary Content-addressable Memory, *J. Appl. Phys.*, vol. 111, pp. 07E3361–07E3363, 2012. DOI: 10.1063/1.3677875
96. S. Matsunaga, S. Miura, H. Honjou *et al.,* A 3.14 μm^2 4T-2MTJ-cell Fully Parallel TCAM Based on Nonvolatile Logic-in-memory Architecture, in *Symp. VLSI Circuits*, pp. 44–45, 2012. DOI: 10.1109/VLSIC.2012.6243781

97. S. Matsunaga, A. Mochizuki, N. Sakimura *et al.,* Complementary 5T-4MTJ Nonvolatile TCAM Cell Circuit with Phase-selective Parallel Writing Scheme, *IEICE Electron. Express*, vol. 11, pp. 201402971–201402977, 2014. DOI: 10.1587/elex.11.20140297
98. S. Matsunaga, J. Hayakawa, S. Ikeda *et al.,* Fabrication of a Nonvolatile Full Adder Based on Logic-in-memory Architecture Using Magnetic Tunnel Junctions, *Appl. Phys. Express*, vol. 1, pp. 0913011–0913013, 2008. DOI: 10.1143/APEX.1.091301
99. H.-P. Trinh, W. Zhao, J.-O. Klein *et al.,* Magnetic Adder Based on Racetrack Memory, *IEEE Trans. Circuits Systems*, vol. 60, pp. 1469–1477, 2013. DOI: 10.1109/TCSI.2012.2220507
100. E. Deng, Y. Zhang, W. Kang *et al.,* Synchronous 8-bit Non-volatile Full-adder Based on Spin Transfer Torque Magnetic Tunnel Junction, *IEEE Trans. Circuits Systems*, vol. 62, pp. 1757–1765, 2015. DOI: 10.1109/TCSI.2015.2423751
101. M. Natsui, D. Suzuki, N. Sakimura *et al.,* Nonvolatile Logic-in-memory Array processor in 90 nm MTJ/MOS Achieving 75% Leakage Reduction Using Cycle-based Power Gating, *in Proc. of IEEE Intl. Solid-State Circuits Conf.*, pp. 194–195, 2013. DOI: 10.1109/ISSCC.2013.6487696
102. M. Natsui, D. Suzuki, N. Sakimura *et al.,* Nonvolatile Logic-in-memory LSI Using Cycle-based Power Gating and its Application to Motion-vector Prediction, *IEEE J. Solid-State Circuits*, vol. 50, pp. 476–489, 2015. DOI: 10.1109/JSSC.2014.2362853
103. Y. Ma, T. Shibata, T.Endoh, An MTJ-Based Nonvolatile Associative Memory Architecture with Intelligent Power-saving Scheme for High-speed Low-power Recognition Applications, i*n Proc. of IEEE Intl. Symp. Circ. Syst.,* pp. 1248–1251, 2013. DOI: 10.1109/ISCAS.2013.6572079
104. H. Mahmoudi, T. Windbacher, V. Sverdlov, S. Selberherr, RRAM Implication Logic Gates, *Patent:* Intl., No. Wo 2014/079747 A1; EP 12193826.0. http://www.google.ch/patents/EP2736044A1
105. H. Mahmoudi, V. Sverdlov, S. Selberherr, MTJ-based Implication Logic Gates and Circuit Architecture for Large-Scale Spintronic Stateful Logic Systems, in *Proc. of ESSDERC*, pp. 254 – 257, 2012. DOI: 10.1109/ESSDERC.2012.6343381
106. A. Makarov, V. Sverdlov, S. Selberherr, Geometry Optimization of Spin-Torque Oscillators Composed of Two MgO-MTJs with a Shared Free Layer, in *Proc. of the Intl. Conf. on Nanoscale Magnetism (ICNM)*, p.69, 2013. Available: www.iue.tuwien.ac.at/pdf/ib_2013/CP2013_Makarov_2.pdf
107. T. Windbacher, H. Mahmoudi, V. Sverdlov, S. Selberherr, Spin Torque Magnetic Integrated Circuit, *Patent*: Intl., No. Wo 2014/154497 A1; Patent priority number EP 13161375.4. https://www.google.com/patents/EP2784020B1
108. T. Windbacher, A. Makarov, V. Sverdlov, S. Selberherr, A Universal Nonvolatile Processing Environment, in "Future Trends in Microelectronics - Journey into the Unknown", S.Luryi, J.Xu, A.Zaslavsky (ed); J.Wiley&Sons, pp. 83–91, 2016, DOI: 10.1002/9781119069225.ch1-6
109. Y. Ma and T. Endoh, A Novel Neuron Circuit with Nonvolatile Synapses Based on Magnetic-tunnel-junction for High-speed Pattern Learning and Recognition*, in Proc. Asia-Pacific Workshop Fundam. Appl. Adv. Semicond. Devices (AWAD)*, vol. 4B-1, pp. 273–278, 2015.
110. https://newsroom.intel.com/editorials/intels-new-self-learning-chip-promises-accelerate-artificial-intelligence/

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A Novel Mix-Mode Universal Filter Employing a Single Active Element and Minimum Number of Passive Components

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Abstract: A Novel biquadratic mixed mode tunable universal filter is presented. The mix mode filter is based on a new versatile active element dual X current conveyor differential input transconductance amplifier (DXCCDITA). The filter is capable of realizing high pass (HP), low pass (LP), band pass (BP), notch pass (NP) and all pass (AP) responses in voltage mode (VM), current mode (CM) and trans-impedance mode (TIM). In trans-admittance (TAM) mode the filter can realize HP and BP responses. The striking feature of the design is that it is the first reported mix mode Multi Input Single Output (MISO) filter employing a single active element for the design. Only a few passive elements are required for the design (two capacitors and two resistors). The second resistor is required only for obtaining TIM filter response. By properly exciting the filter structure with appropriate current or voltage signals the filter response in all four modes can be obtained. Additionally, VM response can be obtained both in inverting and non-inverting form simultaneously. The pole frequency and quality factor of the filter are tunable. The analysis of non-idealities and sensitivity is conducted to further study the effect of process variability on the filter response. The filter is simulated in Spice using 0.35µm CMOS model parameters obtained from TSMC. Additionally, the DXCCDITA is also constructed using commercially available integrated circuits (ICs) AD844 and LM13700. The ideal and measured results of the filter for Voltage mode are given to further validate its performance.

Keywords: Current mode; Current conveyor; Cascadable; Mix Mode; Tunable

Nov univerzalen filter z mešanim načinom delovanja z enim aktivnim elementom in minimalnim številom pasivnih komponent

Izvleček: Predstavljen je nov dvokvadrantni univerzalen in nastavljiv filter v mešanem načinu. Filter temelji na novem prilagodljivem aktivnem dvojnem X tokovnem diferencialnem transkonduktančnem ojačevalniku (DXCCDITA). Deluje lahko v visoko, nizko ali pasovno prepustnem načinu (HP, LP ali BP) ter tokovnem, napetostnem ali transimpedančnem načinu (CM, VM, TIM). Je prvi dizajn filtra, ki omogoča mešan način delovanja z le enim aktivnim elementom. Uporabljeni so le štirje pasivni elementi (dva upora in dva kondenzatorja), pri čemer je drugi upor potreben le za doseganje TIM odziva. S pravim tokovno napetostnim vzbujanjem lahko filter deluje v vseh štirih načinih. Dodatno, VM način omogoča simultan invertiran in neinvertiran odziv. Filter je simuliran v SPICE okolju v 0.35µm CMOS tehnologiji. DXCCDITA filter je realiziran s komercialnimi integriranimi vezji AD844 in LM13700. Validacija je prikazana na osnovi simuliranih in merjenih vrednosti v napetostnem načinu delovanja.

Ključne besede: Tokovni način; tokovni ojačevalnik; kaskade; mešan način

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1 Introduction

Filters are an integral part of almost every electronic system and so their synthesis and development remains an ever evolving field. They find applications in signal processing, bio-medical, instrumentation, communication systems etc. Among various filter structures universal filters are the most versatile as all the standard filter functions can be derived from them [1]. They serve as standalone solution to many filtering needs.

Owing to their inherent advantage of wide bandwidth, high slew rate, low power consumption, simple circuitry and excellent linearity [1-3] current conveyors (CC) are widely used in electronic design. Moreover, the requirement of low voltage low power operation put forward by portable electronic devices and the energy harvesting systems [4] etc. further encourages the use of CC. In the present day mixed mode design environment where many systems interact, many times the need arises for the current mode and voltage mode circuits to be connected together. This requirement can be met by employing trans-admittance mode (TAM) and trans-impedance mode (TIM) filter structures which can serve as the interface providing distortion free interaction. Although a number of TAM and TIM filter structures can be found in the literature but a single topology providing the CM, VM, TAM and TIM responses will be an added advantage in terms of area and power requirements. In the past two decades, a number of mixed mode filters have been proposed utilizing different current mode active elements like dual output current controlled current conveyor (DOCCCII), multi output current conveyor (MOCCII) [3], current controlled current conveyor transconductance amplifier (CCCCTA) [3], Current feedback operational amplifiers (CFOA) [3], fully differential current conveyor (FDCCII) [3], differential difference current conveyor and digitally programmable current conveyor (DPCCII) [3] etc.

The filter structures can be classified in three basic groups single input multi output (SIMO) [9], multi input multi output (MIMO) [5], multi input single output (MISO) [6]. The mix mode filters can be categorized based on many criteria like number of active elements utilized, number of passive components employed, requirement of components matching, whether the filter is tunable, number of filter responses realized in each mode, cascadability of the filter etc. The designs in [5, 6, 7, 8, 11, 12, 13, 17] require three or more active elements which results in large chip area and increased parasitic effects. The filter topologies in [10, 14, 16] requires two active elements but four or more passive elements. The mix mode filters in [5, 7, 8, 11] cannot realize all standard filter responses in all the four modes. In addition, filter structures in [6, 12, 13, 14, 16] did not posses inbuilt tuning capability. A comprehensive comparison of some of the exemplary mix mode filter designs with the proposed filter is presented in Table 1. The literature survey shows that except [15] no other single active element based filter to date exists that can function in all the four modes. Furthermore, the design of [15] is MIMO type filter which uses a complex building block, the FDCCII and did not posses inbuilt tuning property and cascadability for all responses in any mode. The filter in [15] requires a matching condition

Table 1: Comparison of the proposed filter with state of art filter topologies available in the literature

Reference	Filter responses realized				Number/Type of Active Block	Passive Elements used	
	VM	CM	TAM	TIM		C	R
5	LP, BP, HP, NP	LP, BP, HP, NP	LP, BP, HP, NP	LP, BP, HP, NP	4/CCCII	2	0
6	All Five	All Five	All Five	All Five	7/CCII	2	8
7	LP, BP, HP	All Five	All Five	LP, BP, HP	3/CCCCTA	2	0
8 Fig. 4	Not Realized	All Five	Not Realized	All Five	2/CCII, 1/MOCCII	2	3
9	All Five	All Five	Not Realized	Not Realized	2/DO-CCCII	2	0
10	All Five	All Five	All Five	All Five	2/CCCII	2	2
11	LP, HP, BP	LP, HP, BP	LP, HP, BP	LP, HP, BP	5/MOCCCII	2	0
12	All Five	All Five	All Five	All Five	4/CFOA	2	9
13	Not Realized	All Five	Not Realized	All Five	3/MOCCII	2	5
14	All Five	All Five	All Five	All Five	3/DDCC	2	4
15	All Five	All Five	HP, BP	All Five	1/FDCCII	2	3
16	All Five	All Five	All Five	All Five	1/FDCCII, 1/DDCC	2	6
17	All Five	All Five	All Five	All Five	4/MOCCCII	2	0
Proposed	All Five	All Five	HP, BP	All Five	1/DXCCDITA	2	2

to realize AP response in all three modes. Moreover, excessive number of Input/output terminals are used in the design. In addition, the circuit cannot be constructed using the off the shelf popular ICs AD844 which is a slight disadvantage since every time it is not possible to fabricate the concept. The proposed filter on the other hand can be readily constructed using AD844 [33] and LM13700 [34] making it possible to test our design in hardware or employ the design in practical applications. Furthermore, the proposed mix mode filter realizes non-inverting responses in all four modes unlike [15]. The proposed filter is further compared with the state of the art recently published filter structures using single active elements to highlight the merits of the structure. The survey shows that majority of the single active element based implementations work in a single mode. The Table 2 presents the detailed comparison.

In this research the authors propose a mixed mode universal filter synthesized by single DXCCDITA [35]. The filter uses only two capacitors and two resistors. The second resistor is required only for obtaining TIM filter response. The filter can be termed as MISO since for a particular mode all the filter responses are obtained from a single node. By proper excitation with appropriate current or voltage signals the filter structure can perform in all four modes. The filter is capable of realizing all five standard filter responses in VM, CM and TIM modes. Additionally, in VM both inverting and non-inverting outputs are available simultaneously. In TAM mode the filter can realize HP and BP responses. The merits of the filter includes (i) it is the first reported MISO type mix mode filter using single active element (ii) no matching for VM, TAM, CM (HP, BP) and TIM (LP, BP) responses (iii) tunability of pole frequency via bias current (iv) use of minimum number of passive elements (v) availability of VM output at low impedance node (vi) availability of CM and TAM output at high impedance node (vii) low active and passive sensitivities (viii) provision for independent control of frequency and bandwidth (ix) provision for gain tuning in TIM mode. The simulations in 0.35µm technology parameters obtained from TSMC are conducted to test the performance of the filter. The DXCCDITA utilized in the filter design is also constructed using ICs AD844 and LM13700 to further validate the filter design.

2 Dual X current conveyor differential Input transconductance amplifier (DXCCDITA)

The proposed Dual X current conveyor differential Input transconductance amplifier (DXCCDITA) [35] is functionally a connection of DXCCII and OTA. The new block carries features of CCII, ICCII and tunable transconductor in one single architecture which is also simple to implement as an integrated circuit. The Voltage current characteristics of the developed DXCCDITA are given in matrix Equation 1 and the block diagram is presented in Fig. 1.

Table 2: Comparison of the proposed filter with state of art MISO filter topologies available in the literature

Reference	Type of Active Block	Filter responses realized	Number of Capacitors/ Resistors Used	Matching Condition	Number/Type of Filtering Modes realized	Whether Tunable	Is output available from a single Node
18	CCII	LP, HP, BP, NP ,AP	2C/3R	Yes	1/VM	No	No
19 Fig. 16	DVCCII	LP, BP	2C/3R	No	1/VM	No	Yes
20 Fig. 4	FDCCII	LP, HP, BP, NP ,AP	2C/2R	No	1/VM	No	Yes
21 Fig. 8	DDCCTA	LP, HP, BP, NP ,AP	2C/1R	No	1/CM	Yes	No
22	VDIBA	LP, HP, BP, NP ,AP	2C/1R	No	1/VM	Yes	No
23	VDTA	LP, HP, BP, NP ,AP	2C/1R	No	1/VM	Yes	Ye
24	VDTA	LP, HP, BP, NP ,AP	2C/1R	No	1/VM	Yes	Yes
25	VD-DIBA	LP, HP, BP, NP ,AP	2C/1R	No	1/VM	Yes	Yes
26	CDBA	LP, HP, BP, NP ,AP	4C/4R	Yes	1/VM	No	Yes
27	CFOA	LP, HP, BP, NP ,AP	2C/3R	Yes	1/VM	No	Yes
28	CDTA	LP, HP, BP, NP, AP	2C/3R	Yes	1/CM	Yes	Yes
29	CFOA	LP, HP, BP, NP ,AP	2C/3R	Yes	1/VM	No	Yes
30	CDBA	LP, HP, BP, NP, AP	2C/5R	Yes	1/VM	No	Yes
31	CCII	LP, HP, BP, NP, AP	2C/2R	Yes	2/VM, CM	No	No
32 Fig. 2	FDCCII	LP, HP, BP, NP ,AP	2C/2R	No	1/CM	No	No
Proposed	DXCCDITA	LP, HP, BP, NP, AP (only HP, BP in TAM)	2C/2R	No (Only CM Mode)	4/CM, VM,TIM,TAM	Yes	Yes

$$\begin{bmatrix} I_Y \\ V_{XP} \\ V_{XN} \\ I_{ZP1} \\ I_{ZP2} \\ I_{ZN1} \\ I_{ZN2} \\ I_{0+} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & g_m & 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{XP} \\ I_{XN} \\ V_{ZP1} \\ V_{ZP2} \\ V_{ZN1} \\ V_{ZN2} \\ V_O \end{bmatrix} \quad (1)$$

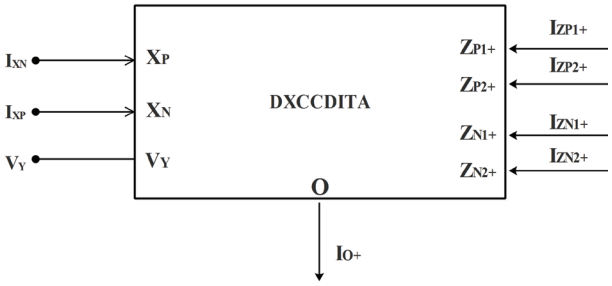


Figure1: Block diagram of DXCCDITA

The CMOS implementation of DXCCDITA is presented in Fig.2. It is a eight terminal active element. The first stage consists of DXCCII transistors (M1-M24). The voltage at Y appears at V_{XP} and in inverted form at V_{XN}. The current input at V_p node is transferred to nodes Z_{P1} and Z_{P2}. In the same way the input current from X_N node is transferred to Z_{N1} *and* Z_{N2}. The second stage is composed of OTA transistors. The transconductance is realized using transistors (M25-M34).The output current of the trans-conductor depends on the voltage difference between voltages at terminals Z_{P1} and Z_{N1}. Assuming saturation region operation for all transistors and equal W/L ratio for transistors M25 and M26 the output current I_o of the OTA is given by Equation 2.

$$I_O = g_{mi}\left(V_{ZP1} - V_{ZN1}\right) = \left(\sqrt{2I_{Bias}K_i}\right)\left(V_{ZP1} - V_{ZN1}\right) \quad (2)$$

Where, the transconductance parameter $K_i = \mu C_{ox} W/2L$, (i=25, 26) W is the effective channel width, L is the effective length of the channel, C_{ox} is the gate oxide capacitance per unit area andμ is the carrier mobility. It is evident from (2) that the transconductance can be tuned by the bias current thus imparting tunability to the structure.

3 The Proposed Single Active Element Mixed Mode Filter

The proposed mix mode universal filter is presented in Fig. 3. The filter utilizes two resistors and two capacitors. The second resistor R_2 is only needed to obtain TIM response. The VM, CM and TAM responses can be obtained using only three passive elements. The filter can realize all five generic filter responses in VM, CM, TIM while it can realize HP, BP functions in TAM mode of operation.

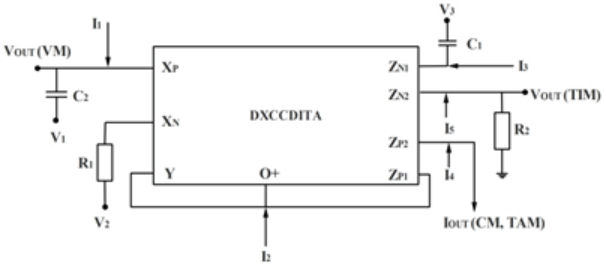


Figure 3: Mix Mode filter topology

3.1 Voltage Mode Operation

In voltage mode operation the input currents I_1 to I_5 are set to zero. The filter transfer function is given in Equation 3. The filter is capable of realizing all five standard filter functions. The input excitation sequence is given

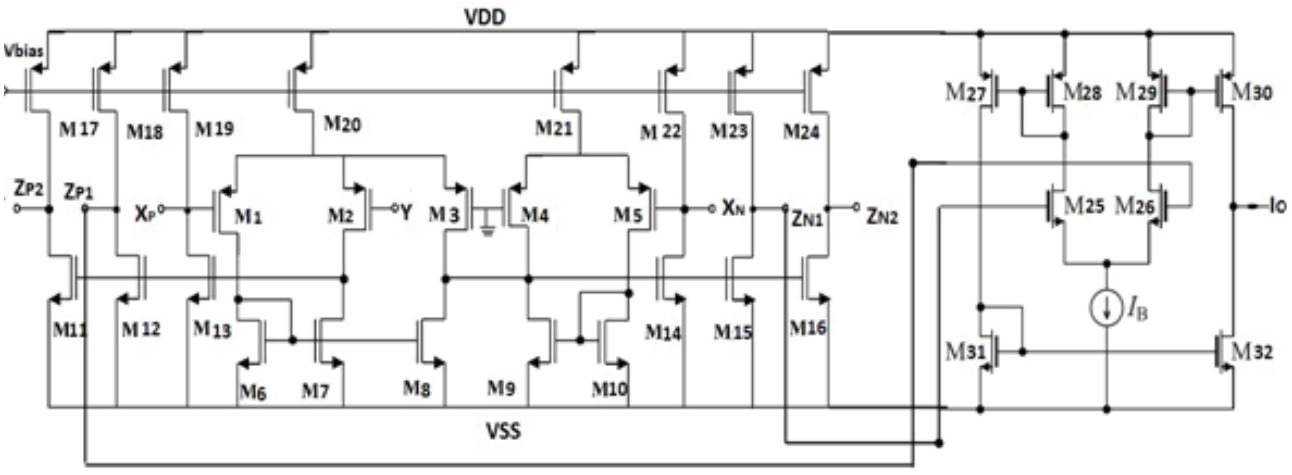


Figure 2: CMOS Implementation of DXCCDITA

in Table 3. The output of the filter is available at low impedance X_P terminal. It is worth emphasizing that by tapping the output from X_N node inverting VM response can also be obtained simultaneously which is an added advantage of the filter. In addition, in VM LP response both the capacitors are grounded which is again an advantage.

$$V_{Out(VM)} = \frac{V_1 S^2 C_1 C_2 \, R_1/g_m - V_2 + V_3 S C_1 R_1}{S^2 C_1 C_2 \, R_1/g_m + S C_1 R_1 + 1} \quad (3)$$

Table 3: Input Excitation sequence for VM realization

V_{Out} (VM)	V_1	V_2	V_3	Matching Required
LP	0	-1	0	No
HP	1	0	0	No
BP	0	0	1	No
NP	1	-1	0	No
AP	1	-1	-1	No

3.2 Current Mode Operation

In current mode the voltages V_1 to V_3 are set to zero. Hence all the passive elements are grounded. The input currents are applied as shown in Fig. 3. It is to be noted that input current I_5 and resistance R_2 are not needed for CM operation so only four current inputs are necessary to achieve five standard filter responses. The transfer function is presented in Equation 4 and filter excitation sequence is given in Table 5. All the outputs are available at high impedance Z_{P2} node which is good for cascadability.

3.3 Trans-Impedance Mode Operation

In TIM mode the voltages V_1 to V_3 are set to zero grounding all the passive elements. In TIM mode an extra resistor is needed to obtain the output. In this mode input current I_4 is not required. To realize HP and NP responses a matching condition of $R_1 = 1/g_M$ is required which can be easily set by fixing R_1 and changing the bias current of the trans-conductor. The analysis of the filter leads to the transfer function as given in Equation 5. The excitation sequence of the filter is given in Table 5. The gain of the filter can be varied by changing the value of R_2 which is an advantage.

Table 4: Input Excitation sequence for CM realization

I_{Out}	I_1	I_2	I_3	I_4	Matching Required
LP	-1	0	-1	0	$C_1=C_2$
HP	0	-1	0	0	No
BP	0	0	1	0	No
NP	0	0	-1	1	$C_1=C_2$
AP	0	0	-2	1	$C_1=C_2$

Table 5: Input Excitation sequence for TIM realization

V_{Out}(TIM)	I_1	I_2	I_3	I_5	Matching Required
LP	0	0	-1	0	No
HP	1	0	1	1	$R_1=1/g_M$
BP	1	0	0	0	No
NP	1	0	0	1	$R_1=1/g_M$
AP	1	-1	0	1	$R_1=R_2=1/g_M$
AP (alternative option to make filter gain tunable)	2	0	0	1	$R_1=1/g_M$

3.4 Trans-Admittance Mode Operation

In TAM operation the filter transfer function is given in Equation 6. The filter can only realize HP and BP functions. The excitation table is given in Table 6. The output of the filter is available at high impedance Z_{P2} node.

$$I_{Out(TAM)} = \frac{-V_1\left(S^2 C_1 C_2 R_1 + SC_2\right) - V_2\left(SC_2\right) + V_3\left(S^2 C_1 C_2 R_1\right)}{S^2 C_1 C_2 \, R_1/g_M + SC_1 R_1 + 1} \quad (6)$$

I_{Out}(TAM)	V_1	V_2	V_3	Matching Required
HP	0	0	1	No
BP	0	-1	0	No

$$I_{Out(CM)} = \frac{I_4(S^2 C_1 C_2 \, R_1/g_M + SC_1 R_1 + 1) - I_1\left(SC_1 R_1 + 1\right) - I_2(S^2 C_1 C_2 \, R_1/g_M) + I_3(SC_2 R_1)}{S^2 C_1 C_2 \, R_1/g_M + SC_1 R_1 + 1} \quad (4)$$

$$V_{Out(TIM)} = \frac{I_5(S^2 C_1 C_2 \, R_1 R_2/g_M + SC_1 R_1 R_2 + R_2) - I_1\left(SC_1 R_2/g_M\right) + I_2\left(SC_1 R_1/g_M\right) - I_3(R_2)}{S^2 C_1 C_2 \, R_1/g_M + SC_1 R_1 + 1} \quad (5)$$

The expression for pole frequency, quality factor and bandwidth for all four modes are given in Equations 7-9. It can be inferred by examining the equations that if R_1 or $R_M(1/g_M)$ is varied but their ratio is kept constant then frequency can be varied independent of the quality factor. This can be easily achieved by changing R_1 and adjusting the bias current of transconductance amplifier. The frequency and bandwidth also enjoy non interactive tuning capability through R_1 and R_M.

$$\omega_P = \sqrt{\frac{1}{C_1 C_2 R_1 R_M}} \tag{7}$$

$$Q = \sqrt{\frac{R_M C_2}{C_1 R_1}} \tag{8}$$

$$BW = {}^{1}\!\!\diagup\!\!{}_{R_M C_2} \tag{9}$$

where $R_M = 1/g_M$ is the transconductance of the transconductance amplifier.

The property of tunability allows changing the pole frequency of the filter without changing the passive components and it is also advantageous for cancelling out the variations in the pole frequency caused due to slight change in capacitance values during fabrication. The tuning can be achieved by changing the bias current of the OTA, any variation in the pole frequency introduced due to random variations in capacitance and device parasitics can be easily nullified. Moreover, the two resistors can be designed using the MOS transistors [36-37] this will impart dual tunability to the filter structure hence by properly tuning the control voltage of the MOS resistors and the bias current of the transconductance amplifier changes in the capacitance values can be easily accommodated.

4 Non-Ideal Analysis

In this section the Non-idealities of the DXCCDITA are considered and their influence on the proposed mix mode filter circuit is analyzed. A simplified non-ideal model of DXCCDITA is presented in Fig. 5 for analysis. The most important aspects contributing to the deviations in frequency performance are the non-ideal frequency dependent current and voltage transfer gains $a_i(s)$ and $b_i(s)$, where $a_i(s) = a_{0i}/(1 + s/w_{ai})$ and $b_i(s) = b_{0i}/(1 + s/w_{bi})$. Ideally, $a_i = b_{0i} = 1$ and $w_{ai} = w_{\beta i} = \infty$. Another

$$\begin{bmatrix} I_Y \\ V_{XP} \\ V_{XN} \\ I_{ZP1} \\ I_{ZP2} \\ I_{ZN1} \\ I_{ZN2} \\ I_{0+} \end{bmatrix} = \begin{bmatrix} (sC_Y + \frac{1}{R_Y}) & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \beta_P(s) & Z_{XP} & 0 & 0 & 0 & 0 & 0 & 0 \\ -\beta_N(s) & 0 & Z_{XN} & 0 & 0 & 0 & 0 & 0 \\ 0 & \alpha_P(s) & 0 & (sC_{ZP1} + \frac{1}{R_{ZP1}}) & 0 & 0 & 0 & 0 \\ 0 & \alpha_P(s) & 0 & 0 & (sC_{ZP2} + \frac{1}{R_{ZP2}}) & 0 & 0 & 0 \\ 0 & 0 & \alpha_N(s) & 0 & 0 & (sC_{ZN1} + \frac{1}{R_{ZN1}}) & 0 & 0 \\ 0 & 0 & \alpha_N(s) & 0 & 0 & 0 & (sC_{ZN2} + \frac{1}{R_{ZN2}}) & 0 \\ 0 & 0 & 0 & \gamma g_m & 0 & -\gamma g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{XP} \\ I_{XN} \\ V_{ZP1} \\ V_{ZP2} \\ V_{ZN1} \\ V_{ZN2} \\ V_O \end{bmatrix} \tag{10}$$

$$V_{Out(VM)} = \frac{\alpha_P V_1 S^2 A - \alpha_N V_2 + V_3 SB}{\alpha_P \beta_P S^2 A + SB + \alpha_N \beta_N} \tag{11}$$

Where, $A = C_1 C_2 R_1 / g_m$, $B = C_1 R_1$

$$I_{Out(CM)} = \frac{I_4(\alpha_P \beta_P S^2 A + SB + \alpha_N \beta_N) - I_1 \alpha_P \left(\alpha_P \beta_P S^2 A + BS + \alpha_N \beta_N\right) + I_1(\alpha_P \beta_P S^2 A) - I_2 \beta_P (S^2 A) + I_3 \beta_P (SC_2 R_1)}{\alpha_P \beta_P S^2 A + BS + \alpha_N \beta_N} \tag{12}$$

$$V_{Out(TIM)} = \frac{I_5(\alpha_P \beta_P S^2 R_2 A + SBR_2 + \alpha_N \beta_N R_2) - I_1 \alpha_P \alpha_N \beta_N \left({}^{SC_1 R_2}\!\!\diagup\!\!{}_{g_m}\right) + I_2 \alpha_N \beta_N \left({}^{SB}\!\!\diagup\!\!{}_{g_m}\right) + I_3 \alpha_N \beta_N (R_2)}{\alpha_P \beta_P S^2 A + BS + \alpha_N \beta_N} \tag{13}$$

$$I_{Out(TAM)} = \frac{V_1 \left(\alpha_P \beta_P S^3 C_1 C_2 {}^{R_1}\!\!\diagup\!\!{}_{g_m}\right) - V_2 \left(\alpha_N \beta_P S C_2\right) - \alpha_P S C_2 V_1 + V_3 \beta_N \left(S^2 C_1 C_2 R_1\right)}{\alpha_P \beta_P S^2 A + BS + \alpha_N \beta_N} \tag{14}$$

important performance parameter is the associated parasitics at the X nodes which can be quantified as $Z_{XP} = Z_{XN} = R_{X(N,P)} + sL_{X(N,P)}$. The parasitic resistances and capacitance associated with the Y and Z nodes are R_{ZP}, R_{ZN} and R_Y, while the associated capacitances are C_{ZP}, C_{ZN} and C_Y. There ideal values are equal to zero. γ represents the transconductance transfer inaccuracy of the OTA while R_o and C_o are parasitics at the OTA output. The modified V-I relations of DXCCDITA including the non-ideal gains and parasitic elements are given in Equation 10. Considering only the effect of the non-ideal gains the transfer functions, pole frequency and quality factor of the above filter will be modified as presented in Equations 11-16.

$$\omega_P = \sqrt{\frac{\alpha_N \beta_N}{C_1 C_2 R_1 R_M \alpha_P \beta_P}} \tag{15}$$

$$Q = \sqrt{\frac{R_M C_2 \alpha_N \beta_N \alpha_P \beta_P}{C_1 R_1}} \tag{16}$$

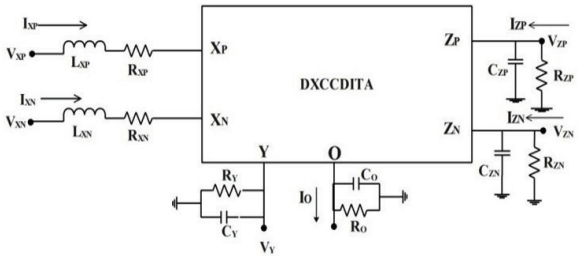


Figure 4: Non-Ideal model of DXCCDITA

The sensitivity analysis of the filter is also carried out to get a measure of active and passive sensitivities of the filter. It can be deduced from the analysis that the filter has low sensitivities.

$$-S_{R1}^{\omega} = -S_{C2}^{\omega} = -S_{C1}^{\omega} = S_{gm}^{\omega} = \frac{1}{2}$$

$$-S_{R1}^{Q} = S_{C2}^{Q} = -S_{C1}^{Q} = -S_{gm}^{Q} = \frac{1}{2}$$

$$-S_{\alpha P}^{\omega} = -S_{\beta P}^{\omega} = -S_{R1}^{\omega} = -S_{C2}^{\omega} = -S_{C1}^{\omega} = S_{\alpha N}^{\omega} = S_{\beta N}^{\omega} = S_{gm}^{\omega} = \frac{1}{2}$$

$$S_{\alpha P}^{Q} = S_{\beta P}^{Q} = -S_{R1}^{Q} = S_{C2}^{Q} = -S_{C1}^{Q} = S_{\alpha N}^{Q} = S_{\beta N}^{Q} = -S_{gm}^{Q} = \frac{1}{2}$$

5 Simulation results

In order to establish the performance of the proposed dual X current conveyor differential input transconductance amplifier (DXCCDITA) it was designed in 0.35 µm parameters from TSMC. The circuit was simulated in SPICE to measure the important design metrics. The aspect ratios of the transistors are given in Table 7. The supply voltages are kept at $V_{DD} = -V_{SS} = 1.5V$. The bias voltage was fixed at $V_{bias} = 0.55V$. The bias current of OTA was set to 50 µA which resulted in a transconductance of $g_m = 0.1$ mS. The proposed active element is characterized using the method stated in [38]. The performance parameters of the active block are summarised in Table 8.

Table 7: Aspect Ratios of the Transistors

Transistor	Width (W µm)	Length (L µm)
M1- M2	1.4	0.7
M3- M5	2.8	0.7
M6- M7	2.4	0.7
M8- M10	4.8	0.7
M11-M24	9.6	0.7
M25-M32	2	1

Table 8: Performance Parameters of the Proposed DXCCDITA

Voltage Gain (V_{XP}/V_Y)	0.98
Voltage Gain (V_{XN}/V_Y)	0.95
Current Gain (I_{ZP}/I_{XP})	1.05
Current Gain (I_{ZN}/I_{XN})	1.05
DC Voltage transfer range	±400mV
DC Current Transfer range (I_{ZP})	±60µA
DC Current Transfer range (I_{ZN})	±60µA
Voltage Transfer B.W. (V_{XP}/V_Y)	632MHz
Voltage Transfer B.W. (V_{XN}/V_Y)	728MHz
Current Transfer B.W. (I_{ZP}/I_{XP})	932MHz
Current Transfer B.W. (I_{ZN}/I_{XN})	1.32GHz
Parasitic Resistance at X_P node R_{XP}	71.1Ω
Parasitic Resistance at X_N node R_{XN}	38.2 Ω
Resistance at Z_N node R_{ZN}	305K Ω
Resistance at Z_P node R_{ZP}	305 K Ω
Resistance at O node Z_0	1.05M Ω

The operation of the filter in voltage mode is analyzed first. The filter is designed for unit quality factor (Q=1) and pole frequency of 318.30KHz by selecting the passive components values as R_1 =10KΩ, C_1 = 50pF, C_2 = 50pF the bias current is set at I_{bias} = 50µA. The filter responses are given in Fig. 5-6. Next, the tunability of the filter is examined by varying the bias current and observing the BP response. It can be inferred from the Fig. 7 that the filter is perfectly tunable. The total harmonic distortion (THD) of the filter is evaluated and plotted for different signal amplitudes as shown in Fig. 8. It can be seen that THD is within acceptable limit for wide range of voltage signal amplitudes. To study the effect of process variability on the filter performance Monte

Carlo analysis, assuming Gaussian distribution, for 10% deviation in capacitor values (C_1&C_2) is conducted for 100 runs as shown in Fig. 9. It can be deduced from the figure that there is only slight deviation from the expected value which can be easily nullified by adjusting the bias current of the filter as discussed in the preceding section.

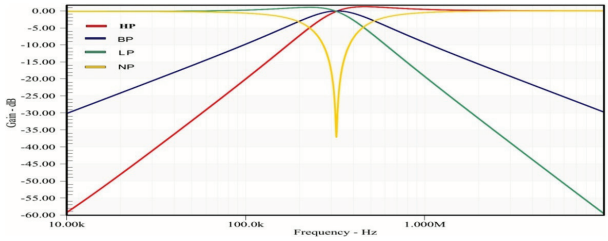


Figure 5: VM filter responses

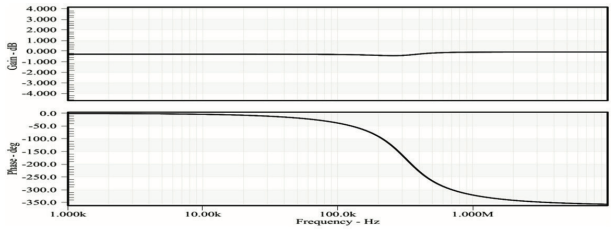


Figure 6: VM All Pass filter gain and phase response

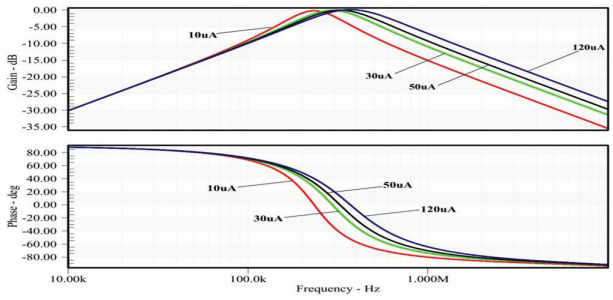


Figure 7: Band pass response of VM filter for different bias currents

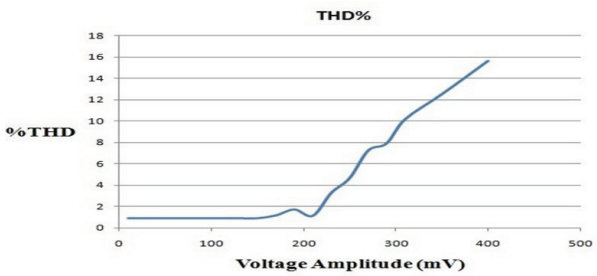


Figure 8: Total Harmonic Distortion of filter in voltage mode operation for BP response

The current mode filter is now designed for a pole frequency of 318.30 KHz by selecting R_1 = 10KΩ, C_1 = 50pF, C_2 = 50pF the bias current is set at I_{bias} = 50µA.

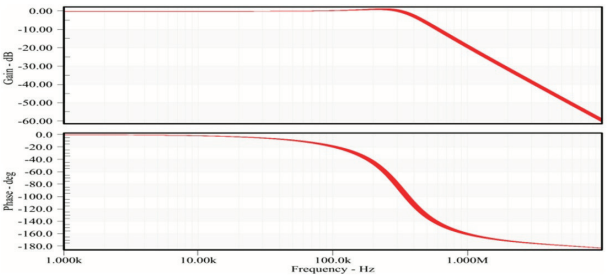


Figure 9: Monte Carlo analysis of the low pass response for 10% variation in capacitance value

The response of the filter is given in Fig. 10-11. The total harmonic distortion (THD) of the filter is evaluated and plotted for different signal amplitudes as shown in Fig. 12. It can be seen that THD is less than 1.5% for wide range of signal amplitudes.

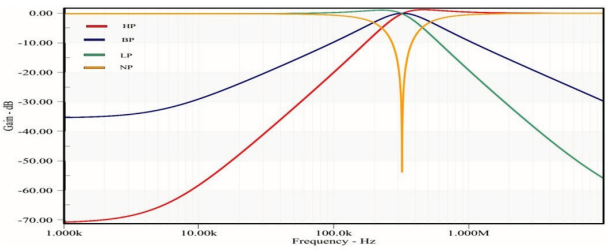


Figure 10: CM filter responses

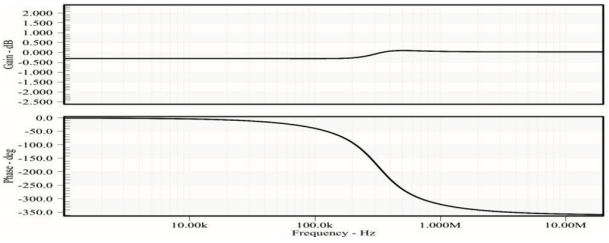


Figure 11: CM All Pass filter gain and phase response

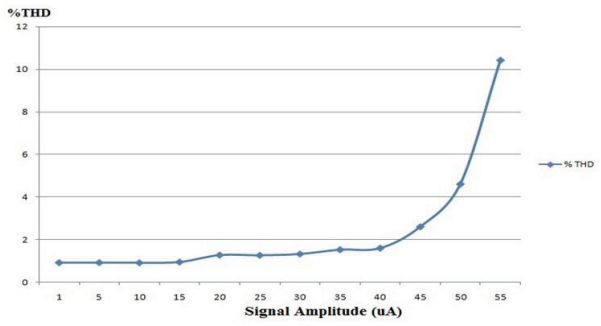


Figure 12: Total Harmonic Distortion of filter in current mode operation for BP response

Now the TIM response is analysed. The passive elements are fixed at R_1=R_2=10KΩ, C_1 = 50pF, C_2 = 50pF. The bias current is selected as I_{bias} = 50µA(g_M = 0.1ms)

to satisfy the condition of $R_1 = 1/g_M$. The resulting pole frequency is 318.30 KHz. The responses of the filter are shown in Fig. 13-14.

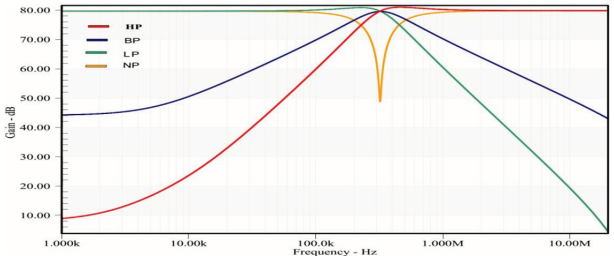


Figure 13: TIM filter responses

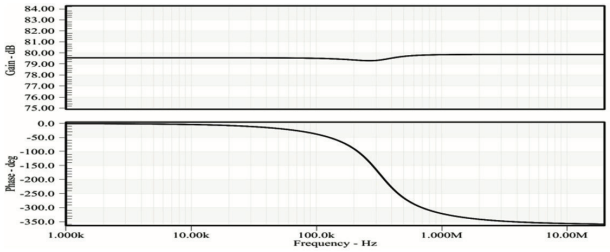


Figure 14: CM All Pass filter gain and phase response

To further validate the performance of the proposed topology. The DXCCDITA is constructed using the commercially available ICs AD844 and LM13700. The possible implementation of DXCCDITA is given in Fig. 15.

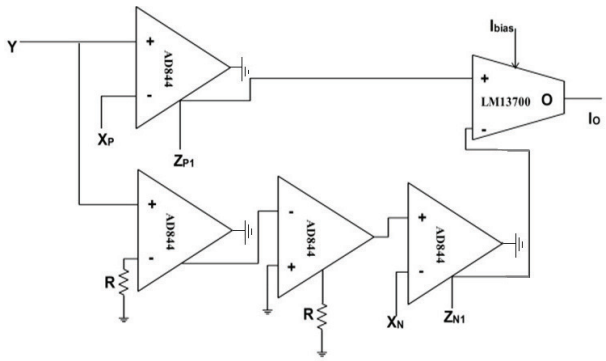
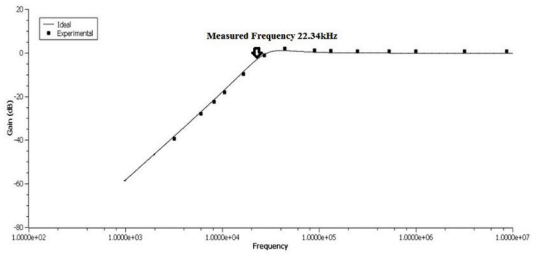


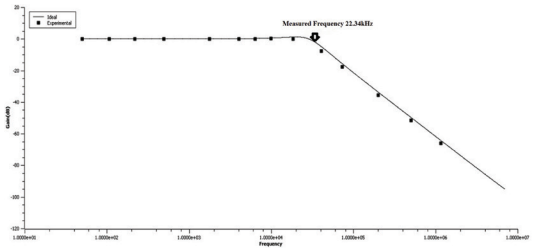
Figure 15: Implementation of the DXCCDITA from the commercially available ICs

The hardware implemented DXCCDITA is then used to measure the VM filter responses. The Agilent technologies MSO-X 3024A oscilloscope, IDL-800 digital lab prototype board, and Agilent technologies function generator were used in the test setup. The passive components values selected were $C_1 = 560pF$, $C_2 = 560pF$, $R_1 = 10K\Omega$. The supply voltage are kept at $V_{DD} = -V_{SS} = 5V$. The theoretical pole frequency of the filter is found to be 28.420 KHz. The ideal and measured filter responses are given in Fig. 16 (a-d). The all pass response is given in Fig. 17 (a-b).

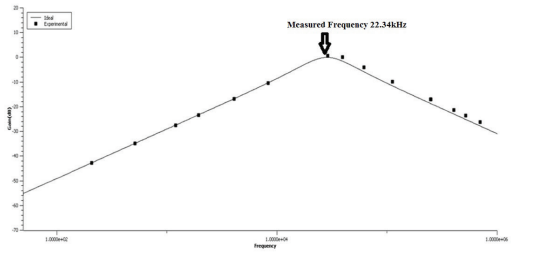
a)



b)



c)



d)

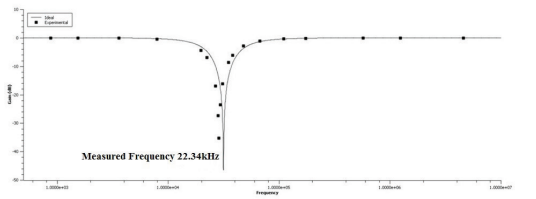
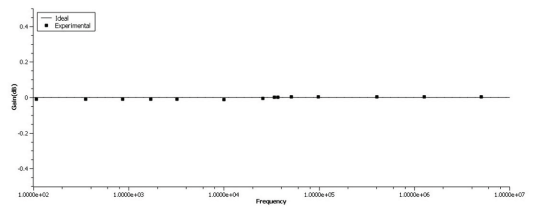


Figure 16: The VM filter responses constructed using the AD844 and LM13700 ICs

a)



b)

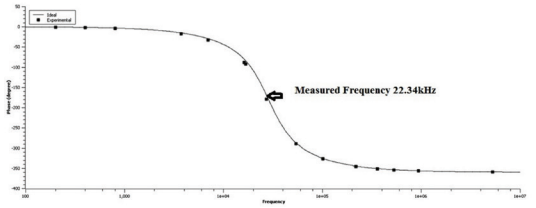


Figure 17: The VM filter all pass response constructed using the AD844 and LM13700 ICs (a)Gain (b) Phase

6 Conclusion

A novel minimum component MISO type mix mode universal filter is presented. The filter is designed using a single DXCCDITA as active element. To the best knowledge of the authors the reported filter is the first MISO type mix mode single active element based implementation capable of working in all four modes. The filter can realize all five standard responses in voltage mode, current mode and trans-impedance modes. The filter gives HP and BP responses in trans-admittance mode. No components matching condition are required in any mode except for trans-impedance mode (LP, NP, AP) and current mode (LP, NP, AP) responses. The filter offers low impedance voltage mode output and high impedance current and trans-admittance mode output leading to cascadability. The pole frequency, quality factor and bandwidth of the filter are tunable. There is a provision for gain adjustment of the filter in trans-impedance mode as well. The filter also enjoys low active and passive sensitivities. The experimental results are also given to validate the theory.

7 Acknowledgement

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8 Reference

1. J.-W. Horng, "High-input impedance voltage-mode universal biquadratic filter using three plus-type CCIIs," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, pp. 996-997, 2001.
2. M. Faseehuddin, J. Sampe, S. Islam, "Schmitt Trigger based on Dual Output Current Controlled Current Conveyor in 16nm CMOS technology for digital applications", In IEEE International Conference on Semiconductor Electronics (ICSE), pp. 82-85, 2016.
3. R. Senani, D. Bhaskar, A. Singh, "Current conveyors: variants, applications and hardware implementations", *Springer*, 2014.
4. J. Sampe, F. F. Zulkifli, N. A. A. Semsudin, M. S. Islam, and B. Y. Majlis, "Ultra low power hybrid micro energy harvester using rf, thermal and vibration for biomedical devices," *International Journal of Pharmacy and Pharmaceutical Sciences*, vol. 8, pp. 18-21, 2016.
5. M. T. Abuelma'atti, "A novel mixed-mode current-controlled current-conveyor-based filter," *Active and passive electronic components*, vol. 26, pp. 185-191, 2003.
6. M. T. Abuelma'atti, A. Bentrcia, and S. a. M. Al-Shahrani, "A novel mixed-mode current-conveyor-based filter," *International Journal of Electronics*, vol. 91, pp. 191-197, 2004.
7. S. Maheshwari, S. V. Singh, and D. S. Chauhan, "Electronically tunable low-voltage mixed-mode universal biquad filter," *IET circuits, devices & systems*, vol. 5, pp. 149-158, 2011.
8. J.-W. Horng, "High-order current-mode and transimpedance-mode universal filters with multiple-inputs and two-outputs using MOCCIIs," *Radioengineering*, vol. 18, pp. 537-543, 2009.
9. M. Siripruchyanun, W. Jaikla, "Three-input single-output electronically controllable dual-mode universal biquad filter using DO-CCCIIs," *Active and Passive Electronic Components*, vol. 2007, 2007.
10. N. Pandey, S. K. Paul, A. Bhattacharyya, and S. Jain, "Realization of Generalized Mixed Mode Universal Filter Using CCCIIs," *Journal of Active and Passive Electronic Devices*, vol. 55, pp. 279-293, 2009.
11. L. Zhijun, "Mixed-mode universal filter using MCCCII," *AEU-International Journal of Electronics and Communications*, vol. 63, pp. 1072-1075, 2009.
12. V. Singh, A. K. Singh, D. R. Bhaskar, and R. Senani, "Novel mixed-mode universal biquad configuration," *IEICE Electronics Express*, vol. 2, pp. 548-553, 2005.
13. J.-W. Horng, " Current-mode and transimpedance-mode universal biquadratic filter using multiple outputs CCIIs," *Indian Journal of Engineering & Materials Sciences*, vol. 17, pp. 169-174, 2010.
14. W. B. Liao, J. C. Gu, "SIMO type universal mixed-mode biquadratic filter", *Indian Journal of Engineering and Materials Sciences*, vol. 18, no. 6, pp. 443-448, 2011.
15. C. N. Lee, C. M. Chang, "Single FDCCII-based mixed-mode biquad filter with eight outputs", *AEU-International Journal of Electronics and Communications*, vol. 63, no. 9, pp. 736-742, 2009.
16. C. N. Lee, "Independently tunable mixed-mode universal biquad filter with versatile input/output functions", *AEU-International Journal of Electronics and Communications*, vol. 70, no. 8, pp. 1006-1019, 2016.
17. N. Pandey, S. K. Paul, "Mixed mode universal filter", *Journal of Circuits, Systems and Computers*, vol. 22, no. 1, pp. 1250064(1-10).
18. H. P. Chen, "Single CCII-based voltage-mode universal filter", *Analog Integrated Circuits and Signal Processing*, vol. 62, no. 2, pp. 259-262, 2010.
19. T. M. Hassan, S. A. Mahmoud, "New CMOS DVCC realization and applications to instrumentation amplifier and active-RC filters", *AEU-International*

Journal of Electronics and Communications, vol. 64, no. 1, pp. 47-55, 2010.
20. F. Kaçar, A. Yeşil, "Voltage mode universal filters employing single FDCCII". *Analog Integrated Circuits and Signal Processing*, vol. 63, no. 1, pp. 137-142, 2010.
21. N. Pandey, S. K. Paul, "Differential difference current conveyor transconductance amplifier: a new analog building block for signal processing", *Journal of Electrical and Computer Engineering*, 2011, vol. 17, 2011.
22. K. L. Pushkar, D. R. Bhaskar, D. Prasad, "Voltage-mode new universal biquad filter configuration using a single VDIBA", *Circuits, Systems, and Signal Processing*, vol. 33, no. 1, pp. 275-285, 2014.
23. D. Prasad, D. R. Bhaskar, M. Srivastava, "Universal voltage-mode biquad filter using voltage differencing transconductance amplifier", *Indian Journal of Pure & Applied Physics (IJPAP)*, vol. 51, no. 12, pp. 864-868.
24. W. Mekhum, W. Jaikla, "Three input single output voltage-mode multifunction filter with independent control of pole frequency and quality factor", *Advances in Electrical and Electronic Engineering*, vol. 11, no. 6, pp. 494, 2014.
25. K. L. Pushkar, D. R. Bhaskar, D. Prasad, "A new MISO-type voltage-mode universal biquad using single VD-DIBA", *ISRN Electronics*, 2013.
26. 27. A. Ü. Keskin, "Multi-function biquad using single CDBA", *Electrical Engineering*, vol. 88, no. 5, pp. 353-356, 2013.
28. J. W. Horng, C. K. Chang, C. H. U. Jie-Mei, "Voltage-mode universal biquadratic filter using single current-feedback amplifier", *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. 85, no. 8, pp. 1970-1973, 2012.
29. D. Prasad, D. R. Bhaskar, A. K. Singh, "Multi-function biquad using single current differencing transconductance amplifier", *Analog Integrated Circuits and Signal Processing*, vol. 61, no. 3, pp. 309-313, 2009.
30. R. K. Sharma, R. Senani, "Universal current mode biquad using a single CFOA", *International Journal of Electronics*, vol. 91, no. 3, pp. 175-183, 2004.
31. S. A. Bashir, N. A. Shah, "Voltage Mode Universal Filter Using Current Differencing Buffered Amplifier as an Active Device", *Circuits and Systems*, vol. 3, no. 3, pp. 278-281, 2012.
32. J. W. Horng, " Voltage/current-mode universal biquadratic filter using single CCII+", *Indian Journal of Pure & Applied Physics*, vol. 48, pp. 749-756, 2010.
33. C. M. Chang, B. M. Al-Hashimi, C. L.Wang, C. W. Hung, "Single fully differential current conveyor biquad filters", *IEE Proceedings-Circuits, Devices and Systems*, vol. 150, no. 5, pp. 394-398, 2003.
34. Analog Devices,"AD844, Datasheet, MHz 2000V/µs Monolithic Op Amp, Analog Devices, Rev." 2009.
35. N. Semiconductor, "LM13700 dual operational transconductance amplifiers with linearizing diodes and buffers", 2000.
36. F. Mohammad, J. Sampe, S. Shireen, S. H. M Ali, "Minimum passive components based lossy and lossless inductor simulators employing a new active block". *International Journal of Electronics and Communications (AEU)*, vol. 82, pp. 226-240, 2017.
37. Z. Wang, "Novel electronically-controlled floating resistors using MOS transistors operating in saturation". *Electronics letters*, vol. *27 no.* 2, pp. 188-189, 1991.
38. B. Metin, N. Herencsar, J. Koton, J. W. Horng, "DCCII-based novel lossless grounded inductance simulators with no element matching constrains". *Radioeng J*, vol. *23*, pp. 532-4538, 2014.
39. A. Fabre, O. Saaid, H. Barthelemy, "On the frequency limitations of the circuits based on second generation current conveyors", *Analog Integrated Circuits and Signal Processing*, vol. 7, no. 2, pp.113-129, 1995.

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Synthesizable 2D Vernier TDC based on gated ring oscillators

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Abstract: Time to digital converter (TDC) is a device, which measures time interval between two edges of signals and converts it to digital code. Lately it is used as phase detector in all-digital frequency synthesizers. One of main parameters of TDC is resolution, which describes smallest time interval, which can be measured using TDC. Resolution of basic inverter-based TDC improves with reduction of delay of inverter in modern nanometric CMOS technology nodes. But in more mature technologies delay of inverter does not provide needed TDC resolution. In this paper sub-inverter-resolution 2D Vernier TDC, which is based on gated ring oscillators and is implemented in VHDL hardware description language for easy migration to various technology nodes, is presented. It is synthesized, placed and routed in 65 nm CMOS technology. Main blocks of TDC are two gated ring oscillators, their lap and edge counters, arbiter matrix, output decoder and control block. Frequency and single stage delay of gated ring oscillators is changed by switching parallel-connected sections of three-stage oscillators. Tuning step of single stage delay of gated ring oscillator, which is equal to the resolution of TDC, can be changed from 3.2 to 0.8 ps at typical operation conditions, when number of enabled stages of oscillator is changed from 22 to 48. TDC occupies 123,0 μm × 148,8 μm area of silicon.

Keywords: CMOS; integrated circuit; time to digital converter; Vernier; gated ring oscillator

Sestavljivi 2D Vernier TDC na osnovi obročnih oscilatorjev

Izvleček: Časovno digitalni pretvorniki (TDC) so naprave, ki merijo časovni interval med dvema roboma signal in ga pretvorijo v digitalno obliko. Pretvornik je uporabljen kot fazni detektor v digitalnih frekvenčnih sintetizatorjih. Glavni parameter TDC je resolucija, ki je opisana kot najmanjši časovni interval, ki ga še lahko izmeri. Resolucija osnovnih invertirajočih TDC se izboljša z znižanjem zakasnitev inverterja v moderni nanometrski CMOS tehnologiji. Pri zrelih tehnologijah zakasnitev ne omogoča doseganja željene resolucije TDC. V članku je predstavljen 2D Vernier TDC na osnovi obročnega oscilatorja s podinvertersko resolucijo. Zaradi lažje migracije v različne tehnologije je realiziran v VHDL strojnem jeziku. Sestavljen je v 65 nm CMOS tehnologiji. Glavni bloki TDC so: dva krožna oscilatorja na osnovi vrat, njihov krog, robni števci, arbitna matrika, izhodni dekoder in kontrolni blok. Frekvenčne in enostanjske zakasnitve se spreminjajo s preklapljanjem vzporedno vezanih sekcij tristanjskega oscilatorja. Korak je nastavljiv od 3.2 do 0.8 ps pri tipičnem delovanju in predstavlja resolucijo TDC. Velikost TDCja je 123,0 μm × 148,8 μm.

Ključne besede: CMOS; integrirana vezja; časovno digitalen pretvornik; Vernier; obročni oscilator

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1 Introduction

Time to digital converter (TDC) is electronic device which converts time interval between edges of two signals into digital code. It is often used as phase detector in all-digital phased locked loops, which are used as high frequency synthesizers. Such synthesizers are gaining popularity in recent years, since it becomes harder to implement conventional charge-pump synthesizers in modern nanometric integrated circuit (IC) technology nodes. Therefore, there is a lot of effort put into research and development of all-digital frequency synthesizers and their constituting blocks.

The output of TDC is digital, therefore due to quantization, which is related to resolution of TDC, it affects phase noise of whole synthesizer [1]. The most

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basic TDC is based on inverter delay line. In such TDC signal generated by digitally controlled oscillator (DCO) propagates through delay line and its value after each inverter is sampled by the edge of reference signal. At the output, there is a pseudo thermometric code, which shows how many inverters are between edges of reference and generated signals. The minimal time interval, which can be measured by this TDC, is equal to inverter delay.

Therefore, performance of this TDC increases and its quantization decreases in newer technology nodes as the delay of inverters decreases. Although in more mature technology nodes performance of such TDC decreases and consequently there is a need for TDC which can measure time intervals lower than inverter's delay. There are several structures of TDC with sub-inverter delay resolution, such as multi-stage TDC, Vernier family of TDC's (1 dimensional (1D), 2 dimensional (2D), 2D Gated Ring Vernier), stochastic TDC etc. [2]–[7]. Although these structures can achieve high resolution, their complexity is much higher compared to TDC based on inverter delay line. Also, often TDCs are manually designed and routed despite of digital nature of TDC, what defeats one of the advantages of all-digital frequency synthesizers – easy migration from one IC technology to another.

The aim of this work is to design time to digital converter, which has sub-inverter delay resolution, large input time range and can be easily implemented in various IC technology nodes. Proposed TDC is implemented using VHDL hardware description language and is fully synthesized in 65 nm CMOS technology. It employs 2D Vernier properties and as in 2D Gated Vernier TDC [6], its delay lines are replaced with gated ring oscillators. Also, compared to [6] different phase detection technique and structure of oscillator and its tuning method is used to make design synthesisable. Output decoding procedure and its issues in 2D Vernier architecture are also addressed in this paper.

2 Structure of TDC

The structure of proposed time to digital converter is presented in Fig. 1. Two main inputs for reference and DCO signals are respectively marked as F_{REF} and F_{DCO} and output is marked as TD_{COUT}. Main blocks of TDC are lower frequency gated ring oscillator (GRO_L), higher frequency gated ring oscillator (GRO_H), lap counter of lower frequency oscillator, edge counter of higher frequency oscillator, matrix of arbiters, control block and output decoder.

2.1 Gated ring oscillators and counters

Lower and higher frequency gated ring oscillators share same structure, which is shown in Fig. 2. They are composed of N parallel-connected three-stage gated ring oscillators, made of tristate inverters, similar as in [8]. Such inverters are available in most IC manufacturing technologies. Therefore, usage of these inverters does not prevent synthesis of oscillators. The frequency of an oscillator can be tuned by turning on different numbers of parallel-connected sections of oscillator.

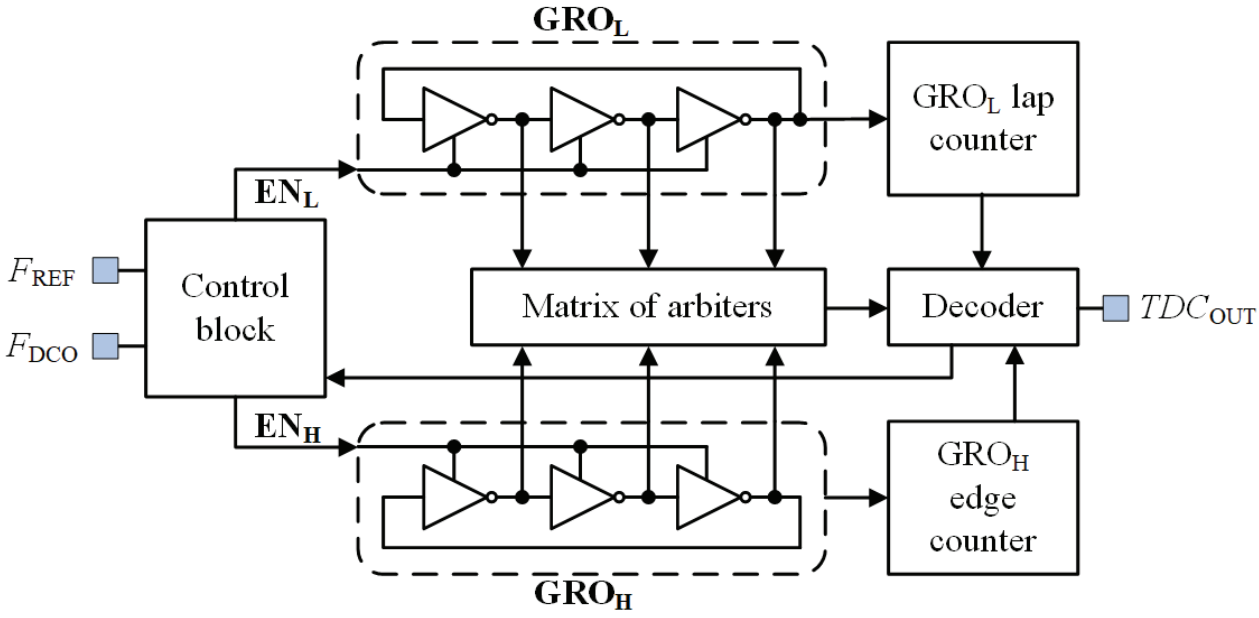

Figure 1: Structure of proposed time to digital converter

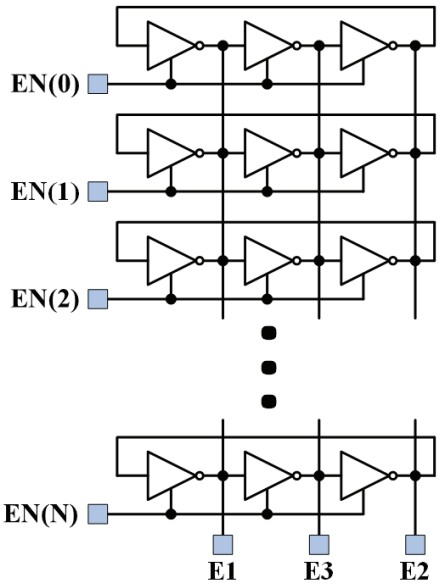

Figure 2: Structure of Gated Ring Oscillators

The output of oscillators is a periodic signal, but in this case oscillators are turned on only when the edge of the reference signal or the edge of the signal generated by the frequency synthesizer (i.e. DCO output signal) is received and oscillators are treated as infinite delay lines. To calculate the output of TDC we need to know through how many delay elements (oscillator's stages) signal has propagated. For this task lap counters are used to calculate through how many oscillator's laps the signal has travelled and edge counters to calculate signal's edges in one lap (i.e. through how many delay elements the signal has traveled in current lap). From values of both counters the total number of propagated delay elements may be calculated.

Only rising edges of gated ring oscillator's signals are used to calculate the time interval between edges of TDC input signals to avoid mismatch between edge rise and fall times [9]. Since oscillators are made of tristate inverters, edges used for calculation are distributed not in succession as shown in Fig. 2 (ports E1, E3, E2), because the signal is inverted after each stage. Therefore, one logical delay element is made of two tristate inverters and one logical lap is counted after two laps.

2.2 Arbiters

Often D type flip-flops are used as arbiters in time to digital converters – data input can be used as input for delayed versions of reference signals and clock inputs are used as input for delayed versions of generated signals. As it is known, for correct operation of D flip-flop, its data signal should be constant during setup and hold time near clock signal edge i.e. in metastability window (time interval $T_S + T_H$, shown in Fig. 3). Otherwise, if signal changes in metastability window, the output of the flip-flop can acquire any value (Fig. 3, (b)). Correct operation of flip-flop is essential in TDC application, because in locked state of the frequency synthesizer or when the edge of generated signal catches up with the edge of reference signal (in Vernier operation), edges of clock and data signals are very close to each other. One of the common method to address this issue is to use sense amplifier flip-flops, which have a narrow metastability window [1]. But unfortunately, these flip-flops are not suitable for synthesis.

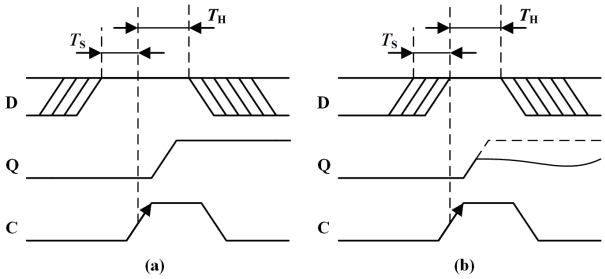

Figure 3: Operation of D type Flip-Flop: correct output (a) and possible metastability (b). T_S – setup time, T_H – hold time

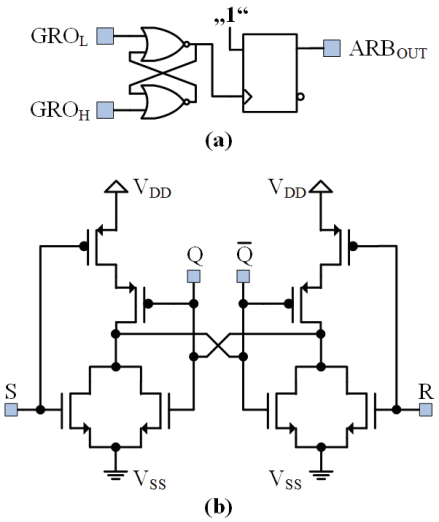

Figure 4: Arbiters made of SR latch and D flip-flop (a) and symmetrical structure of SR latch, composed from NOR gates (b)

Arbiters made of SR latch and D type flip-flop shown in Fig. 4, (a), can be used to narrow the metastability window [5], [9]. Latch is a level sensitive device, so even if edges of input signals are received close to each other, the output of the latch will settle to a known logic level. D type flip-flop is edge sensitive, so its metastability is eliminated by connecting data input to constant logical "1" level and the output of the SR latch is used as a clock signal. It should be noted, that the D flip-flop in such an arbiter should be reset before each

measurement, since it can't change its state to logic "0" after it was set to "1", because its data input is constant high. Also, SR latch made of NOR or NAND gates has symmetrical structure (Fig. 4, (b)), so it is equally loading both ring oscillators, although if it is implemented in hardware description language, designer is dependent on foundry-provided standard cells and usually cannot affect schematics and layout of individual gates.

3 Operation of TDC.

The control algorithm of proposed TDC is shown in Fig. 5. To simplify overall design of the TDC and lower used area of silicon, TDC is measuring only positive time intervals, i.e. when the edge of the reference signal is received earlier than the edge of the signal generated by digitally controlled oscillator. On the other hand, negative delays are equal to large positive delays (larger than half of the period of the reference signal).

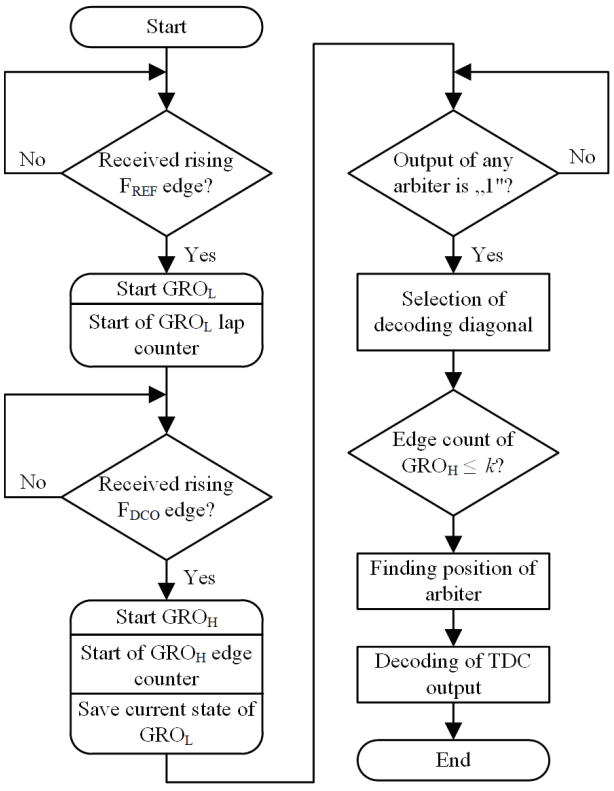

Figure 5: Control algorithm of proposed time to digital converter

At the beginning of the measurement TDC is waiting for the rising edge of the reference signal. When it is received, the lower frequency gated ring oscillator and its lap counter are started and the TDC's input for the reference signal is disabled. After that TDC is waiting for the rising edge of the signal generated by synthesizer's DCO. When it is received, the state of lower frequency oscillator (signal levels after each inverter) is saved, higher frequency oscillator and its edge counter are started and the TDC's input for the signal of DCO is disabled. When both oscillators are started, the output values of arbiters are monitored. When the output of any arbiter changes to high logic level, position of that arbiter is searched and depending on that position, the output signal of TDC is decoded. After that, all counters are reset, both inputs of TDC are enabled and TDC is waiting for another pair of the input signals for new measurement. Such operation allows to avoid usage of complex phase detector, introduced in [6].

Distinct case of 2D Vernier operation is obtained when the delays of stages composing two oscillators (or delay lines) are related with such dependency [5, 6]:

$$\Delta = \tau_{res} = \tau_1 - \tau_2; \quad \tau_1 = k \cdot \Delta; \quad \tau_2 = (k-1) \cdot \Delta \qquad (1)$$

where τ_1 and τ_2 are delays of respectfully lower and higher frequency oscillator's stages. Coefficient k should be set depending on values of τ_1 and τ_2 to meet this dependency.

In this case, the resolution of 2D Vernier TDC is same as of 1D Vernier TDC, but we are obtaining continuous Vernier plane of TDC's output time samples without breaks or missing points. The values of this plane can be calculated as shown in equation (2).

$$TDC_{OUT} = k \cdot X - (k-1) \cdot Y \qquad (2)$$

where X and Y are coordinates of Vernier plane, which show through how many stages propagated respectfully reference and DCO's signal.

Fragment of calculated plane of TDC's output time samples, when τ_1 is set to 10 ps, τ_2 is set to 9 ps, and k = 10, is shown in Fig. 6. GRO_{LL} and GRO_{HL} are lap counts of respectfully lower and higher frequency gated ring oscillator, GRO_{LE} and GRO_{HE} are edge counts in one lap of respectfully lower and higher frequency gated ring oscillator. Part of the plane, which is marked in green is used for calculation of TDC output. Grey area is not used for calculation - it marks negative time intervals which aren't measured by TDC. White area of the plane can be used for TDC output calculation if coefficient k is set to a different value, e.g. if k is set to 15, green area in first diagonal would extend to 15, recalculated values of second diagonal would be equal from 16 to 30, values of third diagonal – from 31 to 45, etc.

One of the main tasks in 2D Vernier TDC, which is based on gated ring oscillators, is output decoding. The output of arbiter will change to high logic level when arbiter's input, connected to GRO_H stage, will be high and

GRO_{HL}	GRO_{HE}	Y															
4	3	15	-125	-115	-105	-95	-85	-75	-65	-55	-45	-35	-25	-15	-5	5	15
	2	14	-116	-106	-96	-86	-76	-66	-56	-46	-36	-26	-16	-6	4	14	24
	1	13	-107	-97	-87	-77	-67	-57	-47	-37	-27	-17	-7	3	13	23	33
3	3	12	-98	-88	-78	-68	-58	-48	-38	-28	-18	-8	2	12	22	32	42
	2	11	-89	-79	-69	-59	-49	-39	-29	-19	-9	1	11	21	31	41	51
	1	10	-80	-70	-60	-50	-40	-30	-20	-10	0	10	20	30	40	50	60
2	3	9	-71	-61	-51	-41	-31	-21	-11	-1	9	19	29	39	49	59	69
	2	8	-62	-52	-42	-32	-22	-12	-2	8	18	28	38	48	58	68	78
	1	7	-53	-43	-33	-23	-13	-3	7	17	27	37	47	57	67	77	87
1	3	6	-44	-34	-24	-14	-4	6	16	26	36	46	56	66	76	86	96
	2	5	-35	-25	-15	-5	5	15	25	35	45	55	65	75	85	95	105
	1	4	-26	-16	-6	4	14	24	34	44	54	64	74	84	94	104	114
0	3	3	-17	-7	3	13	23	33	43	53	63	73	83	93	103	113	123
	2	2	-8	2	12	22	32	42	52	62	72	82	92	102	112	122	132
	1	1	1	11	21	31	41	51	61	71	81	91	101	111	121	131	141
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15 X
			1	2	3	1	2	3	1	2	3	1	2	3	1	2	3 GRO_{LE}
			0			1			2			3			4		GRO_{LL}

Figure 6: Calculated plane of TDC's output time samples, when τ_1 = 10 ps, τ_2 = 9 ps, k = 10

input, connected to GRO_L stage, is low. Since arbiters in 2D structure are connected between all stages of both gated ring oscillators, even first rising edge of GRO_H will trigger one or two arbiters. It happens because in three-stage ring oscillator, at any given moment the output signal of one or two inverters is low (it can be seen in Fig. 8, provided in next section). For this reason, such TDC can't measure time intervals lower than k using 2D structure and it is needed to evaluate if the output of arbiter is valid. E.g. in our example, if input time interval is lower or equal to 10, arbiter connected between first stage of GRO_H and second stage of GRO_L will become high with first GRO_H edge, since it will always lead second edge of GRO_L and output of TDC will be incorrectly set to 11 (X = 2, Y = 1 position in Fig. 6). This issue is solved by saving the state of arbiters after first GRO_H edge, which corresponds to GRO_{LE} in Fig. 6. This value, combined with lap count of GRO_L, will give total number of propagated GRO_L stages – coordinate X. After that checking is done in 1D Vernier manner: going diagonally up in Vernier plane, but only in diagonal, which is starting at coordinate X.

As discussed earlier, value of the coefficient k should meet equation (1). Coefficient k shows, that the total delay of k-1 stages of the lower frequency oscillator should be equal to the total delay of k stages of the higher frequency oscillator. Therefore, stage counters of the both oscillators can be employed to set needed value of the coefficient k.

Following guidelines can be used to set the values of coefficient k and number of turned on oscillator's sections (N_{OSC}) for both oscillators. At the beginning (e.g. after power-on of the chip) N_{OSC} for higher frequency oscillator can be set to highest available value N_{OSCH}, since, as it will be seen in the following section, frequency step, which corresponds to the resolution of TDC, is smaller at highest values of N_{OSC}, and N_{OSC} for lower frequency oscillator can be set to N_{OSCH}-1. After that both oscillators should be enabled and counters should count through how many stages of each oscillator signal has propagated. When value of stage counter of higher stage oscillator reaches targeted value of k, stage count of lower frequency oscillator should be checked:

- if it is equal to k-1, correct values of N_{OSC} are set for both oscillators;
- if it is equal to k – tuning step is too small for current value of coefficient k. Value of N_{OSC} for lower frequency oscillator should be decreased by one and measurement should be repeated. After that, if value of the counter drops to k-2, N_{OSC} for higher frequency oscillator should be decreased by one and measurement should be repeated. Also, coefficient k can be increased, since, as it can be seen from equation (1), higher k value is needed for lower tuning step when value of stage delay is constant.
- if it is equal to k-2 – tuning step is too large for current value of k. coefficient k should be decreased and measurement should be repeated.

After initial settings, measurement can be repeated for longer period of time, to validate correct values e.g. count to 4×k higher frequency oscillator's stages and check if count of lower frequency oscillator's stages is equal to 4×(k-1).

Additional fine-tuning can be done by using technique, described in [8] which takes advantage of the irregularity in automatic place-and-route, when different sections of the oscillator have different effective driving strength, resulting in different tuning step. i.e. same number of the enabled oscillator's sections can result in different stage delay, depending on the position in chip layout of the sections.

It should be noted, that incorrect value of k will introduce nonlinearity when TDC is operating in 2D Vernier mode i.e. measuring large input time intervals. When input time intervals are small and TDC is operating in 1D Vernier manner, value of the coefficient k has no effect for it.

Another advantage of 2D Vernier TDC is faster calculation of output signal, compared to 1D structure. The time duration to calculate the output of proposed TDC can be expressed as:

$$T_{IN} + \tau_2 \le T_{OUT2D} \le T_{IN} + k \cdot \tau_2 \qquad (3)$$

where T_{IN} – TDC's input time interval.

As it can be seen from equation (3), the time duration of TDC's output signal calculation depends nonlinearly on input time interval. Maximal time duration to calculate output signal of TDC is equal to $T_{IN} + k \cdot \tau_2$, i.e. after receiving the rising edge of DCO signal, it has to propagate through k stages of higher frequency gated ring oscillator.

The output of 1D Vernier TDC is calculated after:

$$T_{OUT1D} = T_{IN} + \frac{T_{IN}}{\Delta} \cdot \tau_1 \quad (4)$$

Output calculation time dependency on input time interval, when 2D and 1D TDC structure is used, is shown in Fig. 7. If τ_1 = 10 ps, τ_2 = 9 ps and TDC input time interval is 21 ps, from equations (3) and (4) it can be seen that TDC output will be calculated after 30 ps, when proposed TDC is used, and it will take 231 ps to calculate the output signal, if 1D Vernier TDC is used. Such long interval in latter case is obtained, because arbiters in 1D Vernier TDC are comparing signals only after respectful stages of ring oscillator (or delay line). After each stage, time interval between edges of reference and DCO output signals is reduced by Δ ps. Therefore, after receiving rising edge of DCO signal, it has to travel T_{IN}/Δ stages, to catch up with the edge of reference signals.

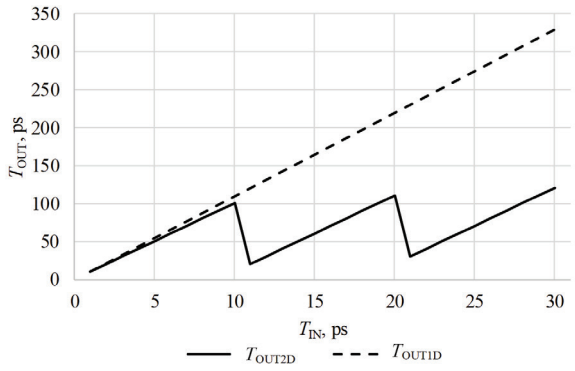

Figure 7: Output calculation time dependency on input time interval of proposed 2D time to digital converter and 1D Vernier time to digital converter

4 Modeling results

Functional modelling of TDC, implemented in VHDL hardware description language, was done using ModelSim environment. Figure 8 shows the results of functional modelling and main signals of TDC, when τ_1 and τ_2 are respectfully set to 10 ps and 9 ps. As it can be seen, when input time interval is equal to 8 ps, the output of TDC is calculated when eighth edge of higher frequency oscillator outruns eighth edge of lower

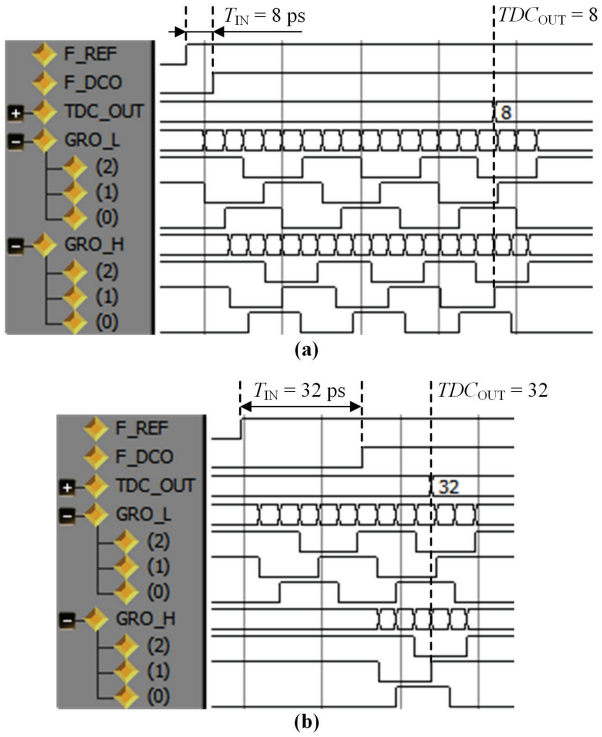

Figure 8: Time to digital conterver's functional modeling results, when input time interval is equal to 8 ps (a) and 32 ps (b)

frequency oscillator. When input time interval is equal to 32 ps, the output of TDC is calculated when second edge of higher frequency oscillator outruns fifth edge of lower frequency oscillator. These results correspond to data in Vernier plane, shown in Fig. 6.

TDC was synthesized, placed and routed in 65 nm CMOS technology using Cadence software. 48 parallel GRO sections were used to form both oscillators used in TDC. It is hard to model oscillators and their tuning using digital IC design tools. Therefore, additional post-layout transient simulations of synthesized oscillators were made using analog design approach to investigate its frequency and stage delays dependency on enabled number of GRO sections.
Simulations were made in three conditions:

- Typical: typical process corner, 1.2 V supply voltage, 40 °C temperature;
- Worst: slow process corner, 1.1 V supply voltage, 80 °C temperature;
- Best: fast process corner, 1.3 V supply voltage, -40 °C temperature;

Simulation results of frequency F_{OSC} dependency on number of turned on oscillator's sections N_{OSC} is shown in Figure 9 and corresponding stage delay τ is shown in Figure 10.

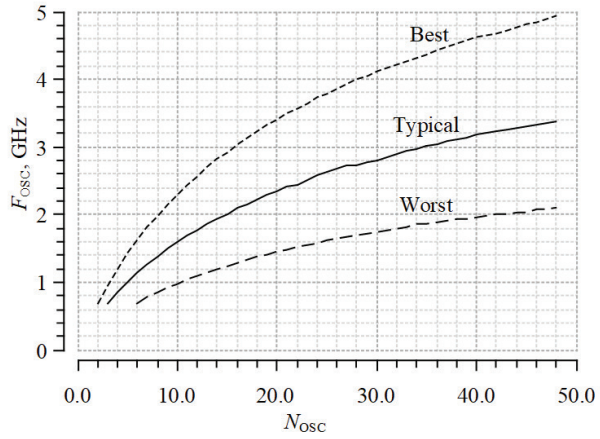

Figure 9: Dependency of frequency F_{OSC} on number of turned on oscillator's sections N_{OSC}

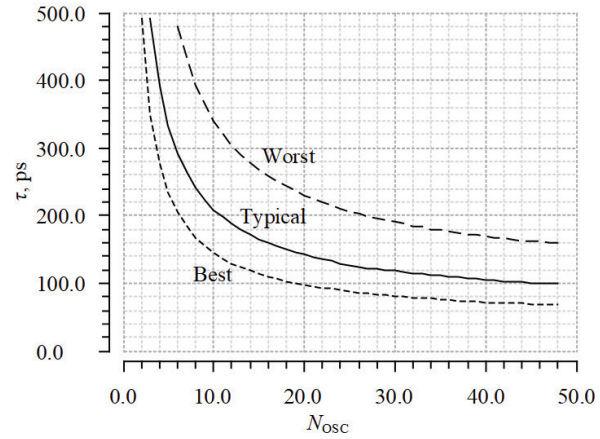

Figure 10: Dependency of stage delay τ on number of turned on oscillator's sections N_{OSC}

As it can be seen from Fig. 9 and Fig. 10, the stage delay changes depending on working conditions (process, voltage, temperature). Although in the 1D and 2D Vernier operation the difference of time delay is more important than the absolute value of stage delay, to compensate variation of the stage delay and to maintain same value

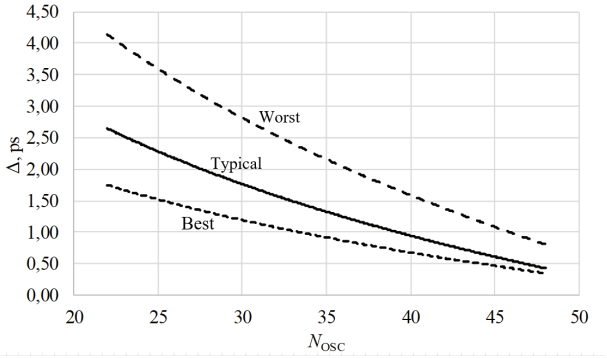

Figure 11: Step of oscillator's stage delay when number of enabled oscillator's sections changes from 22 to 48

of coefficient k at different values of temperature (e.g. at 25 °C and 65 °C), tuning technique from [8], which was mentioned earlier, can be used.

The frequency of GRO can be tuned from 0.68 GHz to 3.38 GHz in typical conditions, from 0.70 to 2.10 GHz in worst conditions, from 0.68 GHz to 4.93 GHz in best conditions. At least 3, 6 and 2 sections of oscillator need to be enabled respectfully in typical, worst and best condition for oscillator to start. Delay of single stage can be changed from 491 ps to 98 ps in typical conditions, from 479 ps to 158 ps in worst conditions and from 491 ps to 67 ps in best conditions.

As it can be seen, dependency of frequency and stage delay on turned on number of oscillator sections is nonlinear, similar to hyperbolic. Its slope is higher at low values of N_{OSC} and lower at higher values of N_{OSC}. Therefore, to achieve higher resolution of Vernier TDC, higher numbers of N_{OSC} should be used, where steps of oscillator's frequency and stage delay are smaller, since step of stage delay $\Delta = \tau(N_{OSC}-1) - \tau(N_{OSC})$ corresponds to the resolution of TDC if N_{OSC} sections are enabled in higher frequency oscillator and N_{OSC}-1 sections are enabled in lower frequency oscillator.

Table 1: TDC's performance comparison to other works

Reference	Structure	Technology	Resolution, ps	Supply, V	Current, mA	Area, mm²	Synthesised
This work	2D Vernier GRO	65 nm	3.2-0.8	1.2	3.0	0.008 (core); 0.018 (full)	Yes
[1]	Delay line	65 nm	10-30	1.2	N/A	N/A	No
[2]	Three-step	0.13 µm	1	1.2	2.9	N/A	No
[3]	Two-step	0.13 µm	4	1.2	3.7	0.028	No
[5]	2D Vernier delay line	65 nm	4.8	1.2	1.42	0.02 (core)	No
[6]	2D Vernier GRO	90 nm	2.2	1.0	2.3	0.068	No
[7]	Stochastic	0.13 µm	0.7	1.2	2.25	0.11	No
[8]	1D Vernier GRO	65 nm	5.5	1.0	1.4	0.006	Yes
[9]	1D Vernier GRO	90 nm	3.2	1.2	3.0	0.027	No

Recalculated step of oscillator's stage delay in close to linear fragment of Figure 10, when N_{OSC} changes from 22 to 48, is shown in Figure 11. In this part step of stage delay changes from 3.2 ps to 0.8 ps in typical conditions, from 4.0 ps to 1.1 ps in worst conditions and from 1.8 ps to 0.5 ps in best conditions. It should be noted, that the correct value of coefficient k should be set to meet the requirements of equation (1) as it was described in the previous section.

Summary of TDC's parameters and comparison to other works is presented in Table 1.

5 Layout

Layout of proposed time to digital converter, synthesized in 65nm CMOS technology is shown in Figure 12. The core of TDC occupies 75 µm × 100.8 µm space of silicon, total area of TDC including power rings is 123 µm × 148.8 µm.

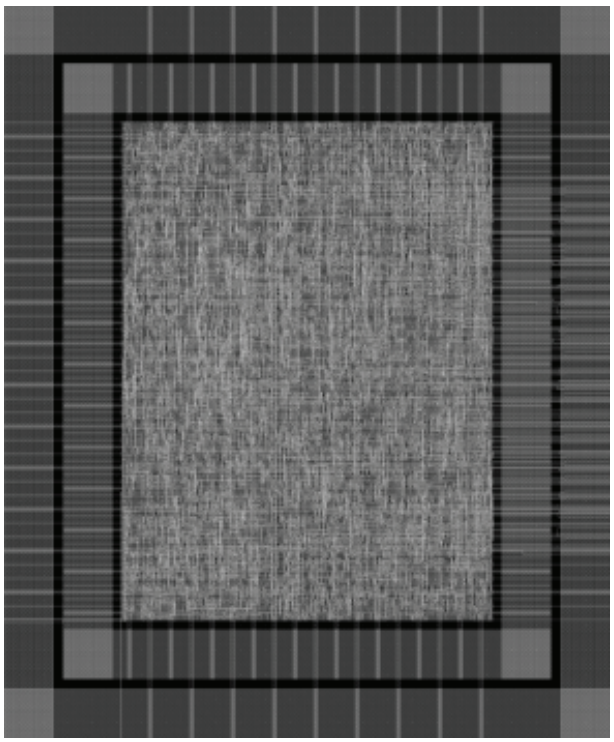

Figure 12: Layout of proposed time to digital converter

6 Conclusions

In this paper, synthesizable 2D Vernier time to digital converter (TDC) based on two gated ring oscillators and its control algorithm was proposed. Such TDC can measure sub-inverter delay time intervals and its result is calculated faster, compared to 1D Vernier TDC. Proposed TDC is implemented using VHDL hardware description language, therefore it can be easily migrated to various technology nodes. It was synthesized, placed and routed in 65 nm CMOS technology.

Main blocks of TDC are two oscillators, made of parallel-connected three stage gated ring oscillators (GRO), their lap and edge counters, arbiter matrix, decoder and control block. Frequency of oscillators and corresponding delay time of single stage are controlled by changing number of enabled GROs. To reduce metastability window of arbiters, they are composed of SR latches and D flip-flops.

Tuning step of single stage delay of gated ring oscillator, which is equal to the resolution of TDC, ranges from 3.2 ps to 0.8 ps at nominal conditions, when number of enabled oscillator's sections is changed from 22 to 48.

Total area of silicon occupied by time to digital converter, including power rings, is equal to 123 µm × 148,8 µm.

7 Acknowledgment

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8 References

1. R. B. Staszewski, K. Waheed, F. Dulger, and O. E. Eliezer, "Spur-Free Multirate All-Digital PLL for Mobile Phones in 65 nm CMOS" IEEE J. Solid-State Circuits, vol. 46, no. 12, pp. 2904–2919, Dec. 2011. https://doi.org/10.1109/JSSC.2011.2162769
2. Y. G. Pu, A. S. Park, J. S. Park, and K. Y. Lee, "Low-power, all digital phase-locked loop with a wide-range, high resolution TDC" ETRI J., vol. 33, no. 3, pp. 366–373, 2011. http://dx.doi.org/10.4218/etrij.11.0110.0295
3. A. Samarah and A. C. Carusone, "A digital phase-locked loop with calibrated coarse and stochastic fine TDC" IEEE J. Solid-State Circuits, vol. 48, no. 8, pp. 1829–1841, 2013. https://doi.org/10.1109/JSSC.2013.2259031
4. P. Dudek, S. Szczepański, and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line" IEEE J. Solid-State Circuits, vol. 35, no. 2, pp. 240–247, 2000. https://doi.org/10.1109/4.823449
5. L. Vercesi, A. Liscidini, and R. Castello, "Two-dimensions vernier time-to-digital converter" IEEE J. Solid-State Circuits, vol. 45, no. 8, pp. 1504–1512, 2010. https://doi.org/10.1109/JSSC.2010.2047435

6. P. Lu, Y. Wu, and P. Andreani, "A 2.2-ps Two-Dimensional Gated-Vernier Time-to-Digital Converter with Digital Calibration" IEEE Trans. Circuits Syst. II Express Briefs, vol. 63, no. 11, pp. 1019–1023, 2016. https://doi.org/10.1109/TCSII.2016.2548218
7. V. Kratyuk, P. K. K. Hanumolu, K. Ok, U.-K. M. U.-K. Moon, and K. Mayaram, "A Digital PLL With a Stochastic Time-to-Digital Converter" Circuits Syst. I Regul. Pap. IEEE Trans., vol. 56, no. 8, pp. 1612–1621, 2009. https://doi.org/10.1109/TCSI.2008.2010109
8. Y. Park and D. D. Wentzloff, "A cyclic vernier TDC for ADPLLs synthesized from a standard cell library" IEEE Trans. Circuits Syst. I Regul. Pap., vol. 58, no. 7, pp. 1511–1517, 2011. https://doi.org/10.1109/TCSI.2011.2158490
9. P. Lu, A. Liscidini, and P. Andreani, "A 3.6 mW, 90 nm CMOS gated-vernier time-to-digital converter with an equivalent resolution of 3.2 ps" IEEE J. Solid-State Circuits, vol. 47, no. 7, pp. 1626–1635, 2012. https://doi.org/10.1109/JSSC.2012.2191676

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A Meta-Heuristic Approach for Wavelength Assignment in Long-Haul Optical System

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Abstract: Routing and Wavelength Assignment (RWA) problem is one of the optimization problems in optical networks. The aim is to minimize the blocking probability and the number of wavelengths used. The RWA problem can be solved by number of algorithms like Genetic Algorithm (GA), Ant Colony Optimization (ACO), etc. In the proposed research, Shuffled Frog Leaping Algorithm (SFLA) has been implemented in optical networks to solve the RWA problem. The optimization parameters considered are cost, number of wavelengths, hop count and blocking probability. The problem is analyzed for different wavelength assignment methods such as first fit, random, round robin, wavelength ordering and Four Wave Mixing (FWM) priority based wavelength assignment. Fitness function devised includes cost, number of wavelengths, hop count and setup time. The proposed SFLA algorithm has been compared with GA and is found to minimize the blocking probability, cost and computational complexity.

Keywords: GA; RWA; SFLA; WDM

Metahevristični pristop določitve valovne dolžine optičnega sistema Long-Haul

Izvleček: Osnoven problem optičnih omrežjih je njihova pot in določitev valovne dolžine (RWA). Namen je minimizacija verjetnosti združevanja in števila uporabljenih valovnih dolžin. RWA problem se lahko reši s številnimi algoritmi, kot so generičen algoritem (GA), Ant Colony optimizacija (ACO) in drugi. V predstavljeni raziskavi je bil uporabljen Shuffled Frog Leaping Algoritem (SFLA). Parametri optimizacije so bili strošek, število valovnih dolžin ter število poskokov in verjetnost združevanja. Problem je bil analiziran za različne določitve valovnih dolžin, kot so prvi približek, naključnost, sistem vsak s vsakim, urejanje valovnih dolžin ter Four Wave Mixing (FWM) prednostna določitev valovne dolžine. Predlagan SFLA algoritem je bil primerjan z GA algoritmom. Izkazalo se je, da SFLA zmanjšuje verjetnost združevanja, strošek in kompleksnost računanja.

Ključne besede: GA; RWA; SFLA; WDM

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1 Introduction

In high capacity telecommunication networks, Optical networks play a major role. Routing, grooming and restoration are the wavelength based services provided by optical networks. Fiber optics is to transmit data in the form of light. Electrically powered switching equipment such as a router or a switch aggregator is used in active optical system. It is used to regulate signal distribution and to direct the signals to different users. The switch controls the incoming and outgoing signals. Optical splitters are used to isolate and collect optical signals. The aim of optical communication systems is to transfer large amount of information with simple equipments (Batagelj 2014).Optical fiber communication performs better in terms of transmission capacity and communication range (Vidmar 2001).

An optical Wavelength Division Multiplexing (WDM) network is a network with fiber optic transmission links designed to utilize the features of fibers and WDM. Wavelength-division multiplexing meets the high bandwidth demand. Several routing and wavelength assignment problems that exist in optical wavelength division multiplexing are traffic grooming , optimal routing and wavelength assignment, survivability, Quality of service(QoS) routing and physical layer impairment aware (PLI aware) problems (Bhanjaa and Mahapatra 2013). A lightpath is an optical connection

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between two nodes. Depending on the wavelength of the lightpaths, data are optically routed at intermediate nodes (Le et al 2005 and Bisbal et al 2004). Conventional methods to solve these complex problems consume more computational time (Wang et al 2014 and Triay et al 2010). Multi-objective evolutionary algorithms based on swarm intelligence are used to solve the RWA problem, which are in real- world optical networks (Kavian et al 2013 and Largo et al 2012). In the proposed method Shuffled Frog Leaping Algorithm is used to solve this problem. Similar algorithms available are either simple leading to poor performance or too complex to be used. The aim is to use computationally feasible algorithm for better network performance.

In this research paper, routing and wavelength assignment problem model is described with two optimization algorithms, genetic algorithm and shuffled frog leaping algorithm. Genetic Algorithm is used to solve many problems in variety of fields and hence comparison of SFLA is done with this algorithm. The discussions include simulation results, analysis, conclusions of the study and possible future work.

2 Routing and wavelength assignment problem

2.1 Problem Definition

In dynamic routing and wavelength assignment, the lightpath requests arrive dynamically. A lightpath in a network is the path that satisfies the wavelength continuity constraint (that is, same wavelength should be used by the lightpath on all the links in its path). For each lightpath request, source node, destination node and holding time are defined. Holding time is the time during which a lightpath and the associated resources remain occupied. The resources become free, when the holding time elapses and can support other lightpath requests. Fig.1 shows the model to solve the RWA problem (Bhanjaa et al 2013).

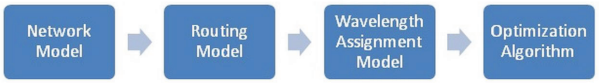

Figure1: Block diagram of optimization method

2.2 Network Model

A network with N nodes can be modeled as a graph G(V,E), where V is the set of nodes denoting the routers or switches and E is the set of edges denoting connectivity between the nodes. The links between the nodes are assumed to be bidirectional. In dynamic routing and wavelength assignment problem, V is the set of nodes denoting routers or wireless routing networks and E is the set of fiber links denoting physical connectivity between the nodes.

2.3 Routing Model

Routing and Wavelength Assignment (RWA) is one of the major problems in optical networking. The goal is to maximize the number of optical connection. A route and wavelength must be assigned for each connection request. Throughout the path, wavelength must be the same, unless the usage of wavelength converters is assumed. Two connections requests can share the same optical link, if different wavelength is provided (Bhanjaa et al 2012).

Fitness function to be maximized is given by

$$f_x = \frac{W_x}{\sum_{j=1}^{k_x-1} C_{gx(j),gx(j+1)}} + \frac{W_x}{\sum_{(i,j)\in E} H_{i,j}^x} + \frac{W_x}{T_x} \quad (1)$$

W_x is free wavelength factor and takes the value of one, if same wavelength is available in all the links of path x or otherwise, zero. Summation in the first term defines the total link cost of the path and summation in the second term represents the total number of hops in the path. The variable $H^x_{i,j}$ is one, if link (i, j) is a part of path x and is zero otherwise. Variable T_x represents the set up time of path x. Variable K_x represents the length of the x-th chromosome or number of memeplexes. The route is optimal when the objective function maximizes with the following constraints being satisfied.

$$\sum_{(i,j)\in E} I_{ij}^{lp} - \sum_{(j,i)\in E} I_{ij}^{lp} = 1, \text{ if } i=S, lp \in LP \quad (2)$$

$$\sum_{(i,j)\in E} I_{ij}^{lp} - \sum_{(j,i)\in E} I_{ij}^{lp} = -1, \text{ if } i=D, lp \in LP \quad (3)$$

$$\sum_{(i,j)\in E} I_{ij}^{lp} - \sum_{(j,i)\in E} I_{ij}^{lp} = 0, \text{ if } i \neq S, i \neq D, lp \in LP \quad (4)$$

$$\sum_{\substack{i\neq j \\ (i,j)\in E}} I_{ij}^{lp} \leq 1, \text{ if } i \neq D, lp \in LP \quad (5)$$

$$\sum_{\substack{i\neq j \\ (i,j)\in E}} I_{ij}^{lp} = 0, \text{ if } i=D, lp \in LP \quad (6)$$

$$\sum_{(i,j)\in E} I_{ij}^{lp} \le h_0, \text{ for } t \le T \quad (7)$$

$$h_0 < \sum_{(i,j)\in E} I_{ij}^{lp} \le (N-1), \text{ for } t > T \quad (8)$$

Equations (2) to (6) represent the flow conservation constraint. Equations (7) and (8) represent the hop count constraint.

2.4 Wavelength Assignment Model

First fit and Random fit are the wavelength assignment techniques that are used generally. First Fit method decides the available wavelength with the lowest index while random fit method identifies the available wavelengths and chooses randomly amongst them. O(w) is the complexity of both algorithms, where w is the number of wavelengths. First Fit outperforms Random Fit. Other wavelength assignment techniques used here are round robin technique, wavelength ordering technique and Four Wave Mixing aware wavelength assignment technique. In FWM aware wavelength assignment technique, since the FWM crosstalk power will be more over the center of transmission window, priority is given to the wavelengths towards the edges of the transmission window. $O(N^3 \log^2 N)$ is the complexity of this method, where N is the number of nodes in the network. In the proposed fitness function, Wx the free wavelength factor is updated after the wavelength assignment phase. In the wavelength assignment model, if the link (i, j) is used by the lightpath lp, the variable I_{ij}^{lp} assumes one else it assumes zero. Variable I_{ijw}^{lp} is the lightpath wavelength indicator. It shows whether the lightpath lp uses wavelength 'W' on link (i, j). Variable $I_{ijw}^{lp}(x,y)$ is the lightpath wavelength link indicator and is one when the lightpath uses wavelength 'W' on link (i, j) between the nodes x and y. I(x,y) equals one if a physical link exists between the nodes x and y (Bhanjaa et al 2010).

The wavelength continuity constraints are

$$I_{ij}^{lp} = \sum_{w=0}^{W-1} I_{ijw}^{lp}, \ \forall \ (i,j) \quad (9)$$

$$I_{ijw}^{lp(x,y)} \le I_{ijw}^{lp}, \ \forall \ (i,j), \forall \ (x,y), \forall \ w \quad (10)$$

$$\sum_{i,j} I_{ijw}^{lp(x,y)} \le 1, \ \forall \ (x,y), \forall \ w \quad (11)$$

$$\sum_{w=0}^{W-1}\sum_{x} I_{ijw}^{lp(x,y)} l^{(x,y)} - \sum_{w=0}^{W-1}\sum_{x} I_{ijw}^{lp(y,x)} l^{(y,x)} = I_{ij}^{lp}, \ y=j \quad (12)$$

$$\sum_{w=0}^{W-1}\sum_{x} I_{ijw}^{lp(x,y)} l^{(x,y)} - \sum_{w=0}^{W-1}\sum_{x} I_{ijw}^{lp(y,x)} l^{(y,x)} = -I_{ij}^{lp}, \ y=I \quad (13)$$

$$\sum_{w=0}^{W-1}\sum_{x} I_{ijw}^{lp(x,y)} l^{(x,y)} - \sum_{w=0}^{W-1}\sum_{x} I_{ijw}^{lp(y,x)} l^{(y,x)} = 0, \ y \ne i, y \ne j \quad (14)$$

3 Optimization algorithms

3.1 Genetic Algorithm

The methodology of Genetic Algorithm is shown in Fig.2. This method works iteratively on an initial solution set which is referred to as population and converges to arrive on best solution (Kavian et al 2009).

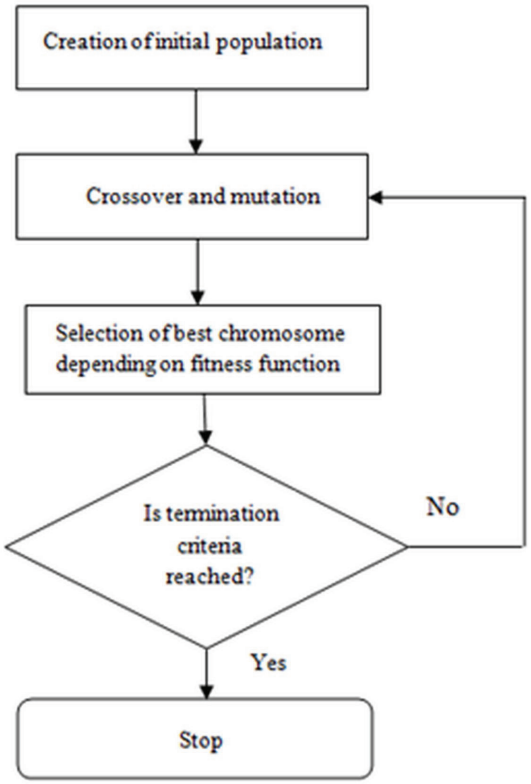

Figure 2: Flow diagram of GA

3.2 Representation of chromosome and Initialization of population

Route or path encoded from source to destination is represented by a chromosome. A sequence of nodes creates each chromosome and is generated randomly satisfying the topology of particular network. The chromosomes are of variable length, each of which is the encoding of a path from the source node S to the destination node D. Random selection of solutions create

initial population. The initial population has only one chromosome.

3.3 Crossover and Mutation

Crossover does not depend on the position of nodes in routing paths. One pair is randomly taken and the crossing site of each chromosome is identified by the locus of each node. The crossing points of two chromosomes may be different from each other (Ahn and Ramakrishna 2002). During mutation, the mutation site of the parent chromosome is chosen randomly. From the mutation site to the destination, different path chosen is based on the topology database.

3.4 Calculation of fitness function

The fitness function is formulated as in equation (1) and is to evaluate the quality of the chromosomes.

3.5 Shuffled Frog Leaping Algorithm

Shuffled Frog Leaping Algorithm (SFLA) is a natural inspired metaheuristic algorithm. Novelty of this algorithm is its fast convergence speed. It combines the advantages of the both the genetic-based memetic algorithm and the behavior-based Particle Swarm Optimization (PSO) algorithm. In the SFLA, possible solutions are defined by a group of frogs which is referred to as population. These groups of frog are partitioned into several communities referred to as memeplexes. Each frog in the memeplexes perform local search. The behavior of individual frog is influenced by behaviors of other frogs within each memeplex and it develops through a process of memetic evolution. After a certain number of memetic evolutions, the memeplexes are forced to mix together and through shuffling process, new memeplexes are formed. Until convergence criteria are satisfied, the local search and the shuffling processes continue. The flowchart of Shuffled frog leaping algorithm is illustrated in Fig.3 (Roshni et al 2016).

The various steps are as follows:

a) SFLA involves a population 'P' of possible solution, defined by a group of virtual frogs(n).
b) Frogs are sorted in descending order based on their fitness and partitioned into subsets called as memeplexes (m).
c) Frog i is expressed as $X_i = (X_{i1}, X_{i2}, \ldots..X_{in})$ where X represents number of variables.
d) Frogs with worst and best fitness are identified as X_w and X_b within each memeplex.
e) Frog with global best fitness is identified as X_g.
f) The frog with worst fitness is improved based on the following equation.

$$D_i = \text{rand}() \ (X_b - X_w) \quad (15)$$

$$X_{neww} = X_{oldw} + D_i \quad (16)$$

Rand() is a random number in the range of [0,1] (Muzaffar 2006).

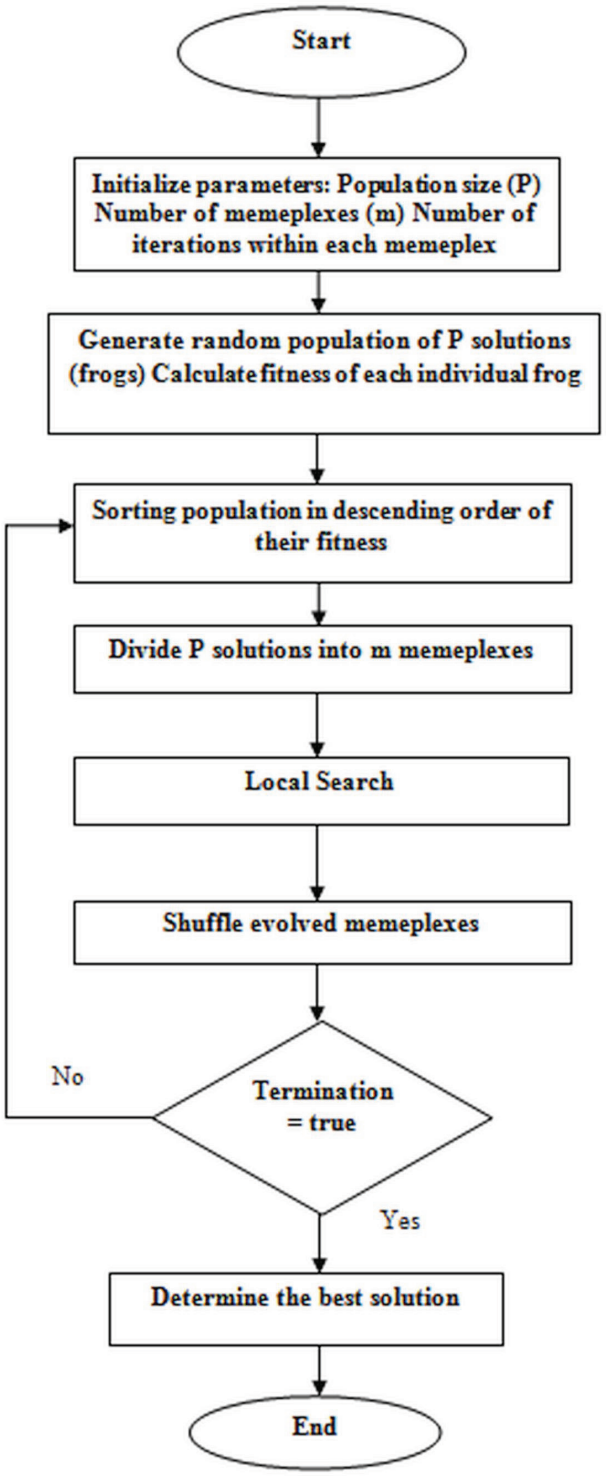

Figure 3: Flow diagram of SFLA

D_i is the step size of i-th leaping frog and D_{max} is the maximum step size allowed. If the fitness value of new X_w is better than the current one, X_w will be accepted. Otherwise, the calculated step size of leaping frog D_i and new fitness X_{neww} are recomputed with X_b replaced by X_g. Further if no improvement is achieved, a new X_w is generated randomly. The update operation is repeated for specific number of iterations. After a predefined number of memetic evolutionary steps within each memeplex, the solutions of evolved memeplexes are replaced into new population. This is called shuffling process. Global information exchange among the frogs is promoted by the shuffling process. The population is then sorted in order of decreasing performance values and updates the population based on best frog's position, repartition the frog group into memeplexes and progress the evolution within each memeplex until the convergence criteria are satisfied (Samuel and Rajan 2014).

4 Simulation results

The optimization algorithms have been carried out in MATLAB R2012b. Simulations are carried out for a 14 node network similar to NSFNET network topology with 21 bidirectional links. Fig.4 depicts the fitness of the genetic algorithm and shuffled frog leaping algorithm against the execution time. The fitness function involves cost, number of hops and holding time. Better fitness is achieved for a smaller execution time.

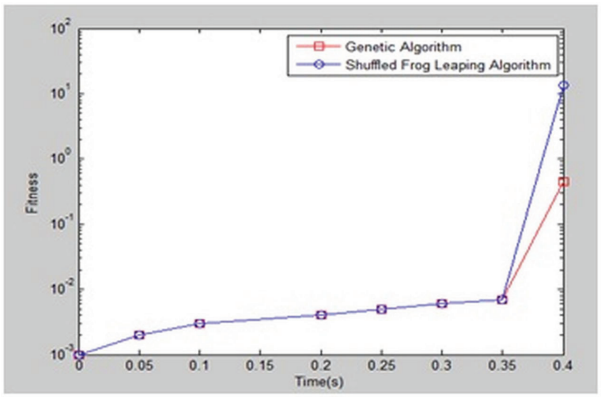

Figure 4: Fitness function of GA and SFLA

Fig.5 and 6 shows the variation in the blocking probability assuming different values of adjacent wavelength rejection ratios for GA and SFLA respectively. In each case by executing the program several times and then by computing the average, mean blocking probability is estimated. In FWM aware priority based wavelength assignment, the mean blocking probability decreases for a reduction in each of the adjacent wavelength rejection ratio. To reduce the FWM crosstalk equal and unequal channel spacing is also used which is said to be spectrum separation technique. The comlexity is lower in this technique. But the mean blocking probability is lesser and fitness score is better in the dynamic wavelength allocation based on FWM aware based priority assignment that makes it advantageous to be used.

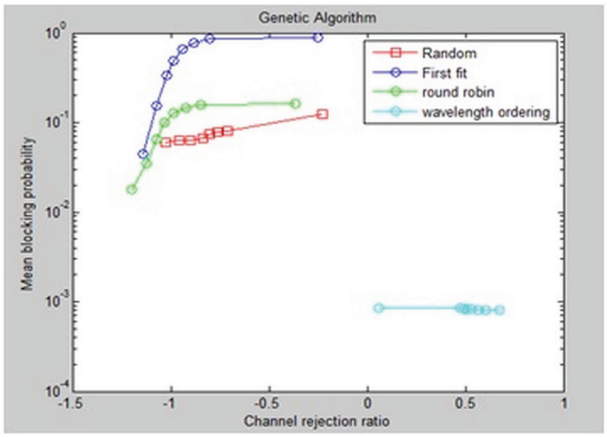

Figure 5: Mean blocking probability for a fixed network load using GA

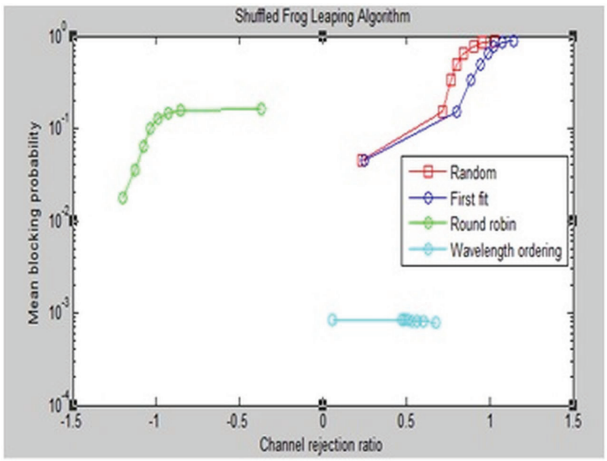

Figure 6: Mean blocking probability for a fixed network load using SFLA

Fig.7 shows the rate of convergence of genetic algorithm and shuffled frog leaping algorithm for first fit, random, round robin, wavelength ordering and FWM aware priority based wavelength assignment techniques. By randomly selecting an individual and fixing the best fitness value, the curves are plotted. The average fitness score decreases with increase in generations. Average fitness score for GA and SFLA using different wavelength assignment techniques are approximately the same. FWM priority based assignment has higher average fitness score.

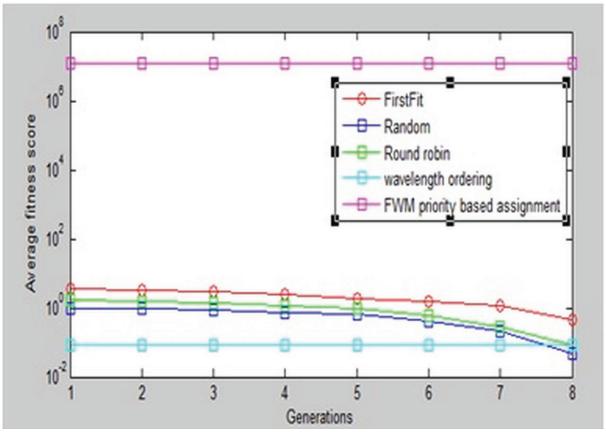

Figure 7: Average fitness score for GA and SFLA

The mean execution time of the five wavelength assignment techniques for different network load in Erlang using GA and SFLA are in Table 1. FWM aware priority based wavelength assignment technique has the least mean execution time for different network loads in both the algorithms. However, the mean execution time is minimum using SFLA compared to GA.

The experimental results in Table 2 show that wavelength ordering and round robin exhibits less mean blocking probability with respect to channel rejection ratio and number of generations respectively. Average fitness score is higher and the mean execution time is minimum in FWM aware priority based wavelength assignment technique. Comparing Genetic Algorithm and Shuffled Frog Leap Algorithm, Shuffled Frog Leap Algorithm achieves least mean blocking probability and a mean execution time for different wavelength assignment techniques such as First Fit, Random, Round Robin, Wavelength Ordering and FWM aware priority based wavelength assignment though the average fitness score is approximately same for both the algorithms.

5 Conclusions

Routing and Wavelength Assignment (RWA) problem is one of the most complex optimization problems in optical networks. In the proposed work, Genetic Algo-

Table 1: Mean Execution Time of different wavelength assignment techniques using GA and SFLA

Wavelength Assignment Techniques	Mean Execution Time (w.r.to network load(Erlang)) using GA					Mean Execution Time (w.r.to network load(Erlang)) using SFLA				
	0	1.4	2.7	3.6	4.4	0	1.4	2.7	3.6	4.4
First Fit	0.1200	0.0432	0.0689	0.1038	0.1019	0.1191	0.0423	0.0654	0.1018	0.1003
Random	0.3000	0.2372	0.2328	0.3155	0.3762	0.2987	0.2372	0.2328	0.3155	0.3762
Round Robin	0.1200	0.1736	0.1613	0.2004	0.2251	0.1198	0.1703	0.1610	0.2001	0.2248
Wavelength Ordering	0.0500	0.0062	0.0123	0.0302	0.0415	0.0490	0.0059	0.00117	0.0295	0.0409
FWM priority based Assignment	0.0050	4.275e-11	8.509e-11	2.1167e-10	2.94e-10	0.038	4.257e-11	8.503e-11	2.1068e-10	2.85e-10

Table 2: Comparison of GA and SFLA for different wavelength assignment techniques

Wavelength Assignment Techniques	GA				SFLA			
	Mean Blocking Probability (w.r.to channel rejection ratio)	Average fitness score	Mean Blocking Probability (w.r.to no. of generations)	Mean Execution Time	Mean Blocking Probability (w.r.to channel rejection ratio)	Average fitness score	Mean Blocking Probability (w.r.to no. of generations)	Mean Execution Time
First Fit	0.8910	2.1184	0.5176	0.0829	0.8899	2.1184	0.4508	0.008025
Random	0.7875	0.6087	0.6035	0.2711	0.7802	0.6087	0.5805	0.2709
Round Robin	0.5225	1.023	0.2018	0.1619	0.1009	1.023	0.0010	0.1618
Wavelength Ordering	0.0959	0.08175	-	0.0266	0.0947	0.08175	-	0.0256
FWM based Assignment	-	12.481	-	0.00070	-	12.481	-	0.00067

rithm and Shuffled Frog Leaping Algorithm are used to solve this problem. The fitness function minimizes the cost, number of hops and blocking probability. Five different wavelength assignment techniques such as first fit, random, round robin, wavelength ordering and FWM aware priority based wavelength assignment are used while evaluating the performance of GA and SFLA.

In SFLA, better fitness value is achieved compared to GA. Among different wavelength assignment techniques, FWM aware priority based wavelength assignment technique gives maximum average fitness score and least mean execution time. Comparing these optimization algorithms, SFLA is better than GA with minimum mean blocking probability, less mean execution time and better fitness value. SFLA approach has a lower time complexity compared to Genetic Algorithm and hence the proposed scheme may provide certain degree of flexibility in the network design.

6 References

1. A. Adhya and D. Datta, 2009. Design methodology for WDM backbone networks using FWM-aware heuristic algorithm. Optical Switching and Networking, 6: 10–19.
2. C. W. Ahn and R. S. Ramakrishna, 2002. A genetic algorithm for shortest path routing problem and the sizing of populations. IEEE Transactions on Evolutionary Computation, 6: 566–579.
3. A´ lvaro Rubio-Largo, Miguel A. Vega- Rodriguez, Juan A. Gomez-Pulido and Juan M. Sanchez-Pe´rez, 2012. A Comparative Study on Multi objective Swarm Intelligence for the Routing and Wavelength Assignment Problem. IEEE Transactions on systems, man, and cybernetics , 4: 1644–1655.
4. David Bisbal, Ignacio de Miguel and Fernando Gonzalez, 2004. Dynamic Routing and Wavelength Assignment in Optical Networks by Means of Genetic Algorithm. Photonic Network Communications, pp: 43-58.
5. G. Giftson Samuel and C. Christober Asir Rajan, 2014. A Modified Shuffled Frog Leaping Algorithm for Long-Term Generation Maintenance Scheduling. Springer, 258: 11-24.
6. Joan Triay and Cristina Cervello-Pastor, 2010. An Ant-Based Algorithm for Distributed Routing and Wavelength Assignment in Dynamic Optical Networks. IEEE journal on selected areas in communications , 28: 542-552.
7. V. T. Le, X. Jiang, S. H. Ngo and S. Horiguchi, 2005. Dynamic RWA Based on the Combination of Mobile Agents Technique and Genetic Algorithms in WDM Networks with Sparse Wavelength Conversion. IEICE Transactions on Information and Systems, 9: 2067-2078.
8. Muzaffar, Kevin and Fayzul Pasha, 2006. Shuffled frog-leaping algorithm: a memetic meta-heuristic for discrete optimization. Engineering Optimization, 38, 2: 129–154.
9. R. Ramaswami and K.N. Sivarajan, 2000. Optical Networks: A Practical Perspective. Morgan Kaufmann Publishers, San Francisco.
10. D. Srinath and J. Janet, 2013. Secured Ant Colony Optimization Routing for Wireless Network. Asian Journal of Information Technology, 12: 83-90.
11. Urmila Bhanjaa, Sudipta Mahapatra and Rajarshi Roy, 2010. A novel solution to the dynamic routing and wavelength assignment problem in transparent optical networks. International Journal of Computer Networks and Communications, 2: 119-130.
12. Urmila Bhanjaa, Sudipta Mahapatra and Rajarshi Roy, 2012. FWM aware evolutionary programming algorithm for transparent optical networks. Photonic Network Communications, 3: 285-299.
13. Urmila Bhanjaa and Sudipta Mahapatra, 2013. A metaheuristic approach for optical network optimization problems. Elsevier-Applied Soft Computing, 13: 981–997.
14. Urmila Bhanjaa, Sudipta Mahapatra and Rajarshi Roy, 2013. An evolutionary programming algorithm for survivable routing and wavelength assignment in transparent optical networks. Elsevier-Information Sciences, 222: 634–647.
15. X. Wang, M. Brandt-Pearce, and S. Subramaniam, 2014. Distributed Grooming, Routing, and Wavelength Assignment for Dynamic Optical Networks Using Ant Colony Optimization. IEEE/OSA Journal of Optical Communications and Networks, 6: 578-589.
16. Y. S. Kavian ,W. Ren , H. F. Rashvand, M. S. Leeson , M. Naderi and E. L. Hines, 2009. Genetic Algorithm for Designing DWDM Optical Networks under Demand Uncertainty. Proceedings of ICTON Mediterranean Winter Conference, December 10-12, 2009, Angers, pp: 1-4.
17. Yousef S. Kavian, Arash Rashedi, Ali Mahani and Zabih Ghassemlooy, 2013. Routing and wavelength assignment in optical networks using Artificial Bee Colony algorithm. Elsevier-Optik, 124: 1243-1249.
18. Roshni. V. V, R. Hemalatha and R. Mahalakshmi, 2016. Optimization of Routing and Wavelength assignment in passive optical networks. Pak. J. of Biotechnology, Special issue on innovations in information embedded and communication sys-

tems, Vol. 13: 247-251.
19. B. Batagelj, V. Janyani and S. Tomazic, 2014. Research Challenges in optical communications towards 2020 and beyond. Informacije MIDEM, Vol. 44:177-184.
20. M. Vidmar, 2001. Optical-fiber communications: components and systems. Informacije MIDEM, Vol. 31:246-251.

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A New Low-Power CMOS Sample-and-Hold Circuit Based on High-Speed Dynamic Body Biased Switches

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Abstract: In this paper, a low-power open-loop CMOS sample-and-hold (S/H) circuit with improved linearity is presented. The incorporated switches utilize dynamic body connection technique to reduce distortions due to threshold voltage variations during track mode as well as signal feedthrough in the hold mode. To accomplish dual-edge sampling characteristic and differential operation, the proposed S/H circuit utilizes two pairs of the proposed switch and a 2:1 multiplexer. A current mode logic multiplexer without tail current is utilized to reduce power consumption while still fulfilling the speed and linearity requirements. The proposed S/H circuit is designed in a 90-nm CMOS process where it consumes approximately 610 μW from a 1.2 V supply voltage. Post-layout results show that a SFDR of about 73 dB is achieved when sampling a 1 GHz differential sinusoidal input at 2 GS/s rate using both edges of a 1 GHz clock signal.

Keywords: Sample and hold circuits; high-speed switches; body biasing; dual-edge sampling

Novo vzorčevalno vezje nizke moči na osnovi hitrih dinamičnih stikal

Izvleček: Članek opisuje odprtozančno CMS vzorčevalno vezje nizke porabe z izboljšano linearnostjo. Vgrajena stikala vnašajo dinamično povezovalno tehniko za zmanjševanje distorcij pri nihanju pragovne napetosti v načinu sledenja, kakor tudi prenos signala v stanju zadržanja. Za zagotaljanje dvorobne vzorčevalne karakteristike in diferencialnega delovanja sta v predlaganem vzorčevalnem S/H vezju uporabljena dva para stikal in 2:1 multiplekser. V tokovnem načinu je uporabljen logični multiplekser za zniževanje porabe energije, pri čemer se hitrost in linearnost ohranjata. Predlagano S/H vezje je načrtano v 90 nm CMOS tehnologiji in pri napajalni napetosti 1.2 V porabi okoli 610 μW. Rezultati izkazujejo 73 dB SFDR pri vzorčenju z 2 GS/s in difenecialni sinusni vzorčevalni frekvenci 1 GHz.

Ključne besede: vzorčevalna vezja; stikala velikih hitrosti; dvorobno vzorčenje

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1 Introduction

High speed sample-and-hold (S/H) circuits have found many applications in emerging communication systems such as software defined radio, direct RF sampling receivers and sub-sampling RF architectures [1-3]. The S/H circuits are substantially classified into two main groups of closed-loop and open-loop configurations. There is a main trade-off between linearity and speed in both types. Closed-loop S/Hs [4], [5] are more linear than open-loop counterparts while open-loop S/Hs [6-8], on the other hand, have relatively higher speed, less power consumption and less circuit complexity [7]. However, in very high speed applications, distortions imposed by embedded switches seriously limit their application. Charge injection and signal feedthrough, in the hold mode, beside threshold voltage variation due to body effect along with amplitude and phase distortion due to finite channel resistance, in the track mode, are blamed as the main sources of distortions [9], [10].

Transmission gates implemented by parallel connection of PMOS and NMOS transistors are the simplest way to implement a CMOS switch. However, the unequal turn-on and turn-off delays of PMOS and NMOS transistors makes them suitable only for applications with moderate precisions especially when fast switching operation is required [11]. A vast varieties of boot-

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strap switches have been reported as linear and high-precision switches [12-14]. However, due to their circuit complexity and thus relatively lower speeds, they are not applicable in high speed applications. In this paper, a low-power high-speed sample-and-hold (S/H) circuit is proposed which takes the advantage of dynamic body connection technique to improve the linearity and speed of the incorporated switches. The paper is organized as follows; Section 2 illustrates the operation and analysis of the employed CMOS switches in details and then illustrates the implementation of the proposed S/H circuit. The results and discussion are provided in Section 3 followed by the conclusion in Section 4.

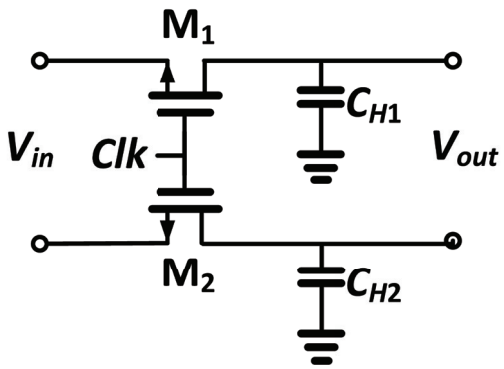


Figure 1: A simple differential CMOS switch

2 Proposed S/H circuit

Shown in Fig. 1, a simple differential switch can be realized using a pair of nMOS (or pMOS) transistors M_1, M_2 and holding capacitors C_{H1}, C_{H2}. When the switch is conducting (Clk=1), the transistors are in deep triode region and exhibit a channel resistance of:

$$R_{ON} = \frac{1}{\mu_n C_{ox} S (V_{GS} - V_{th})} \quad (1)$$

where μ_n is the electron mobility, C_{ox} is the gate-oxide capacitance, S denotes the transistor's aspect ratio and V_{GS} and V_{th} are gate-source voltage and threshold voltage, respectively. Reducing both R_{ON} and C_H results in better speed performance, however, a small C_H will significantly increases the impact of signal feedthrough on the sampled values leaving R_{ON} as the main means for alleviating the speed constraints. The simple switch shown in Fig. 1 also imposes phase and amplitude distortion during track mode mainly due to non-negligible switch resistance which can be evaluated as

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{1}{\sqrt{(\tau\omega)^2 + 1}} \exp\left(-j \tan^{-1} \tau\omega\right) \quad (2)$$

where $\tau = R_{ON} C_H$ is the switch time constant.

Charge injection and clock feedthrough are other sources of distortion in CMOS switches. Methods such as differential design and using dummy transistor have been suggested [11] to mitigate these problems. However, in the case of differential design, each side of the differential switch receives different input voltage, which causes unequal impact of charge injection and clock feedthrough on each side that cannot be totally removed in a common mode scheme. Moreover, process-related variations also worsen the problem so that charge injection and clock feedthrough always partially impose inevitable residues at the output.

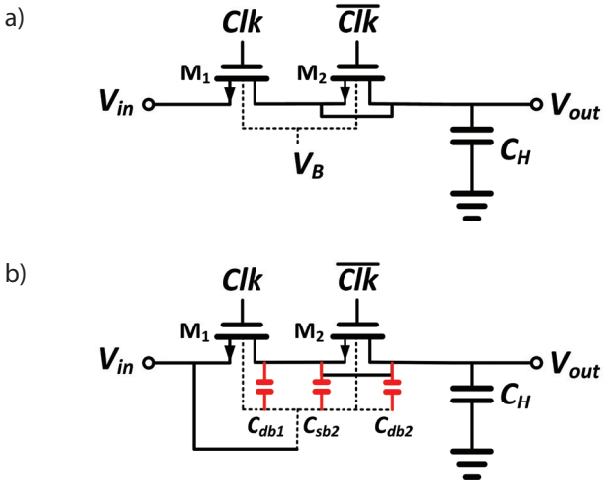


Figure 2: (a) MOS switch with constant body bias, (b) Signal feedthrough via parasitic capacitances when the body is connected to the source.

Shown in Fig. 2(a), to reduce the effects of non-idealities, there is benefits to using body-biasing technique. It is well-known that by applying a bias voltage to the bulk terminal of a MOS transistor, the threshold voltage decreases, which according to (1) and (2), lightens the amplitude and phase distortion. Obviously, the body bias voltage, V_B, should be applied to both switch transistor (M_1) and the dummy transistor (M_2) as it should be noted that an appropriate value for V_B, which allows for maximum input dynamic range with a symmetrical swing of at most 0.5 V, is the common-mode level of the input signal V_{in}. However, a problem which arises with applying a constant body bias to the bulk is that since the source-bulk voltage (V_{sb}) of switch transistor varies with V_{in}, its threshold voltage depends on the input signal, acting as a main cause of distortion. This problem can be solved by connecting the bulk terminal to the source instead of connecting it to a constant voltage of V_B. Nonetheless, an advantage of applying a positive voltage to the bulk, in comparison to tying the bulk to the source, is preventing the input signal to leak

to the output through drain-bulk parasitic capacitance in the hold mode. To elaborate more on this issue, Fig. 2(b) schematically illustrates this problem indicating that the ratio of the leaked signal to the output is

$$\frac{V_{out}}{V_{in}} = \frac{C_1}{C_1 + C_H} \tag{3}$$

where $C_1 = C_{BD1}+C_{BS2}+C_{BD2}$ in which C_{BD} and C_{BS} are drain-bulk and source-bulk parasitic capacitances, respectively, so that subscripts 1 and 2 associate the parameters to M_1 and M_2, respectively. The both mentioned problems of the threshold voltage variation of constant-body-biased switches and signal feedthrough of switches with their body connected to the source can be effectively solved using body-bias control circuit first introduced in [15], and modified and then called here as dynamic body bias (DBB) switch. Shown in Fig. 3, the M_3 connects the body terminal of M_1 to its source terminal during track mode thus preventing threshold voltage variation due to the body effect. During hold mode, M_3 turns off disconnecting M_1 body node from its source node avoiding signal feedthrough through drain-bulk parasitic capacitance.

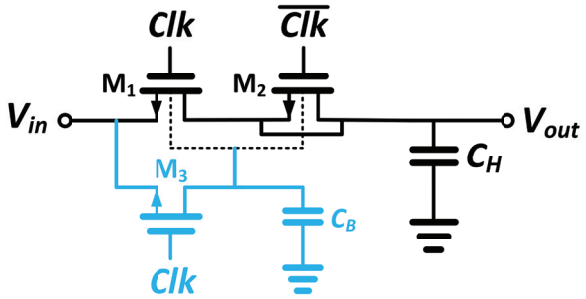


Figure 3: MOS switch with dynamic body connection technique. M3 connects the body nodes to the input to prevent distortion due to threshold voltage variation.

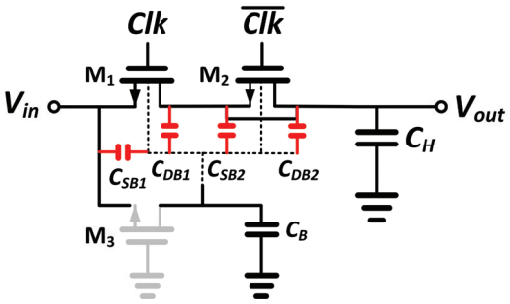
To analyze the feedthrough issue in the proposed DBB switch during hold mode (Clk=0), Fig. 4(a) shows how a capacitive coupling path between input and output is constructed by the parasitic capacitances of the M_1 and M_2 The equivalent circuit of the parasitic path is shown in Fig. 4(b) where the amount of feedthrough can be expressed by

$$\frac{V_{out}}{V_{in}} = \frac{C_{BS1}.C_1}{C_B\left(C_1 + C_H\right) + C_H\left(C_{BS1} + C_1\right) + C_{BS1}.C_1} \tag{4}$$

Since C_B and C_H are sufficiently larger than C_{BS1} and C_1, (4) simplifies to

$$\frac{V_{out}}{V_{in}} \approx \frac{C_{BS1}}{C_B}\frac{C_1}{\left(C_1 + C_H\right)} \tag{5}$$

a)



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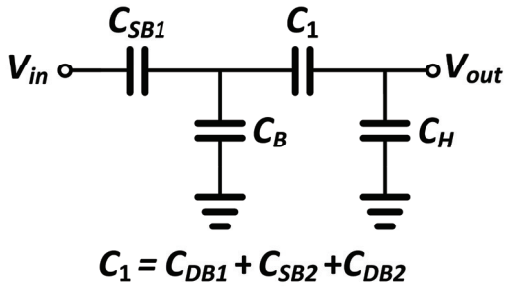


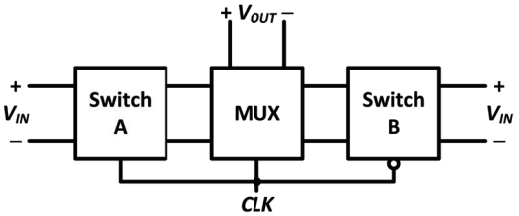
$$C_1 = C_{DB1} + C_{SB2} + C_{DB2}$$

Figure 4: (a) The signal feedthrough via parasitic capacitances of the proposed switch, (b) equivalent circuit of the parasitic path.

Comparing (5) with (3), the amount of feedthrough has been considerably reduced by a factor of C_{BS1}/C_B.

The dual edge triggered S/H circuit is realized using a pair of the proposed switch in differential configuration and a 2:1 multiplexer (MUX) circuit as conceptually illustrated in Fig. 5(a). The circuit is designed fully differential to improve its performance against common-mode distortions as well as supply and substrate noises [16]. Fig. 5(b) depicts the schematic circuit of

a)



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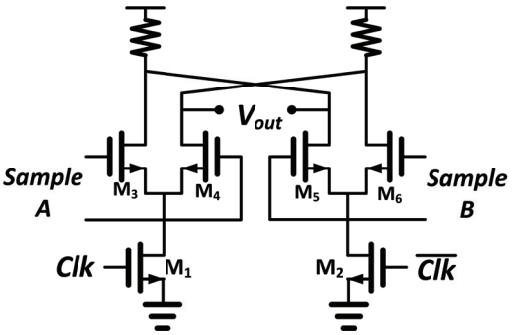

Figure 5: (a) The block diagram of the proposed dual-edge triggered S/H, (b) schematic circuit of the 2:1 CML MUX.

the incorporated 2:1 MUX. A high-speed current mode logic (CML) MUX without any specific tail current is utilized. The reason is to reduce the number of stacked transistors allowing for higher output swing. The M_1 and M_2 operate as current switches working in deep triode region (when turned on) with a small drain-source voltage. In addition, since higher voltage headroom is now available for M_3-M_6, their transconductances can be higher. In other words, we can reduce the sizes of these transistors while still having the same value of g_m comparing to the case with a specific tail current. Thus, the parasitic capacitances are reduced resulting in an improved speed.

Fig. 6(a) shows the structure of the proposed S/H circuit. The operation of the circuit is as follows. On the rising edge of the Clk, the switches B1 and B2 turn off providing a sample of the input signal at their output. At the same time, the switches A1 and A2 are conducting and track the input signal. On the falling edge of the Clk, the input will be sampled by the switches A1 and A2. Thus, on each clock edges a sample of the input is provided and thus the 2:1 MUX can choose the samples on each proper switch output. The circuit implementation of the proposed S/H circuit is shown in Fig. 6(b). Each differential switch is implemented using a pair of DBB switch where no explicit holding capacitor (i.e. C_H and C_B) is utilized. In fact, parasitic capacitances of the associated circuit nodes are sufficient for holding the samples over a short time.

a)

b)

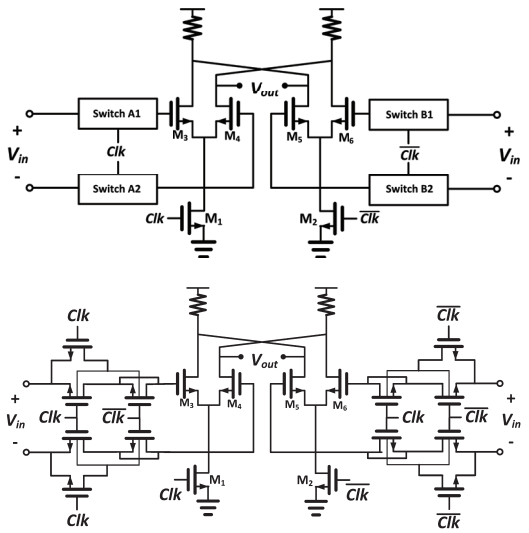

Figure 6: (a) The structure of the proposed S/H circuit, (b) The schematic circuit of the proposed dual-edge triggered S/H circuit.

3 Simulation results

The proposed S/H circuit is implemented in a 90 nm CMOS process and post-layout simulations are carried out with a 1.2 V supply voltage while it consumes about 610 µW. To evaluate the performance of the switches, Fig. 7 compares the outputs of the switch with constant body bias (CBB) (shown in Fig. 2(a)) and the switch with dynamic body bias (DBB) (depicted in Fig. 3) when taking samples from a 500 MHz sinusoidal input having 200 mV amplitude (over 0.5 V common mode level). Their sampled values include an error voltage of about 12 mV and 7.5 mV, respectively. The dynamic body bias switches offer higher speed and less distortion.

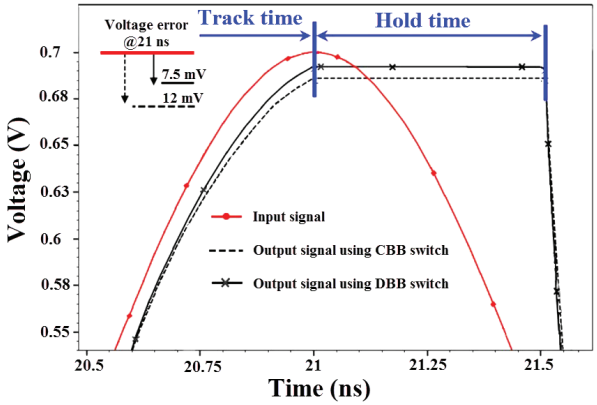

Figure 7: Comparison of samples taken by constant body bias (CBB) and dynamic body bias (DBB) switches.

Fig. 8 indicates the SFDR of the proposed S/H circuit employing various switches, i.e. the simple switch (shown in Fig. 1) and the CBB and DBB switches, supposing a differential sinusoidal waveform with 0.2 V amplitude is applied to the inputs sampled at a rate of 2 GS/s. The SFDR at Nyquist rate when incorporating the proposed DBB switch is about 73 dB. If using CBB switch the SFDR drops to about 69 dB. For the sake of comparison, the SFDR if using simple nMOS switch is also shown that is about 48 dB. Obviously, the circuit that benefits from

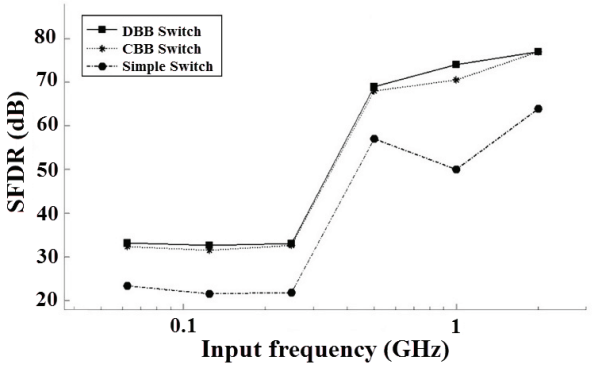

Figure 8: SFDR of the proposed S/H circuit versus input frequency incorporating different switches.

proposed switch achieves better SFDR since threshold voltage variations are reduced.

Table 1: Performance summary of the proposed dual edge triggered S/H circuit and its comparisons with some prior work

Design	This work	Ref. 3	Ref. 6	Ref. 8	Ref. 5	Ref. 7	
Technology	90 nm	90 nm	0.35 µm	0.18 µm	0.35 µm	0.18 µm	0.35 µm
Sampling rate	2 GS/s	~810 MS/s	250 MS/s	200 MS/s	400 MS/s	500 MS/s	250 MS/s
Supply voltage	1.2 V	1.2 V	_	1.8 V	2 V	_	_
Power consumption	610 µW	-	_	12.5 mW	6.7 mW	_	_
SFDR	73dB@ 1GHz	27.3dB* @ ~20GHz	_	76dB@200MHz	_	_	_
Configuration type	Open-loop	Open-loop	Open-loop	Open-loop	Closed-loop	Open-loop	Open-loop

The output of the circuit in response to a 1.25 GHz sinusoidal input sampled at a rate of 5 GS/s is also shown in Fig.9. The delay from the clock edges to the time that the samples settle at the output implies that the whole circuit has less than 0.1 ns delay from input to the output. Table 1 shows the proposed S/H circuit performance summary and its comparison with other recently published CMOS realizations. The circuit do not have static power consumption and the input switches are fully passive without extra power consumption causing the overall circuit to operate with a lower power. The ability of the circuit to operate at a relatively high sampling rate mainly comes from appropriate MUX architecture and the optimized switches.

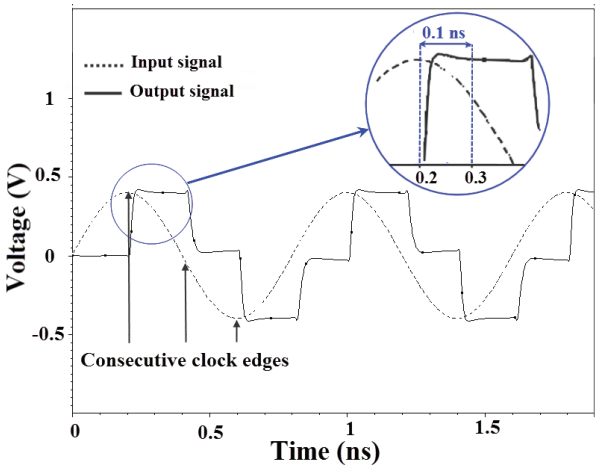

Figure 9: Sampling a 1.25 GHz sinusoidal input at a rate of 5 GS/s using a 2.5 GHz clock signal.

4 Conclusion

In this paper, a new architecture for open-loop S/H circuits was presented providing higher precision in sampling. The switches were optimized using dynamic body bias technique in order to reduce distortions. It utilizes a CML multiplexer at the output operating in a switching manner as a means for dual edge sampling. The proposed S/H has some advantages compared to other open-loop counterparts, such as low complexity, low-power operation and fully differential configuration.

5 References

1. R. Bagheri *et al.*, "An 800-MHz–6-GHz Software-Defined Wireless Receiver in 90-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2860-2876, Dec. 2006.
2. M. Motoyosh, T. Koizum, T. Maehata, S. Kameda and N. Suematsu, "High SNR CMOS S/H IC for multi-carrier direct RF under sampling receiver," *2016 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Taipei, 2016, pp. 1-3.
3. J. Cheng, N. Qi, P. Y. Chiang and A. Natarajan, "A Low-Power, Low-Voltage WBAN-Compatible Sub-Sampling PSK Receiver in 65 nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3018-3030, Dec. 2014.
4. T. Koizumi *et al.*, "A CMOS series/shunt switching type S/H IC for Ka-band direct RF under sampling receiver," *Asia-Pacific Microwave Conference (APMC)*, Nanjing, 2015, pp. 1-3.
5. T. S. Lee, C. C. Lu, S. H. Yu, and J. T. Zha, A very-high-speed low-power low-voltage fully-differential CMOS sample-and-hold circuit with low hold pedestal, *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)* (2005), pp. 3111-3114.
6. M. Mousazadeh, K Hadidi, and A. Khoei, A novel open-loop high-speed CMOS sample-and-hold. *AEU-Int. Journal of Electronics and Communications.* 62 (2008) 588-96.
7. K. D. Sadeghipour, A new passive sample and hold structure for high-speed, high-resolution ADCs. *AEU-Int. Journal of Electronics and Communications*. 65 (2011) 799-805.

8. A. Shirazi, S. Mirhaj, S. Ashtiani, and O. Shoaei, Linearity improvement of open-loop NMOS source-follower sample and hold circuits, *IET Circuits, Devices & Systems*. 5 (2011) 1-7.
9. M. Hasan-Sagha, and M. Jalali, Very high speed and low voltage open-loop dual edge triggered sample and hold circuit in 0.18 µm CMOS technology, *Proc. IEEE Int. Conf. Semiconductor Electronics (ICSE)* (2012), pp. 645-648.
10. A. Boni, A. Pierazzi, and C. Morandi, A 10-b 185-MS/s track-and-hold in 0.35 µm CMOS, *IEEE J. Solid State Circuits.* 36 (2001) 195-203.
11. D. Jakonis, and C. Svensson, A 1GHz linearized CMOS track-and-hold circuit. *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)* (2002) pp. 1265-1277.
12. B. Razavi, Design of Analog CMOS Integrated Circuits (McGraw-Hill, New York, 2016).
13. C. J. B. Fayomi, G. W. Roberts and M Sawan, Low voltage CMOS analog bootstrapped switch for sample-and-hold circuit: design and chip characterization, *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)* (2005) pp. 2200-2203.
14. K. Ohhata, K. Yayama, Y. Shimizu and K. Yamashita, A 1-GHz, 56.3-dB SFDR CMOS track-and-hold circuit with body-bias control circuit, *Journal of IEICE Electronics Express*. 4 (2007) 701-706.
15. G. Huang and P. lin, A fast bootstrapped switch for high-speed high-resolution A/D converter, *Proc. IEEE Asia Pacific Conf. Circuits and Systems* (2010) pp. 382-385.
16. K. Ohhata, K. Yayam, Y. Shimizu and K. Yamashita, A 1-GHz, 56.3-dB SFDR CMOS track-and-hold circuit with body-bias control circuit, *Journal of IEICE Electronics Express* 4 (2007) 701-706.
17. H. Movahedian, B. Sedighi and M. S. Bakhtiar, Wide-range single-ended CMOS track-and-hold circuit, *Journal of IEICE Electronics Express* 4 (2007) 400-405.

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An Improved Low Phase Noise LC-VCO with Wide Frequency Tuning Range Used in CPPLL

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Abstract: Based on TSMC 0.18μm CMOS process, a complementary cross-coupled differential LC voltage controlled oscillator (LC-VCO) used in charge pump phase-locked loop (CPPLL) frequency synthesizer for satellite receiver with low phase noise and wide frequency tuning range is designed and implemented. The VCO adopts self-bias structure to remove flicker noise produced by tail current. Programmable LC tanks are introduced at the common source of cross-couple transistors to eliminate second harmonics of resonant frequency. Distributed biasing is applied for a wider linear tuning range. An optimized switch is proposed to lower on-resistance. The measured results show that the VCO exhibits a 53.8% tuning range from 1.02GHz to 1.77GHz. From the carrier frequency of 1.4 GHz, the phase noise of the VCO can reach -131.2 dBc/Hz at 1MHz offset. The core circuit consumes 7.7mA with 1.8V supply voltage.

Keywords: low phase noise; wide tuning range; distributed biasing; optimized switch

Izboljšan LC-VCO z nizkim faznim šumom in širokim področjem nastavljanja frekvence za uporabo v PLL s črpalko nabojev

Izvleček: Razvit in uporabljen je bil komplementarni sklopljen difencialni LC napetostno krmiljen oscilator (LC-VCO) za uporabo v frekvenčnem sintetizatorju s fazno-skelnjeno zanko (PLL) s črpalko nabojev, namenjen uporabi v satelitskih sprejemnikih z nizkim faznim šumom in širokim področjem nastavljanja frekvenc. Izveden je v TSMC 0.18 um CMOS tehnologiji. VCO uporablja samonapajalno strukturo za izničenje šuma 1/f, ki bi ga povzročal tokovni vir. Za izločanje drugega harmonika frekvence so uvedene nastavljive LC zapore na skupnem viru napajanja križno sklopljenih tranzistorjev. Za širšo območje nastavljanja je uporabljeno porazdeljeno napajanje uglaševalnih varaktorjev. Rezultati izkazujejo 53.8% nastavljivo območje VCOja med 1.02 GHz in 1.77 GHz. Pri nosilni frekvenci 1.4 GHz in odmiku 1 MHz lahko fazni šum VCO doseže -131.2 dBc/Hz. Pri napajalni napetosti 1.8 V jedro vezja porablja 7.7 mA.GHz.

Ključne besede: nizek fazni šum; široko območje nastavljanja; porazdeljeno napajanje; optimizirano stikalo

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1 Introduction

Frequency modulation is widely used in communication system especially for long distance communication. A wide utilization of frequency synthesizer in the RF system makes it possible to generate an accurate frequency signal for frequency modulation [1]. In the RF system, noise produced by frequency synthesizer directly deteriorates the overall noise performance of the system [2]. Meanwhile, the VCO is one of the major contributors of the out-of-band noise in a PLL frequency synthesizer [3]. Thus, to design a low phase noise VCO is necessary and significant for a high performance communication system, which is a challenge for us in consideration of tuning range, power consumption and other characteristics.

With a mature understanding of phase noise mechanism [4]-[6], many attempts to optimize phase noise of VCO have been made in recent years. In reference [7], switchable cross-coupled pairs are used for lower transconductance and thereby improve $1/f^3$ noise. However, as a result, the complexity of the timing logic is inevitably increased. In order to prevent the *Q*-factor degradation of resonant tanks in VCO, MOS switches

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featuring high off-on resistance ratio (R_{OFF}/R_{ON}) are used, and transistors with large gate width are introduced to achieve a sufficiently low R_{ON}. However, the C_{OFF} associated with such wide transistors will cause serious performance degradation [8, 9].

This paper introduce how VCO contribute phase noise to CPPLL, presents a complementary cross-coupled differential *LC*-VCO that can achieve low phase noise and large frequency tuning range. Self-bias structure is applied to remove flicker noise produced by tail current. Programmable *LC* tanks are introduced at the source of cross-coupled transistors to eliminate second harmonics of resonant frequency. Distributed biasing is adopted to widen the linear tuning range of every selected band. The switches used in the design have been optimized to enhance the *Q*-factor. The presented VCO is fabricated using TSMC 0.18μm CMOS technology, measurement of which is performed for validation.

2 CPPLL noise analysis

We choose CPPLL rather than others for its stability and larger acquisition range. A brief block diagram of the CPPLL is shown in Fig. 1. Phase/frequency detectors (PFD) sense phase and frequency differences between reference clock signal and output of divider. Charge pump sinks or sources current for a limited period of time according to the voltage produced by the previous PFD. The loop filter (consisting of R_1, C_1 and C_2) following CP produces voltage which controls VCO. The low dropout regulator (LDO) supplies for the VCO. The frequency divider (FD) between VCO output and PFD input makes a feed-back loop to ensure that output signal frequency is independent of process, supply voltage, temperature and other interferences.

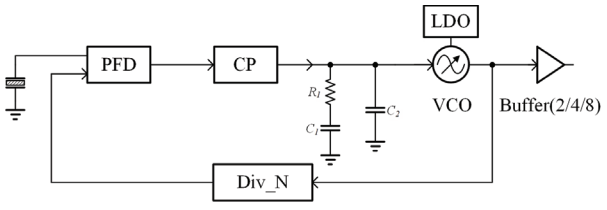


Figure 1: CPPLL block diagram.

To formulate the CPPLL output phase noise contributed by VCO, we need to derive the transfer function from the VCO phase to the CPPLL output phase. Although CPPLL is a nonlinear system, in the vicinity of lock state we can make a linear approximation in phase domain for intuitive understanding. A linear model is constructed in Fig. 2, where $\frac{I_p}{2\pi}\left(R_1+\frac{1}{sC_1}\right)//\frac{1}{sC_2}$, $\frac{K_{VCO}}{s}$ and $\frac{1}{N}$ represent CP, VCO and FD respectively.

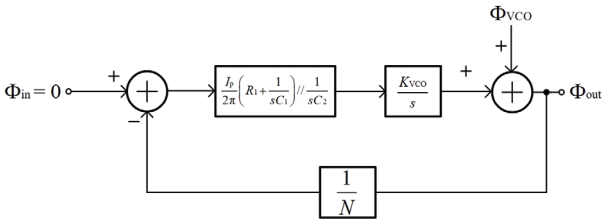


Figure 2: Phase-domain linear model for deriving VCO's effect on CPPLL phase noise

In order to analyze VCO's effect, we make $\Phi_{in} = 0$ to signify that reference clock signal is noiseless. Starting from the output, we have:

$$-\frac{\phi_{out}}{N}\left[\frac{I_p}{2\pi}\left(R_1+\frac{1}{sC_1}\right)//\frac{1}{sC_2}\right]\cdot\frac{K_{VCO}}{s}+\phi_{VCO}=\phi_{out} \quad (1)$$

Equation （1） allows us to derive phase transfer function from VCO to PLL output as :

$$\frac{\phi_{out}}{\phi_{VCO}}(s)=\frac{s^3+\frac{C_1+C_2}{R_1C_1C_2}\cdot s^2}{s^3+\frac{C_1+C_2}{R_1C_1C_2}\cdot s^2+\frac{1}{N}\cdot\frac{I_pK_{VCO}}{2\pi C_2}\cdot s+\frac{1}{N}\cdot\frac{I_pK_{VCO}}{2\pi R_1C_1C_2}} \quad (2)$$

The transfer function contains two zeros at the origin and one zero near origin, three poles on the right of the zeros, exhibiting a high-pass behavior. The VCO phase noise is shaped by the transfer function. It can be proved that the phase noise out of loop bandwidth follows VCO's phase noise [3].

Taking other noise sources (reference clock, PFD, CP, FD and etc.) into consideration, we can make a conclusion that PLL's output phase noise measured at high offset frequencies is worse than VCO's.

3 Circuit Design

The theories to derive the phase noise of VCO have been researched for many years. Based on the derivation in [10], the theory proposed by D.B. Leeson [4], which can make a qualitative prediction about the phase noise is described in equation (3):

$$L\{\Delta f\}=10\cdot\log\left\{\frac{FkT}{2P_s}\cdot\left[1+\left(\frac{f_0}{2Q_L\Delta f}\right)^2\right]\cdot\left(1+\frac{\Delta f_{1/f^3}}{\Delta f}\right)\cdot 1\text{Hz}\right\} \quad \text{[dBc/Hz]} \quad (3)$$

where *F* is the noise figure of the active device used under large signal conditions in this design, *k* is Boltzmann's constant in Joules/Kelvin, *T* is the temperature in Kelvin, P_s is the average power dissipated in the resistive part of the tank in Watt, f_0 is the carrier frequency

(Hz), Q_L is the effective quality factor of the tank, Δf is the offset frequency (Hz) from the carrier and $\Delta f_{1/f^3}$ is the frequency (Hz) of the corner between the $1/f^3$ and $1/f^2$ regions. The corner frequency of the semiconductor process we used in the design is about 20 kHz, which means $\Delta f_{1/f^3}$ is about 20 kHz.

In this design, guided by equation (3), the *LC*-VCO with optimized phase noise is presented, the core schematic of which is shown in Fig. 3.

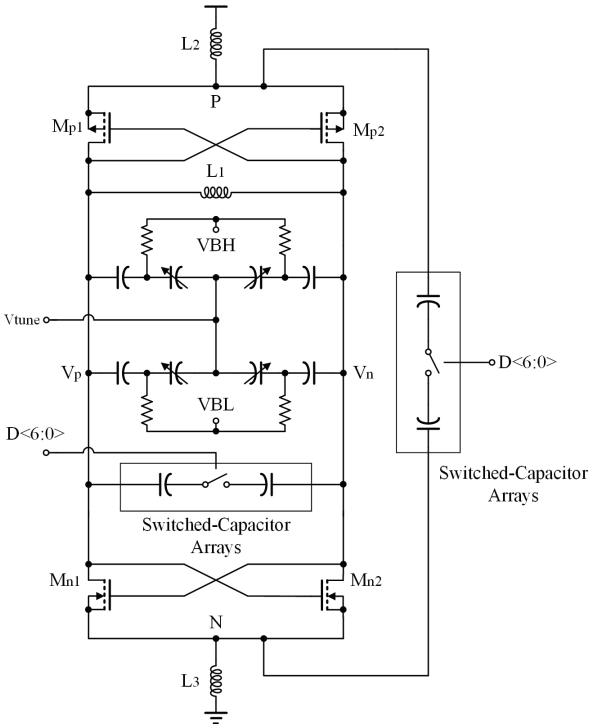


Figure 3: The proposed VCO core schematic.

There is no current source in the schematic, so the flicker noise due to current source can be removed totally. A complementary cross-coupled structure is adopted rather than only a cross-coupled structure because the structure can produce twice the voltage swing for a given current and inductor design, which can reduce phase noise according to equation (3). The direct-current operating points are determined by diode-connected MOS transistors between power and ground provided by LDO which can reduce VCO's sensitivity to supply voltage. MOS transistors here are used to work as negative resistor, cancelling loss in the LC tank due to parasitic resistance of inductor, capacitor and others. In this design, the parameters of PMOS and NMOS are set to produced symmetric output swing by simulation iteration operation for a given frequency range, which benefits phase noise optimization [11]. The parameter of main components in VCO is shown in Table 1.

Table 1: Parameters of main components in VCO

Components	Parameter	Value
L_1	Inductance[nH]	2.95
$L_2(L_3)$	Inductance[nH]	1.69
$Mn_1(Mn_2)$	W/L[μm/μm]	32*(2/0.2)
$Mp_1(Mp_2)$	W/L[μm/μm]	32*(6/0.2)

There are two 7-bit binary-weighted switched capacitor arrays controlled by the same digital codes, D<6:0>, in the proposed topology. For a compromise of the linearity and layout area, the codes are implemented with a segmented architecture, in which the 2 LSBs are implemented using a binary architecture while the 5 MSBs are implemented in a unary way. The capacitor array in parallel with L_1 is proposed to extend the tuning range instead of increasing VCO gain, which can realize coarse tuning. The other connected between nodes P and N is in parallel with L_2 and L_3, whose purpose is to compose a narrow band circuit for resonance at second harmonic, preventing the degradation of the *Q*-factor of the tank when the transistors operate in the triode region [12]. We choose programmable switched capacitors between nodes P and N rather than a fixed capacitor because we can choose appropriate resonant frequency according to the band selection.

In order to perform the fine tuning of VCO with a wide linear range, distributed MOS varactor biasing is applied [13].The varactor we used in the design is accumulation-mode MOS varactor, which is shown in Fig. 4 (a). This structure is obtained by placing an NMOS transistor inside an n-well. If $V_G<V_S$, then electrons in the n-well are repelled from silicon/oxide interface and a depletion region is formed. Under this condition, the capacitance seen from the gate is given by the series combination of the oxide and depletion capacitance. As V_G exceeds V_S, the interface attracts electrons from the n^+ source/drain terminals, creating a conduction channel. As a result, the total capacitance seen from the gate rises to that of the oxide. The *C/V* characteristics of the varactor is shown in Fig. 4 (b). The linear range of the structure is limited. To solve this problem, we shunt two varactors in parallel with two different voltage bias, VBH and VBL, which is shown in Fig. 3. The *C/V* characteristics of distributed biasing varactors is shown in Fig. 5. Compared to the conventional structure whose varactor is biased by a single reference voltage, this design can achieve almost twice linear range. As a consequence, we can enlarge tuning range of every selected band and reduce the VCO gain for a given frequency range, which makes a good trade-off between phase noise and tuning range.

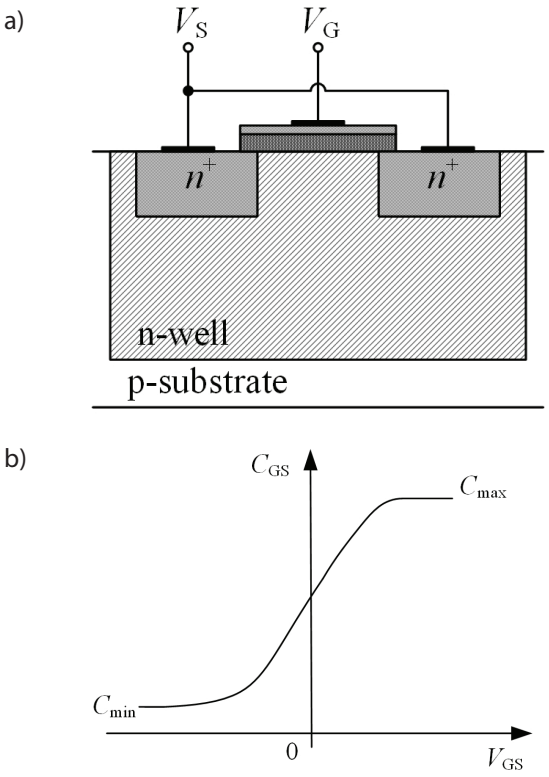


Figure 4: (a) MOS varactor, (b) resulting *C/V* characteristic of the varactor

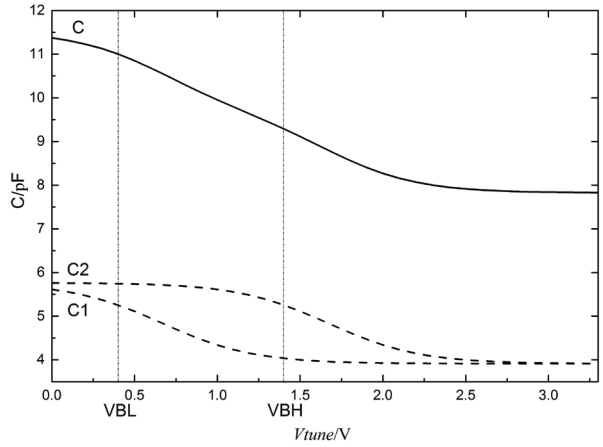


Figure 5: *C/V* characteristic of the varactors with distributed biasing

Another issue should be paid attention to is the design of the switch used in capacitor arrays, which concerns the *Q*-factor of the *LC* tank. We hope the switch is ideal, but the parasitic effect and voltage swing between the switch make it hard to implement an ideal switch. There is a trade-off in the design of switch size. To realize high quality of capacitor when the switch is on, we need large size switch to minimize the on-resistance. To minimize parasitic capacitance of the switch when the switch is off, we need to design small size switch MOS transistor to degrade C_{gs} and C_{gd}. A conventional structure is shown in Fig. 6 (a), where the on-resistance is introduced by MOS switch. Ideally, the switch transistor is in deep triode region when the switch is on. The resistor is equal to

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{4}$$

However, the voltage swing appearing at source of the MOS switch may drive it out of the region. As a result, the on-resistance varies along with the output voltage swing of the VCO, which will deteriorate the phase noise of the VCO. To solve the problem, an optimized structure is used in this design as described in Fig. 6 (b). Since the structure is symmetrical with differential voltage swing, node A is ac ground here. When the switch is on, the common source of the two transistor experiences little voltage swing and the on-resistance almost keeps a constant consequently. Additionally, when the switch is off, the optimized structure is switched off more thoroughly and introduces almost half parasitic capacitance if the switch sizes are equal in the two structures.

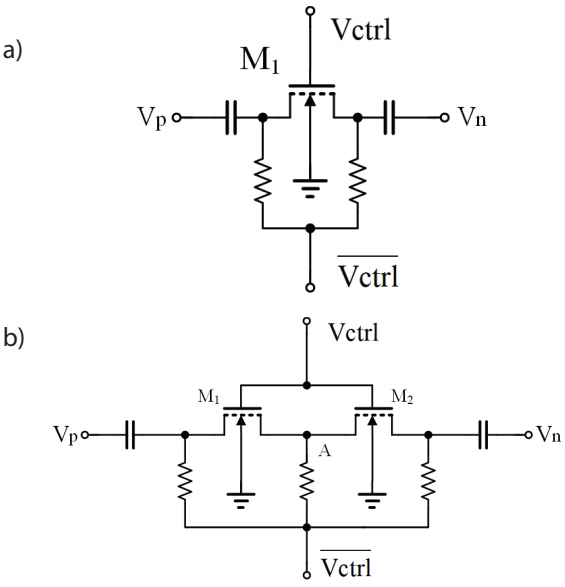


Figure 6: (a) a conventional switch (b) an optimized switch

4 Implementation and Measurements

This proposed low phase noise VCO is integrated in a receiver which is fabricated using TSMC 0.18μm CMOS technology. In our frequency synthesizer, the VCO output is divided by a divide-by-2 quadrature frequency divider to generate quadrature local oscillating (LO)

signal for quadrature down conversion. After the divider, an output buffer is adopted for testing. According to the system requirement, the loop bandwidth of the frequency synthesizer is set to 100 kHz. Fig. 7 shows a micrograph of the proposed VCO, occupying an area of 820*1080μm^2.

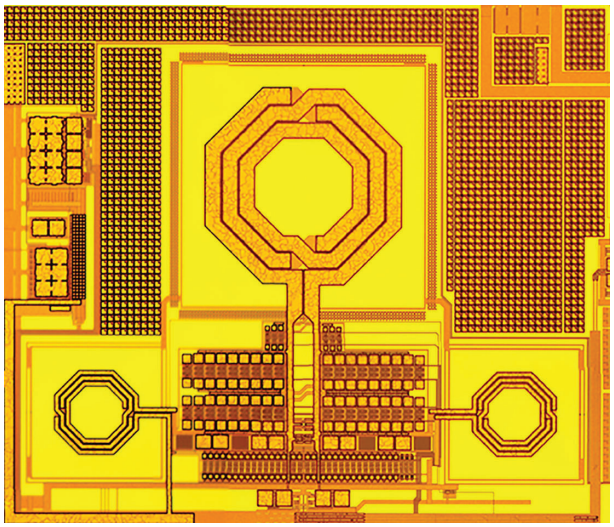


Figure 7: Micrograph of proposed VCO.

An Agilent E5052B signal source analyzer is used to measure the synthesizer parameters in the test. The *f* -V tuning characteristic of the VCO is shown in Fig. 9 (a). The VCO achieves a tuning range of 53.8% from 1.02 GHz to 1.77 GHz. Fig. 9 (b) shows the phase noise measured at the carrier frequency of 700 MHz. The measured result is -104.3 dBc/Hz at 100-kHz offset and -135.6 dBc/Hz at 1-MHz offset respectively. The VCO phase noise is -98.3 dBc/Hz at 100-kHz and -129.6 dBc/Hz at 1-MHz offset respectively after adding 6 dB, while consuming current of 7.7 mA from a supply voltage of 1.8V. Fig. 9 (c) shows phase noise performance across the VCO frequency range at 1 MHz offset, which confirms the VCO has a good noise performance in the entire frequency range. In contrast, Fig. 8 shows the simulation result of the free running VCO at the carrier frequency of 1.4 GHz, which is close to the test result at 1 MHz offset.

A figure-of-merit (FOM) is employed to evaluate the four performance parameters of the VCO: frequency, phase noise, power consumption and frequency tuning range [14], which can be expressed as:

$$\mathrm{FOM_T}=20\log\frac{f_o}{\Delta f}-10\log\frac{P}{1\mathrm{mW}}-\mathrm{PN}+20\log(\mathrm{FTR}/10) \quad (5)$$

$$\mathrm{FTR}=[(f_{max}-f_{min})/f_c]\times 100\% \quad (6)$$

Where f_o is the oscillation frequency, f_{max}, f_{min} are the maximal, minimal operation frequency, respectively, f_c is the center oscillation frequency, Δf is the offset frequency, P is power dissipation valued in mW, and PN is the phase noise valued in dBc/Hz.

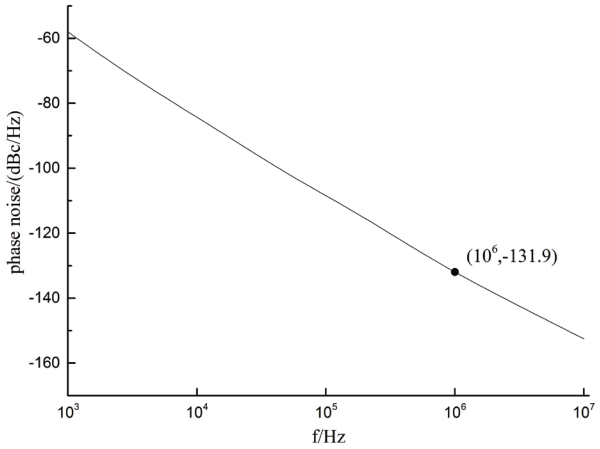


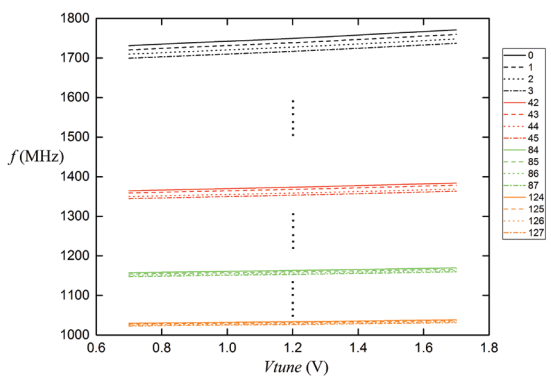
Figure 8: free running VCO output phase noise simulation result at 1.4 GHz

Based on the measured results above, Table II summarizes the measured performance comparison of the VCO in this work with other recent state-of-the-art VCOs in published literatures. The wide frequency tuning range with the proposed scheme shows better performance than the *LC*-VCO in [8] and the two *LC*-VCOs in [9] which have ordinary phase noise performance at higher oscillation frequency with higher power consumption. The *LC*-VCO reported in [7] has lower power

Table 2: Performance comparison CMOS VCO

Ref	CMOS process (nm)	Power (mW)	Tuning range (GHz)	fc (GHz)	Phase noise (dBc/Hz)	FoMT (dBc/Hz)
[7]	65	8	1.6~2.6	2.1	-124@1MHz	195.0
[8]	90	23	2.55~4.08 4.9~5.75	2.1	-126@1MHz -125@1MHz	192.1 181.9
[9]	180	18	1.35~2.05 2.05~2.75	1.7 2.4	-122@1MHz -119.5@1MHz	186.3 183.8
This work	180	14	1.02~1.77	1.4	-129.6@1MHz	195.7

a)



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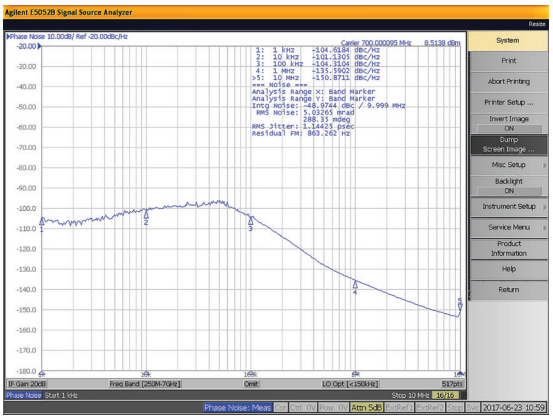

c)

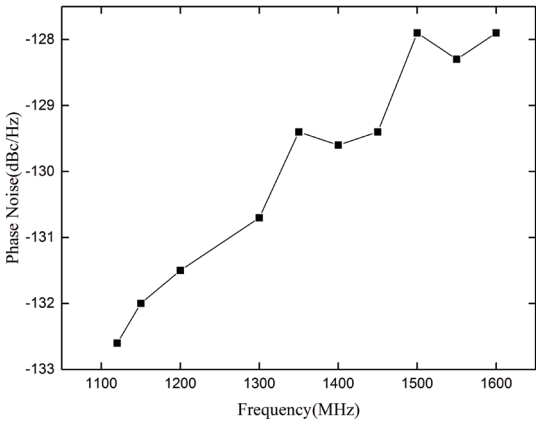

Figure 9: (a) f-V tuning characteristic refers to the 7-bit binary-weighted digital codes, D<6:0>,(b) PLL output phase noise measured at 700MHz, (c)phase noise performance across VCO frequency tuning range at 1-MHz offset

consumption and ordinary phase noise performance at higher oscillation frequency, but utilizing a more expensive 65nm process.

5 Conclusion

In this letter, a wide-tuning-range low-phase-noise VCO is reported. An optimized switch structure and programmable *LC*-tanks are applied in the self-bias structure of VCO to optimize noise performance. The performance outcomes well validate the effectiveness of the topologies and methodologies used in the design. The fabricated VCO exhibits a tuning range of 53.8% from 1.02 GHz to 1.77 GHz, a phase noise of -129.6 dBc/Hz at 1 MHz offset from the carrier frequency of 1.4 GHz. The measured results show a wide tuning range, good noise performance of the presented *LC*-VCO.

6 Acknowledgment

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7 References

1. Q. Gu,*RF system design of transceivers for wireless communications*, Springer Science & Business Media, 1st ed.,2005.
2. B. Razavi,*RF Microelectronics*, Prentice Hall, 2nd ed., 2012.
3. A. Mehrotra, "Noise analysis of phase-locked loops," *IEEE/ACM International Conference on Computer-aided design*, Nov. 2000.
4. D.B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*,vol.54, no.2 pp.329-330,1966.
5. B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 331-343, Aug. 1996.
6. A. Hajimiri and T.H. Lee, "A general theory of phase noise in electrical oscillators." *IEEE Journal of Solid-State Circuits*, vol. 33, no.2, pp. 179-194, Feb.1998.
7. F. Pepe, A. Bonfanti, S. Levantino, C. Samori, and A.L. Lacaita,"Analysis and minimization of flicker noise up-conversion in voltage-biased oscillators," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 6, pp. 2382-2394, Jun. 2013
8. P. Andreani, K. Kozmin, P. Sandrup, M. Nilsson, and T. Mattsson, "A Tx VCO for WCDMA/EDGE in 90 nm RF CMOS,"*IEEE J. Solid State Circuits*, vol. 46, no. 7, pp. 1618-1626, Jul. 2011.
9. C.Sánchez-Azqueta, et al., "High-resolution wideband LC-VCO for reliable operation in phase-locked loops," *Microelectronics Reliability*, vol. 63, pp. 251-255, 2016.
10. R. W. Rhea, *Oscillator Design and Computer Simulation*, New York: McGraw-Hill, 2nd ed., 1995.

11. Y.H. Kao and M.T. Hsu, "Theoretical analysis of low phase noise design of CMOS VCO," *IEEE Microwave & Wireless Components Letters*, vol.15, no.1, pp. 33-35, 2005.
12. E. Hegazi, H. Sjoland, and A.A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1921-1930, 2001.
13. J. Mira, et al. "Distributed MOS varactor biasing for VCO gain equalization in 0.13 µm CMOS technology," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 131-134, 2004.
14. J. Kim, J.O. Plouchart, N. Zamdmer, et al., "A 44 GHz differentially tuned VCO with 4 GHz tuning range in 0.12 µm SOI CMOS," *IEEE Int Solid-State Circuits Conf, Dig Tech Papers*, pp. 1-416, 2005.

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Space transformer connector characterization for a wafer test system

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Abstract: Standard connections from the probe head to the PCB for vertical type probe cards in wafer test are individual separate wires in space transformers (STs), traditionally used for device pitches 80 µm and above for quick turn inexpensive solutions compared to multilayer ceramic substrates. There are inherent signal integrity issues using separate wires in controlling impedance, bandwidth, and cross-talk of STs and probe cards. A method of wiring that includes parallel pairs and twisted pairs is proposed and electrical characterization was performed to establish predictive specifications on the test cards.

Keywords: Semiconductor test; space transformers; paired-wiring schemes

Karakterizacija konektorja prostorskega pretvornika za testni sitem silicijevih rezin

Izvleček: V nasprotju s keramičnimi substrati se za razmake nad 80 µm uporablja poceni in hitre standardne priključke. Standardni priključek med glavo sonde in PCBjem vertikalnih sond pri testiranju silicijevih rezin predstavljajo ločene žičke in prostorski pretvorniki (ST). Uporaba posameznih žičk predstavlja problem inherentne integritete signala pri kontroli impedance, pasovne širine in presluha med ST in sondami. Predlagana je metoda povezovanja s prepletenimi paralelnimi pari. Opravljena je bila električna karakterizacija in napovedane specifikacije testnih kartic.

Ključne besede: test polprevodnikov; prostorski pretvorniki; sheme parnega ožičenja

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1 Introduction

In wafer test, main space transformers which provide connection between the probe head to the PCB in the test system include two common types. First one is typically wired space transformers (WST) and the second one is multilayer ceramic (MLC) or multilayer organic (MLO) types. Although MLC or MLO type space transformers offer better signal integrity for the test system, there are lead time and cost issues affecting the first silicon arrival on test floor. Typical WSTs utilize individual and separate wires for signals or gnd/power lines and are simple to produce mechanically without requiring photolithography. It makes them inexpensive and allow for quick turn vertical probe cards for mainly testing area-array devices such as logic, SoC, and microprocessors as the requirements for finer pitch, higher densities and lower cost of test are accelerating [1-3]. Higher total pin counts above 1000 for area array configurations are more difficult to accommodate depending on the designs compared to MLC type STs.

It is difficult to manufacture a ST with separate-wire-method according to well defined bandwidth or cross-talk specifications for vertical probe cards since there are inherent signal integrity issues using separate individual wires in controlling impedance, bandwidth, and cross-talk. High-speed data transmission using twisted pair cables for transport of telecommunication services or computer networks have been used in the telecom field [4-5]. These type of cables constitute larger diameters with long distances (i.e. Cable lengths of 100 m).

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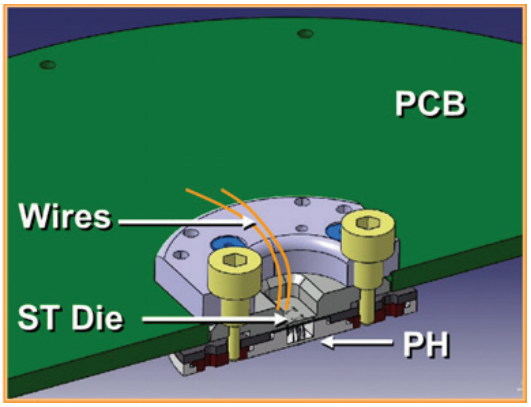
In this study, we have designed these interconnections with new wiring schemes and applied them on conventional space transformers where there is only one guide plate mounted on a PCB. We have experimentally measured the electrical characteristics of these wiring schemes on conventional or wired space transformers (WST). We have proposed earlier the interconnection and wiring schemes in a patent (US 8,430,676 B2) [6] and however, no measurement data was provided in the patent. The space transformer designs proposed were modular type which were different compared to electrical connection assembly of WSTs. In the patent, both parallel-pair or twisted wiring schemes were designed to apply to modular space transformers where there are two guide plates and wiring distances are much shorter, typically less than 20 mm, since spring pin contacts were (Fig 1D and 1E) also used. The top plate had spring pins inserted to mounting holes. The wire ends were connected via several means to the bottom ends of the pin springs inside an aperture. However, wire lengths required for WSTs are typically much higher from the guide plates to the solder connection pads on PCBs. This study provides actual experimental measurements on WSTs for the first time using paired wiring schemes to improve their electrical performance.

a)



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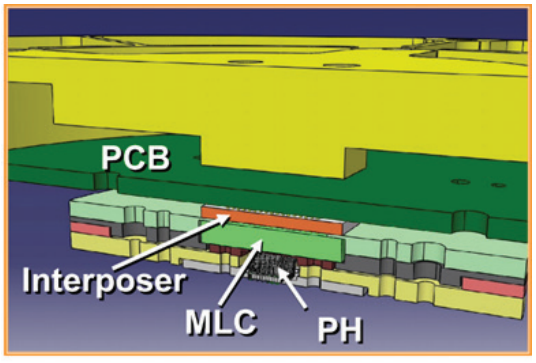


Figure 1: Illustrations of cross-sections of cards with two configurations; a) Probe card showing probe-head (PH) and wired space transformer; b) Probe card with PH, MLC and interposer structure

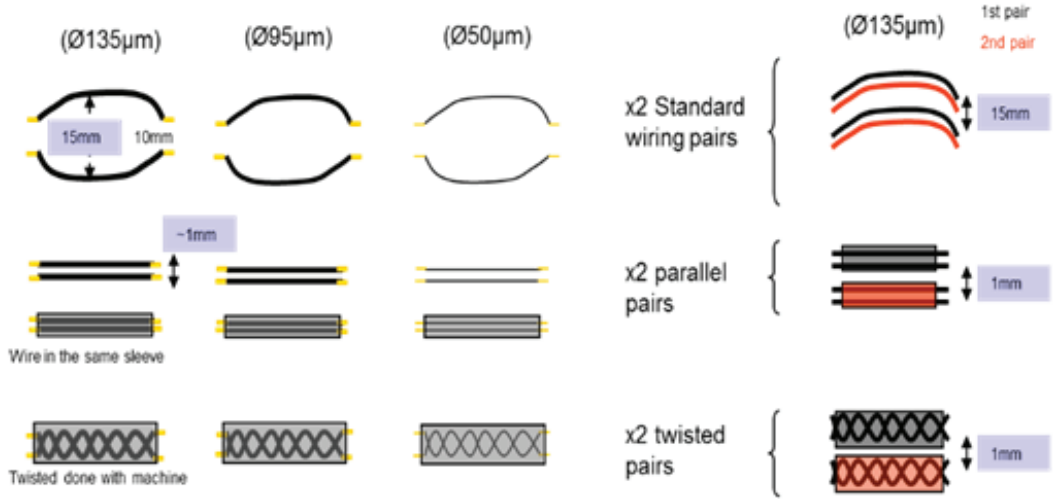
In this investigation, we propose a simple method of wiring that includes parallel and twisted pairs to improve performance and establish reliable ST specifications for semiconductor test system environment. The electrical characterization was performed on the test cards.

2 Design of wired ST and test prototypes

Fig. 1a shows a probe card showing a mechanical assembly of a probe-head (PH), wired space transformer and PCB (printed circuit board). It shows wire connection starting from PH side all the way to PCB sites. A probe card with a PH with probes, MLC and an interposer structure making connection to PCB is shown in Fig. 1b.

A test vehicle was designed and manufactured to characterize the bandwidth and cross-talk for three main vertical probe types corresponding to three different wire diameters, 50µm, 95µm, and 135µm. Wires are made of copper conductors. Bandwidth tests for wires corresponding to 2, 3, 4-mil probes according to wiring configuration which represents the parallel wire and the twisted wire. Crosstalk tests were designed with 3-mil probe configured ST wires according to new wiring configuration: parallel wire and twisted wire pairs. Standard ST electrical performance is not very predictable and the bandwidth is typically limited to 350 MHz and variable crosstalk values were observed based on simulations and characterizations done previously [3, 7]. The wire separation distances may vary greatly depending on the manufacturing process. We assume 10 mm to 15 mm in our studies for standard wiring. With newer configurations of wire connectors proposed, it will be possible to establish the specifications of the bandwidth and the crosstalk for both twisted wire vs parallel wire pairs for WST. The wire length for the experiments was fixed to 60 mm for all samples. Fig. 2 illustrates samples prepared for WST used in RF testing for bandwidth (50µm, 95µm, and 135µm wire pairs) tests on the left and for crosstalk tests for wire pairs for 135µm on the right. Parallel pairs were also inserted in a sleeve for better control of distances on separate wires. Distances between pairs were kept to 1 mm.

The measurement of S parameters was carried out using network analyzer, HP8722D, on a Gigatest GTL3030 probe station using Model Pico probes with appropriate pitch for contacting probe tips. Time domain reflectometry (TDR) measurements were also done to observe impedance variations in the same setup.



a. Bandwidth test **b. Crosstalk test**

Figure 2: Wire configurations for test vehicle; a) Samples for bandwidth tests; b) Samples for crosstalk tests

Both parallel and twisted paired wiring and the standard wiring in ST were built in a similar fashion and the wire still must travel through the PCB and over mechanicals. For simplicity, only critical and high speed lines were paired on the ST to keep manufacturing cycle short and achieve optimum performance. The design of device and pin configurations, location of signal and return paths, is important to establish GNDS on either side of the critical signal for a given test system.

On probe heads, the characteristic impedance and the bandwidth are mainly dependent on the electrical pitch since we can assume relatively short probes (< 4 mm in total length) are used compared to much longer wires in ST. The electrical signal-return path and pitch of the test system may not be the same as the device pitch, because other forward and return path probes can be utilized. It is critical to determine forward and return current paths in the design cycle of STs. Simulations indicated that speeds up to 10 GHz are possible for 2 or 3 mil-dia probes for their minimum allowable pitch configurations. However, this performance is not achieved for wired STs because the length of wires needed is much longer and it is difficult to control separation distance along the wire connection. So for a test system, we can ignore the PH for test speed requirements of 1 GHz, the critical components of the assembly become the space transformer and its connection to the PCB.

Table 1: Bandwidth measurements on the test vehicle with three different wire types and configurations for STs.

Configuration/ Wire Diameter	1 cm separation	1 mm separation	Parallel pair	Twisted pair
50 µm	100 MHz	180 MHz	640 MHz	3 GHz
95 µm	50 MHz	230 MHz	1.45 GHz	1.29 GHz
135 µm	100 MHz	270 MHz	1.65 GHz	1.27 GHz

3 Results

Table 1 summarizes the findings for three different diameters of wires for STs. For 4-mil probes (135µm wire ST configuration), results are very close to simulation results done earlier. As expected at 10mm wire separation, the bandwidth is measured close to 100 MHz at – 3 dB. It indicates that at 1mm separation, the bandwidth rises to 270 MHz at – 3 dB. When the parallel pair inside sleeve version is tested for the same wire diameter, it is good up to 1.6 GHz at – 3 dB. The bandwidth for the twisted pair is close to that of parallel pair, but it has little bit less bandwidth, 1.3 GHz at – 3 dB. This may be due to the fact that the twisted-pair wire separation is too close and there are variations along the length. A difference on the bandwidth is not expected between the twisted-wire versus the straight-wire on the measurements. The difference may be created if the twisted wire length is more than the straight wire length. The measured length of the wires on probe card was 60 mm on average. It is expected that the twisting of wire will provide crosstalk performance improvement since the induced voltage from different segments of the wire cancels out. For this type of wire layout with

1mm distance, the crosstalk is less than 30 dB (Fig. 3). To prevent serious crosstalk problems, the wire pairs should be close to each other. It is typically assumed that the distance between the two wires (ground and signal) is kept same along the 60 mm wire connection. In reality however, this is not the case for the end connections, especially for the ground connections near the probe-head side. The variation in the separation distance between the ground and the signal wire on main body of wires can introduce serious bandwidth performance issues.

As a general rule, the wire diameter is not the main source of the bandwidth limitation since the distance in between can be adjusted to achieve 50-ohm for a given diameter as long as mechanical probe card design rules allow. It is possible then to achieve the expected bandwidth with 95 µm dia. wire on built parts and the same bandwidth can be obtained with 135 µm or 165 µm dia. wires as long as the separation distance is adjusted properly. To optimize the probe card, the distance between two wires for a 95 µm wire case should be close to 105 µm. The insulation thickness for the wire should be 5 µm. The distance between two wires for a 135 um dia. wire case should be close to 147 µm. This implies the insulation thickness should be 6 µm. The distance between two wires for a 165 µm dia. wire case should be close to 181 µm. The insulation thickness needed is 8 µm.

For a proper manufacturing of a twisted-wire pair, wires should be in close contact with each other and irregular air gaps should not be allowed. For the optimum connection trace lines, the total length of wires should be reduced as much as possible. The total electrical performance of this structure is mostly dominated by the length of the wires (60 mm) rather than the wire diameter in the design. It is known that the number of twists on wire pairs will affect the crosstalk. A higher crosstalk cancellation on higher frequencies is expected, as the number of twist rises. To cancel the crosstalk, it is best at least to make one twist per one tenth of the wavelength for a given frequency. To calculate the wavelength we can use 'wavelength = speed of light / frequency'. For example, a twist per 3-mm will give rise to a crosstalk attenuation up to 10 GHz. Similarly, a twist per 6-mm of wire pair length will support a crosstalk attenuation up to 5 GHz. Another effect to consider is the angle between the victim line and aggressor line when they are less than 180 degree. This would also make the analysis complex. More number of twists allow for better attenuation on crosstalk. It should be noted that if the twisting increase the total wire length significantly compared to a straight-wire case, the bandwidth will be reduced compared to a straight-line case. Therefore, moderate twisting in wire-pair formation process should be preferred for optimal results.

3.1 S-parameter in dB

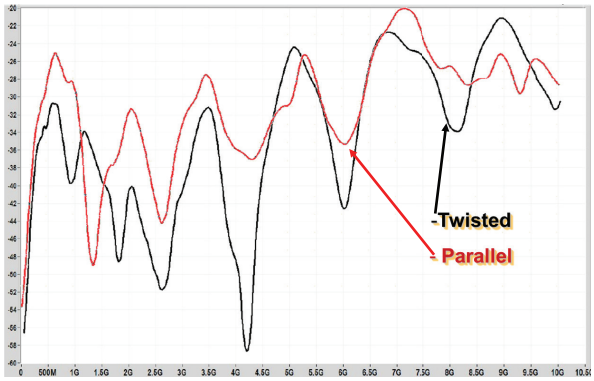


Figure 3: S21 data-Crosstalk for ST with 1 mm-distance for parallel and twisted pairs of 135µm diameter wires.

In wafer test, there are many configurations of device types especially for logic and mixed signal applications and the multi-device testing is always critical from the test efficiency and yield perspectives. However, the fab teams require very short lead times for initial test results from the design time and fab to the first silicon. This forces teams to use certain vertical probe-card types which allow versatile designs and short cycles. In this family, vertical or cobra type probe cards with WSTs offer a good solution due to their simplicity and cost. The pitch is easy to customize and several suitable wire types with proper diameters are readily available for WSTs. WSTs offer lead time advantages of at least 4-5 weeks (1-2 weeks vs 6-8 weeks) compared to MLC (multilayer ceramic substrate) or MLO (multilayer organic substrate) in the probe card assembly. This lead time differential is crucial in some cases for the first silicon test. The cost for MLC/MLO is also 5-10 times more expensive. If the lead time is not critical and the volume count for probe cards are high, only then the probe card solutions with MLC/MLO assembly become a reasonable option. The factors to consider when choosing the best fit of STs for device types include the pitch, line numbers per device (1 or 2 rows), peripheral rows (1-3), number of DUTs (device under test), configuration (partial area array or full array) and area size for each DUT. There are five common classes of substrate systems of interconnects different than WSTs that are used in connecting probe heads to PCB and tester system. These can mostly support impedance-matched traces for signal transmission lines, except for via-sections, produced by layered-lithographic production methods.

MLC: Multi-Layer Ceramic, can be with standard thin film or Multi-layer Thin Film (MTF)

MLC: LTCC (low-temperature co-fired ceramic) or HTCC (hi-temperature co-fired ceramic) types.

MLO: Multi-Layer Organic made from packaging technology, laminated core with several microvia build-up layers

HDI PCB: High Density Interconnect made from PCB technology, laminated layers with through hole and microvia on 1 buildup layer

Direct Attach: PCB with embedded pads in the center area

These substrates or space transformers are either connected by BGA (Ball Grid Array) using soldering or spring pin connected by PGA (Pin Grid Array) to main PCB and the test system. Interconnects with BGA-arrays are hard to repair due to solder-connection in case of channel failures. PGA-type interconnects are repairable, however, they can apply very high force levels when pin counts are above 2500. PGA-type connection is used mainly for HTCC since they are strong and thick ceramic substrates can better withstand bending. WSTs are typically repairable and do not induce any pin force into the PCB or the probe-head. They are also the lowest cost STs. HDI PCB density limitations arise as the pitch shrinks and Direct Attach process are only feasible when large pitch allows manufacturing PCBs for a particular design. Fine pitch device testing typically cannot be supported by HDI PCB or Direct Attach.

4 Conclusion

Electrical characterization of proposed designs of wire pairs of parallel and twisted types was carried on test vehicles for vertical probe card applications. When the parallel pair inside sleeve version is tested for the wire diameter of 95 µm, it is good up to 1.45 GHz at – 3 dB. To optimize the probe card, the distance between two wires for 95 µm wire should be close to 105 µm. So the insulation thickness for the wire should be 5 µm. Studies on wire diameters of 50µm, and 135µm were performed and presented for both parallel pair and twisted wire types for space transformers.

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6 References

1. ITRS roadmap 2015: https://www.semiconductors.org/clientuploads/Research_Technology/ITRS/2015
2. Yoo, S.K., Kim, T.K., Cho, Y.A. and Yook, J.K.: 'Optimization for polyimide circuit design of space transformer on probe card', IEEE Semiconductor Wafer Test Workshop, San Diego, USA, June 2016, S05-01
3. Mialhe, L., Garidi, I. and Tunaboylu, B: 'Cobra FP probe card for multidut, logic and memory applications', IEEE Semiconductor Wafer Test Workshop, San Diego, USA, June 2005, S04-02
4. Mahmoud, A. F. and Abdallah, M. I.: 'Performance testing of twisted pair cables', J. of Computer Systems, Networks and Communications, 2008, pp. 1-8. http://dx.doi.org/10.1155/2008/586427
5. Siebert, W. P.: 'High frequency cable connector for twisted pair cables', IEEE Trans. Comp. and Pack. Tech., vol 26, 3, 2003, pp. 642-650.
6. S. Dang, R. Kazmi, G. Back, B. Tunaboylu. 'Modular space transformer for fine pitch vertical probing application', Patent No: US 8,430,676 B2, 2013.
7. Kilicaslan, H. and Tunaboylu, B: 'Bandwidth improvement techniques on probe cards', IEEE Semiconductor Wafer Test Workshop, San Diego, USA, June 2006, S07-03

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Modelling Overvoltage Protection Components: Verilog Simulations of Combined MOV and GDT Arresters

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Abstract: Overvoltage protection systems are used to protect sensitive electrical and electronic equipment from voltage surges and lightning strikes. These systems are mostly based on the use of gas discharge tubes (GDTs) and metal-oxide varistors (MOVs), which are utilised individually or in various combinations. Adequate computer simulations play an important step in the process of designing overvoltage protection systems and selecting adequate parameters. In this paper, the modelling of low-voltage GDT and MOV components is performed using the Verilog-A hardware description language. The presented models are designed for integration with other overvoltage protection system components to form an integrated overvoltage protection system. The current–voltage characteristics of the GDTs and MOVs are highly nonlinear and frequency dependent. The developed Verilog-A mixed behavioural and structural models of GDTs and MOVs ensure a stable convergence of numerical processes during the simulations of circuits with these elements. The simulations of overvoltage protection systems were completed using a TINA circuit simulator. Two laboratory tests were performed using GDT and MOV components. In the first test, the time responses of the current and voltage on a GDT and MOV serial connection were measured in the laboratory. In the second test, the response of the GDT and MOV serial connection was tested in a power line network environment, where a surge current impulse and power line voltage of 400 V peak and frequency of 50 Hz existed simultaneously. The dynamic response of the GDT and MOV serial connection obtained through the simulations agrees well with the measurement results.

Keywords: Verilog; modelling; gas discharge tubes; metal-oxide varistor; overvoltage protection.

Modeliranje komponent prenapetostne zaščite: Simulacija serijske vezave prenapetostnih odvodnikov MOV in GDT v jeziku Verilog

Izvleček: Sistemi prenapetostne zaščite se uporabljajo za zaščito občutljive električne in elektronske opreme pred prenapetostjo in udari strele. Običajno so ti sistemi zasnovani na plinskih odvodnikih prenapetosti (GDT) in metal-oksidnih varistorjih (MOV), ki se uporabljajo posamezno ali v različnih vezavah. Računalniške simulacije predstavljajo pomemben korak pri načrtovanju sistemov prenapetostne zaščite in izbiri ustreznih parametrov. V tem članku predstavimo modeliranje nizkonapetostnih komponent GDT in MOV v jeziku Verilog-A. Predstavljeni modeli so namenjeni integraciji z drugimi komponentami, ki tvorijo integriran sistem prenapetostne zaščite. Tokovno- napetostne karakteristike GDT in MOV so močno nelinearne in frekvenčno odvisne. Razviti modeli GDT in MOV v jeziku Verilog-A uporabljajo opis obnašanja in strukturni opis, kar zagotavlja stabilno konvergenco numeričnih procesov. Simulacije sistemov prenapetostne zaščite so potekale z uporabo simulatorja TINA. V praktičnem delu smo izvedli dva laboratorijska testa. V prvem testu so bili v laboratoriju izmerjeni časovni odzivi toka in napetosti na serijski vezavi GDT in MOV. V drugem testu smo preizkusili odziv serijske vezave GDT in MOV ob hkratni prisotnosti impulza prenapetostnega toka in omrežne napetosti amplitude 400 V in frekvence 50 Hz. Dinamični odziv serijske vezave GDT in MOV, pridobljen s simulacijami, se dobro ujema z rezultati meritev.

Ključne besede: Verilog; modeliranje; plinski odvodnik prenapetosti; metal oksidni varistor; prenapetostna zaščita.

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1 Introduction

Overvoltage protection components have become an inevitable part of the devices aimed to protect sensitive equipment against overvoltage surges caused by atmospheric discharges and transients in power networks. An overvoltage protection system must be designed to capture the atmospheric discharge to a preferred point, conveying the energy into the ground and protecting all incoming power and communication lines using surge protection devices (SPDs).

SPDs must discharge high-magnitude impulse currents and limit the overvoltage levels [1, 2]. SPDs are primarily based on metal-oxide varistors (MOVs) and gas discharge tubes (GDTs), which are used individually or in serial combinations.

Overvoltage protection components can be divided into voltage switching and voltage limiting components [1]. Voltage switching components operate by switching from a high to low resistance state at certain breakdown voltages and behave as a short circuit. GDTs operate in accordance with this principle. The components in the second group limit a transient overvoltage impulse to a predefined voltage level. MOVs belong to this set of overvoltage components.

Modelling and simulation can significantly facilitate the process of designing overvoltage protection systems. Typically, simulations are based on models of the individual components comprising the overvoltage protection system, commonly described with mathematical expressions.

The modelling and simulation process is more complex when some of the components have nonlinear characteristics and states that vary depending on excitation input values. In addition, the models need to be developed in a form that allows their integration with the existing components within the electronic simulation program.

MOVs and GDTs have highly non-linear current–voltage characteristics [1–4]. The simulation of a system with these components can lead to non-convergent numerical calculations [5], which is especially critical during the transition of individual components from one state to another.

The simulation of overvoltage protection systems is mostly based on SPICE models and implemented using SPICE-based simulation tools [5]. Using intrinsic components as the basic building blocks for a larger model, designers can define new SPICE models. SPICE accepts netlists as a text description of a circuit that is comprised of interconnected basic components [6]. The models of these basic components are provided within the simulator.

The existing GDT models available in the literature are largely SPICE based, in the form of structured netlists composed of basic components [7–9]. The solution presented in [7] uses controlled switches and diodes with specified breakdown voltages. The model in [8] is created with transistors, providing theoretical triac voltage–current characteristics. Conversely, the GDT models in [10–12] are based on mathematical descriptions of basic operational principles developed for the Matlab/Simulink environment.

Several MOV models have been proposed in the literature [5, 12–17], aiming to properly represent MOV's nonlinear characteristics and frequency dependence behaviour. The IEEE W.G. 3.4.11 proposed a frequency-dependent model with two nonlinear resistors [14], which was further simplified by [15], preserving its basic principle. In [16], the authors neglected the first inductance in the IEEE model as well as the simplified parameter determination procedure [16]. The MOV model presented in [12] was developed in the Matlab/Simulink environment for simulations of transients in low voltage power-lines. A review of the existing models and their implementation for transient behaviour of electrical circuits is presented in [13].

Verilog-A, a subset of Verilog-AMS, has emerged as a standard language for the development of compact models of circuit components based on mathematical descriptions of the electrical behaviour of individual components [18]. This language allows the description and simulation of components and circuits at a higher level of abstraction [18, 19]. The compact models were originally coded in FORTRAN or C, with relatively complex codes [18]. The compact models should be sufficiently simple to be easily developed and incorporated in circuit simulators. Verilog-A, as a hardware design language (HDL) for analog circuits and system design, uses a text-file code to describe the mathematical models [19, 20]. The Verilog-A code is converted into low-level C language by a code generator [19]. The generated C code is then directly compiled into the simulator, resulting in an equivalent SPICE model. In this way, it is possible to simulate electronic circuits that include both Verilog and SPICE models. TINA supports simulations including Spice netlists along with components modelled in Verilog, Verilog-A and Verilog-AMS [21].

The presented MOV and GDT Verilog-A models are based on mathematical descriptions of the transfer function in the MOV modelling and transition between states during the GDT modelling. The developed mod-

els ensure a stable convergence of numerical process during simulations of circuits with these elements.

Verilog-A models of MOV and GDT are used to simulate a serial connection of these components. Using such a serial connection reduces some of the shortcomings that arise when using these components individually, especially in the first stage of overvoltage protection systems. For example, high GDT resistance eliminates leakage currents in MOVs. On the other hand, the use of MOVs in serial connections resolves fast surge discharges, as GDTs have a much longer response. The performed simulations demonstrated that the developed models ensure stable convergence of the numerical processes.

The validation of the developed models was performed by comparing the simulation results with the measurement results of the residual voltage measured on the GDT and MOV serial connection. In the laboratory, waveforms of residual voltage under surge currents of 40 kA (10/350 μs) and 20 kA (10/700 μs) were measured. The results obtained by performing simulations with the TINA program tool were verified by laboratory tests. In the first scenario, the residual voltage at the GDT and MOV serial connection ports were measured after stress with the current pulse shape. In the second scenario, the overvoltage protection was focused on measurement of voltage waveform at the terminals of the MOV and GDT serial connection when a surge impulse and power line voltage of 50 Hz existed simultaneously. The second scenario corresponds to a real application of an overvoltage protection device.

The rest of this paper is structured as follows: Section II describes the basic operational principles of GDTs and MOVs and appropriate current/voltage characteristics. Verilog-A GDT and MOV models (presented with simplified pseudo codes) are developed using the TINA circuit simulator and described in Section III. Section IV presents the results of the measurements and numerical simulations for two overvoltage protection system scenarios. Conclusions and recommendations for future research are given in the last section of the paper.

2 Overvoltage Protection Components

A basic description of the GDT and MOV components is given in this section to simplify the presentation of the developed models described in the next section.

GDTs consist of two or more metal electrodes separated by a small gap filled with a gas insulation medium and held by a ceramic or glass cylinder [1–3]. During normal operation at nominal voltage, GDTs behave as an insulator.

GDTs dissipate voltage transients through a contained plasma gas when an overvoltage pulse reaches the spark-over (breakdown) voltage (Fig. 1). The spark-over voltage is not constant but rather depends on the rate of rise of the surge voltage. As the voltage increases across the GDT, the gas in the tube starts ionising due to the charge developed across it [1-3]. In this region, known as the *glow region* with voltage U_{glow}, the increasing current flow generates an avalanche effect, transitioning the GDT into a virtual short. This is the arc burning phase. The glow region is shown in Fig. 1. During the short-circuit event, the voltage developed across the device is known as the arc voltage, U_{arc}. This region is known as the *arc region* (Fig. 1). The transition time between the glow and arc regions is dependent on the physical characteristics of the GDT [3]. In the arc region, the GDT diverts the transient current away from the protected device. During the extinguishing process, the transition from the arc to glow regions may be at a lower current than during the transition from the glow to arc regions (dashed line in Fig. 1.).

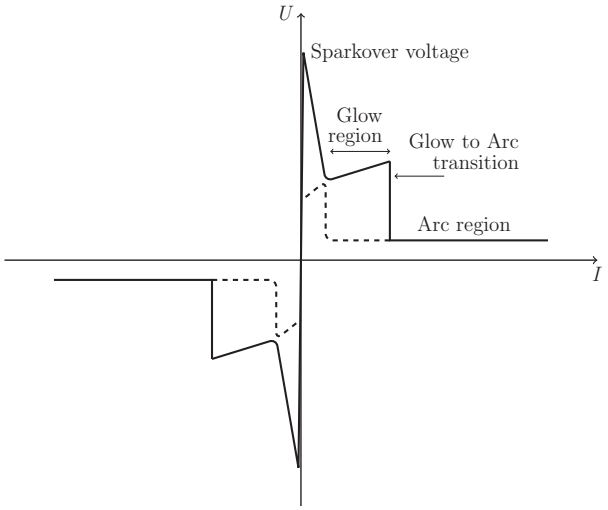

Figure 1: GDT *U-I* characteristics

GDT components have high insulation resistance and low capacitance. When a voltage applied to the GDT electrodes is below its spark-over voltage, the leakage current through the arrester is close to zero. A low leakage current ensures minimal influence on the normal operation of the equipment.

MOVs are resistors with a nonlinear *U-I* characteristic (Fig. 2.). Unlike GDTs, these elements do not cause short-circuits in the power supply network. MOVs are produced of a ceramic material obtained by mixing zinc oxide (ZnO) with a small amount of additives. The

ZnO grains have low resistance and are surrounded by granular layers of additives with high resistance [1]. This structure behaves like diodes connected in series/parallel, ensuring that the MOV has nonlinear characteristics.

When a low voltage is applied to the MOV electrodes, the diodes are not conductive and the MOV behaves as an insulator. After the electric field reaches a value above 100 kV/mm, the current starts to flow and varies from 1 mA to 1 kA. With a high electric field, the voltage drop in the MOV is linear since it is determined by the voltage drop in the ZnO grain resistance [1]. The voltage drop at the barrier can be neglected due to the tunnel effect. This part of the *U-I* characteristic is linear.

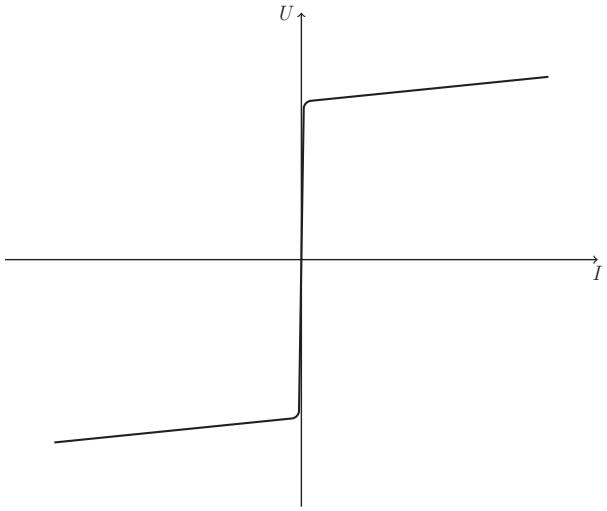

Figure 2: MOV *U-I* characteristics

The ability of components to withstand high-energy pulses is measured by the different pulse shapes (8/20 µs, 10/350 µs, 10/700 µs, and 1.2/50 µs) and amplitudes.

3 Verilog-A Models of Overvoltage Protection Components

The Verilog-A hardware description language is accepted for the modelling of electronic components and circuits due to its simplicity and flexibility when writing model code. The descriptions of the developed models of overvoltage components are based on pseudo code. For presentation purposes in this text, some blocks of the code are represented with mathematical equations.

GDTs can be in three different states, as described in the previous section [1, 7, 9]. A simplified GDT model can be presented as a symmetrical low-capacitance voltage and current controlled switch, whose resistance may instantly change from several GΩ during normal operation to values less than 1 Ω after ignition caused by a surge voltage. The transition from an open to closed switch includes an ionising state, and the GDT model must include these three states. The Verilog-A GDT model presented in this paper includes these three states, defined in accordance with the characteristic shown in Fig. 1.

The modelling of the GDT transition in SPICE is implemented with voltage and current control switches. The required voltage levels are ensured by diodes with the specified breakdown voltages [7]. The model presented in [8] does not include switches. The transition from a high-value impedance state to a very low impedance state in [8] is solved using bipolar transistors connected to provide theoretical triac behaviour of the GDT model as a whole.

The Verilog-A module may contain equations for behavioural modelling and instantiations of other modules such as structural modelling. The behavioural models define the relationships between the outputs and inputs, and they contain procedural statements that control the simulation and manipulation of the variables of the defined data types. The behavioural models are more abstract, and the focus is on the functionality of the design. Structural modelling defines the system in terms of basic components and their interconnections, describing the interconnection between the predefined components in the model. The model in Verilog-A is defined with the nodes and branches, so the behaviour of each branch must be specified.

The simplified pseudo-Verilog-A code of the proposed GDT model is shown in Fig. 3. The first line, *discipline.va*, provides common definitions that are used to specify the type of a continuous wire. The *discipline* includes a collection of related natures as physical signal types. Electrical discipline, used in our models, consists of voltages and currents. The second line defines the name of the component, in this case *GDT*, and the input/output nodes. The nodes *a* and *c* are declared as *inout* ports and presented with *electrical* discipline. The *a* and *c* pins are nodes that the GDT shares with the rest of the circuit (line 3). The pins are then declared as being electrical, meaning that the potential of each pin is a voltage and the flow into the pin is a current. The parameters, defined below, are treated as constants within the module and cannot be changed from within the module (lines 5 to 12). In Verilog-A, the description of the model is given as an analog process, which is denoted with the keyword *analog* in line 13.

The initial values and state of GDT is defined in (Fig. 3, line 14). The capacity *C* of GDT shows the behaviour at

nonconductive state, and is modelled using *ddt* function in line 16. The charge is first calculated in line 15 [18]. The construction of GDT is such that it has very low capacitance *C*. This allows GDT usage in high-frequency circuit applications protecting communication and data lines from overvoltage.

The inductance *L* takes into account dynamic response. If the voltage at GDT terminals has low rate of rise, the spark-over voltage will be determined by electrode spacing, the gas type and pressure, and pre-ionization of the enclosed noble gas [3]. When the overvoltage pulse has fast rate of rise the spark-over voltage of GDT will be increased. This is caused by the finite time necessary for the gas to ionize. The estimation of spark-over voltage is based on measured voltage levels for different values of rate of rise and provided by manufacturers of GDT components. The estimation of spark-over voltage is listed in lines 20 and 21.

GDT stressed by overvoltage impulse can be in previously described three states. The Verilog-A model of GDT, including descriptions of three states, can be simplified by using an 'IF THEN ELSE' conditional statement. From the current-voltage characteristic curve shown in Fig. 1, it is clear that the GDT has bi-directional symmetrical characteristics. The GDT can operate or function in either direction or overvoltage pulse polarity, and the GDT model must take this property into account.

When the voltage at the GDT terminals is greater than the spark-over voltage, the GDT goes into an ON state (line 23). After ignition, the voltage drops from the spark-over voltage to the glow voltage level. This transition can lead to a loss of convergence during the process of solving the voltage and current waveforms. In order to avoid this loss of convergence, the transition from the high resistance state to the glow region is modelled using the transition function (line 30):

$$u(t) = \left(U_p - U_{glow}\right) e^{-\frac{t-t_1}{10^{-8}}} + U_{glow} \quad (1)$$

where *u(t)* is the voltage at the GDT terminals, U_p is the spark-over voltage, U_{glow} is the voltage in the glow region and t_1 is the time at the moment when the overvoltage pulse reaches the spark-over voltage. The voltage in the glow region is represented by U_{glow}.

A similar transition exists when the GDT switches from the glow to arc regions. This transition can also lead to a loss of convergence. Hence, the transition from the glow to arc regions is modelled using the following equation:

$$u(t) = \left(U_{glow} - U_{arc}\right) \tau^{I_{glow} - I_{arc}} + U_{arc} \quad (2)$$

where U_{arc} is the voltage in the arc region, I_{glow} is the current in the glow region before transition and I_{arc} is the current in the arc region after transition. This transition is presented on line 33 in Fig. 3.

Using the two previously described functions, a smooth transition from one state to another is provided, and the standard use of switches in the GDT model is avoided. The resistance of the GDT in normal operation is R_{OFF} and is calculated in line 42. The calculated voltage *U*, using the contribution operator (<+) in line 44, determines the value of the potential between the *n* and *c* nodes *V(n,c)*.

MOVs are voltage-dependent resistors with a highly non-linear voltage-current relation, and they have different delays in the conduction mechanism at different surge current wavefronts. The IEEE model is the most used model in the literature for transient analysis of varistors. The Verilog-A model of MOV, presented in this paper, is based on the IEEE model. The model is frequency dependent and is suitable for the numerical simulation of fast transients [4, 5]. The simplified pseudo-Verilog-A code of the MOV model is shown in Fig. 4.

The non-linear voltage-current relation is represented by two non-linear branches separated by an *R*, *L* filter. This filter has an important role in taking into account different delays in the conduction mechanism at different surge current wavefronts [4, 5, 16].

The first line in Fig. 4 defines the *discipline* required for analog simulations. The second line lists the module name of the component, in this case *MOV*, and the list or node names (*p* and *n*). The port direction (line 3) and port and node types (line 4) are then declared. The parameters provide a way to pass values into the module at the time of instantiation. The parameters of the MOV model were computed using the procedure given in [14, 15]. The analog block describes the MOV model and includes lines from 18 to 45.

The series inductance is first introduced (line 20). The *L1* represents the inductance of the current path through the arrester. The resistance *R1* in line 21 provides convergence in the numerical simulations. These two components (*R1* and *L1*) also represent the input filter of the model.

The first and second nonlinear elements are modelled with the following expression [17]:

$$U = U_n k b^I I^c \quad (3)$$

where *U* is voltage across the varistor, *Un* clamping voltage and *I* is the current through the varistor. The

coefficients *k*, *b*, and *c* are obtained from fitting of the curves proposed by the IEEE Working Group. The first nonlinear element is listed in lines 22 to 30. The nonlinear *VI* characteristic is divided in three regions. The code of second nonlinear branch is listed in lines 36 to 44. The nonlinear elements are divided by the *R-L* filter (lines 34 and 35). The MOV capacitance *C* is presented in line 32.

MOV and GDT components are described using the module in Verilog-A [19]. These two components are then combined as a GDT and MOV serial connection (Fig. 5). The GDTMOV model uses previously presented

```
1: 'include "disciplines.va"
2: module GDT(a, c);
3: inout a, c;
4: electrical a, c, n;
5: parameter real Cgap = 0.5e-12;
6: parameter real Riso = 1.0e9;
7: parameter real L =1.0e-9;
8: parameter real Uglow=150.0;
9: parameter real Uarc=40.0;
10: parameter real tau=0.01;
11: parameter real Iarc=9.0;
12: parameter real Imin=90.0e-3;
13: analog begin
14: Initialize basic values and state of GDT
15: q=Cgap*V(a,c);
16: I(a,c) <+ ddt(q);
17: V(a,n) <+ L*ddt(I(a,n));
18: I(a,n) <+ V(a,n)/Rp;
19: Estimation of sparkover voltage U_p
20: absslope=abs(ddt(V(a,c))*1e-6);
21: U_p < +table_model(absslope,"table_slope.tbl","L");
22: if U > U_p then
23:     GDT goes into ON state
24:     define time t_1
25: else
26:     GDT remains in OFF state
27: end if
28: if GDT is in ON state then
29:     if I < I_arc then
30:         U = (U_p - U_glow)e^(-(t-t1)/10^-8) + U_glow
31:     else
32:         if I > I_arc + ΔI then
33:             U = (U_glow - U_arc)τ^(I-I_arc) + U_arc
34:         else
35:             U = U_arc
36:             if I < I_min then
37:                 GDT goes into OFF state
38:             end if
39:         end if
40:     end if
41: else
42:     U = I · R_OFF
43: end if
44: V(n,c)<+U;
45: end
46: endmodule
```

Figure 3: The pseudo Verilog-A code of the GDT model

models (Fig. 3, Fig. 4) of the *GDT* and *MOV*, which are included in the code (lines 10 to 13). In line 14, the module starts with the name of the model and the input and output nodes. Next, the direction of two *electrical* nodes are defined: *p* and *n* (line 16). Internal node *i1* is defined as *electrical*. The nodes are used as interconnection points for ports.

```
1: 'include "disciplines.va"
2: module MOV (p, n);
3: inout p, n;
4: electrical p, n, n1, n2;
5: parameter real L1 = 0.6e-9;
6: parameter real L2 = 45e-9;
7: parameter real R1 = 0.3;
8: parameter real R2 = 0.195;
9: parameter real k1 = 1.2968167;
10: parameter real k2 = 0.9713959;
11: parameter real b1 = 1.000005;
12: parameter real b2 = 1.000004;
13: parameter real c1 = 0.0376332;
14: parameter real c2 = 0.0510025;
15: parameter real Imin=1e-5;
16: parameter real Un=450.0;
17: parameter real C = 0.3e-12;
18: analog begin
19: // The first RL filter
20: V(p,n1) <+ L1 * ddt(I(p,n1));
21: V(p,n1) <+ I(p,n1) * R1;
22: // Te first nonlinear branch
23: i_1 = I(n1, n);
24: if i_1 > I_min then
25:     U_1 = U_n · k_1 · b_1^(i_1) · i_1^(c_1)
26: else
27:     R_L = U_n · k_1 · b_1^(I_min) · I_min^(c_1)/I_min;
28:     U_1 = R_L * i_1;
29: end if
30: V(mid1, n) <+ U_1;
31: // Varistor capacity
32: I(n1, n) <+ C * ddt(V(n1, n));
33: // The second RL filter
34: V(n1,n2) <+ L2 * ddt(I(n1,2));
35: V(n1, n2) <+ I(n1, n2) * R2;
36: // The second nonlinear branch
37: i_2 = I(n2, n);
38: if i_2 > I_min then
39:     U_2 = U_n · k_2 · b_2^(i_2) · i_2^(c_2)
40: else
41:     R_L = U_n · k_2 · b_2^(I_min) · I_min^(c_2)/I_min;
42:     U_2 = R_L * i_2;
43: end if
44: V(n2, n) <+ U_2;
45: end
46: endmodule
```

Figure 4: The pseudo Verilog-A code of MOV model

The GDTMOV model itself is constructed by creating instances of predefined GDT and MOV modules, wiring them together by connecting them to nodes and then specifying parameters for them. This is done for the GDT model (line 18) and the MOV model (line 19).

The statement in line 18 directs that an instance of the module *GDT* be connected to nodes *p* and *i1* and be named *GDT1*. The parameters of *GDT* are defined in the GDT module and are not stated here. The second statement (line 19) directs that an instance of *MOV* be named *MOV1* and connect to *i1* and *n*. The module terminates with the *endmodule* statement.

```
1:  ////////////////////////////////
2:  //TINA HDL Macro Description Begin
3:  //entity_name:GDTMOV;
4:  //arch_name:ignored;
5:  //ports:p,n;;
6:  //Mode:VerilogAMSTyp;
7:  //TINA HDL Macro Description End
8:  ////////////////////////////////
9:  ‘include "disciplines.va"
10: module GDT(a, c);
11: The code of GDT from Fig. 3.
12: module MOV (p, n);
13: The code of MOV from Fig. 4.
14: module GDTMOV (p, n);
15: inout p, n;
16: electrical p, n;
17: electrical i1;
18: GDT #( ) GDT1( .a(p), .c(i1) );
19: MOV #( ) MOV1( .p(i1), .n(n) );
20: endmodule
```

Figure 5: The pseudo Verilog-A code of GDT and MOV in serial connection

The parameters of the GDT and MOV models are adapted to the components used in the experimental tests. These parameters are based on data provided by the producers of the overvoltage components.

4 Numerical Simulations and Measurements

The validation of the developed GDT and MOV models is based on comparisons of the residual voltages obtained using numerical simulations and experimental tests when the MOV and GDT serial connection is stressed with a current pulse of a given shape and amplitude. The model of the MOV and GDT serial connection, developed in Verilog-A, is simulated using the TINA circuit simulator.

In the first scenario, the residual voltage at the GDT and MOV serial connection ports is measured after stress with a 10/350 µs current pulse shape with an amplitude of 40 kA. The measurement setup of the first test system is presented in Fig. 6. For this measurement, a surge generator (TUG-200 generating an impulse of direct atmospheric discharge 10/350 µs short circuit), a digital scope Tektronix (100 MHz, 1 GSample/s), and a Pearson current monitor model 1423 were used. The test system from Fig. 6 is simulated in the TINA software tool. The scheme of the circuit with the GDT and MOV serial connection as an integrated component modelled in Verilog-A is presented in Fig. 7. The 10/350 µs current pulse is modelled using the piecewise linear signal definition as a set of *Time/Value pairs*.

The residual voltage is measured at the terminals of the MOV and GDT serial connection and presented in Fig. 8. The residual voltage waveform obtained by the simulation is presented in Fig. 9. The time response of the GDTs and MOVs depends on the rate of rise and the magnitude of the surge pulses [3–5].

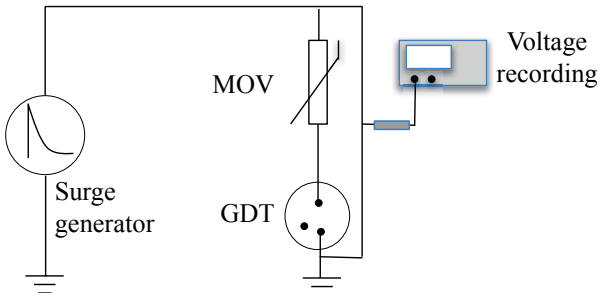

Figure 6: Measurement setup of the GDT and MOV in serial connection (surge current shape is 10/350 µs and the amplitude is 40 kA)

GDTs provide insulation between the protected lines and the ground potential during normal operation. High GDT resistance eliminates the leakage current that occurs when MOV-based surge devices are used. GDTs are also characterised by a high surge current discharge capacity, which can take more than ten thousand amperes (8/20 µs). However, GDTs have a slightly slower response compared to MOVs. The voltage drop in GDTs remains constant and low regardless of the surge current and behaves as a low impedance switch.

MOVs can also be used to meet the requirements of lightning protection class I with low protection levels due to high-performance varistor ceramics and the ability to discharge high surge pulses in acceptable installation spaces. The fast response time of MOVs (nanosecond range) makes them suitable for limiting even particularly dynamic surge voltage phenomena.

In normal operation, GDTs cut off leakage currents. During the surge pulse, the GDT and MOV serial connection effectively discharges the transients to ground and limits the voltage below the dielectric strength of the end device. The typical dielectric strength value of end devices is about 1.5 kV.

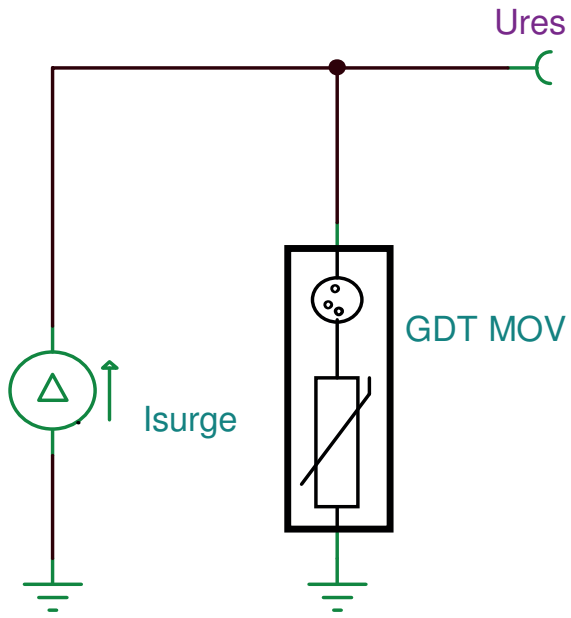

Figure 7: The circuit for numerical simulation of the MOV and GDT in serial connection

The serial connection of GDTs and MOVs takes advantage of both technologies and eliminates certain deficiencies of the single components. GDTs and MOVs together provide faster response and require lower capacitance when power lines are used as communication media. The MOV in this configuration eliminates follow-on currents and allows the GDT arc to be extinguished. The follow-on current is supplied by the electrical power system and flows through the GDT after the discharge current impulse disappears.

The residual voltage at the GDT and MOV terminals (Fig. 6) is observed by a digital oscilloscope and presented in Fig. 8. The residual voltage obtained by measurements is 940 V. Equal values for residual voltage and a

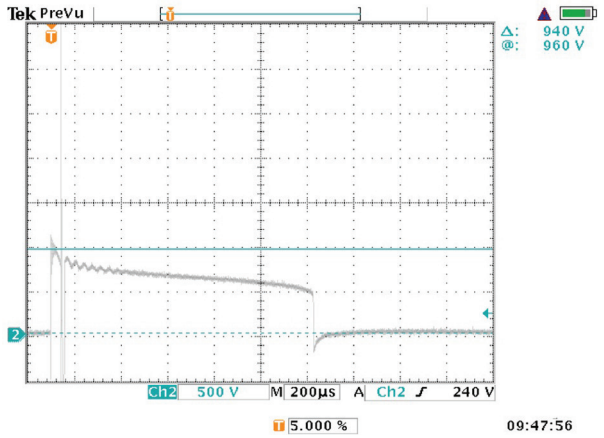

Figure 8: The residual voltage measured using the measurement setup presented in Fig. 6

similar waveform of voltage at the GDT–MOV terminals is obtained by numerical simulation (Fig. 9).

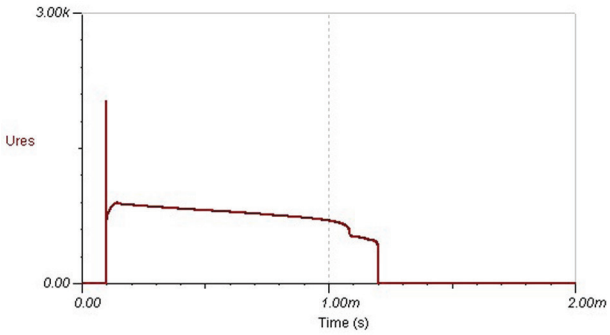

Figure 9: The waveform of the residual voltage obtained by simulation in TINA

The second case of the overvoltage protection laboratory tests and simulations is focused on the measurement of the voltage waveform at the terminals of the MOV and GDT serial connection when the surge impulse (10/700 µs surge pulse shape) and a power line voltage of 50 *Hz* exist simultaneously. The surge impulse appears on the LV network during its operation. In the laboratory measurements and in the numerical simulations, it is assumed that a surge wave appears at a certain moment on an energised LV conductor. The SPD device is connected to a phase conductor, and phase voltage exists during the measurements and numerical simulations.

A schematic representation of the measurement setup is presented in Fig. 10. Measurement equipment consists of: a surge generator TUG-200 (generating an impulse of direct atmospheric discharge 10/700 µs short circuit), an auto-transformer for the power line voltage, an oscilloscope LeCroy (350 MHz, 2,5 GSample/s), a digital scope Tektronix (100 MHz, 1 GSample/s), and a Pearson current monitor model 1423. The currents are measured in the MOV and GDT branch and the power line branch. The voltage drop at the terminals of the GDT and MOV serial connection is also measured.

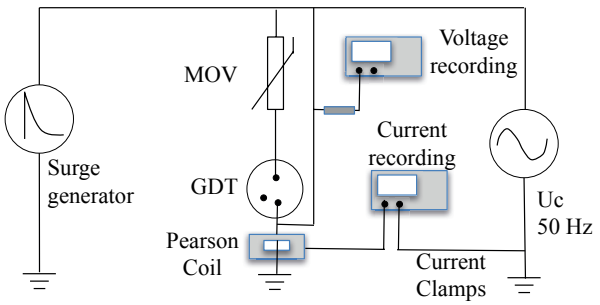

Figure 10: Measurement setup of the GDT and MOV in serial connection

The measurement setup from Fig. 10 is simulated using the TINA software tool. The scheme of the circuit with the GDT and MOV serial connection when the surge impulse (10/700 µs surge pulse shape) and a power line voltage of 400 V peak and frequency of 50 Hz exist simultaneously is presented in Fig. 11. An RC circuit is used to simulate a 10/700 µs single output impulse generator. This type of surge generator is designed according to the description of impulse generators proposed in [22]. The scheme of the 10/700 µs surge generator is shown in Fig. 11. An overvoltage pulse is generated using a capacitor with initial voltage, and with a switch defining the time of the pulse. A capacitor bank, represented by *C1*, will be charged to an initial DC voltage, U_{dc}. The capacitor will be discharged through a wave-shaping RC network. The voltage of the power frequency is added as a branch connected in parallel with the surge generator (Fig. 11).

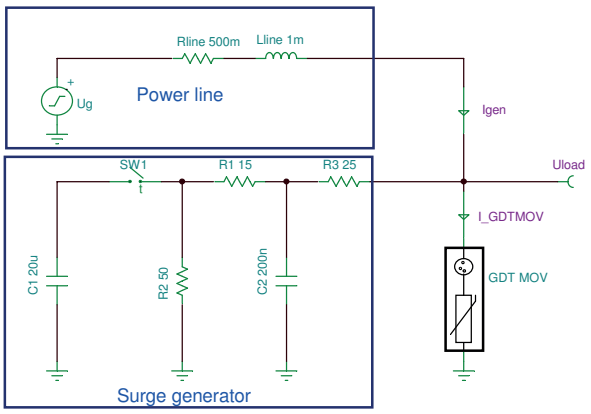

Figure 11: The circuit for the measurement setup of the GDT and MOV in serial connection

The measured values of these three waveforms are presented in Fig. 12. The three signals, presented on the screen of an oscilloscope, have different horizontal scales. The current waveform is indirectly observed through the voltage waveform and presented on the oscilloscope screen as an F1 waveform (Fig. 12). The waveform F1 has a time base of 200 µs/div and a vertical scale of 10 kA/div. The second waveform is current flowing through the power line branch. This signal has a time base of 200 ms/div and a vertical scale of 200 A/div. The third signal is the voltage at the terminals of the GDT and MOV serial connection. This waveform has the same time base as the second signal. The vertical scale is 500 V/div. After the appearance of the surge current impulse (F1 in Fig. 12), the surge arrester reacted and started to conduct. The surge current amplitude is 21 *kA*, with a 10/700 µs current pulse shape. It is evident from Fig. 12 that the surge wave appeared after 40 ms. The current from the surge generator also flows through the power line branch. The maximum value of the current in the power line branch during the surge current pulse is 198 *A*.

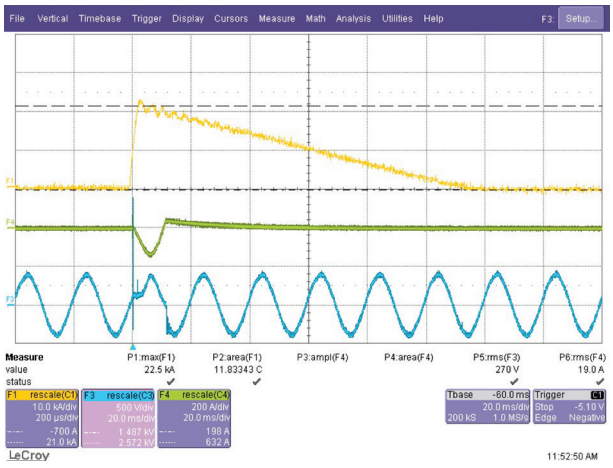

Figure 12: Surge current pulse, current in the power frequency branch and the voltage across the GDT and MOV serial connection

Fig. 13a shows the time diagram of the surge current generator presented in Fig. 11. After the appearance of the surge current pulse, the GDT and MOV responded and started to conduct. The voltage drop across the GDT and MOV stayed below 1000 V (Fig. 13b). The main part of the surge current was grounded through the GDT and MOV surge arrester. A small portion of the surge current during the conductive phase of the GDT and MOV was flowing through the power line branch. Extinguishing of the electric arc is assured when the MOVs are connected in series with GDTs.

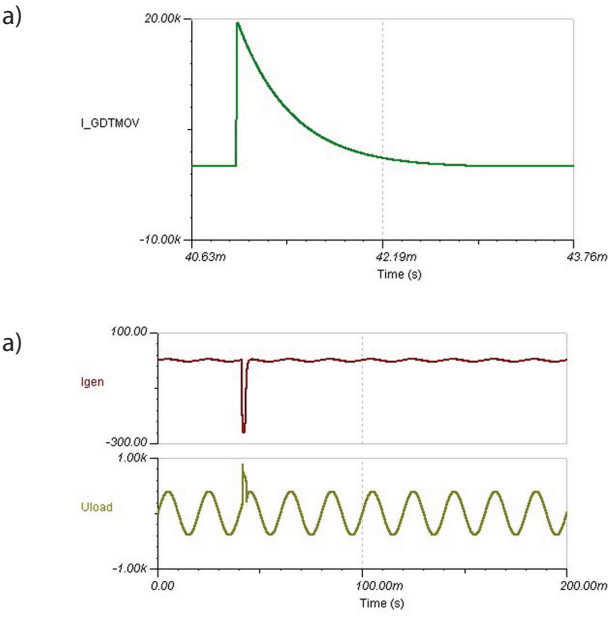

Figure 13: Surge current pulse, current in the power line branch and voltage of power frequency.

5 Conclusions

This paper presented overvoltage component models based on the Verilog-A language utilising a simplified approach to modelling components with nonlinear transfer characteristics and their description with built-in nonlinear functions. GDT and MOV Verilog-A models were provided, and simulations were completed using the TINA circuit simulator. A serial connection of GDTs and MOVs was constructed by creating instances of developed modules. The developed Verilog-A models were used together with SPICE models of other components for the simulation of surge protection devices.

The GDT and MOV serial connection was analysed, and the simulation results were compared with adequate laboratory measurements. Two types of measurements of the response of overvoltage components during the overvoltage impulse are presented. The validation of the developed models is based on a comparison of the residual voltages obtained by measurements and simulations. The first measurement is a standard test of overvoltage components, while the second measurement tests overvoltage components in a real environment.

The difference between simulation results and measurements is directly dependent on the accuracy of mathematical description of physical components at a higher abstraction levels. The compact models of GDT and MOV are based on presented mathematical descriptions. The differences that arise between the simulations and measurement results have been recognized by adjusting the models of surge pulse sources to better fit the measurement results. In the first case, a piecewise linear description of surge pulse is utilized and in the second case modelling with discrete elements is used.

We conclude that varistors connected in series with the arrester are well suited for limiting the follow-on current. The advantages of the serial connection of GDTs and MOVs are proven, and we showed that this topology eliminates certain deficiencies of individual components.

6 References

1. R. B. Standler, *Protection of electronic circuits from overvoltages*, Dover, Publications, Inc. New York, 1989.
2. V. Murko, N. Suljanović, A. Mujčić, J. F. Tasič, Universal SPD coordination towards an effective surge protection of power supply networks, *Journal of Electrical Engineering and Computer Science/ Elektrotehniški vestnik*, Volume 78, No. 3, 2011.
3. T. Ardley, *First Principle of Gas Discharge Tube (GDT) Primary Protector*, www.bourns.com.
4. H. Chen, Y. Du, A comprehensive study on the nonlinear behavior of metal oxide varistors, *33rd International Conference on Lightning Protection (ICLP)*, September 2016.
5. N. Suljanović, A. Mujčić, V. Murko, "Practical issues of metal- oxide varistor modeling for numerical simulations", *International Conference on Lightning Protection ICLP*, Kanazawa, 2006.
6. T. Tuma, A. Buermen, *Circuit Simulation with SPICE OPUS*, Birkhäuser Basel, 2009
7. T. Basso, T. Sinard, T. France. (1997, Jul. 3). Spice model simulates spark-gap arrestor—*EDN access*.
8. J. G. Zola, Gas Discharge Tube Modeling with PSpice, *IEEE Transactions on electromagnetic compatibility*, Vol. 50, No. 4, 2008.
9. EPCOS Product Profile 2017, Surge Arresters and Switching Spark Gaps, EPCOS AG 2017, www.epcos.com.
10. J. Ribič, J. Pihler, J. Voršič, Overvoltage, Overvoltage Protection Using a Gas Discharge Arrester Within the MATLAB Program Tool, *IEEE Transactions on Power Delivery*, Volume: 22, Issue: 4, Oct. 2007.
11. J. Ribič, J. Pihler, J. Voršič, Mathematical Model of a gas discharge arrester based on physical parameters, *IEEE Transactions on Power Delivery*, 99, Feb. 2014.
12. J. Ribič, Impact of line length on the operation of overvoltage protection in LV networks, *Electric Power System Research 121*, Nov. 2014.
13. V. S. Brito, G. R. S. Lira, E. G. Costa, M. J. A. Maia, A Wide-Range Model for Metal-Oxide Surge Arrester, *IEEE Transactions on Power Delivery*, Volume: PP, Issue: 99, May 2017.
14. IEEE Working Group 3. 4. 11, Modeling of Metal Oxide Surge Arresters, *IEEE Transactions on Power Delivery*, Vol. 7, No. 1, January 1992.
15. P. Pinceti, M. Giannettoni, "A simplified model for zinc oxide surge arresters", *IEEE Trans. on Power Delivery,* Vol.14, No.2, 1999, pp. 393-398.
16. F. Fernandez, R. Diaz, "Metal oxide surge arrester model for fast transient simulations", *The International Conference on Power System Transients* IPST'01, Rio De Janeiro, Brazil, 20-24 June 2001, paper 144.
17. B. Žitnik, M. Babuder, M. Muhr, M. Žitnik, R. Thottappillil, Numerical modelling of metal oxide varistors, *Proceedings of the XIVth International Symposium on High Voltage Engineering*, Tsinghua University, Beijing, China, August 25-29, 2005.

18. C. McAndrew, et al. Best Practices for Compact Modeling in Verilog-A, *Journal of Electron Devices Society*, Vol, 3, No. 5, September 2015.
19. K. S. Kundert, O. Zinke, *The Designer's Guide to VERILOG-AMS*, Kluwer Academic Publishers New York, Boston, Dordrecht, London, Moscow, 2004.
20. Accellera, "Verilog-AMS Language Reference Manual, version 2.2", 2004, http://www.accellera.org, 2010.
21. *TINA v10, The Complete Electronics Lab for Windows,* DesignSoft, Inc., 1990-2014. M. J. Maytum, *Impulse generators used for testing low-voltage equipment*, IEE PES- Surge Protective Devices Committee, 2012.
22. M. J. Maytum, *Impulse generators used for testing low-voltage equipment*, IEE PES- Surge Protective Devices Comittee, 2012.

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