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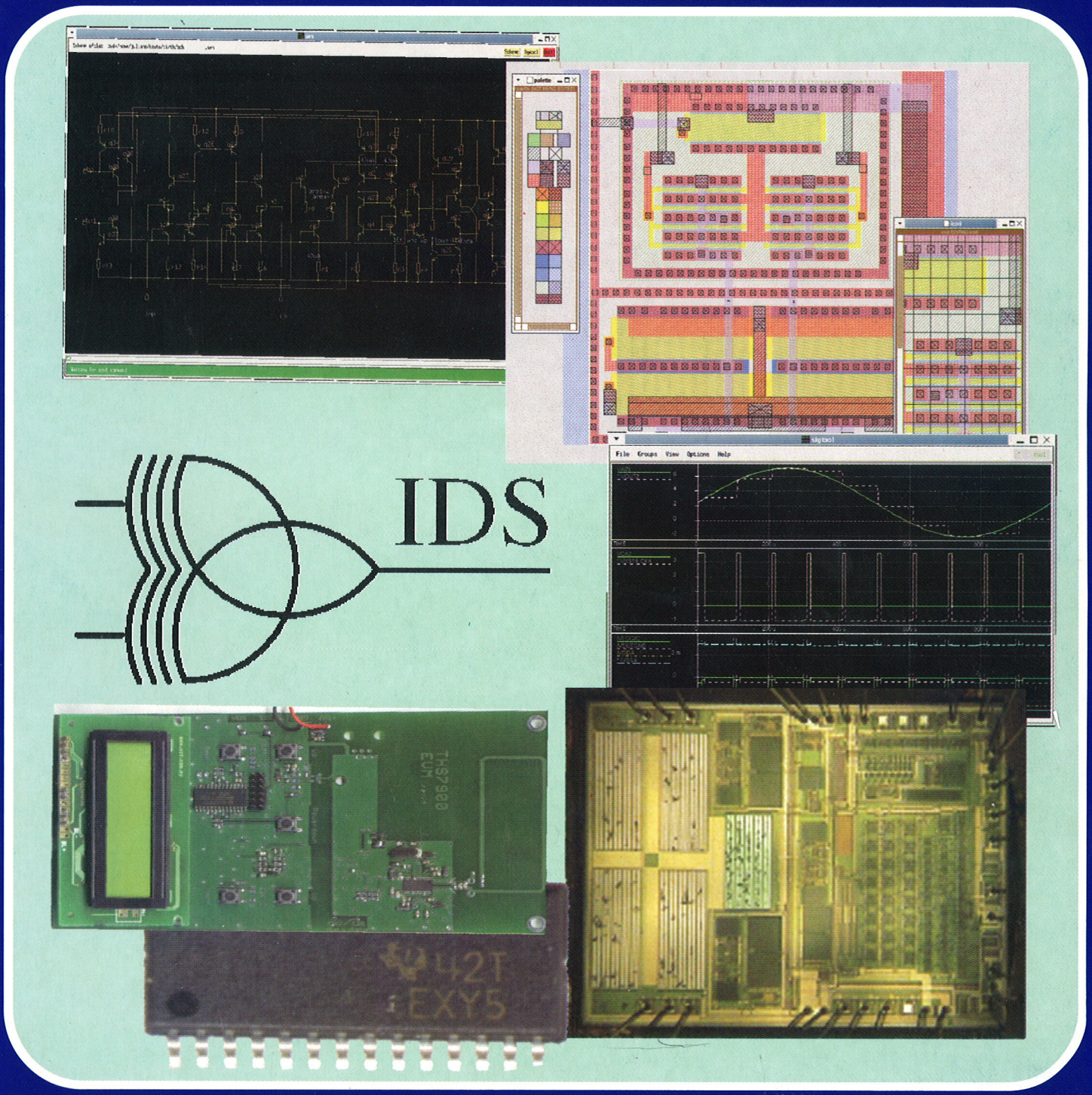
INFORMACIJE MIDEM, LETNIK 34, ŠT. 2(110), LJUBLJANA, junij 2004



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DESIGNING INDUCTORS FOR A FREQUENCY DEPENDENT Q-FACTOR

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Key words: plating, higher harmonics, matching network, nickel plating, nonlinear load, oscillations, plated coil, Q-factor, resonance, RF applications, RF plasma, signal distortion

Abstract: Power dissipation in inductors for radio frequency (RF) applications is a function of frequency because of the skin effect. If a coil is plated with a ferromagnetic material, the dissipation as a function of frequency can be tailored to yield a Q-factor that decreases with frequency much faster than that of an unplated coil. This effect is useful to prevent oscillations at higher harmonics of a frequency of interest. One such application is RF power systems for plasma processing, in which RF plasma presents a time-variable, nonlinear load where nonlinearities introduce harmonic frequencies.

Zasnova tuljave z izrazito frekvenčno odvisnostjo upornosti

Kjučne besede: harmonske frekvence, impedančna prilagoditev, kvaliteta nihajnega kroga, kvaliteta tuljave, načrtovanje RF vezij, nelinearno breme, nelinearno ojačenje, nelinearna vezja, niklanje, oscilacije, resonanca, RF plazma

Izvleček: Upornost tuljave, in z njo povezana intenzivnost prehajanja elektromagnetne v toplotno energijo, je funkcija frekvence zaradi kožnega pojava. Če tuljavo galvaniziramo s feromagnetnim nanosom ustrezne debeline, močno povečamo odvisnost upornosti tuljave od frekvence toka, oziroma z ustreznim feromagnetnim nanosom povzročimo izrazito frekvenčno odvisnost kvalitete tuljave. Pojav je uporaben za preprečevanje oscilacij pri višjih harmonskih frekvencah osnovnega signala, kar predstavlja problem pri, na primer, dovajanju RF energije v plazemske procese.

1. Introduction

Power dissipation in high frequency inductors takes place mostly within the skin depth δ, which is a function of frequency. Magnitudes of the electric field $\vec{E}$, magnetic field $\vec{B}$, and current $\vec{j}$ decrease exponentially with the penetration into the conductor. Skin depth is defined as the depth at which fields and current decrease to *1/e* of their values at the surface. For example, skin depths for copper at frequencies of 1, 10, and 100 MHz are 0.06, 0.02, and 0.003 mm /9/. This is the primary reason to build inductors for RF applications mostly from tubes instead of from solid conductors. Benefits of tube usage are savings in weight, material, and possibility of intra-coil cooling with air circulation. High frequency and high power inductors are used in RF power equipment such as generators, impedance matching networks /1, 3/, and power delivery coils, i.e., antennas /10/. Low power RF inductors are usually made from solid material, i.e., from solid wire since low power implies small dimensions where usage of tubes in inductor manufacturing becomes unrealistic and nonprofitable.

Inductors are classified by inductance and by quality, that is, by Q-factor. This is a measure of a relationship between stored energy and rate of energy dissipation in a component, thus indicating the components' efficiency.

In circuits, the Q-factor is a measure of the quality of a resonance. A high Q-factor is important for the efficiency of RF transmitters and for the sensitivity of RF receivers. A low Q-factor at the higher harmonics of the operating frequency is important to prevent propagation and amplification of harmonics, and, in the worst case, to prevent resonance of a resonant circuit at harmonic frequencies. Such unwanted resonance does happen in plasma processes such as RF plasma enhanced sputtering, etching, coating, and cleaning, where RF induced plasma behaves as a time-variable nonlinear load.

Unwanted resonance at higher harmonics is detrimental to the operation of circuits by causing sustained and transient oscillations that cause noise, signal distortion and the possibility of damage to circuit elements. In plasma processing, such resonance affects quality of the process.

The Q-factor is defined as the ratio between the total energy of a system with periodic action and the energy lost in one period /6/. When the resonance is reasonably narrow (Q ≤ about 3), the Q-factor can be approximated by the resonant frequency divided by the bandwidth:

$$Q = \omega_0 / \Delta\omega . \qquad (1)$$

Bandwidth is defined as the difference between frequencies where circuit response corresponds to 0.7 (or, -3 *dB*) of a maximum response. The Q-factor for a simple resonant circuit (an ideal capacitor coupled to a non-ideal inductor) equals

$$Q = \frac{2\pi E}{|\Delta E|} = \frac{\omega_0 L}{R} = 1/R_L \sqrt{L/C}. \qquad (2)$$

The present paper shows that by plating power inductors one can make a coil's resistance a controlled function of frequency within a certain range. An obvious application is the reduction of the coil's Q-factor at higher harmonics of the operating frequency. We derive here the general design formulae for such an application.

The independent variables are the frequency (*f*), and variables in Figure 1: the tube's inner radius (*a*), the wall thickness (*w*), the plating thickness (*p*), the tube's length (*dL*), the conductances (σ_w, σ_p), the permeabilities (μ_w, μ_p) and the skin depths (δ_w, δ_p) of the wall and plating metals. The power dissipation in such a coil is

$$P = RI^2, \qquad (3)$$

where *I* is the RMS current and *R* is the effective resistance at the given frequency.

It is usually convenient to express a physical property that is a function of geometry and materials (the resistance *R* in this case) as the product of a reference property i.e., R_0 and of a dimensionless factor referred to as a "form factor" i.e., *F*, which characterizes the geometry and materials. Taking as a reference R_0, the resistance of the unplated tube, we may thus write

$$R = R_0 F. \qquad (4)$$

Our objectives are to determine the reference resistance R_0 and the form factor *F* as functions of all listed variables.

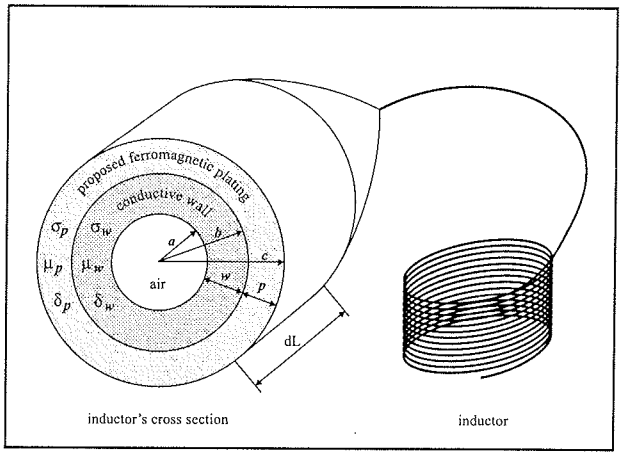

Figure 1 Proposed structure of an inductor for RF power applications.

2. Derivation of the reference resistance R_0, and of the form factor F

The total effective resistance is computed from the total power dissipation as

$$R = P/I^2. \qquad (5)$$

The power dissipation is obtained by integration over the cross section. To this end, we need the current densities

$$\left.\begin{aligned} \vec{j}_p(r) &= \sigma_p \vec{E}_p\ (r) \text{ for } b \le r \le c \\ \vec{j}_w(r) &= \sigma_w \vec{E}_w\ (r) \text{ for } a \le r \le b \end{aligned}\right\}, \qquad (6)$$

where *r* denotes the radial distance from the centerline of the tubing, *b* the outer radius of the tube ($b = a + w$) and *c* that of the plating, ($c = b + p$). The current densities are determined by longitudinal electric fields, which are, respectively

$$\left.\begin{aligned} E_p(r) &= E_0 \exp\left(-(c-r)/\delta_p\right) \\ E_w(r) &= E_0 \exp\left(-p/\delta_p\right)\exp\left(-(b-r)/\delta_w\right) \end{aligned}\right\}, \qquad (7)$$

where E_0 is the field at the outer surface and the skin depths δ_p and δ_w are given by the general expression

$$\delta = \sqrt{\frac{1}{\sigma\mu\pi f}}. \qquad (8)$$

The total current,

$$I = I_p + I_w, \qquad (9)$$

is proportional to the field E_0,

$$\left.\begin{aligned} I_p &= K_p E_0 \\ I_w &= K_w E_0 \end{aligned}\right\} \qquad (10)$$

where the coefficients K_p and K_w characterize the tubing. They depend only on the two metals and on the geometry:

$$\begin{aligned} K_p &= 2\pi\sigma_p \exp\left(-c/\delta_p\right)\int_b^c \exp\left(r/\delta_p\right) r\,dr \\ &= 2\pi\sigma_p\delta_p\left[c - \delta_p - \left(b - \delta_p\right)\exp\left(-p/\delta_p\right)\right], \end{aligned} \qquad (11)$$

$$\begin{aligned} K_w &= 2\pi\sigma_w \exp\left(-p/\delta_p\right)\exp\left(-b/\delta_w\right)\int_a^b \exp\left(r/\delta_w\right) r\,dr \\ &= 2\pi\sigma_w\delta_w \exp\left(-p/\delta_p\right)\left[\left(b-\delta_w\right) - \left(a-\delta_w\right)\exp\left(-w/\delta_w\right)\right]. \end{aligned} \qquad (12)$$

The field variable E_0 may now be expressed as a function of the total current *I*,

$$E_0 = \frac{I}{K_p + K_w}. \qquad (13)$$

The power dissipated in a length *dL* of plated tubing is

$$P = P_w + P_p = \int_b^c dP_p + \int_a^b dP_w, \qquad (14)$$

where

$$dP_p = \frac{\rho_p dL}{2\pi r dr}\left[2\pi r dr j_p\right]^2 = 2\pi\rho_p dL j_p^2 r dr, \qquad (15)$$

$$dP_w = \frac{\rho_w dL}{2\pi rdr}\left[2\pi rdrj_w\right]^2 = 2\pi\rho_w dL j_w^2 rdr. \qquad (16)$$

Integration yields

$$\begin{aligned} P_p &= 2\pi\rho_p dL\int_b^{b+p} j_p^2 rdr \\ &= 2\pi\rho_p\sigma_p^2 E_0^2 dL\exp\left(-2c/\delta_p\right)\int_b^c \exp\left(2r/\delta_p\right)rdr \\ &= I^2\frac{\pi\sigma_p\delta_p dL}{\left(K_p+K_w\right)^2}\left(\left(c-\frac{1}{2}\delta_p\right)-\left(b-\frac{\delta_p}{2}\right)\exp\left(-2p/\delta_p\right)\right) \end{aligned} \qquad (17)$$

$$\begin{aligned} P_w &= 2\pi\rho_w dL\int_a^b j_w^2 rdr \\ &= I^2\frac{2\pi\rho_w\sigma_w^2 dL}{\left(K_p+K_w\right)^2}\exp\left(-2p/\delta_p\right)\exp\left(-2b/\delta_w\right)\int_a^b \exp\left(2r/\delta_w\right)rdr \\ &= I^2\frac{2\pi\rho_w\sigma_w^2 dL}{\left(K_p+K_w\right)^2}\exp\left(-2p/\delta_p\right)\left(\left(b-\frac{\delta_w}{2}\right)-\left(a-\frac{\delta_w}{2}\right)\exp\left(-2w/\delta_w\right)\right) \end{aligned} \qquad (18)$$

By relation (5), the effective resistance is

$$\begin{aligned} R = &\frac{\pi\sigma_p\delta_p dL}{\left(K_p+K_w\right)^2}\left(b+p-\frac{\delta_p}{2}-\left(b-\frac{\delta_p}{2}\right)\exp\left(-2p/\delta_p\right)\right) \\ &+\frac{\pi\sigma_w\delta_w dL}{\left(K_p+K_w\right)^2}\exp\left(\frac{-2p}{\delta_p}\right)\left(b-\frac{\delta_w}{2}-\left(a-\frac{\delta_w}{2}\right)\exp\left(\frac{-2w}{\delta_w}\right)\right), \end{aligned} \qquad (19)$$

where

$$K_p = 2\pi\sigma_p\delta_p\left(b+p-\delta_p-\left(b-\delta_p\right)\exp\left(\frac{-p}{\delta_p}\right)\right) \qquad (20)$$

$$K_w = 2\pi\sigma_w\delta_w\exp\left(\frac{-p}{\delta_w}\right)\left(b-\delta_w-\left(a-\delta_w\right)\exp\left(\frac{-w}{\delta_w}\right)\right). \qquad (21)$$

The reference resistance corresponds to the special case of no plating, i.e., $p = 0$,

$$R_0 = \frac{\pi\sigma_w\delta_w dL}{K_{w0}^2}\left(b-\frac{\delta_w}{2}-\left(a-\frac{\delta_w}{2}\right)\exp\left(\frac{-2w}{\delta_w}\right)\right), \qquad (22)$$

where

$$K_{w0} = 2\pi\sigma_w\delta_w\left(b-\delta_w-\left(a-\delta_w\right)\exp\left(\frac{-w}{\delta_w}\right)\right). \qquad (23)$$

The reference resistance of a tube is a function of eight variables (three geometric variables, four material constants and frequency):

$$R_0 = f\left(dL, a, w; \sigma_w, \sigma_p, \delta_w, \delta_p; f\right),$$

likewise with the form factor, with the modification that the form factor does not depend on the length dL, but rather on the plating thickness p,

$$F = F\left(a, w, p; \sigma_w, \sigma_p, \delta_w, \delta_p, f\right).$$

3. Impact of plating thickness and frequency on the form factor F

Explicitly writing the full functions for R_0 and F is impractical on the printed page, but also unnecessary for practical calculations by computer. To get insight into the form factor, we consider two examples: a copper tube (a = 5 mm, w = 1 mm) plated with nickel, (a ferromagnetic material - assumed linear), and a nickel tube of the same cross-section plated with copper. The material properties are /9/:

$$\sigma_{cu} = 5.8\times10^7\ \text{S/m},$$
$$\sigma_{ni} = 1.1\times10^7\ \text{S/m},$$
$$\mu_{cu} = 4\pi\times10^{-7}\ \text{H/m},$$
$$\mu_{ni} = 250\times4\pi\times10^{-7}\ \text{H/m},$$
$$\delta_{cu} = \frac{0.0670}{\sqrt{f}}\ \text{mm},$$
$$\delta_{ni} = \frac{0.0088}{\sqrt{f}}\ \text{mm}.$$

For the purpose of this calculation, we designed and coded a simulation tool in C++ Builder. Other tools, i.e., simulation packages for mathematics could alternatively have been utilized for the simulation.

Displaying the form factor as a function of plating thickness (in the range of 0 to 0.07 mm) and frequency (in the range of 0 to 50 MHz), we obtain the graph in Figure 2.

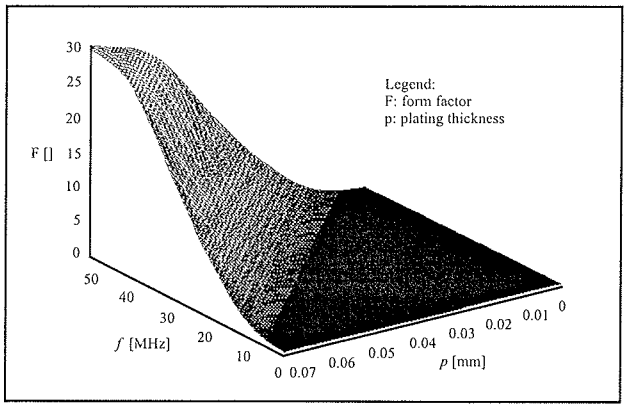

Figure 2 Form factor F for nickel plating on copper tubing.

For p = 0 μm, we have F = 1 at all frequencies, which is exactly true by definition, since, in this case, $R = R_0$. We also have F = 1 for direct current, since the thin plating of nickel affects the DC resistance of the copper tube negligibly. The greatest effect is F = 30, achieved at 50 MHz and 70 μm of plating.

Interchanging the metals and leaving the geometry unchanged results in the graph in Figure 3.

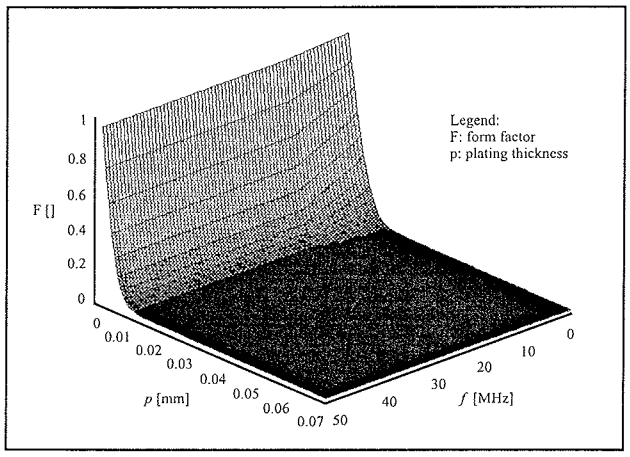

Figure 3 Form factor F for copper plating on nickel tubing.

DC resistance gradually decreases as the plating thickness of the better conductor increases. The same is true at all frequencies, but the effect is more pronounced at higher frequencies. This is because less current flows in the more resistive nickel tubing as the skin depth limits it to the copper plating.

4. Form factor F and the quality of resonance

A low form factor *F*, i.e., low resistance of an inductor is preferred to minimize losses and to reach high quality for resonant circuits at a resonant frequency. A high form factor, i.e., high resistance of an inductor is preferred to obtain high losses at frequencies where resonance should not take place. The authors predict that the frequency-dependent form factor of an inductor will be recognized as important when:

- a power inductor delivers power to a nonlinear load, such as RF plasma where nonlinearities /8/ introduce harmonic frequencies,
- the load capacitance varies, as it is the case with RF plasma at the onset of plasma excitation /2, 4, 5/, and when
- the RF signal on the output of RF power stages, at the input of the load impedance matching networks, is less than a perfect sine (power amplifiers do trade fidelity for efficiency, i.e., efficient class AB, B, C, and E /7/ RF amplifiers introduce higher harmonics).

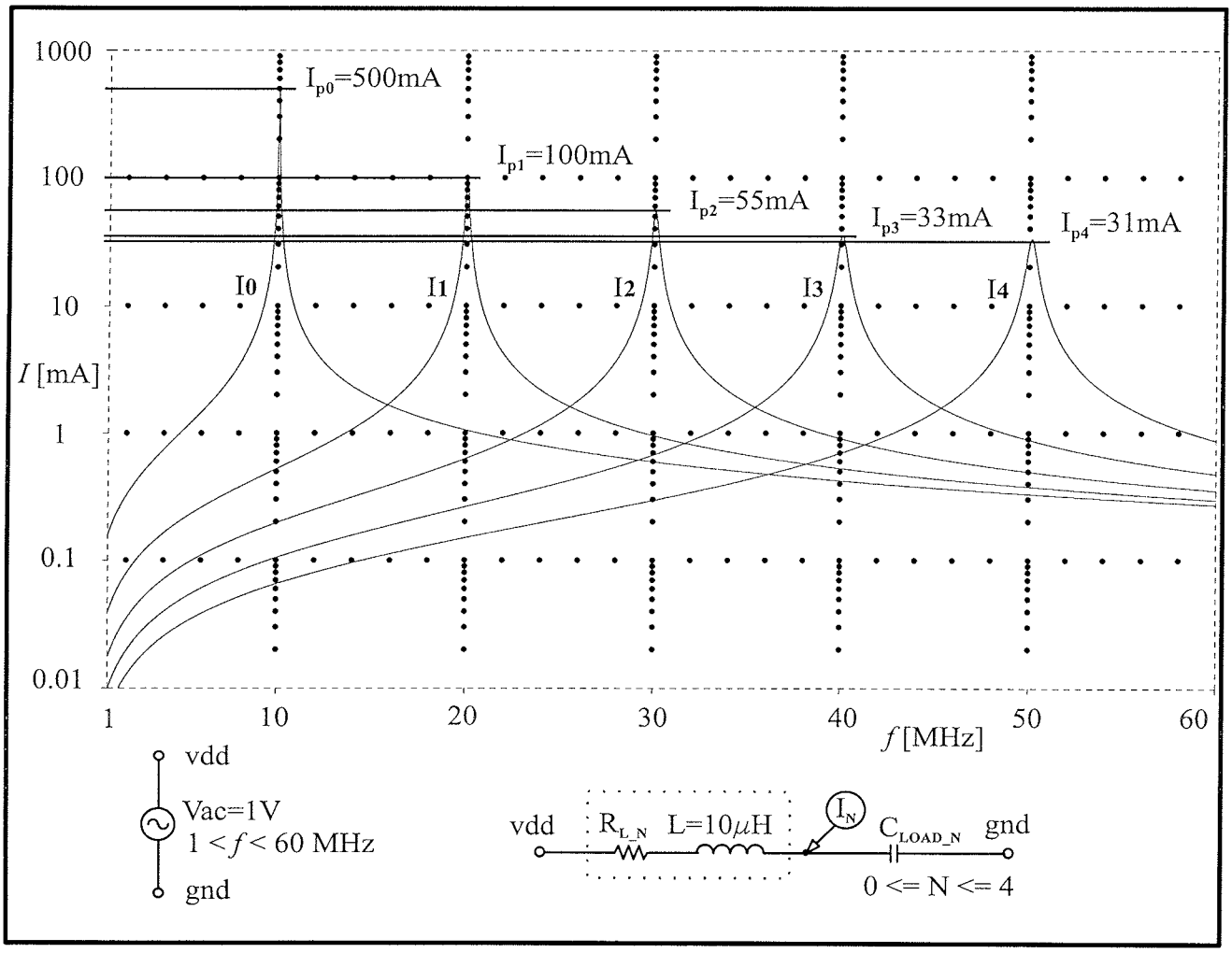

Figure 4 Frequency responses of five series resonance circuits with different Q-factors.

Figure 4 shows frequency responses of five series resonance (SR) circuits, built from ideal capacitors, and from inductors with L = 10 mH and with different Q-factors. Form factors are read from Figure 2 for 70 mm nickel plating at 10, 20, 30, 40, and 50 MHz, and R_0 is one Ohm. Corresponding inductor resistances at 10 MHz and at the first four harmonics are 2, 9.5, 18, 28, and 30 Ohm.

$$\mathrm{SR0}: f_r = 10\ \mathrm{MHz},\ Q\ \mathrm{B}320,\ I_{peak} = 500\ \mathrm{mA},$$
$$(R_L = 2\ \mathrm{Ohm},\ C_{LOAD} = 25.33\ \mathrm{pF},)$$

$$\mathrm{SR1}: f_r = 20\ \mathrm{MHz},\ Q\ \mathrm{B}130,\ I_{peak} = 100\ \mathrm{mA},$$
$$(R_L = 9.5\ \mathrm{Ohm},\ C_{LOAD} = 6.33\ \mathrm{pF},)$$

$$\mathrm{SR2}: f_r = 30\ \mathrm{MHz},\ Q\ \mathrm{B}100,\ I_{peak} = 55\ \mathrm{mA},$$
$$(R_L = 18\ \mathrm{Ohm},\ C_{LOAD} = 2.81\ \mathrm{pF},)$$

$$\mathrm{SR3}: f_r = 40\ \mathrm{MHz},\ Q\ \mathrm{B}100,\ I_{peak} = 33\ \mathrm{mA},$$
$$(R_L = 28\ \mathrm{Ohm},\ C_{LOAD} = 1.58\ \mathrm{pF},)$$

$$\mathrm{SR4}: f_r = 50\ \mathrm{MHz},\ Q\ \mathrm{B}100,\ I_{peak} = 31\ \mathrm{mA},$$
$$(R_L = 30\ \mathrm{Ohm},\ C_{LOAD} = 1.01\ \mathrm{pF},)$$

The resonant current ratios of a 10 MHz signal and its first four harmonics are 1 / 0.20 / 0.11 / 0.07 / 0.06. Were the Q-factor of an inductor not frequency-dependent, then all five resonant currents would be equal. That being the case, a resonant circuit would be more sensitive to propagation of harmonic frequencies (introduced by nonlinear loads and to some extent by nonlinear gain stages) and to resonance at harmonic frequencies (as load capacitance changes, as it is the case with the capacitance of RF plasma). In RF plasma processing, impedance matching networks address changes in load impedance. However, the frequency-dependent Q-factor of inductors reacts to load changes instantly since it is implemented in the inductors' material structure, which has no built-in memory[1] and therefore reacts instantly.

5. Conclusion

Power dissipation in high frequency inductors takes place mostly within the skin depth, which is a function of frequency. By plating high current inductors used in RF power equipment, one makes the coil's resistance a controlled function of frequency within a certain range. An obvious application is the reduction of the Q-factor at higher harmonics of the operating frequency. This effect needs to get recognition in applications with time-variable and/or nonlinear components that introduce higher harmonics.

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1 *In matching networks, motors adjust geometries of variable capacitors to adjust impedances. Matching process takes more or less time, depending on the difference between the new and the last setting.*

PARALLEL SIZING OF ROBUST ANALOG ICs

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Key words: circuit sizing, analog IC, parametric optimization, parallel optimization, CAD.

Abstract: Automated robust IC design is a time consuming process. The resulting circuit must fulfill all the performance constraints in several different operating conditions and under the influence of different manufacturing process variations (corners). To achieve this, a large number of circuit analyses must be performed for the circuit, considered by the sizing algorithm. By distributing these simulations among multiple computers speedup can be obtained. A major problem is the synchronous nature of the optimization algorithm that in combination with variable duration of a circuit analysis causes the computers in the parallel system to be idle. This results in a reduction of speedup. The paper presents the corner parallel approach to the problem of parallel robust analog IC sizing. The method is tested with a sample opamp sizing problem. The speedups are measured, and an approach is proposed for reducing the idle time of the computers.

Vzporedno dimenzioniranje robustnih analognih integriranih vezij

Kjučne besede: dimenzioniranje vezij, analogna integrirana vezja, parameterska optimizacija, vzporedna optimizacija, računalniško podprto načrtovanje.

Izvleček: Avtomatsko robustno načrtovanje analognih integriranih vezij je časovno zahteven postopek. Cilj je najti vezje, ki zadosti vsem načrtovalskim zahtevam za dano območje pogojev delovanja in variacij parametrov postopka izdelave (vogalnih točk). V ta namen je potrebno narediti veliko število analiz za vsako vezje, ki ga računalnik med postopkom iskanja preizkusi. S porazdelitvijo teh analiz med več računalnikov je mogoče postopek pospešiti. Vendar pa sinhrona narava optimizacijskega postopka v kombinaciji s spremenjlivo dolžino analize povzroči, da so računalniki v vzporednem sistemu del časa brez dela. Rezultat je zmanjšana pospešitev postopka. Članek opisuje pristop k paralelizaciji robustnega načrtovanja vezij preko porazdelitve vogalnih točk med več računalnikov. Podani so rezultati v odvisnosti od števila vzporedno računajočih računalnikov. Predlagan je tudi postopek za skrajšanje časa, med katerim so računalniki brez dela.

1 Introduction

As the competition in the IC design industry is becoming sharper, methods for automating parts of the IC design process are gaining on importance /1/. Up to recently circuit simulation was the tool that gave "the edge" to an IC designer. It may have taken a relatively long time for a circuit simulator to evaluate circuit's performance under the influence of various operating conditions and manufacturing process variations, but that was compensated with designer's knowledge and experience in choosing circuit parameter values. Experienced designers are capable of sizing a circuit in a reasonable amount of time when compared to the time spent for simulation. Various approaches for speeding up the simulation were developed and tested during that time /2/.

The available computing power steadily increased and the simulation time began to decrease until it reached the point where simulation is no more a bottleneck in the design process. This trend is becoming more and more obvious as the techniques (e.g./3/, /4/) and tools (e.g. /5/, /6/) for automating the circuit sizing process begin to appear. These tools put an optimization algorithm (/7/, /8/) in the role of a human designer. The basic idea is to emulate a part of the designer's knowledge and experience by transforming the search for a "better circuit" into the search for a lower cost function (CF) value. An optimization algorithm searches for such circuit parameter (e.g. MOS widths and lengths) values where the CF reaches its lowest value. When using such tools the designer's job is to define

- circuit structure (e.g. the unsized schematic of an opamp),
- element matching /9/ (some circuit element parameters are not independent, e.g. width and length of the two MOS transistors in a differential pair),
- which analyses to perform and what circuit characteristics to extract from them (we consider circuit area as yet another circuit characteristic, although it is not the result of some analysis),
- set of corners for which the circuit is to be analyzed (a corner is a particular combination of operating conditions and manufacturing process variations), and
- performance constraints on circuit characteristics and their relative importance with respect to each other.

The optimizer then handles the rest of the work. Of course if the performance constraints are set to some values that cannot be achieved with the given circuit structure, the resulting circuit doesn't fulfill all performance constraints.

A typical optimization run requires the evaluation of several hundred up to several thousand different circuits with the same structure and different parameter values. As every circuit has to be evaluated in all of the specified cor-

ners, the optimization may take a long time (at the time being, using a state-of-the-art computer it takes typically from a few hours up to several days). Therefore every reduction of this time represents a significant benefit to the designer. There exist different approaches for accelerating the process of optimization by means of parallelization.

This paper presents the so-called corner-parallel approach. The remainder of the paper is subdivided as follows. First the method of constructing the cost function is presented. The various levels at which parallelism can be introduced are briefly discussed. The use of PVM /10/ for implementing the corner-parallel approach is described and runtimes for a sample circuit sizing problem are given. Finally the synchronization penalty is discussed and an approach for its alleviation is proposed.

2 Defining the cost function

2.1 Circuit design and corner points

In order to obtain a robust circuit it must exhibit adequate performance in all corners. A corner is a combination of some process variation (like the worst power and worst speed MOS corner) and M operating conditions (like temperature, supply voltage, etc.). Suppose that we have n_0 possible process variations. Let n_i denote the number of different values for the i-th operating condition that are of interest to the designer. Then the total number of corner points is

$$K = \prod_{i=0}^{M} n_i \tag{1}$$

Of course (1) quickly grows beyond any reasonable value. Therefore the designers usually examine the circuit for a subset of corners (C_S). M_S denotes the number of corners in C_S.

The performance of the circuit can be described by a vector $\underline{y} = [y_1,...,y_N] \in R^N$ of N real valued performance measures (like gain, bandwidth, rise time, etc.). When sizing a circuit the optimizer has to find the values of n circuit parameters represented by a vector $\underline{x} \in R^n$. The circuit itself can be viewed as a transformation (2) that for some combination of n circuit parameters denoted by vector $\underline{x}$ and some corner point denoted by q produces a vector of circuit characteristics $\underline{y}$.

$$D:(\underline{x},q) \mapsto \underline{y} \qquad \underline{x} \in R^n, q \in C, \underline{y} \in R^N \tag{2}$$

$$y(\underline{x},q) = [y_1(\underline{x},q), y_2(\underline{x},q),..., y_N(\underline{x},q)]$$
$$= [D_1(\underline{x},q), D_2(\underline{x},q),..., D_N(\underline{x},q)]$$

The designer's goal is to either minimize or maximize the performance measure. Typically one tries to minimize measures like rise time and fall time and maximize measures like bandwidth and gain. Let h_i be 1 if y_i is to be maximized and 0 if it is to be minimized. Now let b_i denote the worst still acceptable y_i value. A circuit has acceptable performance with respect to performance measure y_i under minimization if $y_i \le b_i$. On the other hand if y_i is being maximized, acceptable circuit performance with respect to y_i requires $y_i \ge b_i$.

Finally the circuit is considered to have acceptable performance if its performance is acceptable with respect to all performance measures for all corners $q \in C_S$.

Let y^{worst} denote the vector of worst performance measure values across all corners.

$$y_i^{worst}(\underline{x}) = \begin{cases} \min\limits_{q \in C_S} y_i(\underline{x},q) & h_i = 1 \\ \max\limits_{q \in C_S} y_i(\underline{x},q) & h_i = 0 \end{cases} \tag{3}$$

2.2 Constructing the cost function

Suppose $g(x)$ is a continuous monotonically increasing function defined for $x \ge 0$. Then

$$f(x) = \begin{cases} 0 & x < 0 \\ g(x) - g(0) & x \ge 0 \end{cases} \tag{4}$$

We know that the optimizer searches for the lowest CF value. Therefore better performing circuits should be assigned a lower CF value. For that purpose a partial CF can be defined using (3) and (4):

$$F_P(\underline{y}) = \sum_{i=1}^{N} \left((1-h_i) f\left(\frac{y_i^{worst} - b_i}{A_i} \right) + h_i f\left(\frac{b_i - y_i^{worst}}{A_i} \right) \right) \tag{5}$$

Finally the CF that is used by the optimizer is the sum of partial CF values across all corners.

$$F(\underline{x}) = \sum_{q \in C_S} F_P(y(\underline{x},q)) \tag{6}$$

By minimizing this function the optimizer actually searches for the circuit (vector of parameters $\underline{x}$) with minimal constraint violation. If a circuit with CF value 0 is found, it means that all the constraints are satisfied and the optimization can be stopped.

The optimizer must consider the fact that the simulator used for evaluating the circuit is not always capable of solving the circuit equations. As a matter of fact there exists a plethora of pathologic circuits for which the simulator fails to find a solution. In such a case we assign either $y_i = L$ (if $h_i = 0$) or $y_i = -L$ (if $h_i = 1$) to all y_i that can't be evaluated due to simulator failure. L is a large positive value. Such strategy produces a very high CF value for pathological circuits and thus forces the optimizer to avoid those parts of the parameter space, where such circuits are found.

3 Parallel circuit sizing

The innermost level (level 1 in fig. 1) at which parallelism can be introduced is the simulator level. If one wants to exploit parallelism at this level a special simulator is required. In the past a lot of effort was invested in developing such

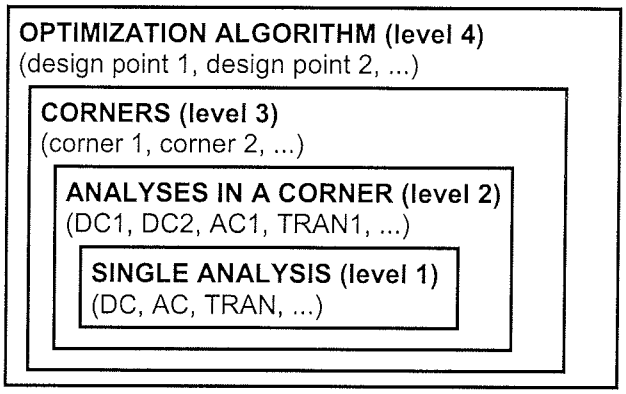

Fig 1: possible levels of parallelism.

simulators, but none of them grew to be as general and widespread as today's circuit simulators (e.g. /12/).

The outermost level is the optimization algorithm level. The amount of speedup that can be gained from parallelism at this level depends on the type of optimization algorithm. Genetic algorithms /13/ (GA) and simulated annealing /14/ (SA) are well suited for such parallel execution. Unfortunately they require many CF evaluations before they reach a solution. So the large speedup that can be gained from parallel execution is lost due to the fact that these algorithms are extremely time consuming per se. On the other hand algorithms like the simplex algorithm need fewer CF evaluations (between one and two orders of magnitude less than SA and GA), but the amount of speedup that can be obtained by introducing parallelism seems to be limited (/15/, /16/).

What remains are the two intermediate levels. As a matter of fact there really is no distinct border between them. The two levels are depicted separately in fig. 1 to emphasize the way the CF is evaluated, i.e. for every corner several different circuit analyses are performed and every one of them is an independent entity that can be simulated in an independent simulator run. One or more performance measures are then extracted from results of every analysis and are used to build a part of the CF according to (5). Introducing parallelism at this level means that the CF evaluation is distributed among several computers, where every computer evaluates the part of the cost function that belongs to a subset of corners and analyses. Effectively this means that one computer runs one or more analyses and extracts performance measures from the obtained analysis results. In the remainder of this paper we focus on corner-level parallelism (level 3).

In the parallel computing community two major tools are available for implementing parallel algorithms: PVM /10/ and MPI /11/. MPI is the official standard. Recently the PVM library gained a wide audience due to its flexibility and the portability of its open source implementation. Today it is recognized as the de-facto standard for parallel processing. Currently the most popular hardware platform for parallel processing is the loosely coupled (ethernet) cluster of ordinary PCs, usually running LINUX.

PVM consists of two parts. The PVM deamon runs as a server on every computer of the cluster. It manages processes and the communication between them. The second part is the PVM library that comprises a large set of C

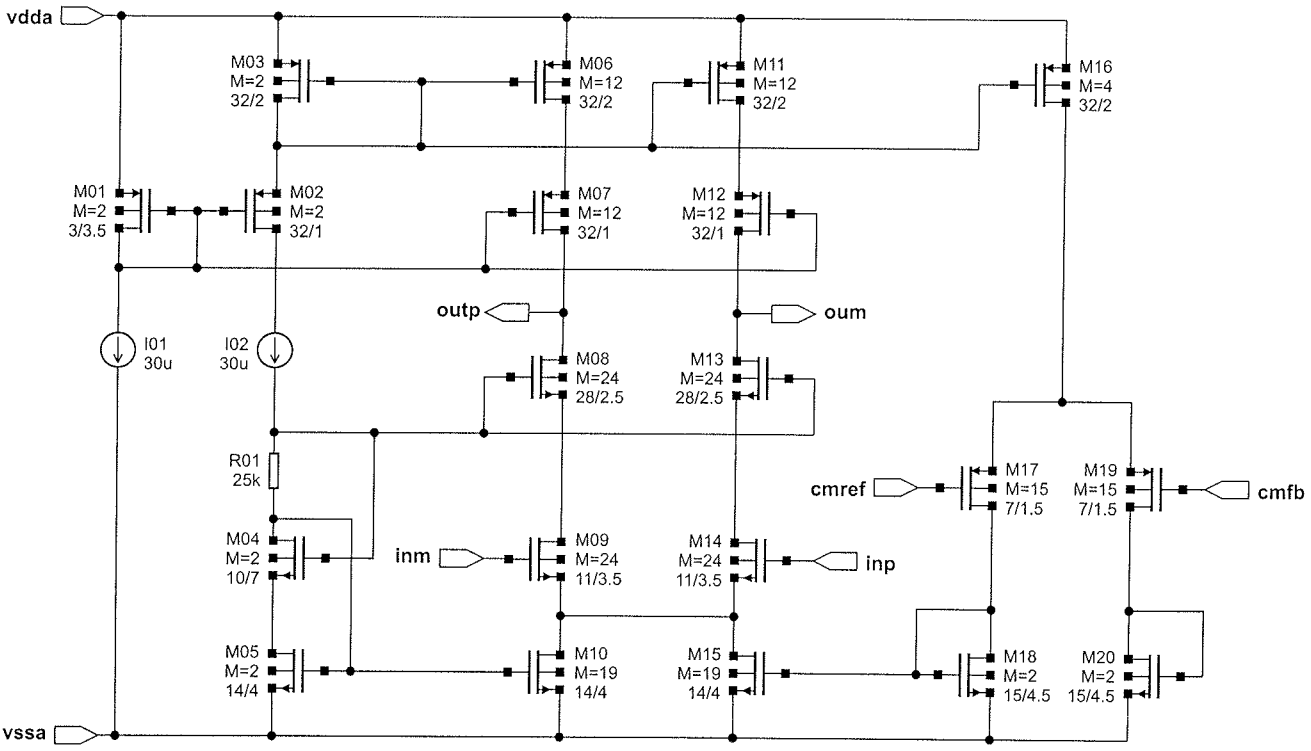

Fig. 2: Sample opamp with M and W/L values. The scale is 0.3μm (all W/L values must be multiplied by 0.3μm to obtain physical dimensions).

functions for process management, and interprocess communication. Typically a PVM application starts as an ordinary process on the master computer. Upon entering PVM the process becomes the master process. Next it spawns worker processes on remote computers in the cluster upon which the parallel algorithm can start executing.

The work is divided among the workers in such a manner that every worker handles one corner (one $q \in C_S$), i.e. one term from the sum in (6). One doesn't have to have M_S computers in the cluster for that. If the number of computers (P) is smaller than M_S then at first only P corners are divided among the workers. The worker that first finishes evaluating its corner obtains a new corner from the master computer. This continues until the master computer collects the partial CF values for all corners. After that the optimization algorithm on the master computer selects a new point ($\underline{x}$) in the parameter space and the parallel CF evaluation is repeated for that point.

The above-proposed parallel approach is synchronous. The evaluation of the CF from collected partial CF values at the master computer represents a synchronization point. The master cannot continue from this point until all partial CF values are collected from the workers. The duration of a partial CF evaluation is not constant since the simulator (SPICE) solves the circuit by means of various iterative techniques. As a consequence some workers finish sooner than the others. If the master doesn't have a partial CF evaluation for them that will keep them busy, those workers remain idle until the master starts evaluating the next trial circuit.

4 Example

To illustrate the proposed approach to parallel circuit sizing, a sample opamp circuit (fig. 2) was used. 9 corners were taken into account representing all possible combinations of 3 Vdd values (3.0V, 3.3V, and 3.6V), 3 operating temperatures (-10°C, 27°C, and 80°C), and 3 MOS corners (TYP, BCS, WCS). W/L/M values in fig. 2 represent a circuit sized by an experienced designer.

The test circuit in fig.3 was used to evaluate the performance of the circuit in fig. 2 during the process of sizing. Several analyses were performed and performance measures were extracted from the results for every corner. Table 4 lists the performance measures, goals, and corresponding penalty coefficients from equation (5).

Although there are 20 MOS transistors in the circuit with 3 adjustable parameters per transistor, the number of optimization parameters is only 18. This number is reduced by grouping transistors like current mirrors and differential pairs in groups /9/. Table 1 lists the optimization parameters, the MOS transistors groups to which these parameters belong and their explicit constraints.

The parallel approach was tried out with different numbers of workers. The workers and the master were AMD ATHLON 2100XP computers running LINUX with PVM. In the first set of tests the optimization was stopped after 160 CF evaluations and the runtime was measured. Table 2 lists the runtimes, the corresponding speedups, and the overall CPU usage. Speedup was obtained by dividing the time spent in a single worker run with the time spent in a N-worker run. The CPU usage was obtained by dividing the

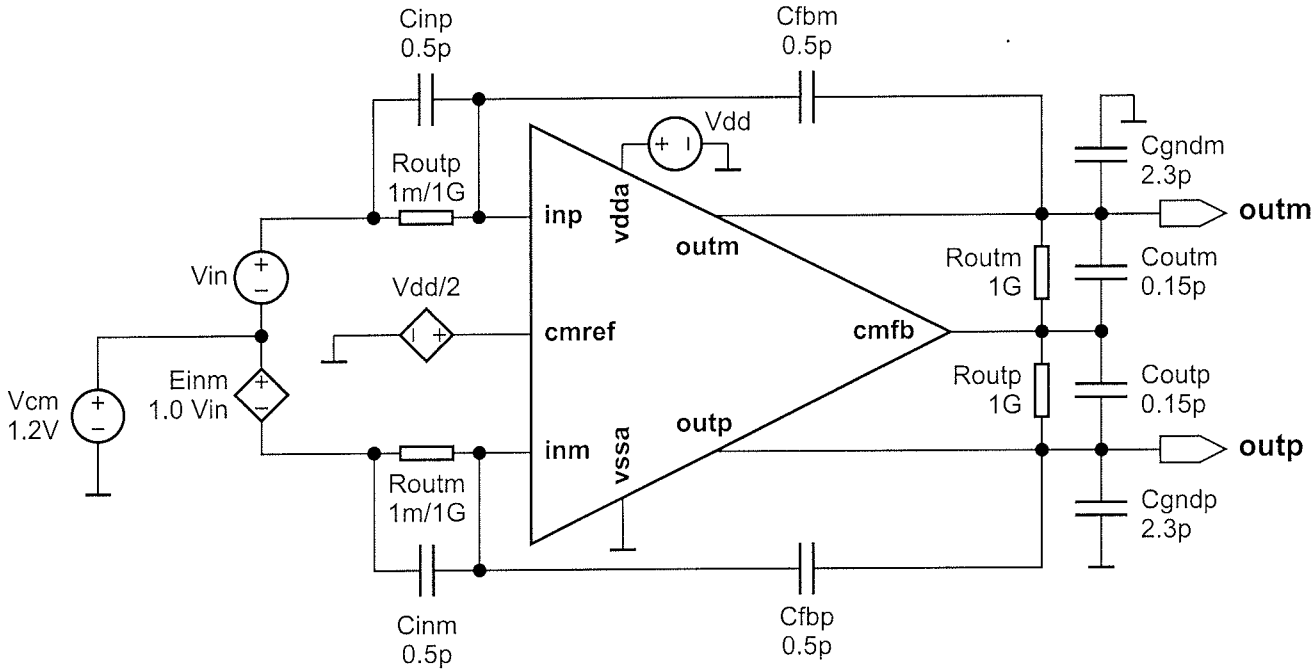

Fig 3: The test circuit. If two values are specified for some element, the first one is valid for all analyses but the transient. For the transient analysis the second value is used.

Table 1: Optimization parameters and matching. The scale is 0.3μm. During optimization widths and length are rounded to the nearest multiple of 0.5. M factor is rounded to the nearest integer.

W=2..50	L=1..10	W=10..50	L=1..10	L =1..10	W=10..50	L=2..10	W=10..50	L=2..10
M1	M1	M2,M3,M6, M7,M11, M12,M16	M2,M7, M12	M6,M6, M11,M16	M4	M4	M5,M10, M15	M5,M10, M15

W=10..50	L=1..10	W=10..50	L=1..10	M=6..24	W=2..10	L=1..10	W=5..50	L=2..10
M8,M13	M8,M13	M9,M14	M9.M14	M10,M15	M17,M19	M17,M19	M18,M20	M18,M20

speedup with the number of workers. From the obtained results it is clear that using 4-5 workers is a reasonable choice. This way speedup values around 2.7 can be obtained.

A large part of the performance degradation (overall CPU usage below 1.0) can be attributed to the variations of the partial CF evaluation time. If the master has no more partial CF evaluations for the current point in the design space, the workers that finish sooner remain idle until the master collects all partial CF values and moves on to the next point in the design space. It is often the case that the designer wants to try several different tradeoffs. Such tradeoffs can be examined by executing multiple optimization runs. If these runs are executed concurrently on the given set of workers one can expect a decrease of worker idle time. With more than one optimization run taking advantage of a worker, the probability that all of the optimization runs will leave the worker idle at some point in time decreases with the number of concurrent runs. Table 2 illustrates this for the case of 2 and 3 concurrent optimization runs.

For multiple concurrent optimization runs the equivalent time is obtained by dividing the total run time with the number of concurrent runs. This figure can be compared directly to the duration of a single run on a single worker (t_1). The quotient of t_1 and equivalent time represents the effective speedup. Finally the overall CPU usage is obtained by dividing the effective speedup with the number of workers. Effective speedup for 5 workers improved to 3.6 (2 concurrent optimization runs) and 4.2 (3 concurrent optimization runs).

With these indications the second set of tests was conducted where several full optimization runs were executed. This time the optimization was stopped when the final solution was found (after 1965 CF evaluations). One run with a single worker and several runs with 5 workers were conducted. Table 3 lists the runtime, equivalent runtime per optimization run, effective speedup, and overall CPU usage. The speedup and overall CPU usage are similar to the ones obtained from truncated runs (stopped after 160 CF evaluations).

Table 3: Performance for different numbers of concurrent parallel optimization runs on 1 and 5 workers.

	1 worker	5 workers		
	1 run	1 run	2 runs	3 runs
Total time [s]	3870.1	1391.3	2170.5	2871.6
Equivalent time [s]	3870.1	1391.3	1085.3	957.2
Effective speedup	1.00	2.78	3.57	4.04
Overall CPU usage	1.00	0.56	0.71	0.81

The final results are presented in table 4. It is worth noting that the computer started from an initial point that wasn't even a feasible opamp. Using 5 workers the computer sized the circuit in 1391s (20 minutes).The resulting circuit had performance comparable to or better than the performance of the human-designed circuit.

Table 2: Time spent for 160 CF evaluations with 1, 2, and 3 optimization runs in parallel. The equivalent time, effective speedup, and overall CPU usage are also listed. Optimization was stopped after 160 CF evaluations.

		Number of workers (N)					
		1	2	3	4	5	6
1 run	Time [s]	617.0	362.1	275.6	243.2	228.4	223.8
	Effective speedup	1.00	1.70	2.24	2.54	2.70	2.76
	Overall CPU usage	1.00	0.85	0.75	0.64	0.54	0.46
2 runs	Time [s]	-	591.4	427.6	358.5	345.2	350.0
	Equiv. time [s]	-	295.7	213.8	179.2	172.6	175.0
	Effective speedup	-	2.09	2.90	3.44	3.57	3.53
	Overall CPU usage	-	1.04	0.97	0.87	0.71	0.59
3 runs	Time [s]	-	-	587.8	484.8	438.4	464.0
	Equiv. time [s]	-	-	195.9	161.6	146.1	154.7
	Effective speedup	-	-	3.14	3.82	4.22	3.99
	Overall CPU usage	-	-	1.06	0.96	0.84	0.67

Table 4: Comparison of performance constraints (b), penalty coefficients (A), human-designed circuit, and computer-designed circuit worst-corner performance. ↑ stands for maximize and ↓ for minimize.

Analysis	Measurement		b	A	Human	Computer
-	Area	↓	1000μm^2	100μm^2	985μm^2	983μm^2
OP	Supply current at V_{in}=0V	↓	0.5mA	0.1mA	0.49mA	0.48mA
DC	Swing (50% gain drop)	↑	2.0V	0.1V	2.09V	2.02V
	Open-loop gain (-1V..1V)	↑	60dB	1dB	57.2dB	56.1dB
AC	Unity gain bandwidth	↑	100MHz	10MHz	83.5MHz	131.2MHz
	Phase margin	↑	70°	1°	73.9°	75.9°
	Gain margin	↑	12dB	1dB	13.0dB	13.8dB
NOISE	RMS output Integ. noise (1kHz..1GHz)	↓	3mV	0.1mV	3.75mV	2.96mV
	Output spot noise (at 10Hz)	↓	15μV/√Hz	1μV/√Hz	16.7μV/√Hz	11.2μV/√Hz
TRAN	Overshoot	↓	0.1%	0.01%	0.11%	0.086%
	Slewrate	↑	20V/μs	1V/μs	13.3 V/μs	21.4 V/μs
	Settling time	↓	10ns	1ns	11.3ns	7.0ns
	Rise time	↓	10ns	1ns	13.5ns	8.4ns
	Fall time	↓	10ns	1ns	13.6ns	8.5ns

5 Conclusion

The corner-parallel approach to robust circuit sizing has been presented. The mathematical formulation of the cost function used in the process of optimization represents the basis for dividing the work among the workers. Every worker evaluates a piece of the cost function that belongs to a particular corner of the circuit. The optimization algorithm needs the cost function value for choosing the next trial point in the design space. Therefore all partial cost function values must be collected first. Duration of the partial cost function evaluation varies significantly since circuit simulation is an iterative procedure. Some workers finish sooner than the others. If the master has no more partial cost function terms for handing over to the workers, these workers remain idle until all partial cost function values are collected by the master. At that point the optimization algorithm running on the master chooses a new point in the design space and provides the workers with new partial CF terms for evaluation.

The consequence of worker idle time is the reduced speedup. For a circuit with M_S corners optimized using M_S workers the speedup should be near M_S. Unfortunately the large variations in partial cost function evaluation time greatly reduce this number. The designer often wants to explore various design tradeoffs resulting from different parallel optimization runs. These optimization runs can be executed concurrently. The experiments show that running 2 or 3 concurrent parallel optimization runs greatly improves CPU usage. This is due to the fact that with the increasing number of optimization processes running on a single worker the probability that all of them will be idle at the same time decreases.

Taking into account Moore's law (CPU power doubles every 18 months) one can expect that in the following 5 years sizing circuits (like the one in fig. 2) will become a matter of minutes, making automated circuit sizing a standard tool for every IC designer. Considering the fact that sizing such a circuit manually can be a matter of days even for experienced designers, manual circuit sizing will become economically unfeasible for many standard circuits (like opamps, linear regulators, etc.). This of course doesn't mean that virtually anyone will be able to do IC design. Setting up an optimization run requires specific designer knowledge in the process of choosing the circuit structure, performance constraints, and element matching. Sensible explicit constraint values on optimization parameters reduce mismatch, but on the other hand increase the minimum achievable circuit area. Choosing these tradeoffs still requires extensive design experience.

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ON COST FUNCTION PROPERTIES IN ANALOG CIRCUIT OPTIMIZATION

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Key words: computer aided design, analog circuits, optimization algorithms, cost function, parameter space

Abstract: Analog circuit design is a very complex and time consuming process. The largest percentage of the time is spent trying to achieve the best performance by varying the circuit parameters. This is actually an optimization process and there is a growing desire to automate at least a part of the optimization procedure. Unfortunately the optimization algorithms are still very slow. This is mostly due to the sheer number of circuit analyses it takes for the optimization algorithm to converge to a minimum. Obviously any previous knowledge about the shape of the cost function could help the optimization algorithm to converge faster. Unfortunately (again) the shape of the cost function is generally too unpredictable to draw any conclusions prior to the optimization run. This paper tries to show that with a special formulation of the cost function the shape of the cost function itself can be at least partially predicted.

Vpogled v značilnosti kriterijskih funkcij optimizacijskih algoritmov

Kjučne besede: računalniško podprto načrtovanje, analogna vezja, optimizacijski algoritmi, kriterijska funkcija, parameterski prostor

Izvleček: Načrtovanje analognih vezij je zelo zapleten postopek, najtežji del katerega pa je zagotovo določanje optimalnih vrednosti parametrov vezja. Pri tem gre v bistvu za optimizacijski postopek, kjer načrtovalec s spreminjanjem vrednosti parametrov skuša doseči čim boljše delovanje vezja. Zaradi zahtevnosti postopka se pojavlja vse večja želja po določeni avtomatizaciji, to je uporabi optimizacijskih algoritmov za določanje teh parametrov. Žal so optimizacijski algoritmi zelo zamudni, to pa zaradi velikega števila analiz, ki jih morajo opraviti. Vsaka vnaprejšnja informacija o lastnostih kriterijske funkcije je zato zelo dobrodošla saj lahko skrajša čas optimizacije. V splošnem velja, da je oblika kriterijske funkcije nepredvidljiva. Ta članek skuša nakazati, da je v določenih primerih mogoče obliko kriterijske funkcije do določene mere vnaprej predvideti.

1. Introduction

Analog circuit design is a very complicated job. An engineer performing it must be highly skilled and must posses an intimate knowledge of circuit topologies. In addition he must have a fairly high amount of patience. The problem lies in the fact that analog circuit design is a trial and error process. As the complexity of analog circuits grows it becomes practically impossible to compute the circuit parameters analytically. The designer has to vary the circuit parameters and simulate the circuit in hope of finding the optimal set of values. As this is actually an optimization problem there is a growing desire to employ optimization algorithms to automate at least part of the task /5-9/.

The main reason for computer circuit optimization not to be widely used in circuit design is the computational intensity of optimization algorithms. Although the raw computing power of modern computers is steadily increasing the length of optimization runs is still measured in days. The sheer number of circuit analyses the algorithms require and the size of the parameter space are the main reasons for the slow convergence rate. It is understandable that there is a strong interest in the designer community for such tools and much effort has been (and still is) poured into the investigation of various optimization algorithms. The focus of this research is the minimization of the required number of circuit analyses to perform an optimization run. It is interesting to note that all the research has been focused on the optimization algorithms alone and that the formulation of the cost function has been left untouched.

At first glance this would seem reasonable enough as common sense indicates that the behavior of the optimized circuit should vary unpredictably across the parameter space investigated by the optimization algorithm. While this is usually true there are certain cases where the behavior of the cost function in the parameter space can be at least partially predicted and taken into account by the optimization algorithm.

This paper tries to shed some light on the properties of a analog circuit cost functions.

The paper is partitioned as follows. First the cost function formulation is explained. A mathematical analysis of the resulting cost function follows. The analytical results are then substantiated by the numerical results of optimization runs on real world circuits. Finally the conclusions are summed up and some suggestions for future work are given.

2. The cost function formulation

The behavior of a circuit can be described with a number of measurements. More detailed the description must be, more measurements it takes. This is also true for optimization algorithms. The cost function is usually defined as a

function of a set of measurements, which are in turn the results of circuit simulations. In most cases this is an ordinary linear combination of suitably weighted measurement values.

$$cost(x) = \sum_i a_i * measurement_i(x) \quad (1)$$

Although some research has been done into cost function formulation it was mainly centered around the robustness of the resulting optimized circuit /1-4/ while little thought has been spent on the possible implications for the optimization algorithm. Even if this work /1,2/ is not directly connected to the investigated problem it can nevertheless form a solid base for the analysis of the cost function behavior. Before proceeding further with the task it would be best to examine the proposed cost function formulation.

As mentioned earlier the cost function is usually a linear combination of suitably weighted measurement values. The investigated cost function formulation takes a different approach. Instead of combining the measurement values directly a set of criterion functions is built. These criterion functions are actually nonlinear transformations that translate measurement values into cost values. These cost values are then summed up and form the cost function itself. The criterion functions are defined in expression (2).

$$cost(x) = \begin{cases} -k_t(x_G - x) & : x \le x_G \\ k_p(x - x_G) & : x \ge x_G \end{cases} \quad (2)$$

The situation is shown in figure 1.

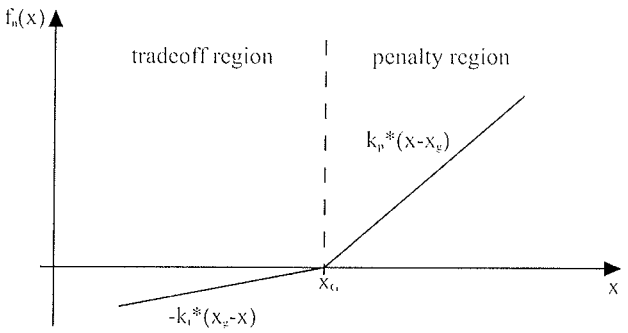

Figure 1: A graphical representation of a criterion function

Geometrically the criterion function is the combination of two ramps. The criterion function has two regions, one is the tradeoff region and the other is the penalty region. A measurement value in the penalty region means a working circuit with lower than specified characteristics that is penalized with a positive cost value. A measurement in the tradeoff region belongs to a circuit that meets the design specification and so it is awarded with a negative cost value.

Another important concept in robust circuit design that needs underlining is corners. A corner is simply put a set of circuit operating parameters. These can be environmental parameters (temperature, humidity), process parameters (process and element tolerances) and operating conditions (supply voltage).

Optimization results /1,2/ have already shown that this cost function formulation yields robust circuit designs. Now it must be seen whether there is anything that can be done analytically.

3. Mathematical analysis

The problem that will be investigated is the behavior of the cost function when the number of criterion functions increases. To tackle this problem it must be simplified first.

There is a number of assumption to be made to make the analytical approach manageable. First only a bounded region of the measurement space will be observed. Second the criterion functions will be evenly spaced across the observed interval of the measurement space. The slopes of all criterion functions will be equal. Fourth the tradeoff coefficients will be all 0.

Even if this set of assumptions seems very restrictive there will still be a number of useful conclusions to be drawn from the results. The described configuration is depicted in figure 2.

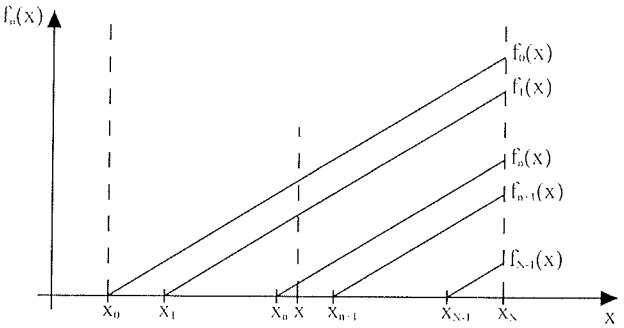

Figure 2: The investigated scenario

The notation is as follows: x_0 and x_N are the limits of the observed region, N is the number of ramps, x_n are ramp starting points and x is an arbitrary point in the observed region. The ramps are defined in equation (3).

$$f_n(x) = \begin{cases} k(x - x_n) & : x \ge x_n \\ 0 & : otherwise \end{cases} \quad (3)$$

The difference between two consecutive x_n is d. An arbitrary point x is then defined in equation (4).

$$x = x_0 + t(x_N - x_0) = x_0 + tNd \quad (4)$$

and the ramp starting points is expressed in equation (5).

$$x_n = x_0 + nd = x_0 + \lfloor tN \rfloor d \quad (5)$$

The cost function is then the sum of all ramp functions in the observed interval of the measurement space.

$$F_N(x) = \frac{1}{N} * \sum_{n=0}^{N} f_n(x) \tag{6}$$

Expression (6) is still general but after the substitution of $f_n(x)$ with the ramp function definition (expression (3)) the cost function expression (7) is obtained.

$$\begin{aligned} F_N(x) &= \frac{1}{N} * \sum_{n=0}^{\lfloor tN \rfloor} k(x - (x_0 + nd)) = \\ &= \frac{k}{N} \sum_{n=0}^{\lfloor tN \rfloor} (x - x_0) - \frac{kd}{N} \sum_{n=0}^{\lfloor tN \rfloor} n = \\ &= \frac{\lfloor tN \rfloor + 1}{N} k(x - x_0) - \\ &\quad \frac{kd}{N} \frac{\lfloor tN \rfloor (\lfloor tN \rfloor + 1)}{2} \end{aligned} \tag{7}$$

This expression can be improved with the introduction of a new variable ε.

$$\lfloor tN \rfloor = (t - \epsilon)N = tN - \epsilon N$$

$$\epsilon = \frac{tN - \lfloor tN \rfloor}{N} \leq \frac{1}{N} \tag{8}$$

The floor (⌊tN⌋) notation in expression (7) can now be substituted with expression (8) to get the equation (9).

$$\begin{aligned} F_N(x) &= \frac{(t - \epsilon)N + 1}{N} k(x - x_0) - \\ &\quad - \frac{k\frac{x_N - x_0}{N}}{N} \frac{(t - \epsilon)N((t - \epsilon)N + 1)}{2} = \\ &= ((t - \epsilon) + \frac{1}{N}) k(x - x_0) - \\ &\quad - k(x_N - x_0) \frac{(t - \epsilon)^2}{2} - \frac{(x_N - x_0)(t - \epsilon)}{2N} k \end{aligned} \tag{9}$$

Apart from the simplification of equation (7) expression (8) presents an upper bound for ε, which will be useful later.

In expression (9) the cost function is dependent on the number of criterion ramp functions N. Since the number of criterion functions is the product of the number of measurements and corners it tends to get very large. It will prove useful to compute the limit of the cost function with N approaching infinity. The result is expression (10).

$$\lim_{N \to \infty} F_N(x) = k(x - x_0)t - \frac{k}{2}(x_N - x_0)t^2 \tag{10}$$

Notice that both x and t are present in expression (10). Since they are both rigidly tied by expression (4) equation (10) can be expressed with just one of them. The variable t can be expressed from equation (4).

$$t = \frac{x - x_0}{x_N - x_0} \tag{11}$$

The resulting expression (11) can then be substituted in equation (10).

$$\begin{aligned} \lim_{N \to \infty} F_N(x) &= k\frac{(x - x_0)^2}{x_N - x_0} - \frac{k}{2}\frac{(x - x_0)^2}{x_N - x_0} = \\ &= \frac{k}{2(x_N - x_0)}(x - x_0)^2 = a * (x - x_0)^2 \end{aligned} \tag{12}$$

The resulting expression (12) is obviously a quadratic function of variable x. The conclusion that can be drawn is that the larger is the number of criterion functions the more the cost function resembles half a quadratic parabola.

The obtained result applies directly only to the minimization of measurement values. It would be straightforward to show that the same result follows from the analysis of a measurement maximization criterion function.

Notwithstanding the interesting results it must be born in mind that the analysis was done in measurement space. The relationships between circuit parameters and measurement values are highly nonlinear. Further the assumptions that were made are generally not fulfilled. It must therefore be expected that the shape of the cost function in the parameter space will not be an ideal quadratic parabola. All that needs to be done is to check whether the analytical results resemble in any way real optimization data obtained on a real world test circuit.

4. The test circuit

The test circuit is the core segment of a real world operational amplifier. The heart of the amplifier is a differential telescopic amplifier stage. The stage consists of transistors m06-m15. There is also a simplified bias circuitry (m01-m05) where a complex compensation circuit is substituted by two current sources (i01 and i02) and a common mode feedback circuit (m17-m20). The bias circuit has also a temperature compensation made of the transistors m04 and m05 and the resistor r01. The schematic diagram of the operational amplifier is shown in figure 3. Figure 4 shows the test application of the operational amplifier.

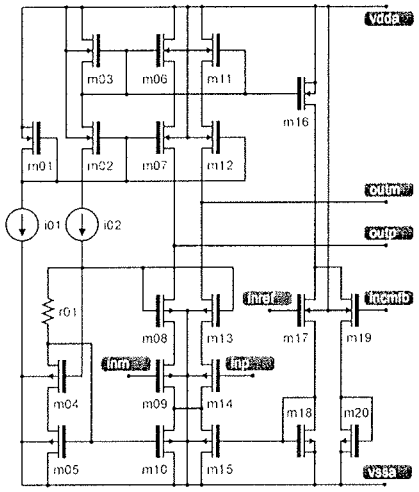

Figure 3: The schematic diagram of the simplified operational amplifier

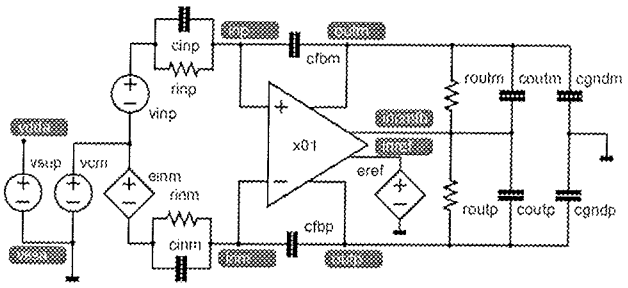

Figure 4: Operational amplifier test application

The test-bench circuit simulates the working condition of the operational amplifier. The element values are: rinp and rinm are both 1mΩ, routp and routm are both 1GΩ, cinp, cinm, cfbp and cfbm are all 500fF, routp and routm are both 150fF and cgndp and cgndm are both 2.3pF.

There are 18 matching groups of optimization parameters in the circuit. These are:

1) the lengths of transistors m03, m06, m11 and m16
2) the lengths of transistors m02, m07 and m12
3) the lengths of transistors m18 and m20
4) the lengths of transistors m08 and m13
5) the lengths of transistors m09 and m14
6) the lengths of transistors m05, m10 and m15
7) the lengths of transistors m17 and m19
8) the length of transistor m01
9) the length of transistor m04
10) the widths of transistors mm02, m03, m06, m07, m11, m12 and m16
11) the widths of transistors m18 and m20
12) the widths of transistors m08 and m13
13) the widths of transistors m09 and m14
14) the widths of transistors m05, m10 and m15
15) the widths of transistors m17 and m19
16) the width of transistor m01
17) the width of transistor m04
18) the multiplication factors of transistors m10 and m15

From the matching groups it is evident that channel widths and lengths of all transistors are optimized in addition to the multiplication factors of transistor m10 and m15.

There are also 9 corners involved in the circuit evaluation.

There are 11 design goals the optimization algorithm must fulfill. These are:

- Maximum current consumption 0.48mA
- Maximum common mode feed-back offset 180mV
- Minimum output swing 2.6V
- Minimum open loop gain 61dB
- Minimum unity gain frequency 90MHz
- Minimum phase margin 75°
- Minimum gain margin 13dB
- Maximum overshoot 0.3%
- Maximum settling time 11ns
- Minimum slew rate 13MV/s

Each design goal is checked with a suitable measurement. Combined with the number of corners this means the cost function consists of 99 criterion functions. All trade-off weights are set to 0 and all penalty weights are set to 1.

Now the optimization problem has been introduced it is time to see the results.

For the sake of clarity only 5 matching group cost profiles out of the 18 will be shown. There are the matching groups 8, 12, 13, 16 and 18.

Figures 5-9 show the cost profiles of the cost function for the chosen axes of the parameter space. On each figure there are the profiles of the nine separate corners (thin lines) together with the complete cost function (bold line).

As expected the cost function profiles are not exactly quadratic parabolas. Nevertheless it is still notable that they are quite smooth and near the optimal parameter values they are remarkably quadratic-like, specially in the neighborhood of the cost function minimum. This seems to imply that the relationship between the cost function in the measurement space and the cost function in the parameter space becomes linear in the vicinity of the cost function minimum but additional research would be needed to shed more light on the subject.

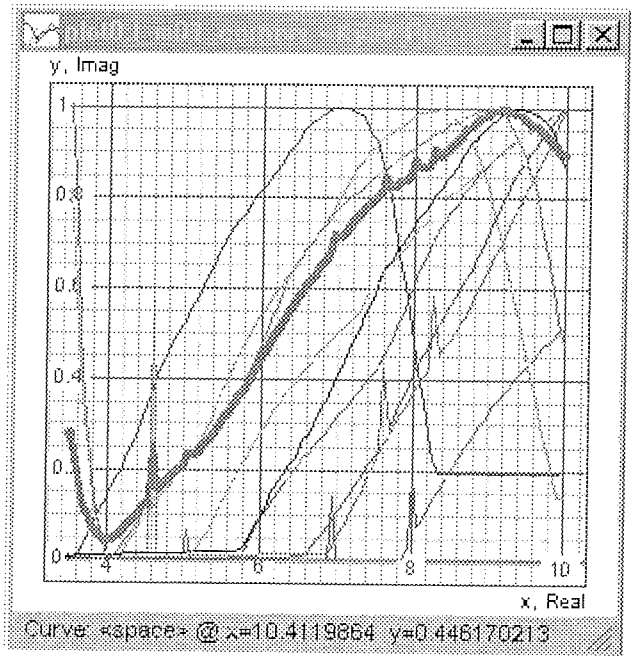

Figure 5: The cost profiles as functions of the matching group 8.

The profiles in figures 5,6 and 7 are reasonably close the predictions. There is only the question about the spikes

that are present on the otherwise smooth curves. Before delving into those it is noteworthy to have a look at figure 8. In this figure the profiles are full of spikes. A careful analysis of the measurement values near the spikes revealed that the spikes are caused by numerical noise that should have been foreseen.

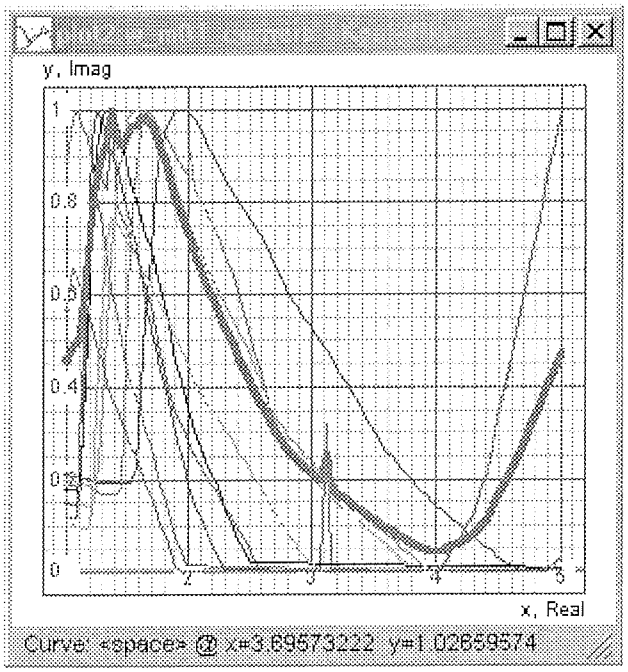

Figure 6: The cost profiles as functions of the matching group 16.

The main reason for the spikes is the far too tight overshoot design goal. With such a pressing goal it is normal that the circuit will hover just below the required performance. In such a situation any numerical error in the measurement computations can result in a worse than required performance causing the observed spikes. In figures 5, 6 and 7 the measurements were well clear of the goal threshold so there is a limited number of spikes. In the case of figure 8 on the other hand the circuit hovers right on the goal threshold with the result that the cost profile is extremely noisy. When the spikes are taken into account it can be seen that even the cost profile in figure 8 is reasonably like the profiles in figures 5, 6 and 7.

The remaining cost profile in figure 9 differs from the others in one point. It is not smooth. On this figure the cost profile is the function of the multiplication factor of transistors m10 and m15. Since the multiplication factor is an integer value the steps in the cost profile are expected. Non-smooth cost functions are still a major problem for optimization algorithms /10-13/ so it is remarkable that the optimization algorithm /8,9/ successfully converged to the minimum with little trouble.

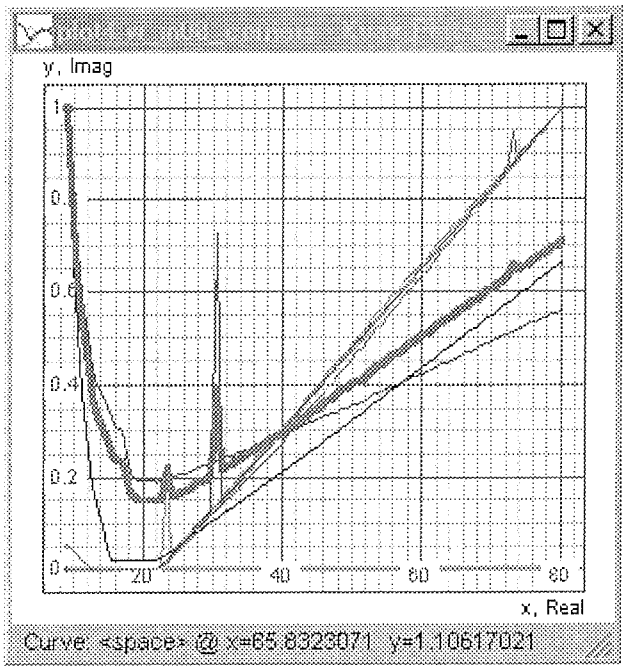

Figure 7: The cost profiles as functions of the matching group12.

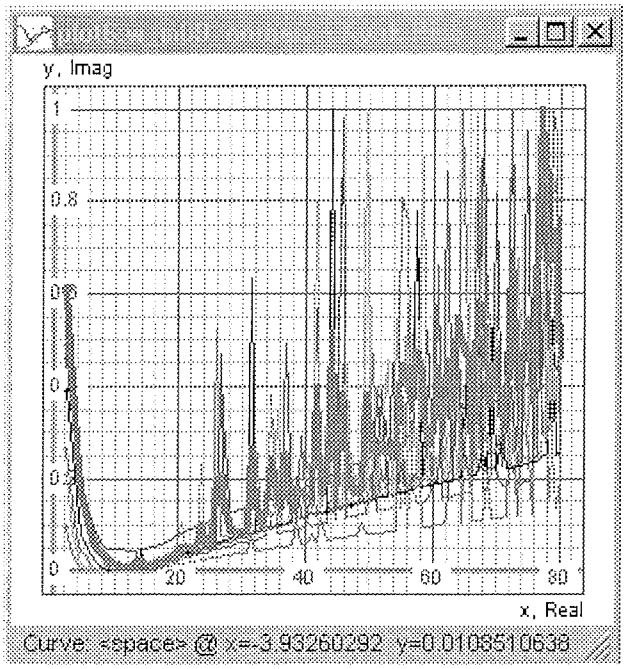

Figure 8: The cost profiles as functions of the matching group 13.

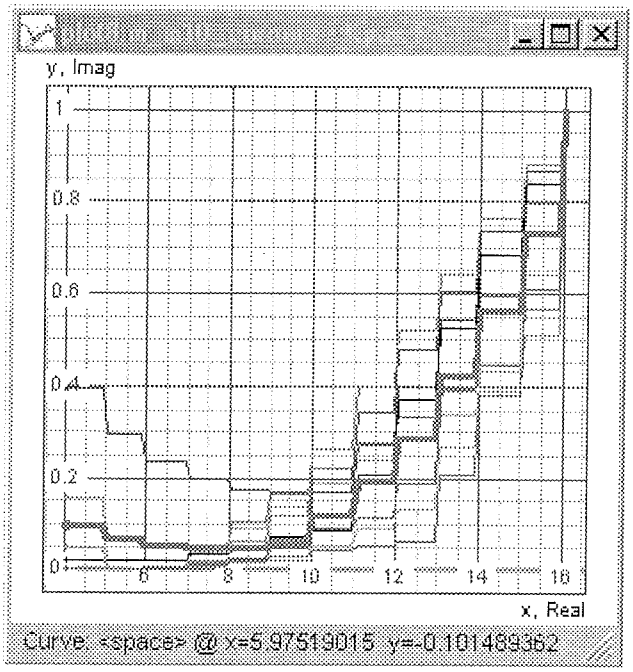

Figure 9: The cost profiles as functions of the matching group 18.

5. Conclusions

The evidence presented in this paper leads to several conclusions.

First, the cost function in the measurement space is shown analytically to limit to a quadratic parabola. This is due to the formulation of the cost function /1,2/ and the presence of a large number of corners and measurements needed for a robust circuit design /1-4/. Even if the relationship between measurement space and parameter space cost functions is highly nonlinear this result can still prove highly useful.

Second, the cost function of a real-world integrated operational amplifier was studied. The cost function profiles showed a general smoothness while in the vicinity of the minimum the cost function profile displayed a near quadratic shape. This seems to imply that the relationship between measurement space cost functions and parameter space cost functions tends to become linear in the vicinity of the minimum. If proved true this would be in itself a most remarkable result but at this stage it is still too early to draw a definite conclusion. Additional research is needed to shed more light into this subject.

Third, the quadratic shape of the cost function in the vicinity of the minimum suggests the development of an optimization algorithm that could exploit such cost function properties. The fact that the quadratic shape is present only in the vicinity of the minimum a multi-stage optimization algorithm is needed. Multi-stage optimization algorithms have been investigated in the past /14-18/ but unfortunately the research was centered on the algorithms themselve without delving into the properties of the underlying cost functions. It would be expected that the exploitation of the quadratic near-minimum cost function shape could help the convergence of optimization algorithms. To build such a multi-stage optimization algorithm suitable basic optimization algorithms would have to be chosen first, then an adequate algorithm for dynamically switching to the appropriate optimization method based on the cost function properties would have to be developed.

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SPAJKANJE ELEKTRONSKIH VEZIJ S SPAJKAMI BREZ SVINCA

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Kjučne besede: spajke brez svinca, tiskana vezja, spajkanje brez svinca

Izvleček: Opisali smo osnovne korake za uvajanje novega proizvodnega postopka spajkanja brez svinca elektronskih vezij. V laboratoriju za razvoj tiskanih in hibridnih vezij smo izmerili osnovne lastnosti spajkalnih past brez svinca. Primerjali smo in analizirali eksperimentalne rezultate testa omočljivosti in tvorbe spajkalnih kroglic spajkalnih past brez svinca , ki so bili narejeni v dveh laboratorijih.

Soldering Electronic Circuits Using Lead-free Solder Pastes

Key words: lead-free solder pastes, printed circuits, hybrid circuits, lead-free soldering

Abstract: Electronics manufacturers worldwide are converting to a lead-free soldering process for a variety of reasons, including environmental concerns and compliance with impending legislation. Due to European legislation known as WEEE (the directive on Waste of Electrical and Electronic Equipment) and RoHS (the directive on Restriction of the use of certain Hazardous Substances) the electronics industry must ban the use of hazardous substances by the 1st of July 2006.

The successful implementation of lead-free soldering in a printed-circuits production line requires careful planning and rigorous process monitoring to ensure quality and process control. In order to introduce lead-free soldering in a printed circuits production line, a five-step soldering program was developed. The program begins with selecting the right materials and equipment, after this it is necessary to define the process and develop a robust process, followed by the implementation of the lead-free manufacturing. The last step of the program is control and improvement of the new process.

New materials should be tested in particular ways for hybrids and PCBs with lead-free coatings application. These lead-free solder pastes are not appropriate for hybrid circuits and for PCB applications, because todays technology is based on different materials for soldering (tin-lead solders) and different materials for solder pads. Therefore special lead-free pastes used for soldering hybrid circuits as well as PCBs with lead-free preservative coatings must be developed. The new lead-free solder pastes have a higher melting point than eutectic tin-lead alloys. This has an inf1uence on the wettability of conductor lines in circuits and the technological window of soldering. The basic properties of the selected lead-free pastes such as viscosity, tackiness, solder ball, wettability, and printability were investigated. The optimum parameters for the soldering will be established, and later the soldering surface insulation resistance (SIR) and the electromigration in humid conditions will be tested on hybrid and printed circuits.

The components are the weakest point in the lead-free soldering chain. More often than not, they are only available with SnPb terminations The reliability of the components at high temperatures is another problem. Reliability tests in several projects indicate that some standard components can also be soldered at slightly higher temperatures. However for some components it will be necessary to modify the currently used plastic material accordingly.

The use of standard material in printed circuit board (PCB) production must also be changed. Alternative PCB materials will include materials such as glass/epoxy or glass/polyimide.

The results of European projects and industrial research on new soldering materials support the use of SnAgCu solder for lead-free reflow processes and SnCu for wave soldering.

In this paper we have reported the results of testing a new Pb-free solder paste for the soldering of electronic in a hybrid and printed circuits production line. The principal characteristics of the SnAgCu and SnAg lead-free solder pastes were tested in two research laboratories. The results of solder-paste wetting and solder-ball occurrence after the reflow soldering process were compared and discussed.

The test samples for electronic component soldering with selected solder pastes were developed on ceramic substrates and on printed circuits. Electronic components with lead-free terminations will be soldered and the reliability tests of soldered joints between components and conductor pads on the circuit will be tested.

1. Uvod

Svinec je znan kot tvegan element za človeško zdravje in že majhne količine povzročajo okvare živčnega sistema in možganov. Če se ostanki svinca nahajajo v naravi, lahko onesnažijo tekočo vodo in z njo pridejo v človeški organizem.

Svinec se že desetletja uporablja kot sestavina v spajkah za spajkanje elektronskih komponent v elektronskih vezjih. Delež svetovne porabe svinca v elektronski industriji je relativno majhen, glede na to, da elektronska industrija predstavlja 1-2% svetovne industrije, vendar je odpad električnih in elektronskih naprav razpršen in težko nadzorovan. Zakonodaja EU je pripravila direktivo WEEE (Waste from Electrical and Electronic Equipment - elektronski odpad) in

Tabela 1. Plan vpeljave spajkanja brez svinca v Evropi

		1999	2000	2001	2002	2003	2004	2005	2006	2007	2008
Material	vsi produkti										
Komponente	prvi produkti										
	pol-produkti										
	vsi produkti										
Montaža	prvi produkti										
	pol-produkti										
	vsi produkti										

RoHS (Restriction of Hazardous Material - prepoved uporabe nevarnih snovi), ki določa skrajni datum za prenehanje uporabe spajke na osnovi svinca. Februarja 2003 je bilo na European Lead-Free Soldering Technology sprejeto, da produkti namenjeni za Evropo, po 1.7.2006 ne bodo smeli vsebovati svinca. Za produkte brez svinca se smatrajo vsi tisti produkti, pri katerih vsebnost svinca ne preseže vrednosti 0,1 odstotka na težo modela.

V elektroniki se svinec uporablja za spajkanje elektronskih komponent. Spajkanje je spajanje dveh kovinskih površin z zlitino Sn-Pb, ki mora stični površini v čimkrajšem času zaliti tako, da je dosežena zadovoljiva mehanska trdnost in dober električni kontakt. Prednost uporabe svinca v spajki SnPb je nizka temperatura tališča (183°C) in s tem delovna temperatura (250°C za valno spajkanje in 200 - 230°C za pretaljevalno spajkanje), nizka cena svinca in dosegljivost na tržišču, stabilnost zlitine SnPb ter dobre mehanske lastnosti.

Glavni razlogi za prenehanje uporabe svinca v elektronski industriji so: zakonodaja, zdravju in okolju prijazna tehnologija, enostavnejša reciklaža odpadkov, prednost na tržišču in zahteve kupca po ekološko prijaznih izdelkih.

Nova tehnologija spajkanja mora ostati v skladu s standardi in ne sme bistveno ožiti tehnološke zmožnosti ter zmanjševati stopnje zanesljivosti delovanja elektronskih vezij.

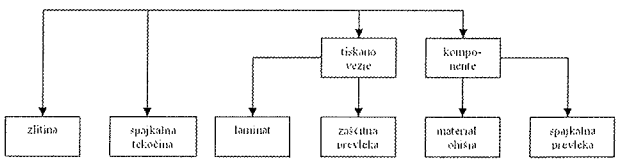
2. Vpeljava tehnologije spajkanja brez svinca

Za uspešno vpeljavo spajkanja s spajkami brez svinca je potrebno slediti naslednjim petim korakov. Prvi in hkrati najpomembnejši korak je izbira materialov in opreme za proizvodnjo. Ko je le-to določeno, je potrebno definirati procese, preveriti robustnost procesov in vpeljati proces spajkanja brez svinca v proizvodnjo. Vpeljan proces je potrebno skrbno kontrolirati, spremljati kvaliteto spajkanja in stalno izboljševati.

Spajke so običajno zlitine različnih kovin, najpogosteje pa vsebujejo kositer in svinec (npr. Sn60/Pb40). Za novo tehnologijo spajkanja brez svinca se uporabljajo različne zlitine, ki imajo praviloma višjo temperaturo tališča. Višja temperatura spajkanja in drugačna kemična sestava spajk pa pogojujeta:

- uporabo elektronskih komponent, ki prenesejo višje temperature
- uporabo materialov za tiskanine, ki prenesejo višje temperature
- primerno obdelavo površin spajkalnih blazinic na tiskaninah
- uporabo primernih prevodnih materialov pri hibridnih vezij
- uporabo primernih spajkalnih tekočin
- uporabo primernih čistil
- prireditev obstoječe procesne opreme ali izbira nove
- uvedba novih kriterijev za vizuelno kontrolo kvalitete spojev

Pri izbiri materialov je glavni poudarek na ploščah tiskanega vezja in komponentah. Za tiskana vezja je potrebno izbrati ustrezen laminat in zaščitno prevleko brez svinca. Komponente zahtevajo bolj vzdržljiv material za ohišja in ravno tako spajkalno prevleko brez svinca. Za pretaljevalno in valno spajkanje pa se izbere ustrezna zlitina za spajkalno pasto in spajko ter spajkalno tekočino.



Slika 1: Izbira materialov

2.1. Izbira materialov

2.1.1. Izbira zlitine

Izkušnje kažejo, da se bo kot alternativa za SnPb uporabljala SnAgCu (za pretaljevalno spajkanje) in SnAgCu oziroma SnCu (za valno spajkanje). Izbira zlitine je odvisna od:

- termično mehanske lastnosti zlitine in temperatura tališča
- testa omočljivosti

- raziskav
- dosegljivosti in cene
- izkušenj podjetja s tehnologijo brez svinca

Tabela 2: Izbira zlitine

Izbira zlitine			
temperatura		aplikacija	opombe
zlitine z visokimi tališči (250-300°C)			
227	SnCu	nizki stroški, valno spajkanje	temperatura
221	SnAg	ustrezno območje, odlične termične lastnosti, zanesljivejši spoji	strupeno srebro
217	SnAgCu	valno in pretaljevalno spajkanje, višja razteznost, pogosto uporabljena zlitina	strupeno srebro
217	SnAgCuSb	Sb poveča zanesljivost pri valnem spajkanju	strupeno srebro, antimon, štiri-komponentna zlitina
srednje območje (180 -205°C)			
200-216	SnAgBi	SMT aplikacije, valno in pretaljevalno spajkanje, Bi znižuje tališče	strupeno srebro
199	SnZn	nizke temperature	oksidacija cinka, zahteva aktivnejšo spajkalno tekočino, slaba omočljivost
zlitine z nizkimi tališči (180-205°C)			
138	SnBi	zaradi nizke temperature primeren za občutljive komponente, pretaljevalno in valno spajkanje	Bi je stranski produkt v rudnikih Pb, prenizko tališče pri posameznih aplikacijah

2.1.2. Izbira spajkalne tekočine

Spajkalna tekočina je sestavni del spajkalne paste in predstavlja ~ 10 odstotni delež. Vpliva na viskoznost same spajkalne paste.

Spajkalna tekočina se uporablja tudi pri valnem spajkanju. Njena naloga je, da najprej očisti površino in jo hkrati aktivira, ostanki po spajkanju pa ne smejo povzročati korozije.

Iz okolje varstvenega izhodišča spajkalna tekočina ne sme vsebovati hlapnih ogljikovodikov (zaradi zmanjševanja VOC emisije) in halogenov.

2.1.3. Izbira tiskanega vezja

Material za plošče tiskanega vezja (laminat) mora zdržati višje temperature spajkanja, ne da bi pri tem bistveno spremenil lastnosti oziroma se skrivil in ne sme vsebovati halogenov. Najpogosteje uporabljene prevleke na prevodnih likih tiskanega vezja so zbrane v Tabeli 3.

Tabela 3: Izbira prevleke za prevodne like tiskanega vezja

Izbira zaščite priključkov komponent		
prevleka	aplikacija	opombe
NiPd	SMT komponente: IC	materialni stroški, razpoke, spajkljivost
NiPdAu	alternativa Ni Pd, rahlo izboljšano omočenje	materialni stroški
SnBi	SMT komponente: I C - klasične komponente: IC, diode, tranzistorji	združljiv z Sn/Pb spajko
Sn	klasične komponente: CCD	"whiskering" Sn, visoka temperatura tališča
SnAg (potopno)	SMT komponente: diode - klasične komponente: IC, tranzistorji, diode	možnost galvaniziranja š e ni zagotovljena
SnCu	klasične komponente: diode	"whiskering" Sn, majhna vsebnost Cu, potrebna redna kontrola Cu kot nečistoče

2.1.4. Izbira komponent

Pri izbiri komponent moramo upoštevati naslednje zahteve:

- komponenta ne sme vsebovati svinca in halogenov
- nove plastike za ohišja morajo biti obstojne na višje temperature

Proizvajalci komponent najpogosteje uporabljajo za priključne površine spajkalne prevleke, ki so zbrane v Tabeli 4.

Tabela 4: Izbira zaščite priključkov komponent

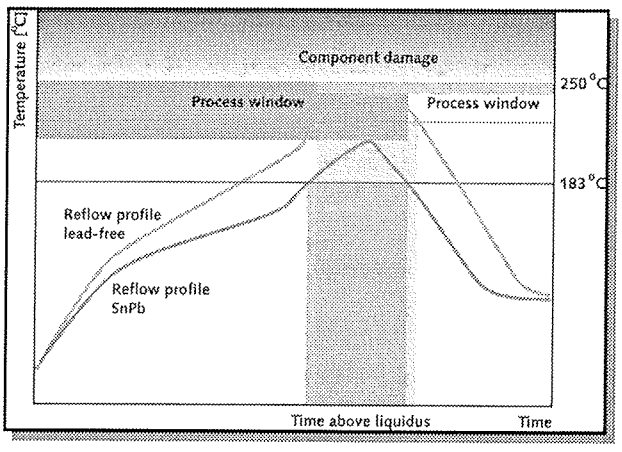
Izbira prevleke za prevodne like tiskanega vezja			
	opis	opomba	opombe
OSP	organska zaščita	nizka cena, dobra spajkljivost	čas skladiščenja, visoke temperature, večkratno spajkanje
Kem. NiAu	nikelj, zlato	primerno za višje temperature, večkratno spajkanje, za visoko zahtevne produkte	visoka cena
Kem. Sn	potapljanje v čistem kositru	večkratno spajkanje, stabilen proces	različni rezultati
Kem. Ag	potapljanje v srebru	dobra zapolnitev izvrtin, stabilen proces	tanek nanos
HASL (brez Pb)	nanos z vročim zrakom - brez Pb	dobro omočenje	krivljenje TIV zaradi visokih temperatur

2.2. Strojna oprema

Pri prehodu na spajkanje brez svinca se bistveno spremeni oprema, namenjena pretaljevalnemu in valnemu spajkanju.

2.2.1. Pretaljevalno spajkanje

S spajkanjem brez svinca se približamo maksimalni dovoljeni temperaturi 250°C. To je območje, ki še ne povzroča poškodb komponent in krivljenja plošč tiskanega vezja. S tem se zmanjša tudi samo procesno okno, kar je razvidno na Sliki 2.



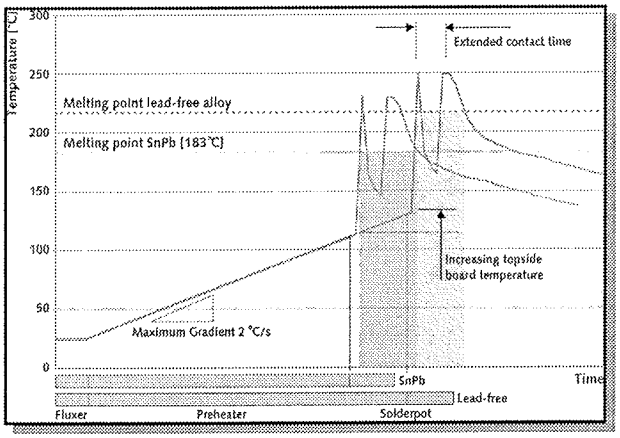
Slika 2: Temperaturni profil za pretaljevalno spajkanje

Višje temperature bodo povečale možnost krivljenja plošč, kar lahko preprečimo z ustrezno podporo v peči med samim spajkanjem. Uporaba dušika med spajkanjem je priporočljiva pri uporabi organske zaščite površin na tiskanih vezij. Dušik izboljša omočljivost, vendar so pri pretaljevalnem spajkanju opazili tudi pojav večjega števila drugih napak spajkanja (dvignjena komponenta - tombstoning).

2.2.2. Valno spajkanje

Bistvena razlika med SnPb spajkanjem in spajkanjem brez svinca je v višjih temperaturah tališča zlitin brez svinca. Lete zahtevajo ustrezno višje temperature predgretja zaradi morebitnih temperaturnih šokov na prvem valu in uporabo spajkalnih tekočin na vodni osnovi, ki ustrezajo tem zahtevam in so hkrati okolju prijazne.

Za nanos spajkalne tekočine na plošče tiskanega vezja je priporočljiva uporaba razpršilne naprave, ki spajkalno tekočino zelo drobno razprši, saj mora vsa voda odhlapeti, preden pride plošča na prvi val. Temperatura plošče na zgornji strani bo narasla na 130°C v zadnji coni predgretja. Uporaba spajk brez svinca bo zahtevala višje temperature kopeli odvisno od vrste zlitine (za SnCu 270°C in za SnAgCu 260°C). Priporočljiva je tudi uporaba dušika in s tem spajkanjem v inertni atmosferi. Prednost uporabe dušika je v boljši omočljivosti spojev, manjšemu nastajanju oksida, slabost pa cena dušika.



Slika 3: Temperaturni profil za valno spajkanje

2.3. Vizuelni izgled spojev brez svinca

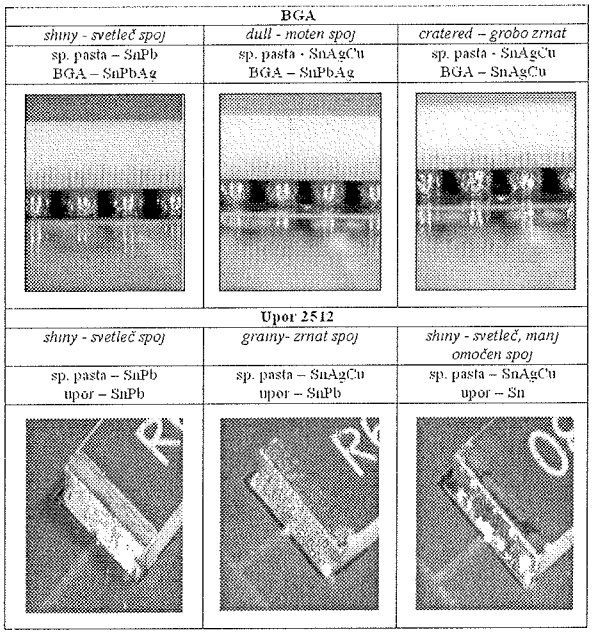
Spajkalni spoji, ki so zaspajkani s spajko SnPb, se že vizuelno ločijo od spojev, ki so zaspajkani s spajko brez Pb. Na Sliki 4 so prikazani primeri spajkanja BGA ob uporabi:

1. spajkalna pasta - SnPb, BGA - SnPbAg
2. spajkalna pasta - SnAgCu, BGA - SnPbAg
3. spajkalna pasta - SnAgCu, BGA - SnAgCu in primeri spajkanja upora 2512 ob uporabi:

1. spajkalna pasta - SnPb, upor - SnPb
2. spajkalna pasta - SnAgCu, upor - SnPb
3. spajkalna pasta - SnAgCu, upor - Sn

3. Eksperimentalno delo in rezultati

V primerjalnih laboratorijih Iskratel Electronics-a in Inštituta Jožef Stefan smo preizkusili in testirali spajkalne paste različnih proizvajalcev in sestav (Tabela 5) ter jih primerjali med seboj.



Slika 4: Vizuelni izgled spojev

Tabela 5: Spajkalne paste

Spajkalne paste brez Pb	
X 13018	Sn95,5Ag4,0Cu0,5
OM 310	Sn95,5Ag4,0Cu0,5
F 610	Sn95,5Ag4,0Cu0,5
NX 9900	Sn96,5Ag3,0Cu0,5
R 910	Sn95,5Ag3,8Cu0,7
R 910	Sn96,5Ag3,5
Referenčna spajkalna pasta	
R 244	Sn62Pb36Ag2

Po standardu IPC-TM650 smo naredili sledeče analize in testiranja:

- test omočljivosti (Metoda 2.4.45)
- test tvorbe spajkalnih kroglic (Metoda 2.4.43)
- merjenje površinske izolacijske upornosti - SIR (Metoda 2.6.3.3)
- razlezenje (Metoda 2.4.35)
- merjenje viskoznosti (Metoda 2.4.34.4)

Rezultate testa omočljivosti in tvorbe spajkalnih kroglic smo primerjali med seboj in so zbrani v Tabeli 6 in Tabeli 7. Kot referenčno spajkalno pasto smo uporabili spajkalno pasto SnPbAg.

Tabela 6: Rezultati testa tvorbe spajkalnih kroglic

	Referenca SnPbAg R 244	SnAgCu NX 9900	SnAgCu X 13018	SnAg R 910
Iskratel Electronics	brez kroglic	brez kroglic	brez kroglic	tvorba kroglic
IJS		brez kroglic	brez kroglic	tvorba kroglic

Tabela 7: Rezultati testa omočljivosti

	Referenca SnPbAg R 244	SnAgCu NX 9900	SnAgCu X 13018	SnAg R 910
Iskratel Electronics	dobra omočljivost	dobra omočljivost	slaba omočljivost	slaba omočljivost
IJS		slaba omočljivost	slaba omočljivost	slaba omočljivost

4. Zaključek

Zahteva direktiv RoHS in WEEE po prepovedi uporabe svinca kot nevarne snovi po 1.7.2006 je prinesla nove tehnološke študije in raziskave v elektronsko industrijo na področju spajkanja. Različne študije so pokazale, da bo potrebno velik poudarek nameniti izbiri materialov, vpeljavi spajkanja brez svinca v proizvodnjo in vizuelni kontroli spojev. Zanesljivost novih produktov bo potrebno preveriti s klimo mehanskimi testi in testi življenjske dobe.

Po standardu IPC-TM 650 so bile testirane spajkalne paste brez svinca s sestavo SnAgCu in SnAg različnih proizvajalcev. Rezultate testa omočljivosti in tvorbe spajkalnih kroglic smo primerjali z referenčno spajkalno pasto SnPbAg. Razlika je predvsem opazna v slabši omočljivosti nekaterih past brez svinca. Ravno tako pa bo potrebno preveriti zanesljivost spojev z uporabo različnih spajkalnih past brez svinca in različnih prevlek na prevodnih likih tiskanih vezij na testnih ploščah s klimo mehanskimi testi in testi življenjske dobe.

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AVTOMATIZIRANO MERJENJE ENOSMERNIH KARAKTERISTIK POLPREVODNIŠKIH ELEMENTOV

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Kjučne besede: merjenje, avtomatizirano, mikrokrmilnik, LabVIEW, polprevodniški elementi, DA-pretvornik, AD-pretvornik, razdeljevalnik kanalov.

Izvleček: V prispevku obravnavamo avtomatizirano merjenje enosmernih karakteristik polprevodniških elementov. Na področju avtomatiziranega merjenja karakteristik obstajajo številne rešitve. Večina le-teh je ozko namenska in omogočajo merjenje le določenih polprevodniških elementov. Cilj je razviti široko zasnovan merilni sistem, ki bo omogočal avtomatsko merjenje različnih polprevodniških elementov. Takšna izvedba omogoča merjenje enostavnih karakteristik na primer diode in merjenje bolj kompleksnih parametričnih karakteristik na primer tranzistorja. Dodatna prednost take zasnove je možnost enostavne razširitve z novimi funkcijami na primer z raznimi analizami izmerjenih podatkov. Prikazani so splošna blokovna shema, lastnosti merilnega sistema in merilni rezultati. Za nastavljanje vrednosti vhodnih signalov in merjenje izhodnih je uporabljen mikrokrmilnik, za nadzor, predstavitev rezultatov, hranjenje vrednosti in obdelavo pa osebni računalnik. Zasnova merilnega sistema omogoča prosto izbiro programskega orodja, ki ga bomo uporabljali na osebnem računalniku. V našem primeru smo izbrali programski paket LabVIEW, ki omogoča hiter in enostaven razvoj, ter možnost nadgradnje programa z novimi funkcijami. Predstavljeni so primeri avtomatiziranih meritev in primerjava našega merilnega sistema s komercialno merilno kartico. Prednost našega merilnega sistema je predvsem v širšem merilnem območju merjenja, bistveno boljši tokovni zmogljivosti in cenovni ugodnosti sistema.

Automatic Measuring of One-way Characteristics of Semiconductor Elements

Key words: measuring, automatic, microcontroller, LabVIEW, semiconductor, DA-converter, AD-converter, multiplexer.

Abstract: On field of measuring of one-way characteristics of semiconductor elements we have always the same methods and procedures. Therefore is automation of those methods and procedures a logical step. There are many solutions in this field. Most of them have a very selected purpose, like measuring only certain semiconductor elements. Our goal was to develop as widely designed measuring system as possible. Such approach enables automatic measuring of different semiconductor elements. With our measuring system we can measure simple characteristics and more complex parametric characteristics.

General block scheme, properties of measuring system and examples of automatic measuring are shown. In general we have a personal computer on one side and microcontroller on the other side. Personal computer is used to control and present the results of the measuring. To make that possible, a computer program must be developed. The most appropriate tool for that is program package LabVIEW, which enables quick and simple development and possibility to upgrade program with new functions. LabVIEW is a development environment based on graphical programming. LabVIEW uses terminology, icons, and ideas familiar to technicians, scientists, and engineers, and relies on graphical symbols rather than textual language to describe programming actions. Further advantage of such design is the possibility of simple extension with new functions. For example in future different analyses of acquired data could be implemented. Microcontroller on the other side regulates control and data signals of DA-converter, AD-converter and multiplexer.

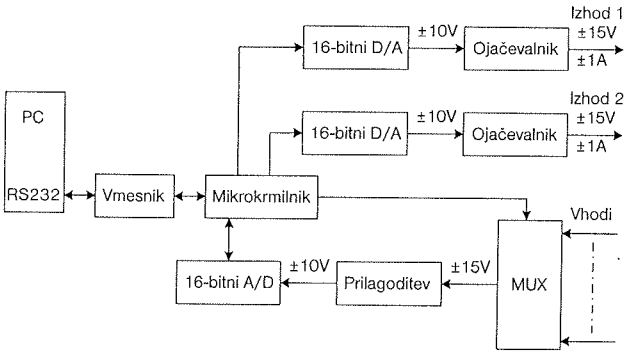
Our measuring system has two independent analog outputs with voltage range ±15V and ±1A current. Voltage range of ±15V is enough for measuring characteristic of most popular semiconductors. With 16-Bit DA-converter we have achieved accuracy of output value in range ±1mV. Measuring system can measure up to six input channels. At the end of the article one example of automatic measuring of simple characteristics and one of more complex parametric characteristics is shown. Also comparison with commercial measuring card with similar characteristic is shown. Advantage of our measuring system is wider measuring area, better current efficiency and lower price of system.

1 Uvod

Na področju merjenja enosmernih karakteristik polprevodniških elementov se srečujemo z znanimi postopki merjenja. Smiselna je avtomatizacija teh merilnih postopkov, za katere najdemo rešitve v podatkih proizvajalcev elementov in v strokovni literaturi /1/. Ponavadi te rešitve omogočajo merjenje le določenih karakteristik, ki so lastna posameznim elementom. Tako imamo primere, ko je avtomatizirano merjenje omejeno na posamezen tip polprevodniškega elementa in na posamezne karakteristike. Želeli smo zgraditi univerzalnii merilni sistem, ki bo omogočal merjenje različnih karakteristik. Postavili smo si naslednje zahteve za merilni sistem: - imeti mora vsaj dva neodvisna analogna izhoda, ki zmoreta dati na svojih izhodih napetosti v območju ±15V in tok ±1A, - za potrebe merjenja naj ima vsaj 6 analognih vhodov ter - obdelava izmerjenih rezultatov in prikaz le-teh se naj izvaja na osebnem računalniku. Takšen merilni sistem smo načrtovali z uporabo mikrokrmilnika, ki upravlja z vhodno izhodnimi enotami, hkrati pa je povezan z osebnim računalnikom in tvori celovit merilni sistem. Na strani osebnega računalnika je potrebno razviti primerno programsko opremo za prikaz in nadzor meritev.

2 Blokovna shema in opis delovanja sistema

Blokovno shemo merilnega sistema prikazuje slika 2.1. Merilni sistem sestavljajo naslednji sklopi: vmesnik, mikrokrmilnik, dva DA-pretvornika, dva izhodna ojačevalnika, razdeljevalnik kanalov (MUX), prilagoditev in AD-pretvornik. Za povezavo med računalnikom in merilnim sistemom smo izbrali RS232 vmesnik. Vmesnik prilagodi napetostne nivoje med osebnim računalnikom in mikrokrmilnikom. Na ukaz iz računalnika mikrokrmilnik ustrezno nastavi vhodno izhodne enote: AD-pretvornik, DA-pretvornik in razdeljevalnik kanalov in posreduje izmerjene vrednosti računalniku. Ker želimo čim večjo točnost izhodnih vrednosti je potrebno izbrati DA-pretvornik, ki bo imel dovolj veliko bitno ločljivost in možnost nastavljanja pozitivnih in negativnih vrednosti. Izbrali smo DA-pretvornik z izhodnim obsegom ± 10V, 16-bitno ločljivostjo in zaporednim vpisovanjem nove vrednosti /2/. Izbor je temeljil na kompromisu med ceno in zmogljivostjo DA-pretvornikov, ki so na voljo na tržišču.



Slika 2.1: Blokovna shema merilnega sistema.

Ker je tokovna zmogljivost DA-pretvornika nekaj mA je potreben izhodni ojačevalnik. S pomočjo ojačevalnika smo razširili izhodno območje sistema na ± 15V in tokovno zmogljivost na ± 1A. Ker potrebujemo več analognih vhodov imamo v vezju razdeljevalnik kanalov. Merilni sistem smo s tem razširili na 6 analognih vhodov. Prilagoditev je potrebna zaradi AD-pretvornika, ki zmore meriti znotraj območja ± 10V. Realizirana je lahko z enostavnim uporovnim delilnikom in operacijskim ojačevalnikom. Paziti je potrebno na impendanco takega delilnika, da ne vplivamo na dejansko vrednost, ki jo merimo. AD-pretvornik mora imeti podobne lastnosti kot DA-pretvornik, če želimo dobro točnost celotnega merilnega sistema. Izbrali smo AD-pretvornik, s katerim lahko merimo napetost v območju ± 10V s 16-bitno ločljivostjo /3/.

Uporabniški vmesnik za osebni računalnik smo razvili v programskem paketu LabVIEW. LabVIEW omogoča hitrejši način programiranja merilnih in instrumentacijskih sistemov brez izgube zmogljivosti sistema /4, 5/. Na čelno ploščo virtualnih instrumentov (VI), postavimo kontrole in prikazovalnike za podatke potrebne v našem sistemu z enostavno izbiro objektov iz nabora kontrol. Kontrole so lahko enostavni prikazovalniki, analogni merilniki, grafi, stikala, itd. Ko je virtualni instrument izdelan, lahko preko čelne plošče upravljamo s procesom oziroma aplikacijo. Programiramo v diagramskem oknu, kjer iz nabora funkcij izberemo grafične objekte ali ikone. Posamezne ikone nato med seboj povežemo in jim določimo želeni pretok podatkov v našem programu. Vodenje izvajanja programa glede na tok podatkov med posameznimi ikonami omogoča enostavno izdelavo aplikacij, kjer lahko več operacij znotraj enega programa opravljamo simultano.

Izbor programskega paketa za razvoj uporabniškega vmesnika prinaša določeno prednost pred drugimi podobnimi sistemi. Tako je možno sistem dokaj enostavno in hitro prilagoditi potrebam uporabnika.

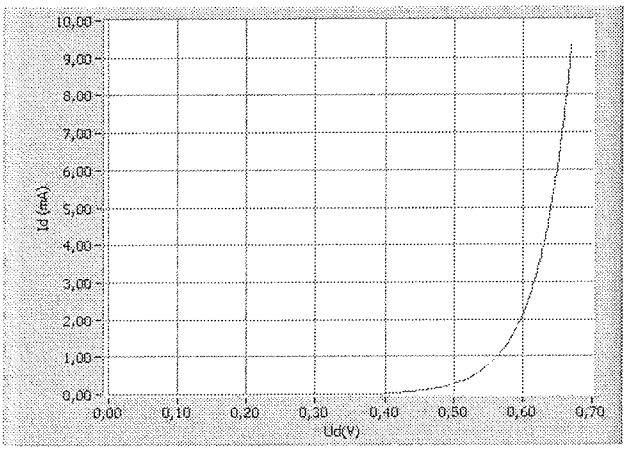
3 Rezultati

Avtomatizirano merjenje polprevodniških elementov lahko s stališča merilnega sistema uvrstimo v dve skupini. V prvo skupino elementov uvrstimo enovhodne elemente, kot je na primer dioda. V drugo skupino elementov uvrstimo dvovhodne elemente, kjer merimo karakteristiko elementa v odvisnosti od dveh neodvisnih napetosti ali tokov. Predstavnik te skupine je MOS-FET tranzistor. Zato so v nadaljevanju prikazani le rezultati avtomatiziranega merjenja tipičnega predstavnika vsake skupine.

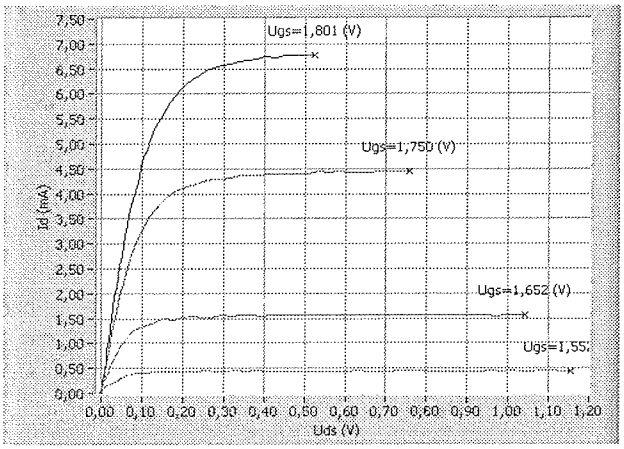
Za lažjo primerjavo in ovrednotenje merilnih rezultatov smo za primerjavo rezultatov meritev uporabili komercialno kartico NI PCI-6014 podjetja National Instruments /6, 7/. Kartico je možno uporabiti za različne aplikacije. Kartice ima šestnajst analognih vhodov s 16-bitno ločljivostjo (± 10V), dva analogna izhoda s 16-bitno ločljivostjo (± 10V) in tokovna zmogljivostjo nekaj mA. Če primerjamo te podatke z našim merilnim sistemom opazimo, da ima naš sistem večje vhodno in izhodno območje merjenja (± 15V), ter bistveno boljšo tokovno zmogljivost (± 1A).

Tako pri kartici kot pri našem merilnem sistemu je bilo potrebno program za prikaz enosmernih karakteristik polprevodniških elementov posebej razviti. Pri komercialnih karticah ponavadi specifična programska oprema, kot je na primer merjenje enosmernih karakteristik polprevodniških elementov, namreč ni vključena v ceno samega sistema in jo je potrebno razviti oziroma dodatno kupiti.

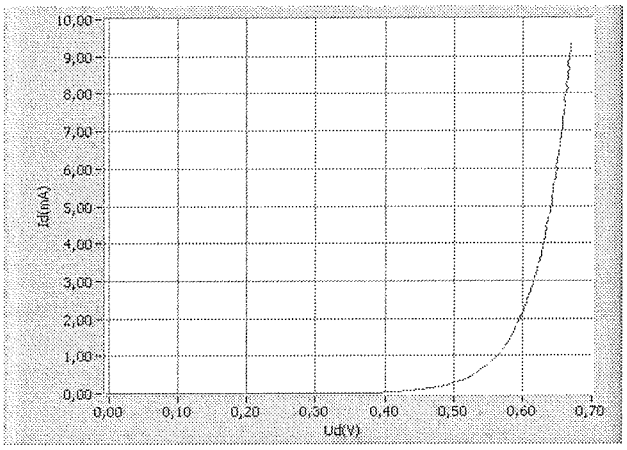
Na sliki 3.1 si lahko ogledamo karakteristike diode izmerjeno s kartico NI PCI-6014. Na sliki 3.2 je prikazana karakteristika iste diode ob enakem številu merilnih točk in območju merjenja z našim merilnim sistemom. Opazimo lahko, da sta izmerjeni karakteristiki identični. Z izgradnjo lastnega merilnega sistema smo tako dobili sistem, ki je primerljiv z drugimi komercialnimi merilnimi sistemi in omogoča meritve v napetostnem in tokovnem območju, ki jih z opisano komercialno kartico ne bi mogli izvesti.



Slika 3.1: Primer meritve diode s kartico NI PCI-6014.



Slika 3.3: Primer meritve MOS-FET tranzistorja.



Slika 3.2: Primer meritve diode z našim merilnim sistemom.

Slika 3.3 prikazuje avtomatizirane meritev parametrične karakteristike MOS-FET tranzistorja. Merjenje parametričnih karakteristik je zahtevnejše predvsem iz vidika prikaza merilnih rezultatov v grafični obliki. Na grafu je potrebno izrisati več krivulj in za vsako krivuljo prikazati vrednost parametra, ki ga predstavlja. Program omogoča še številne možnosti za delo z merilnimi rezultati, kot so na primer: podrobnejši ogled dela krivulje, izpis posameznih vrednosti v merilnih točkah in istočasen prikaz lege le teh na grafu, določanje izgleda samega grafa (barve, imena osi, ime parametra).

Ocena točnosti in odstopanj meritev obeh merilnih sistemov smo opravili na vzorcu 100 meritev. Prva vrstica v tabeli 3.2 in 3.1 predstavlja vrednost, ki jo želimo nastaviti na izhodu sistema. V drugi koloni podana napetost, ki smo jo izmerili z digitalnim voltmetrom z oznako HP 3455A. Tretja

Tabela 3.1: Izmerjene vrednosti za kartico NI PCI-6014.

U (V)	-10	-5	0	5	9.5[1]
Dig. voltmeter HP 3455A	-9,9987	-5,9986	0,0008	5,0007	9,5006
Srednja vrednost meritev	-9,9982	-4,9982	0,0015	5,0015	9,5010
Odstopanje od želene vred.	0,0018	0,0018	0,0015	0,0015	0,0010
St. deviacija meritev (mV)	0,450	0,433	0,460	0,413	0,412

Tabela 3.2: Izmerjene vrednosti za naš merilni sistem.

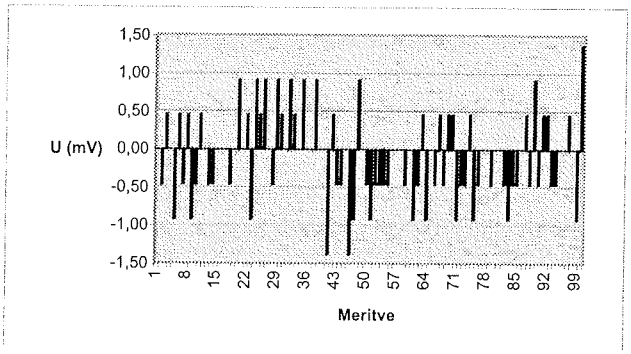
U (V)	-15	-10	-5	0	5	10	15
Dig. voltmeter HP 3455A	-15,001	-10,0004	-4,9991	0,0013	5,0024	10,0035	15,003
Srednja vrednost meritev	-14,9973	-10,0008	-4,9997	0,0014	5,0033	10,0044	14,9981
Odstopanje vred.	0,0027	0,0004	0,0003	0,0014	0, 0033	0,0044	0,0019
St. deviacija meritev (mV)	0,768	1,204	1,254	1,389	1,586	1,108	0,636
St. deviacija meritev (n=10)	0,242	0,577	0,363	0,510	0,423	0,531	0,309

1 *Meritev pri +10V je bila za oceno točnosti in odstopanj meritev nerealna, ker je bila merjena napetost na zgornji meji, ki jo je še možno izmeriti s kartico in smo zato dobili za rezultat vedno točno +10V.*

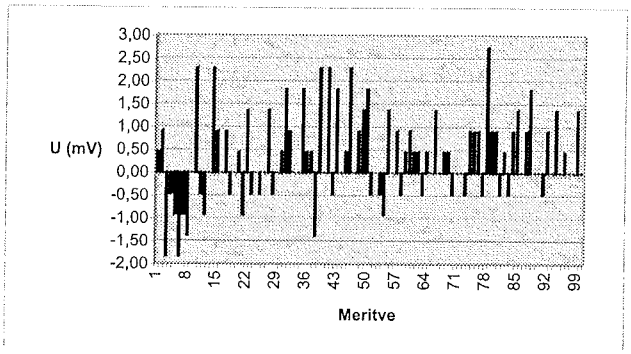
kolona predstavlja srednjo vrednost vseh 100 meritev. V četrti koloni je izračunano odstopanje od vrednosti, ki smo jo želeli nastaviti. Peta kolona predstavlja izračunano standardno deviacijo meritev.

Posledica širšega območja, ki ga pokrivamo (LSB[2] izraženo v mV predstavlja za 50% večjo vrednost) je večje odstopanje v primerjava s komercialno kartico. Boljše rezultate glede odstopanja posameznih meritev dosežemo z večkratnim merjenjem iste vrednosti in izračunom povprečne vrednosti (zadnja kolona v tabeli 3.2). Standardna deviacija se z številom meritev n zmanjša za faktor $\sqrt{n}$ /8/. Z izbiro n=10 smo izboljšali standardno deviacijo za približno 3 krat. Rezultati so v tem primeru primerljivi s komercialno kartico. Merilni sistem omogoča, da faktor n izberemo glede na točnost, ki jo želimo doseči pri meritvi.

Sliki 3.4 in 3.5 predstavljata grafični prikaz odstopanja posameznih meritev v primeru ko merimo konstantno napetost. Na sliki 3.4 smo merili referenčno napetost. Zato je odstopanje meritev odvisno le od točnosti merilnega dela. Na sliki 3.5 je odstopanje odvisno še od točnosti dela merilnega sistema, s katerim nastavljamo izhodno napetost. Zato je tudi območje, v katerem se pojavljajo rezultati meritev, širše.



Slika 3.4: Odstopanje posameznih meritev v primeru merjenja neke referenčne napetosti (n=100).



Slika 3.5: Odstopanje posameznih meritev v primeru nastavljanja in merjenja neke napetosti z našim sistemom (n=100).

2 *LSB - least significant bit (najmanj uteženi bit).*

Če na koncu povzamemo bistvene lastnosti merilnega sistema:

- napetostno območje ± 15 V,
- tokovno območje ± 1A,
- točnost nastavljanje izhodne vrednosti je ± 2mV,
- točnost merjenja ± 2mV,
- dva izhodna kanala in
- šest vhodnih kanalov.

Programska oprema omogoča:

- prikaz osnovnih karakteristik (npr. dioda),
- prikaz parametričnih karakteristik (npr. tranzistor),
- posredno merjenje (merjenje električnega toka),
- shranjevanje merjenih rezultatov v tekstovni obliki (tabela) in
- shranjevanje merjenih rezultatov v grafični obliki.

Pretočnost podatkov merilnega sistema je neposredno odvisna od načina komunikacije med mikrokrmilnikom in osebnim računalnikom. Z izbiro zaporedne komunikacije z RS232 vmesnikom je pretočnost podatkov 19200 Baud/s. Ker merimo enosmerne karakteristike, ki se časovno ne spreminjajo sama hitrost merjenja ni tako bistvena za učinkovitost merilnega sistema. Prav tako ima merilni sistem vgrajena dva varnostna mehanizma (elektronski in programski). Elektronski varnostni mehanizem preprečuje uničenje samega merilnega sistema. Največjo nevarnost za uničenje merilnega sistema predstavlja prevelik izhodni tok. Zato je ta omejen na maksimalno ± 1A. Prav tako imata izhodna ojačevalnika vgrajeno termično zaščito, ki izklopi izhodna ojačevalnika ob preveliki obremenitvi. S pomočjo diod je narejena še zaščita pred napetostni na izhodu, ki so večje od napajalnih napetosti izhodnih ojačevalnikov. Programski varnostni mehanizem nam omogoča predvsem zaščito merjenca. S programom je omogočena izbira maksimalnega toka v območju od 0 do 1 A, ki sme teči skozi merjenec med meritvijo.

4 Zaključek

V članku smo prikazali merilni sistem za merjenje enosmernih karakteristik polprevodniških elementov. Predstavljen merilni sistem je uporaben za merjenje enosmernih karakteristik različnih polprevodniških elementov. Omejitev predstavlja edino izhodno območje oziroma območje merjenja, saj je možno merjenje karakteristike v območju ± 15V. Vendar v tem napetostnem območju deluje večina polprevodniških elementov, ki se najbolj pogosto uporabljajo v elektroniki. Z meritvami in analizo našega merilnega sistema smo ugotovili, da je sistem primerljiv s podobnimi merilnimi sistemi oziroma jih v določenih pogledih celo presega. Pomembna prednost razvitega merilnega sistema pred drugimi je tudi v cenovno ugodni razširljivosti.

Tabela 3.3: Primerjava obeh merilnih sistemov.

	Napetostno območje	Tokovna zmogljivost	Število merilnih kanalov	Število izhodnih kanalov	LSB	Relativna točnost	Največji absolutni pogrešek
NI PCI-6014	± 10V	± 5mA	8	2	305μV	1084μV	1,9mV
Naš sistem	± 15V	± 1A	6	2	457μV	2mV	4,5mV

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NEW NONVOLATILE MEMORY TECHNOLOGIES - A SURVEY

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Key words: nonvolatile memory, flash ram, feroelectric memory, magnetoresistive memory, ovonic unified memory

Abstract: The use of nonvolatile memory is growing rapidly. Their use ranges from the applications in computers, digital photography to mobile telephony. The drawbacks of current nonvolatile memory technology (flash ram) are relatively low endurance, low speed and the use of high voltages for program/erase operations. In recent years several new nonvolatile memory technologies have emerged based on different physical phenomenons. They tend to provide unlimited endurance, high speed and are easier to integrate into the process flow of standard logic circuit. The main challenging technologies to traditional flash ram are ferroelectric memory, magnetoresistive memory and ovonic unified memory. Several largest companies already developed memories based on this new technologies but currently only low capacity devices are available.

Pregled novih tehnologij neizbrisljivega pomnilnika

Kjučne besede: neizbrisljiv pomnilnik, pomnilnik flash, feroelektrični pomnilnik, magnetouporovni pomnilnik, sprememba faznega stanja

Izvleček: Neizbrisljiv pomnilnik se vedno bolj uporablja na različnih področjih. Uporabljamo ga tako v računalnikih, digitalnih fotoaparatih kot tudi v mobilnih telefonih ter tudi mnogih drugih napravah. Pomanjkljivosti obstoječe tehnologije neizbrisljivega pomnilnika so predvsem relativno kratka življenjska doba, počasnost ter uporaba relativno visokih napetosti pri zapisovanju vsebine. V zadnje času so se pojavile nove tehnologije, ki za shranjevanje podatkov uporabljajo druge fizikalne pojave. Nove tehnologije obetajo predvsem neomejeno življenjsko dobo, večje hitrosti delovanja kot tudi lažjo integracijo v proizvodnjo električnih vezij. Nove tehnologije neizbrisljivega pomnilnika so feroelektrični pomnilnik, magneto-uporovni pomnilnik ter pomnilnik na osnovi spremembe faznega stanja materialov. Nekateri največji proizvajalci so že razvili pomnilniška vezja osnovana na teh tehnologijah, a kapaciteta le-teh je še relativno majhna.

Introduction

Since the beginning of the use of computers, nonvolatile memory was their essential part. Semiconductor ROM and PROM were one of the first technologies of the nonvolatile memory however their lack of changing their contents limited its widespread use. The EPROM and EEPROM were their successors. This technology enabled to clear the contents of the device by submitting them to the ultraviolet light or high voltage. While these devices were suitable for storing the firmware and BIOS (Basic Input/Output System), which changes very rarely, they couldn't be used as a storage device.

It was the appearance of the Flash RAM that dramatically changed the use of nonvolatile memory. As one could expect the Flash RAM initially made its way to the computers BIOS and firmware of different peripheral devices. But due to its programmability it soon became a vital part of nearly every electronic system. In the cell phone the flash RAM holds the instructions to send and receive calls, stores the phone numbers, messages and phone settings. Electronic products of all types, from consumer appliances to the industrial machinery, use them for storing the operational instructions.

Flash RAM

Flash memory is a programmable, read-only, non-volatile memory similar to EPROM and EEPROM memory /1/. While it is a derivate of EEPROM the main difference is in the ERASE operation. Flash memory uses in-circuit wiring to apply erase function to the predetermined sections known as blocks or the whole memory.

Flash memory cell is composed of MOS transistor constructed with two gates: the control gate (CG) and the floating gate (FG), which is placed between the control gate and transistor's channel. Floating gate is isolated from the control gate and the channel by a thin oxide layer as shown in Figure 1. This isolation allows the floating gate to store the electrons (electric charge) when the power is cut off, so the memory is non-volatile.

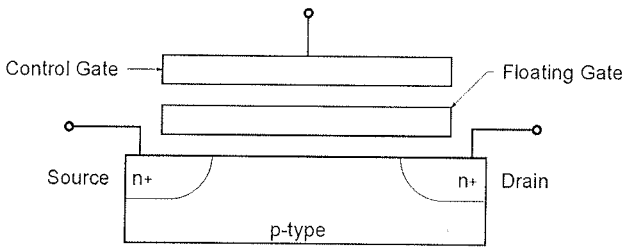

Figure 1: The structure of flash memory cell

Reading the value of the flash cell is relatively simple. The control gate is brought to logic 1 level. If there are no electrons at the floating gate then the transistor turns on. But if there are electrons at the floating gate, the charge blocks the impact of the electrical field induced by the control gate and the transistor remains in off state.

Writing to the flash memory is actually a two-phase process. First the trapped electrons are removed from the floating gate of a block of memory (ERASE operation). Blocks can consists of several thousand transistors. The ERASE operation is performed using the Fowler-Nordheim tunnelling effect. The high voltage (Vpp=12V) is applied to the source of the transistor while the control gate grounded and the drain of the transistor is not connected as depicted in Figure 2. By applying this high voltage the electrons trapped on the floating gate are drained across the thin oxide isolation barrier to the source

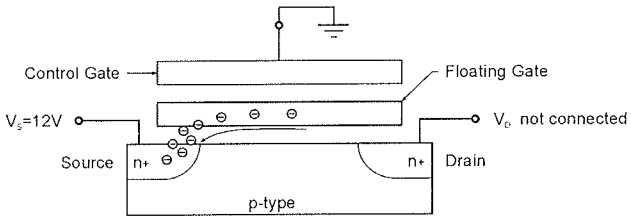

Figure 2: Erase operation using Fowler-Nordheim tunnelling effect

In the second phase the cell is programmed by transferring the electrons to the floating gates of the designated cells (WRITE operation). This is achieved using channel hot electron injection. The high programming voltage (Vpp=12V) is applied to the control gate, which forms the inversion region in the p-type substrate. The drain voltage is increased while the source is grounded. With the formed inversion region the current between the drain and source increases. This causes the electrons to gain sufficient energy to overcome the oxide barrier and collect on the floating gate as shown in Figure 3.

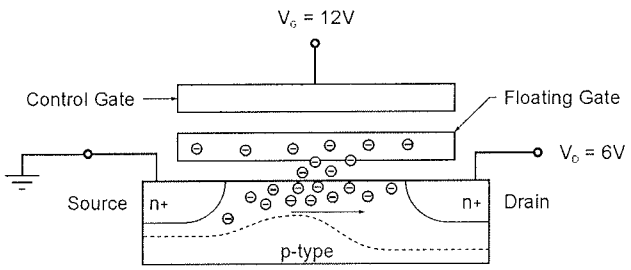

Figure 3: Write operation using the Channel Hot Electron Injection

This last operation is the cause for the main drawback of the flash memory, its endurance. Electrons shooting through the oxide barrier create defects in it that eventually cause the leakage between the floating gate and the channel. The flash memory sustains only a couple of ten thousands write cycles. This is not a problem for storing a computer BIOS, device firmware or even a cell phone, but it is a limitation for the use of digital cameras and other portable storage devices. This is especially notable with the use of nonvolatile disks.

Feroelectric memory

Ferroelectric memory (FeRAM or FRAM) technology /2,3/ is the most advanced rival of the flash technology. The core of the FeRAM cell is a capacitor formed by depositing a film of ferroelectric material in crystalline form between its plates. Lead-Zirconium-Titanate (PZT) or Barium-Strontium-Titanate (SBT) are usually used as a ferroelectric material. A model of a ferroelectric crystal is shown in Figure 4. A ferroelectric crystal has a mobile atom in the centre of the crystal. Applying electrical field to the lattice move the central atom in the field's direction. Reversing the field cause the atom to move in opposite direction. The central atom has two stable positions: at the top and at the bottom of the crystal lattice thus when the electrical field is removed the atom stays in the stable position.

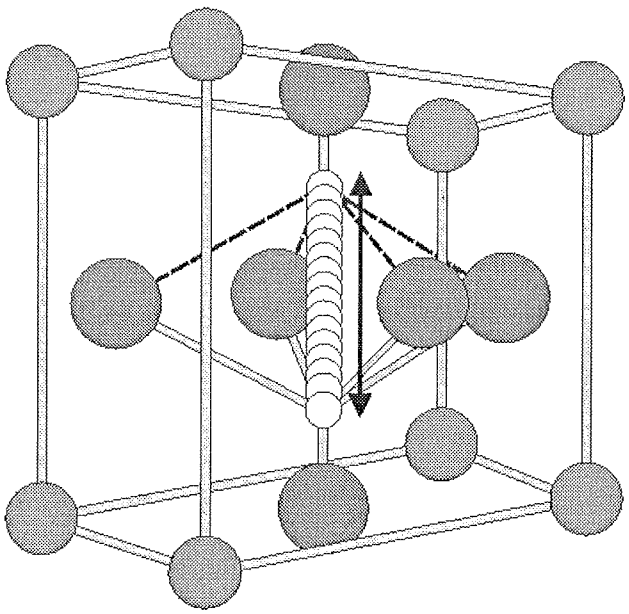

Figure 4: The structure of the ferroelectric crystal

As mentioned, the memory element of FeRAM is capacitor, however it does not store the data as linear charge but as electrical dipole. In order to read the memory cell the position of the central atoms has to be determined. Unfortunately this cannot be directly measured. Read operation is performed by employing the electrical field to the capacitor. If the central atoms in the lattice are in stable position opposite to the field direction they move in the field direction. If they are already in the stable position in the field direction, they stay put. As the atoms moves through the crystal a charge spike is emitted. A capacitor with switching electrical dipole of ferroelectric crystal produce larger charge spike than a capacitor where the dipole remains the same. The non-switching capacitor emits the charge equivalent to the charge emitted by ordinary capacitor. The memory circuit must determine whether the capacitor switched.

Read operation of the FeRAM cell involves the change of cell's state therefore the memory circuit has to restore the

initial cell state, just like in a DRAM cell. In fact FeRAM cell is similar to the DRAM cell. DRAM cell for the capacitor dielectric uses the silicon oxide and the data is stored as charge of cell's capacitor, which leaks into the substrate unless it is periodically rewritten. The state switch of FeRAM cell occurs in less than 1 ns and the complete circuit access is done in less than 50 ns.

Write operation of the FeRAM cell is very simple and does not require additional circuit. The data is applied to the FeRAM cell capacitor and the state of the ferroelectric crystal switches if necessary. The access time in the case of write operation is similar to the access time in read operation.

Initial FeRAM memory architecture consisted of two-transistors/two-capacitors (2T/2C) as shown in Figure 5.a. In this architecture for each data bit its own reference is provided achieving the robust data retention reliability. However the drawback of this architecture is relatively large cell size. With advances in ferroelectric materials and processing the need for internal reference capacitor was eliminated. As result one-transistor/one-capacitor architecture similar to DRAM architecture depicted in Figure 5.b was introduced.

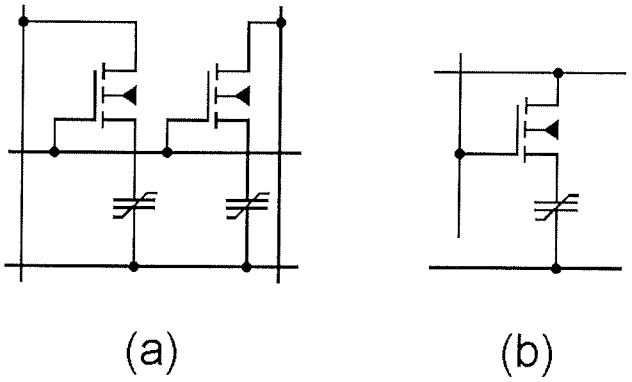

Figure 5: The structure of the FeRAM memory cell (a) 2T/2C and (b) 1T/1C

The major difference between FeRAM and flash memory is in difficulty of write operations. Writing the data to the flash memory involves erase and write operation in which electrons are pushed through the oxide barrier. This requires high voltages and relatively long time. Write time for flash memory is several tens ms while write access time for FeRAM is under 100 ns. Additionally flash memory allow very limited numbers of write operation due to the oxide barrier degradation. The endurance of the FeRAM memory is more then 10^{12} write cycles since write operation does not produce any stress. Finally no high voltages are needed for the write operation of the FeRAM memory.

While Ramtron International Corp. already fabricates and sells FeRAM devices since 1992 their capacity is still relatively small. Largest memories produced by Ramtron are 256Kb, which represents a small fraction of the gigabit chips offered by the major flash memory producers. Several other companies are also pursuing FeRAM as a replacement for today's non-volatile flash memory. Texas Instruments reported to produce a 64 Mb device for embedded applications /4/. Fujitsu, Samsung and others are also working on the development of larger FeRAM devices mainly for the use in the embedded systems.

Magneto-resistive memory

The magneto-resistive memory (MRAM) is an emerging memory technology that stores information using the magnetic moments of a thin ferromagnetic layer /2,5/. Atoms in a ferromagnetic material act like tiny magnets and respond to the external magnetic field aligning themselves in its direction. Similar to the ferroelectric materials they form domains. Applying an external magnetic field to the ferromagnetic material its domains line up with the external magnetic field and remain oriented in the same direction when the magnetic field is removed. When the magnetic field in opposite direction is applied, the domains flip over. MRAM uses the magnetic moments of a thin ferromagnetic material to store information.

The core of MRAM cell is Magnetic Tunnel Junction (MTJ) composed of two ferromagnetic layers, storage layer and reference layer, separated by thin insulating layer. If the insulation layer is ticker then few nanometers, the insulator stops the passage of the electrons. However insulation layer of the tunnel junction is thinner than 2 nm and some electrons can tunnel across it from one ferromagnetic layer to another. The magnetic moment of the reference layer is fixed while the magnetic moment of the storage layer change its direction in response to the applied magnetic field. In order to read the memory cell the orientation of the magnetic moment of the storage has to be determined. As in the case of FeRAM cell this cannot be measured directly. The orientation of the magnetic moment of storage layer can be parallel or anti-parallel with the orientation of the magnetic moment of the reference layer. When the magnetic moments are parallel the resistance of the MTJ is smaller then when they are anti-parallel.

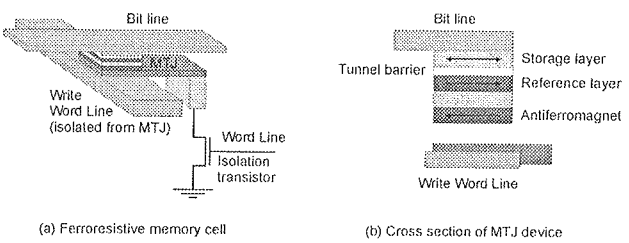

Figure 6. The structure of the Magnetic Tunnel Junction

Reading the MRAM cell is straightforward, small electric current is passed via word and bit lines through the MTJ of the selected cell. When the orientation of the magnetic moments is parallel the resistance is low and if the orienta-

tion is anti-parallel the resistance is high. To determine whether the resistance is high or low, the resistance is compared to the resistance of the reference memory cell along the same wordline. As reported by Motorola one reference cell is needed for every 64 memory cells in their 1Mb MRAM sample.

Writing the data into the cell is achieved by passing the current pulses through the wires close to (but not connected to) the magnetic cells. The magnetic field generated by the current in wires is used for changing the direction of magnetic moment in MTJ. The wires and cells are arranged in cross-point architecture depicted in Figure 7. The set of wires called bit lines run in parallel above the magnetic cells. The other set of wires called word lines runs under the magnetic cells perpendicular to the bit lines. Word lines are isolated from memory cells. MTJ are set up at intersections of the word and bit lines. To write a data to chosen memory cell the current pulse is applied to both its bit line and its word line. Only joint magnetic field of both lines is strong enough to change the direction of magnetic moments thus other MTJ along the bit and word lines remain unaffected.

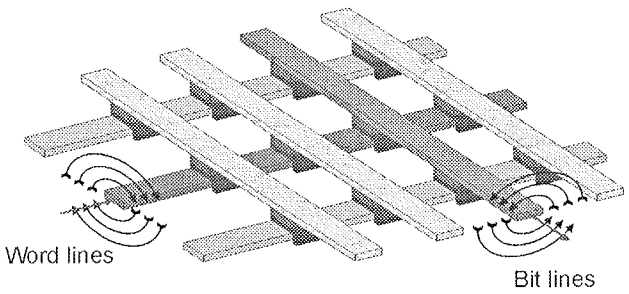

Figure 7: Cross-point architecture of the memory

MRAM has many advantages over other types of memory. It is faster than Flash memory, actually it could be even faster then DRAM and almost as fast as SRAM (Static RAM) /6/. MRAM has also the potential of extremely dense packaging. The only limiting factor is the density of the set of wires. Several MRAM layers can also be placed on top of a single die. The endurance of MRAM is also extremely high (10^{14} write cycles) and at last MRAM is nonvolatile since the magnetic moments maintain their alignment even when the power is switched off.

MRAM also has several potential drawbacks. It requires relatively high power to write and the MRAM layer may interfere with heat dissipation. Main problems in MRAM production are related to the thin insulation layer a key element of each MTJ. It must be uniform across the wafer since the resistance of MTJ rises exponentially with its thickness. To ensure reliable readout of the cell the difference in the resistance of the parallel and anti-parallel magnetic moments in MTJ must be significant. At the beginning of the development of MRAM cell it was around 5% but with the use of different materials in MTJ and reducing insulation thickness the 40% change of resistance was achieved.

The research and development of MRAM memory started in IBM, where similar techniques were introduced in design of hard disks heads which drastically increased the capacity of new hard drives. Infineon joined IBM in development of new MRAM chip /7/. It is expected that first prototypes of capacity 256Mb should be available in year 2004. Motorola, considered a leader in the development of MRAM technology, introduced their 1Mb MRAM chip in April 2002 /8/ and new 4Mb MRAM chip in October 2003 /9/. NEC and Toshiba joined in the development of their own 256Mb MRAM device.

Ovonic unified memory

The Ovonic Unified Memory (OUM) technology is another promising nonvolatile technology. It uses the reversible structural phase-change from the crystalline phase to amorphous phase as a storage mechanism /2,10/. Several chalcogenide alloys exhibit reversible phase-change and are used in optical fibers and rewriteable CDs and DVDs. The OUM technology uses a thin film chalcogenide alloy of germanium, antimony and tellurium ($Ge_xSb_yTe_z$). These alloys are suitable for memory elements because it can rapidly switch, when heated and cooled, between both amorphous and crystalline phase. Each phase state represents different digital value. When alloy is in amorphous phase it has low light reflectivity and high resistance, while in crystalline phase its reflectivity is high and the resistance is low. This property of the chalcogenide alloys is also used in rewriteable optical media.

The schematic illustration of the OUM memory cell cross section is shown in Figure 8. It consists of a layer of the chalcogenide alloy and a resistive heating element placed in between connecting electrodes. The portion of the thin chalcogenide alloy in the junction with the heater is heated and cooled in order to switch the phase of the alloy. This switch in the phase of material causes significant change in alloy resistance. Because of the ultra small size of the media programmed thermal time constant of the device are very shot, on the order of a nanosecond. Since the write energy also scale with the programmed media volume the power consumption of the write operation is very low.

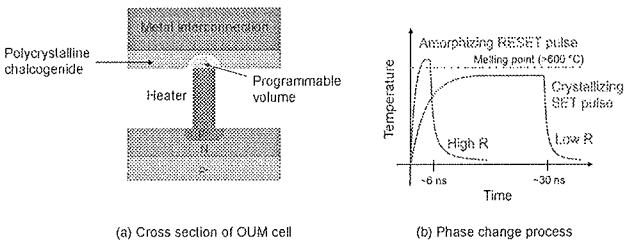

Figure 8: (a) schematic cross section of the OUM memory cell, (b) phase change process

Reading the content of the OUM memory cell is similar to reading the MRAM memory cell. It is done by measuring

its resistance however the change of the resistance is much larger, approximately a factor of 100. Due to the large range of programmed resistance a multi-bit per cell storage capability is possible.

Writing the data into OUM memory cell is achieved by heating the chalcogenide near its melting point and then rapidly cooling it. The actual parameters of the heating process depend on the value to be programmed into the device. The set pulse is applied to change the phase of chalcogenide to crystalline phase. During this pulse the temperature of the material is held just below the melting point for a time sufficient for crystal growth. The reset pulse change the phase of the material to amorphous phase. This pulse has slightly higher amplitude and cause the programmed material to melt and eliminates the crystalline structure. When the reset pulse is terminated the material "freeze" in the disordered amorphous structure.

OUM memory technology is more endurable and faster then Flash memory. Potentially, it can be even denser than both MRAM and FeRAM memory technology. It has faster read/write access than FeRAM technology however MRAM cells are faster. On the other hand the power dissipation is lower then the power dissipation of MRAM cell. Its main advantage over their competitors is easy integration into conventional CMOS process technology.

OUM memory technology is based on proprietary technology originally developed by and exclusively licensed from Energy Conversion Devices, Inc (ECD, Inc). The Ovonyx, Inc. the wholly owned subsidiary of ECD, Inc is further developing the OUM technology. The largest device made to date is 4Mb array built with partner Intel Corp. /11/. Ovonyx is also working with other semiconductor producers namely STMicroelectronics, which has announced to present their first OUM samples in 2005.

Summary

Besides the presented new memory technologies there is ongoing effort in developing other memory technologies as well. Polymer memories, carbon nanotube memory, single electron memories and nitride storage memory are only some of them. However they are still more or less at the beginning of the development phase.

The well-established technologies as flash RAM are also further developed to overcome their weakness. Multi-bit storage is that would rise the device density is considered in several technologies. Also the use of diode instead of transistor or even cells without transistor are developed to achieve higher memory density.

Presented technologies are adopted by major semiconductor producers and, while each of them provides technical challenges to be overcome, first product can be expected soon. The comparision of described technologies with proven memory technologies is given in following table.

As one can see new technologies outperform the flash memory and can even be compared with DRAM. However their current capacity is too small to present a serious threat for both flash and DRAM memory. Currently they are mainly used in embedded systems where the memory is placed on a same die as processor and other devices. Due to the rapid development of these new as well as traditional technologies the given comparison may soon become inaccurate. The race for predominant memory technology is still open.

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	SRAM	DRAM	Flash	FeRAM	MRAM	OUM
Capacity [Mb]	4		4096	64	4	4
Structure	6T	1T/1C	1T	1T/1C	1T/1MTJ	1T
Cell size [F^2]	50-80	6-12	7-11	18	10-20	5-8
Access time [ns]	1	20	50	20	15	20
Write time [ns]	1	20	2 ms	20	15	20
Voltage [V]	3.3	3.3	3.3 and 12	3.3	3.3	3.3
Write Power	high	medium	high	medium	medium	low
Retention	volatile	volatile	> 10 yrs	> 10 yrs	> 10 yrs	> 10 yrs
Endurance			10^5	10^{13}	10^{15}	10^{13}
Multi-bit	no	no	yes	no	no	yes
Availability	now	now	now	now	2004	2004

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APPARATUS FOR MEASUREMENTS OF PHYSIOLOGICAL PARAMETERS IN FISH

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Key words: fish physiology, in vivo experiments, apparatus, ECG, water flow pressure, gill movement

Abstract: A special apparatus for simultaneous recording of a fish gill movement, ECG and water flow through a fish mouth was designed, developed and experimentally tested. A pair of single channel force transducers with linear dependence of the output voltage upon the load 0.5 mV/mN over the nominal range of 0-70 mN at a bridge excitation of 5V was used for recording the curves of gill movements. Wires fixed with the fishing hooks into the fish body and on the other side connected to the amplifier were used for ECG recordings. A pressure transducer recorded a water flow through a fish mouth. We recommend our set up as a simple and useful tool for recording the described physiological parameters in experiments with fish.

Naprava za merjenje fizioloških parametrov pri ribah

Kjučne besede: ribja fiziologija, poskusi v živem, naprava, ECG, tlak vodnega pretoka, pomik škrg

Izvleček: Razvili, izdelali ter testirali smo posebno napravo za merjenje gibanja ribjih škrg, EKG, ter pretoka vode skozi ribja usta. Gibanje ribjih škrg smo spremljali s parom mehansko-električnih pretvornikov, ki linearno merita mehanske obremenitve v razponu 0-70 mN. EKG smo snemali prek izoliranih žic, ki so bile s trnki na eni strani pritrjeni v ribjo kožo na drugi strani pa v ojačevalnik. S posebnim merilcem pritiska smo spremljali pretok vode skozi usta testirane živali. Izdelana aparatura je preprosta, praktična in poceni pripomoček za spremljanje določenih fizioloških parametrov pri ribah.

1. Introduction

In vivo experiments on fish represent a problem when vital parameters have to be recorded in a simulated "natural" environment. There is not much commercially available recording equipment for simultaneous measurements of respiratory activity and cardiac function. However, various measuring equipment has been developed of different authors for the certain experimental purposes /1-3/. We designed, developed and experimentally tested a special setup for simultaneous recording of fish gill movements, ECG and water pressure change in the mouth of fish. The pressure change produces the necessary water flow through the gills by coordinated mouth and gill movements.

2. Material and Methods

The frame of the apparatus was made of a plastic block fixed on a plastic plate. Into a plastic block a cone was drilled with a small hole in the front side of the cone. The broad part of the cone was opened to the back. On both sides of the back half of the cone wall a narrow, and horizontally oriented fissure was drilled. Plastic holders for the fish body were placed a few centimetres from the back opening of the cone.

The force transducer was made up of full Wheatstone bridge composed of four semiconductor strain gages (resistance in ohms: 500.0±0.3%), bonded on a specially designed cantilever. A full Wheatstone bridge equipped with terminals for connection of wires leading to the connector /4-6/ was mounted in a tool made of Plexy Glass. The tool was fixed into the narrow horizontally orientated fissure of the apparatus framework cone. Horizontal orientation of the cantilever was changed by the arm of the tool and adapted to a fish gill. Horizontal force induced by a fish gill caused an elastic deformation of the cantilever and thus resulted in a change of the output voltage. The output voltage directly represents the information about a mechanical load applied on the cantilever /7-9/. Tinny wires fixed with the fishing hooks into a fish body insulated on one side and on the other side connected to the amplifier were used for ECG recordings.

The water flow through the fish mouth was recorded by using a commercially available semiconductor Wheatstone bridge pressure transducer (Statham, USA). The transducer was pushed into a fish mouth through the hole at the front part of the cone. Signals from the transducers were amplified (D. Peterec, SLO) and connected to the A/D converter (Axon instruments, USA) and an IBM compatible PC. The data were processed with the software *Axoscope* 3.1 freely available on the Internet. The experiments on fish were provided in fresh oxygenated water cooled to 15°C.

3. Results and Discussion

In our experiment we had no trouble in positioning of a fish into the cone of our apparatus as fish simply swam into the cone so that fixation was unnecessary (Fig.1).

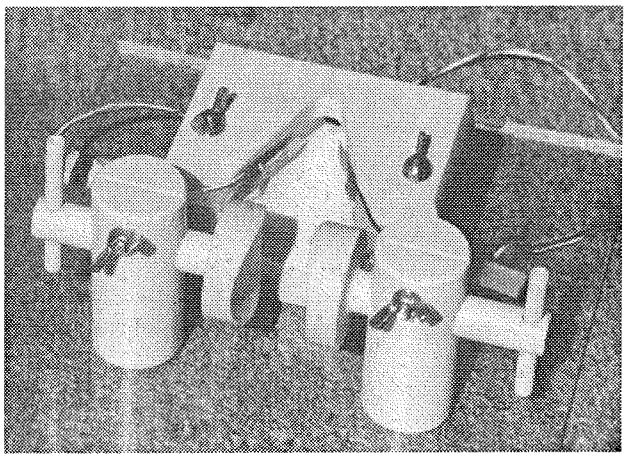

Fig.1. Experimental apparatus. The fish is placed into the equipment so that its movements are restricted, but not completely prevented. On the front side a flow transducer is placed into the fish mouth. One mechano-electrical transducer is placed on each side of the apparatus in order to measure the gill movements.

Nevertheless, we restricted the fish movements gently by the adaptable holders attached on each side. Introduction of the pressure transducer into a fish mouth and the fixation of the ECG wires were effortless.

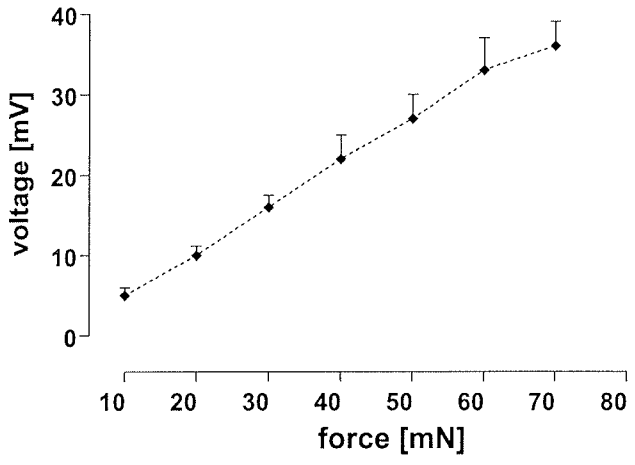

Fig.2. The force transducer has linear voltage response in a range of forces from 0-70 mN

The pair of force transducers has linear dependence of the output voltage upon the load of a gill movements 0.5 mV/mN over the nominal range of 0-70 mN at a bridge excitation of 5V (Fig.2) The linear response of the force transducer could give us the data about the real forces of the gill movement in case the force is calibrated beforehand. A similar transducer was successfully used also for other applications where the contractions of an isolated muscle, rings of pig coronary artery, movement of an animal leg were measured /4-9/.

We obtained reproducible ECG recordings of fish heart beating (Fig. 3). The recordings of the gill movements and those of the water flow pressure through the fish mouth were also reproducible, and enabled the study of correlation of water pressure changes and gill movements.

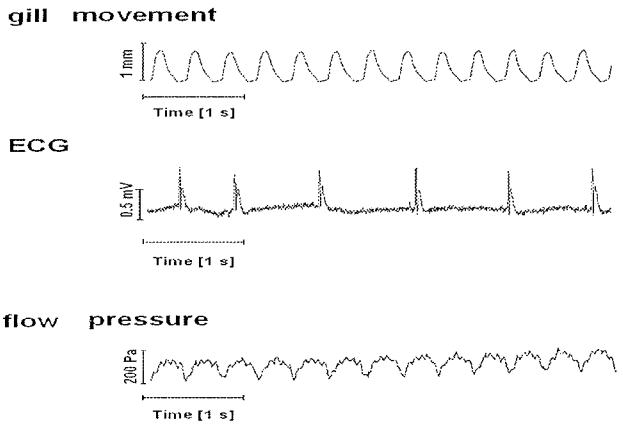

Fig. 3. Experimental data from fish in control conditions. Besides the amplitude of gill movements, the ECG and water flow pressure through the fish mouth can be measured reliably.

The results presented in Fig. 3 suggest that the fish in our experiment was under substantial stress due to its prior exposure to equinatoxin II, a haemolytic toxin that exposed lethal effects in vivo /10-12/. The speed of gill movements was over 100 per minute.

In our experiments we just wanted to demonstrate the measurement characteristics of our equipment. Of course during the experiments with the fish we should take care about lowering the discomfort and stress to a fish that could influence the obtained measurements. The advantage of our equipment is open construction, so different kinds of manipulations with the fish are possible. The fish is quite free and the experimental equipment gives it a more natural environment than some other setups. In the latter cases the treated fish were usually closed in a glass tube of the experimental equipment /1-3/ and far more stress was put on them. Therefore it is difficult to distinguish between the effects of the stress due to the experimental equipment and the effects of the tested substances, in the case of toxicological experiments on fish.

4. Conclusion

According to the presented results we recommend our setup as a simple, inexpensive and suitable tool for *in vivo* experiments on fish even in their natural environment.

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APLIKACIJSKI ČLANEK
APPLICATION ARTICLE

Technology Focus

Small Ceramic Capacitors Address Temperature Compensation Issue

Technical innovations in chip monolithic ceramic capacitors are being accelerated to meet the needs of small and high performance electronics devices. In the area of capacitors for temperature compensation, small-sized and high capacitance capacitors have been developed. These products are now used in markets that were previously monopolized by film capacitors as they can now compete with film capacitors in terms of performance and cost.

This article discusses the technology for high capacitance capacitors for temperature compensation, which maintain the high frequency and high reliability characteristics of monolithic ceramic capacitors, and which use dielectric materials with excellent temperature and voltage characteristics.

Ceramic Capacitor for Temperature Compensation

Monolithic ceramic capacitors are classified into two classes – those for temperature compensation (class I) and high dielectric constant products (class II) – according to the materials used (Fig. 1). High dielectric constant products use as their main material ferrodielectric material represented mainly by barium titanate, and are characterized by a dielectric constant of 1,000 or more. These capacitors are available as small-sized high capacitance products and are extensively used in ordinary electronic devices for bypass,

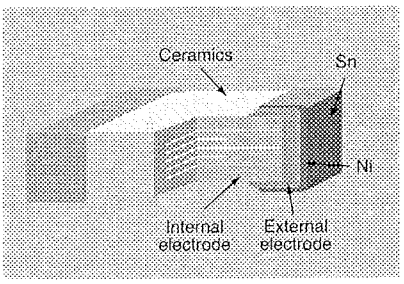
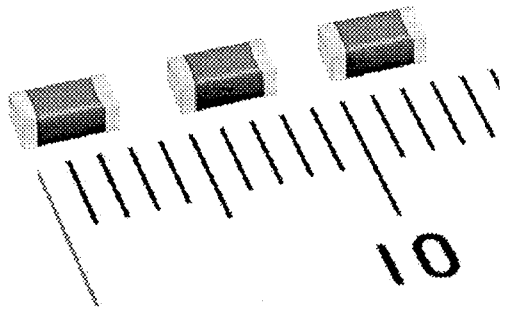


Fig. 1: Structural diagram of monolithic ceramic capacitor



High capacitance temperature compensation capacitors

coupling and decoupling uses. On the other hand, their shortcoming is that their change in capacitance due to temperature is relatively large and that their capacitance and dielectric loss also change to a great extent when DC or AC current passes through them.

In contrast to high dielectric constant type capacitors, those for temperature compensation whose specific dielectric constant is relatively small use electrically stable paraelectric material. Paraelectric material is limited in temperature and voltage dependence and their dielectric loss is very small at 0.05 percent. Viewed from the standpoint of electric characteristics, it may be said that they are close to an ideal temperature compensation capacitor. With a low loss characteristic, temperature compensation capacitors have been used widely for oscillation, tuning, filter and other circuits.

Higher Capacitance Products

Temperature compensation capacitors can obtain a lower capacitance because of their low specific dielectric constant compared with high dielectric constant type capacitors. Thus, according to conventional technology, the highest capacitance that can be obtained from a 1206 size product is low at 0.01μF, so that it needs size reduction and increase in capacitance to meet current market needs.

On the other hand, the shortcomings of high dielectric constant type capacitors is that they generate shock noise because of their piezoelectric characteristic and has an effect on passing signals to distort them. Because of these characteristic defects, there is a restriction on expanding their market.

To solve this problem, Murata Manufacturing Co., Ltd. pioneered in the industry in introducing to the market a high capacitance series of temperature compensation capacitors. Thus, in May 2002, the company introduced a series with a C0G characteristic – 1) 1206/0.1μF/25V – and in November of the same year another series with a U2J characteristic -- 2) 1206/0.1μF/50V.

Particularly, the U2J characteristic products represented a series made smaller and lower in cost than the C0G characteristic series, reducing the number of layers of dielectric devices by designing materials higher in specific dielectric constant, compared with the C0G series.

In developing these series, thin multilayer, super-fine powder, and high distribution technologies for already marketed high dielectric constant type capacitor were used. At the same time, the development of these series represented an expanded use of base metal (nickel) to internal electrodes -- the previous use of precious metal for internal electrodes was impossible for a marketable product because of its high cost.

1) C0G:-55°C~+125°C 0+/-30ppm/°C
2) U2J:-55°C~85°C -750+/-120ppm/°C

Temperature Compensation Capacitors

Capacitors of this type, which use paraelectric ceramic material, are excellent in capacitance-temperature characteristic and distortion, and suffer little change in capacitance after application of DC bias voltage, exhibiting stable voltage dependence.

In the following, general-purpose high dielectric constant type capacitors, C0G

characteristic temperature compensation capacitors, U2J characteristic temperature compensation capacitors and chip type film capacitors are compared as to their representative electric characteristics.

I. Lock-Up Time (LUT)

The results of comparison among the LUT levels of the loop filters for PLLs (Phase Locked Loops) for VCOs (Voltage-Controlled Oscillators) -- filters mounted with different types of capacitors, respectively, are illustrated (Fig. 1).

The LUT is one of the important operating characteristics of PLL circuits, and the shorter the LUT is, the better the modulation precision of a set is, so that a short LUT contributes to faster channel switchover time. There is no difference among them in C0G or U2J characteristics. This is due to the fact that the loss (ESR) of temperature compensation capacitors is very small and that they depend very little on voltage (Figs. 2 and 3).

Capacitors of this type are most suitable for mobile phones and tuners that use PLL circuits.

Table 1: Comparison of LUT

Capacitance: 0.01μF
Output frequencies: 1,742MHz to 1,769.5MHz

	LUT
MLCC U2J characteristic product	1.1ms
MLCC C0G characteristic product	1.1ms
Film capacitor	1.4ms
MLCC X7R characteristic product	6.0ms

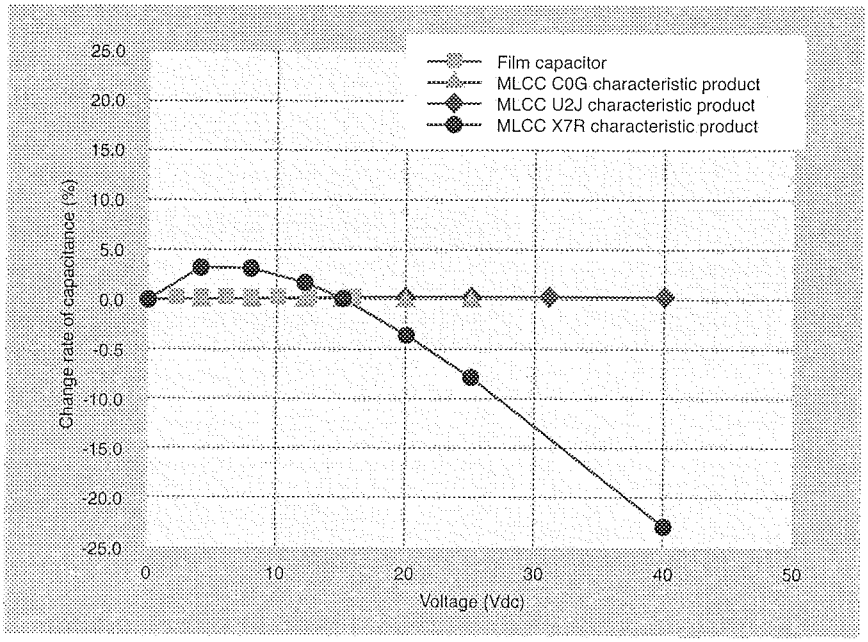


Fig. 3: DC bias characteristic (Tester: HP4284A, measuring condition: 1kHz, 1.0Vrms, 60sec)

II. Shock Noise

For filter, oscillation and other circuits, it is important that no malfunctions occur that are caused by external mechanical shocks or vibration. The results of a comparison under the test conditions mentioned below showed that shock noise caused in C0G/U2J characteristic temperature compensation capacitors are less than the normally acceptable level. This means they have excellent anti-shock noise characteristics.

This is because temperature compensation types use paraelectric material and do not have a piezoelectric characteristic such as seen in high dielectric type capacitors (Fig. 4). Temperature compensation types are particularly suitable for the preamplifier circuits of audio systems that process very small signals and are liable to be affected by shock noise and also for car electronics, which are liable to be exposed to vibration during startup and when the car is running.

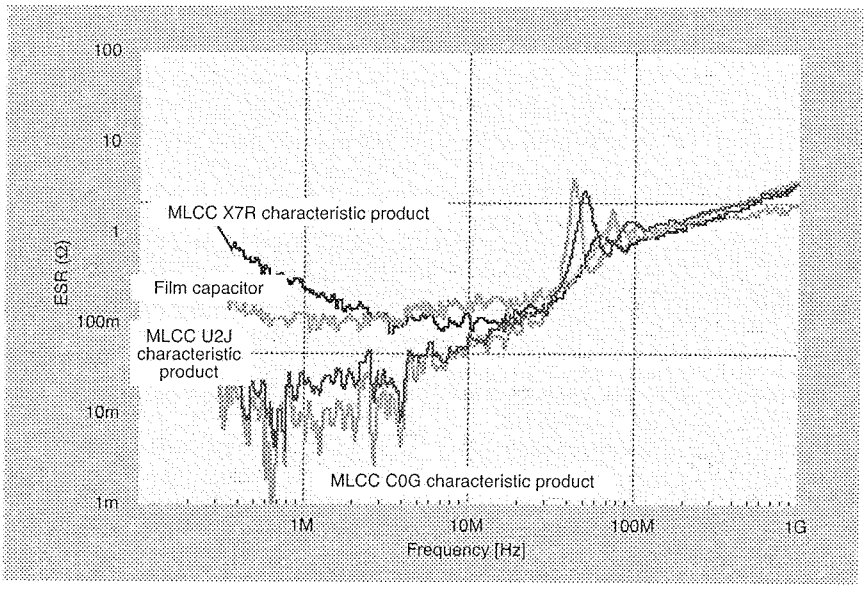


Fig. 2: ESR (Tester: HP8753D)

III. 3rd Harmonic Distortion

The 3rd harmonic distortion means an index of distortion given passing signals in audio and other systems. Illustrated here are the results of comparison of the occurrence rate of 3rd harmonic components (30kHz) in case a reference signal voltage of 10kHz is applied. It may be said that the lower the distortion rate is, the smaller is the effect on signal waveforms. In this respect, too, temperature compensation types excel the other types. This shows their differences in dielectric loss and voltage dependence (Fig. 5).

This type of capacitors is most suitable for audio circuits, which are especially important because of their effect on sound quality. As explained earlier, high capacitance temperature compensation types are excellent in capacitance stability and response, and can be used sufficiently for the circuits for which film capacitors were previously used.

Furthermore, chip film capacitors, which use organic film as their dielectric material, are not characteristically resistant to heat, whereas it is an important characteristic of chip monolithic capacitors that they are highly resistant to heat. Particularly, because of environmental conservation considerations, lead-free devices that require high soldering temperature were introduced. Ceramic capacitors can respond to a demand for high soldering temperature for electronic devices.

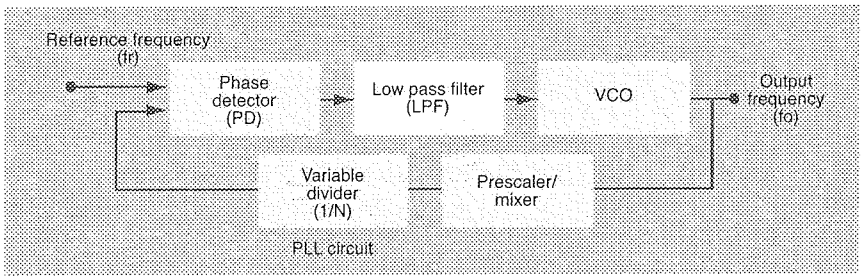


Fig. 6: Application to loop filters

Circuits Used

The following are the main applications of high capacitance temperature compensation type: Loop filters of PLL circuits of VCOs (Voltage Controlled Oscillators); Preamplifier circuits, tone control circuits and coupling circuits of audio systems; Integrating circuits; Peak hold circuits; Filter circuits; Resonance capacitors in inverter circuits for backlights; and Snubber circuits for power supplies.

These devices are extensively used for ordinary electronic equipment, including mobile phones, tuners, audio systems, panel systems and communication modems, and the market for these applications is expected to grow steadily in the future. At present, capacitors of this type are being adopted for the PLL circuits of mobile phones and equipment using LCD panels.

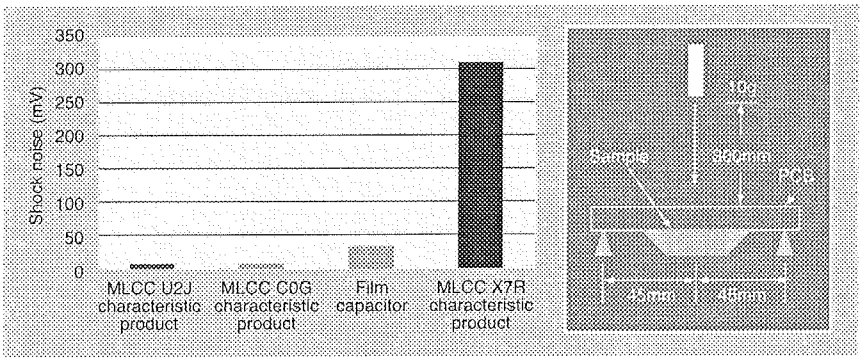


Fig. 4: Shock noise comparison (when 50Vdc is impressed)

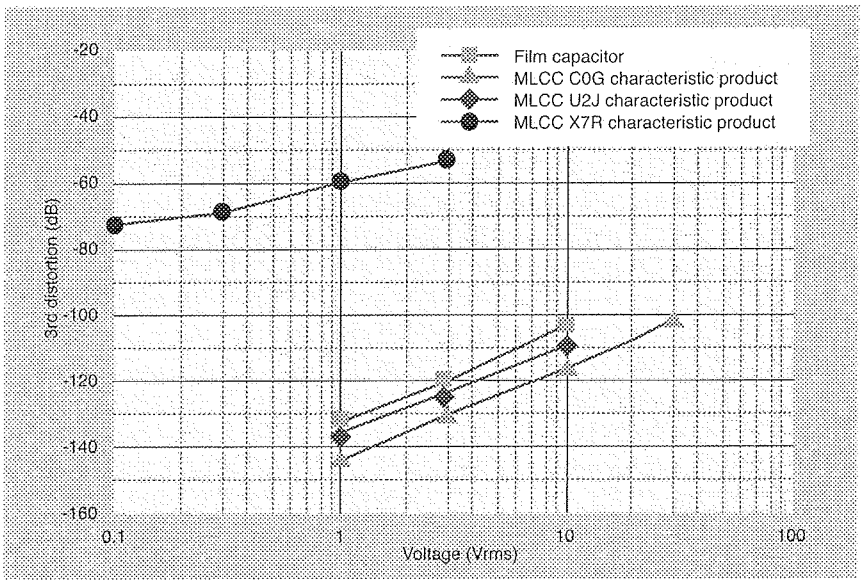


Fig. 5: Measurement results of 3rd harmonic distortion
Tester: CLT-1 (manufactured by Radio Meter, measurement conditions: 10kHz, 1.0Vrms)

Line-Up of Products (only maximum capacitance levels are shown)

U2J characteristic products

- GRM1887U1H103JA01 0603 size/0.01μF/50V
- GRM21B7U1H473JA01 0805 size/0.047μF/50V
- GRM31M7U1H104JA01 1206 size /0.1μF/50V

C0G characteristic products

- GRM1885C1H272JA01 0603 size/0.0027μF/50V
- GRM21B5C1H223JA01 0805 size/0.022μF/50V
- GRM31C5C1E104JA01 1206 size/0.1μF/25V

Electronic systems will tend toward high speed and high frequency in the future as is seen in telecommunication circuits. This is due to the fact that, together with the development of near-next-generation communication networks such as Bluetooth, FTTH (Fiber-To-The-Home), FWA (Fixed Wireless Access) and other networks, communication-information systems are increasingly required to process higher speed signals. In this situation, there will be an increased market need for capacitors that have more excellent capacitance stability and high-speed response.

Murata Manufacturing Co., Ltd. will endeavor to develop products that meet market needs by developing new materials and utilizing more advanced production technologies.

About This Article

The author, Hiroki Muto, works at the Technical Administration Section, Technical Administration Department of Fukui Murata Manufacturing Co., Ltd.

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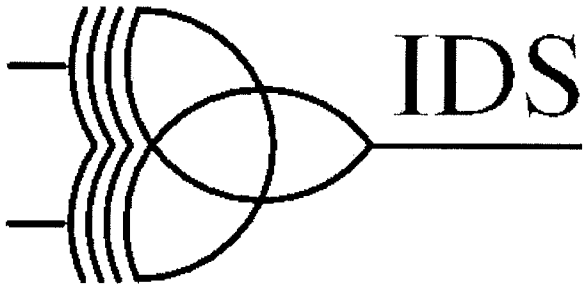

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IDS is a fabless semiconductor company providing ASSPs, ASICs, IPs and design services for specific wireless, sensor and isolation applications.

IDS is a privately owned company with headquarters in Ljubljana in Slovenia and sales offices in Europe and North America.

IDS is a dynamic company providing customers with ASSPs, ASICs, design services and complete turn-key system solutions based on our extensive IP and patents in wireless, sensor and isolation applications.

IDS started as an ASIC/ASSP design center in 1996 and in 2002 our strategy was extended to become a fabless semiconductor company.

IDS is constantly extending its portfolio to include competitive silicon system solutions fulfilling modern market demands.

IDS has build a custom CAD system supporting analog and mixed analog-digital design with interfaces to wafer fabs and industry standard tools (e.g. Cadence™).

IDS provides customers with design services and complete turn-key solutions to many electronic and electro-mechanical system design requirements. IDS has successfully participated in the development of a wide variety of ICs for telecommunication, measurement, contactless identification and automotive applications.

Your Partner in Analog and Mixed Signal silicon systems

We excel in analog and mixed analog-digital system solutions. With our experience and comprehensive IP library, IDS enable our customers to become most competitive in targeted applications by providing innovative, cost-efficient, turn-key and on-time solutions.

Texas Instruments as one of the world leaders in semiconductor business uses IDS patented technology in its products.

IP Library:

- High voltage generation ASIC
- High voltage cells for flash memories and EEPROM
- 12 bit flash ADC
- Sigma/delta converters in systems
- Fast receiver/transmitter twisted pair in BiCMOS (640MHz)
- *High bandwidth amplifiers*

Wireless IPs:

- Tag IC for frequency range 400MHz to 2.5GHz
- Tag ICs 13.56MHz
- Reader ICs 125/133 kHz RFID
- *Reader IC for 13.56 MHz RFID*

Sensor IPs:

- Integrated Hall devices
- External magneto resistive sensors
- Optical position encoder
- Integrated photo diodes
- External photo sensors
- Analog front end for x-ray scanning equipment
- Absolute capacitive angle/linear measurement system
- Capacitive proximity sensor/switch
- Programmable encoder
- Precision encoder with programmable IF
- Universal analog front-end for optical signal processing
- Re-timer/line driver IC
- *Temperature sensor IC*

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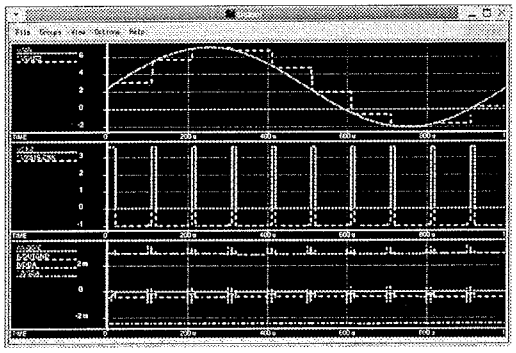

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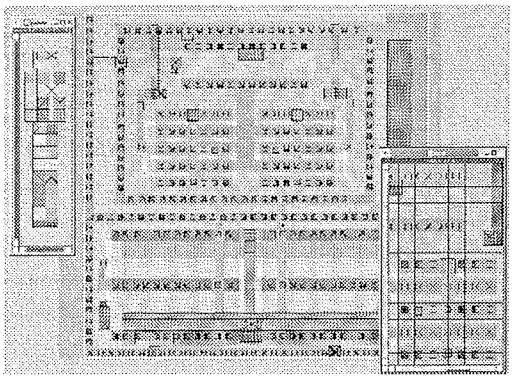

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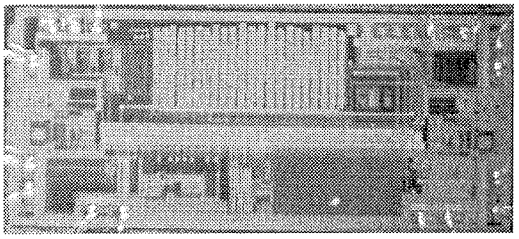
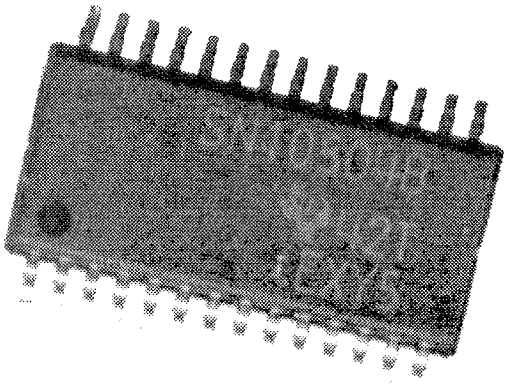
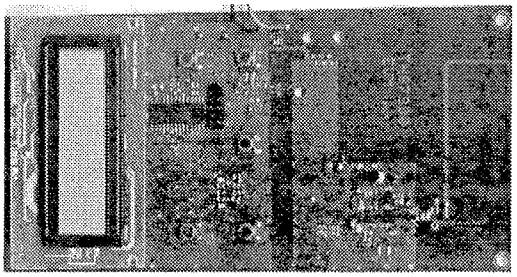






NOVICE NEWS

IR to bring 200mm on-line in Wales

INTERNATIONAL RECTIFIER (IR) plans to invest $40mn to bring on-line 200mm facilities and double production capacity at its site in Newport, Wales. International Rectifier's planned investment of $40mn in IR-Newport will result in more than 120 additional jobs and the potential to quadruple the facility's production capability in the future.

Many of the newly created jobs will be devoted to the company's latest high voltage 1C (HVIC) proprietary technology. Newport previously produced leading-edge low voltage devices on a 150mm wafer line. The new HVIC silicon can be used in integrated motor controllers for a variety of industrial, appliance and automotive applications.

Since the site's acquisition from the liquidation of European Semiconductor Manufacturing (ESM), IR has invested more than $66mn to expand production capabilities and has increased the staff by more than 100.

The site also included areas in which 200mm production had been planned by its previous owners.

International Rectifier acquired the Newport facility in 2002. Work since then has included consolidation of IR's low voltage trench product line, the doubling of Newport's initial production capacity and support for IR's low voltage R&D programme.

New record year?

The US Semiconductor Industry Association (SIA) has revised its predictions with a compound annual growth rate (CAGR) of 10.4% through to 2007. This year is expected to be above average at 28.6% resulting in world IC sales of $214bn. This beats the $204bn sales of the previous record year, 2000. Next year, growth is expected to be 4.2% and in 2006 sales are expected to fall by 0.8%. The year 2007 is expected to show a rebound to 11.7% growth with sales reaching $250bn.

"While this [compound] growth rate is lower than the historical growth rate of the past several decades, it represents very healthy growth for a $200bn-plus industry," comments SIA president George Scalise. Regional market share for IC consumption is expected to reflect further moves to Asia Pacific, going from 40% now to 43% by 2007. The Americas is expected to lose share, going from 19% to 17%. Europe is expected to have a steady 20% share over the period. Japan is also forecast to maintain its IC consumption at 22%.

Germany joins organic solar cell hunt

The German Federal Ministry for the Environment, Nature Conservation and Nuclear Safety (BMU) will fund a joint research project on organic solar cells by Germany's Hahn-Meitner-Institute (HMI), chemicals supplier Covion Organic Semiconductors and Aixtron. Within this project AIXTRON will install an organic vapour phase deposition (OVPD) system at the HMI for the deposition of organic thin films.

Organic materials appear to be promising for application in low cost thin film solar cells. While conversion efficiencies do not match silicon, it is hoped that the processing required will be lower cost. First samples have achieved conversion efficiencies of more than 5%. In the mid-to-long term the researchers hope that organic solar cells will achieve efficiencies even higher than Si thin film cells. A further advantage is that the materials can be more eco friendly.

Aixtron has an exclusive licensing agreement and a joint development programme with Universal Display (UDC) in the USA. Aixtron has developed a low cost, high-throughput process, for high-end device mass production of high resolution full-colour organic light emitting diode (OLED) displays and other products.

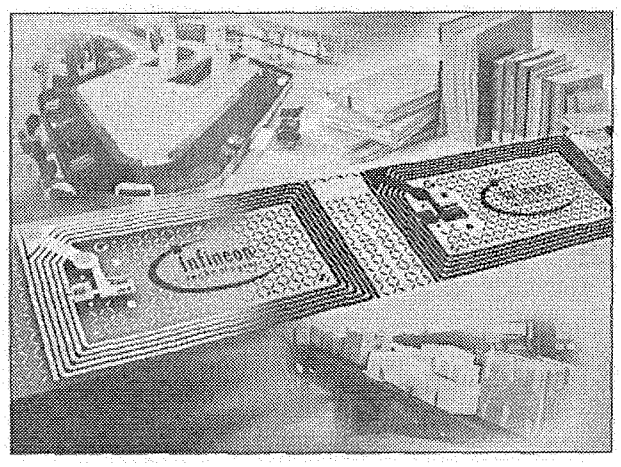
Seeking RFID excellence

INFINEON TECHNOLOGIES added a radio frequency identification (RFID) chip solution excellence centre and system lab to its facility in Graz, Austria. Of the 140 employees at the site, around 40 will work in RFID. The company is developing a range of RFIDs including smart label technology, where an RFID chip and antenna are integrated into paper or plastic.

The company is also developing a system platform for smart label readers to integrate RFID logistics into a company's operations, and services for development, rollout and maintenance of logistics systems. Applications in the automotive and textile industries are foreseen.

Developers in Graz have already developed an integrated RFID system platform called the You-R OPEN (OPerating ENvironment). This is an operating system environment that links a company's existing logistics IT infrastructure to RFID applications. You-R OPEN supports applications from smart labels to readers, PC and servers, and links to IT networks.

The technology supports J2EE, Microsoft .net, http, C++, XMLor PML programming and standard development tools.



The RFID system lab performs four separate tasks - application demonstrations, development and verification, technology evaluation and training.

Depending on the sector and task, a variety of different RFID technologies can be employed in logistics processes. A distinction is made between ultra high frequency (UHF), in the frequency band around 900MHz, and high frequency (HF) systems at 13.56MHz.

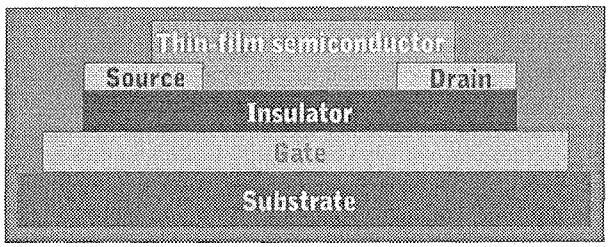
UHF systems allow ranges of 3-4m. Technologies operating at 13.56MHz have a shorter read range. Infineon's 13.56MHz systems implement phase jitter modulation (PJM) that supports reading of labelled objects as they pass a reader unit at high speed on conveyor belts.

Nippy spin-on semi films

SCIENTISTS at IBM's TJ Watson Research Center have developed a high-mobility ultrathin semiconducting film prepared by spin coating (Nature, March 18, 2004). The technique promises simple, low-cost products. The researchers have boosted electron mobilities by about 10 times over that reported for similar approaches.

The new approach spin coats a 50A thick layer of crystalline and continuous metal chalcogenide films. Chalcogens are the four chemical elements -oxygen, sulphur, selenium and tellurium - that reside in the sixth column of the Periodic Table. The term is derived from two Greek words meaning "ore formers". Some metal chalcogenides - such as cadmium sulphide, tin selenide and zinc telluride - are high-performance semiconductors.

The spin-coat deposition is based on the low-temperature decomposition of highly soluble hydrazinium precursors. Hydrazine is a molecule made up of two nitrogen and two hydrogen atoms. To dissolve the semiconducting material, the researchers combined a very strong hydrazine solvent with equal numbers of chalcogen atoms and semiconducting metal chalcogenide molecules such as sulphur and tin sulphide. While hydrazine is generally not a good solvent for metal chalcogenides, the presence of the extra chalcogen atoms both improves solubility and enables control over the film composition and grain structure.



Thin-film transistor structure films.

Heating the resulting film causes both the hydrazine and extra sulphur to dissociate and evaporate, leaving just a very thin layer of solid metal chalcogenide with a uniform thickness as small as 5nm. When the team optimised the molecular proportions, spin-coating conditions and heat/annealing procedures, the films exhibited charge mobilities approaching that of polycrystalline silicon and 10 times that of any previously spin-coated material or amorphous silicon.

The team also made thin-film field effect transistors based on semiconducting $SnS_{2-x}Se_x$

These layers exhibit n-type transport with current densities of more than $10^5 A/cm^2$. Mobilities exceed $10cm^2/V/s$.

The spin coating technique is expected to apply to a range of metal chalcogenides -particularly those based on main-group metals. Applications for solution-processed electronics include advanced displays, flexible devices, smartcards, RFID tags, photovoltaic solar cells, thermoelectrics and phase-change solid-state memories.

A spin-coated film's thickness is usually determined by the solution's viscosity (its resistance to flow) and the rate and duration of spinning. The liquid is then cured into a solid thin film upon which transistors and other various electronic devices can be made.

The next step for the researchers is to reduce or replace the use of hydrazine, a highly energetic molecule also used as rocket fuel, with a more benign but still effective solvent.

Until now, the only semiconducting materials that could be made using spin coating had limited usefulness due to low charge mobility. Better semiconductors could not be dissolved in any liquid that would result in a thin film that retained the desired mobility.

IBM researchers believe the new technique will accelerate progress to widespread use of thin-film electronics produced using fast, inexpensive, high-throughput solution

processes such as spin coating, printing, stamping, nanoimprinting, InkJet printing and dipping.

STMicroelectronics, CEA-Leti and AIXTRON Develop Ultra-Thin Gate-Insulation Process for Advanced CMOS Transistors

Industry first as ST and CEA-Leti joint development research program demonstrates excellent results for new advanced process technology

Geneva, May 26, 2004 - STMicroelectronics (NYSE: STM) today announced that ST, CEA-Leti and AIXTRON have developed an advanced process technology for the creation of ultra-thin transistor-gate-insulation layers for low-power applications at the 65nm and 45nm CMOS transistor technology nodes. The new process significantly reduces transistor leakage current by the deposition of 'high-k' gate-insulation material.

To meet the future requirements of highly integrated devices postulated by Moore's law and described via the International Technology Roadmap for Semiconductors (ITRS), it will eventually be necessary to introduce new materials into the manufacture of advanced silicon devices. The three companies are developing new process technology aimed at the 45nm or 65nm technology nodes for low-power CMOS platforms optimized for portable applications.

Based on AIXTRON's Tricent® reactor technology, CEA-Leti and ST have created a joint development program for 'high-k' materials, fulfilling the specifications of advanced nano-metric CMOS gate-stacks that require a thick physical layer with a low leakage current equivalent to ultra-thin oxide.

The process, called AVD® (Atomic Vapor Deposition), has demonstrated excellent Equivalent Oxide Thickness (EOT) values of 1.15nm or 11.5Å (Angstroms) based on hafnium dioxide / silicon dioxide / silicon (HfO2/SiO2/Si) stacks offering leakage current densities as low as $JL=6.8x10^{-2}A/cm^2$ at 1.5V.

The results were obtained by the Advanced Modules team of researchers from ST and CEA-Leti at ST's Crolles facility using a Tricent AIXTRON 200/300 mm bridge cluster tool. The HfO2 deposited layer process was developed in conjunction with AIXTRON, and the wafer processing and the characterization were performed at CEA-LETI facilities in Grenoble.

Metallic oxides of the hafnium family are believed to be excellent candidates for the 'high-k' dielectric material that will eventually replace silicon dioxide in the basic CMOS transistor structure.

In addition to the ability to precisely deposit thin dielectric 'high-k' layers, the AVD technique also allows the deposition of metal gates necessary for the 45nm-and-below CMOS technology nodes.

"These proof-of-concept results are a first for this process technology," said Daniel Bensahel, Project Leader and Front-End Program Director at STMicroelectronics. "This joint development program between ST and CEA-Leti, in conjunction with AIXTRON, is not only the first in the industry to implement this advanced process in an industrial environment; but more importantly, it is also achieving excellent results."

"The co-operation with STMicroelectronics and CEA-Leti is an integral part of our strategic CMOS development effort strengthening AIXTRON's position in emerging semiconductor applications. By working with one of the leading semiconductor device manufacturers and one of the top research organizations in the industry, AIXTRON will remain at the forefront of cutting edge enabling MOCVD process technology development. We have been highly impressed by the professionalism and the technical competencies of the STMicroelectronics and CEA-Leti team, and look forward to combining our expertise to develop solutions for advanced CMOS devices," said Tim McEntee, Executive Vice President and COO Semiconductor Equipment/ AIXTRON AG.

About AIXTRON

AIXTRON (Aachen, Germany) is, as verified by an independent market research institute, the world leading supplier of equipment for III-V semiconductor epitaxy. Its equipment is used by a diverse range of customers worldwide to manufacture critical, advanced components such as HBTs, PHEMTs, MESFETs, Lasers, LEDs, Detectors and VCSELs used in fiber optic communications systems, wireless and mobile telephony applications, optical storage devices, illumination, signaling and lighting, as well as a range of other leading edge technologies. Originally focusing on compound semiconductor applications over the last years AIXTRON has broadened its product portfolio to enabling MOCVD Technologies for advanced materials for next generations of mainstream semiconductor devices and Organic LED applications. To date, AIXTRON's total installed base of systems exceeds 800 tools worldwide. AIXTRON AG (FSE: AIX ISIN DE0005066203) is listed in the Prime Standard and Tec DAX of the German Stock Exchange (Deutsche Börse) and is included in the MSCI World Index.

About CEA-Leti

CEA-Leti (Grenoble, France) is a CEA Grenoble laboratory at the leading edge of European microelectronics and microtechnologies research. It employs about 800 people and with its more than 120 patents filed per year and its 30 start-ups created or being created, it ranks among the major partners of the industrial world. CEA is a polyvalent scientific and technological research organization, specialized in the fields of nuclear power, both civil and

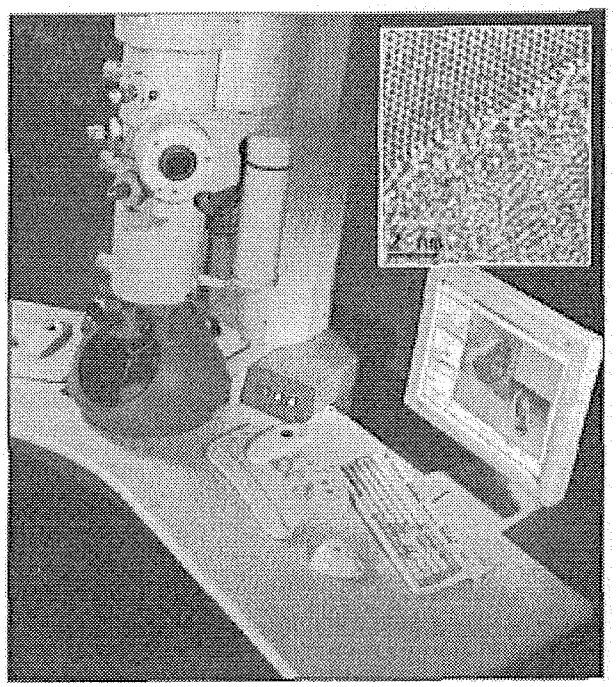
military, new energy technologies, information and communication systems and biotechnologies. Its ability to combine fundamental research and valorization in an industrial framework enables it to play a leading role in innovation. Some 16,000 people are employed at CEA in 10 sites in France.

About STMicroelectronics

STMicroelectronics is a global leader in developing and delivering semiconductor solutions across the spectrum of microelectronics applications. An unrivalled combination of silicon and system expertise, manufacturing strength, Intellectual Property (IP) portfolio and strategic partners positions the Company at the forefront of System-on-Chip (SoC) technology and its products play a key role in enabling today's convergence markets. The Company shares are traded on the New York Stock Exchange, on Euronext Paris and on the Milan Stock Exchange. In 2003, the Company net revenues were $7.24 billion and net earnings were $253 million. Further information on ST can be found at www.st.com.

Sub-Angstrom electron imaging

FEI's nanotechnology scientists have broken the 1A (0.1nm) image resolution barrier with a 200kV transmission electron microscope (TEM). FEI believes that this is the first time that images have been viewed directly with a resolution of less than 1A using commercially available technologies. This resolution is approximately one-third the size of a carbon atom - a key dimension for atomic level research.



The Tecnai F20 ST tool with (inset) an image of a silicon transistor gate interface

The sub-A resolution was achieved using FEI's Tecnai F20 ST transmission electron microscope, using advanced electron optics capabilities developed by FEI and its partner, Corrected Electron Optical Systems (CEOS) of Heidelberg, Germany. CEOS develops correction for high-resolution electron microscopy and provided spherical aberration correction (Cs-correction) for the 200kV TEM equipment. The Cs-corrector uses hexapoles with additional round lenses. FEI developed an e-beam gun monochromator to further improve the resolution.

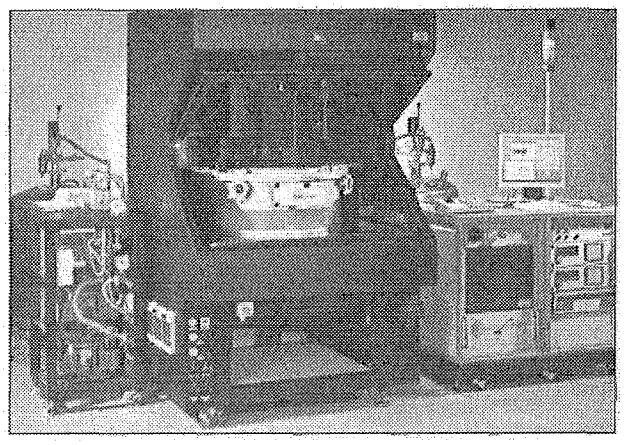
Dr Michael O'Keefe of the US National Center of Electron Microscopy in Berkeley, California, comments: "Theory has long predicted that a monochromator would be able to push the resolution of the super-twin lens beyond the 1.4A resolution demonstrated with Cs-correction alone. However, the difficulties involved in implementation of a monochromator without compromising the imaging qualities of the electron beam are well known. FEI deserves to be congratulated for this outstanding achievement."

Professor Dr Hannes Lichte of Dresden University in Germany, also comments on the scientists' achievement: "As evident from their diffractograms, they are not far off the theoretical limit of about 0.07nm in at least some directions. Congratulations!"

Very cool probing

SUSS MicroTec claims installation of the world's first 300mm semiautomatic cryogenic probe system capable of DC testing down to 100 femtoA at temperatures from 400 K (127°C) down to 30K (-243°C) at a "leading semiconductor manufacturer".

The customer will use the PAC200/300 system for materials research and device characterisation of next generation ICs including new superconductive devices. Although it has been designed to test 300mm wafers, the tool can also test 200mm wafers and smaller substrates.



SUSS-designed carriers with a special wafer fixing mechanism ensure an optimal thermal contact between the heat exchanger/chuck and the wafer without using any contact

grease in between. This mechanism is designed to avoid use of contact grease as this can contaminate the device under test (OUT) and works as an electrical isolator.

Using either liquid nitrogen or liquid helium (depending on the temperature range required), the prober has two separate cooling cycles (one for the specially designed triaxial cryo chuck and one for the cryogenic shield).

Running the two cycles simultaneously speeds up cooling.

German production line for ZigBee CMOS

The Fraunhofer Institute for Microelectronic Circuits and Systems (IMS) organisation in Germany has set up a CMOS production line in Duisburg for the ZigBee wireless standard. Fraunhofer argues that the bandwidth offered by alternative standards such as Bluetooth exceed what many devices need while the power consumption is also often more than necessary.

ZigBee primarily uses the same frequency ranges as Bluetooth but delivers a lower maximum data rate of 250kbits/sec that is adequate to the needs of devices such as sensors in weather stations and medical equipment, security systems, light switches, wireless computer mice or monitoring systems in industry. While ZigBee's data rate is 10-25% that of Bluetooth, depending on frequency, batteries can last anywhere from a few months to several years, depending on data traffic and range. When the device has nothing to do it goes into an energy-conserving hibernation mode.

The IEEE has established the 802.15 WPAN Task Group 4 to address the ZigBee standard. Firms like Honeywell, Invensys, Mitsubishi, Motorola and Philips have been building 802.15 devices since last year. Series production is set to start in 2004.