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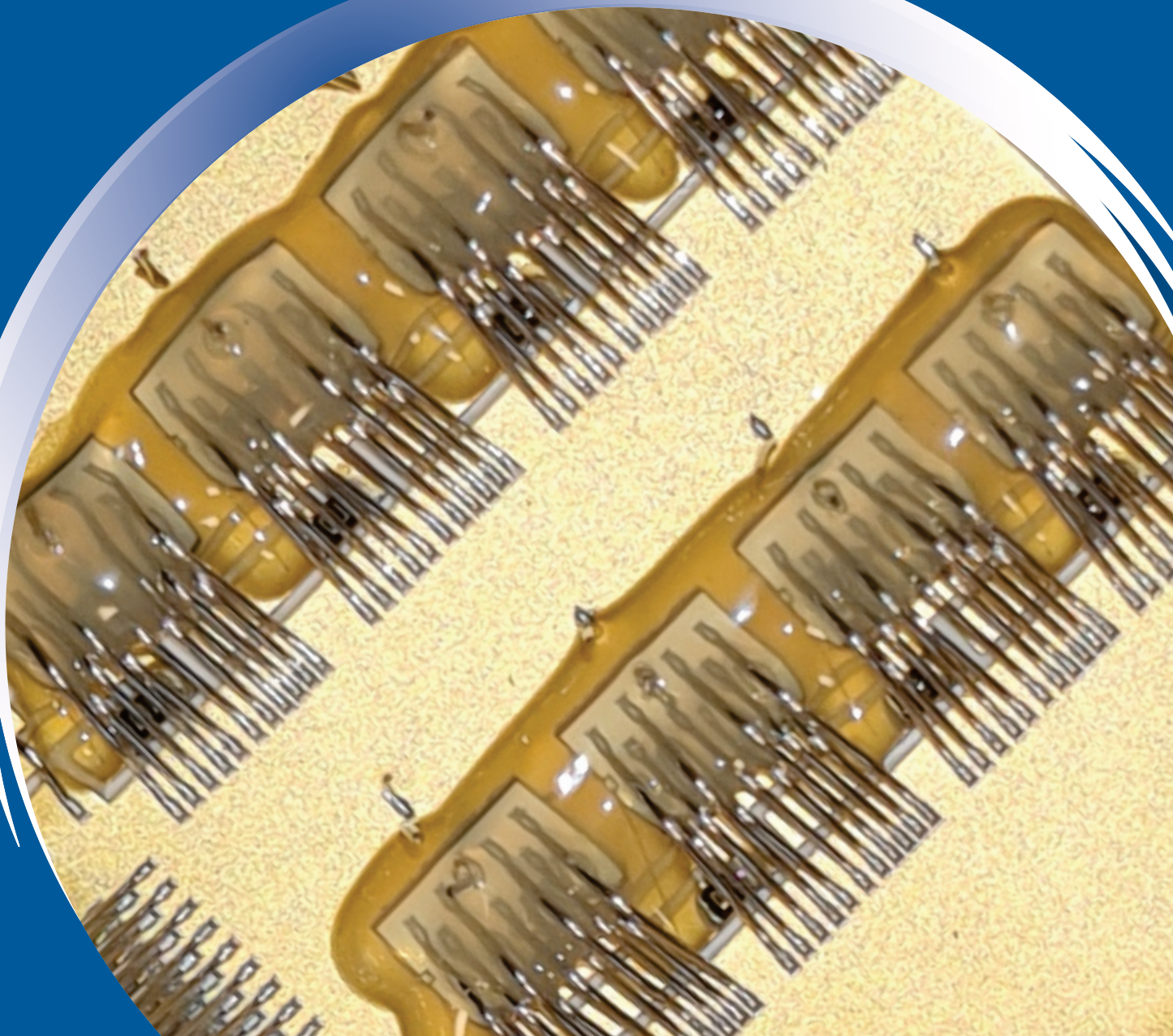

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Simulations of Mode Division Multiplexed Free Space Optics with Photonics Traversal Filter using Multi-Mode Fiber

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Abstract: The ever-increasing demands for ubiquitous connectivity for faster high-capacity communication systems has driven the quest for sixth-generation(6G) communication systems. It is expected to address the need for higher capacity, lower latency systems with higher Quality of Service (QoS) than fifth-generation 5G communication systems. Aerial Access Networks (AANs) have attracted attention and are considered as a potential solution for 6G systems. Heterogeneous networks with fiber and Free Space Optics (FSO). FSO front haul architecture is expected to meet the demands for the low-cost deployment of 6G networks. However, an increase in transmission capacity of FSO by mode division multiplexing to meet the needs for 6G communication has been least explored. Improvements in fiber multiplexing and demultiplexing techniques have enabled the possibilities for novel Mode Division Multiplexing (MDM) techniques to improve the capacity of fiber networks at a low cost. In this work, we have discussed the design of a novel photonics traversal filter to perform Mode Division Multiplexing in Multimode Fiber (MMF), thereby increasing the fiber's capacity. The performance of Mode Division Multiplexed FSO links is further examined through simulations to identify its capabilities to meet the demands of 6G communication systems.

Keywords: 6th generation communication systems; Multimode Fiber; Mode Division Multiplexing; Photonics Filter; Multiplexing; Demultiplexing

Simulacije delitve rodov multipleksirane optike prostega prostora z uporabo večrodovnega vlakna

Izvleček: Vedno večje zahteve po vseprisotni povezljivosti za hitrejše komunikacijske sisteme z visoko zmogljivostjo so spodbudile iskanje komunikacijskih sistemov šeste generacije (6G). Pričakuje se, da bo zagotavljal večjo zmogljivostjo, manjšo zakasnitev in višjo kakovostjo storitev (QoS) kot komunikacijski sistemi pete generacije 5G. Kot potencialna rešitev za sisteme 6G se omenja prostorsko dostopna omrežja (Aerial Access Networks - AANs). Heterogena omrežja z optičnimi vlakni in optiko v prostem prostoru (FSO). Pričakuje se, da bo arhitektura FSO izpolnjevala zahteve po nizkocenovnem uvajanju omrežij 6G. Kljub temu je bilo povečanje prenosne zmogljivosti FSO z multipleksiranjem delitve rodov za potrebe komunikacij 6G najmanj raziskano. Izboljšave tehnik multipleksiranja in demultipleksiranja optičnih vlaken so omogočile možnosti za nove tehnike multipleksiranja delitve rodov (MDM) za izboljšanje zmogljivosti optičnih omrežij z nizkimi stroški. V tem članku smo obravnavali zasnovo novega fotonskega potovalnega filtra za izvajanje multipleksiranja delitve rodov v večrodnih vlaknih (MMF) in s tem povečanje zmogljivosti vlaken. Zmogljivosti za izpolnjevanje zahtev komunikacijskih sistemov 6G so bile raziskane s simulacijami.

Ključne besede: 6. generacija komunikacijskih sistemov; večrodna vlakna; milipleksiranje delitve rodov; fotonski filter; multipleksiranje; demultipleksiranje

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1 Introduction

There has been an exponential increase in the amount of data being transferred due to the ease of use of intelligent devices. The number of smartphones is expected to surpass 8 billion by 2022 [1]. The mobile data traffic is expected to increase seven-fold and reach 77.5 Exa-

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bytes per month [2, 3]. The very rapid development of technologies like Artificial Intelligence (AI), Internet of Things (IoT), Virtual Reality (VR) has led to a massive increase in data traffic. It is predicted that the existing communications and network infrastructure would not be sufficient to handle the amount of data expected to be transferred. The fifth-generation communication is currently being deployed and is aimed at providing faster, high-capacity transmission. By 2030, 5G communication would reach its limits, requiring higher capacity systems with lower latency. Artificial Intelligence would play a significant role in 6G networks providing network adaptation and management. [4]. 6G should meet the demands for a fully digital and connected world. 6G networks would have high bitrate, low latency, high energy, spectral efficiency, high Quality of Service (QoS), and high reliability.

FSO is one of the key technologies expected to enable a 6G wireless communication system [5]. Backhaul connectivity should have a high capacity supporting large volumes of traffic. Remote geographic locations, deployment complexities in congested cities have increased the deployment cost of fifth-generation communication systems. Optical Fibers and Free Space Optical Communication Systems (FSO) would meet the demands for 6G communication systems [6, 7]. FSO would support high-capacity connectivity in hard-to-deploy places proving to be an efficient communication technique for front and backhaul. Mode Division Multiplexing has been least explored to increase the capacity of fibers. Mode Division Multiplexing can result in modern, adaptive systems directly combining components like an amplifier for all channels [8]. This paper would discuss the role of FSO in 6G communication and provide multiplexing techniques for reliable high capacity FSO communication debating the challenges and future research to be performed.

Sending signals in strands of glass called fibers is Optical Fiber Communication. The fiber consists of center glass through which photons are guided by a cladding that traps the photons inside the core. Single-Mode Fiber (SMF) has a small core diameter, allowing only one mode of light to propagate. Multimode fibers have a large core diameter which allows multiple ways of light to propagate. Modes of fiber are defined by the Helmholtz equation, an extension of Maxwell's equations which gives Laplacian relation between amplitude and wavenumber. Among various modes in optical fibers, Linearly Polarized modes (LP Modes) are used in Mode Division Multiplexing. LP modes are typically used in graded fibers, LP mode field components in the direction of propagation are small compared to the components perpendicular to the direction of propagation. The transmitter and receiver characteristics of Free Space Optics (FSO) systems are comparable to optical fibers.

We have designed and simulated a novel photonics traversal filter using Multi-Mode Fiber, and the capacity of the channel is increased by using Mode Division Multiplexing (MDM). The use of a single multimode fiber provides space demultiplexing to eliminate optical interference and time delays between filter taps.

2 Mode division multiplexing

Mode Division Multiplexing utilizes multiple modes as different transmission channels within fibers. As a result, mode Division Multiplexing can increase the bandwidth of transmission, and it'san alternate solution to Multi-Core Fiber [9].

2.1 Tunable mode division multiplexing

The block diagram for the tunable multimode fiber for mode division multiplexing is shown in Figure 1.

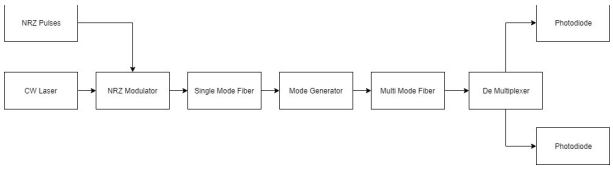


Figure 1: Tunable Multimode Fiber with Mode Division Multiplexing. Tunability of the filter is obtained by changing the incident angle of different beams at MMF.

The input signal is generated using Pseudo-Random Binary Source and encoded with the Non-Return to Zero (NRZ) pulse. The optical carrier signal used here is Continuous Wave Laser(CW laser) which gets modulated with the binary signal using Mach Zehnder modulator (MZM). [10-12]

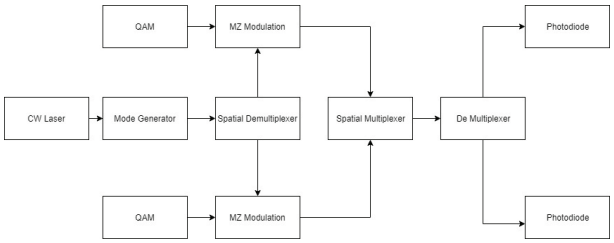
Photonics filter has been used for various RF signal processing tasks [13]. Microwave photonics filter have provided significant improvement in performance when compared to conventional electrical RF filters. Microwave photonics filter provides high bandwidth with low loss and provides increased tunability and flexibility. Our photonics filter is based on a single wavelength multimode optical delay module [14]. The Photonics traversal filter acts as an optical delay line module. An optical carrier of a single wavelength is split into several beams and is incident at the Multi-Mode Fiber (MMF) at different incident angles. As a result, different spatial modes can be excited within the core MMF region, which acts as filter taps. Modal dispersion acts as a time delay between adjacent taps. By changing the incident angle of the light from SMF, the modes can be tuned.

Table 1. Simulation Parameters.

Parameters	Values
Data Rate	10 Gbps
Wavelength used	1550 nm
Laser Power	Ten dBm
Line width	10 MHz
Attenuation (MMF)	1.8 dB/km
PIN Responsivity	1 A/W

The input from the CW laser is fed into the mode generator. For simulation, the mode generator is used as a transversal filter that converts single-mode into multimode. The generated multimode that are orthogonal to each other are multiplexed using MDM. The multiplexed signal is then fed into Multimode fiber. The simulation layout of the tunable multimode optical delay line with MDM is shown in Figure 2. For simulation, spatial Multiplexer is used as Traversal Photonics Filter, which is then fed into MMF. The use of a single multimode fiber provides space demultiplexing to eliminate optical interference and time delays between filter taps using modal dispersion. The delayed signals from the MMF are demultiplexed using a spatial demultiplexer. Finally, the optical signal from the demultiplexer is received by the photodiodes. The simulation parameters are shown in Table 1.

Figure 2: Layout of Tunable Multimode Fiber with



Mode Division Multiplexing

3 Simulation results

3.1 Transmitted modes

The Linearly Polarized (LP) modes, designated as LPlm, are good approximations formed by exact modes TM, TE, EH, and HE. The mode subscripts' l' and 'm' describe the electrical field intensity profile. There are '2l' field maxima along the fiber core circumference and 'm' field maxima along the fiber core radial direction. The LP modes are generated by setting the power ratio parameter in the multimode generator as (1, 2). Similarly, we can generate Laguerre Gaussian (LG) modes and Hermite Gaussian (HG) modes. In this work, two-LP modes, LP (0, 1) and LP (1, 1), have been taken, and their performance in terms of BER and Quality factor is analyzed based on different length parameters.

3.2 Transmitted LP Mode (0, 1):

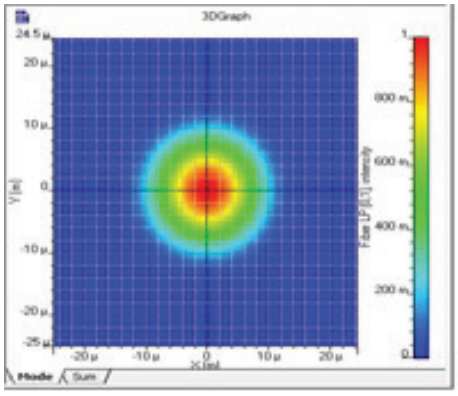


Figure 3: LP (0, 1)

From Figure 3, LP (0, 1) indicates no maxima around the fiber core circumference and single field maxima along the fiber core radial direction.

3.3 Transmitted LP Mode (1, 1):

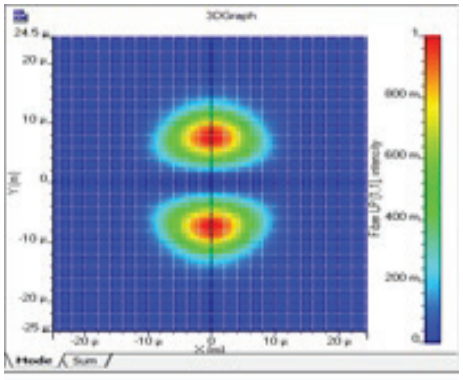


Figure 4: LP (1, 1)

From Figure4, LP (1, 1) indicates two field maxima around the fiber core circumference and single field maxima along the fiber core radial direction. Figure 5 and Figure 6 tells about LP(1,2) and LP(1,3).

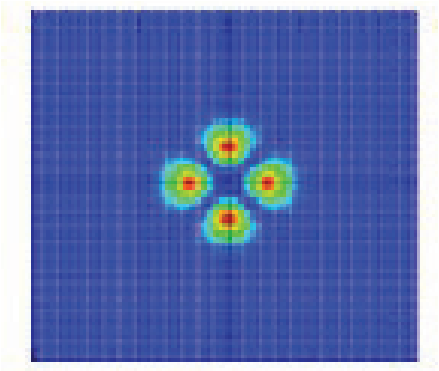


Figure 5: LP (1,2)

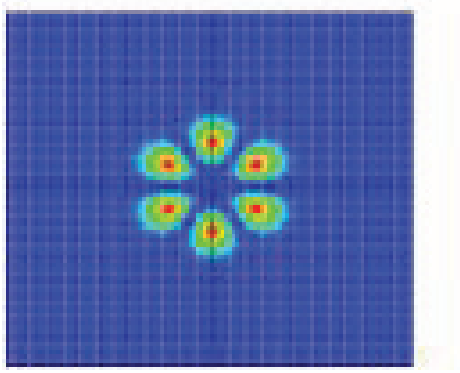


Figure 6: LP (1,3)

3.4 Modes after multiplexing:

The modes LP (0, 1) and LP (1, 1) are multiplexed using Ideal mux. An ideal Multiplexer is equivalent to a perfect adder. There is no power splitting or filtering when in an Ideal Mux. The modes after multiplexing are visualized by using a spatial visualizer. The modes after multiplexing are shown in Figure 7.

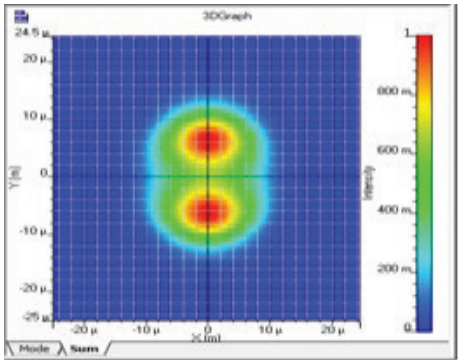


Figure 7: Multiplexed LP (0, 1) and LP (1, 1)

4 Free Space Optics

Free Space Optics uses photonics that propagates through the air like a wireless transmission. Free Space Optics has all the advantages of wireless radio transmission with a high transfer rate and bandwidth. Still, Free Space Optics is limited to short-range communications at a direct line of sight. The basic architecture of Free Space Optical Communication Systems is given in Figure 8.

The modulated Input Pulse is fed into the MZM, which converts the electrical pulses into an equivalent optical signal. The photonic signal generated from the MZM is then transmitted into free space with the help ofan optical lens so that the dispersion of light is minimal. Free Space Optics is affected by weather conditions and

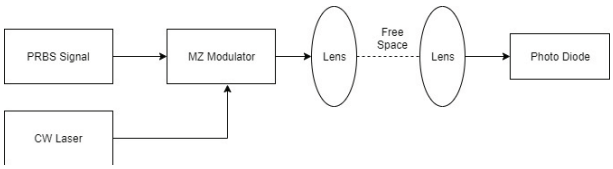


Figure 8. Basic Architecture of Free Space Optics

other atmospheric factors, which reduces the transmitting distance of the signals.

4.1 Radio over free space optics

Radio over FSO (RoFSO) is an extension of Radio over Fiber techniques in which RF baseband signals make use of optical light as carriers for distribution over networks [15]. For transmission over the atmosphere, Radio over Fiber signals is amplified and emitted into free space. The demerits of RoFSO technology are its dependence on atmospheric conditions, which can be solved using various dispersion compensation techniques presented in this paper.

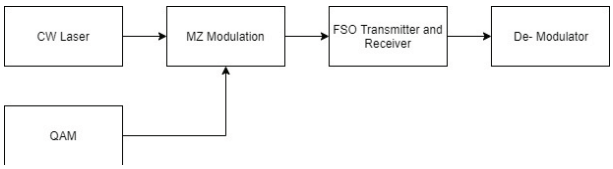


Figure 9. Radio over Free Space Optics where modulated signals are transmitted over free air.

Mm-Wave frequencies are limited by range. With its limited range of capabilities, and adaptive fronthaul architecture is required. Fibers combined with RoFSO provide the flexibility to network designers to design a system that can be adapted to the design environment.

4.2 FSO based backhaul and front haul architecture

In fifth-generation wireless architecture, fibers are being deployed for front haul because of their higher capacity. Previously, it is discussed that using Multi-Mode Fibers, the bandwidth of the fibers can be increased. Similarly, we have proposed a design methodology where RoFSO can be deployed in fronthaul and Backhaul as per design needs. 6Gcommunication systems are expected to meet the demands of a fully digital and connected world. High-speed, high-capacity communication with low latency is expected to be the basic norm to meet the needs of technologies such as VR and IoT. Remote geographic locations have made the deployment of 5G internet communication more costly and complex. 6G communication systems should have flexibility and adaptability in deployment [16]. Aerial Access Networks (AANs) are a potential solution for

6G communication. Unlike terrestrial wireless communication networks, AANs use satellites and airships to deploy networks in hard-to-reach places. AANs are expected to work synchronously with existing terrestrial wireless communication methodologies. FSO can connect Core Office with satellites which in turn beam signal to remote 6G antenna nodes. FSO plays a significant role in inter-satellite communication and ground-satellite communication.

Also, FSO could significantly replace fibers in metro cities where the deployment of fibers is challenging due to congestion. FSO can be used as a medium of transmission instead of fibers providing flexibility to network designers.

5 High-capacity Ro-FSO transmission with mode division multiplexing

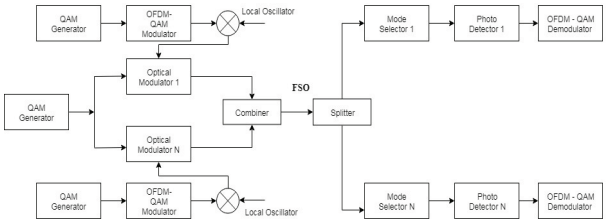


Figure 10: High-Capacity Ro-FSO Transmission with Mode Division Multiplexing.

A schematic diagram of the proposed hybrid high-speed Ro-FSO transmission system is shown in Figure 10. In the proposed system, Laguerre Gaussian/Hermite Gaussian was multiplexed through free space. Two independent 40 GHz radio signals were modulated using a 4-level Quadrature Amplitude Modulation (QAM) followed by modulation by 512 OFDM subcarriers. The purpose of the Orthogonal Frequency Division Multiplexing(OFDM) modulation is to reduce the multipath fading effect incurred during the transmission through the FSO link [17]. The OFDM approach divides the data over a vast number of sub-carriers, which are separated from each other at narrow frequencies.

The OFDM signal was then modulated at 7.5 GHz by using Quadrature Modulator (QM). This OFDM-QM modulated signal was then fed to a lithium niobate modulator which modulated the experimental LG/HG modes at 40 GHz. The modulator is assumed to preserve the modal stability of the channels. The output from the channels was transmitted over the FSO link.

The modes were demultiplexed using a spatial photodetector wherein an inner circular aperture of 5 cm was used to extract the modes. The received power between the apertures was adjusted such that the intensities on both the circular and outer apertures were equal. A 40 GHz was applied after the photodetector using a mixer to recover the Sub Carrier Multiplexing (SCM) signal. Finally, the output signal after the mixer was fed to the OFDM demodulator followed by the Quadrature Multiplexing (QM) demodulator to recover the original data. Given table shows the constellation plot of various modes after 1 km of FSO transmission. Table 2 shows the constellation diagram of Ro Direct Detection OFDM (DD-OFDM) 4-LG modes. Table 3 shows the constellation diagram of RoFSO DD-OFDM 4-HG modes. Future work is to deploy IIR based post dispersion compensation methodology to increase performance [18]. The proposed photonics filter can be deployed along with opto-electronics oscillator in order to get a low phase noise, however further work needs to be done to evaluate the performance of the filter in above configuration [19].

Table 2. Constellation Diagram of RoFSO DD-OFDM (4LG Modes).

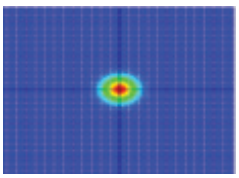
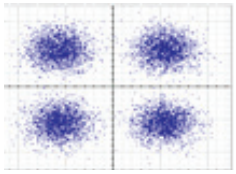
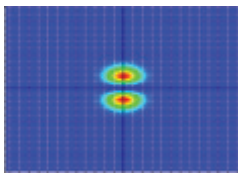
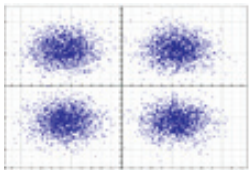
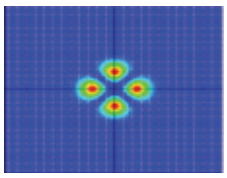
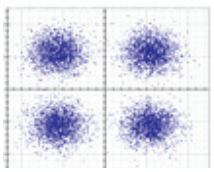
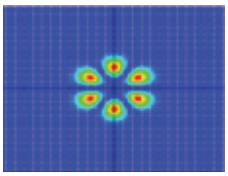
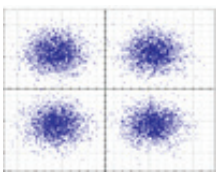
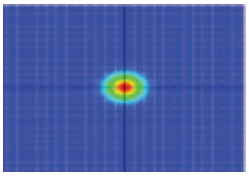
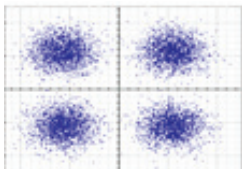
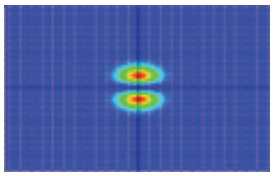
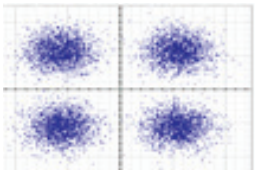
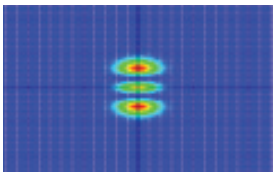
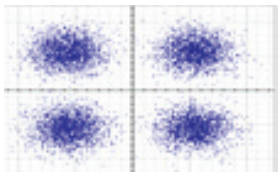
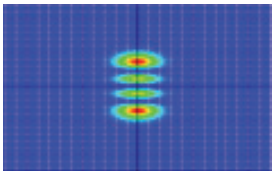
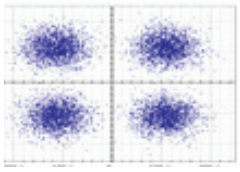
Modes	Constellation diagram
 (0, 0)	
 (0, 1)	
 (0, 2)	
 (0, 3)	

Table 3. Constellation Diagram of RoFSO DD-OFDM (4 HG Modes)

Modes	Constellation diagram
 (0, 0)	
 (0, 1)	
 (0, 2)	
 (0, 3)	

6 Conclusion

A design of novel photonics traversal filter to perform simulations of Mode Division Multiplexing in Multimode Fiber to increase the capacity of fiber is proposed. Model dispersion in the MMF is used as the time delay between filter taps. By using a single wavelength of 1550 nm, the capacity of the channel is increased by mode division multiplexing. We have proposed a design for FSO based fronthaul and backhaul architecture in next-generation 6G communication. We simulated various modes in multimode fiber in both FSO based and fiber-based network designs. Dispersion characteristics of FSO in long-distance transmission and higher capacity transmission need to be examined. Future works need to be done to verify the dispersion compensation performance of IIR based filters in FSO based transmission medium.

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Performance Assessment of Dispersion Compensation Using Fiber Bragg Grating and Dispersion Compensation Fiber Techniques

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Abstract: Dispersion should be flattened to achieve the most optimal output of the contact device. Since dispersion induces pulse spreading, which causes the output signal pulses to overlap, dispersion compensation is the most important attribute needed in an optical fiber communication device. A unique dispersion compensation system for a long-haul transmission system with a 5 Gbit/s data rate for each channel has been devised in this paper employing Fiber Bragg Grating (FBG) and Dispersion Compensation Fiber (DCF). The performance of dispersion compensation is evaluated using both grating and non-grating techniques. In this, primarily the proposed system is implemented without applying the grating technique and the outcomes are simulated and analyzed. Subsequently, the system is designed and implemented with FBG and DCF and the outcomes are simulated with opti-system-16.0 software. The proposed scheme is simulated with the 32768 numeral of samples with a bit rate of 109 bits/sec. The optical fiber's length can range from 50 to 200 kilometers. The parameters like Q-factor, Bit Error Rate (BER) and Signal to Noise Ratio (SNR) were simulated and calculated by exploiting the 8-channel device. With minimal 0.6 dB/km attenuation, FBG achieves a Q-factor of 288.335 and DCF achieves a Q-factor of 284.994 for 8 x 1 WDM MIMO communication systems with a 5 Gbit/s data rate. At the receiver end of systems, the suggested model improves performance in terms of bit error rate (BER) and quality factor.

Keywords: FBG; DCF; BER; Q-factor; WDM

Ocena učinkovitosti kompenzacije disperzije z uporabo Braggovih vlaknatih rešetk in kompenzacijo disperzije z vlakni

Izvleček: Disperzija mora biti izravnana, da se doseže najbolj optimalen izkoristek kontaktne naprave. Ker disperzija povzroča širjenje impulzov, zaradi česar se impulzi izhodnega signala prekrivajo, je kompenzacija disperzije najpomembnejša lastnost, ki je potrebna v komunikacijski napravi iz optičnih vlaken. V tem članku je bil zasnovan edinstven sistem za kompenzacijo disperzije za prenosni sistem na dolge razdalje s hitrostjo prenosa podatkov 5 Gbit/s za vsak kanal, ki uporablja FBG (Fiber Bragg Grating) in DCF (Dispersion Compensation Fiber). Učinkovitost kompenzacije disperzije je ocenjena z uporabo tehnik z rešetkami in brez njih. Pri tem je predlagan sistem izveden predvsem brez uporabe tehnike rešetk, rezultati pa so simulirani in analizirani. Nato je sistem zasnovan in izveden s FBG in DCF, rezultati pa so simulirani s programsko opremo opti-system-16.0. Predlagani sistem je simuliran s 32768 vzorci s hitrostjo prenosa 109 bitov/sek. Dolžina optičnega vlakna je lahko od 50 do 200 kilometrov. Parametri, kot so Q-faktor, stopnja bitne napake (BER) in razmerje med signalom in šumom (SNR), so bili simulirani in izračunani z uporabo 8-kanalne naprave. Z minimalnim slabljenjem 0,6 dB/km doseže FBG Q-faktor 288,335, DCF pa 284,994 za komunikacijske sisteme 8 x 1 WDM MIMO s hitrostjo prenosa podatkov 5 Gbit/s. Na sprejemni strani sistemov predlagani model izboljša učinkovitost v smislu BER in faktorja kakovosti.

Ključne besede: FBG; DCF; BER; Q-faktor; WDM

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1 Introduction

The introduction of WDM systems has expanded the spectrum of optical fiber's application to meet the requirements of high-speed, high-bandwidth, and high-capacity networks. Multiple signals with various wavelengths can be transmitted through WDM networks. At the same time, different signals from different users of different wavelengths are multiplexed in these networks [1]. The optical communication system transfers data from one place to another through light signals. Before being launched into the optical fiber, data or information in the form of an electrical signal is transferred into a light signal. The Transmitter, optical fiber, and Receiver are all components of the system. Depending on the application, the optical fiber used can be multimode or Single-Mode Fiber (SMF). SMF (Single-Mode Fiber) is used extensively in this paper [2].

Because optical fiber communications are a significant and quickly evolving technology, it's reasonable to compare their development to that of radio transmission over a century ago. Spark-gap transmitters and rudimentary receivers were used in the early days of radio. Optical fiber communications began about 25 years ago using directly modulated Light Emitting Diodes and lasers whose optical signal spectrum was far wider than the information bandwidth, similar to early radio systems. The vacuum-tube amplifier was a significant breakthrough in radio communications. [3]

Indeed, the race for faster speeds, higher quality, and massive capacity continues to drive significant advancement in the field of optical communications. Multilevel modulations, polarization multiplexing, coherence detection, and digital processing all play a key role in this regard, as they support and complement each other [4]. The current, well-established scheme of General Multiprotocol Label Switching (GMPLS) will be superseded by telecommunication traffic Software Defined Networking (SDN). This will make the deployment of programmable transponders easier, as well as the network's flexibility and management. [4]

The technique of dispersion compensation is used in fiber optic communication systems to deal with the dispersion introduced by the optical fiber. A light wave moving within the fiber is widened due to dispersion. Two consecutive pulses overlap due to the broadening of the pulse, creating Inter Symbol Interference (ISI). The receiver is unable to differentiate between two symbols due to ISI. This causes symbol recognition errors. It is for this purpose that dispersion compensation is necessary. Dispersion compensation can be done using a range of techniques, including Dispersion Compensating Fiber (DCF), Optical Filter, Fiber Bragg Grating (FBG), Optical Phase Conjugation, Electrical Dispersion Compensation, and so on [5]. Since DCF and FBG are commonly used techniques, these papers focus on them.

1.1 Fiber Bragg Grating (FBG)

FBG is a compensator for dynamic dispersion. At multiple wavelength variations, the FBG system can compensate for chromatic dispersion. As a result, it is the favored method of compensating for chromatic dispersion. The chirped FBG is based on the diffraction grating theory. Inside the propagating medium, Bragg gratings have a periodic variation of refractive index. The grating's chirped FBG allows it to reflect various wavelengths at different points along its length. As a result, it causes various delays for any of the different frequencies or wavelengths [5]. The shorter wavelength (blue light region) will arrive at the FBG first and will be mirrored higher up the FBG, where its Bragg condition will be met. As a result, the shorter wavelength has a longer delay [6]. The longer wavelength (red light region) would have a shorter delay because it travels slower. As a result, the pulse would be un-distributed at the circulator.

Although FBG filters are a cost-effective method for suppressing one of the sidebands in optical double sideband (DSB) modulation schemes, they lack flexibility in terms of adjusting the optical carrier wavelength [7]. Because chromatic dispersion is zero at 1310 nm, it could be another option for avoiding the power cost. The downside of employing the 1310 nm wavelength is that optical losses are higher than for the 1550 nm wavelength (0.2 dB/km for 1550 nm and 0.35 dB/km for 1310 nm) [7].

1.2 Dispersion Compensation Fiber (DCF)

Dispersion compensating fiber is a simple and effective way to upgrade single-mode fiber links that have already been built [8]. Negative dispersion-compensating fibers have a negative dispersion of 300 ps/nm/km and can be used to compensate for transmission fiber's positive dispersion. Group velocity dispersion, Kerr nonlinearity, and the accumulation of amplified random emission noise due to intermittent amplification all contribute to performance degradation in the optical WDM system. System output is dependent on the power levels at the input of various types of fibers, the location of the DCF, and the amount of dispersion due to the nonlinear nature of propagation [8]. Pre, post, and symmetrical compensation schemes are the three types of compensation schemes in which the DCF is mounted before, after, or symmetrically around the SMF. To minimize the size of a DCF, it should have low

insertion loss, low polarization mode dispersion and low optical nonlinearity, as well as a high chromatic dispersion coefficient [8].

To distribute a power-penalty-free millimeter-wave signal in the radio access network, a unique flexible technique with a single-loop optoelectronic oscillator at the sending end and a configurable dispersion-compensation module at the receiving ends is presented. One solution to the power penalty would be to replace the existing infrastructure with a dispersion-shifted fiber (DSF) instead of a conventional G.652D single-mode fiber. This is the most expensive option, but it provides wideband RF capabilities. However, it is limited in terms of optical wavelength since any deviation from the DSF's zero-dispersion wavelength results in chromatic dispersion effects [9].

2 Proposed methodology

The WDM 8*1 MIMO channel with compensation using Fiber Bragg Grating (FBG) and dispersion compensation fiber (DCF) is depicted in Figure 1. The block diagram is alienated into three subsystems: transmitter, receiver, and channel. The transmitter sub-block is made up of 8*1 input channels that go through a WDM (Multiplexer) MUX. The MUX signal travels through the channel, which is made up of optical fiber, an EDFA amplifier, FBG and DCF compensation techniques. The receiver sub -block consists of WDM, (Demultiplexer) DEMUX, and the received signal is transferred to the output channels in the final stage.

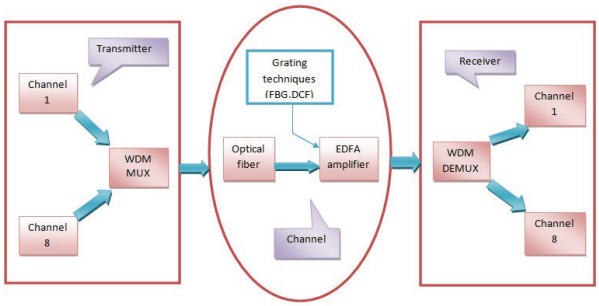

Figure 1: Block diagram of WDM MIMO 8 x 1channel with Compensation techniques using (FBG and DCF).

Figure 2 shows the subsystem of the WDM transmitter in which the Pseudo-Random Bit sequence generates sequence random bits (0 or 1). Due to the generator's characteristic of returning signals to zero between bits, the Non-return-to-zero (NRZ) pulse generator has the benefit of controlling bandwidth. In terms of bit rates, a pseudo-random bit sequence generator is used to scramble data signals. The Mach-Zehnder Modulator

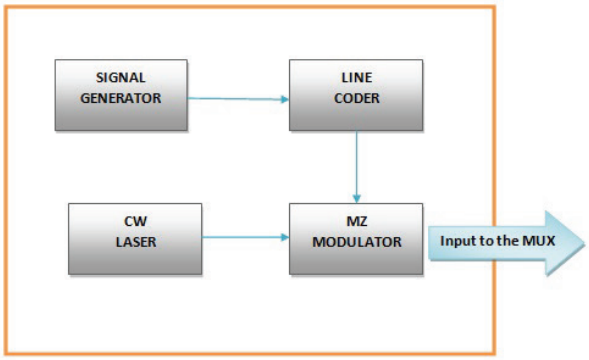

Figure 2: Subsystem of WDM transmitter

(MZM) has one output and two inputs (optical and electrical signals). A semiconductor laser represented by a Continuous Wave (CW) laser modulates the input signal via a Mach-Zehnder Modulator.

To produce optical signals, a continuous laser diode provides an input signal with a wavelength of 1550 nm and a 5 dBm input power that is externally modulated at 10 Gbit/s.

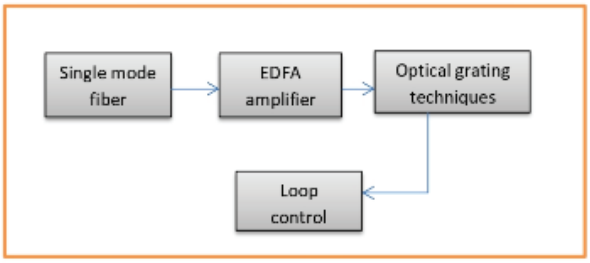

Figure 3: Optical fiber channel design installed with grating technique

Figure 3 shows the optical fiber channel design installed with the grating technique. Single-mode optical fiber is deployed as a transmission network because it has a faster data rate, less dispersion, and can be used over long distances. In the proposed model, the grating length is 6 mm. Optical amplification is sufficient to tackle fiber loss and enhance the signal before it is received by the PIN diode in the receiver segment.

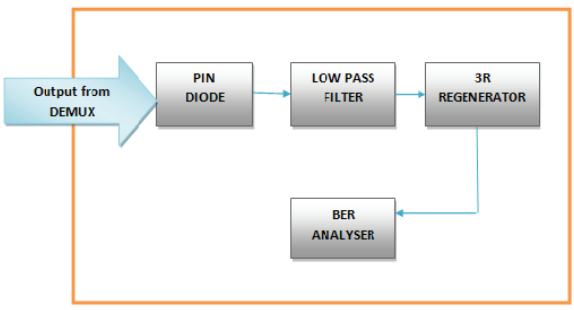

Figure 4: Receiver Sub block

Figure 4 illustrates the receiver sub-block of the 8 x 1 channel in which the Positive Intrinsic Negative (PIN) diode translates the optical signal into an electrical signal. One photon yields one electron. After the modulation, high-frequency noises are eliminated using filters. Bessel filter provides flat propagation. Low pass Bessel filter has flat phase and group delay. This has shallow frequency bands. The order of the low pass filter is 4. Bessel filter has the transfer function [10] as follows

$$\mathbf{H}(\mathbf{S}) = \frac{\alpha d_0}{B_N(S)} \tag{1}$$

$$d_0 = \frac{(2N)!}{2^N N!} \tag{2}$$

where H(s) represents the transfer function, **α is the parameter insertion loss** of unit in dB, N is the parameter order, and $B_N(s)$ an nth-order Bessel polynomial. BER visualizer allows the user to calculate and display the bit error rate (BER) of an electrical signal automatically. BER visualizer can estimate the BER using different algorithms such as Gaussian and Chi-Squared.

The flow chart of the proposed system is shown in figure 5. The simulation layout of FBG, DCF, transmitter subsystem, and receiver sub-system is shown in figure 6 and figure 7.

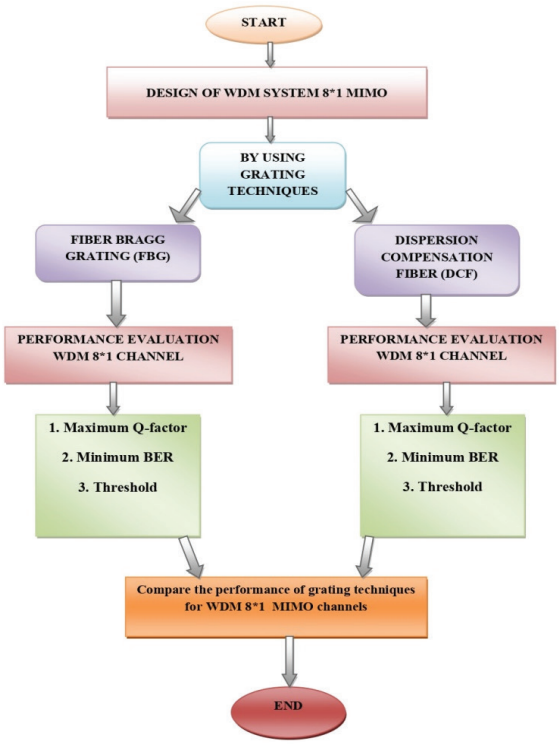

Figure 5: Flow chart of the proposed system

2.1 Flow chart

Figure 5 symbolizes the flow chart of the proposed system. The flow chart is intended to help visualizing the

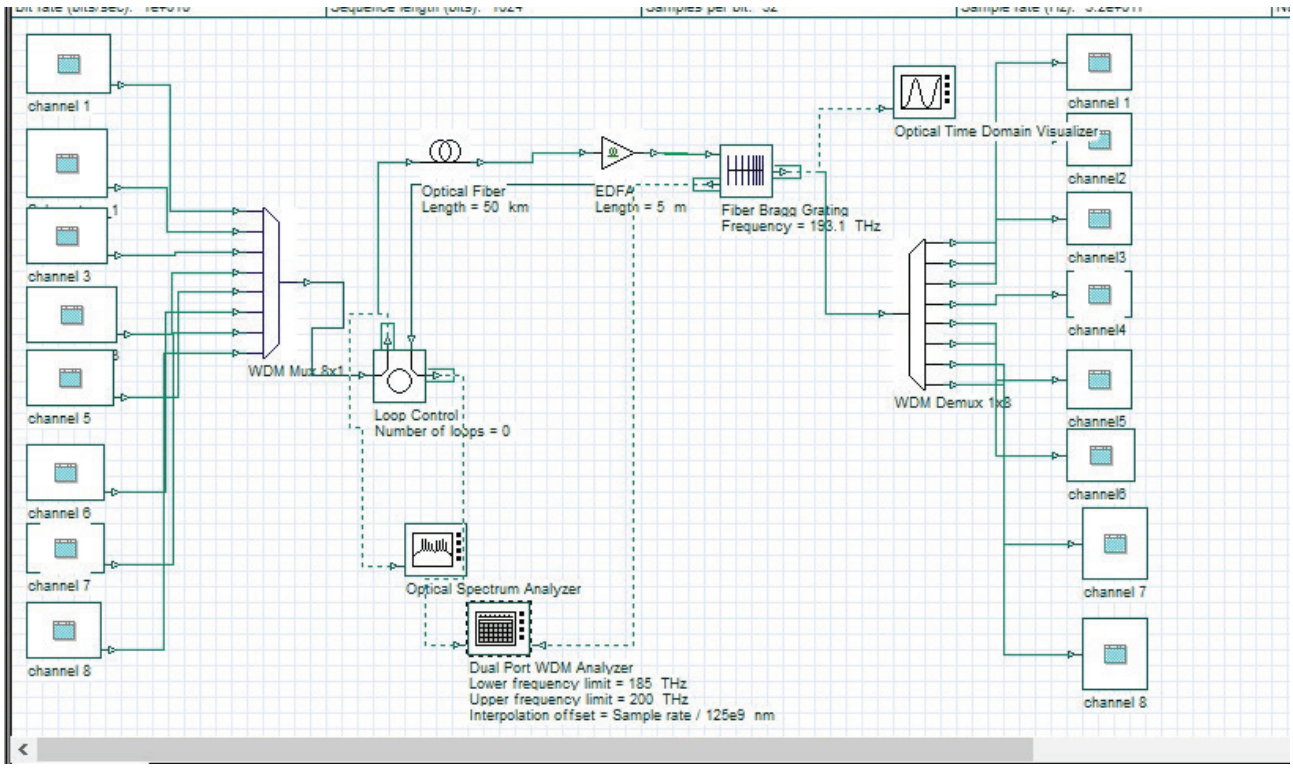

Figure 6: Simulation layout diagram of FBG in WDM system

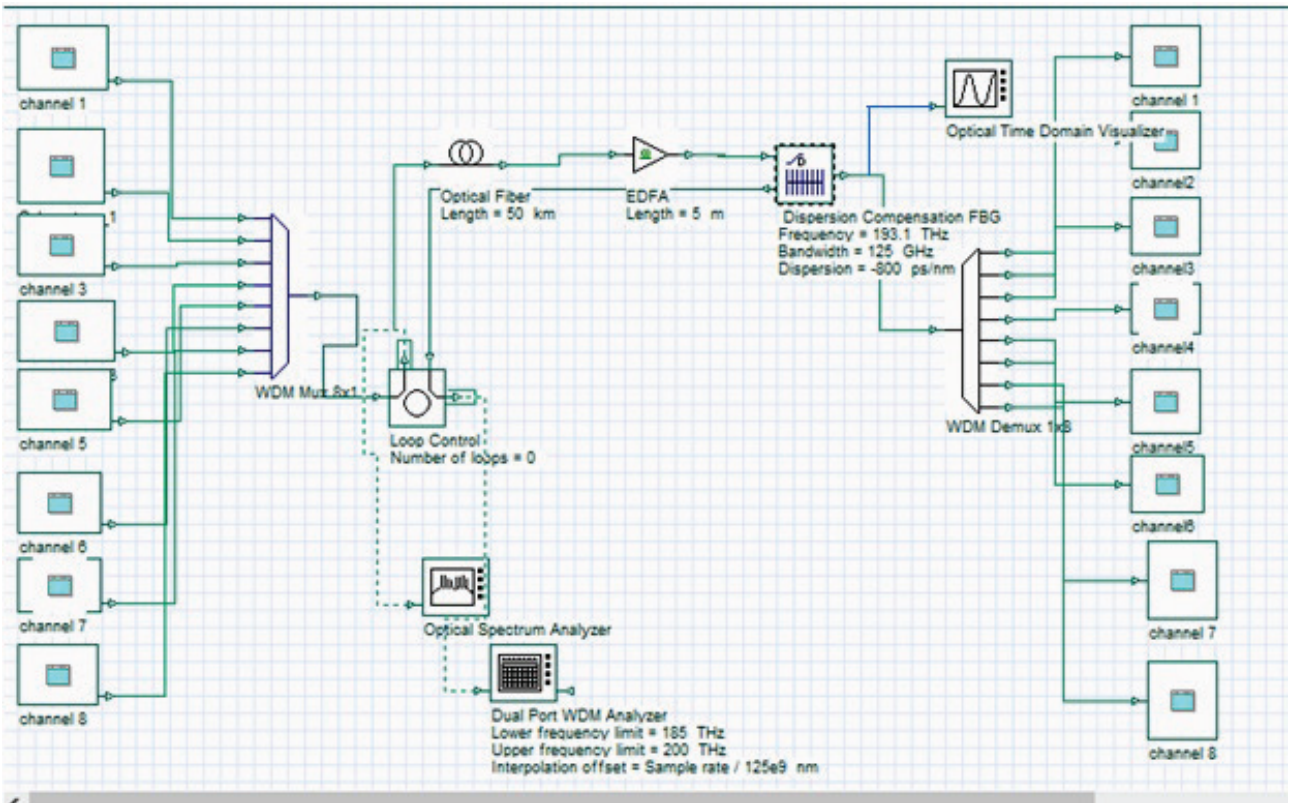

Figure 7: Simulation layout diagram of DCF in WDM system

proposed system. The proposed WDM system is made up of 8 x 1 WDM Multi Input Multi Output communication systems with a data throughput of 5 Gbit/s. The outcomes are simulated and analyzed.

Both grating and non-grating methodologies are used to evaluate the performance of dispersion compensation. The proposed system is first developed using a non-grating technique. In this proposed system, two grating techniques have been designed and implemented. They are FBG and DCF. The performance of both grating techniques was compared to that of a non-grating technique, and measures such as Q-factor, Bit Error Rate, and Signal to Noise Ratio were examined.

2.2 Layout

Figure 6 and 7 shows the simulation layout diagram of fiber Bragg grating and dispersion compensation fiber. This layout indicates the transmitter subsystem of 8 channels. The optical signal from the output of the transmitter is then directed in the direction of the WDM 8*1 multiplexer channels with the assist of an optical fiber. An optical receiver subsystem accepts the incoming signal as part of the WDM de-multiplexer system's receiver output. The signal is then directed in the direction of an avalanche photodiode (APD) which converts the optical sign into its electric counterpart. The APD photodiode is accompanied with the aid of using a Bessel low-pass filter which eliminates any high-frequency noise present inside the obtained signal.

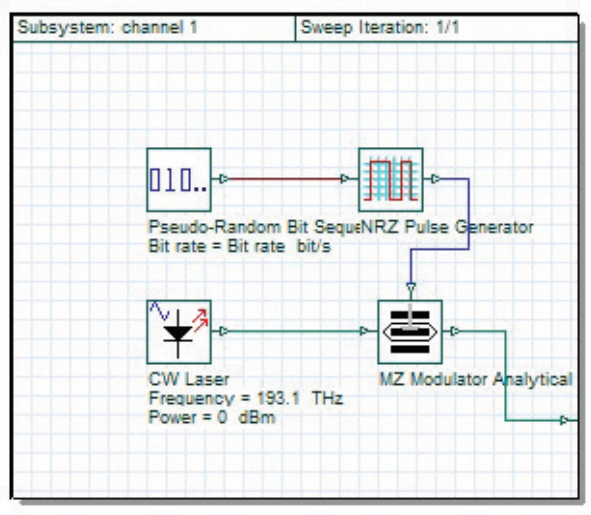

Figure 8: Layout diagram of Transmitter subsystem

Figure 8 confirms the layout of the transmitter subsystem which comprises a pseudorandom pulse generator that produces the information to be broadcasted in the structure of binary data. Binary data is fed into an NRZ pulse generator, which converts it into electrical pulses for transmission. The output of the NRZ pulse generator

is directed to an MZM, which modulates the electrical pulses with a 1,550 nm continuous wave laser.

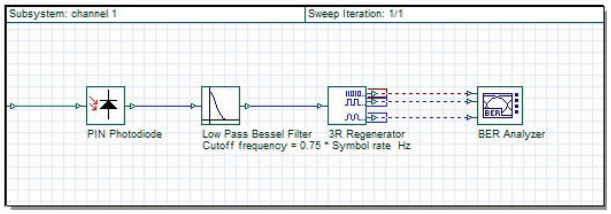

Figure 9: Layout diagram of Receiver subsystem

Figure 9 reveals the layout of the receiver subsystem which has a PIN diode accompanied with the aid of using a Bessel low-pass filter which eliminates any high-frequency noise present inside the obtained signal.

3 Results and discussion

This section presents the details of the experiment carried out for implementation. The system was simulated with opti-system-16.0 software. The simulation parameters used for developing the model are shown in Table 1 and Table 3.

3.1 Result analysis of Non-Grating technique

Initially, the proposed system is implemented for the non-grating technique. The outcomes are simulated and analyzed. The following figure shows the eye diagram of the non-grating technique of the proposed system. Figure 10 furnishes a small eye-opening in the eye diagram which means that the Inter Symbol Interference (ISI) is high.

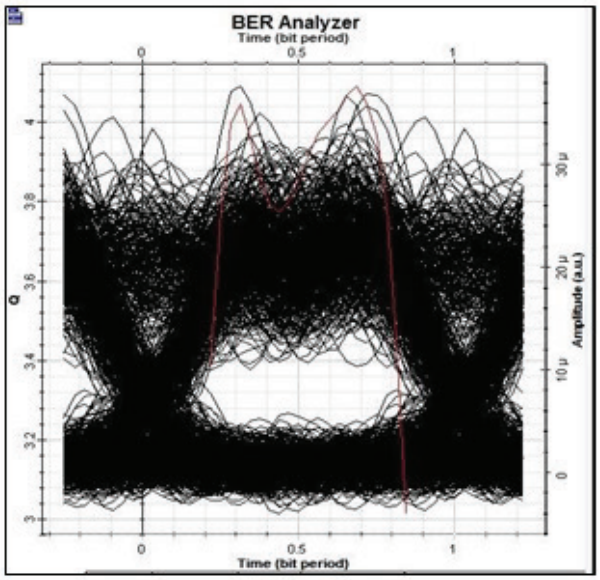

Figure 10: Result of non-grating technique

The simulation for the non-grating technique is done to analyze the Q factor of the single mode fiber 8 x 1 WDM channels. The results revealed a decrease in quality factor with slightly increased BER shown in Figure 10. To avoid dispersion and high inter-symbol interference, the proposed system is designed and simulated by using FBG and DCF techniques.

3.2 Fiber Bragg Grating simulation parameters

The simulation parameters of fiber Bragg gratings are indicated below.

Table 1: Parameters and their values

FIBER BRAGG GRATING	
Parameters	Values
Frequency	193.1-193.8 THz
Effective index length	1.45
Noise threshold	-100 dB
Noise dynamic	3 dB
Number of segments	101
Maximum number of spectral path	1000

Table 1 depicts the simulation parameters deployed to implement the proposed WDM system. Table 1 signifies the simulation inputs of FBG used in the proposed system. The values given in table 1 are attained using the trial and error method. Continuous Wave Laser (CWL) is used as the source with the transmitter frequency of 193.1 THz. The proposed system is simulated with the 32768 number of samples with a bit rate of 109 bit/sec. 100GHz of transmitter frequency spacing with 15 dBm of transmitter power is taken. The wavelength used for simulation is 1550 nm. The proposed system consists of a 5×8 Gbit/s WDM system with 8 channels sending 5 Gbit/s each with channel spacing 100 GHz. NRZ formatting is done in these 8 channels and is multiplexed at the transmitter side.

3.3 Result Analysis of FBG

Using FBG, the proposed system is simulated and the values are tabulated below.

Table 2: Outcomes of FBG in WDM system

Distance in km	Maximum Q-factor	BER	SNR
50	288.335	0	61.704
100	287.516	0	61.626
150	286.176	0	61.669
200	285.096	0	61.68

Table 2 shows the FBG outputs obtained in the WDM system. These outputs are obtained with the varied inputs given in table 1.Table 2 reveals the outcome of FBG in the WDM system which has the Max Q-factor, minimum bit error rate (BER). The outcome of FBG shows the maximum Q-factor of 288.335 obtained at a distance of 50 km. As the distance increases, Q-factor decreases with reduced SNR. BER is reduced to a minimum though the distance increases.

Eye Diagram of FBG

The eye diagram of FBG in terms of quality factor and BER is discussed below. Figures 11&12 represent the Q-factor and BER curve for using Fiber Bragg grating with a maximum Q factor of 288.335 and a minimum Q factor of 286.176 respectively.

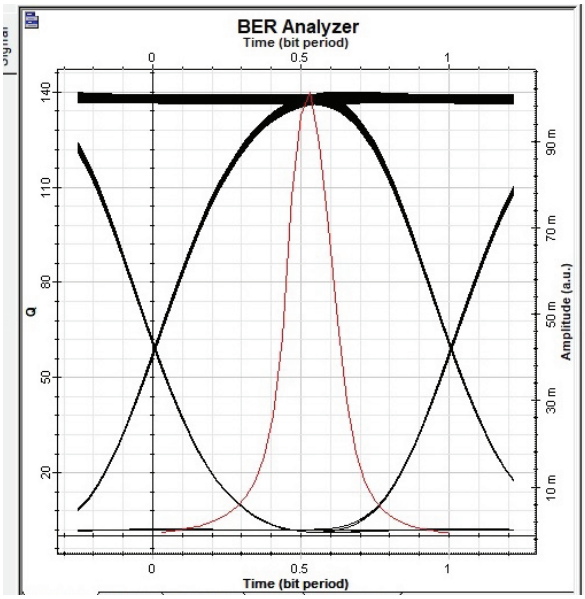

Figure 11: Eye diagram of FBG

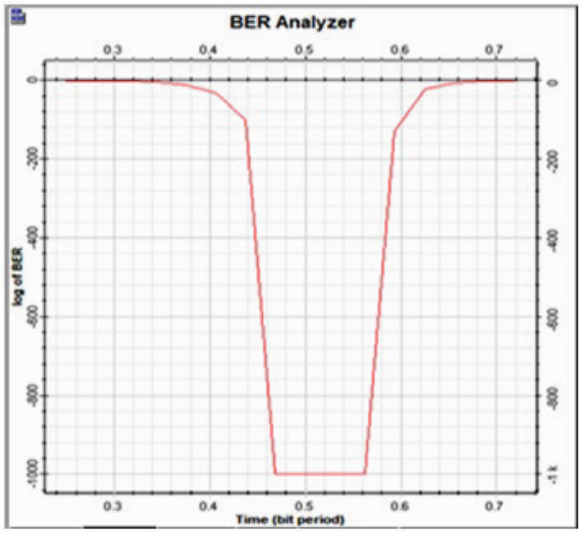

Figure 12: BER curve of FBG over bit period

The channel outcomes for using grating techniques in terms of eye diagrams are shown above. Q-factor represents the quality of the SNR in the 'eye' of a digital signal, the "eye" being the human eye-shaped pattern on an oscilloscope that indicates transmission system performance. The best place for determining whether a given bit is a "1" or a "0" is the sampling phase with the largest "eye-opening". The larger eye-opening, the greater the difference between the mean values of the signal levels for a "1" and a "0". The greater that difference is the higher the Q-factor and the better the BER performance. Q- Factor is usually defined as the eye-opening (difference between upper and lower signal levels) divided by the sum of the individual noise standard deviations on the two levels.

3.4 Dispersion Compensation fiber

The simulation parameters of dispersion compensation fiber are indicated below.

Table 3: Simulation parameter of DCF used in the proposed system

DISPERSION COMPENSATION FIBER	
Parameters	Values
Differential group velocity	3 ps / (nm km)
PMD coefficient	0.5 ps / $km^{1/2}$
Reference wavelength	1550 nm
Attenuation	0.6 dB / km
Dispersion	-80 ps / nm / km
Effective area	30 μm^2

Table 3 depicts the simulation parameters of DCF deployed to implement the proposed system. Table 3 signifies the simulation inputs of DCF used in the proposed system. The values given in table 3 is attained using the trial and error method

3.5 Result Analysis of DCF

Table 4: Outcomes of DCF in WDM system

Distance in km	Max Q-factor	BER	SNR
50	284.994	0	61.655
100	283.765	0	61.535
150	284.761	0	61.684
200	282.356	0	61.66

Table 4 reveals the outcome of DCF in the WDM system which has the maximum Q-factor, minimum bit error rate (BER). The outcome of FBG shows the maximum Q-factor of 284.994 obtained at a distance of 50km. As the distance increases, Q-factor decreases with reduced SNR. BER are reduced to minimum though the distance increases.

The Q-factor and BER curves for dispersion compensating fiber are shown in Figures 13 and 14. The obtained Q factor of 284.994 is greatest at a distance of 50km and a Minimum Q factor of 286.155 is obtained at 200km distance respectively.

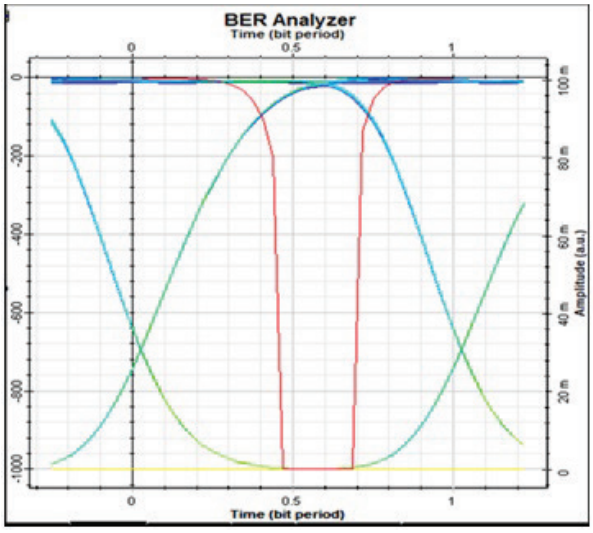

Figure 13: Eye diagram of DCF

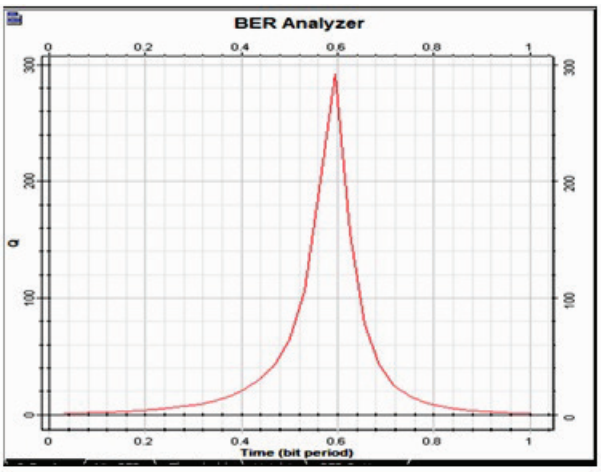

Figure 14: Q-factor of DCF over bit period

3.6 Comparative analysis of FBG, DCF and Non-grating techniques

The overall comparative Q factor analysis of all three techniques are tabulated and shown below.

Table 5: Comparative analysis of Q-factor

Type of Grating	Q factor
Fiber Bragg grating	288.335
Dispersion Compensation Fiber	284.994
Without any compensation	80.729

Table 5 depicts the overall comparative Q factor analysis of all three techniques and it is confirmed that the Q factor is maximum with FBG and least with dispersion compensation fiber. The Q factor is very poor for non-grating compensation technique.

Graphical representation of FBG vs. DCF

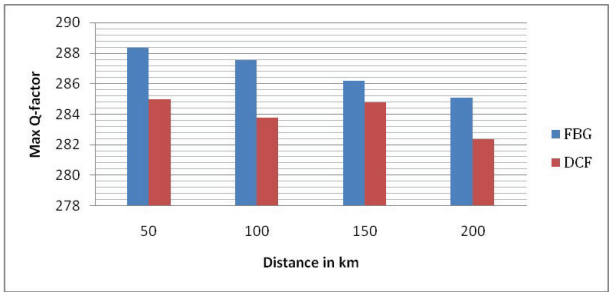

Figure 15: Graphical representation of FBG vs. DCF

4 Conclusions

The overall objective of the paper is achieved by mitigating the dispersion present in the optical fiber channel. As a dispersion compensator for a 200 km long-distance optical communication network, a novel dispersion compensation model incorporating FBG and DCF has been devised in this paper. This paper focuses on the usage of optical grating methods with an 8 x 1 WDM MIMO communication system having a 5 Gbit/s data rate. Since the interference of the signal had its considerable effect on the received output spectrum, the Fiber Bragg grating and dispersion compensation fiber performance were analyzed with a WDM system. The capacity of the design is made maximum and promising equal output response for all users present in the channel.NRZ line coding techniques are analyzed as line codec methods irrespective of Return-to- Zero (RZ) because of the high sensitivity of NRZ. A detailed comparison of the system without grating and with grating is made. After simulation, the Q-factor and BER were determined using the eye-diagram analyzer. The improved Q factor of 288.335 is attained with FBG, 284.994 is achieved for DCF, considering minimum of 0.6 dB/km attenuation. The output signal spectrum results from the spectrum analyzer are dispersion-free after compensation with the grating technique. The bit error rate is minimized as much as possible at the receiver. As a result, the suggested dispersion compensator technique enhances Q-factor, reduces bit error rate and transfers a large amount of data, boosting the overall performance of an optical fiber network.

5 Conflict of interest

The author of this document does not have any Conflict of Interest (COI) in publishing this paper.

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Programmable Universal Filter and Quadrature Oscillator Using Single Output Operational Transconductance Amplifiers

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Abstract: This paper presents a new programmable universal filter and quadrature oscillator based on the single output operational transconductance amplifiers (OTAs). The proposed universal filter and quadrature oscillator can be achieved into single topology by programming analog switches. When the circuit performs as a universal filter, it can realize low-pass, high-pass, band-pass, band-stop and all-pass filters with orthogonal and electronic controls of the natural frequency and quality factor. When the circuit performs as a quadrature oscillator, it provides a three-phase quadrature output signal which the condition and frequency of oscillations can be controlled orthogonally and electronically. The proposed structure can be realized based on the single output OTAs which are easily implemented as both commercially available integrated circuits (ICs) as OTAs and complementary metal-oxide semiconductor (CMOS) OTAs as IC forms. SPICE simulation using standard 0.18 µm CMOS process is used for investigating the performance of the proposed circuit whereas the workability of new circuit is confirmed by LM13600 discrete-component integrated circuits as OTAs.

Keywords: Universal filter; quadrature oscillator; operational transconductance amplifier; analog signal processing; voltage-mode circuit

Programirljiv univerzalni filter in kvadraturni oscilator z uporabo enojnih izhodnih operacijskih transkonduktančnih ojačevalnikov

Izvleček: Članek predstavlja nov programirljiv univerzalni filter in kvadraturni oscilator, ki temelji na enojnih izhodnih operacijskih transkonduktančnih ojačevalnikih (OTA). Predlagani univerzalni filter in kvadraturni oscilator je mogoče s programiranjem analognih stikal združiti v enotno topologijo. Ko vezje deluje kot univerzalni filter, lahko izvede nizkoprepustne, visokoprepustne, pasovne, zaporne in vseprepustne filtre z ortogonalnim in elektronskim upravljanjem lastne frekvence in faktorja kakovosti. Če vezje deluje kot kvadraturni oscilator, zagotavlja trifazni kvadraturni izhodni signal, katerega stanje in frekvenco oscilacij je mogoče ortogonalno in elektronsko krmiliti. Predlagano strukturo je mogoče realizirati na podlagi enojnih izhodnih OTA, ki jih je mogoče enostavno izvesti tako v obliki komercialno dostopnih integriranih vezij (IC) kot OTA kot komplementarnih kovinsko oksidnih polprevodniških (CMOS) OTA v obliki IC. Simulacija SPICE z uporabo standardnega 0,18 µm CMOS procesa je uporabljena za raziskovanje delovanja predlaganega vezja, medtem ko je uporabnost novega vezja potrjena z diskretnimi integriranimi vezji LM13600 kot OTA.

Ključne besede: Univerzalni filter; kvadraturni oscilator; operacijski transkonduktančni ojačevalnik; analogna obdelava signalov; napetostno vezje

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1 Introduction

The operational transconductance amplifiers (OTAs) are commonly used to realize analog signal processing circuits [1], [2]. There are numerous advantages of using OTA such as electronic tuning capability, simple structure, easy for implementing both bipolar junction transistor (BJT) and complementary metal oxide semiconductor (CMOS) with the same structure and powerful ability to generate various circuits. The OTA based circuits require no resistors therefore making it suitable for integrated circuits (ICs) implementation. There are discrete-component ICs as OTAs such as CA3080, LM13600, LM13700, NE5517 and MAX435 commercially available. It should be noted that discrete-component ICs as OTAs are single output devices therefore the utilization of single output OTA based circuits is very crucial. Although numerous outputs can be obtained by connecting the input terminals in paralled using discrete component ICs, the number of devices utilized will equal the number of required outputs, incresing the component count and power consumption.

The universal biquad filters are the topologies that usually provide variant second-order filtering responses from the same topology including low-pass (LP), band-pass (BP), high-pass (HP), band-stop (BS) and all-pass (AP). This filter can be applied to electronic, control and communication systems such as cross-over network used in a three-way high-fidelity loudspeaker, touch-tone telephone used for tone decoders and phase-locked loop used for FM stereo demodulators [3]. Additionally, it can also be used as a subcircuit for realizing high-order filters [4]. Many universal biquad filters have been reported, for example, see [5]-[28]. OTA-based universal filters have been proposed already in [9]-[28]. Considering input and output terminals, these universal filters can be classified into three categories: (i) single-input multiple-output (SIMO) filter [9], [10], (ii) multiple-input single-output (MISO) filter [11]-[22] and (iii) multiple-input multiple-output (MIMO) filter [23]-[28]. The SIMO filter provides variant filtering responses for the output terminals of LP, BP, HP, BS, and AP when a single input signal is applied. The MISO filter delivers variant filtering responses by appropriately applying the input signal and output signal can be obtained with single output terminal while MIMO filter provides filtering responses by appropriately applying the input signals and appropriately selecting the output terminals. Compared to the SIMO filter, the MISO and MIMO filters usually require lesser active and passive elements. The voltage-mode universal filters typically require the properties such as high-input and low-output impedances to obviate additional buffer circuits, absent from inverting-type input signal requirements to avoid additional inverting amplifiers and orthogonal controls of the natural frequency and quality factor.

Quadrature oscillators are the circuits that usually provide two sinusoids with 90° phase difference for a variety of applications such as for telecommunications in quadrature mixers, single-sideband generators, direct-conversion receivers or for measurement purposes in vector-generators and phase sensitive detection [29], [30]. Several quadrature oscillators have been reported, for example, see [30]-[36]. Quadrature oscillators that enjoy orthogonal control of the condition and frequency of oscillations are required. OTA-based quadrature oscillators have been proposed, for example, see [37]-[39].

Recently, the structures that can give both universal filter and quadrature oscillator have been reported [40]-[57]. The universal filter and quadrature oscillator can be obtained with the same topology [40]-[49] however, it is necessary to change the connection for obtaining either a universal filter or a quadrature oscillator. Futhermore, several of these topologies suffer from some drawbacks such as exciting the input signal through capacitors [40], [41], requiring component-matching condition for obtaining all-pass filtering responses [42], [45], [47], [48], requiring minus-type input signal or double input signal for obtaining some filtering responses [43], lacking orthogonal control of the natural frequency and the quality factor [44] and obtaining the current output that flowing through capacitor which is not ideal for integrated circuits implementation [49].

The structure in [50] realizes universal filter and quadrature oscillator without changing any connection, but only LP, HP and BP filters are provided. The structure in [51] realizes quadrature oscillator and its structure can be modified to work as universal filter, but only LP and BP filtering responses are obtained. The structures in [52]-[57] realize universal filter and quadrature oscillator without changing any connection. In [52]-[53], either a universal filter or a quadrature oscillator can be obtained by selecting the switches, but passive-matching condition is required for obtaining HP filtering response. In [54], the universal filter or the quadrature oscillator can be obtained by adjusting the ratio of resistances while in [55]-[57], the universal filter or the quadrature oscillator can be obtained by adjusting the ratio of bias currents. It is well-known that the filters are commonly realized based on linear system whereas oscillators are generally realized based on non-linear system. As a result, the condition for obtaining universal filter and quadrature oscillator by adjusting the ratio of resistances [54] and the ratio of bias currents [55]-[57] must be careful. Especially, in case of the circuits

are operated as high-Q filters, self-oscillation must be avoided.

OTA-based universal filter and quadrature have been already reported [18], [25]-[28], but these systems provide universal filter and quadrature oscillator by adding or modifying the feedback connection.

This work proposes a new programmable voltage-mode universal filter and three-phase quadrature oscillator using single output OTAs and grounded capacitors. Universal filter and quadrature oscillator can be achieved into single topology by programming using analog switches. If the circuit acts as universal filter, it is a four-input one-output universal filter that offers the advantages such as realizing LP, BP, HP, BS, and AP filters by appropriately applying input signal, without inverting-type signal requirements and high-input impedance. The natural frequency and quality factor can also be controlled orthogonally and electronically. In case the circuit works as quadrature oscillator, it is a three-phase quadrature oscillator that the condition and frequency of oscillation can be controlled orthogonally and electronically. For IC implementation, the usage of grounded capacitor is ideal and the use of single-output OTAs is also easily implemented as commercially integrated circuits (ICs). SPICE simulation results using standard 0.18 μm CMOS technology are used to verify the characteristic of the proposed circuit. The results of an experiment are used to confirm the workability of the new topology.

The comparison of the proposed circuit with those of previous universal filters and quadrature oscillators is shown in Table 1. Compared with the circuits in [53]-[54], the proposed circuit offers electronic controls, without component-matching condition, high input impedance and using ground capacitor. Compared with the current-mode circuits in [55]-[57], the proposed circuit offers a new technique for obtaining universal filter and quadrature oscillator. Namely the programmable technique which can be easy obtained universal filter or quadrature oscillator. If focusing only universal filter, the comparison of the proposed circuit with some universal filters is shown in Table 2. Comparing with voltage-mode universal filters in [20], [21], the proposed filter does not require component-matching condition or inverting-type input signal for obtaining five filtering responses. Compared with the current-mode universal filters in [46], [47], the proposed filter is absent from passive resistors.

2 Proposed circuit

The circuit symbol of OTA is shown in Fig. 1 and its ideal characteristic can be described by

$$I_o = g_m \left(V_{in+} - V_{in-} \right) \tag{1}$$

where I_o is the output current, g_m is the transconductance gain, V_{in+} and V_{in-} denote respectively non-inverting and inverting input terminals.

Table 1: Comparison of this work with those of previous universal filter and quadrature oscillator.

Factor	[53]	[54]	[55]	[56]	[57]	Fig. 4
Number of active devices	2-DVCC	2-CFA	3-CFTA	2-CCCII	2-CCFTA	5-OTA
Number passive components	2-C, 2R	2-C, 3-R	2-C, 1-R	2-C	2-C	2-C
Operation mode	CM	VM	CM	CM	CM	VM
Using grounded capacitor	Yes	No	Yes	Yes	Yes	Yes
Offer universal filter/quadrature oscillator into single topology	Yes	Yes	Yes	Yes	Yes	Yes
Technique to obtaining filter/oscillator	SW	Con	Con	Con	Con	Pro
Independent control of ω_o and Q of filter	Yes	No	Yes	Yes	Yes	Yes
No component-matching condition for obtaining five responses	No	No	Yes	Yes	Yes	Yes
Independent control of CO and FO of oscillator	Yes	No	Yes	Yes	Yes	Yes
Offer electronic controls	Yes	No	Yes	Yes	Yes	Yes
Obtaining results	Sim/Exp	Sim	Sim	Sim/Exp	Sim	Sim/Exp

Note: CFA = current feedback amplifier, CFTA = current follower transconductance amplifier, CCCII = current controlled second-generation current conveyor, CCFTA = current controlled current follower transconductance amplifier, VM = voltage-mode, CM = current-mode, SW = using switch, Con = using condition, Pro = using programmable, Sim = simulation, Exp = experimental

Table 2: Comparison of this work with those of previous universal filters.

Factor	[20]	[21]	[26]	[47]	[49]	Fig. 2
Number of active devices	5-OTA	5-OTA	5-OTA	2-VDCC	1-VDGA	5-OTA
Number passive component	2-C	2-C	2-C	2-C & 2-R	2-C & 2-R	2-C
Type of filter	MISO	MISO	MISO	SIMO	SIMO	MISO
Independent control of ω_o and Q of filter	Yes	No	Yes	Yes	Yes	Yes
No component-matching condition for obtaining five responses	No	No	Yes	No	No	Yes
No need of input inverting/matching for obtaining five filtering responses	Yes	No	Yes	Yes	Yes	Yes
Offer electronic controls	Yes	Yes	Yes	Yes	Yes	Yes
Obtaining results	Sim	Sim	Sim/Exp	Sim	Sim	Sim/Exp

Note: DVGA = voltage differencing gain amplifier, VDCC = voltage differencing current conveyor.

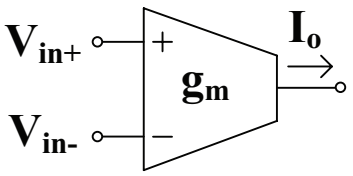


Figure 1: Electrical symbol of OTA.

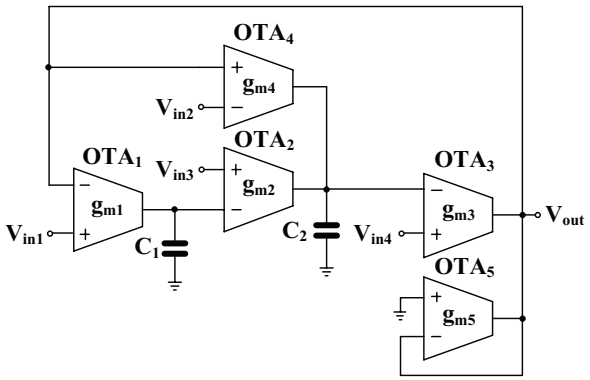


Figure 2: Universal biquad filter using single output OTAs.

Fig. 2 shows the voltage-mode universal biquad filter with four-input single-output using single output OTAs. This work is continuously developed next from previous work in [14]. The input signals V_{in1}, V_{in2}, V_{in3} and V_{in4} of filter are supplied to high impedance terminals of OTAs (infinite for ideal case), thus it requires no buffer circuits because the loading effect is vanished.

If V_{in1}, V_{in2}, V_{in3} and V_{in4} are input signal voltages, the output voltage of the proposed filter can be expressed by

$$V_{out}=\frac{s^2C_1C_2\left(\frac{g_{m3}}{g_{m5}}\right)V_{in4}-s\left(\frac{C_1g_{m2}g_{m3}}{g_{m5}}\right)V_{in3}+s\left(\frac{C_1g_{m3}g_{m4}}{g_{m5}}\right)V_{in2}+\left(\frac{g_{m1}g_{m2}g_{m3}}{g_{m5}}\right)V_{in1}}{s^2C_1C_2+s\left(\frac{C_1g_{m3}g_{m4}}{g_{m5}}\right)+\left(\frac{g_{m1}g_{m2}g_{m3}}{g_{m5}}\right)} \quad (2)$$

From (2), five standard filtering responses can be obtained as

The non-inverting LP response: $V_{in2}=V_{in3}=V_{in4}=0$ (grounded), $V_{in1}=V_{in}$.

The non-inverting BP response: $V_{in1}=V_{in3}=V_{in4}=0$ (grounded), $V_{in2}=V_{in}$.

The inverting BP response: $V_{in1}=V_{in2}=V_{in4}=0$ (grounded), $V_{in3}=V_{in}$.

The non-inverting HP response: $V_{in1}=V_{in2}=V_{in3}=0$ (grounded), $V_{in4}=V_{in}$.

The non-inverting BS response: $V_{in2}=V_{in3}=0$ (grounded), $V_{in1}=V_{in4}=V_{in}$.

The non-inverting AP response: $V_{in2}=0$ (grounded), $V_{in1}=V_{in3}=V_{in4}=V_{in}$.

Therefore, five standard filtering responses can be obtained by appropriately applying the input signals and realization to obtain these filtering functions without component-matching conditions and inverting-type input signal requirements. The output impedance of the proposed universal filter in Fig. 2 is given by $1/g_{m5}$.

The natural frequency (ω_o) and quality factor (Q) of all filtering responses can be expressed by

$$\omega_o=\sqrt{\frac{g_{m1}g_{m3}}{C_1C_2}\cdot\frac{g_{m2}}{g_{m5}}} \quad (3)$$

$$Q=\frac{1}{g_{m4}}\sqrt{\frac{C_2g_{m1}}{C_1g_{m3}}\left(g_{m2}g_{m5}\right)} \quad (4)$$

Letting $g_{m2}=g_{m5}=g_m$, (3) and (4) can be rewritten as

$$\omega_o=\sqrt{\frac{g_{m1}g_{m3}}{C_1C_2}} \quad (5)$$

$$Q = \frac{g_m}{g_{m4}}\sqrt{\frac{C_2 g_{m1}}{C_1 g_{m3}}} \tag{6}$$

From (3) and (6), parameter ω_o for all filtering responses can be controlled electronically through g_{m1} and g_{m3} by keeping $g_{m2} = g_{m5}$ and $C_1 = C_2$ while parameter Q can be controlled electronically and independently through g_m ($g_m = g_{m2} = g_{m5}$) or g_{m4} by keeping $g_{m1} = g_{m3}$ and $C_1 = C_2$. This keeping is used only for easy to control parameters ω_o and Q which is not meaning of component-matching conditions.

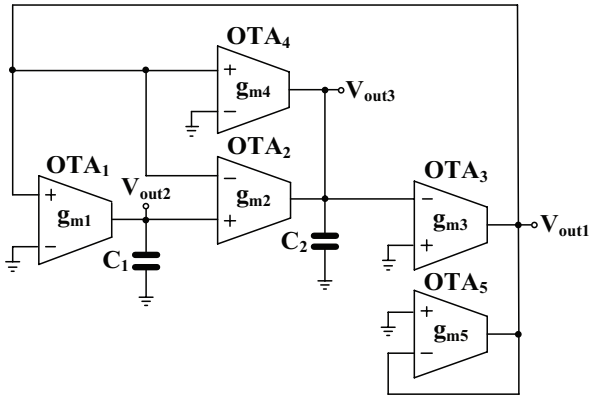


Figure 3: Three-phase quadrature oscillator modified from universal filter.

The universal biquad filter in Fig. 2 has been slightly modified to work as a three-phase quadrature oscillator as shown in Fig. 3. The oscillator can be obtained by interchanging the connections between non-inverting and inverting terminals of OTA_1 and between non-inverting and inverting terminals OTA_2 in Fig. 2. The inputs V_{in1}, V_{in3}, V_{in4} are connected to ground while the input V_{in3} will connect to the output V_{out} to creating a positive feedback loop. Thus, the transfer function between V_{out} and V_{in3} of Fig. 2 in case work as oscillator can be expressed as

$$\frac{V_{out}}{V_{in3}} = \frac{s\left(\frac{C_1 g_{m2} g_{m3}}{g_{m5}}\right)}{s^2 C_1 C_2 + s\left(\frac{C_1 g_{m3} g_{m4}}{g_{m5}}\right) + \left(\frac{g_{m1} g_{m2} g_{m3}}{g_{m5}}\right)} \tag{7}$$

Setting $V_{out}/V_{in3} = 1$ (V_{out} is connected to V_{in3}), characteristic equation of quadrature oscillator can be expressed by

$$s^2 + s\frac{g_{m3}}{C_2 g_{m5}}\left(g_{m4} - g_{m2}\right) + \left(\frac{g_{m1} g_{m3}}{C_1 C_2}.\frac{g_{m2}}{g_{m5}}\right) = 0 \tag{8}$$

The condition of oscillator (CO) and frequency of oscillation (FO) can be expressed respectively by

$$g_{m4} = g_{m2} \tag{9}$$

$$\omega_o = \sqrt{\frac{g_{m1} g_{m3}}{C_1 C_2}.\frac{g_{m2}}{g_{m5}}} \tag{10}$$

Letting $g_{m2} = g_{m5}$, (10) can be simply expressed by

$$\omega_o = \sqrt{\frac{g_{m1} g_{m3}}{C_1 C_2}} \tag{11}$$

From (9) and (11), it is evident that the CO can be controlled electronically by g_{m4} and keeping $g_{m2} = g_{m5}$ and the FO can be controlled electronically and independently by g_{m1} and/or g_{m3} and keeping $C_1 = C_2$. Thus, the proposed quadrature oscillator provides electronically and independently control of CO and FO.

It should be noted that the quadrature oscillator in Fig. 3 provides three output terminals V_{out1}, V_{out2} and V_{out3}. To express that three output-terminals provide sinusoidal with 90° phase different, the transfer functions can be expressed by

$$\frac{V_{out2}}{V_{out1}} = \frac{g_{m1}}{sC_1} \tag{12}$$

$$\frac{V_{out3}}{V_{out2}} = \frac{g_{m2}}{sC_2} \tag{13}$$

Letting $s = j\omega_o$, (12) and (13) can be rewritten respectively as $V_{out1} = j\left(\omega_o C_1 / g_{m1}\right)V_{out2}$ and $V_{out2} = j\left(\omega_o C_2 / g_{m2}\right)V_{out3}$ which indicates that the voltages V_{out1}, V_{out2}, V_{out3} are in the quadrature form.

The universal filter in Fig. 2 and quadrature oscillator in Fig. 3 can be blended into single topology. Fig. 4 shows the proposed programmable universal filter and quadrature oscillator. Universal filter and quadrature oscillator can be programmed by analog switches SW_1 and SW_2. The commercially available analog switches i.e., MAX14689, MAX4735, TMUX1136, TS3A44159, CD4016B, can be used to implement switches SW_1 and SW_2. Assume that analog switch MAX14689 [58] is used in Fig. 4 for selecting a universal filter or a quadrature oscillator.

The status of switch can be controlled by CB (i.e., logic "0" or "1"). Assume that the present status of SW_1 and

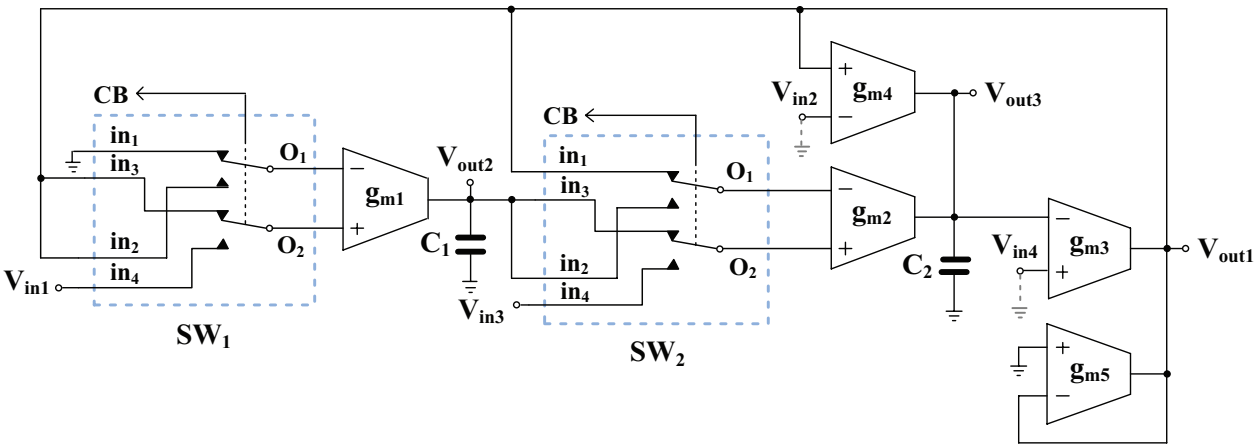


Figure 4: Proposed programmable filter and quadrature oscillator.

SW_2 as shown Fig. 4 is CB = 0 (i.e., "0' = 0V), the circuit will be worked as a quadrature oscillator by connecting V_{in2} and V_{in4} to ground. Three-phase outputs can be obtained as V_{out1}, V_{out2}, V_{out3}. It should be noted that the operation of the circuit in this case is similar the quadrature oscillator in Fig. 3.

Continually, if the status of SW_1 and SW_2 is CB = 1 (i.e., "1" = 5V), the circuit in Fig. 4 will be operated as a universal filter by applying the input signals to V_{in1}, V_{in2}, V_{in3} and V_{in4} while the output signal is obtained as V_{out1}. The operation of circuit in this case is similar the universal filter in Fig. 2. Therefore, the proposed circuit can be worked as universal filter and quadrature oscillator by programming technique. There is no topology that operates similar the proposed circuit available in open literature. The condition for obtaining universal filter and quadrature oscillator is concluded in Table 3.

Table 3: Using proposed programmable universal filter and quadrature oscillator

Circuit type	SW_1 and SW_2	Input terminal	Output node
Quadrature oscillator	CB=0	V_{in2}=V_{in4}=0 (grounded)	V_{out1}, V_{out2}, V_{out3}
Universal filter	CB=1	V_{in1}, V_{in2}, V_{in3}, V_{in4}	V_{out1}=V_{out}

3 Non-ideal analysis

Considering non-idealities of OTA, non-ideal transconductance gain g_{mni} is given by

$$g_{mni}(s) = \frac{g_{mi}\omega_{gi}}{s+\omega_{gi}} \tag{14}$$

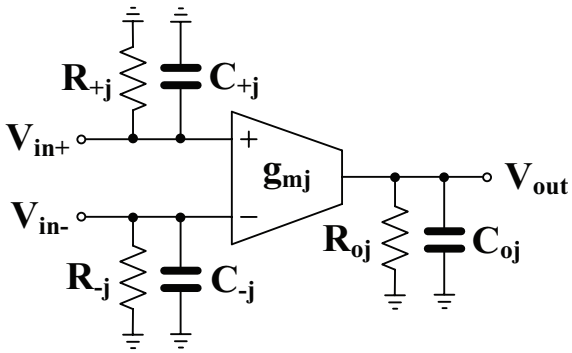


Figure 5: Modeling the non-idealities in the OTA [16].

where ω_{gi} and g_{mi} denote the first-order pole frequency and the open-loop transconductance gain of OTA_i (i = 1, 2, .., n). In the frequency range of interest of this paper, g_{mni} can be modified as [17]

$$g_{mni}(s) \cong g_{mi}(1-\mu_i s) \tag{15}$$

where $\mu_i = 1/\omega_{gi}$.

Consider first-order pole frequency ω_{gi}, it is a result of the parasitic input and output resistances (R_{in} and R_o) and the input and output capacitances (C_{in} and C_o) as shown in Fig. 5. The high-resistance and small-capacitance values will be resulted to high-value of ω_{gi} and small-value of μ_i.

Using (15), denominator of transfer function of universal filter can be written as

$$s^3 C_1 g_{m3} g_{m4}(\mu_3\mu_4 - B) + s^2 C_1 C_2 (1-C) + sC_1 g_{m3} g_{m4}(1-D) + A \tag{16}$$

Were

$$A = g_{m1} g_{m2} g_{m3}$$

$$B = \frac{C_1 C_2 \mu_5 + A\mu_1\mu_2\mu_3}{C_1 g_{m3} g_{m4}}$$

$$C = \frac{C_1 g_{m3} g_{m4}\mu_3 + C_1 g_{m3} g_{m4}\mu_4 - A\mu_1\mu_2 - A\mu_1\mu_3 - A\mu_2\mu_3}{C_1 C_2}$$

$$D = \frac{A\mu_1 + A\mu_2 + A\mu_3}{C_1 g_{m3} g_{m4}}$$

For the effect of OTA parasitic elements, it can be neglected by satisfying the following condition:

$$\left.\begin{aligned} B &\cong \mu_3\mu_4 \\ C &<< 1 \\ D &<< 1 \end{aligned}\right\} \quad (17)$$

The various passive and active sensitivities on the parameters ω_o and Q of the universal filter can be expressed as

$$S_{g_{m1}}^{\omega_o} = S_{g_{m2}}^{\omega_o} = S_{g_{m3}}^{\omega_o} = -S_{g_{m5}}^{\omega_o} = -S_{C_1}^{\omega_o} = -S_{C_2}^{\omega_o} = \frac{1}{2} \quad (18)$$

$$S_{g_{m1}}^{Q} = S_{g_{m2}}^{Q} = S_{g_{m5}}^{Q} = S_{C_2}^{Q} = -S_{g_{m3}}^{Q} = -S_{C_1}^{Q} = \frac{1}{2} \quad (19)$$

$$S_{g_{m4}}^{Q} = -1 \quad (20)$$

Thus, all incremental parametric sensitivities for parameters ω_o and Q are within 1 which has low active and passive sensitivities.

4 Simulation and experimental results

4.1 Simulation results

The proposed universal filter and quadrature oscillator has been simulated using 0.18 µm CMOS technology from TSMC. The CMOS OTA in Fig. 6 [59] was used and the switch was implemented using MOS transistors as shown in Fig 7. If CB = logic "0", switch will be turned on and it will be turned-off if CB = logic "1". Fig. 8 shows analog switch that used to program universal filter and quadrature oscillator and its operation was similar Table 2. The power supply of ±1.2 V was used. The aspect ratios of NMOS and PMOS were given respectively as 5µm/1µm and 10µm/1µm [59]. The logic "0" of 0 V and logic "1" of 1.2 V were given. The performances of OTA and MOS switch were summarized in Table 4.

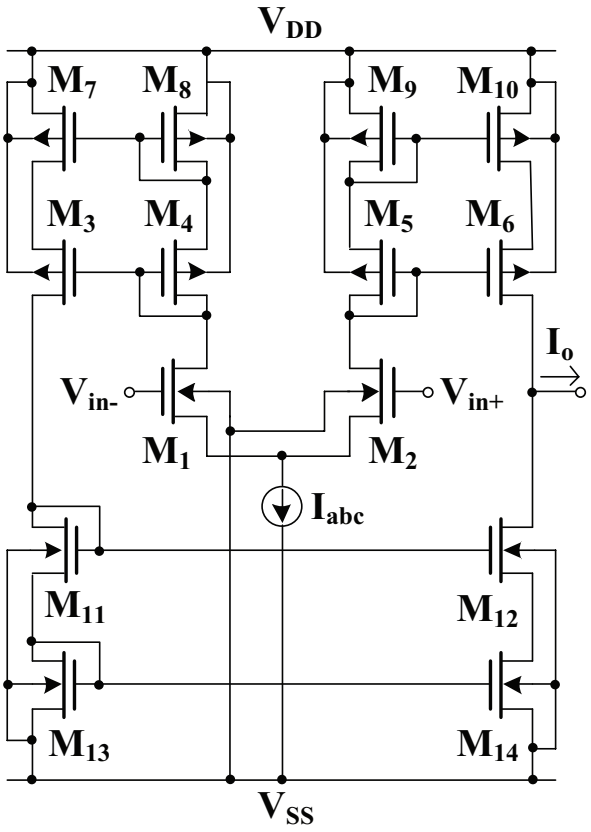


Figure 6: CMOS implementation for OTA [59].

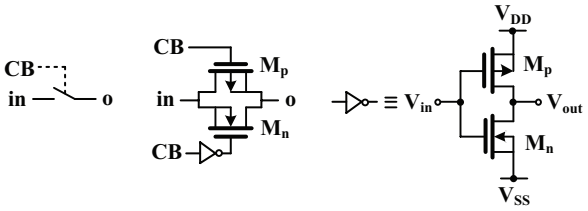
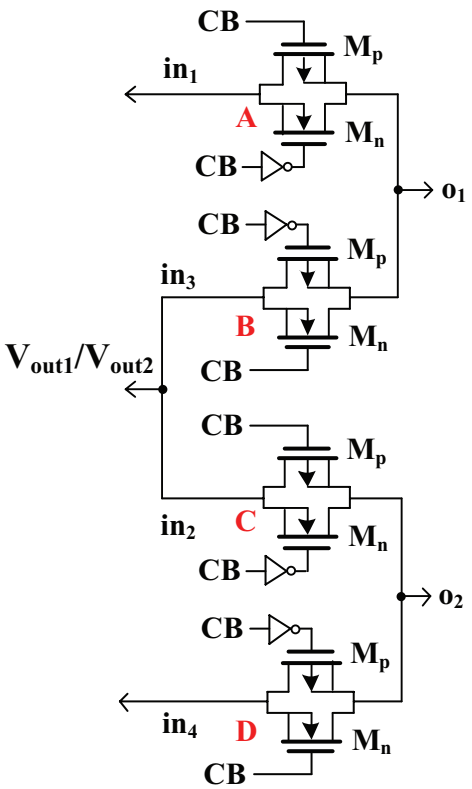


Figure 7: Switch implementation: (a) symbol, (b) MOS switch, (c) CMOS inverter.

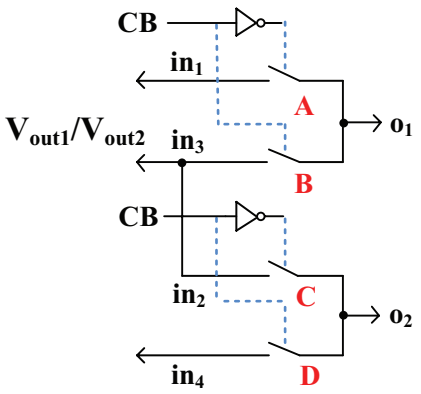
Table 4: Simulated specifications of CMOS OTA and MOS switch.

Parameter	Value
Technology	0.18 µm
Power supply	±1.2 V
OTA	
g_m (I_{abc}=1-50µA)	12 to 220 µA/V
Bandwidth (-3dB) @ I_{abc}=1 µA @ I_{abc}=50 µA	23 MHz 300 MHz
Parasitic parameters @ I_{abc}=50 µA R_o//C_o	 38.6 MΩ//18 fF
Power consumption @ I_{abc}=50 µA	240 µW
MOS switch	
R_{on}	320 Ω
R_{off}	380 MΩ

(a)



(b)



Logic CB	SW A	SW B	SW C	SW D
0	NO	OFF	ON	OFF
1	OFF	ON	OFF	ON

Figure 8: Analog switch implementation: (a) circuit, (b) symbol.

First case, the circuit has been operated as a universal filter by setting CB= "1" (1.2V). The capacitors C_1 = C_2 = 22 pF and the bias currents I_{abc1}=I_{abc2}=I_{abc3}=I_{abc4}=I_{abc5} =20µA (g_m=139.86µS) were designed. This setting has been designed to obtain the LP, BP, HP, BS, and AP filter responses with $f_o \cong$ 1 MHz and Q=1.

Fig. 9 shows the simulated frequency responses of the LP, HP, BP, and BS filters of the proposed filter. At natural frequency, the notch depth of attenuation in case of BS filter was about -25 dB which should be less than -30 dB for an acceptable level. It causes from the parasitic parameters of OTAs which deeper the notch of attenuation can be obtained when the filter was operated as lower natural frequency. Fig. 10 shows the simulated frequency responses of the gain and phase characteristics of the AP filter. It was evident from Figs. 9 and 10 that the proposed circuit provides five standard filtering responses without inverting-type input signal.

Fig. 11 shows the simulated frequency response of BP filter when the biasing currents I_{abc} (I_{abc}=I_{abc1}=I_{abc3}) were respectively adjusted for the values of 5, 10, 20 and 50 µA. This result was confirmed that the natural frequency can be electronically controlled. Fig. 12 shows the simulated frequency response of BP filter when the biasing current I_{abc4} was respectively varied for the values of 2, 5, 20, and 50 µA. This result was confirmed that the proposed circuit provides orthogonal and electronic controls for parameters ω_o and Q.

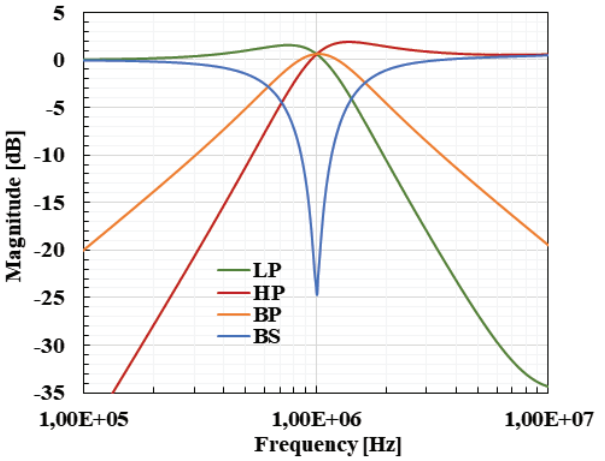


Figure 9: Simulated frequency responses of LP, HP, BP, and BS filters.

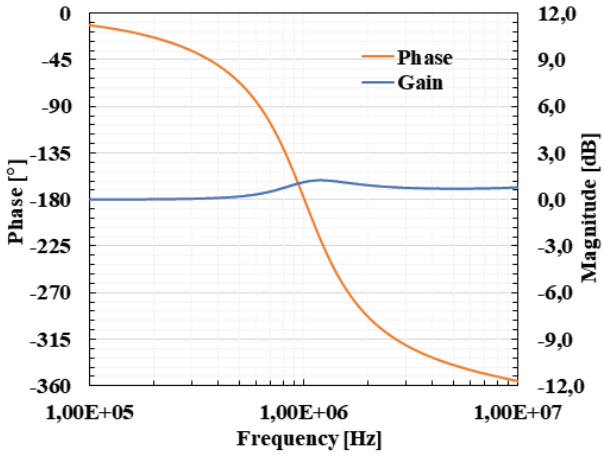


Figure 10: Simulated gain and phase responses of AP filters.

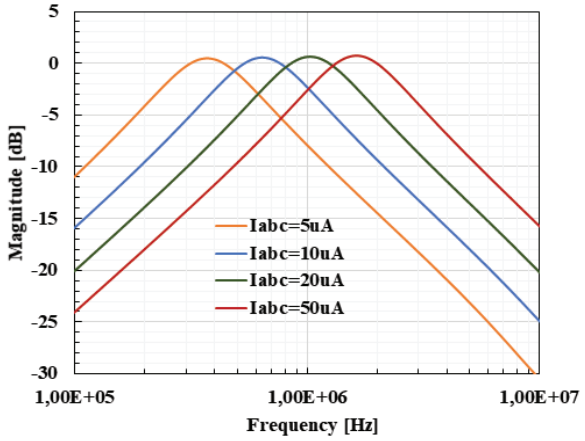


Figure 11: Simulated frequency responses of BP with different ω_o.

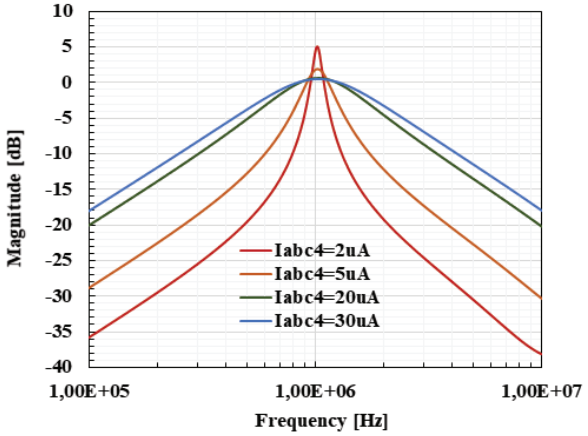


Figure 12: Simulated frequency responses of BP with different Q.

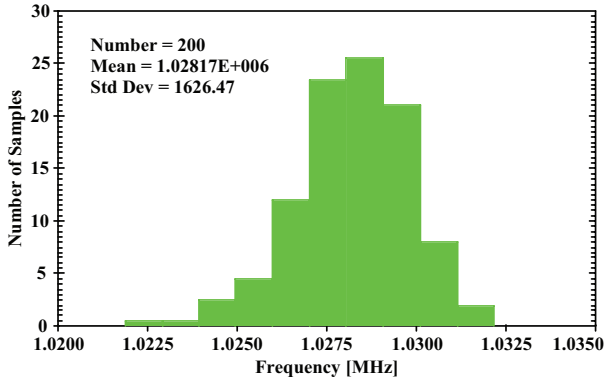


Figure 13: Simulated histogram of Monte-Carlo analysis for BP filter.

The Monte Carlo analysis of the frequency response with 5% variations of the transistor threshold voltage was performed. Fig. 13 shows the results of Monte Carlo analysis using 200 runs. From the derived histogram of f_o, it can be expressed that the standard deviation (σ) was 1.626 kHz, the mean was 1.028 MHz and therefore for the minimal and maximal of f_o were 1.021 MHz and 1.032 MHz, respectively. This result can be used to confirm the reliability of circuit functionality in case transistor mismatch on the CMOS OTA-based filter.

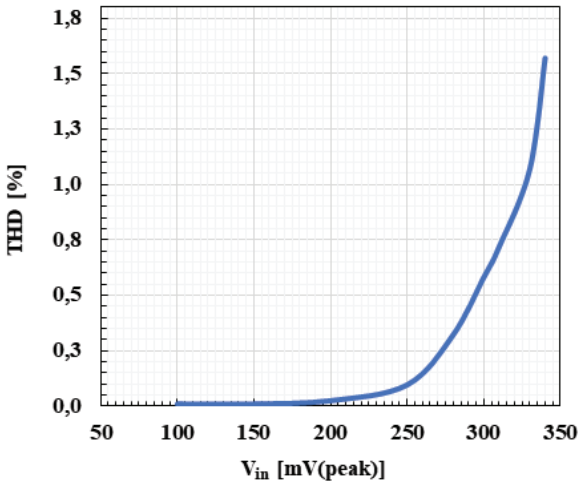


Figure 14: Simulated THD of LP filter

The dependence of the output harmonic distortion of low-pass filter on input voltage amplitude was shown in Fig. 14. It expresses that the THD was below 1 % for the input signal of 320 mV (peak).

Second case, the circuit has been operated as a quadrature oscillator by setting CB= "0" (0V). The biasing

(a)

(b)

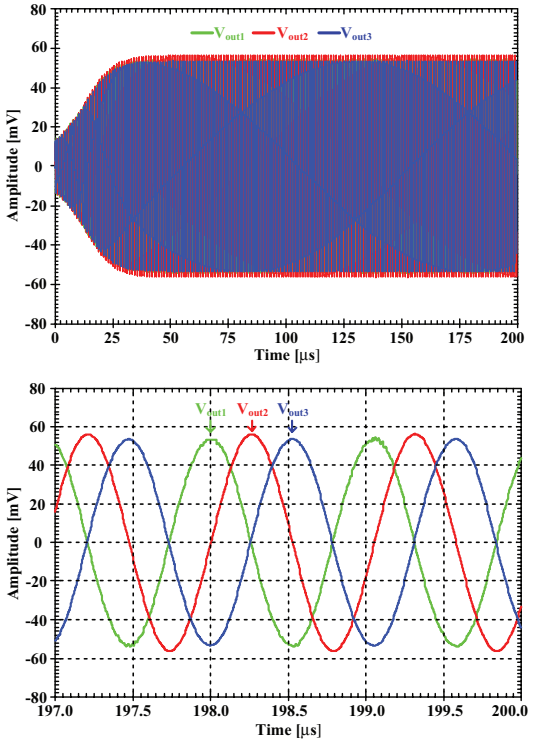


Figure 15: (a) simulated of the quadrature outputs V_{out1}, V_{out2}, V_{out3}, (b) steady state.

current I_{abc4} (≅18.6μA) was used to adjust g_{m4} for controlling the condition of oscillator. Fig. 15 shows the quadrature sinusoidal output waveforms of oscillator. This result shows a frequency of 0.95 MHz whereas theoretical value was 1.01 MHz. Fig. 16 shows the plot of the frequency of oscillation for varying the value of bias currents I_{abc} (I_{abc}=I_{abc1}=I_{abc3}) from 5 to 50μA. Theoretical value was used to confirm simulation results.

Fig. 17 shows output signal levels of V_{out1}, V_{out2} and V_{out3} versus the frequency of oscillation. Total harmonic distortion (THD) and phase error were respectively shown in Figs. 18 and 19.

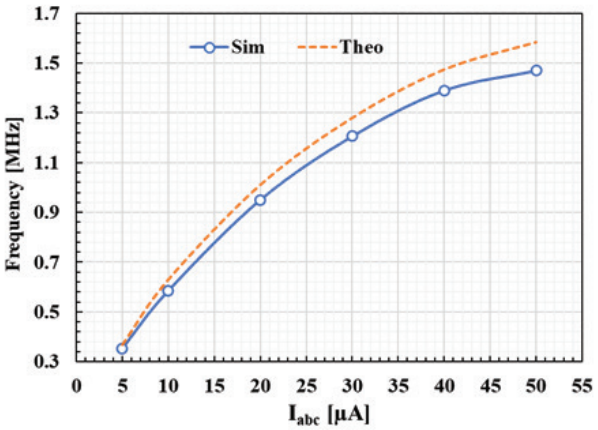


Figure 16: Simulated frequency of oscillation against biasing currents.

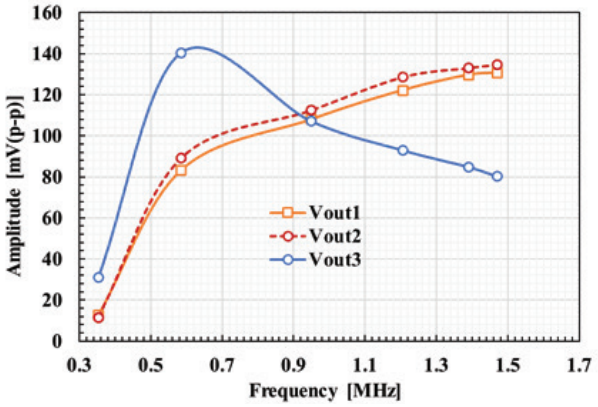


Figure 17: Simulated frequency of oscillation against voltage output amplitude.

4.2 Experimental results

To check the workability of proposed circuit, simulation and experiment tests have been performed simultaneously. The circuit was evaluated by SPICE simulator and experiment test using commercial OTA LM13600 [60]. The switches SW_1 and SW_2 were implemented using 4-channel analog switch CD4016B [61] and it was also available in PSPICE library. Fig. 20 shows the design of

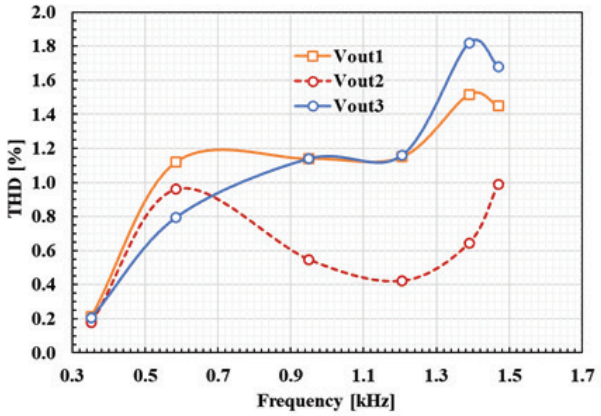


Figure 18: Simulated THD as a function of frequency of oscillation.

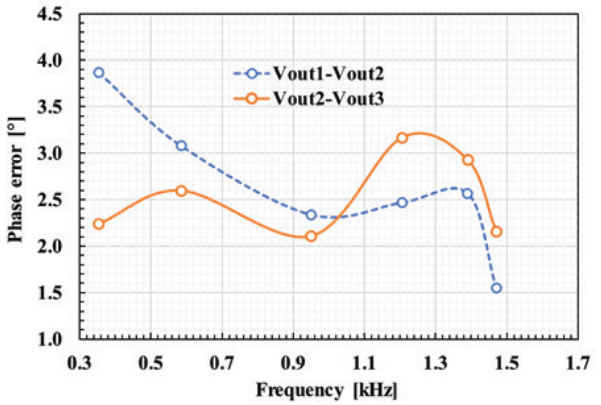


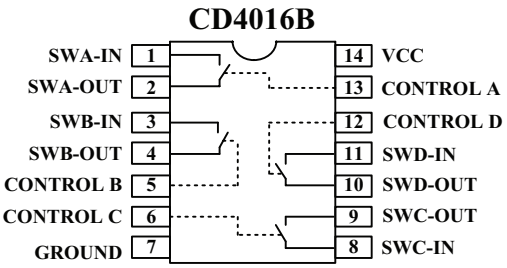
Figure 19: Simulated phase error as a function of frequency of oscillation.

SW_1 and SW_2 using 4-channel analog switch CD4016B that can be used in Fig. 4, namely CB = logic "0" for quadrature oscillator and CB = logic "1" for universal filter. The convention inverter 74LS04 have been used. The supply voltages were selected as V_{DD} = -V_{SS} = 5 V and capacitances C_1 and C_2 were given as 2.2 nF. The sinusoidal input signal and the measured output waveforms were taken using Agilent Technologies DSO-X 2002A oscilloscope.

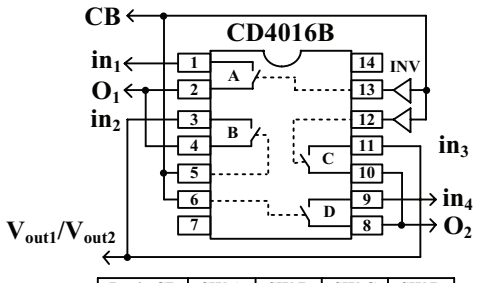
First case, the circuit will be operated as universal filter. The transconductances g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_{m5} = 1.512 mS (g_m = I_{ABC}/2V_T, I_{ABC} = 78.02 μA) were designed to obtain the filter with natural frequency of f_o = 109.38 kHz and quality factor of Q = 1. The bias current I_{ABC} of 78.02 μA can be obtained by using resistance (R_{ABC}) of 47 kΩ. To obtain CB = logic "0" and CB = logic "1", the voltage was set respectively as 0 V and 5 V.

Fig. 21 shows magnitude responses of LP, HP, BP, and BS responses with natural frequency of f_o = 109 kHz. Fig. 22 shows magnitude and phase responses of AP filter. Fig. 23 shows magnitude responses of BP filters when the values of g_m (g_m = g_{m1} = g_{m3}) were varied with the

(a)



(b)



Logic CB	SW A	SW B	SW C	SW D
0	NO	OFF	ON	OFF
1	OFF	ON	OFF	ON

Figure 20: 4-channel analog switch CD4016B: (a) CD4016B pinout, (b) Implementation for SW_1 and SW_2.

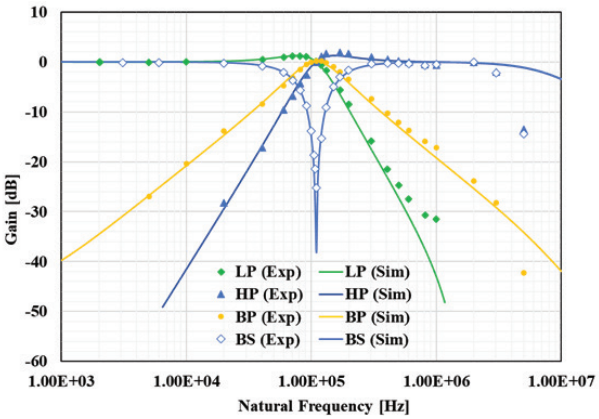


Figure 21: Magnitude responses of LP, BP, HP, and BS filter.

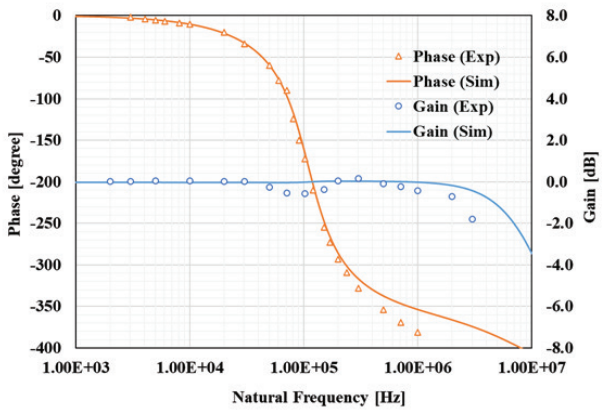


Figure 22: Magnitude and phase responses of AP filter.

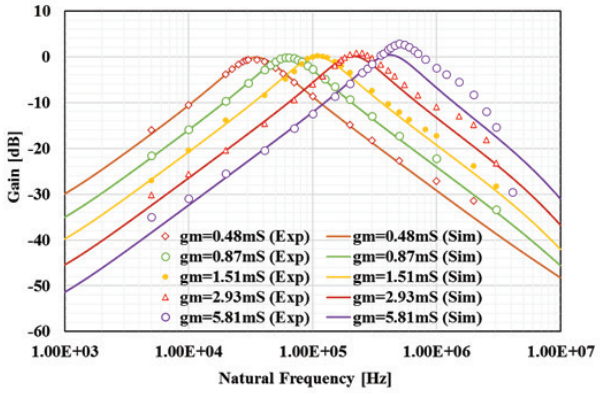


Figure 23: Magnitude responses of BP filter with different parameter ω_o.

values of 0.481 mS (I_{ABC} = 24.84 µA, R_{ABC}=150 kΩ), 0.873 mS (I_{ABC} = 45.06 µA, R_{ABC}=82 kΩ), 1.512 mS, 2.934 mS (I_{ABC} = 151.4 µA, R_{ABC}=24 kΩ) and 5.81 mS (I_{ABC} = 299.8 µA, R_{ABC} = 12 kΩ). In Fig. 23, the natural frequency f_o was varied from 38.9 kHz, 63.2 kHz, 109 kHz, 212.3 kHz and 419.7 kHz when g_m was varied respectively from 0.481 mS, 0.873 mS, 1.512 mS, 2.934 mS and 5.81 mS. Fig. 24 shows magnitude responses of BP filters when the values of g_m ($g_{m2} = g_{m5} = g_m$) were varied with different values of 0.873 mS, 1.512 mS, 2.934 mS, 5.81 mS, 8.45 mS (I_{ABC} = 436.3 µA, R_{ABC} = 8.2 kΩ) to express different parameter Q, while g_{m4} was fixed as 1.512 mS.

The LP filter has been used to test the distortion of the universal filter by setting the natural frequency of 109 kHz and applying the input frequency of 1 kHz. Fig. 25 shows total harmonic distortion (THD) parameter of the LP filter when the amplitude was varied. It expresses that the amplitude of 115 $mV_{(peak)}$, THD was 1 %.

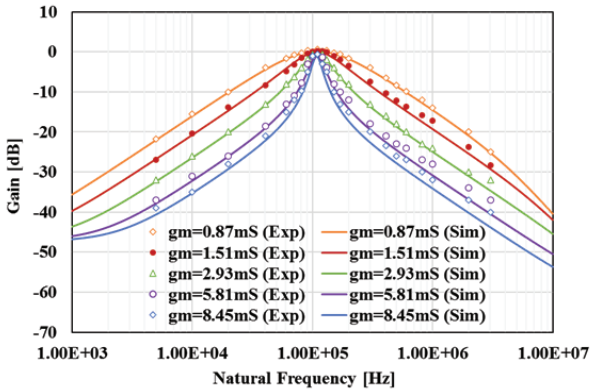


Figure 24: Magnitude responses of BP filter with different parameter Q.

Temperature stability of the proposed filter on parameter ω_o was simulated by varying temperature from -10° to 80° which was shown in Fig. 26. When the temperature was varied from -10 to 80 °, the corresponding f_o

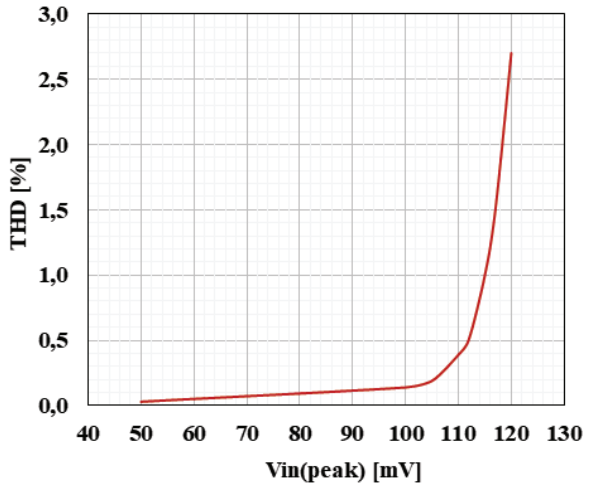


Figure 25: THD variations of the LP filter versus amplitudes of the input voltage at 1 kHz.

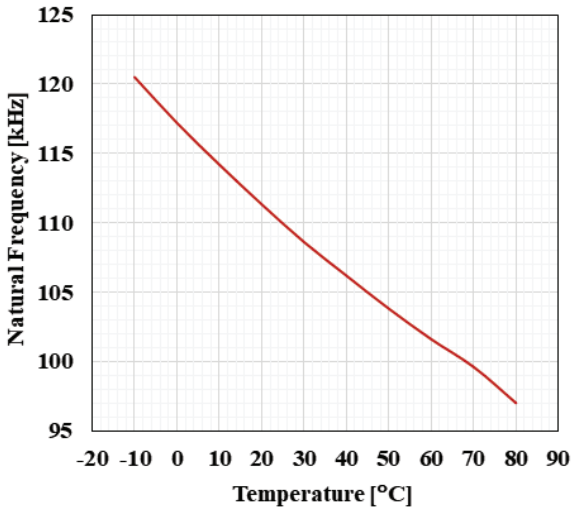


Figure 26: Natural frequency variations of the BP filter versus temperatures.

was changed from 120.5 kHz to 97 kHz. Temperature stability has been investigated because BJT OTA was used in this case, better temperature stability will be obtained if CMOS OTA was used.

The proposed quadrature oscillator was also evaluated by SPICE simulation and experiment test using commercial OTA LM13600. The parameter was set similar the case of universal filter. Namely, the supply voltages were V_{DD}= -V_{SS} = 5 V and the capacitances C_1 and C_2 were 2.2 nF. The measured output waveforms were taken using Tektronix MSO 4034 mixed signal oscilloscope (4-channel oscilloscope).

Fig. 27 shows measured output wave forms of V_{out1}, V_{out2} and V_{out3} when the circuit was designed as g_{m1} = g_{m2} = g_{m3} = g_{m5} = 1.512 mS (R_{ABC} = 47 kΩ) and g_{m4} ≅ 1.48 mS (I_{ABC} = 76.4 μA: R_{ABC} = 48 kΩ) was used for controlling the CO. The circuit generates the frequency of 96.7 kHz while theoretical value was 109.38 kHz, and the amplitudes were nearly equaled. The quadrature output form in Fig. 28 was verified through the XY mode. The quadrature relationships between V_{out1} and V_{out2} and between V_{out2} and V_{out3} were shown in Fig. 28, (a) and (b), respectively.

The experimental result of the FO by changing the value of transconductances g_m (g_m = g_{m1} = g_{m3}) was shown in Fig. 29. From this figure, when the transconductances g_m was changed as 0.481 mS (R_{ABC}=150 kΩ), 0.873 mS (R_{ABC}=82 kΩ), 1.512 mS (R_{ABC}=47 kΩ), 2.934 mS (R_{ABC}=24 kΩ), 5.81 mS (R_{ABC} = 12 kΩ), 8.45 mS (R_{ABC} = 8.2 kΩ), the FO was changed respectively as 32.7 kHz, 58.5 kHz, 96.7 kHz, 200 kHz, 395 kHz, and 580 kHz. The theoretical value has been used to compare the experimental result.

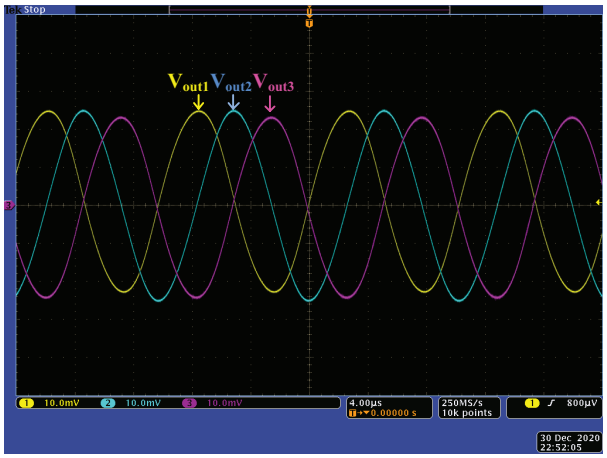


Figure 27: The experimental of quadrature outputs V_{out1}, V_{out2}, V_{out3}.

The plot for amplitude versus FO was shown in Fig. 30. Compared with Fig. 17, it should be noted that when g_m (g_m = g_{m1} = g_{m3}) was varied far from 1.512 mS (lower and higher from 1.512 mS), the amplitude of V_{out1}, V_{out2} and V_{out3} will be changed. The amplitudes of V_{out1} and V_{out2} will increase while the amplitude of V_{out3} will decrease when the FO was increased. If the constant amplitude of output signals was required, it can be obtained using the amplitude-automatic gain control (AGC) circuit [57]. The THD of output signals V_{out1}, V_{out2} and V_{out3} was plotted and shown in Fig. 31. It should be noted that large amplitude of output signal will be suffered from high THD. Fig. 32 shows the phase error that outputs between V_{out1} and V_{out2}, between V_{out2} and V_{out3} deviated from 90° phase different.

(a)

(b)

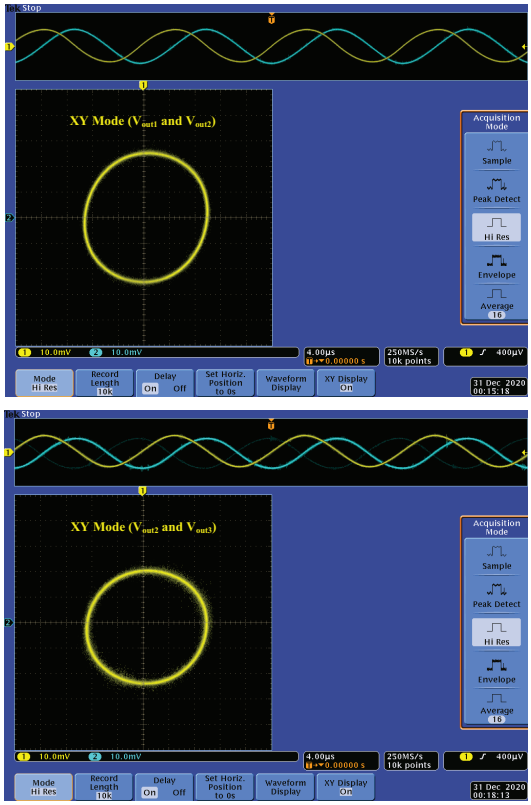


Figure 28: Lissajous pattern: (a) V_{out1} and V_{out2} outputs, (b) V_{out2} and V_{out3} outputs.

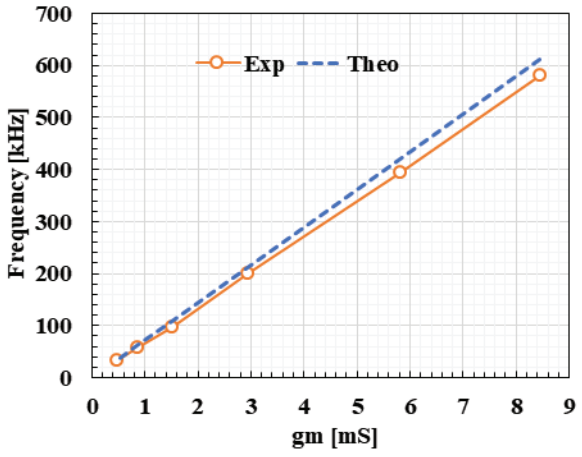


Figure 29: The frequency of oscillation against transconductances g_m.

5 Conclusions

In this paper, a new programmable voltage-mode universal filter and quadrature oscillator using five single output OTAs and two grounded capacitors is presented. The circuit uses analog switch to program either a universal filter or a quadrature oscillator. When the circuit performs function as filter, it is a four-input single-

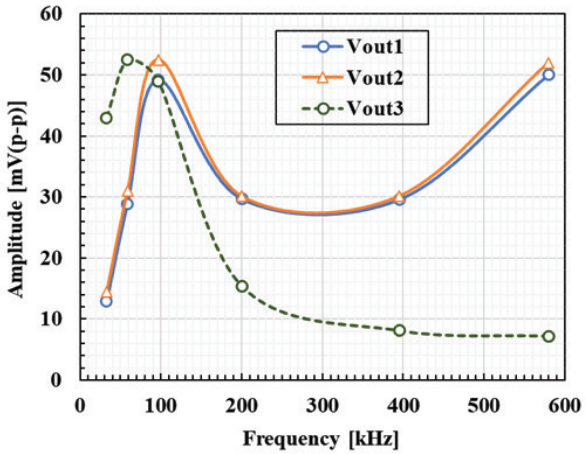


Figure 30: Output amplitude against the frequency of oscillation.

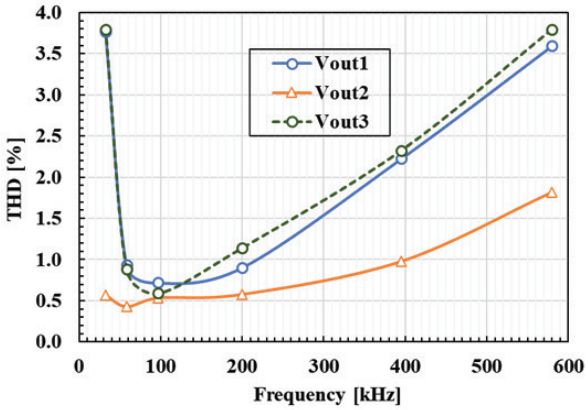


Figure 31: THD as a function of frequency of oscillation.

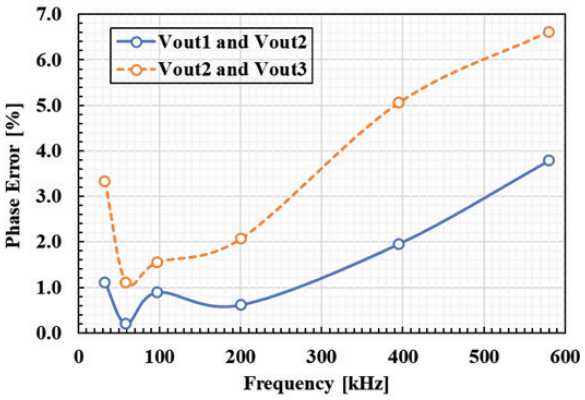


Figure 32: Phase error as a function of the frequency of oscillation.

output universal filter that can be realized LP, BP, HP, BS, and AP voltage responses by applying the input terminals appropriately at high input impedance. The natural frequency and the quality factor can be controlled electronically and independently by adjusting the bias currents of OTAs. Neither component-matching con-

ditions nor inverting-type input signals is required for obtaining five standard filtering functions. When the circuit works as quadrature oscillator, it is a three-phase quadrature oscillator that the condition and frequency of oscillation of oscillator can be independently and electronically controlled. The proposed structure is realized based on single output OTAs which is easily implemented in both as commercially available ICs as OTAs and CMOS as IC forms. The functionality of the proposed circuit is confirmed by SPICE simulation and experiment test.

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Modeling of Power Module for 48 V High Power Inverter

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Abstract: The paper presents simulation and measurement results of high current three-phase inverter power modules used in 48 V motor applications. Firstly, FEM (Finite Element Method) is used to extract circuit parasitics. With the inclusion of MOSFET and parasitic component SPICE models, a highly accurate simulation model is created. Switching characteristics of the power modules are simulated at 300 A load current and 48 V battery voltage. Thermal simulations estimate maximum transistor temperatures at given power losses. Electrical simulations are compared to actual measurements under identical test conditions. The comparison shows good matching between simulations and measurements. The phase voltage rise and fall times are the same in simulations and measurements. The overshoot voltages are also the same in both cases, at around 28 V. The mismatch can be found in the currents of secondary loops. The gate voltage signal is similar with small mismatch of Miller plateau voltage, due to transistor model parameters mismatch.

Keywords: power module; FEM analysis; thermal analysis; MOSFET

Modeliranje močnostnega modula za 48 V pretvornik visokih moči

Izvleček: Članek predstavlja načrtovanje, rezultate simulacij in meritev trifaznega močnostnega modula za velike tokove, ki je uporabljen pri 48 V motorskih pogonih. Najprej je uporabljena metoda končnih elementov (FEM) za izračun parazitnih elementov vezja. Z vključitvijo SPICE modela MOS tranzistorja in parazitnih elementov v model je nastal visokoločljivostni simulacijski model. Preklopne karakteristike so simulirane pri 300 A bremenskega toka in 48 V baterijske napetosti. Termične simulacije prikažejo največje temperature tranzistorja pri določenih močnostnih izgubah in nam podajo termično upornost tranzistorja do hladilnika. Narejena je tudi primerjava električnih simulacijskih rezultatov in dejanskih meritev, ki pokaže dobro ujemanje med njimi. Časa vzpona in padca fazne napetosti sta v primeru simulacij ter meritev enaka. Vrh preklopnega prenihaja je v obeh primeru enak 28 V. Slabše ujemanje je le pri sekundarnih tokokrogih, kjer se v simulacijah pojavi tudi rahli fazni zamik. Potek napetosti vrat je podoben, z manjšimi odstopanji napetosti Milerjevega platoja, zaradi odstopanja modela tranzistorja.

Ključne besede: močnostni modul; FEM analiza; termična analiza; MOSFET

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1 Introduction

Power modules are already well-known parts of all electric motor drives [1]. They work as an interface-inverter and supply the high current required for the operation of electric motors. The requirements for high voltages and high currents are constantly increasing, as high-power motors are needed for all sectors of industry, especially for transportation [2]. The demand for high voltage drives originated in battery-powered motor vehicles, where voltages reach 600 V and above [3]. Normal electric motor drives start at 12 V where automotive applications in vehicles use 12 V auxiliary drives to optimize vehicle performance [4]. The next interesting voltage level is 48 V, where it is the limit for low voltage systems. The parts of the 48 V system are inexpensive and the electrical architecture sits alongside the car's original 12 V system [5].

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The inverters for drives can use different switching electronic components such as silicon MOSFETs [6], SiC transistors [7], IGBT transistors [8], and so on. Each of these switching components has its own advantages and disadvantages. For the lower voltage domain where maximal voltage is 60 V, silicon MOSFET transistors are the right choice for a good price-performance ratio. One of the main issues, besides efficient driving of the inverter stage is also heat dissipation. The cooling system in motor drives can be of various types [9] and can further complicate the assembly and increase final system cost.

In the second chapter of the paper, the design of a 48 V three-phase motor drive, using MOSFETs as switching devices is presented. The third chapter presents power module modeling and parasitics extraction. It continues with thermal and electrical simulations. The paper concludes with the final chapter where a comparison is made between simulations and measured results performed on the prototype system.

2 Design of power module

2.1 Power module

A power module is a part of a three-phase (3P) 48 V Permanent Magnet Synchronous Motor (PMSM) inverter. It is designed to drive a motor with continuous power of 12 kW, maximum peak power of 20 kW and peak current of 600 Arms. Figure 1 shows the cross-section of a module mounted on a heat sink.

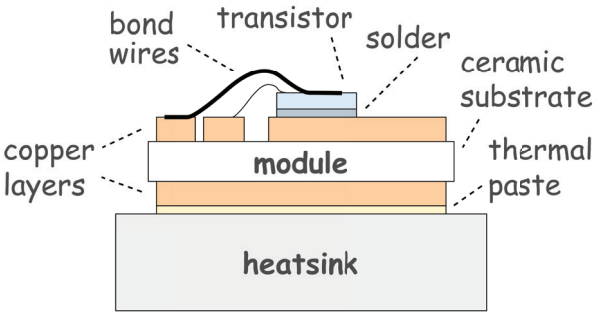

Figure 1: Power module cross section with all important elements annotated. Figure also represents module thermal structure.

Because of high currents and considerable power losses, the circuit is implemented on a ceramic substrate that gives the module a good heat conduction characteristic [10]. The ceramic substrate is a multilayer structure with a 500 µm thick Al_2O_3 (alumina) base and 300 µm copper plating on both sides. The bottom side of the ceramic module is attached to the heatsink via a thin thermal paste layer and additionally glued to the surface with nonconductive adhesive as shown in Figures 1 and 2.

In Figure 2, a gold-plated module is shown with bonded power transistors, capacitors and required gate resistors. High power switching is done by 100 V bare die MOSFET transistors in half-bridge configuration. For increased current carrying capability, four transistors are connected in parallel [14, 15]. Transistors are soldered to wide copper traces with their bottom side (drain) and are connected appropriately to other module connections by aluminum bonds from the top side (source).

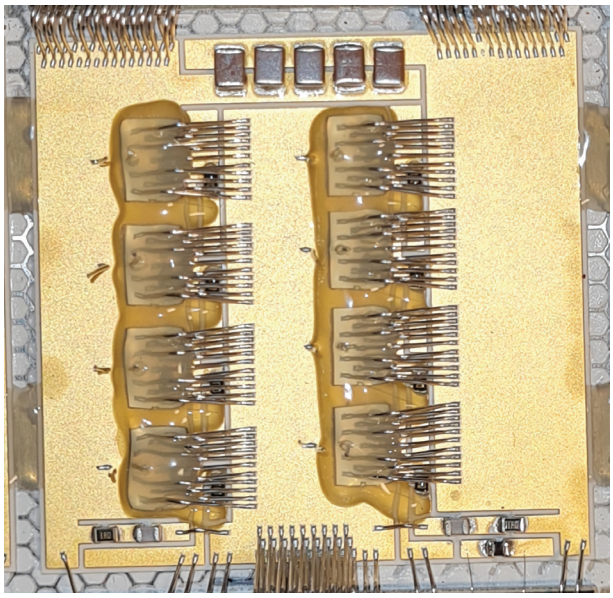

Figure 2: Module top view with 8 bonded transistors.

There are two types of bonds-main high current bonds with 380 µm diameter for source bonding and thin 50 µm gate signal bonds. Additionally, each transistor has its own individual gate resistor to minimize parasitic oscillations, provide the necessary damping and gate decoupling [15]. Module connections to other necessary circuits such as DC-link capacitor plate and driver module are also implemented using thick 380 µm bond wires. Any unwanted drain-source ringing is suppressed by RC snubbers, while onboard ceramic capacitors provide decoupling for high frequency switching transients [18]. An NTC thermistor is also mounted on the module board to monitor the temperature.

2.2 Layout

The board layout design enables three of the power modules to be placed side by side, forming a full 3P inverter power stage. The modules are connected to the power supply leads and capacitor plate on the upper side and

driver board from the bottom side of the 3P system. The capacitor plate is bolted to the busbar for an electrical connection to the power modules. Connections from battery terminals to capacitor plate are done from the top. Phases are connected from the bottom, where the motor is stationed. They are not included in Figure 3, as they can change with application. The geometric limits are the main constraint for power MOSFET placement and parasitics minimization as shown in Figure 3. For this reason, the MOSFETs are placed on rectangular baseplates, as this is the simplest and most intuitive solution, as already shown in Figure 2. The main parasitic components that most affect driver operation are inductances. They are minimized by reducing the loop sizes of the module current paths and maximizing the number of bond wires for all high-power interconnects [16].

The parasitic capacitances were not studied precisely as they are in the range of 10 pF to 100 pF, according to simulations, and do not affect the final module operation, as their value is much smaller than for instance MOSFET input capacitance, which is in the range of 10 nF. Moreover, adding parasitic capacitances in our case hardly affects the switching performance in the simulation. Therefore, the parasitic capacitances are considered as less important and are neglected; a similar approximation is also taken by other authors [17].

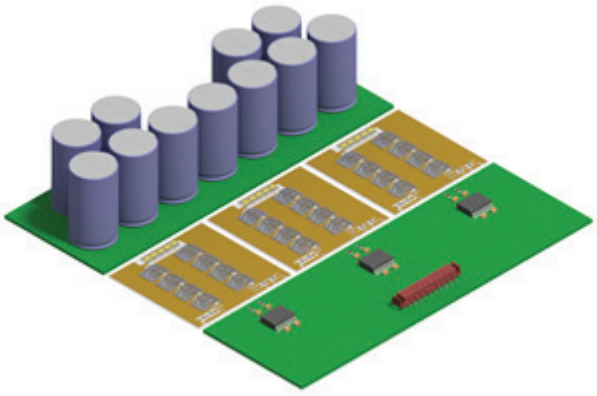

Figure 3: Proposed basic layout of the system (on upper side capacitor plate and at the bottom side controller plate). Connections to the battery and motor terminals are excluded from the image.

3 Simulations

3.1 Modeling

The power module is designed using Autodesk Inventor 3D CAD software. All details from the placement of the components to the shapes and connection geometries are modeled. Therefore, the used 3D model closely represents a real power module. The Ansys Q3D simulation software utilizes represented geometry model and extracts its parasitic circuit structure. The Ansys model is shown in Figure 4. For the simulation purposes, only parasitic resistances and inductances are extracted, capacitances are neglected. This parasitic circuit is used in combination with PSpice models of remaining module components to form a general level 3 [17] simulation model, used in Ansys Twin Builder. In addition to the module model, parasitic circuits of the driver and capacitor boards are also extracted and used.

The module is 47.5 mm wide and 46 mm long. The total 3P system is 103 mm wide. These are optimized dimensions that allow modularity and just enough room for transistor soldering and bonding. The width of the on-module connection traces for gate and electronic components connections are also optimized, not to influence the circuit performance. The typical trace width for the gate connection is 1 mm. Other connections are wider.

Figure 4 presents the Ansys model, including copper, bonds and solder pads, which all influence parasitic components. The MOSFET transistor die models are obtained from the manufacturer's packaged device electro-thermal model [19]. The original packaged device model is adapted by removing the package pins, internal bond wires and lead frame. Their resistances and inductances are removed from the model. Therefore, only the transistor die model remains.

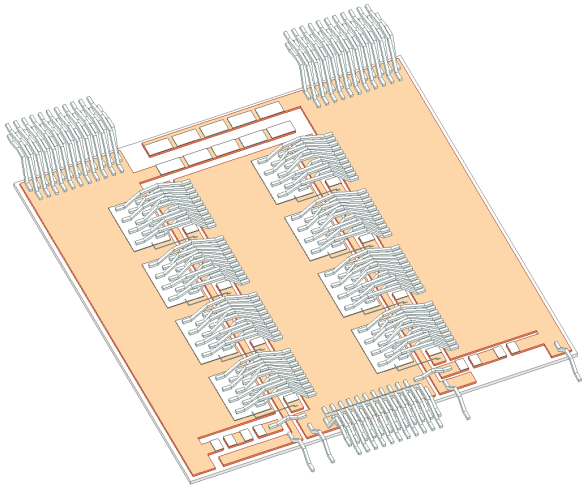

Figure 4: The Ansys Q3D module model, with all passive and active elements removed.

The thermal circuit of the bonds and lead frame are also removed so that the transistor can be simulated at constant junction temperature. The electrical behavior of the transistor is simulated in PSpice. Static and dynamic simulation results match the datasheet parameters.

Passive component parameters are obtained from the original manufacturer's Spice models, datasheets and some from similar measured components. Models for the module-mounted capacitors and DC link capacitors include series parasitic resistances, inductances and capacitances provided by manufacturers, while resistors are modeled as series RL circuits with typical package inductance values [17]. The transistor driver output stage is also obtained from the manufacturers PSpice model. In simulations performed, the gate driver peak currents match calculated values, therefore the gate driving circuit is correctly modeled.

3.2 Electrical simulations model

Parasitic circuit extraction is done at DC for the resistive part, so that circuit steady-state conditions are modeled correctly. Higher frequencies are used for inductive part extraction, so that a good approximation for fast switching transients is obtained [17]. Typical extracted values of parasitics are shown in Table 1.

Table 1: Typical self-inductances.

Lsl, Lsh	5 nH
Ldl, Ldh	2.5 nH
Lcap-, Lcap+	15 nH
Lcer	0.6 nH
Lel	7.5 nH
Lcable-, Lcable+	300 nH

The labels used in Table 1 correspond to the elements drawn in Figure 5. The parasitic extraction also calculates mutual coupling. The method firstly removes all active or passive soldered components from the model, so only basic metallic structure remains (see Fig. 4). To each net, a common sink connection is assigned, like a common surface at the *Vbat+* or *Vbat-* bonds. Nodes of transistors, capacitors and resistors are presented as sources. Together they form a net of connections with different parameters. For each separated connection in the net, Ansys Q3D calculates individual and coupled parasitic parts. Coupled inductances are also calculated between source-sink pairs of different nets. The frequency at which parasitic inductances are extracted is experimentally determined and corresponds to the highest signal frequency used in the circuit. The final result is obtained using frequency at which matching between measurements and simulation is highest. Initial simulations were done using the frequencies in the range of a few MHz [11], meaning typical switching times for MOSFET transistors [12] (see Fig. 9 and 10). The calculated inductances in this case are too small and the initial voltage overshoot is almost not visible. Decreasing the frequency in range of a few 10 kHz increases matching between the two results. The parasitic matrix, formed by Ansys is not presented as it includes a lot of nodes and does not clearly represent the parasitic mesh. The sum of important inductances is presented in Table 1.

Electrical simulations are focused on the inverter switching transients. For basic simulation, a simplified inverter model version is used. A 3P inverter is simplified to a single half-bridge power module. With this simplification, the simulation accuracy is not affected [13], but the total simulation time is considerably shortened. The DC capacitor plate and driver board parasitic models are fully included, as they were already designed and extracted separately for each phase.

The double pulse test (DPT) is used for simulation [13]. The DPT is a well-known test where the upper transistors of the inverter are turned off and the bottom transistors are driven by two pulses of different lengths. The expected load is connected to the output. Current value and the transient behavior are observed, subjecting transistors to worst case operating conditions without the need for prolonged simulations.

The circuit is simulated at 48 V battery voltage, motor load current of 300 A_{rms} and 25 °C transistor temperature. Bottom transistor gates are connected to gate driver driven by a voltage source. Top transistors are connected in body diode configuration, meaning in the off state. The simulation schematic is shown in Figure 5.

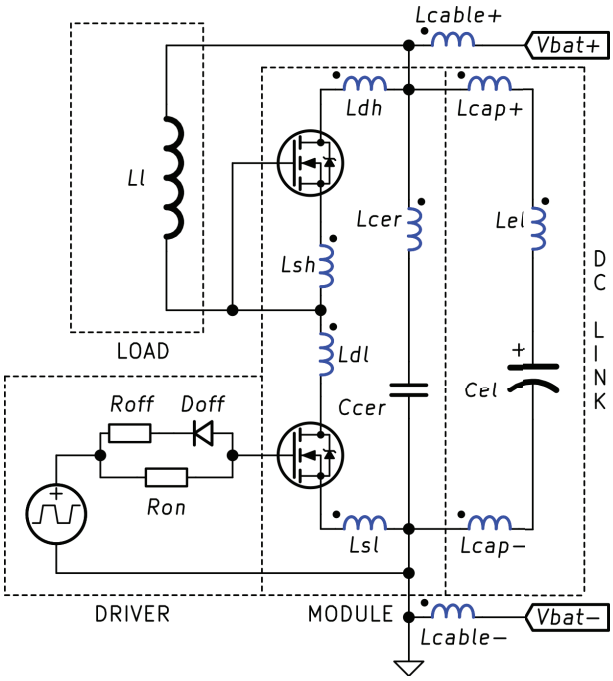

Figure 5: Simplified simulation schematics.

All parasitic inductances in the circuit are marked with a blue inductor symbol and dot showing the relative magnetic field polarity for mutual coupling. Their values are presented in Table 1. As can be noticed, also inductance of cables and bonds are considered. The inductive load is connected from the middle point (phase connection) to the positive battery connection. The simulation results are shown and discussed the in simulation-measurement comparison chapter.

3.3 Thermal simulations

The ceramic power module is placed on the 10 mm thick aluminum plate, serving as a cooler, with thermal conductivity of 237.5 W/mK. The 100 µm thick interface material is thermal paste with thermal conductivity of 2.5 W/mK. Copper and alumina (Al2O3) thermal conductivities are 394 W/mK and 24 W/mK, respectively. The thermal model of solder and transistor consists of two blocks with thicknesses of 100 µm and 220 µm stacked one on top of another. Their thermal conductivities are 63 W/mK for solder and 130 W/mK for silicon MOSFETs [12].

With such a power module model, the thermal simulations are performed, using Ansys Icepack program. The simulation result is shown in Figure 6, where thermal conditions are presented in the top view using a temperature scale on the left.

The aluminum plate bottom surface is maintained at a constant temperature of 65 °C. Module maximal temperature of 85 °C is reached in the middle of transistors where cooling is least effective.

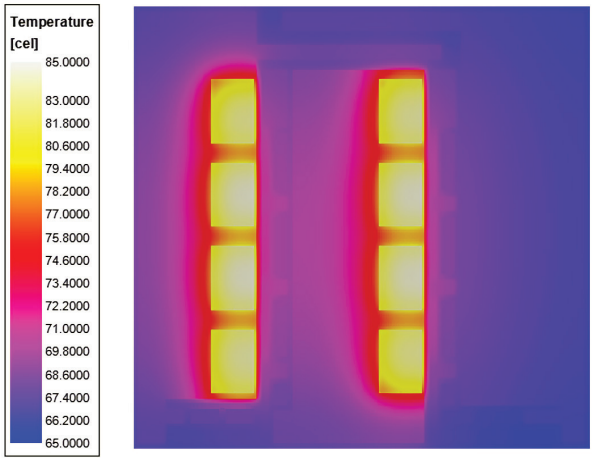

Figure 6: Module temperature conditions simulated in Ansys Icepack. Total module power loss is 200 W or 25 W per transistor.

The system thermal resistance R_{th} can be determined by the equation:

$$R_{th} = (T - 65°\mathrm{C}) / P \quad (1)$$

where T is maximum transistor temperature and P is module power loss. Calculated R_{th} at several power conditions is shown in Table 2.

Table 2: Maximum transistor temperature in relation to dissipated power.

P [W]	100	150	200	250	300	350
T [°C]	74.3	79.0	83.7	88.4	93.0	98.0
Rth [K/W]	0.093	0.093	0.094	0.094	0.093	0.094

As can be seen in Table 2, the temperature linearly depends on the power dissipated, under given conditions. The thermal resistance is constant 93 mK/W. The temperature values reached are not critical; simulated dissipation on the module is around 200 W at 300 A current (transistor channel resistance is 1.7 mΩ, typically).

The obtained thermal data can be used in a heatsink design, which must be carefully adapted due to power loss data from electrical simulations.

Basic thermal measurements are also performed. The module is measured in the saturation region with constant current and voltage, so that the losses applied are more accurate. Measuring module losses while under real load would be difficult. Temperature is measured using two thermocouples, one fixed in the middle of the module and another 0.5 cm away from the edge, directly on the heatsink.

At the 100 W load, the measured temperature difference is 6 °C, which corresponds to the 0.06 K/W thermal resistance between the heatsink and the module. In a simulation, the middle of the module is heated to about 71.5 °C giving us thermal resistance of 0.03 K/W. The difference between the simulation and measurements can be attributed to several factors. After the module inspection, imperfectly applied thermal paste is thought to be the main cause for the difference.

4 Measurements

For the prototype measurements, a single phase module is tested, using an artificial load. The driver was designed and assembled by us and is capable of driving several different kinds of power transistors. In Figure 7 the measurement setup is presented. Setup includes Tektronix MDO4054C oscilloscope and TPP0500B probes for voltage waveform capturing. The load current is measured by the CWT1 Ultra-mini Rogowski current transducer. The Agilent 33500B is connected as a

double pulse generator to control low side transistors. The EA-PS 9080-60 T laboratory power supply generates 48 V for high power switching circuit, other low voltages needed for a driver board are generated using the GWinstek GPD-3303S DC source.

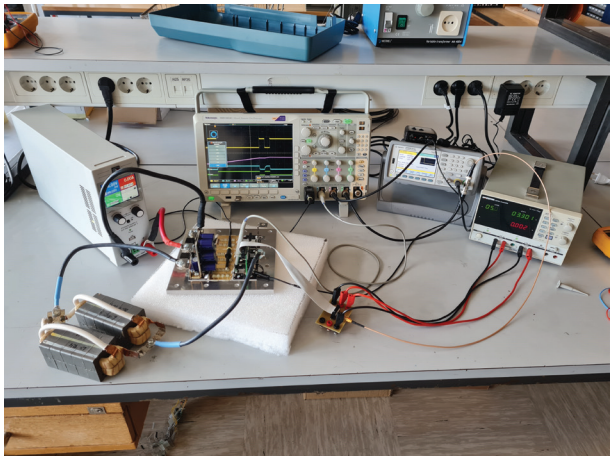

Figure 7: Measurement setup.

The signal generator was manually triggered. At trigger, a gate driver enables low side transistors for 500 us to energize the load coil and the current to reach 300 A. Then the bottom transistor is turned off for 25 µs, and again turned on for another 25 µs. Transistor turn-on and turn-off transients are measured during switching. They are measured directly on transistors. The typical signal curves and measurements results are shown in Figure 8. In Figure 8, on the first top trace, voltage drop on the fourth transistor channel from the module low side can be seen. This transistor is farthest from the power distribution and it suffers from the high parasitic influence on its behavior. Due to that fact, the transients on this transistor are high and greatly expressed. At the first turn on, there are no overshoots due to no current present, but when transistor is turned off, the

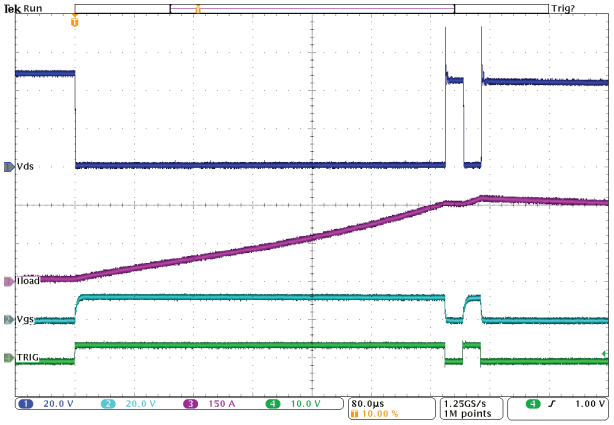

Figure 8: Measurement results - V_{ds} of the fourth transistor, load current, V_{gs} and double pulse trigger as the last waveform.

spikes and "ringing" can be detected. In the next trace, the current through the load is shown. After turn on, current linearly rises up to 300 A and then drops for a bit in off time and then again rises for another 30 A on the second turn on, yields final 330 A of current. The third trace presents V_{gs} signal – transistor control signal with rounded pulse shape in transients – typical RC shape, influenced by the gate resistor and the transistor's C_{gs}. Also, the different shapes and duration of a rise and fall time can be observed. This is due to the different current driving defined by R_{on} and R_{off}. The last trace presents the generator pulse on circuit input.

5 Comparison

In this chapter, simulation and measurement results are presented and discussed. All results shown are valid for the fourth bottom transistor as it is one of the active devices in DPT. The time scales of the top and bottom subgraphs in Figures 9 and 10 are aligned. In Figure 9, V_{gs} and V_{ds} transitions are shown, at full load of 300 A. Figure 9 in the top window, presents the transition of the V_{ds} voltage when the transistor switches on. There are no deviations between simulated (dashed line) and measured results – the voltage drops from 48 V to approx. 0.55 V in 0.8 µs. The V_{gs} transition in the bottom window is not so smooth due to the parasitic capaci-

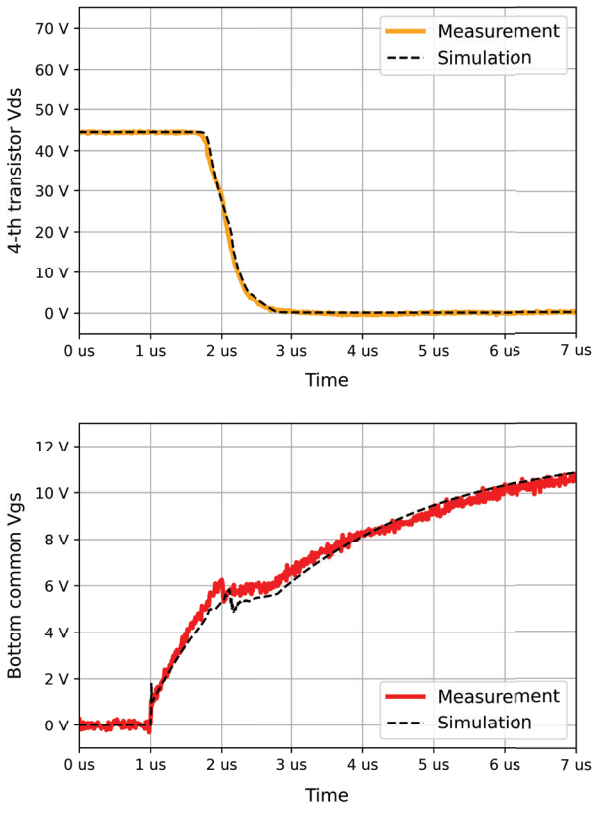

Figure 9: Comparison of V_{ds} and V_{gs} results at turn-on.

tances, and it consists of three parts. First, the voltage V_{gs} starts to rise and when a threshold V_{th} is reached, V_{ds} starts to discharge C_{gd} into the gate. This is the time when V_{gs} is constant in the middle of the rise transition – it is called Muller plateau. When the gate capacitance C_{gd} is fully discharged and the V_{ds} is almost zero the V_{gs} continues its rising to the full value. There is a small discrepancy between simulation and measurement – the Muller plateau is a bit higher, which means that a threshold value is a bit different in simulation; nevertheless, its duration is the same that means the capacitances in the model are correct. Also, C_{gd} is a nonlinear function of V_{ds}, but in this case V_{ds} was the same for the simulation and for the measurement.

Figure 10 presents the same two voltages at the turn off moment. At that time when 300 A current is flowing through the load and transistors, the loop is disconnected. It must be emphasized that this transition is done with a different gate current value, due to the changed gate resistance. The current is higher and turn off occurs faster. We start at the bottom graph, where V_{gs} is presented.

After a 1 µs delay, the V_{gs} is turned off. As can be noticed it starts to fall quickly – discharging the C_{gs}, till Muller plateau is reached. Then the C_{ds} starts to discharge and when discharge is done, the transistor is turned off. The

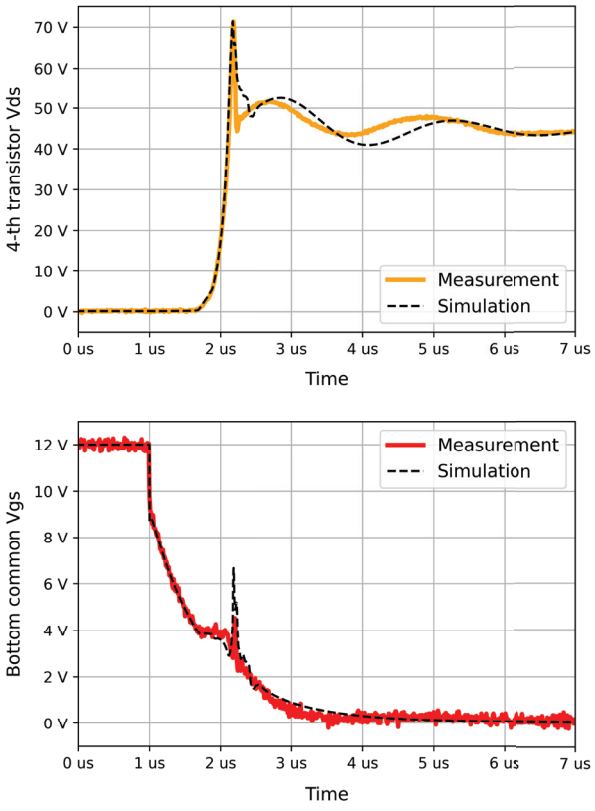

Figure 10: Measured and simulated waveforms compared. Turn-off at 300 A load current.

transient continues until C_{gs} is not discharged completely. The voltage V_{ds} jumps to 48 V at the moment, when C_{ds} is discharged, causing overshoot due to the huge amount of energy in the load and additional parasitic inductances of the system. The initial voltage overshot is suppressed by the DC capacitors mounted on the power module top side. After 28 V overshot, small oscillations can appear which are suppressed with the onboard snubber circuit. There is a bit difference in the simulated and the measured signal curve. The measured curve sharply declines, but the simulation shows a slight hump. Different parasitic inductances variations result in just a small shortening of the hump. Changes to transistor parameters also change waveforms. Usage of AC parasitic resistances instead of DC, decreases the hump but also lowers the initial spike. The lower frequency oscillations, after the overshot, are caused by the energy exchange between ceramic capacitors on the module and electrolytic capacitors placed on a bit remote board. The oscillations can be found also in the simulation results. The signal frequency and amplitude are almost the same.

From the results obtained, it can be concluded that the inductances and capacitances of the module were modeled correctly.

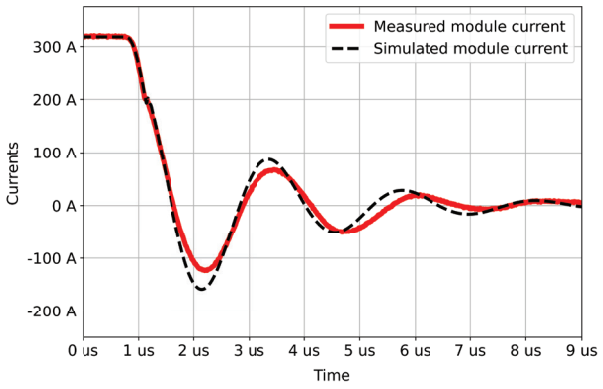

Figure 11: The $I_{Zdh} - I_{ce}$ current.

One of the interesting curves to observe is a total current from the module positive connection, shown in Figure 11. It can be noticed that at the turn-off moment, the transition is smooth. The overshoot in negative current is approximately 1/3 of the "ON" current and it matches well with the simulations. We can say that simulations predict a bit worse result as it is measured. The energy flow can be easiest presented with comparison of three main currents, shown in Figure 12.

It can be found that when the transistor is switched off, the necessary current deficit for the load comes from ceramic capacitors mounted on the module, and therefore satisfy the inductance request for slow current flow change. The oscillations then appear between different capacitors.

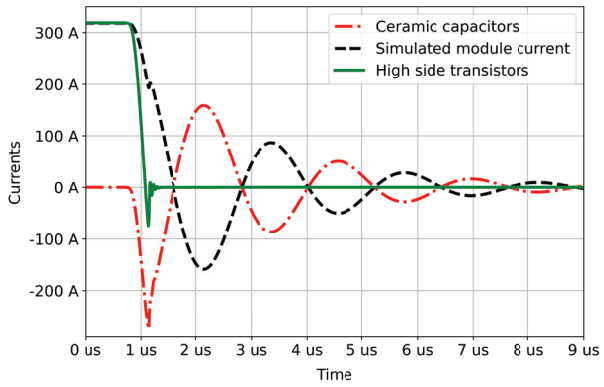

Figure 12: Current values at the on-off transition of module positive terminal, ceramic capacitors and transistors.

6 Conclusion

In the paper, power module design used in a high power motor inverter was presented. The main issue of the design flow is how to minimize parasitic components and include them correctly in the model to perform reliable simulations, which reflect in the correct system operation. The modeling chapter summarized the main steps for modeling and optimization of the model and minimization of parasitic components in a real board. The measurement setup presented main equipment used and explained the DPT test. The last chapter presented a comparison of measured and simulated results, which shows good main curve alignment and confirms values calculated and used in the inverter model. Both simulation and measurements give identical overshoot results of 28V. Small divination can be noticed only during secondary oscillations between different capacitors on the module and DC link caps. A gate-source voltage prediction mismatch only by a small amount due to MOSFET model inaccuracy. A presented model also gives good insight into circuit conditions that cannot be measured due to physical constraints.

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8 Conflict of interest

The authors confirm there are no conflicts of interests in connection to the work presented.

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Reduction of Random Dopant Fluctuation-induced Variation in Junctionless FinFETs via Negative Capacitance Effect

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Abstract: In this study, we investigated the impact of random dopant fluctuation (RDF) on junctionless (JL) fin field-effect transistors (FinFETs) with ferroelectric (FE) negative capacitance (NC) effect. The RDF-induced variations were captured by using built-in Sano methodology in three-dimensional technology computer-aided design (TCAD) simulation. Compared to the regular JL-FinFETs, the variations in JL-FinFETs with NC effect (NCJL-FinFETs) was observed to be less via statistical Monte Carlo analysis, which further enhanced its performance as well. The evaluation and estimation of threshold voltage (V_T), ON-state current (I_{on}), OFF-state current (I_{off}), and subthreshold swing (SS) by different FE layer thicknesses indicated reduction in the standard deviations of VT (δV_T) and Ion (δI_{on}) by 34.7% and 7.08%, respectively; the OFF-state current and its standard deviation shrank by approximately three orders of magnitude than the JL-FinFET counterpart. Although δSS was not monotonous, the SS was significantly improved to sub-60 mV/decade. To sum up, the regular JL-FinFETs containing the FE layer as NC effect not only improved the electrical performance, but also led to the resilience of the RDF-induced statistical variability.

Keywords: Random dopant fluctuations (RDF); negative capacitance effect; junctionless FinFETs; Monte Carlo analysis

Zmanjšanje naključnih nihanj zaradi fluktuacije dopantov v brezspojnih FinFET-ih preko učinka negativne kapacitivnosti

Izvleček: V študiji smo raziskali vpliv naključnega nihanja dopantov (RDF) na brezspojne (JL) poljske fin tranzistorje (FinFETs) s feroelektričnim (FE) učinkom negativne kapacitivnosti (NC). Nihanja, ki jih povzroča RDF, so bila zajeta z uporabo vgrajene Sano metodologije v tridimenzionalni računalniško podprti simulaciji tehnologije (TCAD). V primerjavi z običajnimi JL-FinFET-i je bilo s statistično analizo Monte Carlo ugotovljeno, da so spremembe pri JL-FinFET-ih z učinkom NC (NCJL-FinFET-i) manjše, kar je dodatno izboljšalo tudi njihovo zmogljivost. Ocenjevanje in vrednotenje napetosti praga (V_T), toka v stanju ON (I_{on}), toka v stanju OFF (I_{off}) in pod pragovnega nihanja (SS) z različnimi debelinami plasti FE, je pokazalo zmanjšanje standardnih odklonov V_T (δV_T) in Ion (δI_{on}) za 34,7 % oziroma 7,08 %; tok v stanju OFF in njegov standardni odklon sta se v primerjavi s podobnimi JL-FinFET zmanjšala za približno tri velikostne rede. Čeprav δSS ni bil monoton, se je SS znatno izboljšal, in sicer na manj kot 60 mV/dekado. Če povzamemo, običajni JL-FinFET, ki vsebujejo plast FE kot učinek NC, niso izboljšali le električnih lastnosti, temveč so tudi pripomogli k odpornosti na statistično variabilnost, ki jo povzroča RDF.

Ključne besede: naključne fluktuacije dopantov (RDF); učinek negativne kapacitivnosti; brezspojni FinFET-i; analiza Monte Carlo

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1 Introduction

Over the years, fabrication of the field-effect transistors (FETs) with p-n junctions requires very steep doping concentration gradients between the silicon-bulk channel and source/drain (S/D) region [1-2]. Moreover, the formation of steep gradient p-n junction requires

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ultra-fast thermal annealing process, which greatly increases the cost budget of manufacturing of equipment. To avoid the difficulty of making such p-n junctions, junctionless field-effect transistors (JL-FETs) were introduced [3-5]. JL-FETs involve the identical concentration of a single doping species along the semiconductor region, which are easier to fabricate than the inversion-mode FETs (IM-FETs) [6]. JL-FETs have nearly ideal subthreshold swing (SS), extremely low leakage current and smaller mobility degradation [7]. For these reasons, JL-FETs recently received significant attention as a potential replacement of IM-FETs in the future. In addition, negative capacitance field-effect transistors (NCFETs), which are fabricated by drawing into the ferroelectric (FE) material behaving as a series of NC stacked on the gate of the traditional complementary metal-oxide-semiconductor (CMOS) devices generally possess a higher performance and lower power consumption [8-10]. Owing to the good compatibility of the doped HfO2 layer with conventional high-κ semiconductor technology, the NCFETs have great potential to realize ultra-low power consumption and high-efficient switching even for sub-3 nm technology node [11]. Therefore, JL-FETs with NC effect are considered as a promising candidate for fabricating next generation advanced CMOS devices in lower power application.

However, random dopant fluctuation (RDF) as one of the most concerned variation sources for ultra-small semiconductor devices with further scaling has shown that its impact on the JL-FETs is more serious than the IM counterparts due to the heavy doping of dopant atoms [12-14]. Investigation also reports that JL-FETs are more sensitive to RDF than IM-FETs in baseline doping levels in silicon-bulk channel [15]. In rencent years, many novel junctionless architectures have been published in reputed journals, like Nanowire junctionless FETs and Nano tube junctionless FETs [16-17]. Therefore, electrical properties variability of conventional JL-FETs induced by RDF is going to be a worthwhile concern when the device scales to the nanometer region with the total number of dopant atoms increasingly discretized.

Several works have demonstrated that the NC effect can improve the performance of RDF-induced variability for conventional IM-FETs as well as planar NCFET-based CMOS circuits [18-20]. However, the NC effect on RDF-induced variations in JL triple-gate fin-type FET (JL-FinFET) has not been understood profoundly yet. Therefore, we have focused on the deficiency for JL-FinFET with NC effect in this work. In addition, the impact of doped HfO2 as different FE layer thickness on NC JL-FinFETs has been investigated in detail.

2 Negative capacitance and device structure

In recent years, ferroelectric materials have gained a lot of attention in the field of semiconductors. It was the first time that Sayeef Salahuddin and Supriyo Datta [21] adopted the NC effect of FE layers stacked on the gate of IM-FET, which had the ability to break the fundamental lower limit of 60 mV/decade SS to reduce the power dissipation. Many experiments in NC effect have proved that it can achieve the Sub-60mV/dec SS and lower the power [22-23]. In this study, the structure of the FE stacked around the gate-oxide layer is depicted in Figure .1 (a). The NC and the internal gate capacitance of the body can be considered as the following equivalent circuit depicted in Figure .1 (b). The device parameters are listed in Table 1. Incorporating the Landau–Khalatnikov (L-K) theory of NC effect in FE materials with the JL-FinFET structure constitutes the NCJL-FinFET [24]. The dynamic of NC can be expressed using the L-K equation as shown in Eq. 1:

$$E=2\alpha P+4\beta P^3+6\gamma P^5+\rho\frac{dP}{dt} \quad (1)$$

where α, β and γ are intrinsic parameters for FE materials, and ρ is a constant viscosity parameter which relies on the amplitude of the applied voltage. The voltage across the FE capacitor ($V_{FE} = V_{GS} - V_{IN}$) versus charge can be computed using the L-K equation:

$$V_{FE}=(2\alpha Q+4\beta Q^3)\times T_{fe} \quad (2)$$

where T_{fe} represents FE thickness, and Q is the surface charge density. α and β are Landau coefficients related to L-K equations and can be calculated by adapting the FE Q-VFE characteristics to obtain the existing values of remnant polarization P_r and coercive field E_c. In this study, P_r = 5 μC/cm² and E_c = 1 MV/cm were adopted in the HfO2-based FE material [25]. Based on this, we obtained $\alpha = -\frac{3\sqrt{3}}{4}\times\frac{E_C}{P_r}$, $\beta = \frac{3\sqrt{3}}{8}\times\frac{E_c}{P_r^3}$ and γ = 0 [26]. C_{FE} is the FE capacitance and is defined by dQ/dV_{FE}. From Eq. (2), C_{FE} can be expressed as,

$$C_{FE}^{-1} = (2\alpha + 12\beta Q^2)\times T_{fe} \quad (3)$$

The total gate capacitance C_T for NC-JL-FinFET can be obtained by:

$$C_T^{-1} = C_{FE}^{-1} + C_S^{-1} \quad (4)$$

The equation of the inner gate voltage V_{IN} and Ferroelectric capacitance can be expressed by:

$$V_{IN} = \frac{|C_{FE}|}{|C_{FE}| - C_S} V_{GS} \quad (5)$$

The increased total gate capacitance was derived by the NC effect of the FE layer stacked around the gate, which amplifies the internal voltage.

Table 1: Device parameters of the baseline JL-FinFET

Device Parameters	Value
Fin Width	5 nm
Fin Height	15 nm
Gate Length	20 nm
Oxide Layer thickness	0.9 nm
Spacer Thickness	5 nm
Source/Drain Length	15 nm
Channel Length	30 nm
Doping Concentration	$1.0e^{18}cm^{-3}$-$1.0e^{20}cm^{-3}$

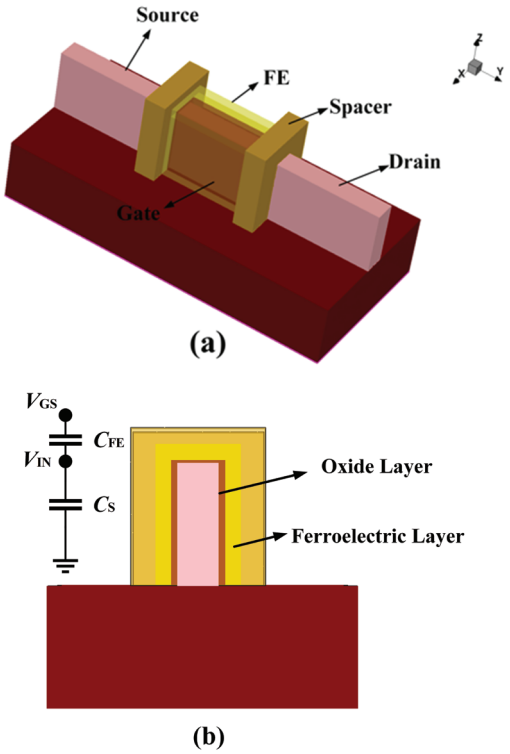

Figure 1: (a) Overall view and (b) lateral view of JL-FinFET.

3 Simulation scheme for RDF effect

To explore three-dimensional (3D) RDF effect on multiple thicknesses of the FE layer stacked around the gate of JL-FinFET, we utilized Sentaurus TCAD toolset, which contains 3D quantum correction (QC) drift-diffusion and QC Monte Carlo (MC) transport models, was employed for accurate mesh description [27]. The doping profile of the n-type NCJL-FinFET is depicted in Figure 2. We can see that the randomization of the arsenic atoms in the silicon-channel has been accomplished by built-in Sano method. The effect of randomization was supported by charge density theory. The doping profile was created using the following equation [28]:

$$\rho(r) = qk_c^3[\sin(k_c r) - k_c r\cos(k_c r)] \,/\, [2\pi^2(k_c r)^3] \quad (6)$$

where $k_C \approx 2n_{D/A}^{1/3}$ is the screening factor, and r is the radial distance from the center of the atoms, the $n_{D/A}$ represents the concentration of donors/acceptors. The Sano method adopts the above function to simulate the doping profile in the channel.

During the simulation, the drift diffusion was adopted in carriers' transport model based on the self-consistent solution of the Poisson equation. To prevent the disturbance of unphysical charge trapping and initiate further efforts to specify the nano-scale electronic devices with the short channel effect [29], the quantum mechanical effect was considered during the simulation of the NCJL-FinFET. The mobility model was incorporated with the high-field saturation and Shockley Read Hall physical model to accomplish the recombination and generation [30]. As a consequence of the time consumption of each randomization device, 200 randomization samples comprising varying doping profiles were reproduced. Subsequently, the overall statistical results of the RDF-induced variations in NCJL-FinFET were reproduced by the simulator.

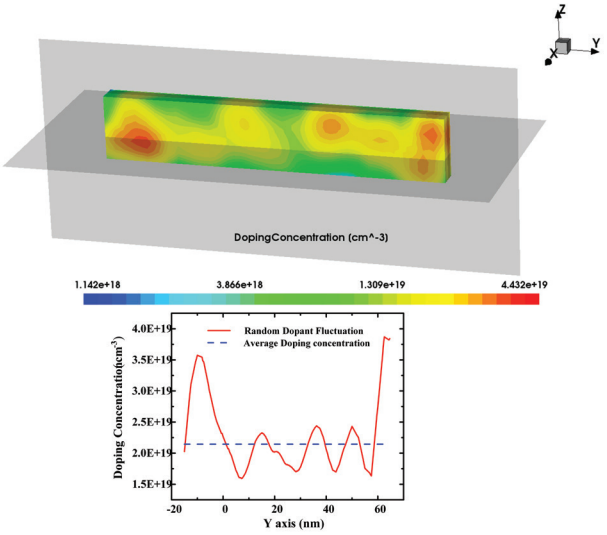

Figure 2: Randomized doping profile and structure of the n-type NCJL-FinFET.

4 Results and discussion

Figures .3(a)–(d) compare the ID-VG transfer characteristics of JL-FinFET without (T_{fe}=0 nm) and with (T_{fe} = 1, 2, 3 nm) NC effect (NCJL-FinFET) in uneven doping concentration levels at a drain biased voltage of 0.7 V. The normalized ID-VG curve was compared and calibrated with other published work. It can be observed that the OFF-state current (I_{off}) obviously decreases and ON-state current (I_{on}) slightly increases with the increase of the FE layer thickness. Due to the NC effect, the transport of the carriers in the silicon-bulk channel at low drain voltage (V_{DS}) was strongly controlled by the longitudinal electric field of gate voltage (V_{GS}) which is subject to the hysteresis in the NC region. In addition, it can be seen that the curve dispersion of randomly reproduced samples is gradually suppressed with the increment of the FE layer thickness; meanwhile the slop of the ID-VG curves gets slightly steeper. It can be computed that the switching current ratio (I_{switch} = I_{on}/ I_{off}) of the devices raises two orders of magnitude and becomes 400 times larger than that of regular JL-FinFETs. The I_{switch} can reach to 4.408e10 at T_{fe} = 3 nm. The huge I_{switch} contributes by the NC effect of the FE layer. However, for the standard deviation of I_{switch} (δI_{switch}), it represents the monotonic trends due to the OFF-state current being more vulnerable to the influence of the discrete dopant atoms. Therefore, JL-FinFETs with the NC effect exhibit more tolerance toward the transfer characteristics fluctuation induced by the RDF.

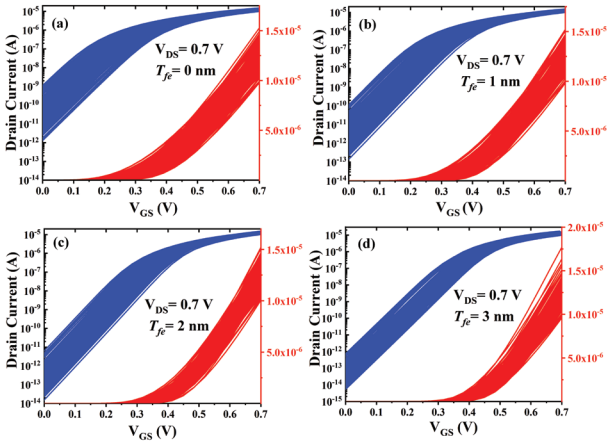

Figure 3: (a)–(d) ID-VG transfer characteristics of NCJL-FinFET with different thicknesses of ferroelectric layers

Figure .4(a) depicts the means of the threshold voltage (V_T) and subthreshold swing (SS) at a drain bias voltage of 0.7 V. We could observe that SS gradually decreases and VT gradually increases at T_{fe} less than 3 nm. However, an inflection point emerges in the curve when T_{fe} is approximately 3–4 nm. The appearance of turning point with an increasing Tfe attributes to the capacitance matching circumstance. Extremely thick FE layer leads to the capacitance mismatch effect because C_{FE} was derived by $2P_r/3\sqrt{3}E_cT_{fe}$ [31]. The perpendicular center-symmetry profile of the channel near the drain is gradually depleted over subthreshold region, which is modulated by the internal gate voltage. In addition, the threshold voltage requirement decreased at a certain range (T_{fe} = approximately 3–4 nm) due to the modulation of the perpendicular channel depletion. It can be concluded that V_T (extracted gate voltage at Id = 0.1 μA/μm) totally shifted towards the right in the coordinate system and its degree of dispersion became smaller. According to Figure .4 b, the V_{T1} (extracted gate voltage from the corresponding to the maximum slope) was positively correlated with V_T and V_{T1} increased rapidly because SS became steeper with an increase in the T_{fe}. Totally, the NC effect actually moderated the RDF-induced variations to the threshold voltage, and the performance of NC-JL-FinFET improved when compared to the regular JL-FinFET counterpart.

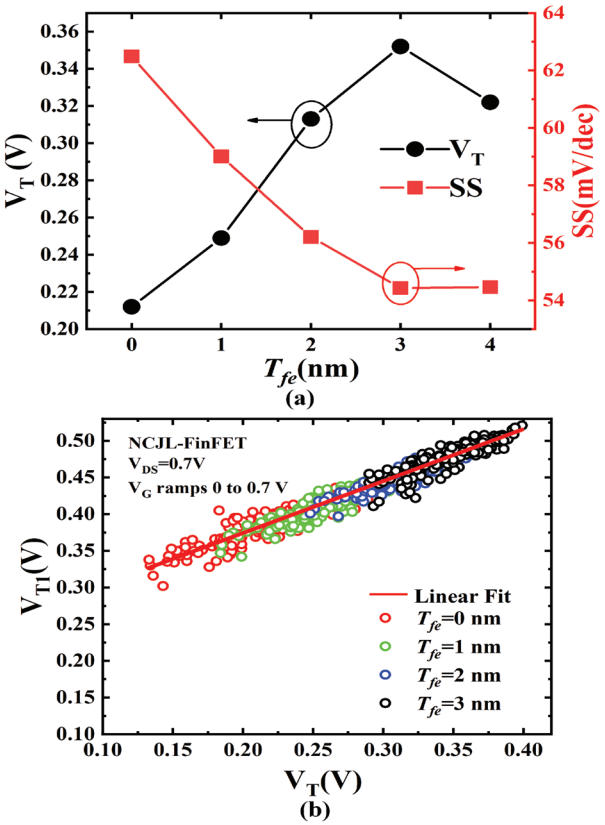

Figure 4: (a) Variation of threshold voltage with the thickness of ferroelectric layer and (b) The shift trend and dispersion between V_T (is extracted gate voltage at Id = 0.1 μA/μm) and V_{T1} (is extracted gate voltage from corresponding to the maximum slope) induced by the random doping in the 3D silicon-bulk channel of NCJL-FinFET.

Figures .5 (a)–(d) describe the expected normal value of the ON-state current and the simulation value of the

actual device model. Each simulation was performed at different particle concentrations, which was modeled via the actual manufacturing process in the TCAD tools flow. It is shown that the average ON-state current is increased from 12.4μA to 12.9μA. The average ON-state current is increased by 4.03% and the standard deviation of I_{on} (**δI_{on}**) is decreased to 7.08%. We could observe that the ON-state current fluctuation caused by the RDF upon the silicon-bulk channel was controlled by the NC effect. With an increase in the FE thickness, the expected values of the ON-state current became less than the actual values. This indicated that the ON-state performance improvement owed to the silicon-bulk channel and the drain/source region did not have the steep mutation particle species boundary. Compared to the JL-FinFET, its counterparts with the NC effect exhibited more immunity toward the impact of RDF in the saturation region.

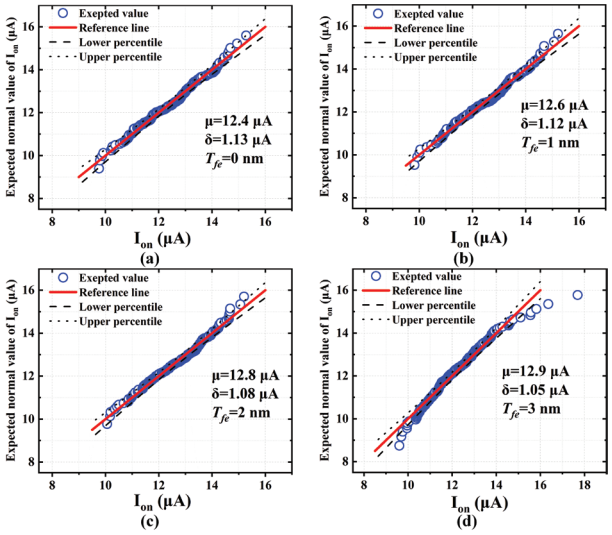

Figure 5: (a)–(d) Expected normal value of the ON-state current (I_{on}) and simulated value of the actual device model

The histogram of V_T distribution for each FE layer thickness at the drain biased voltage of 0.7 V is exhibited in Figures .6(a)–(d). The total dispersion of V_T presents a linear gaussian distribution. It can be observed that the fluctuation of V_T in the device with NC effect is to a small extent. As the FE thickness increases, the threshold voltage is least affected by RDF. The increase in the threshold voltage ensures the stability of the electrical characteristics of the device in the cut-off region because achieving full depletion would be easier if the gate control is enhanced.

In Table 2, it can be observed that mean value of SS among the random samples decreases slightly as the T_{fe} increases. Although the standard deviation of SS (δSS) is reduced, it did not exhibit a nonmonotonic trend all the time. The non-monotonic behavior of the impact of RDF on I_{on} originated from its strong attachment on the matching between FE capacitance and the internal silicon-bulk capacitance [32]. The OFF-state current (I_{off}) of the NCJL-FinFET gradually decreased by two orders of magnitude. Although the fluctuation in OFF-state leakage and threshold voltage were weakened compared to JL-FinFETs, the OFF-state current was actually more sensitive to the RDF in the silicon-bulk channel when compared to the IM transistors. Consequently, we found a monotonic suppression of I_{off} fluctuation with an increase in the T_{fe}

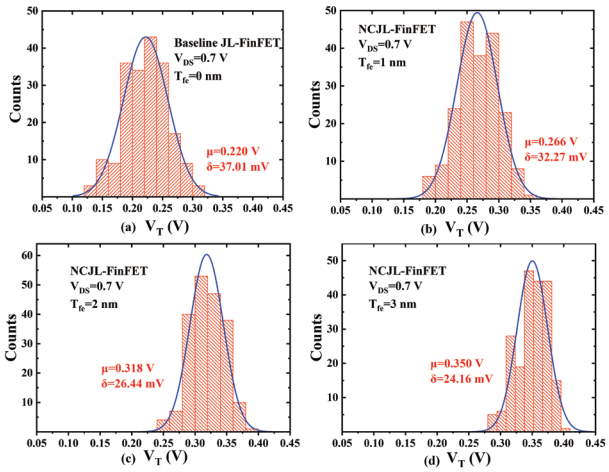

Figure .6: (a)–(d) Histogram of V_T distribution for each ferroelectric layer thickness (1, 2, 3 nm) and the baseline JL-FinFET at the biased drain voltage of 0.7 V

5 Conclusions

In this study, we investigated the impact of RDF on the conventional JL-FinFETs with NC effect. Through the

Table 2: Summary of statistical moments of the distribution of SS and Ioff at biased drain voltage of 0.7 V among the NC-JL-FinFET with different T_{fe}.

Tfe(nm)	SS(mV/dec)	δSS	δSS/SS	Ioff(A)	δIoff (A)	δIoff/Ioff
0	62.49	0.80626	1.29%	1.040e-10	1.881e-10	1.809
1	59.01	0.49307	0.84%	9.525e-12	1.670e-11	1.753
2	56.21	0.70523	1.23%	5.229e-13	8.308e-13	1.588
3	54.43	1.39964	2.57%	8.104e-14	1.154e-13	1.423

TCAD simulation, it can be concluded that the NCJL-FinFETs are more resilient toward the RDF-induced threshold voltage and OFF-state current variability. The significance of the resilience of the device counters against the total variability increases with respect to the increase in the thickness of the FE layer. Threshold voltage and subthreshold swing were not completely linear with the FE layer thickness related to the interaction between the capacitance mismatch effect and junctionless bulk-channel modulation. The leakage current of NCJL-FinFETs in the cut-off region were considerably smaller than that of JL-FinFETs. The increment of ON-state current was not evident in NCJL-FinFETs but also shows upward trend. The subthreshold swing decreased to 54.43 mV/dec, though no improvement was evident on this variation. On the whole, we have shown that there can be suppression of RDF-induced variability and performance enhancement of JL-FinFETs with NC effect, which also depends on the applied bias voltage and FE layer thickness.

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7 Conflict of interest

The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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Horizontal Crack Induced Vertical Crack Formation in Epoxy Mold Compound for Electronic Packaging

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Abstract: Epoxy mold compound (EMC) has been widely applied as the packaging material in the electronic industry. It is due to the unique property of EMC such as high temperature stability, low coefficient of thermal expansion (CTE), excellent electrical properties and manufacturability. Despite of superior properties of EMC, several failures have been reported regarding on the electronic packaging application such as crack on the body (EMC). Most of the research reported that the crack defect was originated from the moisture absorption. This research is intended to examine the phenomenon and effect of moisture absorption on the vertical and horizontal crack formation. A comparison between control and conditioned sample was studied where the conditioned sample was subjected to humidity chamber according to the Moisture Sensitivity Level 3 (MSL3) requirement. Horizontal crack occurrence was observed at the interface EMC. While vertical crack occurrence could be linked with the horizontal crack. Further analysis suggested that horizontal crack occurrence induced vertical crack occurrence. Thus, controlling moisture absorption pathway might minimize horizontal crack and prohibit vertical crack occurrence.

Keywords: BGA component; Epoxy Mold Compound; Horizontal Crack; Moisture Crack; Moisture Sensitivity Level 3; Vertical Crack

Formacija vertikalnih razpok zaradi horizontalne razpoke v epoksi zmesi za elektronsko embalažo

Izvleček: Epoksi zmes (EMC) se pogosto uporablja kot embalažni material v elektronski industriji. To je posledica edinstvenih lastnosti EMC, kot so visoka temperaturna stabilnost, nizek koeficient toplotne razteznosti (CTE), odlične električne lastnosti in možnost izdelave. Kljub odličnim lastnostim EMC je bilo zabeleženih več napak pri uporabi v obliki razpok. Večina raziskav je poročala o nastanku razpok zaradi absorpcije vlage. Namen te raziskave je preučiti pojav in vpliv absorpcije vlage na nastanek vertikalnih in horizontalnih razpok. Raziskana je bila primerjava med kontrolnim in testnim vzorcem, pri čemer je bil testni vzorec izpostavljen vlažni komori v skladu z zahtevami tretjega nivoja občutljivosti na vlago (MSL3). Na površini EMC je bil opažen nastanek vodoravnih razpok. Pojav navpičnih razpok je bil povezan z vodoravnimi razpokami. Nadaljnja analiza je pokazala, da je pojav horizontalno-talnih razpok povzročil vertikalne razpoke. Z nadzorom poti absorpcije vlage bi lahko zmanjšali vodoravno razpoko in s tem preprečili nastanek vertikalnih razpok.

Ključne besede: BGA zmes; Epoksi zmes; horizontalne razpoke; vertikalne razpoke; razpoka zaradi vlage; nivo občutljivosti vlage 3

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1 Introduction

Epoxy mold compound (EMC) is widely used as encapsulation materials in electronic packaging industry due to their excellent electrical properties and manufacturability. However, the reliability of EMC is a concern due to its hygroscopic in nature and has a high tendency to absorb moisture from the surrounding. At high temperature especially during the reflow process in the solder mount assembly (SMA), the absorbed moisture is rapidly vaporized and tend to exhibit 'pop-corning' issue [1]-[3].

The reflow soldering process is the most widely used method of attaching surface mount components to the printed circuit boards (PCBs) by first pre-heating the components, PCB and solder paste then re-melting the solder [4]-[8]. The temperature profile range during the reflow process is around 220 - 250 °C. The crack can be observed at high temperatures during the reflow process if the concentration of moisture within the EMC exceeds the critical value which occurs as an interfacial delamination. Several literatures have reported the crack between the mold compound and the substrate during solder reflow for various die sizes and molding compound thickness [9]-[12].

According to Groothuis, higher content of moisture may be absorbed in high glass transition temperature (Tg) material and ultimately contribute to explosive force during sudden heat [1]. The moisture that presents in the mold compound will vaporize during high temperature and stress the package. This stress induces the package to crack, which causes delamination between the mold compound and lead frame or die. In order to avoid an occurrence of this defect, the package can be baked before assembly to remove the moisture [2]. Lau reported that the crack exists at the early stage of reflow and not at the peak temperature of solder reflow. The initiation of the crack begins at the die corner due to the high stress concentrated. The baking condition for 24 h at 125 °C is considerably insufficient to bake out the whole absorbed moisture [3]. Most of the research on the crack formation of EMC was focused on investigating the moisture absorption, vaporization, and delamination deformation (loss of adhesion).

A comparison between relative humidity (RH) treated sample and without RH treated sample was studied where the RH treated sample was subjected to humidity chamber according to the Moisture Sensitivity Level 3 (MSL3) requirement. Ball grid array (BGA) component encapsulated with the EMC was used as the sample to investigate the orientation effect of the crack. Vertical and horizontal crack were observed and analyzed after running through the reflow process to understand crack formation inside EMC.

2 Materials and methods

EMC encapsulation components were used as the test samples with the size of 17x17x0.8 mm (WxLxt). The solder joint of the component was BGA and was mounted on the PCB. The EMC used was a commercially grade of electronic packaging. The EMC BGA component were subjected to the humidity chamber. The parameters of the chamber were set at 30 °C, 60 % RH for 168 h (Level 3-Moisture Soak Requirement) [13]. The weight of the component was measured using weight balance instrument (AND HR-250AZ) after humidity test. Subsequently, the samples were run through the manufacturing reflow oven (Pyramax150 12Z) using the actual reflow thermal profile with the maximum temperature of 250 °C. Comparatively, the normal EMC component without subjected into the humidity chamber were run through the oven together with the test samples.

The failure analysis was then performed on both samples. Prior to the analysis, the sample was i cold mounted using epoxy resin. About 50 mL resin was mixed with 8 mL hardener and was left at the ambient condition for 12 h to allow curing. Silicon carbide (SiC) grinding paper was used for mechanically grinding the component with the grit size of 180, 240, 600, 800 and 1200 sequentially. The final polishing was performed with alumina (Al_2O_3) powder (0.3 µm and 1 µm). The optical images were evaluated using ultra-high precision digital microscope (VHX-7000 Series) from Keyence. The samples were coated using platinum prior to Field Emission Scanning Electron Microscope (FESEM) analysis to minimize sample charging. The FESEM was performed on the Hitachi SU-8030 to analyze the horizontal and vertical crack. Meanwhile, the close-up observation of the EMC on top view and side view were captured from the cross-section analysis. The size and shape of the solder balls was investigated by GE Phoenix Microme 2D X-ray.

3 Results and discussion

3.1 RH moisture test

The weight of the component increased with increasing RH storage. The component weight gain from RH test was then analyzed according to percentage of moisture absorption as shown in Fig. 1. Apparently, the moisture content of the components increased linearly with time. This behavior indicated that EMC use this study was able to absorb moisture as typical hermetic package from the epoxy based polymeric material.

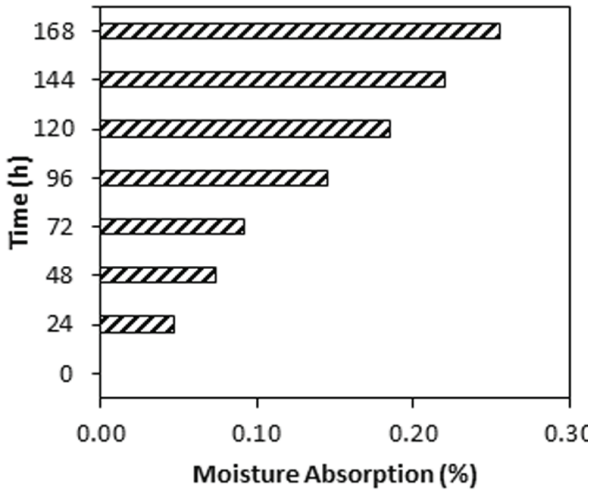

Figure 1: The moisture absorption of the samples at conditioning setting of 30°C/60%RH/168 h

3.2 Crack occurrence time frame

Figure 2a shows the micrograph of different size and location of solder ball from x-ray testing after reflow soldering process. The solder ball size was larger at the edge location and smaller at the middle location of the BGA. This condition might be contributed from uneven stress distribution throughout the component. From Fig. 2b, the solder ball at the middle showed slightly elongated than that of the edge. Interestingly, Fig. 2b also showed that vertical crack in the EMC appeared at the middle of the component. The elongation of the solder ball at the middle suggested that the time frame of the crack occurred during reflow process. During the reflow time, the high temperature induced the formation of crack and simultaneously, the BGA were re-melted. As a result, the solidified solder ball preserved the warping condition of the component.

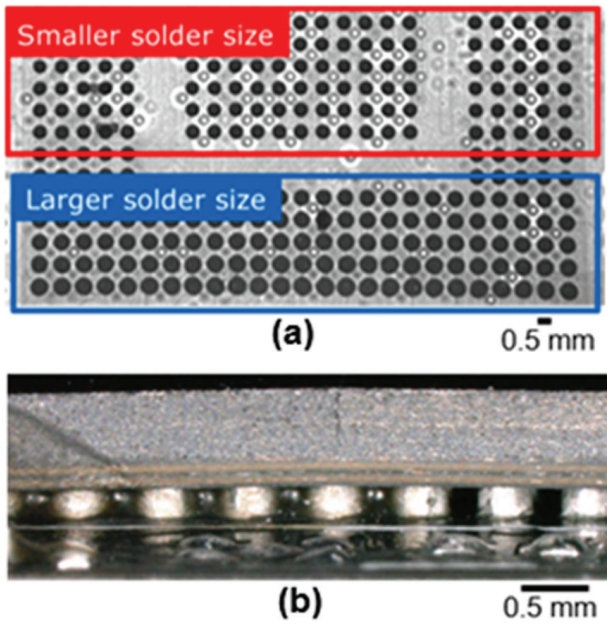

Figure 2: Micrograph of: (a) different size and location of solder ball from X-ray testing after reflow soldering process and (b) side view image of solder ball at the middle showing slightly elongated than that of the edge location

The warping condition of the component could be clearly seen in Fig 3 that signified the different ball shape pattern along the BGA component and its enlargement of the chosen solder ball. The locations of A, D and E were the solder ball at the edge while B and C w at the middle of the component. The balls at the A, D and E showed a compressed shape, meanwhile the B and C indicated an elongated shape with different sizes and shapes of the solder balls array in Fig 3 were corroborated further the evidence of the crack occurrence during the reflow process at high temperatures.

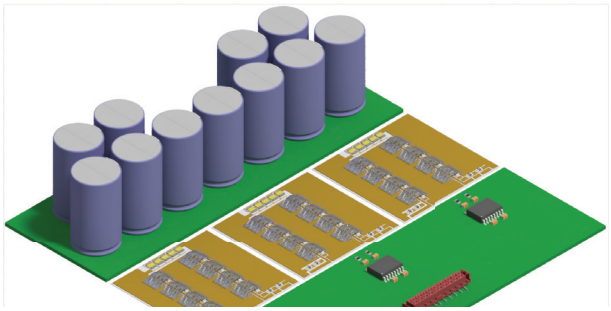

Figure 3: Cross-section of different solder ball shape along the BGA component the enlargementimages represented the compress and elongation solder balls condition

3.3 Vertical and horizontal cracks

Figure 4a and 4b show crack occurrence of the sample that was subjected to the RH testing at 30 °C/60%RH/168 h. Fig 4a shows horizontal crack on the EMC surface in the form of small line at the middle of the component. Whereas Fig 4b shows a side view image of the component with an indication of vertical crack at the middle. It was observed that the vertical crack was perpendicular to the line crack as shown in Fig 4b.

The formation of the crack was attributed to the 'popcorning' from the moisture absorption of the EMC [1]-[3], [11-12], [15]. During the reflow process, the temperature was raised above the glass transition temperature (Tg) of the EMC (ranging from 110 °C to 120 °C) to a temperature of approximately 220 °C or more with the heating rate of 2° c/sec, which was required to melt the solder. At high reflow temperature, the existing moisture inside the conditioned sample vaporized into a steam. The stresses due to the thermal mismatch

between the molding compound and the adhering materials led to the interfacial de-adhesion and followed by package cracking due to the steam pressure and hygroscopic swelling [15], [16]. This thermal stress and steam pressure cause the package to crack and resulted in a delamination between the mold compound and the lead frame or die [2].

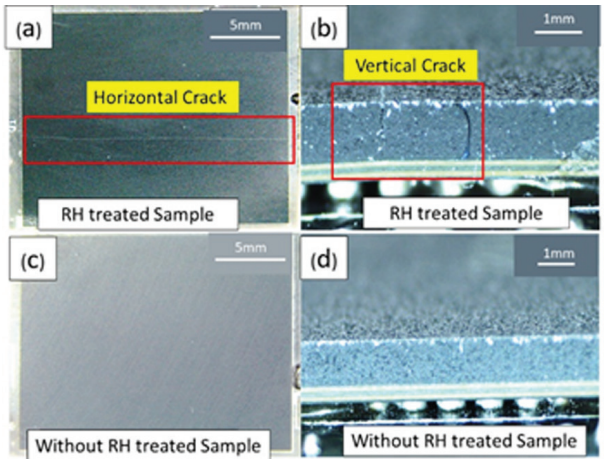

Figure 4: (a,b) Crack observed on RH treated sample and (c,d) no crack observed on non-RH treated sample

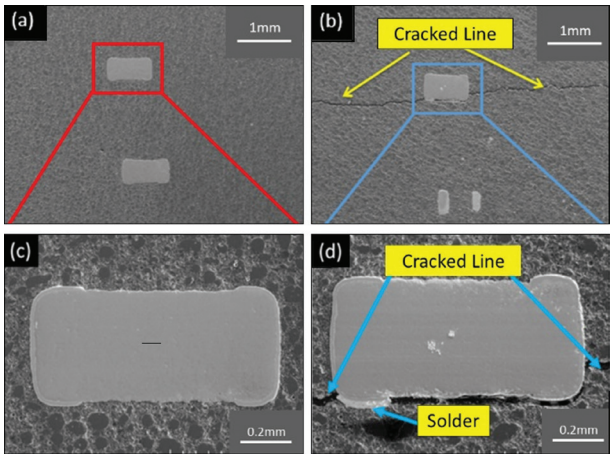

Figure 5: The SEM images of (a) top-down grinding of without RH treated sample (b) top-down grinding of RH treated sample (c) enlarged view of passive component of without RH treated sample and (d) enlarged view of passive component of RH treated sample

To have further understanding on the horizontal crack, the sample was ground from top until reaching the passive components. The path of the crack appearance was clearly observed alongside the passive component as shown in Fig 5b for the RH treated sample but not on the RH non-treated sample (Fig. 5a). Interestingly, Fig. 5d signified the abnormal existence of the solder at the terminal of the passive component (localized) alongside the crack line. It was highly anticipated that the existence of the micro-void at the passive component terminal led to this phenomenon. During the reflow process of the BGA component, the solder material of the passive component was re-melted for the second time and seeped through this micro-void pocket.

Furthermore, the existence of the micro-voids increased the tendency of the EMC to absorb moisture through non-Fickian diffusion [17]. The non-Fickian diffusion behavior was suggested due to the complex nature of the hygrothermal behavior of the polymer network. The moisture uptake may initially exhibit relatively rapid with constant diffusivity but can eventually slow down due to the variable diffusivity. The micro-voids would be a place where the moisture could be concentrated in the EMC. At the high temperature, the volatized concentrated moisture along the component might escape from the EMC rapidly and thus created the horizontal crack line.

Fig. 6 shows the schematic illustration to describe vertical crack phenomena in EMC whereby moisture ingression route originated from the edge of both side component. Fig. 6a shows that during RH testing, the moisture was moving in from both edge of the BGA component and trapped at the middle of BGA component. While Fig 6b illustrates a formation of crack during the reflow process. In general, reflow process involves high temperature, and the concentrated moisture trap induces high pressure at the middle of the BGA component. Then the moisture trap at the middle was vaporized to accommodate pressure distribution thus the resulted in a formation of vertical crack.

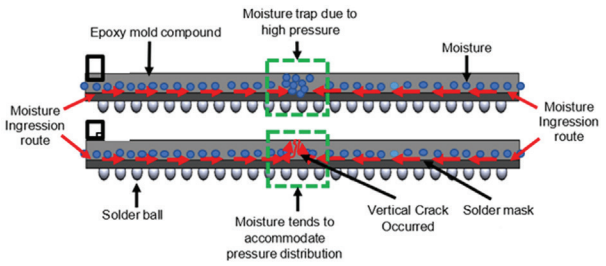

Figure 6: Schematic illustration to describe crack phenomena, (A) moisture ingression route and trap at the middle, (B) moisture tend to find possible route to accommodate pressure distribution

4 Conclusions

This current study successfully investigated the crack occurrence in term of horizontal crack and vertical crack. The horizontal crack appeared in the initial state that was due to moisture ingression route along with the

substrate from both edge and trap at the middle. Subsequently, the moisture moved up vertically, thus inducing the vertical crack formation, perpendicular to the substrate. The vertical crack was apparently signified from side view of the EMC BGA component.

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6 Conflict of interest

The authors declare no conflict of interest for this paper.

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- Nanoelectronics,
- Optoelectronics,
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