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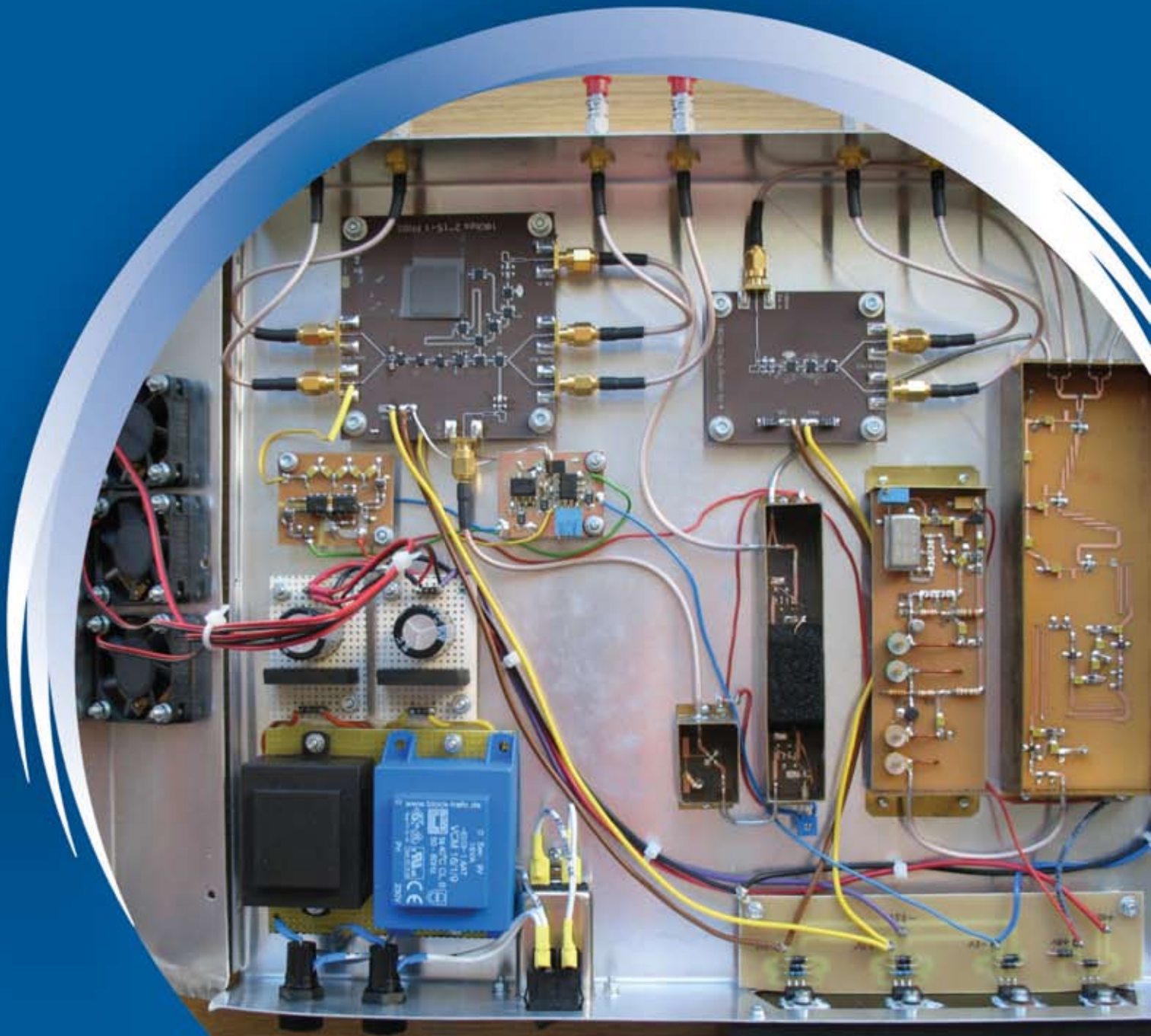

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Original paper

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Modeling and Simulation of High Level Leakage Power Reduction Techniques for 7T SRAM Cell Design

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Abstract: In this paper, the process of 7T SRAM cell is analyzing and also exploring the circuit topologies, high level leakage power reduction techniques and cell parameters. The first segment contains the information about process of the 7T SRAM cell like write operation and read operation. Second segment of this paper characterize high level the leakage power reduction techniques, containing the information about how many types of techniques are available for characterizing the high level leakage power reduction techniques and what is the effect on the high level leakage power reduction techniques on 7T SRAM cell design. The third segment of this paper shows the information about cell parameters means how many parameters we use to describe our circuit. This segment of the paper is the most important segment because this segment contains the information about all the parameters of 7T SRAM cell. In the second segment of this paper contains the information about high level leakage power reduction techniques, by using high level leakage power reduction techniques we can make our 7T SRAM cell much better in different area like power dissipation, leakage power reduction, short circuit power consumption, dynamic power consumption, cell write delay, cell read delay, static noise margin. The data of leakage power consumption shows that after voltage scaling technique leakage power consumption and dynamic power consumption is less.

Keywords: 7T SRAM cell, leakage power reduction, short circuit power consumption, dynamic power consumption, static power consumption, cell write delay, cell read delay, static noise margin.

Modeliranje in simulacije tehnik znižanja visoke stopnje izgub v 7T SRAM celici

Izvleček: Članek opisuje analizo 7T SRAM celice in raziskuje topologije vezja, tehnike znižanja visoke stopnje izgub in parametre celice. V prvem delu je predstavljeno delovanje 7T SRAM celice v smislu operacije pisanja in branja. V drugem delu so karakterizirane tehnike izgub in kakšen vpliv imajo na dizajn celice. V tretjem delu so opisani vsi parametri, ki jih potrebujemo za opis vezja celice. Podatki izgub pokažejo, da so, pri uporabi tehnike skaliranja napetosti, izgube manjše.
Ključne besede: 7T SRAM celica, znižanje izgub, poraba kratkostičnega vezja, dinamična poraba energije, statična poraba energije, zakasnitve pri pisanju in branju, meje statičnega šuma

Ključne besede: 7T SRAM celica, znižanje izgub, poraba kratkostičnega vezja, dinamična poraba energije, statična poraba energije, zakasnitve pri pisanju in branju, meje statičnega šuma

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1. Introduction

In this paper, the process of 7T SRAM cell is analyzing and also exploring the circuit topologies, high level leakage power reduction techniques and cell parameters. In the first segment 7T SRAM cell, describing circuit topologies means how to make our circuit, which type of component used to make our circuit, what are the properties of the component by which we will make our circuit? The second segment contains the information about process of the 7T SRAM cell like write operation and read operation. Third segment of this paper characterize high level the leakage power reduction techniques, containing the information about

how many types of techniques are available for characterizing the high level leakage power reduction techniques and what is the effect on the high level leakage power reduction techniques on 7T SRAM cell design. The fourth segment of this paper shows the information about cell parameters means how many parameters we use to describe our circuit. This segment of the paper is the most important segment because this segment contains the information about all the parameters of 7T SRAM cell. In the third segment of this paper contains the information about high level leakage power reduction techniques, by using high level leakage power reduction techniques we can make our 7T SRAM cell much better in different area like power dissipation, leakage power reduction, short circuit power consumption, dynamic power consumption, cell write delay, cell read delay, static noise margin.

2. Process topology

In this segment we will study about various types of 7T SRAM cell's process[1, 2] like how to write in a 7T SRAM cell to store in the memory. Firstly various types of schematic of the 7T SRAM cell is shows below

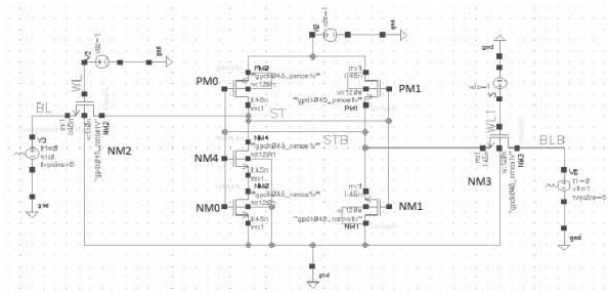

Figure 1: Schematic of 7T1 SRAM cell

This figure shows the schematic of 7T1 SRAM cell, in this circuit seven transistor uses to make the circuit. For making the circuit we use two PMOS which named as PMO and PM1 and five NMOS which named as NMO, NM1, NM2, NM3 and NM4. NM2 and NM3 are called as access transistor and source of the NM2 and NM3 are connected by the BL and BLB respectively and gate of the NM2 and NM3 are connected by the WL and WL1 respectively. The second schematic shows below for 7T2 SRAM cell

This figure shows the schematic of 7T2 SRAM cell, in this circuit seven transistor uses to make the circuit. For making the circuit we use two PMOS which named as PMO and PM1 and five NMOS which named as NMO, NM1, NM2, NM3 and NM4. NM2 and NM3 are called as access transistor and source of the NM2 and NM3 are connected by the BL and BLB respectively and gate of

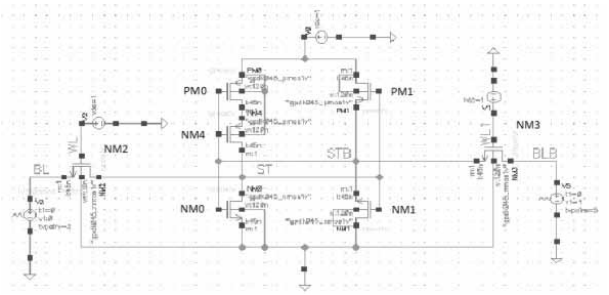

Figure 2: Schematic of 7T2 SRAM cell

the NM2 and NM3 are connected by the WL and WL1 respectively.

The third schematic shows below for 7T3 SRAM cell

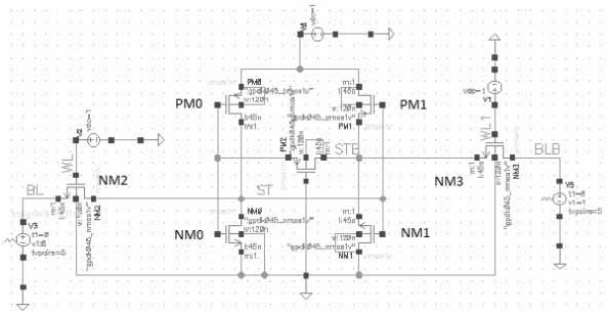

Figure 3: Schematic of 7T3 SRAM cell

This figure shows the schematic of 7T3 SRAM cell, in this circuit seven transistor uses to make the circuit. For making the circuit we use two PMOS which named as PMO and PM1 and five NMOS which named as NMO, NM1, NM2, NM3 and NM4. NM2 and NM3 are called as access transistor and source of the NM2 and NM3 are connected by the BL and BLB respectively and gate of the NM2 and NM3 are connected by the WL and WL1 respectively.

2.1 Write operation

Write operation of various 7T SRAM cell are same for all the 7T SRAM cells. It is started from the NM2 and NM3 transistor because the source of the NM2 and NM3 are working as an input for a write operation. After giving input to the BL and BLB as a VDD and GND respectively and making the WL and WL1 at VDD level, the data goes to the SRAM cell and store at the ST and STB node. The value of the ST and STB node will be opposite means "1V(VDD)" and "0V(GND)" respectively.

The write analysis of the various 7T SRAM cell is shown in the table below

Table 1: Write analysis of the various 7T SRAM cell

S. No	Values	SRAM cell					
		7T1		7T2		7T3	
		1.5 ns	3.5 ns	1.5 ns	3.5 ns	1.5 ns	3.5 ns
1	BL	1V	0V	1V	0V	1V	0V
2	BLB	0V	1V	0V	1V	0V	1V
3	ST	1V	20.66 nV	1V	352 nV	1V	1.4 uV
4	STB	0.6 uV	1V	396 nV	1V	57 uV	1V

2.2 Read operation

The read operation of SRAM cell started from the transistor known as NM2 and NM3 because from these transistors we can either write or read and at this time we will use these transistors as a read transistor. At this point from the source end of the NM2 and NM3 transistor in which BL and BLB connected we will use as a output node.

The write analysis of the various 7T SRAM cell is shown in the table below

Table 2: Read analysis of the various 7T SRAM cell

S. No	Values	SRAM cell					
		7T1		7T2		7T3	
		1.5 ns	3.5 ns	1.5 ns	3.5 ns	1.5 ns	3.5 ns
1	BL	1V	0V	1V	0V	1V	0V
2	BLB	0V	1V	0V	1V	0V	1V
3	ST	1V	186 nV	1V	27 nV	1V	653 mV
4	STB	1.3 uV	1V	42 nV	1V	38 nV	376 mV

3. Leakage power reduction techniques

There are several techniques available for reduction of the leakage power. But here we discuss about only one technique which name is voltage scaling.

3.1 Voltage scaling

Reducing the power supply voltage is the effective technique to reduce static power leakage and the write delay. Keeping all others factors constant if power scaling is scaled down propagation delay will increase. This can be compensated by scaling down the threshold voltage to the same extent as the supply voltage. This allows the circuit to produce the same speed performance at a lower Vdd. At the same time smaller threshold voltages lead to smaller noise margin and increased leakage current.

3.1.1 Write operation after voltage scaling techniques

Write operation of various 7T SRAM cell are same for all the 7T SRAM cells. It is started from the NM2 and NM3 transistor because the source of the NM2 and NM3 are working as an input for a write operation. After giving input to the BL and BLB as a VDD and GND respectively and making the WL and WL1 at VDD level, the data goes to the SRAM cell and store at the ST and STB node. The value of the ST and STB node will be opposite means "1V(VDD)" and "0V(GND)" respectively.

The write analysis of the various 7T SRAM cell after voltage scaling technique is shown in the table below

Table 3: Write analysis of the various 7T SRAM cell after voltage scaling technique

S. No	Values	SRAM cell					
		7T1		7T2		7T3	
		1.5 ns	3.5 ns	1.5 ns	3.5 ns	1.5 ns	3.5 ns
1	BL	0.7V	0V	0.7V	0V	0.7V	0V
2	BLB	0V	0.7V	0V	0.7V	0V	0.7V
3	ST	0.7V	97.43 nV	0.7V	182 nV	329 mV	65.37 nV
4	STB	179 nV	0.7V	532 nV	0.7V	1.4 mV	0.7V

3.1.2 Read operation after voltage scaling techniques

The read operation of SRAM cell started from the transistors known as NM2 and NM3 because from these transistors we can either write or read and at this time we will use these transistors as a read transistor. At this point from the source end of the NM2 and NM3 transistor in which BL and BLB connected we will use as a output node.

The write analysis of the various 7T SRAM cell after voltage scaling technique is shown in the table below

Table 4: Read analysis of the various 7T SRAM cell after voltage scaling technique

S. No	Values	SRAM cell					
		7T1		7T2		7T3	
		1.5 ns	3.5 ns	1.5 ns	3.5 ns	1.5 ns	3.5 ns
1	BL	0.7V	0V	0.7V	0V	0.7V	0V
2	BLB	0V	0.7V	0V	0.7V	0V	0.7V
3	ST	0.7V	77.4 nV	0.7V	83 nV	378 mV	155.4 mV
4	STB	100.5 nV	0.7V	32 nV	0.7V	3.5 nV	0.7 mV

4. Circuit parameters

In this segment of the paper all the parameters described which is related to the 7T SRAM cell design. There are various parameters uses to describe the circuit like short circuit power consumption, dynamic power consumption, static power consumption, cell write delay, cell read delay, static noise margin. But we will discuss about leakage power consumption.

4.1 Leakage power consumption

While the CMOS inverter is in stable state[3], it has either its p- or n- MOS transistor shot off. In an ideal world there would be no current flowing from the power supply to the ground. However there is a small leakage current flowing through the shot off transistor giving rise to leakage power consumption, specified by formula 1.

$$P = I\,leak \times V\,dd \tag{1}$$

By using this formula we can calculate the leakage power consumption for various 7T SRAM cells. After calculating the leakage power consumption we will use the leakage power reduction technique which name is voltage scaling technique and after that we will again calculate the leakage power consumption for the various 7T SRAM cell. This Leakage power consumption is shown in table below

Table 5: Leakage Power Consumption for Various 7T SRAM cells

S. No	SRAM	Leakage Power Consumption			
		Before Voltage Scaling		After Voltage Scaling	
		ST node	STB node	ST node	STB node
1	7T1	0.76 nW	0.97 nW	0.71 nW	0.88 nW
2	7T2	0.66 nW	0.82 7nW	0.51 nW	0.68 nW
3	7T3	0.92 nW	0.58 nW	0.76 nW	0.43 nW

For 7T1 SRAM cell after using the voltage scaling technique we characterize that for the ST node leakage power consumption is 6.57% less with respect to before using voltage scaling technique and for the STB node leakage power consumption is 9.27% less with respect to before using voltage scaling technique. For 7T2 SRAM cell after using the voltage scaling technique we characterize that for the ST node leakage power consumption is 22.72% less with respect to before using voltage scaling technique and for the STB node leakage power consumption is 17.07% less with respect to before using voltage scaling technique. For 7T3 SRAM cell after using the voltage scaling technique we characterize that for the ST node leakage power consumption is 17.39% less with respect to before using voltage scaling technique and for the STB node leakage power consumption is 25.86% less with respect to before using voltage scaling technique.

4.2. Dynamic power consumption

When the CMOS inverter switches from one state to another the output capacitor CL have to be either charged or discharged[4, 5]. Energy is consumed and transformed to heat in the MOS transistors. The energy consumed is equal to the energy needed to charge CL. The energy is specified according to formula 2.

$$E = V_{dd} * Q = V_{dd} * C_L * V_{swing} \tag{2}$$

Vdd is the power supply voltage and V_{swing} the voltage swing on the output of the inverter. If the V_{swing} is the same as Vdd, which is common, the energy becomes,

$$E = C_L * V_{dd} \tag{3}$$

The dynamic power consumption is the energy drawn from the power supply during one second. The power consumed is calculated as in formula 4, where f is the switching frequency.

$$P = ½ * f * C_L * V_{dd}^2 \quad (4)$$

CL is only charged at transition from low to high (zero to Vdd), therefore the division by 2. In a general case, f symbolizes the clock frequency. In this case the constant α is added to express the switching activity as in formula 5.

$$P = ½ * \alpha * f * C_L * V_{dd}^2 \quad (5)$$

By using these formulas we can calculate the dynamic power consumption for various 7T SRAM cells. After calculating the dynamic power consumption we will use the dynamic power reduction technique which name is voltage scaling technique and after that we will again calculate the dynamic power consumption for the various 7T SRAM cell. This dynamic power consumption is shown in table below

Table 6: Leakage Power Consumption for Various 7T SRAM cells

S. No	SRAM	Leakage Power Consumption			
		Before Voltage Scaling		After Voltage Scaling	
		ST node	STB node	ST node	STB node
1	7T1	0.66 nW	0.86 nW	0.53 nW	0.81 nW
2	7T2	0.43 nW	0.74 7nW	0.38 nW	0.65 nW
3	7T3	0.79 nW	0.78 nW	0.71 nW	0.65 nW

For 7T1 SRAM cell after using the voltage scaling technique we characterize that for the ST node dynamic power consumption is 19.69% less with respect to before using voltage scaling technique and for the STB node dynamic power consumption is 5.81% less with respect to before using voltage scaling technique. For 7T2 SRAM cell after using the voltage scaling technique we characterize that for the ST node dynamic power consumption is 11.62% less with respect to before using voltage scaling technique and for the STB node dynamic power consumption is 12.16% less with respect to before using voltage scaling technique. For 7T3 SRAM cell after using the voltage scaling technique we characterize that for the ST node dynamic power consumption is 10.12% less with respect to before using voltage scaling technique and for the STB node dynamic power consumption is 16.66% less with respect to before using voltage scaling technique.

5. Conclusion

The conclusion of the paper explain that after using the leakage power reduction technique which name is voltage scaling the waveform of write operation and read operation is quite different from the initial one. The average leakage power consumption after using voltage scaling technique is 7.92% less from the initial one for 7T1 SRAM cell. The average leakage power consumption after using voltage scaling technique is 19.895% less from the initial one for 7T2 SRAM cell. The average leakage power consumption after using voltage scaling technique is 21.625% less from the initial one for 7T3 SRAM cell. In the next segment of the conclusion the major thing is dynamic power consumption. The average dynamic power consumption after voltage scaling for the 7T1 SRAM cell is 12.75% less than the initial one. The average dynamic power consumption after voltage scaling for the 7T2 SRAM cell is 11.89% less than the initial one. The average dynamic power consumption after voltage scaling for the 7T3 SRAM cell is 13.39% less than the initial one. The whole process for calculating the leakage power and dynamic power after using voltage scaling technique is perform better than the initial one.

Acknowledgements

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Original paper

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Effect of Al addition on the bulk alloy microstructure properties of Sn-1Ag-0.5Cu solder

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Abstract: This study investigated the effect of the addition of 0.2, 0.5 and 1 wt% Al on the bulk alloy microstructural formation of Sn-1Ag-0.5Cu (SAC105). The typical bulk alloy microstructure of SAC105 is composed of large primary Sn grains and a mixture of Ag_3Sn and Cu_6Sn_5 intermetallic compounds (IMCs) which are in the form discontinuous particles at grain boundaries. It is found that the addition of Al to SAC105 alloy gradually suppresses the formation of the bulk Ag_3Sn and Cu_6Sn_5 IMC particles. The addition of 0.2% Al reduces the number of Ag_3Sn and replaces the Cu_6Sn_5, and forms Al-Ag and Al-Cu IMC particles, while the addition of 0.5% Al suppresses the formation of both Ag_3Sn and Cu_6Sn_5 IMC particles. The addition of 1% Al suppresses the formation of both Ag_3Sn and Cu_6Sn_5, and produces Al-Ag, Al-Cu and Al-rich IMC particles. It is also found that increasing the Al content from 0.2% to 1% refines the primary Sn-grains and significantly affects the size and final morphology of the IMCs developed in the bulk alloy. The observation above suggests that the addition of Al makes a big difference in the bulk alloy microstructure of SAC105 alloy. Therefore, one must expect much difference in bulk alloy mechanical properties. This paper is new in the aspect of effect of minor-alloy addition on the bulk alloy microstructure properties of Sn-1Ag-0.5Cu lead-free solder alloy

Keywords: SAC105 alloy, Al addition, bulk alloy microstructure, IMCs formation, Sn-rich grains.

Vpliv dodatka Al na mikrostrukturne lastnosti zlitine Sn-1Ag-0.5Cu

Izvleček: Delo raziskuje vpliv dodatka Al v višini 0.2, 0.5 in 1 wt% Al on na mikrostrukturo zlitine Sn-1Ag-0.5Cu (SAC105). Tipična mikrostruktura zlitine SAC105 sestoji iz velikih primarnih Sn zrn in mešanico Ag_3Sn in Cu_6Sn_5 intermetalnih sestavin (IMCs), ki se nahajajo v obliki diskontinuirnih delcih na robovih zrn. Ugotovljeno je bilo, da dodatek Al postopno zmanjšuje formacijo Ag_3Sn in Cu_6Sn_5 IMC delcev. Dodatek 0.2 % Al zmanjša število Ag_3Sn in jih zamenja z Cu_6Sn_5 pri čemer se formirajo Al-Ag in Al-Cu IMC delci. Pri dodatku 0.5% Al se zmanjša pojav tako Ag_3Sn kakor tudi Cu_6Sn_5 IMC delcev. Dodatek 1% Al zmanša formacijo Ag_3Sn in Cu_6Sn_5 ter sproži pojav Al-Ag, Al-Cu in Al bogatih IMC delcev. Poleg tega dodajanjeod 0.2 % do 1 % Al čisti primarna Sn zrna in močno vpliva na končno morfologijo IMC-ja v zlitini. Opazovanja predlagajo, da ima dodajanje Al velik vpliv na mikrostrukturo zlitine SAC105, kar vodi v različne mehanične lastnosti zlitine. Članek predstavlja nov pogled na vpliv manjšinske zlitine na mehanične lastnosti primarne zlitine pri brezsvinčeni spajki Sn-1Ag-0.5Cu.

Ključne besede: zlitina SAC105, dodatek Al, mikrostruktura zlitine, formacija IMCja, zrna bogata s Sn.

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1. Introduction

Traditionally, tin-lead solder alloy has been the main soldering material for a long time for its superior performance and low cost in modern electronic packaging. The presence of lead in tin-based solder alloys, mostly in the composition of eutectic 63Sn-37Pb, makes the solder superior in terms of thermal and mechanical characteristics for microelectronic assembly and reliability. However, the inherent toxicity of lead has raised serious environmental and public health concerns (Abtew and Selvaduray 2000; Amagai, Watanabe et al. 2002). The near eutectic Sn-Ag-Cu, e.g., SAC305 and SAC405 solder alloys have been considered as promising replacements for the lead-containing solders of microelectronics applications. However, due to the rigidity of the near eutectic SAC alloys, compared with the Pb-containing alloys, more failures have been found in the drop and high impact applications for portable electronic products (Chong, Che et al. 2006; Huang, Hwang et al. 2007). Moreover, the price competitiveness of near eutectic SAC is a weak point due to the high price

of Ag (Yu, Jang et al. 2010). Hence, there is a demand for a more inexpensive and more reliable lead-free solder as a replacement for the near eutectic SAC alloys. Low Ag SAC (e.g., SAC105) was considered a solution for resolving both issues (Kittidacha, Kanjanavikat et al. 2008). However, this approach compromised thermal cycling performance, thus limiting their potential applications in the electronic industries (Huang, Hwang et al. 2007; Kittidacha, Kanjanavikat et al. 2008; Yu, Jang et al. 2010). To help improve the thermal cycling performance of the low Ag SAC, some minor-alloying elements were added to improve fatigue resistivity in bulk solder and strengthen the IMC layer (Huang, Hwang et al. 2007; Kittidacha, Kanjanavikat et al. 2008; Yu, Jang et al. 2010). However, there is a paucity of research on these alloys. The performance issues with near eutectic SAC alloys have forced solder ball suppliers to propose the modified alloys with the low Ag content, and with minor-alloy additions (Henshall, Healey et al. 2008; Kittidacha, Kanjanavikat et al. 2008; Henshall, Healey et al. 2009). The net result of minor-alloying addition is to either (1) alter the bulk alloy characteristics by changing the bulk microstructure and altering the formation and growth of the IMC particles in the bulk solder itself, or (2) control the interfacial IMC layer(s). Pandher et al. (2007) recently published findings that suggest the addition of bismuth (Bi) to SAC0307 alloys contributes to a refinement of grain structure of the bulk solder which improves the thermal cycling performance. Liu et al. (2009) reported that the addition of Mn or Ce to SAC105 solder alloys contributes to the formation of fine and stable IMC particles in the bulk solder which in turn improves the thermal cycling performance. Terashima and et al. (2004) found that the addition of Ni to Sn-1.2Ag-0.5Cu solder alloys contributes a network structure forming around the primary Sn grains in the initial microstructure of the bulk solder, resulting in good thermal fatigue resistance. Given these findings, it is necessary to investigate the influence of further addition of minor alloying elements on the micro-structural formation of the low Ag content SAC lead-free solders. In this paper, the Sn-1Ag-0.5Cu was selected as the basic solder system for exploring the micro-structural formation. The Al was selected as a minor addition, here the influence of the addition of different amount of Al element, 0.2, 0.5 and 1 wt%, on the micro-structural formation of Sn-1Ag-0.5Cu solder was systematically investigated and much attention was paid to the final morphology of bulk intermetallic compounds distributing in the solidified structures.

2. Experimental procedures

The Sn-1Ag-0.5Cu, Sn-1Ag-0.5Cu-0.2Al, Sn-1Ag-0.5Cu-0.5Al and Sn-1.0Ag-0.5Cu-1Al bulk solder specimens

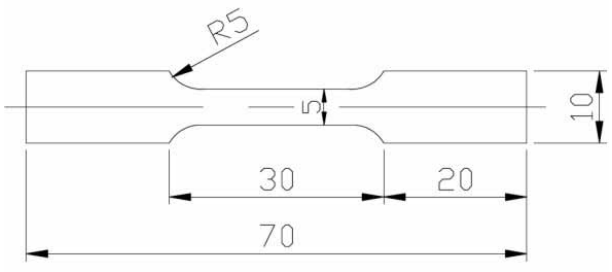

Figure 1: Solder bar specimen

with flat dog-bone shapes were used in this study. Figure 1 shows the solder bar specimen and its dimensions. The thickness of the solder bar is 5 mm. The dog-bone specimens were prepared by melting the Al with pure Tin ingot using an induction melting furnace to make the master alloy (Sn+2wt% Al). Following that, the master alloy was sent to a third party lab (SGS) for composition analysis to confirm the Al concentration. The Sn-Al, Sn-Ag and Sn-Cu master alloy with pure Tin was then melted in the heating furnace in an atmosphere environment. The solder was maintained at 300°C temperature, after which the liquid solder was mixed for 30 minutes by the mixer to prevent the element from separating. After checking to ensure that the Sn, Ag, Cu and impurity of the alloy composition met the specification set by the Atomic Emission Spectrometry (AES), the solder ingots were cast in aluminum molds and naturally-air cooled from 300°C to room temperature (25°C). Then, the solder ingots were re-melted and cast in aluminum dog-bone molds, which had been preheated and kept at a temperature close to the solder alloy melting point. Finally, the molds were cold to the room temperature, disassembled the dog-bone samples were removed and visually inspected to ensure that the surface of the parallel area was without damage and voids. The microstructures of the solders were analyzed based on the Scanning Electron Microscope (SEM), Energy Dispersive Spectroscopy analysis (EDS) and scanning elemental maps. The SEM specimens were prepared by the dicing, resin molding, grinding and polishing processes. They were ground with four grades of SiC paper (# 800, #1200, #2400 and #4000), and then mechanically polished with a diamond suspension (3μm). Finally, the specimens were polished with colloidal silica suspension (0.04μm).

3. Results and discussion

A comparison of the equilibrium microstructures of the solidified lead-free solders would be very useful to clarify how the addition of Al element affects the solidified morphology. Figure 2 presents a SEM micro-structural picture of Sn-1Ag-0.5Cu, Sn-1Ag-0.5Cu-0.2Al, Sn-1Ag-

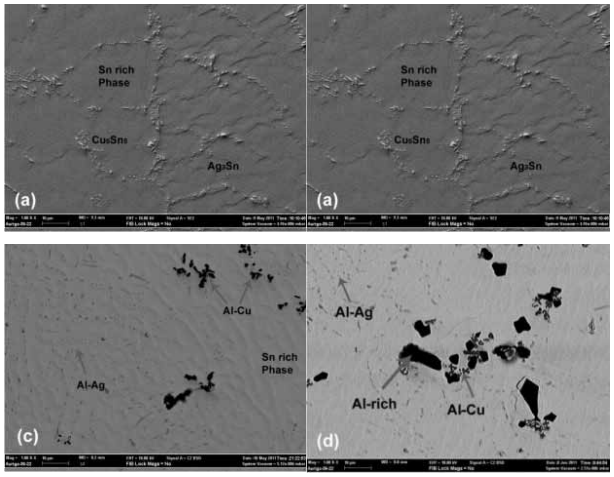

Figure 2: SEM micrograph of (a) Sn-1Ag-0.5Cu, (b) Sn-1Ag-0.5Cu-0.2A, (c) Sn-1Ag-0.5Cu-0.5A (1000X)

0.5Cu-0.5Al and Sn-1Ag-0.5Cu-1Al respectively. It is obvious that the microstructures of the Sn-1Ag-0.5Cu-*x*Al alloys are significantly different from the microstructure of Sn-1Ag-0.5Cu alloy.

The bulk alloy microstructure of Sn-1Ag-0.5Cu, as shown in Figure 2a, is composed of large primary Sn grains and two types of IMC particles which are in the form discontinuous particles at grain boundaries. These IMC particles are Ag14.40 in wt%-Sn85.60 and Cu24.95-Sn71.33-Ag03.72, as indicated in the EDS analysis results (see Figure 3), which are speculated to be Ag_3Sn and Cu_6Sn_5 IMC particles, respectively. The Ag_3Sn and Cu_6Sn_5 IMC particles possess much higher strength than the bulk material in SAC solder, whereas primary Sn has the lowest elastic modulus and lowest yield strength among the constituent phases in SAC

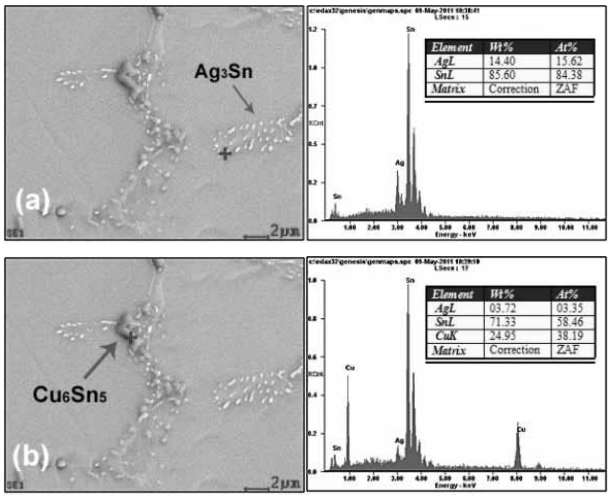

Figure 3: EDS analysis result of the bulk IMC particles in the Sn-1Ag-0.5Cu

solder (Kim, Suh et al. 2007; Suh, Kim et al. 2007). It is well known that the mechanical properties of an alloy consisting of a ductile phase and a hard brittle phase will depend on how the brittle phase is distributed in the microstructure. If the brittle phase is present as grain boundary envelope, the alloy is brittle. If the brittle phase is in the form discontinuous particles at grain boundaries, the brittleness of the alloy is reduced (Dieter 1961). In light of the above mechanism, the SAC105 bulk solder is expected to exhibit high elastic compliance (i.e., low elastic modulus) and high plasticity (i.e., low yield strength) which are identified as key for higher drop resistance.

The bulk alloy microstructure of Sn-1Ag-0.5Cu-0.2Al, as shown in Figure 2b, is composed of large primary Sn grains and three types of IMC particles. The gray large particle is Al6.55-Ag76.34-Sn17.12, and the dark large particle is Al30.47-Cu58.82-Ag3.19-Sn7.52, as indicated in the EDS analysis results (see Figure 4a and 4b). Presumably those particles are primarily IMC of Al-Ag and Al-Cu partially mixed with Sn. The bright fine particles shown in Figure 2b are Sn53.98-Ag46.02, as indicated in the EDS analysis results (see Figures 4c).The bright fine particles are speculated to be Ag_3Sn IMC particles. Figure 5 shows scanning elemental maps of the Sn-1Ag-0.5Cu-0.2Al solder. It is found that the concentration of Ag, Cu and Al has a sudden rise at the location

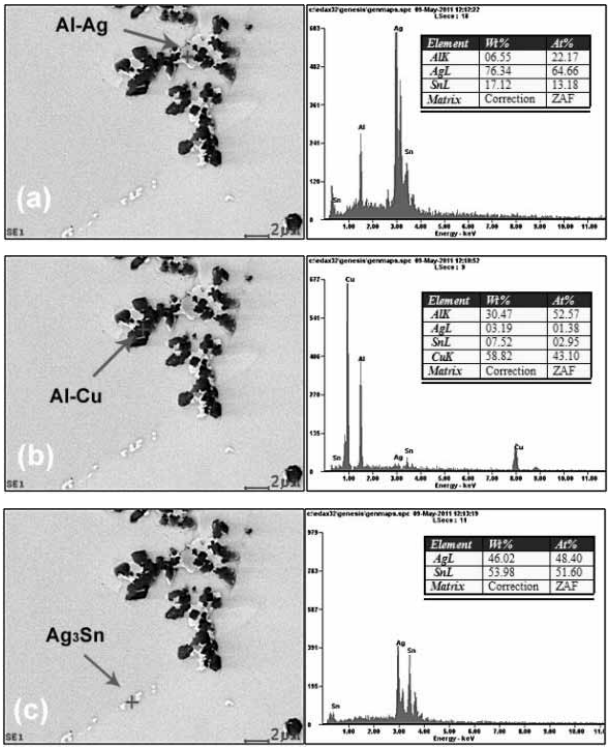

Figure 4: EDS analysis result of the bulk IMC particles in the Sn-1Ag-0.5Cu-0.2Al of (a) Al-Ag, (b) Al-Cu, (c) Ag_3Sn

Figure 5: Scanning elemental maps of the Sn-1Ag-0.5Cu-0.2Al

of the bulk IMC particles. The concentration of Sn becomes small at the location of the bulk IMC particles. All these indicate that elements Ag, Cu and Al constitute the bulk IMC particles with minor Sn dissolving. It can be seen from Figures 2b and 5 that the Al-Ag and Al-Cu are sparsely distributed at and nearby the grain boundaries, beside the Ag_3Sn particle.

The addition of 0.2% Al into SAC105 bulk alloy reduces the number of Ag_3Sn and replaces the Cu_6Sn_5 IMC particles, and forms large Al-Ag and Al-Cu IMC particles. Namely, the Ag and Cu in this alloy will be drained from the solder matrix to react with Al to form large Al-Ag and Al-Cu IMC particles. This is at least in correspondence with the anticipation that Al has solubility in Ag and Cu (Hanson 1985), and very limiting solubility in Sn (Hanson 1985). It is well known that fine particles in alloys impede dislocation movement more efficiently, and produce an alloy with greater yield strength. When these particles grow in size, the yield strength decreases. In addition, when the coherency of particles within the matrix is gradually lost with particles growing, the yield strength is further decreased (Dieter 1976). In light of the above mechanism, beside the discontinuous form of the IMC particles at the grain boundaries (see Figure 6), the 0.2% Al-containing bulk solder is

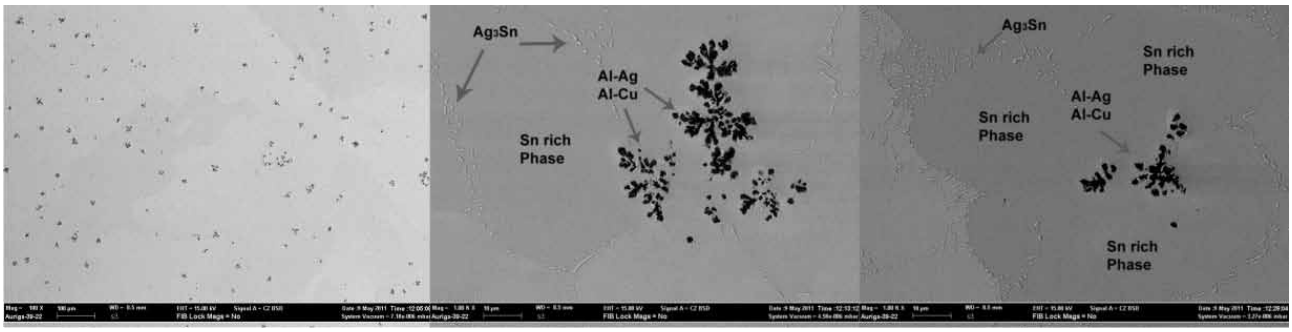

Figure 6: SEM micrograph of Sn-1Ag-0.5Cu-0.2A (100X-1000X)

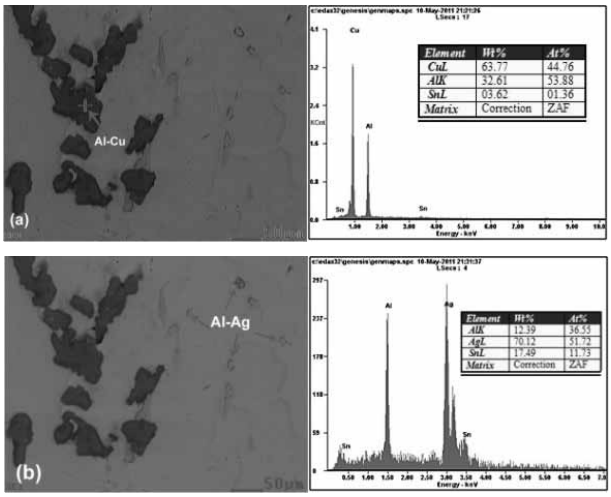

Figure 7: EDS analysis result of the bulk IMC particles in the Sn-1Ag-0.5Cu-0.5Al

expected to show low elastic modulus and low yield strength. The sparse distribution of Al-Ag and Al-Cu IMC particles within the matrix may help to reduce the unfilled interfaces of primary Sn grains at grain boundaries. It is well known that the strength of the interface between primary Sn grains to be lower than that of the primary Sn grains interface filled with the IMC particles.

The addition of 0.5% Al into SAC105 bulk alloy refines the Sn-rich grain structure and produces two types of IMC particles, as shown in Figure 2c. The gray fine particles are Al-Ag IMC particles and the large dark particles are Al-Cu IMC particles, as indicated in the EDS analysis results (see Figure 7) and elemental analysis (see Figure 8). It can be seen from Figure 9 that the large Al-Cu particles appeared sparsely within the Sn matrix. On the other hand, the fine Al-Ag IMC particles form network structure around the primary Sn grains.

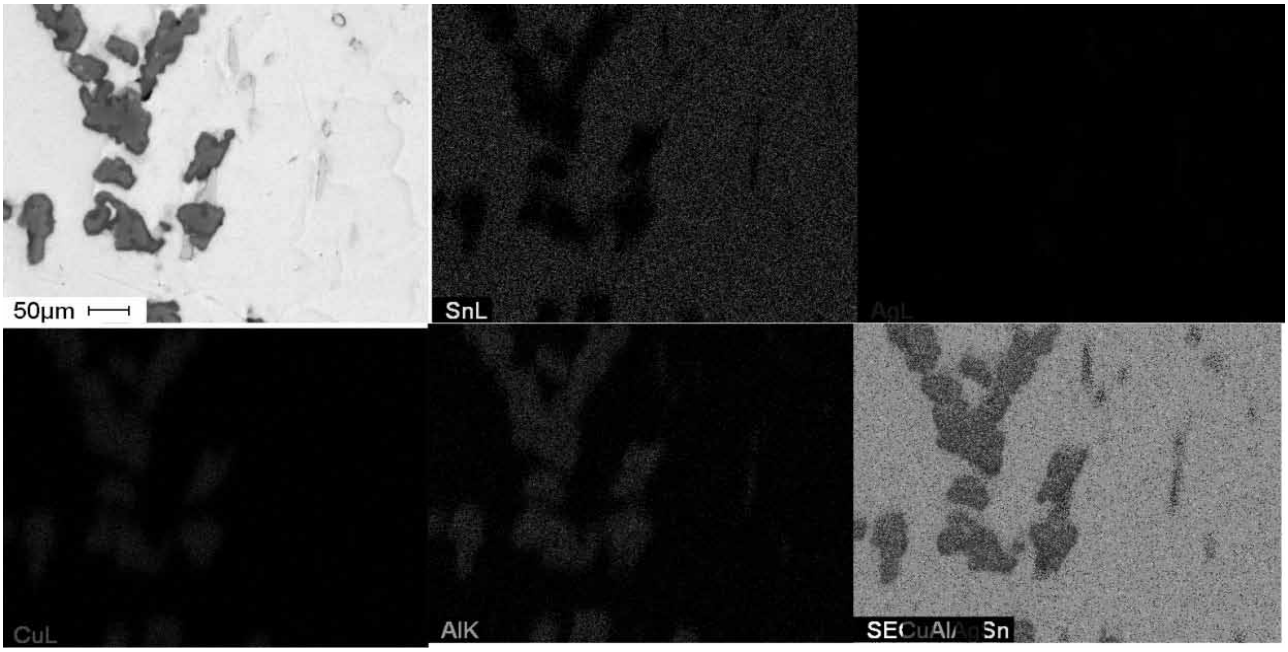

Figure 8: Scanning elemental maps of the Sn-1Ag-0.5Cu-0.5Al

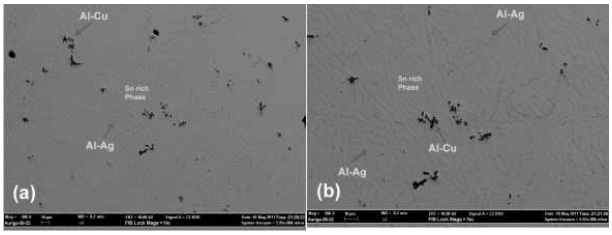

Figure 9: SEM micrograph of Sn-1Ag-0.5Cu-0.5A (a) 300X (b) 500X

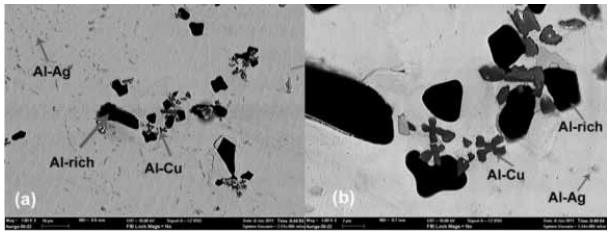

Figure 10: SEM micrograph of Sn-1Ag-0.5Cu-1Al: (a) 1000X, (b) 4000X

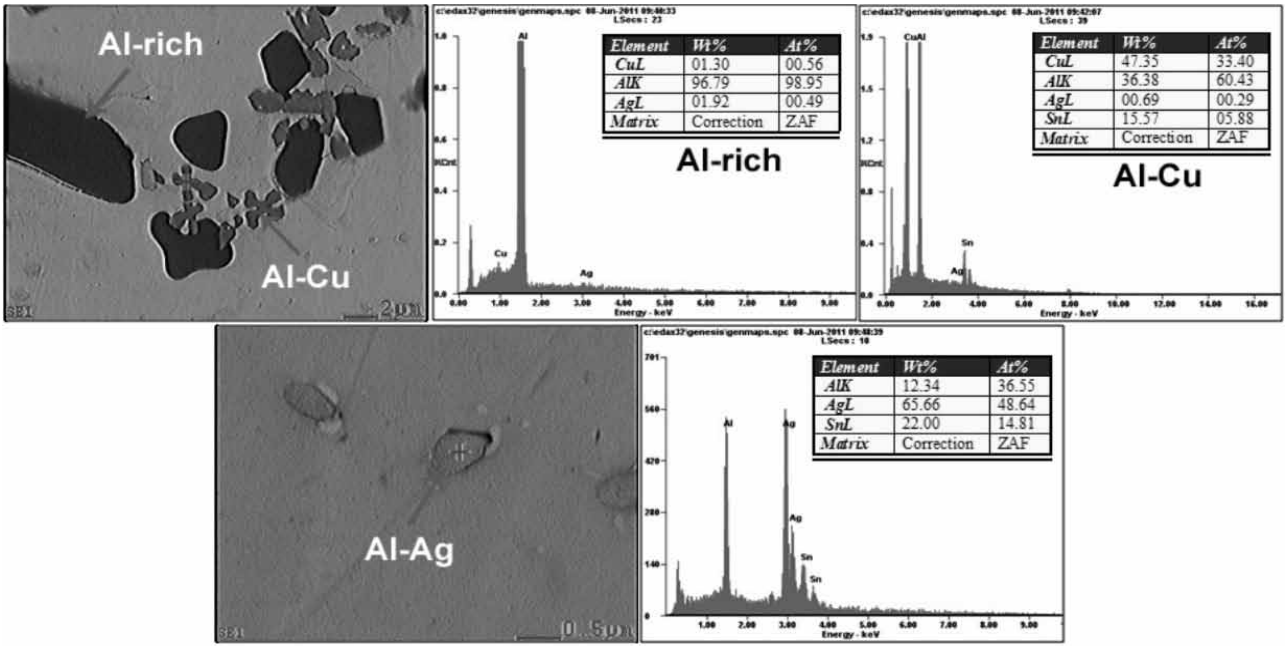

Figure 11: EDS analysis result of the bulk IMC particles in the Sn-1Ag-0.5Cu-1Al

The addition of 0.5% Al into SAC105 bulk solder suppresses the formation of the Ag_3Sn and Cu_6Sn_5 IMC particles, and forms fine Al-Ag IMC particles and large Al-Cu IMC particles. The fine Al-Ag IMC particles form network structure around the primary Sn grains which lead to refine the primary Sn grains of the bulk solder. It is well known that the presence of fine particles dispersed within the matrix can significantly suppress the dislocation movement. Hence, the presence of the fine Al-Ag IMC particles in the bulk alloy significantly strengthens the bulk solder. Therefore, the 0.5% Al-containing bulk solder is expected to show high yield strength and high elastic modulus.

The bulk alloy microstructure of Sn-1Ag-0.5Cu-1Al, as shown in Figure10, is composed of small primary Sn grains and three types of IMC particles. The Al-rich particles (dark large particles) are Al96.79-Ag1.92-Cu1.3, as indicated in EDS analysis results (see Figure 11). The gray large particles are Al36.38-Cu47.35-Ag0.69-Sn15.57, as indicated in the EDS analysis results (see Figure 11). The very fine gray particles are Al12.34-Ag65.66-Sn22, as indicated in the EDS analysis results (see Figure 11), which are speculated to be Al-Cu and Al-Ag IMC partially mixed with Sn, respectively. Figure 12 show that the bulk Al-rich and Al-Cu IMC particles are sparsely distributed within the matrix, whereas the fine Al-Ag IMC particles forms network structure around the primary Sn grains which leads to refine the primary Sn grains. Hence, the 0.5% Al addition is also expected to strengthen the bulk alloy.

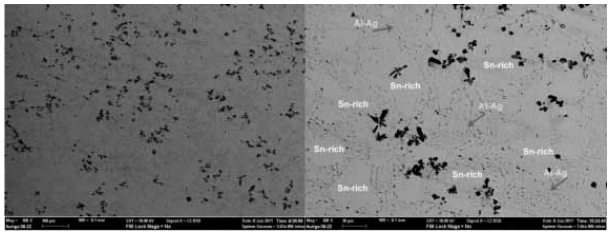

Figure 12: SEM micrograph of Sn-1Ag-0.5Cu-1Al

4. Conclusions

The effect of different Al addition (0.2 wt, 0.5 and 1 wt%) on the bulk alloy microstructure properties of the Sn-1Ag-0.5Cu alloy was investigated in this study. The conclusions can be summarized as follows:

The addition of Al to SAC105 bulk alloy gradually suppresses the formation of the Ag_3Sn and Cu_6Sn_5 IMC particles. The addition of 0.2% Al reduces the number of Ag_3Sn and suppresses the formation of the Cu_6Sn_5, and forms Al-Ag and Al-Cu IMC particles, while the addition of 0.5% Al suppresses the formation of both Ag_3Sn and Cu_6Sn_5 IMC particles. The addition of 1% Al suppresses the formation of both Ag_3Sn and Cu_6Sn_5, and produces Al-Ag, Al-Cu and Al-rich IMC particles.

Increasing the Al content from 0.2% to 1% refines the primary Sn-grains and significantly affects the size and final morphology of the IMCs developed in the bulk alloy. The addition of 0.2wt% Al produces large Al-Ag and Al-Cu IMC particles, whereas the addition of 0.5wt% Al produces fine Al-Ag and large Al-Cu IMC particles. The addition of 1 wt% Al forms fine Al-Ag and large Al-rich and Al-Cu IMC particles. The fine particles form network structure around the primary Sn grains which leads to refine the primary Sn grains, while the large particles sparsely distributed within the matrix
The observation above suggests that the addition of Al makes a big difference in the bulk alloy microstructure of SAC105 alloy. Therefore, one must expect much difference in bulk alloy mechanical properties.

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Analysis from the Perspective of Gate Material under the Effect of Negative Bias Temperature Instability

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Abstract: In this article, we presented the effect of drain current on polysilicon and aluminium based p-MOSFET gates to analyze the Negative Bias Temperature Instability (NBTI) effect, as NBTI is one of the major reliability issues in submicron technology which reduces system lifetime and causes circuit failure. From the perspective of remodeling NBTI, there has been enormous amount of research works in the past. This work analyzed, NBTI from the perspective of the use of transistor gate material and compared two different gate metals under different widths of nanoscale. From the synthesized results, it was shown that NBTI effect is less in aluminium based p-MOSFETs than that of polysilicon as more amount of drain current is drawn by aluminium gate p-MOSFETS.

Keywords: Reliability, Negative Bias Temperature Instability, Drain Current, p-MOSFET

Analiza s stališča materiala vrat pri vplivu temperaturne nestabilnosti pri zaporni polarizaciji

Izvleček: V članku je predstavljen vpliv ponornega toka na vrata p-MOSFET tranzistorja na osnovi polisilicija in aluminija z namenom analize temperaturne nestabilnosti pri zaporni polarizaciji (NBTI). NBTI je ena izmed glavnih problemov zanesljivosti pri podmikronski tehnologiji saj zmanjšuje življenjsko dobo sistema in povzroča napake v vezju. V preteklosti je bilo na področju ponovnega modeliranja NBTI veliko raziskav. V tem delu je raziskan NBTI v perspektivi uporabe dveh različnih kovin vrat z različnimi širinami. Rezultati prikazujejo, zaradi večjega ponornega toka, manjši vpliv NBTIja p-MOSFET-ih na osnovi aluminija kot pri polisilicijevih.

Ključne besede: zanesljivost, temperaturna nestabilnost v zaporni polarizaciji, ponorni tok, p-MOSFET

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1. Introduction

In the field of electronics, prediction of circuit lifetime and system failure analysis has gained significance in the recent times of sub-micron technology. This raises significance concern in the applications of RF electronics, microchips and digital electronics [1-3]. Undoubtedly, these concerns are dependent on transistor reliability aspects. Negative Bias Temperature Instability (NBTI) is one of these reliability aspects; which are responsible for degrading the lifetime of transistors. As a result, the electronic devices stop functioning after a certain period of time. These phenomena have motivated researchers to work on the analysis of NBTI.

Previously, on the degradation of NBTI, various models [4-7] have been proposed by the researchers. Though, these could not find an ultimate solution for NBTI. One of the first models to define NBTI was Reaction-Diffusion model [4], which could not define NBTI in recovery stage. Alam et al. reformed this model and gave solution for many inadequacies of RD model [5]. Though, as per He et al., Alam et al. could not describe NBTI in recovery stage [6]. Many other models on NBTI also contradict with other models. As an example, the theory of Ielmeni et al. [7] contradicts with RD model in terms of frequency dependence. Still, there are works on NBTI degradation and modeling which do not give comparison with the previous models. Hence, it is difficult to get a clear picture on how to solve the NBTI issue from the perspective of degradation models. The incorpora-

tion of HfO_2 was employed by Wilk et al. [8], which could not obtain a solution for NBTI degradation. Another work by Hatta et al. focused on geometric variation of p-MOSFETS where polysilicon was employed as the gate material [9]. But, none of these research works focused on the effect of NBTI when some other material is used in the gate rather than polysilicon.

From these studies, our research objective focused on the variation on the channel width of pMOSFETs by taking two different gate materials. As NBTI lowers the pMOSFET transistor parameters and drain current is one of these [10], our research will focus on the impact of drain current on two different gate materials which are polysilicon and aluminium respectively. On this analysis we will find out, in which material drain current degradation is less when the width is in different scales.

2. Simulation conditions and methods

To observe the NBTI characteristics, we simulated the p-MOSFET by taking a constant length (45nm) and by varying the width at 50nm and 70 nm respectively. This simulation was taken place in two stages with two different materials mentioned earlier. As polysilicon and aluminium are widely used in p-MOSFET design, we employed these two materials in our work. During the simulation process, the Effective Oxide Thickness (EOT) was kept constant and the temperature was kept to 120°. Silvaco simulator was used to study the NBTI effect on different gate materials.

3. Results and analysis

From the simulation we obtained a gate voltage (v) vs. drain current (A) graph. For different negative voltages we plotted a drain current graph where the width was taken 50nm initially. At first, the simulation was performed with a gate material of polysilicon, where at 0.5 voltages we found 1.75×10^{-11}A current as shown in Figure 1. When the voltage was increased more, the current slightly went up and got saturated.

Having obtained the result for polysilicon with 50nm gate width, we simulated another pMOSFET with a gate material of aluminum where the channel width was same as before. At 0.5V stress, the drain current moved slightly above zero level. But, later the drain current started increasing linearly with respect to stress voltage as shown in Figure 2. In our experiment, at 3V, we found a drain current of 3×10^{-5}A.

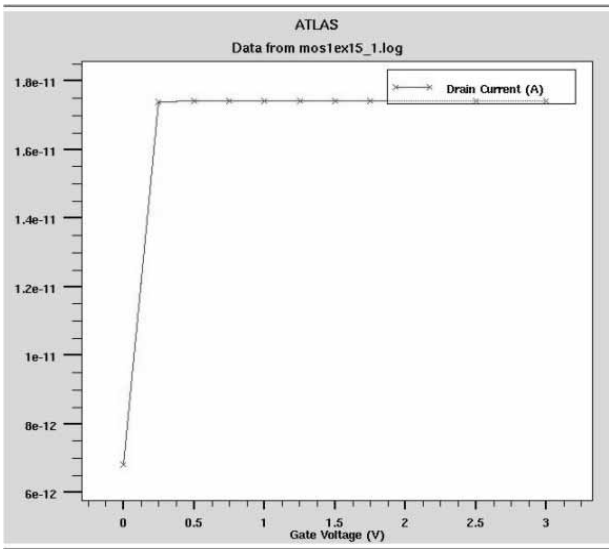

Figure 1: Simulation results where the gate material is polysilicon with 50nm width

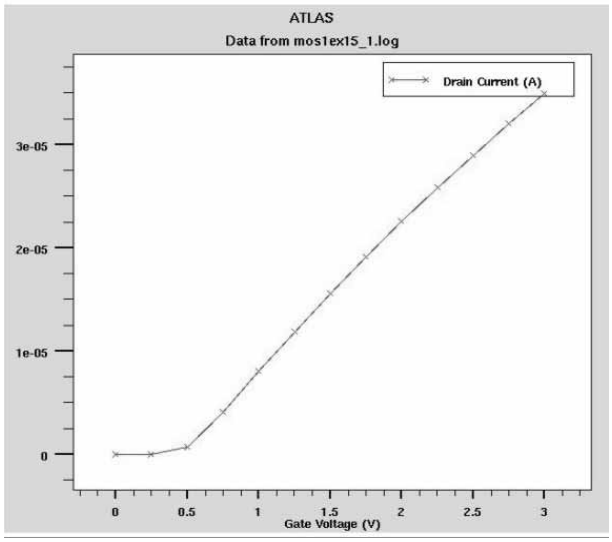

Figure 2: Simulation results where the gate material is aluminium with 50nm width

The simulation with poly with 70nm gate width showed a similar pattern of drain current graph as per Figure 3. Though, it exhibited a high level of drain current which is 8.5×10^{-11}A, which is much higher than the previous experiment with polysilicon.

Lastly, we performed the simulation for alumunium gate pMOSFET where the gate width was fixed to 70nm. The drain current pattern obtained from aluminium gate pMOSFET with 70nm channel width, was similar to the drain current pattern obtained from alumunium gate pMOSFET with 50nm channel width. In our experiment, it showed a maximum drain current of 5.5×10^{-5}A.

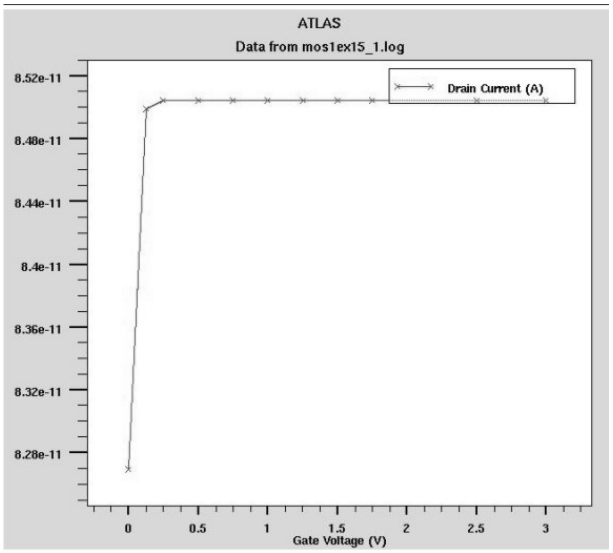

Figure 3: Simulation results where the gate material is polysilicon with 70nm width

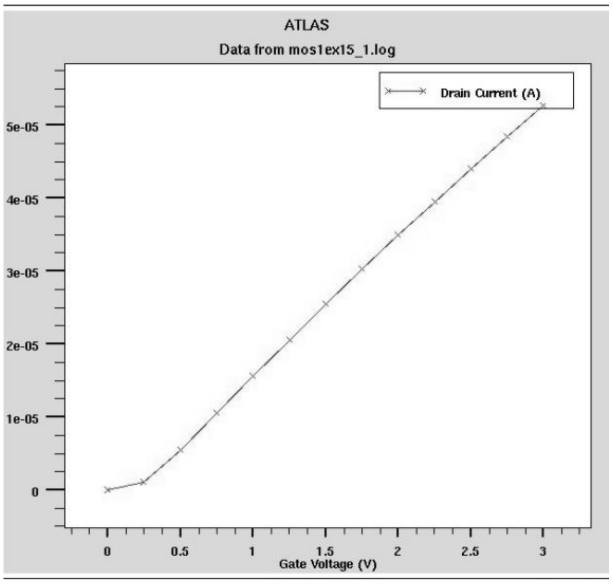

Figure 4: Simulation results where the gate material is aluminium with 70nm width

From the above results, it is clear that at high temperature alumunium gate p-MOSFETS draw more drain current compared to polysilicon where the gate voltage is negative. On the other hand, in poly based p-MOSFETs the amount of drain current is less at an elevated temperature and negative stress. This is a persistent characteristic for different widths of transistors. Under NBTI effect, aluminium is a better choice than poly because it is more attuned with high temperature where polysilicon is more resistive at an elevated temperature. Hence, exploiting aluminium instead of polysilicon will result less NBTI effect.

4. Conclusion

The reliability effect of polysilicon and aluminium gate p-MOSFET has been evaluated from the viewpoint of NBTI. We found a decreasing level of drain current in polysilicon gate p-MOSFETs due to NBTI effect where the widths of the pMOSFETs were varied. Hence, we conclude that, under NBTI effect aluminium is a better gate material than polysilicon.

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Original paper

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Temperature dependence of solar cell characteristics through frequency noise level and ideality factor measurements

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Abstract: Temperature effects and thermally induced noise in photo detectors are significant in the detection processes. Degradation of electrical and optical characteristics of the photo detectors in the increased temperature conditions is one of the most important limitation factors for their application. Since most of the electrical processes in semiconductor devices depend, in some extent, on the temperature, investigations at temperatures higher than room temperature may reveal possible changes in output characteristics of the device. From the technological point of view, thermally induced noise increase minimum signal that can be detected, and this is especially important for the low energy and non ionizing radiation detectors, since the noise level presents the major performance limitation. In this paper these effects are studied through frequency noise level measurements and measurements of the main output characteristics of solar cells.

Keywords: Temperature dependence, 1/f noise, Solar cells, Output voltage, Ideality factor

Temperaturna odvisnost lastnosti sončnih celic glede na nivo frekvenčnega šuma in meritev faktorja kvalitete

Izvleček: Temperaturni efekti in termično vzbujan šum imajo velik vpliv v procesu razpoznavanja v fotodetektorjih. Degradacija električnih in optičnih lastnosti fotodetektorjev pri povišani temperaturi je eden izmed najpomembnejših omejitvenih faktorjev njihove uporabe. Ker je večina električnih procesov temperaturno odvisnih lahko raziskave pri temperaturah nad sobnimi razkrijejo morebitne spremembe njihovih lastnosti. Iz tehnološkega vidika termično vzbujan šum dvigne najnižji nivo signala, ki ga še lahko zaznamo, kar je še posebej pomembno pri nizkoenergijskih detektorjih ne detektorjih neionizirajočih sevanj saj nivo šuma predstavlja največjo oviro učinkovitosti. V članku so ti vplivi raziskani s strani meritev nivoja frekvenčnega šuma in glavnih izhodnih karakteristik sončnih celic.

Ključne besede: temperaturna odvisnost, 1/f šum, sončne celice, izhodna napetost, faktor kvalitete

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1. Introduction

The extensive miniaturization of the semiconductor devices based on semiconductor junctions (p-n, p-i-n, Schottky, etc.) introduces the problem of the temperature effects and thermally induced noise in such devices. Silicon solar cells belong to a wide group of semiconductor detector devises, though somewhat specific in its design (larger than most of the detectors), and that, together with the fact that they are directly exposed to the solar radiation makes them especially susceptible to the effect of the high temperature. For higher temperatures, thermal noise is dominant and significantly influences the detecting signal and output characteristics. Also, other types of noises especially frequency dependent generation-recombination noise, burst noise and 1/f noise increase with the increase of the temperature [1]. Since increased temperature influence all parts of semiconductor device, contact grid is also prone to some changes, particularly because surface effects are expected to be a major cause of 1/f noise. This is especially significant for solar cells because of their design (large surface to volume ratio), so materials for front contact grid should be carefully chosen. Silicides be-

long to a very promising group of materials which are of great interest both in physics of thin films and in microelectronics. Many of them have a low resistivity and good temperature stability that make them desirable for fabrication of reliable and reproducible contacts [2,3]. It is known that low frequency noise (1/f and burst noise) manifests as random fluctuation of the output current or voltage, leading to lowering of the efficiency of the device. Various experiments suggest [4-8] that the origin of this noise is fluctuation of the number of free charge carriers connected to existence of the traps located in the vicinity or directly in the junction area, or fluctuation of the mobility of charge carriers. These effects are more pronounced when the device is exposed to high temperature conditions, since in those conditions defects, surface states and impurities that act as traps for charge carriers could be in addition thermally activated [9]. It has been found [3,10] that ion implantation of As^+ ions in the formation of the silicides could improve electrical characteristics of silicides regarding their noise level.

Recently, a new type of materials, dye-sensitized solar cells (DSSCs) based on nanocrystalline high band gap oxide semiconductors receive much attention as cheap alternatives to the conventional solar cells made from low band gap semiconductors. From the standpoint of 1/f noise, it has been found [5] that some molecular species that strongly chelate to the semiconductor surface, suppress 1/f noise owing to passivation of the recombination sites. Thus in addition to sensitization, the dye adsorbed on the nanocrystallites plays a key role in mitigation of recombination. The mechanism involved seems to be the passivation of the semiconductor surface by the adsorbed dye. Passivation is also the cause that suppresses recombination in the dye-sensitized solar cells.

On the other hand, since all dynamic processes in semiconductor devices are temperature-dependent [1, 11-13], study of the variations of junction characteristic parameters (ideality factor, saturation current, etc.) due to the increased temperature is crucial. One of the most important electrical processes in junction devices is transport of the generated charge carriers across the junction. Type and temperature dependence of the transport mechanism is obtained from dark current-voltage (I-V) measurements of photo detectors. Main parameter that could be extracted from I-V data is the ideality factor (n), direct indicator of the output parameter dependence on the electrical transport properties of the junction. The non-ideal behavior of the device is reflected in the values of n greater than 1, and also in the temperature dependence of the ideality factor. This dependence is the result of the presence of different transport mechanisms that can contribute to the diode current at different temperatures. Determination of the dominant current mechanism is very difficult because the relative magnitude of these components depends on various parameters, such as density of the interface states, concentration of the impurities and defects, height of the potential barrier, device voltage, and device temperature. Even for a given system at a particular temperature rarely only one mechanism dominates the diode current over entire voltage regime. The main transport processes that could occur, even simultaneously, are thermionic emission, field emission, thermionic field emission, recombination-tunneling via interface states, minority carrier injection, and recombination [11]. Beside I-V measurements at different temperatures, measurements of the n(T) and n(V) dependence could narrow down possibilities of the dominant current component. Values of the ideality factor at different temperatures could indicate not only the transport mechanism, but indirectly, the presence and possible activation of the defects and impurities, acting as recombination and/or tunneling centers. Also, the presence of the defects in the material is considered to be the main cause of the existence of the current noise. Some types of noise in photo detectors are correlated with the presence of the excess current [11], binding optical and electrical characteristics of such devices.

Purpose of this paper is to present temperature dependence of main characteristics of solar cells in connection to the temperature dependence of 1/f noise level in silicides and ideality factor in photodiodes.

2. Methods

Due to the complexity of the subject, three types of measurements were performed in this experiment. Investigations of temperature dependence of 1/f noise in silicides were performed for TiN/Ti/Si samples. Ion implantation with As^+ ions, annealing and electrical characterization were performed on the samples. Implantation of arsenic was performed at 350 keV with the dose range between $1x10^{15}$ ions/cm^2 to $1x10^{16}$ ions/cm^2. Thermal treatment for all samples was performed at different temperatures for 20 min. The distinction of these measurements compared to other of this type is that they were based on the temperature dependence of the noise level in silicides for two temperatures: -18°C and 50°C. Noise level measurements were performed with the measurement equipment consisting of the multichannel analyzer ND-100, low noise pre-amplifier, and amplifier (standard ORTEC equipment). MAESTRO II code was used for automatic energy calibration.

Experimental measurements concerning solar cells were carried out on the commercially available silicon

solar cells manufactured by Leybold. Current-voltage data were used for the characterization of the properties of solar cells. Temperature dependence was measured in the range from room temperature (21°C) to slightly above 40°C (41°C).

For determining temperature dependence of ideality factor for commercially available p-i-n and p-n silicon photodiodes were used (all samples were produced by SIEMENS, trademarks BP 104, BPW34, BPW 43, and SFH 205). Direct bias dark I-V characteristics of the diodes were measured at four different temperatures, using standard configuration for I-V measurements (Hewlett-Packard current-voltage source, and two digital multimeters - SIMPSON and LEADER). Temperature range was in agreement with the operating/storage range supplied by manufacturer (21°C - 83°C). Measured I-V data were analyzed using ORIGIN program package. Diode parameters were obtained using standard and numerical fit methods with the correction due to the presence of series resistance.

Experiment was performed in well controlled laboratory conditions with combined measurement uncertainty less than 5% within all measurement procedures [14,15].

3. Results and discussion

3.1 Frequency noise level measurements

Temperature dependence of 1/f noise level was observed for this type of silicides, as could be expected. Spectra of frequency dependent noise on lower (-18°C) and higher (50°C) temperature are shown in Figures 1 and 2, respectively.

Not only that the assumption that higher temperature induces higher noise level was confirmed, but the essential part of this measurement is that it was observed that implantation dose used for fabrication of silicides could influence the increase of noise level. The possibility of improvement of silicide characteristics by ion implantation and thermal annealing was reported earlier [10], but primarily in connection to the radiation damage. Structural RBS analysis has shown that ion implantation did not induce redistribution of components for lower implantation doses. The spectra indicate that the entire titanium layer has interdiffused with the silicon substrate. The presence of the $TiSi_2$ and $TiSi_2$ phase in the implanted samples was observed. In all cases top TiN layer remains unaffected, but for higher doses of implantation ($1x10^{16}$ ions/cm^2) a disordered structure was registered. This corresponds to the amorphization of silicon substrate, which is moving deeper with the ion dose, showing that the physical properties of TiN/Ti/Si are influenced by the implantation. Also, it was found [2,3] that thermal treatment induces relaxation of crystal lattice and improvement of the crystal structure of the silicides.

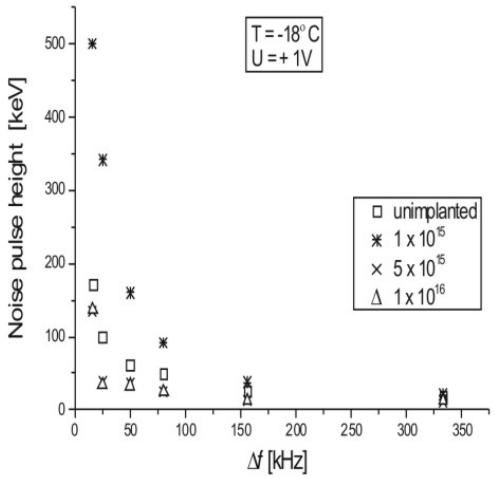

Figure 1: Frequency noise level of three implanted and one unimplanted sample at -18°C.

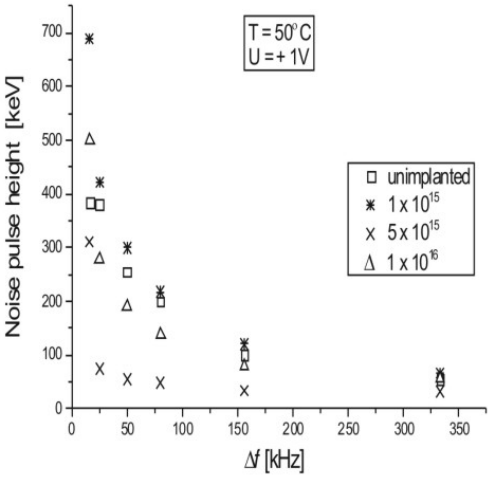

Figure 2: Frequency noise level of three implanted and one unimplanted sample at 50°C.

However, this temperature dependent measurements indicate another very important fact that ion implantation could provide temperature stability of silicides regarding 1/f noise. Namely, from Fig. 1 and 2 could be seen that samples implanted with doses of $5x10^{15}$ions/cm^2 had lowest noise level and very good temperature stability. This could lead to an improvement of electrical characteristics of silicides and devices based on silicides as contacts (for example, solar cells).

3.2. Temperature dependence of electrical characteristics of photo detectors

Though the current transport mechanism is (theoretically) similar for most semiconducting devices based on p-n junction (for example, solar cells), the choice of the material and its structure (monocrystalline, polycrystalline or amorphous) has some influence on the transport processes. Amorphous silicon, a-Si, for example, is a direct-gap material with very high density of states within the energy gap, that could behave like recombination centers for the charge carriers. Though a-Si has high absorption coefficient and is easy to manufacture, the main difficulty in a-Si solar cell technology lies in constant decrease of efficiency during time. This effect is called Staebler – Wronski effect, and is dependent on total number of the absorbed photons, i.e., on the intensity of the light to which the cell is exposed, and the duration of the exposure.

Polycrystalline and monocrystalline solar cells are more reliable than amorphous, but inherent presence of defects and impurities in the basic material could, during time, produce some negative effects. This is specially emphasized if those states are located within the energy gap and are activated during work due to the temperature increase, for example. In such a case they become traps for optically produced electron-hole pairs, and thus decrease the number of collected charge carriers. Macroscopically, this effect could be observed as a decrease of the output current and voltage, and ultimately could lead to the decrease of the efficiency of solar cell.
When the temperature dependence of solar cell characteristics is concerned, although an increase of the current with the temperature increase was observed, main output characteristics such as efficiency were negatively influenced by high temperature. This is due to the fact that open circuit voltage rapidly decreases with an increase of the temperature, as could be seen in Fig. 3.

The rate of the decrease ($\Delta V_{oc}/\Delta T$) for this particular cell was -2,48mV/°C (using linear approximation method), and that made it particularly temperature sensitive. This could be the result of the dependence of the V_{oc} on the dark current J_0 of the cell. Namely, decrease of V_{oc} with an increase of J_0 is connected to the dominating transport mechanisms of the device, and since increased temperature unavoidably leads to the increase of J_0, the decrease of V_{oc} is expected. Also, because of the working conditions of solar cells (direct exposure to the solar radiation), their temperature increases very rapidly (up to 40°C in the first 2-3 minutes of work), so better temperature stabilization of characteristics, and/or adequate cooling are main requirements for successful and long-term operation of solar systems. Also, voltage decrease in the maximum power point (P_m) has great influence on the efficiency. One of the main reasons for this decrease is the increase of the ideality factor, so it could be said that the influence of the ideality factor on the solar cell efficiency is through the voltage. This is especially important because for non-ideal devices ideality factor n is greater than 1, indicating more complex temperature dependence of basic properties such as diffusion length or charge carrier lifetime.

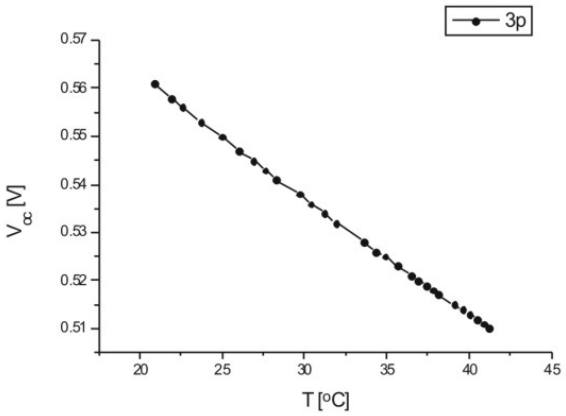

Figure 3: Temperature dependence of open circuit voltage V_{oc}.

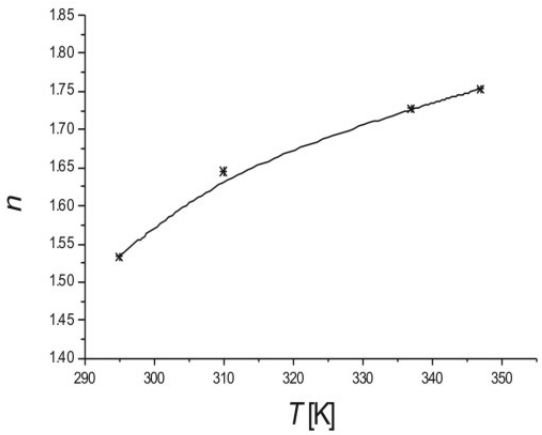

Figure 4: Temperature dependence of the ideality factor n.

Direct dependence of the ideality factor on the temperature for photo detector was shown in Fig. 4, where more or less linear increase of n could be seen. From the physical point of view, this behavior could be explained with the fact that, at the increased temperatures, imperfections of basic material are more pronounced. Namely, defects in the crystal lattice such as vacancies or interstices tend to accumulate when thermally stimulated, disturbing the periodicity of the potential field in the crystal. Such deviations could induce

scattering of the charge carriers, and, consequently, a non-ideal behavior of the device, reflected in the values of n > 1. Besides, dislocations and impurities in the material with energy levels deep in the energy gap also tend to precipitate. Such localized energy states could act as traps or recombination centers for charge carriers, modulating output current and inducing current noise in photo detector devices (at low and medium voltages). Burst and 1/f noises are an example of the low frequency noises characterized by discrete current fluctuations, usually referred to as excess current. This excess current was observed in all samples at medium voltages, indicating the existence of the low frequency noises in the devices.

4. Conclusions

One of the major performance limitations of solar cells is the degradation of electrical and optical characteristics at increased temperatures. First part of the paper was oriented to the frequency dependent 1/f noise in contacts, since temperature increase induces higher level of noise. It was established that both physical and electrical properties of used silicides are influenced by the implantation doses. But the results of frequency noise measurements indicate that ion implantation could successfully be applied in order to achieve a more homogeneous silicidation and very good temperature stability, if carefully optimized dose (in our case $5x10^{15}$ ions/cm^2) was used. One of the most important characteristic of detectors such as solar cells is their energy resolution that primarily depends on noise, and that is why measurements of 1/f noise and improvement of silicides characteristics by lowering 1/f noise in them leads to the production of reliable and thermally stable contacts that could be used to improve solar cells.

On the other hand, from the I-V measurements obtained data have shown that though there is significant increase of solar cells current with an increase of temperature, other electrical characteristics rapidly degrade leading to the decrease of the efficiency. Owing to the strong correlation between burst noise and excess current, degradation of both electrical and optical output characteristics of the device could be monitored through the ideality factor. Obtaining the ideality factor from I-V measurements is quick, simple, non-invasive and effective way to evaluate possible degradation of output characteristics of solar cells and photodetectors in working conditions, and could be used to better understand solar cells. The observed increase of the ideality factor with the temperature indicates an increase of the current noise and detection threshold, and decrease of the resolution of the photo detector device. Although still in the working state, performances of such a detector (solar cell) at the increased temperatures are significantly deteriorated leading to the decrease of the precision of the output signal. For this reason monitoring of the device characteristics should be performed continuously, especially because solar cells are exposed to the severe working conditions such as increased temperature.

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10 Gb/s 2^{15}-1 pseudo-random binary sequence generator

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Abstract: A 10 Gb/s pseudo-random binary sequence generator with a pattern length of 2^{15} – 1 is presented. It is using a novel generation method, practically implemented as a single-stage linear-feedback shift register. The new method is suitable for the highest data rates (several tens of Gb/s), since it allows operation at clock frequencies higher than the traditionally-designed multiple-stage chain, made of the same type of D-flip-flops. Most of the required delays in the PRBS generator are derived from microwave transmission lines instead from active logic devices, thus much simplifying the circuit design. The generator produces the maximum-length bit sequence defined by the $1 + x^{14} + x^{15}$ polynomial and is implemented by a discrete design at 10 Gb/s data rate using commercially-available high-speed logic.

Key words: pseudo-random binary sequence, high-speed logic, linear-feedback shift register, maximum-length sequences.

Psevdonaključni podatkovni izvor z bitno hitrostjo 10 Gbit/s in dolžino zaporedja 2^{15} – 1

Povzetek: V prispevku je predstavljen izvor psevdonaključnih podatkov z bitno hitrostjo 10 Gbit/s in dolžino zaporedja 2^{15} – 1. Izvor izkorišča novo metodo za generiranje psevdonaključnega zaporedja, ki temelji na pomikalnem registru z linearno povratno vezavo, sestavljenem iz ene same (aktivne) stopnje. Nova metoda je primerna za najvišje bitne hitrosti (od nekaj deset Gbit/s naprej), saj omogoča delovanje pomikalnega registra pri višjih taktnih frekvencah, kot običajno izvedeni pomikalni registri (sestavljeni iz verige enakih D flip flopov). Večina potrebnih zakasnitev v izvoru je izvedena s pomočjo mikrovalovnih prenosnih linij (namesto z aktivnimi stopnjami), kar znatno poenostavi načrtovanje vezja izvora. Izvor generira zaporedje maksimalne dolžine, določene s polinomom $1 + x^{14} + x^{15}$, in je sestavljen iz razpoložljivih posamičnih logičnih vezij ter obratuje pri taktni frekvenci 10 GHz.

Ključne besede: psevdonaključni podatkovni izvor, hitra logična vezja, pomikalni register z linearno povratno vezavo, zaporedja maksimalne dolžine

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1. Introduction

Pseudo-random binary sequences, usually maximum-length sequences (m-sequences), are widely used in communications systems. For example, they are used as spreading sequences in direct-sequence spread-spectrum systems (CDMA, GPS, etc.), as white noise, as scrambling and synchronization codes, they are found in many cryptosystems and radar applications, and last but not least they are employed as test-data patterns in Bit-Error-Rate (BER) optical and radio communication-link measurements and high-speed component and devices testing (i.e. digital devices, photodiodes, amplifiers, etc.). They are deterministic, simple to generate, verify and synchronize on, while their mathematical properties resemble random data.

The maximum-length sequences are generated by modulo-2 polynomial division with irreducible polynomials. The latter is practically implemented in the form of linear-feedback shift registers [1], where the linearity of the feedback is achieved by modulo-2 addition with EX-OR logic gates, as shown in Fig. 1 for the $1 + x^{n-1} + x^n$ trinomial. Maximum-length sequences of the length 2^n – 1 (where n is the number of shift-register stages) have several interesting mathematical properties, like the precisely-defined pseudo-random distribution of logical ones and zeros, a two-level autocorrelation function (ideal for the radar application) and a frequency spectrum including equally-spaced, equal-amplitude spectral lines (ideal for the white noise). The maximum-length sequences have 2^{n-2} logic-level transitions, enabling a simple pattern-length synchronization by a

ripple counter [2, 3]. For example, the sequence defined by the $1 + x^{14} + x^{15}$ polynomial has exactly 8192 logic-level transitions.

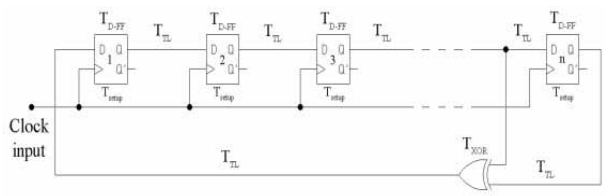

Figure 1: Typical PRBS generator implementation for the $1 + x^{n-1} + x^n$ trinomial.

The maximum operating clock frequency of the traditionally-implemented PRBS generator, as illustrated in Fig. 1, is limited by the sum of several delays in the circuit section comprising the XOR gate, since the latter has the highest delay of all. The clock period T is defined in Eq. 1 as

$$T_{D\text{-}FF} + T_{XOR} + T_{TL} + T_{setup} \leq T, \quad (1)$$

where $T_{D\text{-}FF}$ and T_{XOR} denote propagation delays of the flip-flop and XOR gate, respectively, T_{TL} is the sum of all delays of the connecting transmission lines in this circuit section and T_{setup} is the flip-flop's setup time (valid data before the clock transition). For the integrated PRBS generators with the highest clock frequencies beyond 100 GHz, the propagation delays in the logic devices present the main delay contribution and therefore the maximum-clock-frequency limitation [3, 4].

2. Single-stage PRBS generation method

The single-stage linear-feedback shift register uses a single D-flip-flop and several transmission lines (for example microstrip, coaxial, stripline, etc.) to generate the delay required by the register length [5]. The D-flip-flop is required for the signal regeneration (retiming and reshaping). Fig. 2 illustrates the new PRBS generator, including only a single D-flip-flop, an EX-OR gate and the required transmission (delay) lines.

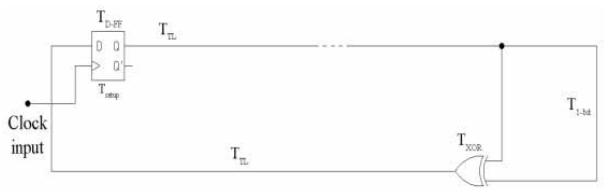

Figure 2: Single-stage PRBS generator implementation for the $1 + x^{n-1} + x^n$ trinomial.

The total loop delay must be equal to the polynomial order times the clock period T, therefore the delays shown in Fig. 2 can be written in Eq. 2 as

$$T_{D\text{-}FF} + T_{XOR} + T_{TL} + T_{setup} \leq (n - 1) * T, \quad (2)$$

where $T_{D\text{-}FF}$ and T_{XOR} denote propagation delays of the flip-flop and XOR gate, respectively, T_{TL} is the sum of all transmission-lines delays (without the $T_{1\text{-}bit}$), T_{setup} is the flip-flop's setup time (valid data before the clock transition) and n is the polynomial order. In an extreme case, the maximum clock-frequency increase of the single-stage over the conventional design is n – 1. This applies for the trinomial shown and the fact that the T_{TL} remains the same in both designs, while $T_{D\text{-}FF}$ being much higher in the single-stage design. In practice such an increase can hardly be accomplished, since the propagation delay of flip-flops is getting smaller with the increased toggle-rate capability (i.e. a flip-flop with high propagation delay and high toggle rate does not exist).

When compared to the conventional LFSR circuit, shown in Fig. 1, the new PRBS circuit has many advantages: simplicity, less logic devices and lower power consumption. A single-D-flip-flop design also eliminates the complex clock-distribution circuits required for several D-flip-flops in conventional high-speed LFSR designs. Finally, the clock frequency can be increased to the upper D-flip-flop toggle limit and the latter is usually much higher than the clock-frequency limit imposed by propagation delays in a traditional multi-stage designs, especially in the case of discrete-packaged devices. The discrete-packaged logic has a significant propagation delay contribution from the package itself, which severly limits the performance, particularly at and above 10 GHz toggle frequencies. The new PRBS generation method is not limited by the flip-flop's propagation delay $T_{D\text{-}FF}$, since the latter can be compensated by a shorter transmission-line delay T_{TL} (Eq. 2).

The single-stage method's drawbacks include: the PRBS polynomial depends on the sum of the delays of the active logic and the transmission lines, respectively, and the PRBS pattern length is limited by the insertion loss, dispersion of the transmission lines used and the input sensitivity of the regeneration stage. The design works only at a single clock frequency (with the typical range of a few percent around the central frequency). If the design is manufactured with fixed transmission lines (i.e. on a printed-circuit board), the polynomial can not be changed easily, except if broadband switches are used for the selected transmission-line lengths. However, almost all high-data-rate PRBS generators (employing the traditional generation method) with the output data rates in excess of several tens of Gb/s

and beyond, are also optimized for a single polynomial operation [3, 4].

3. 10 Gb/s 2^{15}–1 PRBS generator

The generator is a standalone unit and comprises several modules as shown on the block diagram in Fig. 3: PRBS core, pattern-length synchronization divider, clock divider, reference oscillator and multipliers, power supply, maximum-length sequence detector and auto start, phase shifter with amplifier and finally the D-type flip-flop.

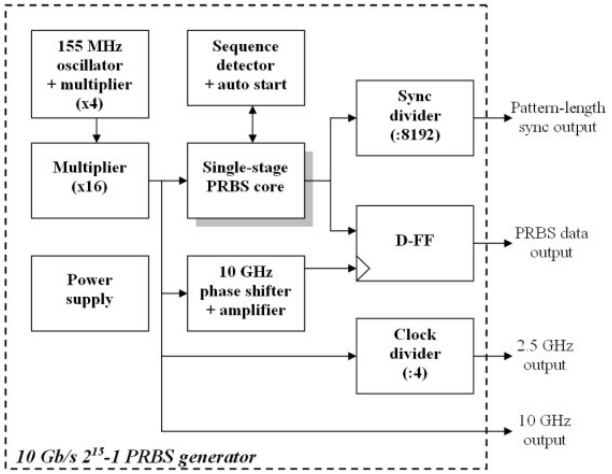

Figure 3: Block diagram of the 10 Gb/s 2^{15}-1 PRBS generator.

The most challenging part was the single-stage PRBS core, operating at 9.95 Gb/s as a standard OC-192 (STM-64) bitrate generator. The core consists of a single (retiming) stage (D-type flip-flop), first 2:1 multiplexer used as a modulo-2 adder (XOR gate) and second one used as a logic-one insertion stage for the auto-start functionality, two buffers used as reshaping and fanout stages and finally transmission lines for the remaining delay of the linear-feedback shift register. The PRBS core is shown in Fig. 4.

The PRBS-core PCB holds also the pattern-length synchronization dividers (three :16 and one :2 divider) and also the D-type flip-flop used as the final regeneration stage for the output PRBS data. The latter is a low-jitter (3 ps_{pp} deterministic and 0.3 ps_{rms} random) high-speed device (rise/fall times typically 16 ps) for the best possible PRBS-data quality. The eye diagram of the output PRBS data, measured by a sampling oscilloscope with a 40 GHz bandwidth, is shown in Fig. 5. The PRBS core is a fully differential design using differential current-mode logic (CML) devices and interconnected by differential microstrip transmission lines. The used 4-layer FR-4

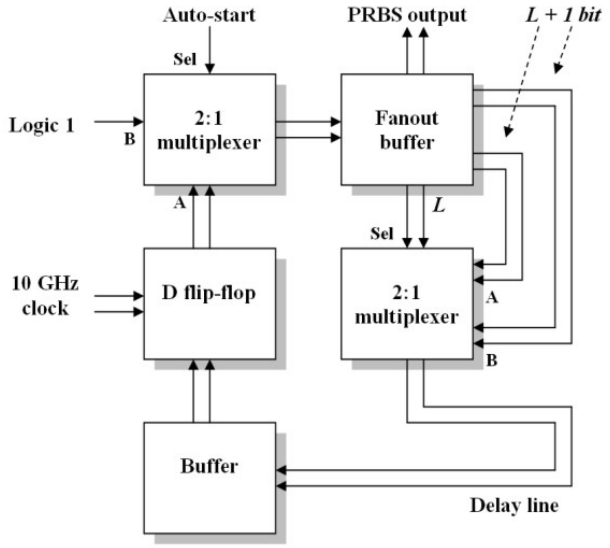

Figure 4: Simplified diagram of the differential PRBS core.

laminate is not an optimal choice due to the noticable loss and dispersion throughout the whole frequency range (DC to more than 10 GHz), but we found it as satisfactory, since its limitations do not impair the differential signalling as much as it would be the case for the single-ended signalling. All microstrip transmission-line interconnections between the logic devices are point-to-point to keep and preserve the signal integrity as high as possible. The PRBS differential output has the CML levels and is DC coupled, while the synchronization differential output has the emitter-coupled logic (ECL) levels and is AC coupled. Describing the PRBS core in more detail (i.e. on the schematic level) is beyond the scope of this article, so it is excluded from the further discussion.

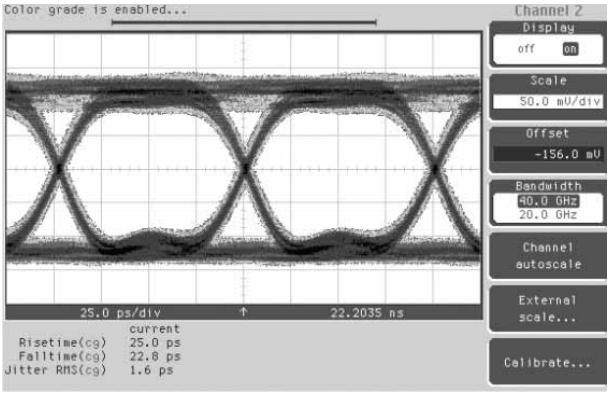

Figure 5: Eye diagram of the output PRBS data.

The calculation of the maximum operating clock frequencies for both methods reveals a big favor to the new single-stage method. If we take into account the real delay values of the traditional linear-feedback shift-register implementation ($T_{D\text{-}FF}$=215 ps, T_{XOR}=135 ps,

T_{setup}=10 ps), using Eq. 1 we obtain the maximum clock frequency of 2.2 GHz for 0 ps delay of the interconnecting transmission lines. Realistically, the interconnection delay would be at least 200 ps, which further limits the maximal operating frequency of the traditional design to 1.8 GHz. The single-stage design can operate at maximum toggle limit, which is more than 12 GHz for the used logic devices in the described generator and that is an increase of more than 6 times.

The 10 GHz clock for the generator is derived from a crystal oscillator running at 155 MHz for an ultra-stable frequency and low phase noise. Several multiplier stages (including filtering, amplifying and multiplying) are used for the frequency multiplication, mostly in steps of doubling the frequency. The filtering from 155 MHz up to 620 MHz is done by lumped components, whereas from 1240 MHz and up to 10 GHz by distributed microstrip filters. Two double-layer FR-4 PCBs are used for the multiplier stages and the multiplier from 620 MHz to 10 GHz is enclosed by a brass housing to minimize the electro-magnetic interference with other circuits within the generator box. Two 10 GHz outputs are single-ended with +4 dBm power level and are AC coupled.

A clock frequency divided by 4 (therefore operating at 2.5 GHz) was added to the system to enable compatibility and to extend flexibility when using older equipment (i.e. sampling oscilloscopes or digital communication analyzers). The divider is composed of a 10 GHz buffer and two :2 divider stages. Its differential output has the CML levels and is DC coupled.

All PRBS generators include a stall-protection mechanism in case of the all-zero state in the linear-feedback shift register. In that case, the generator must automatically recover into the normal state. The described generator includes the maximum-length sequence detection and corresponding automatic recovery in the form of insertion a series of logic ones (high level) into the shift register. When it detects a normal operation, i.e. senses the maximum-length sequence, it disengages the insertion of logic ones into the register. The detection of the maximum-length sequences is done by analog processing (filtering of the first spectral line) of the synchronization output. When the detector senses a spectral line at 10 GHz / 2^{15}-1 = 300 kHz it automatically stops inserting a logic one into the register.

For the final-regeneration D-flip-flop an optimal clock phase was needed to minimize the deterministic and random timing jitter in the output PRBS data. Therefore a phase shifter operating at 10 GHz with more than 360 degrees phase-tuning range was developed with the accompanying 10 GHz amplifier. The amplifier comprises a single high electron mobility transistor (HEMT) on a teflon laminate. The phase shifter is composed of two serially-connected tunable band-pass filters with an intermediate amplifier stage. Each filter is a four-finger interdigital microstrip type with varactor diodes as a tunable elements in each finger. The phase shifter is also built on a 0.5 mm-thick teflon laminate for minimal loss and reliable performance. The final regeneration flip-flop's clock phase is manually adjusted to an optimal position using a resistive trimmer setting the varactor diodes' bias points. The 10 Gb/s PRBS generator prototype is shown in Fig. 6.

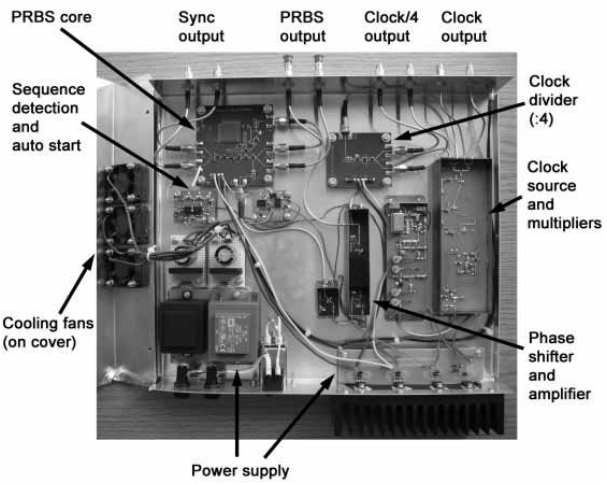

Figure 6: Photograph of the 10 Gb/s 2^{15}-1 PRBS generator.

One of the most simple verifications for the correct operation of the PRBS generators is to check the frequency spacings between the spectral lines of the output PRBS data. The latter must be in precise agreement with the clock frequency divided by the pattern length. In this case the spacing must be 9.95 GHz / 2^{15}-1 = 304 kHz. If the spacing is wider, then the sequence does not

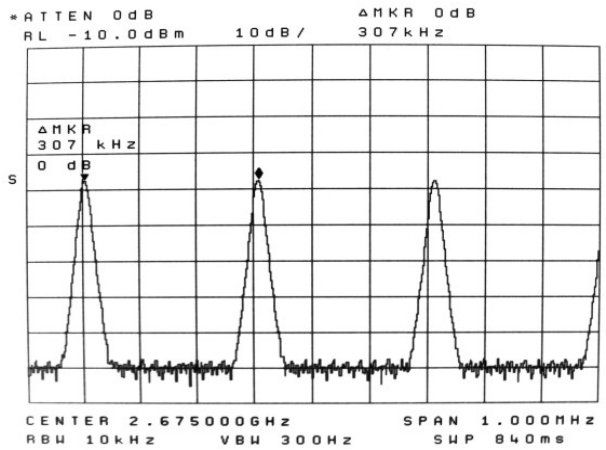

Figure 7: Frequency spacing between the spectral lines of the PRBS data.

have the maximum length and the operation is erroneous. The spacings between the spectral lines of the output PRBS data are shown in Fig. 7 and prove that the sequence has the maximum length (the marker measurement on the used spectrum analyzer has limited resolution and does not show exact spectral-line spacing).

4. Conclusion

The method and design of a PRBS generator operating at 10 Gb/s bitrate was presented. The single-stage implementation of the linear-feedback shift register uses a single retiming stage (D-type flip-flop). If the same logic devices (as built in the generator) would be used in a traditional implementation (the multi-stage chain), the maximum clock frequency would be approximatelly 6 times lower than the clock frequency of the single-stage implementation. The latter is actually equal to the maximum toggle limit of the devices. The single-stage method applies also for the polynomial divider in a PRBS receiver (i.e. bit-error-rate receiver). The 10 Gb/s PRBS generator, producing a pseudo-random pattern length of 2^{15}-1, provides a good data quality with the timing jitter of only 1.6 ps_{rms} at the middle of the eye crossing. Although the PRBS-core circuit was made on the cheap FR-4 laminate, a good performance was achieved due to the fully-differential design. The generator includes also a high-stability clock source and features the pattern-length synchronization. The single-stage-method principles shown in this article are fully scalable to higher clock frequencies. This applies especially for the case of integrated monolithic implementations suitable for and required by the next-generation communication-link bitrates of 80 and 160 Gb/s.

Acknowledgement

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Evaluation of piezoresistive ceramic pressure sensors using noise measurements

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Abstract: The development of low-temperature co-fired ceramic (LTCC) technology is increasing the interest in ceramic pressure sensors (CPS). This technology and materials in combination with conventional thick-film technology offers a feasible solution to increase the sensitivity of pressure sensors and the flexibility in design, both with the aim to replace silicon-based pressure sensors in some applications. The sensor characteristics, i.e., offset stability and sensitivity, are always influenced by the level of electronic noise. We are concentrating our efforts on the use of low-frequency noise as a diagnostic tool for a reliability improvement and sensitivity increase. 1/f noise is dominant in the low-frequency region. It is given by two components; one is connected to the material structure and the second one is influenced by the defects and imperfection in the structure. The measurements of the electronic noise level could be used for an evaluation of different technologies in order to tune the pressure sensor technology and for the evaluation of sensor quality within one technology. We show the correlation between the noise of the sensing resistor technology and the noise of the output voltage on the measured pressure sensor.

Key words: LTCC, noise spectral density, sensitivity, resolution

Evaluacija piezouporovnih keramičnih senzorjev tlaka z meritvijo 1/f šuma

Povzetek: Z razvojem keramičnih tehnologij in materialov z nizko temperaturo žganja (LTCC) se povečuje tudi interes za keramične senzorje tlaka (KST), ki so primerna alternativa silicijevim senzorjem tlaka za nekatera specialna področja uporabe. LTCC tehnologija ponuja nekaj prednosti v primerjavi s konvencionalnimi keramičnimi tehnologijami in je zelo primerna za izdelavo tridimenzionalnih senzorskih struktur. Ena pomembnih prednosti je relativno nizek modul elastičnosti LTCC keramike, ki omogoča doseganje večjih deformacij pod tlačno obremenitvijo in s tem relativno večjo občutljivost senzorja glede na dimenzije. Karakteristike senzorja (stabilnost ničelnega izhoda in občutljivost) pa so odvisne tudi od velikosti električnega šuma izhodnega signala. V tem prispevku obravnavamo meritev nizkofrekvenčnega šuma kot diagnostično orodje za ovrednotenje senzorskih karakteristik in analizo možnosti za izboljšanje resolucije senzorja. 1/f šum je dominanten v nizkem frekvenčnem področju. Podan je z dvema komponentama; prva komponenta je povezana s strukturo uporabljenih materialov in druga komponenta predstavlja vpliv defektov in neidealnosti strukture. Tako lahko meritve električnega šuma uporabimo za evaluacijo različnih materialov in postopkov in na ta način usmerjeno izboljšamo tehnologijo izdelave senzorjev za doseganje optimalnih rezultatov. Predstavili smo korelacijo med šumom debeloplastnih senzorskih uporov in šumom izhodnega signala, ki pomembno vpliva na resolucijo senzorja.

Ključne besede: LTCC, elektronski šum, občutljivost, resolucija

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1. Introduction

The pressure sensor market is dominated by silicon pressure sensors. However, ceramic pressure sensors with a flexible diaphragm have been available for more than 25 years. Ceramic pressure sensors (CPSs), in comparison with semiconductor sensors, are larger, more robust and have a lower sensitivity. But, some new technologies developed in the past few years increase the sensitivity and offer a flexible architecture, with the aim to replace

the silicon-based pressure sensors in some applications. One of these technologies is low-temperature co-fired ceramic (LTCC) technology. Ceramic pressure sensors fabricated using low-temperature co-fired ceramic substrates were studied. LTCC technology and materials in combination with conventional thick-film technology offers a feasible solution to increase the sensitivity of pressure sensors [1, 2, 3]. For the sensor sensitivity increase it is necessary to suppress the electronic noise of the sensor itself, in order to increase the signal-to-noise ratio. The electronic noise level depends on the used materials, i.e., substrates, resistive and conductive pastes, and the resistor geometry. Low-frequency noise in pressure sensors appears during the charge carriers' transport as a result of the carrier interaction with interfaces and defects, on the boundaries among the conductive grains in the resistors structure and on the other scattering centres. The possibility of using noise measurements in the analysis, diagnostics and prediction of the reliability of thick-film resistors was studied before [4, 5].

2. Experimental

2.1 Measured samples

The pressure sensors were fabricated on pre-fired LTCC structures with cavities and thin deformable diaphragms made of the LTCC tape Du Pont 951. On the top of the round diaphragm, four thick-film cermet resistors were connected in a Wheatstone bridge. A photograph of the measured pressure sensor is shown in Fig. 1.

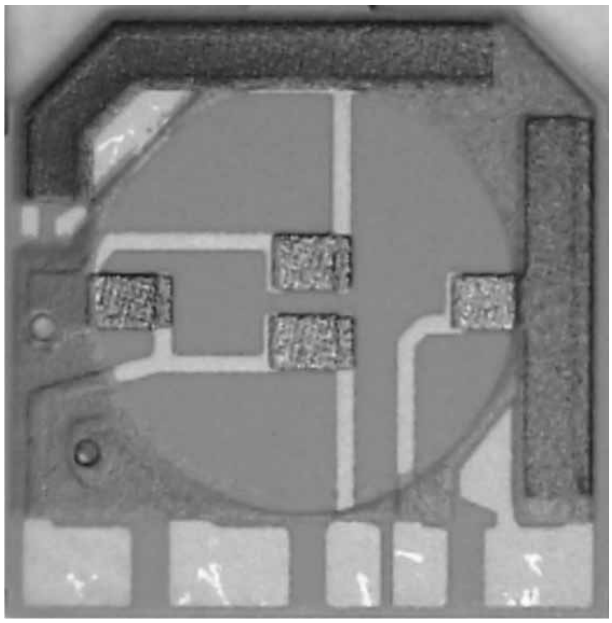

Figure 1: Photograph of the measured pressure sensor (lateral dimensions of 10 mm x 10 mm).

The equivalent electrical circuit of the measured pressure sensor is shown in Fig. 2. Resistors R1, R2, R3 and R4 are sensing resistors on the diaphragm, while resistors R5 and R6 are designed for the tuning of the bridge output and placed at the edges of the substrate (see Fig. 1).

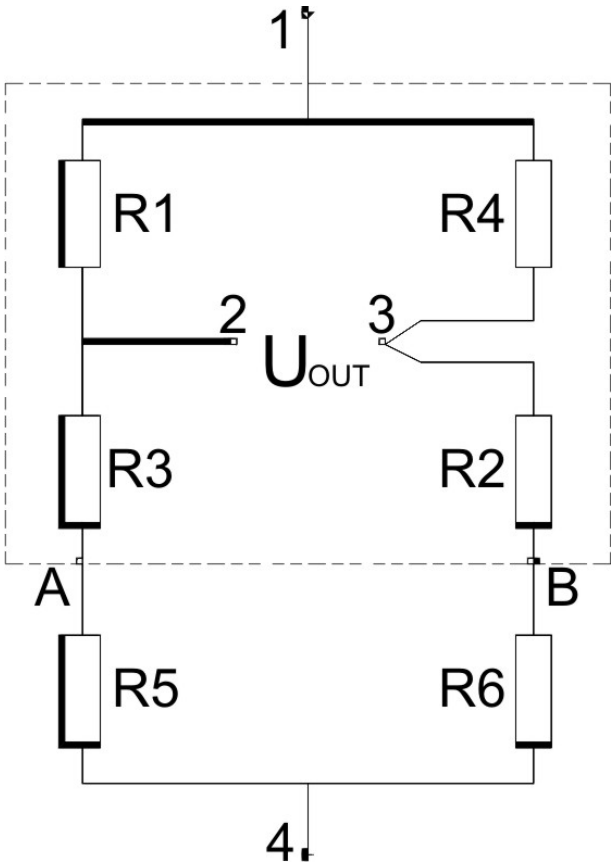

Figure 2: An equivalent electrical circuit of the pressure sensor.

Two types of resistor materials were used: Du Pont resistive paste 2041 (sheet resistance is about 10 kOhm; Gauge Factor is about 10 [6]) – further denoted as Type 1, and Electro Science Laboratories resistive paste 3414 (sheet resistance is about 36 kOhm; Gauge Factor is about 19 [6]) – further denoted as Type 2. Conducting paste DuPont 6143 (Ag/Pd paste) was used for contacts.

The pressure sensor sensitivity is influenced by the materials used for the active resistors R1 to R4. To evaluate the influence of different manufacturing technologies on the sensor noise, special test samples consisting of 12 thick-film resistors with different geometries were prepared on a common LTCC substrate. The layout of these resistors is shown in Fig. 3.

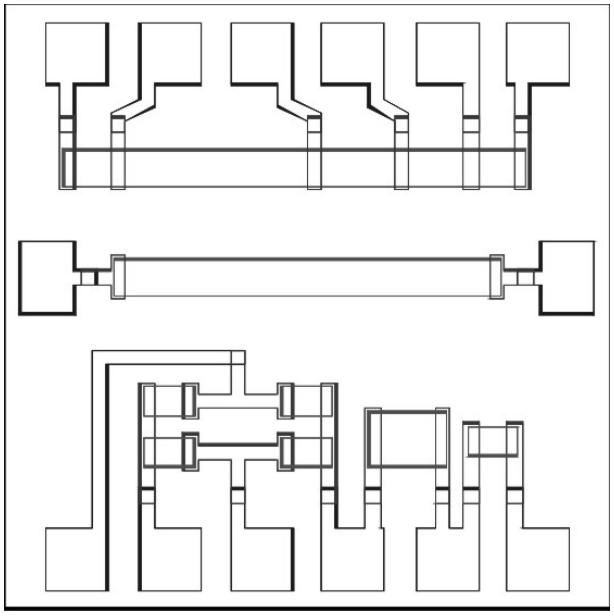

Figure 3: The layout of the test thick-film resistors on the common LTCC substrate (16.6 mm x 16.6 mm).

The test resistors were prepared by different technologies using two different resistive pastes and two conducting pastes (Pd/Ag, 7484 and Au, 8837). The resistors were either screen printed on the green tape and co-fired with the substrate, or printed on the pre-fired LTCC substrate. The resistors made with six different technologies, summarized in Table 1, were evaluated.

Table 1: Description of the technologies for the measured samples

Technology	Resistive paste	Conducting paste	LTCC substrate
TECH 1	2041	7484	green
TECH 2	3414	7484	green
TECH 3	2041	7484	pre-fired
TECH 4	3414	7484	pre-fired
TECH 5	2041	8837	pre-fired
TECH 6	3414	8837	pre-fired

2.2 Low-frequency noise measurements

Low-frequency noise was measured using the measuring set-up according to Fig. 4. The measured noise voltage is pre-amplified using an ultra-low-noise preamplifier a background noise spectral density of 10^{-18} V^2/Hz. Then the signal passes through the band-pass filter and is amplified to the required level. The signal is digitalized and the noise spectrum is calculated in the real time using Fast Fourier transforms.

We measured the fluctuation of the output voltage U_{OUT} on the pressure sensor (voltage between the terminals 2 and 3 – see Fig. 2) for different values of voltage applied on the sensor (between terminals 1 and 2). The output voltage noise spectral density measured for sensor of Type 34 is shown in Fig. 5. The voltage noise spectral density is 1/f type in the range 1–1000 Hz and it can be described by the formula:

$$S_U = \frac{\alpha_H \cdot U_x^{\,2}}{N \cdot f} \tag{1}$$

where S_U is the voltage noise spectral density, U_x is the DC voltage applied to the measured sample, N is the total number of fluctuators, f is the frequency and α_H is the Hooge parameter.

For a stationary and ergodic stochastic process the noise spectral density is proportional to the square of the voltage (see Fig. 6). It is very convenient to normalize the measured noise spectral density for the applied voltage and frequency and to use a noise quality indicator C_Q for the sensor/resistor quality evaluation.

C_Q is a dimensionless parameter with a value dependent on the sample quality and reliability.

$$C_Q = S_U \cdot \frac{f}{U_x^{\,2}} = \frac{\alpha_H}{N} \tag{2}$$

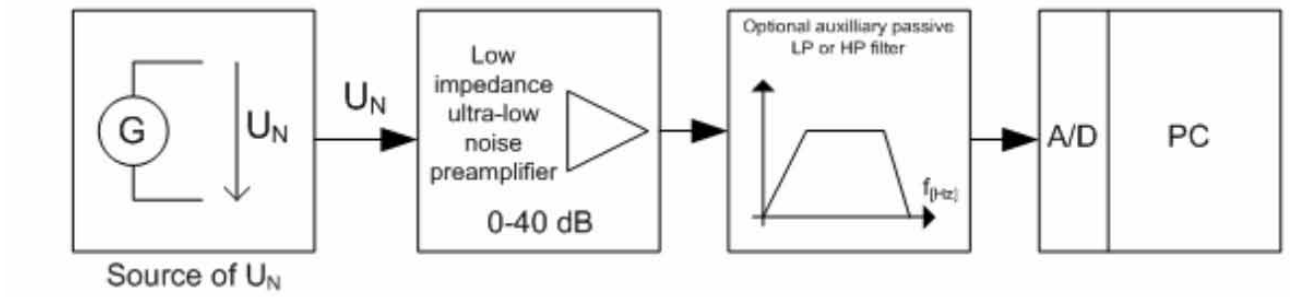

Figure 4: Block diagram of the noise experimental set-up.

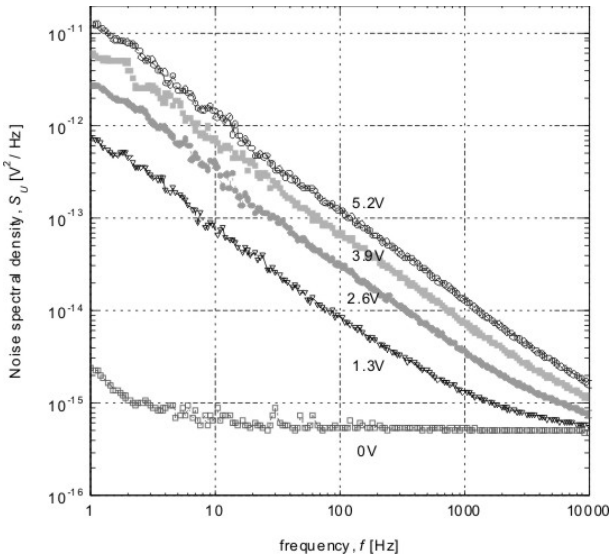

Figure 5: Output voltage noise spectral density vs. frequency for different applied voltages - measured for the pressure sensor Type 2.

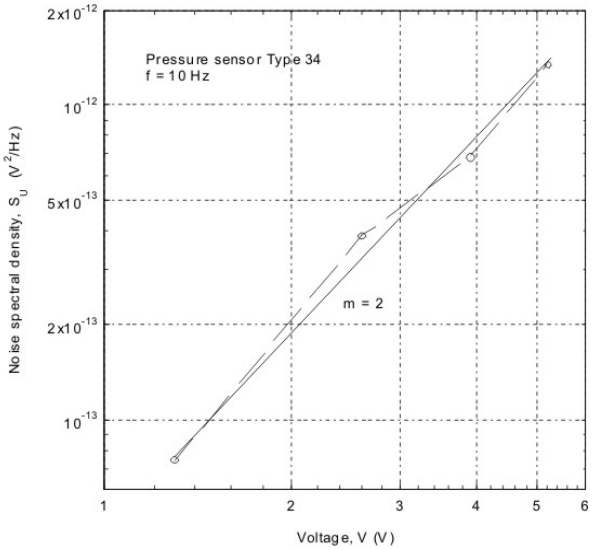

Figure 6: Output voltage noise spectral density vs. applied voltage for the pressure sensor Type 2.

For the comparison of different technologies we measured the low-frequency noise of resistors of sizes 1.5 mm x 1.5 mm, 0.8 mm x 0.8 mm, and the noise of the output voltage on the bridge given by four resistors of size 0.8 mm x 0.8 mm. Two samples of technology 5 and three samples of the other technologies were evaluated. The noise quality indicator C_Q calculated for resistors of size 0.8 mm x 0.8 mm and 1.5 mm x 1.5 mm for different technologies is shown in Figs. 7 and 8, respectively.

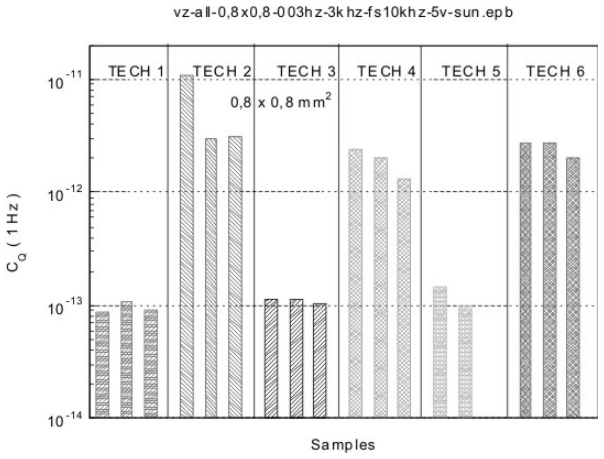

Figure 7: Noise quality indicator C_Q calculated for resistors 0.8 x 0.8 mm^2 for different technologies.

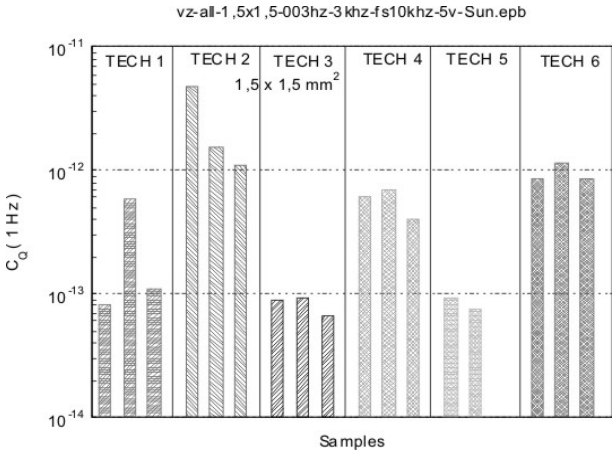

Figure 8: Noise quality indicator C_Q calculated for resistors 1.5 x 1.5 mm^2 for different technologies.

We can see that the noise quality indicator C_Q strongly depends on the resistive paste type. The value of C_Q calculated for the technologies TECH 2, TECH 4 and TECH 6 is about one order of magnitude higher than that obtained for TECH 1, TECH 3 and TECH 5, respectively. Some further influence of the LTCC substrate preparation is observed in the measured data as follows. For the resistors printed on the green tape and co-fired with the substrate a larger distribution of measured data is observed (TECH 1 and TECH 2) compared to the results obtained for the resistors prepared by the same combination of thick-film conductors and resistors that were screen printed on the pre-fired LTCC substrate (TECH 3 and TECH 4). The influence of the resistor size is visible over all technologies. For smaller resistors the noise level increases.

The output voltage noise spectral density frequency dependence measured for an applied voltage of 5.08 V for three bridges of technology TECH 3 and TECH 4,

respectively, is shown in Fig. 9. We can see that the output voltage noise spectral density is two orders of magnitude higher for TECH 4 than for TECH 3.

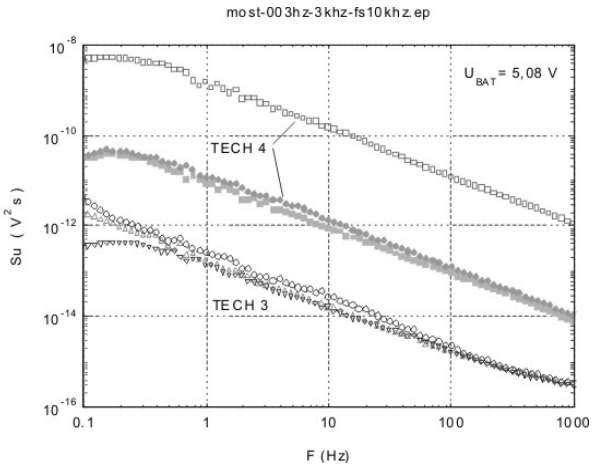

Figure 9: Output voltage noise spectral density vs. frequency for applied voltage 5.08 V - measured for three bridges of technology TECH 3 and TECH 4, respectively.

When we compare the results for the voltage noise spectral density obtained for the single resistor and for these resistors connected to the bridge, we can see that the difference between the technologies TECH 3 and TECH 4 increased for an order of magnitude in the case of resistors connected in the bridge. The value of the output voltage fluctuation influences the offset and the sensitivity of the final pressure sensor.

3. Conclusion

Ceramic pressure sensors based on LTCC technology were evaluated using low-frequency noise measurements. The sensor output voltage noise spectral density is 1/f type in the range 1 to 1000 Hz.

The pressure sensor output voltage noise level influences the background value of the sensitivity of the sensor and this depends on the used material and the technology of the sensing resistors. For the evaluation of the influence of resistive materials (Du Pont 2041 and ESL 3414) and manufacturing technology (co-fired and post-fired resistors) on the sensor noise samples of thick-film resistors prepared on LTCC substrate were studied. A strong influence of the resistive paste type was observed – the difference between the pastes in our case is about one order of magnitude. Some influence of the other parameters, such as LTCC substrate preparation and resistor size, are also presented. The resistors screen printed on the green tape and co-fired with the substrate show a larger distribution of measured data compared to the samples prepared on the pre-fired LTCC substrate. The voltage noise level increases with the decreasing size of the resistors. The influence of the resistive paste type is even more pronounced in the case of the connection of the resistors in the bridge. The difference between the technology TECH 3 and TECH 4 is an order of magnitude for the single resistors and increased up to two orders of magnitude for the case of resistors connected in the bridge. The use of the different conductors in this case study did not reveal a significant influence on the measured results. The best results were obtained with TECH 3 and 5, i.e., the 2041 resistors on the prefired LTCC substrates.

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Time-transfer and synchronization equipment for high-performance particle accelerators

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Abstract: This article talks about accurate time-transfer and synchronization in particle accelerator facilities. Simple industrial solutions like TTL-level pulses and 10 MHz reference clocks distributed over conventional coaxial cables are both much worse than the theoretical limits for timing accuracy, neither do satisfy the requirements of high-performance particle accelerators. Several different approaches to the time-transfer and synchronization problem have been implemented elsewhere. Yet their accuracy is still far from theory limits in most cases. Direct comparisons are difficult due to the very different formats in which the results were published. This article attempts to describe the theoretical backgrounds of timing first, considering natural physical limits rather than particular implementations. Next the limitations of different implementation technologies are examined including practical but very important issues like technology maturity, component availability and obsolescence. Optical-fiber technology is then examined into detail, including all limitations and interface problems with other equipment at both ends of the synchronization links. Different practical approaches using optical fiber as the transmission medium for timing and synchronization are also discussed. At the end, our implementation of a prototype compensated CW modulation timing system is described into detail including the stability-measurement results obtained in a real accelerator tunnel. Industrialization and further developments of our system are also presented. The latter include single-fiber bidirectional operation, already showing further improved timing stability in non-perfect laboratory conditions and a possible development of a high-stability electro-optical master clock oscillator. Our conclusion is that besides the theoretical background a detailed knowledge of many different technologies is required to combine them in a top-performance timing system.

Key words: Timing system, synchronization, technology, optical fiber

Prenos takta in sinhronizacijska oprema za visoko-zmogljive pospeševalnike osnovnih delcev

Povzetek: Predstavljeni članek govori o točnem prenosu časa in sinhronizaciji pospeševalnikov osnovnih delcev. Enostavne industrijske rešitve kot na primer prenos TTL impulzov ali 10 MHz referenčnega takta po konvencionalnih koaksialnih kablih še zdaleč ne dosegajo teoretičnih omejitev točnosti niti ne zadoščajo zahtevam visoko-zmogljivih pospeševalnikov. Za rešitev tega problema je poznanih in implementiranih že kar nekaj prenosnih sistemov. Njihova točnost je v večini primerov žal še vedno daleč od teoretičnih mej. Zahtevne so tudi neposredne primerjave obstoječih sistemov, saj so merilni rezultati predstavljeni v različnih formatih in izmerjeni na različne načine. V članku je sprva opisano teoretično ozadje prenosa točnega časa. Pri tem je bolj kot na dejanskih prenosnih sistemih poudarek na naravnih fizikalnih zakonih in omejitvah. V nadaljevanju sledi pregled različnih tehnologij prenosa, njihovih praktičnih omejitev, zrelosti tehnologije ter dobavljivosti komponent. Uporaba optičnih, vlakenskih tehnologij je nato predstavljena bolj podrobno. Opisane so omejitve ter vmesniški problemi z ostalo opremo na obeh koncih sinhronizacijske povezave. Predstavljeni so tudi različni praktični načini sinhronizacije z uporabo optičnih vlaken kot prenosnim medijem. Na koncu je predstavljen tudi izdelani prototip za stabiliziran prenos moduliranega optičnega signala preko optičnih vlaken. Podane so meritve stabilnosti, izmerjene v pospeševalniškem tunelu ter nakazane bodoče industrijske izboljšave. Ena od njih vključuje prenos mikrovalovnega takta po enem samem stabiliziranem optičnem vlaknu. Prvi testi že kažejo izboljšanje stabilnosti pri prenosu, omenjeni princip pa je mogoče uporabiti tudi pri razvoju visoko-stabilnega elektro-optičnega oscilatorja. Iz navedenega je mogoče zaključiti, da je poleg teoretičnega ozadja, potrebno zelo podrobno poznavanje različnih vrst tehnologij, ki na koncu sestavljajo dovršen sinhronizacijski sistem.

Ključne besede: Sistem za prenos časa, sinhronizacija, tehnologija, optično vlakno

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1 Introduction - Timing accuracy: jitter and drift

One of the design requirements of modern particle accelerators is precise timing and synchronization of the machine components and user experiments at different physical locations [1, 2]. Before designing a high-accuracy timing system, some basic definitions and limitations need to be considered first to select the most suitable technology for a certain task.
Timing accuracy includes at least two different specifications, short-term inaccuracy described as phase noise or jitter and long-term inaccuracy described as wander or drift.

1.1 Jitter

Jitter is mainly caused by random noise added to the timing (clock) signal as shown in Fig. 1.

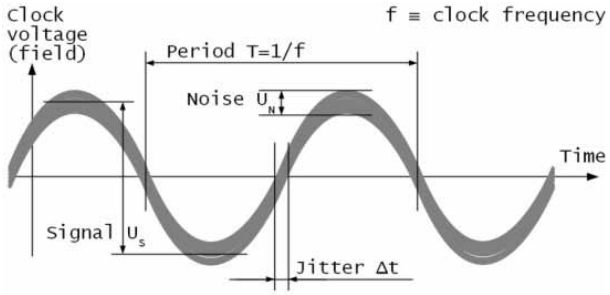

Figure 1: Signal-to-noise ratio and timing jitter.

The resulting jitter Δt is a function of the clock period T (or frequency f) and the signal-to-noise ratio.

$$\Delta t = \frac{T}{2\pi} \cdot \frac{U_N}{U_S} = \frac{1}{2\pi \cdot f} \cdot \sqrt{\frac{P_N}{P_S}} \tag{1}$$

Please note that the signal-to-noise ratio may be expressed in many different physical quantities. Voltages are usually used for electrical signals. Signal and noise powers have a more general meaning. Noise may come from many different sources. Natural noise sources like thermal noise or quantum noise shown in Fig. 2 can not be avoided.

Noise power is usually reduced by narrow-band filtering with resonators having a quality Q. The filter bandwidth $B=f/Q$ is orders of magnitude smaller than the clock frequency f. In narrow-band systems the noise power is simply described by its spectral density N_0. In an electrical timing system operating in the radio/microwave frequency range, natural noise is manly thermal noise. The resulting jitter is inversely proportional to the square root of the frequency.

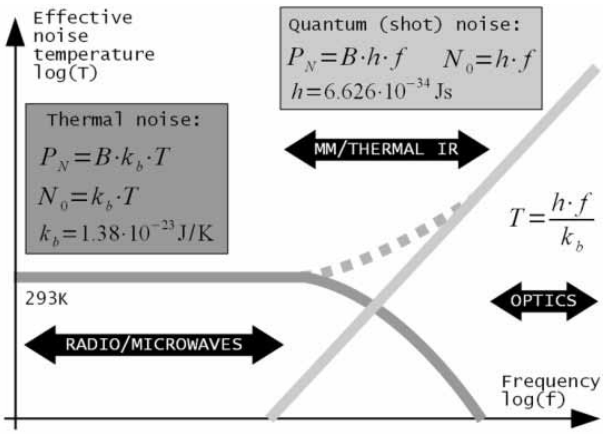

Figure 2: Thermal and quantum noise.

$$\Delta t = \frac{1}{2\pi} \cdot \sqrt{\frac{k_b \cdot T}{f \cdot Q \cdot P_S}} \tag{2}$$

Therefore the performance of such a timing system improves at higher frequencies provided that all of the remaining design parameters remain the same. In an optical timing system operating at visible light or near IR, natural noise is mainly quantum (shot) noise. The resulting jitter is frequency-independent.

$$\Delta t = \frac{1}{2\pi} \cdot \sqrt{\frac{h}{Q \cdot P_S}} \tag{3}$$

Please note that the resonator Q is limited by its mechanical stability and thermal drift in all cases. Therefore there is no particular theoretical advantage in using optical or even higher frequencies for timing.

1.2 Drift

Drift is mainly caused by temperature and other environmental variations, by power-supply variations, by component imperfections like AM-to-PM conversion, by component degradation & aging etc. Drift is not directly related to the theoretical design parameters of a timing system like its clock frequency. On the other hand, drift is related to the technologies used and in particular to their state of maturity.

2 Component Technologies

20 or 30 years ago it was considered that component reliability could be designed into the component itself by very simple means. For example by choosing the right manufacturing process or better packaging for industrialgrade parts. Additional inspections and screening was used for military/aerospace-grade parts. Econo-

mies of scale first hit the personal-computer market. In just 10 years, the personal computer evolved in a top-technology item in 2000. After 2000 inexpensive personal computers with GPU computing (GPU – Graphic Processing Units) quickly displaced much more expensive workstations and other computing hardware [3].

A quality quantum leap was achieved in mobile telephony. Highly-reliable mobile phones had to be manufactured in large volumes at consumer prices but respecting industrial or military quality standards. The distinction among consumer, industrial and military grades suddenly disappeared.

The reliability of modern electronic and optical components is no simple matter. The most obvious example are the failure mechanisms of semiconductor lasers. Individual component screening like performed on military-grade parts many years ago does not help. The correct answer is learning from mass production in million series and correcting the manufacturing process all of the time [4]. This simply means that specialized components can no longer be produced, at least not at the reliability levels that are obvious today.

An increasingly important component issue is complexity. Component complexity is not limited to software, although the latter is the most obvious complexity issue. The hardware design of most electronic and optical components has become so complex that the design of specialized components can no longer be afforded by a small group of engineers, especially not in the limited amount of time allowed by practical projects.

Finally, a completely new problem appeared in the 21st century called component obsolescence. Economies of scale also dictate that the production of a particular component is dropped as soon as the latter becomes obsolete. Due to the component complexity it is usually difficult to have it manufactured at a different location or find similar plug-in replacements.

As shown in Table 1, a design engineer has to be extremely careful while choosing the technologies for a new product. While there are some mass-produced and inexpensive components with fantastic performance, there are many technology failures as well. The support to some frequency ranges and applications may be missing. Even successful technologies may be affected by component obsolescence.

Table 1: Technology successes and failures.

Technology successes	Technology failures
Analog radio/microwave electronics	Millimeter-wave electronics
High-speed digital electronics	RF micro-electro-mechanical devices (RF MEMS)
(Electronic) digital signal processing (DSP)	Long-wave (thermal) IR optics
Silica-glass optical fiber (waveguide)	Fiber-optic laser sources (oscillators): CW, pulsed, mode-locked
Semiconductor lasers, modulators and photo-detectors	Optical signal processing (holography, nonlinear optics)
Erbium-doped fiber laser amplifier (EDFA)	Optical computing

3 Fiber-optic technology

The availability of inexpensive optical fiber triggered the development of all related components: splices, connectors, LED and LASER transmitters, modulators, isolators, circulators, PIN and avalanche photo-diode receivers and even Erbium-doped fiber-optic LASER amplifiers [5]. All these new components changed the meaning of the word optics. Traditionally, optics meant bulk optics with lenses, mirrors and various cumbersome components on optical benches in clean-room environments, requiring precise handling and extremely sensitive to dirt, moisture and vibration. On the other hand, optical fiber and all fiber-optic components are designed right from the beginning for simple handling, stable and reliable operation in the most unforgiving environments ranging from the ocean floor [6] up to the geostationary orbit [7].

Yet optical fiber does have some limitations that have to be understood in order to design a successful system. The most obvious limitation is the frequency or wavelength range. Silica glass only works in the visible and near-infrared range. Other optical-fiber limitations are shown in Fig. 3.

Standard Telecom G.652 single-mode optical fibers have chromatic dispersion due to both waveguide and material effects [8]. Rotationally-symmetrical fibers do not maintain polarization. The random coupling between the two degenerate fundamental modes causes Polarization mode dispersion (PMD). The refractive index of silica glass has a large temperature coefficient. The latter may become unpredictable and up to an order of magnitude larger due to improper (tight) cabling

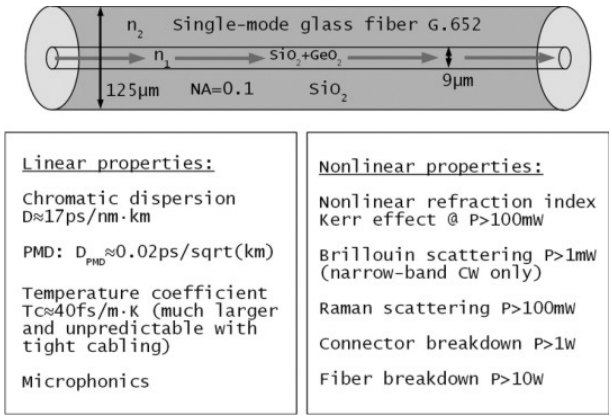

Figure 3: Single-mode optical-fiber properties.

like used in patchcords or FTTH cables [9, 10]. Although much less sensitive to vibration than bulk optics, microphonics may still represent a problem in high-accuracy fiber-optic systems.

A major disadvantage of fiber-optic technology is fiber non-linearity. In most cases the fiber signal power is limited to about 100 mW due to both Kerr and Raman effects. Coherent systems using very narrow-band optical signals may be limited to power levels below 1 mW due to Brillouin scattering.

4 Optical timing systems

The typical distance to be covered by a timing system in a particle accelerator ranges from a few hundred meters to a few ten kilometers. At these distances coaxial cable becomes bulky and lossy as the clock frequency is increased to improve accuracy [11]. Optical fiber is an excellent substitute offering low loss at light-wave frequencies. Usually, no amplification is required in an optical-fiber system up to at least 50 km. As shown in Fig. 4, optical timing systems include:

- Optical CW systems,
- Pulsed systems and
- CW modulation systems.

4.1 Optical CW systems

Optical CW systems should offer the highest resolution and accuracy due to the high clock-signal frequency. Unfortunately the resulting 5.16 fs timing ambiguity at 194 THz is too small for practical applications. Vibrations might cause cycle slips and the system phase can never be recovered after any power down. The extremely narrowband optical signal causes interferometric noise and triggers Brillouin scattering. Polarization changes and PMD in optical fibers are a big problem. Last but not least, no user equipment is currently available that

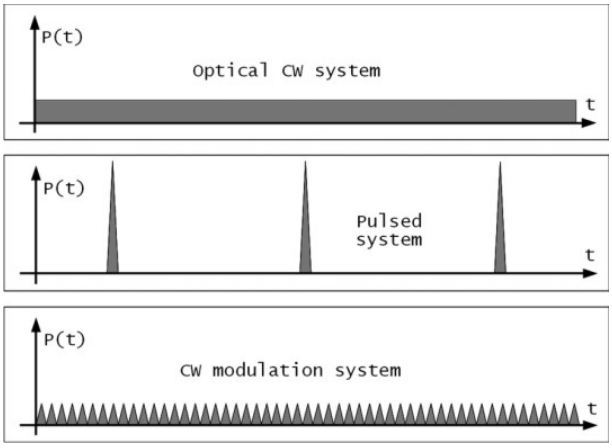

Figure 4: Optical timing systems.

could use the timing information of an optical carrier directly. However, an optical CW signal can be used for optical-link stabilization with an interferometer setup, as shown in [12, 13].

4.2 Pulsed systems

Pulsed systems use an optical carrier while the timing information is carried in the pulse envelope [14, 15]. The spectrum of the latter may extend in the millimeter/long-wave IR to offer precise timing and avoid phase ambiguity at the same time. Unfortunately, pulsed systems are affected by fiber non-linearity, chromatic dispersion and PMD. Compensation of the fiber thermal coefficient is very difficult. Pulsed systems are well understood by the user community although optical signal processing is not here yet and the electrical signal-to-noise ratio from a photodetector may be poor.

4.3 CW modulation systems

Replacing a few large pulses with many more smaller pulses results in a CW modulation system [16-19]. Fiber nonlinearity can be avoided due to the lower peak power. The signal distortion caused by chromatic dispersion and PMD is much less critical than in pulsed systems. Standard, mass-produced, inexpensive, high-performance and high-reliability Telecom components may be used. The electrical input and output of CW modulation systems interface to user equipment directly just like coaxial cable. Unfortunately, the timing jitter of CW modulation systems is rather poor. Most of the signal-to-noise degradation comes from the impedance mismatch between the photo-diode and following electrical amplifier as shown in Fig. 5.

Assuming an electrical noise temperature of T=300 K and a parasitic capacitance of C=1 pF (sum of photodiode and amplifier input) results in a noise voltage of

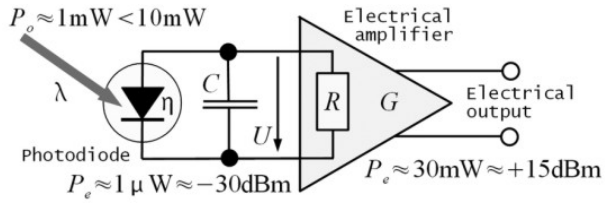

Figure 5: Photo-diode receiver.

U_{Neff}=25.7 μVeff (from Eq.(4)) independent of the frequency range.

$$U_{Neff} = \sqrt{\frac{k_B \cdot T}{2\pi \cdot C}} = 25.7\mu V_{eff} \quad (4)$$

The timing jitter can be reduced by averaging many small pulses. In other words, each small pulse just adds a small amount of momentum to a large flywheel. In electrical terms the flywheel is a narrow band-pass filter. The electrical flywheel is built as a high-Q resonator or VCXO PLL as shown in Fig. 6.

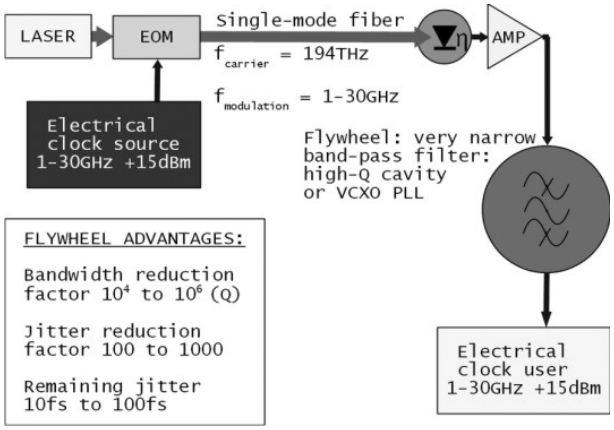

Figure 6: CW modulation system with flywheel.

A high-Q resonator allows a bandwidth reduction in the range between 10^4 and 10^6. The jitter reduction goes with the square root of the bandwidth reduction, resulting in a jitter reduction factor between 100 and 1000.

In a CW modulation system, the optical carrier is not coherent with the timing modulation. Therefore the optical carrier frequency may be modulated to avoid Brillouin scattering. Even more important, changing the optical carrier frequency together with the fiber chromatic dispersion can be used for small adjustments of the group velocity and overall system delay.

As shown in Fig. 7, delay-variation compensation can be achieved in different ways. Fast variations like vibrations can be compensated by electrically tuning the DFB LASER over a restricted bandwidth of just +/-0.1 nm in a very fast way (τ =1 μs). Medium-speed variations can be corrected by thermally tuning the DFB LASER over +/-2 nm (τ =1s). Slow variations like temperature changes of the transmission fiber can be adjusted by heating or cooling a spool of compensating fiber (τ =100 s).

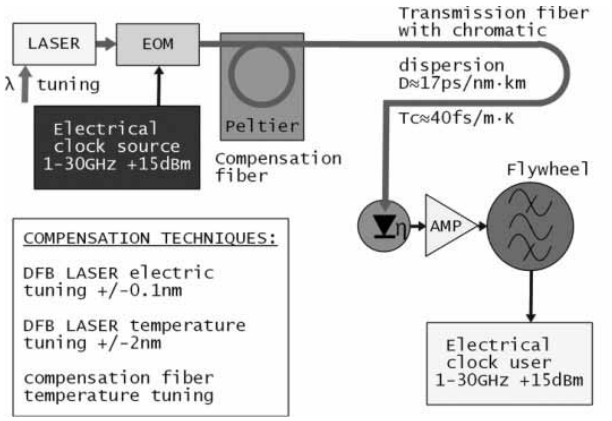

Figure 7: Delay-variation compensation techniques.

5 Prototype compensated CW modulation system

A prototype CW modulation system Libera Sync was built by Instrumentation Technologies [20] for the accelerator "FERMI" distributing a 3 GHz clock over distances up to 300 m. A fiber pair made of two identical optical fibers in the same cable was used for clock distribution. In this way the actual delay could be measured at any time and any variations compensated immediately.

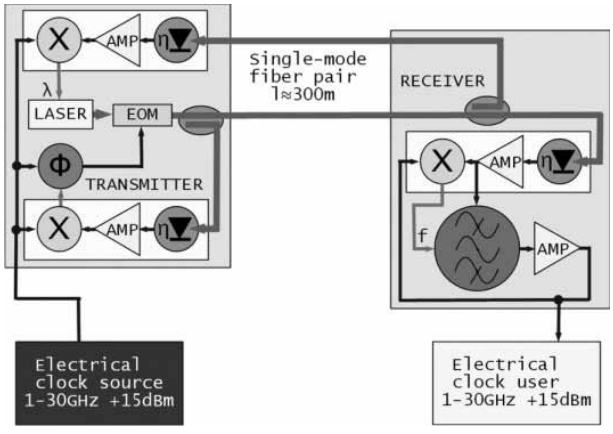

Figure 8: Compensated CW modulation system.

The block diagram of the 3 GHz compensated CW modulation system is shown in Fig. 8. A flywheel resonator with the $Q \approx 10^4$ was used to reduce the timing

jitter. For the phase noise evaluation of the system, a signal source analyser (SSA) Agilent E5052B was used. The phase noise of the 3 GHz signal source is plotted in Fig. 9 (dark curve) in the frequency range from 100 Hz to 10 MHz. The phase noise after Libera Sync is plotted with a bright curve in the same graph. The noise floor of the SSA is at least 10 dB lower then measured curves. The integrated jitter increases from 12.4 fs_{RMS} at the system input (source+SSA) to 13.4 fs_{RMS} at the system output (source+Libera Sync+SSA). The added jitter can be then calculated as

$$jitt_{add} = \sqrt{jitt^2_{source+sys} - jitt^2_{source}} = 5fs_{RMS} \quad (5)$$

Figure 9: Measured phase noise and calculated jitter at 3 GHz: dark curve – the phase noise of the signal source and bright curve – the phase noise at the output of the Libera Sync timing system.

In order to compensate for long-term variations and/or drift, Libera Sync includes three identical receiving blocks. The first receiving block is located in the transmitter to compensate for any phase-shift changes in the transmitter. The second receiving block is also located in the transmitter to compensate for transmission-line-delay variations. Finally, the third receiving block is located in the receiver and compensates for any delay variations of the flywheel resonator.

All three receiving blocks are built using matched components kept in precisely-controlled environments. Further there is a spool of two identical compensating fibers for the forward and backward signal paths that is omitted on Fig. 8 for simplicity. The spool is heated or cooled by a Peltier heat pump.

The long-term phase stability of the proposed system was measured with the the measurement setup shown in Fig. 10a. The RF master-source signal was compared to the signal transfered over the compensated optical link with an independent phase detector. The phase detector (Analog Devices AD8302) was installed in its own, thermally-stabilized enclosure. The detected phase difference on the phase detector was measured with a Datron 1281 multimeter and sampled with a computer acquisitioning system (sampling integration time 5 seconds). The phase stability of the measurement system was 2.5 fs_{RMS} (10 fs_{pp}), observed in 72 hours. The measured long-term drift of the timing system is shown in Fig. 10b. The measured drift is 9.5 fs_{RMS} in 24 hours and 13.4 fs_{RMS} in 38 hours for an installed fiber length of 360 m in the FERMI accelerator tunnel.

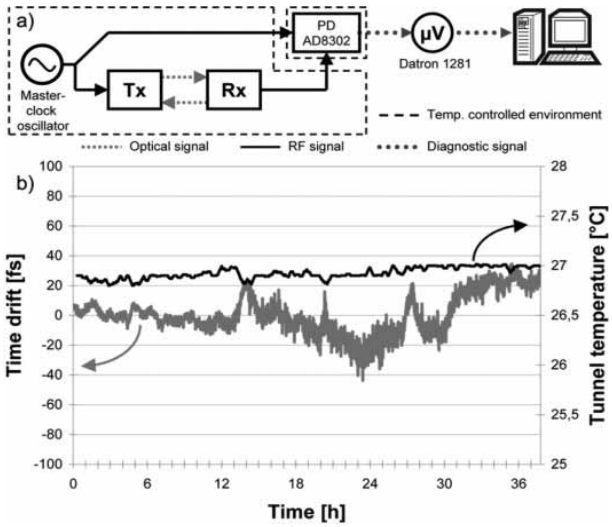

Figure 10: a) Long-term stability measurement setup. b) Measured long-term drift at 3 GHz of a 2-fibre system in the accelerator tunnel.

The achieved long-term phase stability and the value of added jitter are in the same range (below 10 fs_{RMS}) as reported in other advanced optical timing systems working at the same or similar clock frequencies.

6 Further fiberoptic developments

The initial Libera Sync prototype was designed for short distances up to about 300m, where fiber-to-fiber matching is excellent and PMD is not an issue. At longer distances (3 km to 10 km) a Faraday mirror becomes necessary to use a single fiber and compensate PMD precisely as shown in Fig. 11. Some preliminary tests on a single-fiber system have been made under quite noisy laboratory conditions with several degrees centigrade of day/night temperature fluctuations. A 300 m long single-mode fiber on a spool of 1.5 m diameter was used. The measured long-term drift is 20.4 fs_{RMS} in 13 hours as shown in Fig. 12. The signal was picked-up directly after pre-amplifier in the receiver and compared to the reference as shown in Fig. 10a. No additional signal filtering was used in this particular measurement.

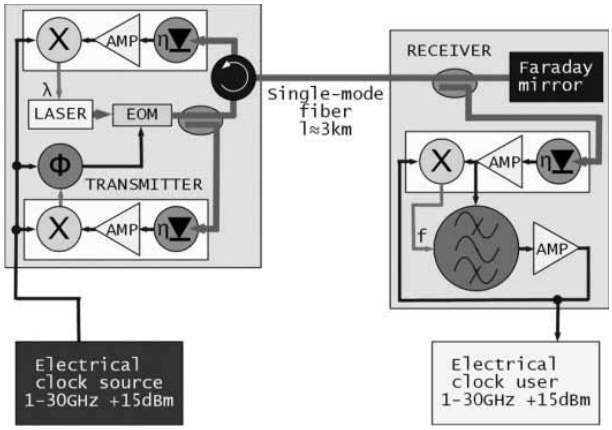

Figure 11: PMD compensation with a Faraday mirror.

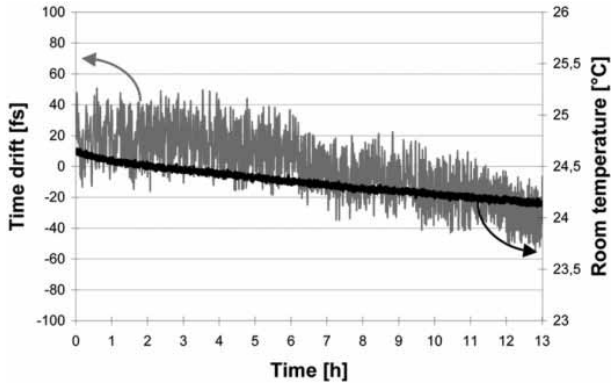

Figure 12: Measured long-term drift at 3 GHz of a single-fibre system placed in noisy laboratory conditions.

Finally, the same design and control technologies can be used to design a top performance, extremely low phase noise master oscillator as shown in Fig. 13. The combined effect of the fiber delay and flywheel resonator is an effective *Q* in the range between 10^5 and 10^7.

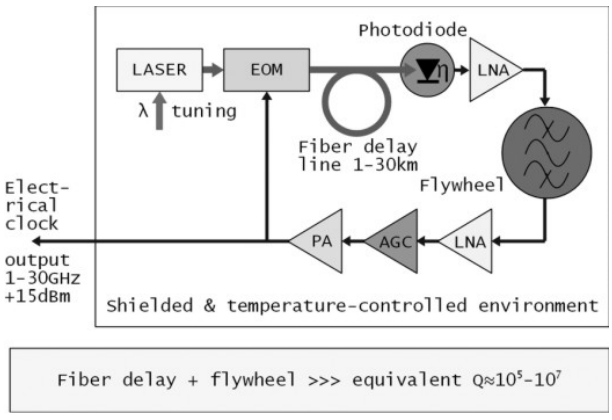

Figure 13: Electro-optical master oscillator.

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Compact Multilayer Bandpass Filter with Modified Hairpin Resonators

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Abstract: Compact selective bandpass filter, based on the Rhodes approximation, is proposed using the novel modified hairpin resonators realized on a double-sided microstrip. The equivalence is presented between the hairpin resonator realized on a single-sided microstrip and the modified hairpin resonator realized on a double-sided microstrip. The footprint area of the filter is reduced by 50% with the multilayer realization. The proposed design methodology is exemplified by a fourth-order multilayer bandpass filter, which is fabricated and measured. The simulated and measured results are in agreement.

Key words: Bandpass filter, modified hairpin resonator, multilayer realization, Rhodes approximation

Kompaktni večslojni pasovni prepusti filter z modificiranimi resonatorji v obliki lasnic

Povzetek: Predlagan je kompaktni selektivni prepustni pasovni filter na osnovi Rhodesove aproksimacije in uporabe novih modificiranih resonatorjev v obliki lasnic. Filter je realiziran na dvostranskem mikrotraku. Predstavljena je primerjava med lasničnimi resonatorji na enostranskem in dvostranskem mikrotraku. Površina odtisa filtra je pri uporabi večslojne realizacije zmanjšana za 50 %. Predlagana metodologija dizajna je predstavljena na, izdelanem in izmerjenem, večslojnem propustnem pasovnem filtru četrtega reda. Rezultati simulacij se dobro ujemajo z meritvami

Ključne besede: prepustni pasovni filter, modificiran lasnični resonator, večslojna izvedba, Rhodesova aproksimacija

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1. Introduction

With the development of modern wireless communications, designing compact and high-performance microwave filters in communication systems is largely required, which exhibit frequency and time-domain requirements.

Among the bandpass filter types, the parallel-coupled half-wavelength resonator filter (PC λ/2) has been widely used for filter structures in wireless systems up to now because of its simple design and easy to control the bandwidth by changing the coupling strength between resonators [1]. However, this filter realization is too large to be used for wireless handset communication systems, where engineers are always looking for smaller microwave components [2]. Several microstrip single-layer structures have been proposed in order to minimize the filter size: the U-turn hairpin [3] resonator, the open-loop resonator [4], the slow-wave resonator [5], and the spiral resonator [6] reduce the size of the parallel-coupled line resonator by folding the resonators to get a more compact configuration.

Another method to reduce the size of filter realizations consists on using multilayer structures. In [7, 8], multilayer bandpass filters, based on resonators with different geometries (square-loop, hairpin, etc.), have been proposed. This multilayer topology consists of two layers of microstrip hairpin resonators. Each resonator itself is printed on a single layer. To ensure couplings between the resonators in the upper layer and those in the lower one, two rectangular slots are etched in a common ground plane placed between the two layers. Using this configuration, the size of the proposed filter can be reduced to half that of conventional microstrip filters.

In this paper, a new method for filter size reduction has been proposed. A novel double-sided microstrip reali-

zation of a narrow bandpass filter is presented that uses modified hairpin resonators (MHR). Arms of each resonator are printed in different layers – the upper and the lower dielectric layer separated by a common ground plane, which can be referred to as a double-sided microstrip. There is no coupling between the arms of the proposed resonator. The arms are connected by a via which passes through the structure without electrical connection to the common ground plane. The undesirable couplings between resonators are minimized as follows: (a) the arm on the lower layer (of each resonator) is shifted with respect to the arm on the upper layer, (b) the structure is housed in a metallic box, and (c) the distance between the top/bottom cover and dielectric is about substrate thickness.

We compare the characteristics (frequency response and footprint) of the hairpin microstrip realization and the proposed multilayer realization. We explain the design methodology and show the results generated by electromagnetic (EM) simulation and the measurement results made on the fabricated structure. Hence, conclusions are drawn about the performance of the analyzed structure.

2. Design of Modified Hairpin Resonators for Multilayer Bandpass Filter

As is known, the open-line resonator (Figure 1a), implemented on a single layer, is folded to form the hairpin resonator (Figure 1b) in order to reduce the size of the parallel-coupled half-wavelength resonator filter (Figure 2a). In the hairpin filter (Figure 2b) the separation between arms (d_0) should be large enough to minimize undesirable coupling between the arms, so that the equivalence of Figure 1 holds.

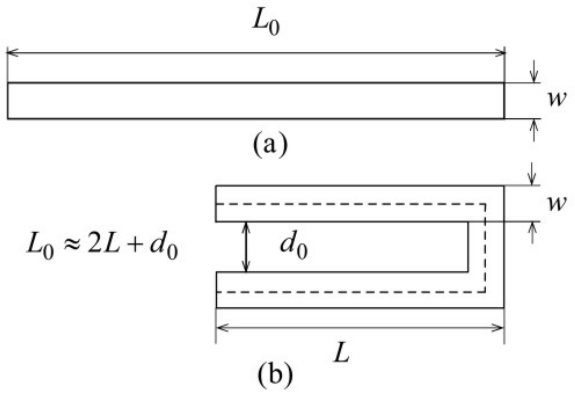

Figure 1: Standard realization of (a) the open-line and (b) the hairpin microstrip resonators.

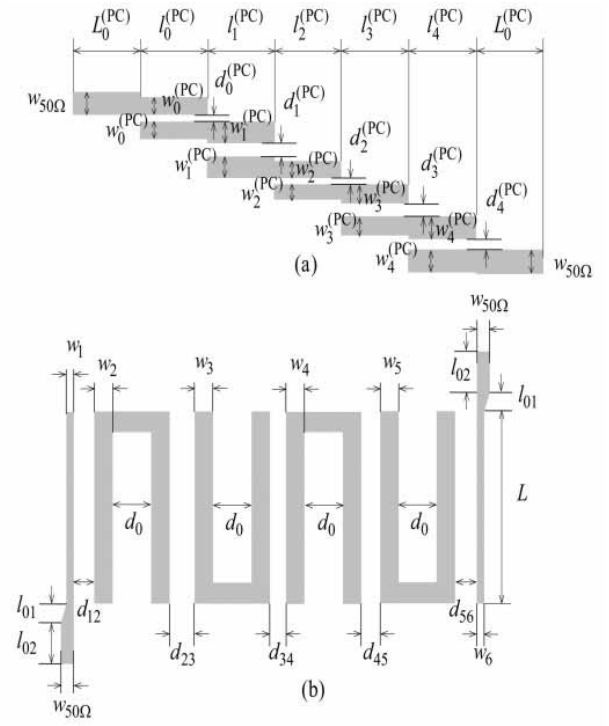

Figure 2: (a) The parallel-coupled half-wavelength resonator filter, (b) the hairpin filter.

To measure the undesirable coupling between the arms of a hairpin resonator we analyzed a symmetrical pair of coupled microstrip lines, and computed (1) the ratio between elements of the characteristics impedance matrix $r_c = |Z_{c12}/Z_{c11}|$ and (2) the ratio between transmission scattering parameters $r_1 = |S_{21}/S_{31}|$, $r_2 = |S_{41}/S_{31}|$.

In this study, we use the Rogers RO4003C substrate: ε_r=3.55±0.5 [9], tanδ=0.0021, thickness of copper foil t = 0.03 mm, and thickness of substrate h = 0.508 mm. The resonant frequency is 2GHz, which corresponds to L0 = 45.3 mm and w = 1 mm. The distance between the hairpin resonator arms is taken from the range $3h \le d_0 \le 20h$ and L = 23 mm.

The ratios r_c, r_1, and r_2 have been computed for various d0. It was estimated that, from the filter design viewpoint, each ratio should be less than 0.01 in order to keep the undesirable coupling sufficiently low, Figure 3. Consequently, for the substrate considered the separation between the arms should be about 10h which increases the footprint of the hairpin filter.

A technique to reduce the undesirable coupling between the arms, and to keep d_0 as small as possible, is to house the filter in a metallic box. The distance, designated by h_u, between the top cover and dielectric is found to be within the range $h \le h_u \le 2h$.

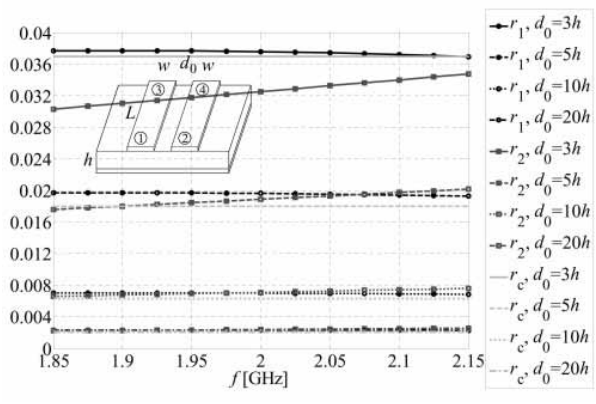

Figure 3: Measure of undesirable coupling between the arms of the hairpin resonator from Figure 1b.

In this paper, we present a new method of further reducing the size of the resonators that constitute the filter by printing the arms in two layers. This multilayer topology consists of two dielectric layers separated by a metallic foil (common ground plane). One arm of a hairpin resonator is printed on the top layer and the other arm is printed on the bottom layer as shown in Figure 4. Since the dielectric layers are separated by a common ground plane, there is no coupling between the arms. The arms of a resonator are connected by a via that passes through the structure without electrical contact with the common ground plane. The length of the via is $H = 2h + h_0 \approx 2h$, where $h_0 = 2t$.

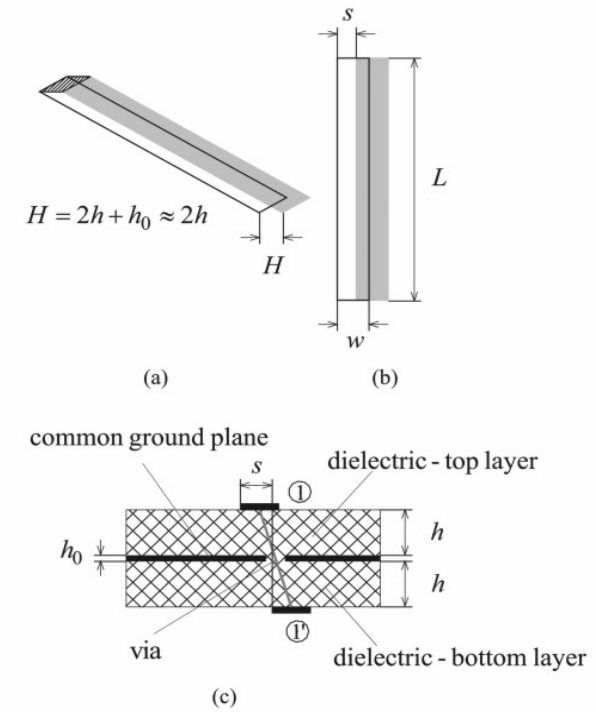

Figure 4: Modified hairpin resonator: (a) 3D view (without the dielectric and common ground plane), (b) top view, and (c) cross section.

The proposed resonators are edge-coupled with quarter-wavelength sections. In order to realize this coupling with only quarter-wavelength sections, the arm on the lower layer (of each resonator) is shifted (for *s*) with respect to the arm on the upper layer (Figure 4b-c). This arrangement of resonator arms minimizes the undesirable couplings between resonators.

Two edge-coupled modified hairpin resonators are shown in Figure 5. The distance between the coupled quarter-wavelength sections is *d*. The shift between the arms of each resonator is designated by s_i, i = 1,2. Sometimes, the distance between the arms of adjacent resonators (D_0) is not sufficient to minimize the undesirable coupling between adjacent sections (on the same side) which should not be coupled. In this case, housing a structure in a metallic box is used to reduce undesirable couplings with the distance between the top/bottom cover and dielectric of $h \leq h_u \leq 2h$.

The main idea of the method is to reduce the size of a hairpin filter by transforming its resonators into a multilayer structure, but without deteriorating the filter performance. With this approach, the size reduction is about 50%.

This method can be summarized as follows:
Step 1. Design the optimal single layer hairpin filter housed in a metallic box.
Step 2. Modify the hairpin filter by printing each resonator in two layers. Preserve the resonator width, the distance (gap) between the edge-coupled quarter-wavelength sections, and the length of the arms. A short microstrip line which connects the arms in a single layer design is replaced by a thru via in a multilayer design. To achieve the equivalence between the single layer hairpin resonator and the multilayer modified hairpin resonator, the length of the via and the via pad should correspond to the line that connects the arms. House the multilayer filter in a metallic box and preserve the distance between the top/bottom cover and dielectric as designed in Step 1.
Step 3. Find the minimal distance D_0 between two adjacent arms, printed on the same layer, that belong to adjacent resonators, but which should not be coupled.

3. Design Example and Experimental Results

In this paper, we consider the fourth-order bandpass filter centered at f_0 = 2GHz, with a relative bandwidth $B = 0.05$, and nominal impedances (at both ports) Z_0 = 50Ω. The maximal insertion loss at the center frequency is A_0 = 3.5 dB and the return loss in the passband is

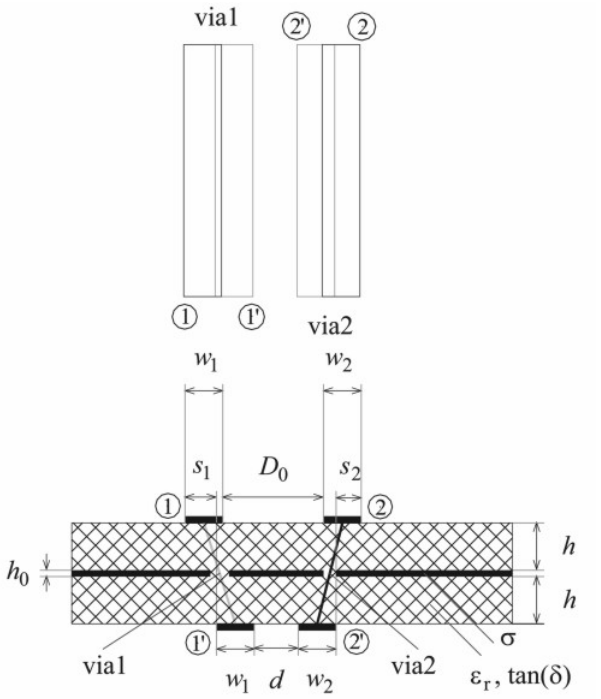

Figure 5: Two adjacent MHRs that are edge-coupled with quarter-wavelength sections.

better than 12 dB. The filter is based on the Rhodes prototype [10], [11]. The filter is housed in a metallic box and the distance between the cover and the dielectric layer is $h_u = 1.5h$.

Coupling coefficients and external quality factors of the hairpin resonators are computed as described in [12]: $M_{12} = 0.032$, $M_{23} = 0.049$, $M_{34} = 0.091$, $Q_{ex1} = 29.94$, $Q_{ex4} = 9.77$.

To estimate the range of possible widths and gaps between the hairpin resonators, first we designed the corresponding parallel-coupled half-wavelength resonator filter with the metallic cover. The dimensions of coupled lines are determined to correspond to the even- and odd-mode impedances $(Z_{0e})_{j,\,j+1}$ and $(Z_{0o})_{j,\,j+1}$ [13], Table 1. It was found that the relevant ranges are: $0.5(w^{(PC)})_{min} < w < 1.5(w^{(PC)})_{max}$) (0.3mm<$w$<1.3mm) and 0.1mm<$d$<0.8mm [14].

Table 1: Dimensions of the PC λ/2 filter ($L_0^{(PC)}$=5mm, $w_{50\Omega}$=0.87mm).

			all dimensions are in mm			
i	$Z_{0e}[\Omega]$	$Z_{0o}[\Omega]$	$w_i^{(PC)}$	$d_i^{(PC)}$	$l_i^{(PC)}$	$w_{i,cor}^{(PC)}$
0	64.075	41.171	0.752	0.172	24.445	0.88
1	52.638	47.614	0.863	0.651	24.225	0.88
2	54.193	46.412	0.853	0.496	24.249	0.88
3	58.119	43.902	0.819	0.3	24.323	0.88
4	78.073	37.992	0.59	0.1	24.658	0.59

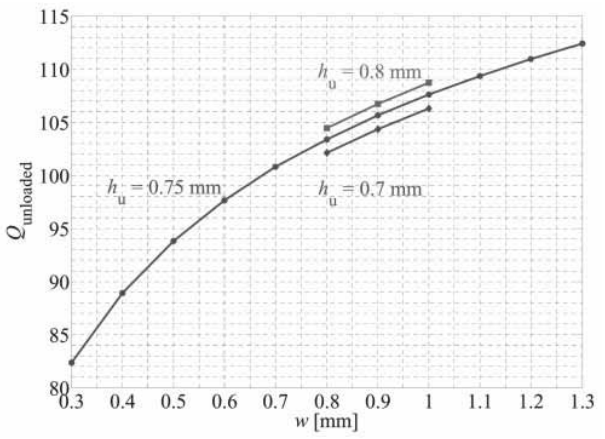

Figure 6: Design curve of unloaded Q-factor of half-wavelength resonator as a function of the line width.

The unloaded Q-factor for the resonators is estimated by using the expected midband filter loss A_0:

$Q_u = \frac{4.343}{B\,A_0}\sum_{i=1}^{N} g_i$ [dB]=105.28, where g_i, i=1,...N, are the lowpass prototype parameters and N is a filter order. The unloaded Q-factor of a half-wavelength resonator is shown in Figure 6, as a function of the line width. Q-factor of the actual fabricated resonator can be sensitive to the manufacturing processes and depends on the distance between the metallic top cover and dielectric. Therefore two additional curves are presented in Figure 6, for h_u=0.7mm and h_u=0.8mm. For expected midband filter loss A_0, we have found that the initial width of the half-wavelength resonator is $w_0^{(PC)}$=0.88mm.

3.1. Covered hairpin filter

To find the optimal dimensions of hairpin resonators we proceed as follows: (1) if the line width $w^{(PC)}$ differs more than 25% from the initial value $w_0^{(PC)}$, we do not change this value; (2) for all other cases we set the line width to the initial value (see Table 1).

The initial length of the hairpin arm is L=22.9mm and the distance between the arms is d_0=5h=2.54mm. From the desired external quality factors, according to the design curves shown in Figure 7, we find the initial width of the feed line and coupling gap (separation) between the feed line and the corresponding resonator, Table 2.

The coupling gaps between resonators are found according to the design curves shown in Figure 8, as follows: d_{23}=0.63mm, d_{34}=0.45mm, and d_{45}=0.3mm, which correspond to the coupling coefficients M_{12}, M_{23}, M_{34} respectively.

The initial dimensions are refined by optimization and the corrected dimensions are presented in Table 3.

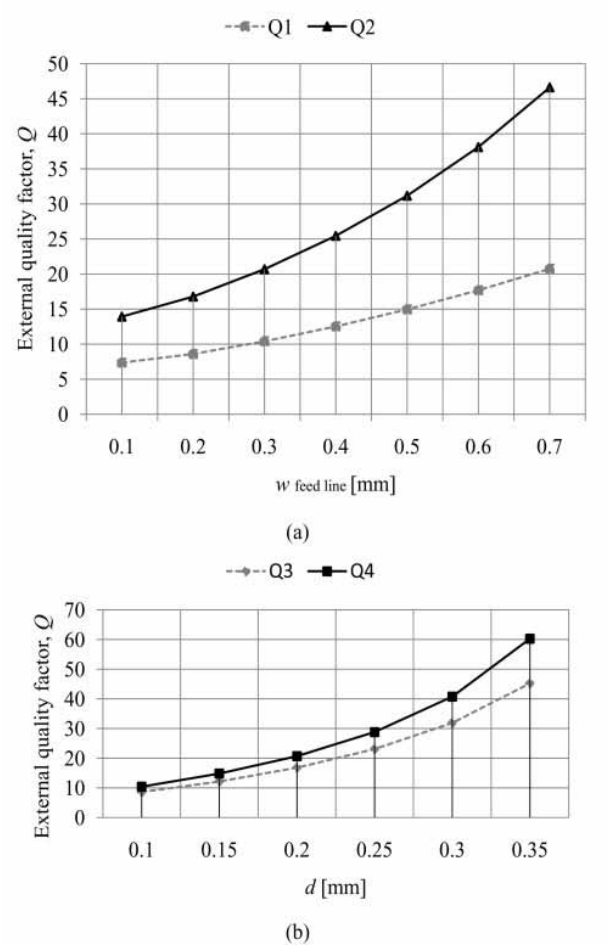

Figure 7: External quality factor for the hairpin band-pass filter when w=0.88mm: (a) Q1 for coupling gap (separation) d=0.1mm and Q2 for d=0.2mm, (b) Q3 for $w_{feedline}$=0.2mm and Q4 for $w_{feedline}$=0.3mm.

Table2: Dimensions of the feed lines and coupling gaps of the single layer hairpin filter.

	w_1	w_2	w_3	w_4	w_5	w_6	$w_{50\Omega}$	L
Initial	0.3	0.88	0.88	0.88	0.59	0.2	0.87	22.9
Optimized	0.3	0.9	0.96	0.89	0.61	0.23	0.87	22.86

	d_0	d_{12}	d_{23}	d_{34}	d_{45}	d_{56}	l_{01}	l_{02}
Initial	2.54	0.25	0.63	0.45	0.3	0.125	4.5	0.5
Optimized	2.54	0.2	0.63	0.45	0.27	0.13	4.5	0.5

Table 3: Dimensions of the single layer hairpin filter (all dimensions are in mm).

No. of port	First	Second
Width (feed line)	0.3 mm	0.2 mm
Coupling gap (feed line & resonator)	0.25 mm	0.125 mm
External Q-factor	30	9.8

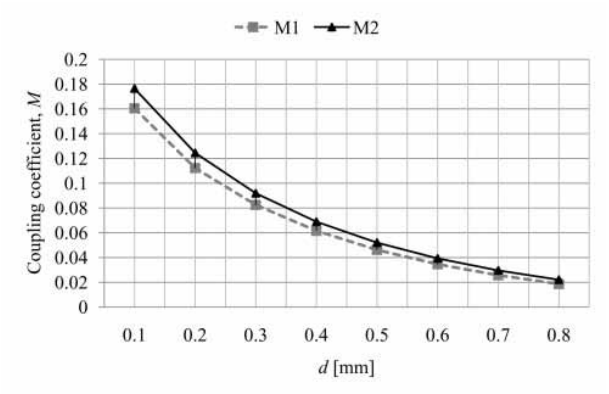

Figure 8: Coupling coefficient for the single layer hairpin filter: M1 for the identical hairpin resonators (w_1=w_2=0.88mm), M2for the resonators with different width (w_1=0.88mm, w_2=0.59mm).

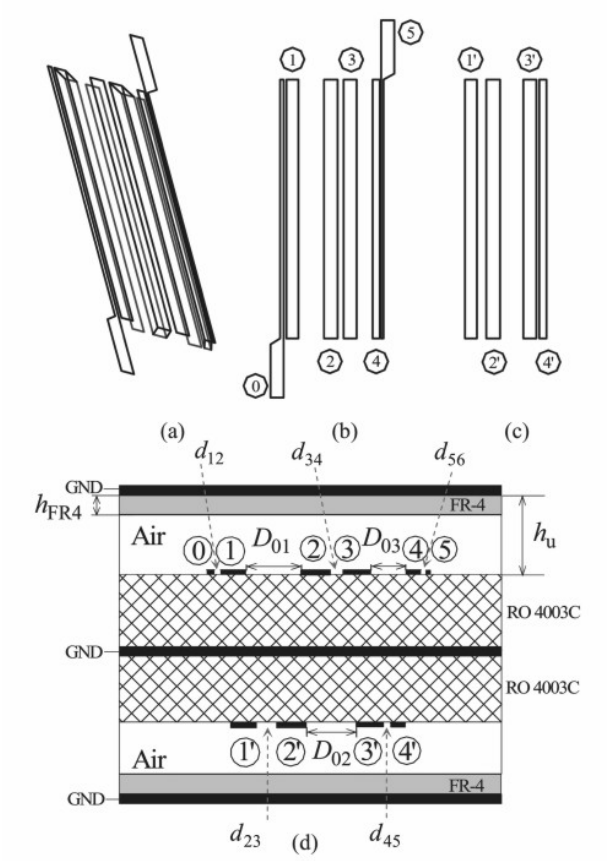

Figure 9: Configuration of the proposed multilayer filter: (a) 3D model (without common ground plane and dielectric layers), (b) top view – top conductor lines, (c) bottom view – bottom conductor lines, (d) cross section of multilayer filter with common ground plane (vias are not shown). The arms of resonators are numbered from 1 to 4 and the feed lines with 0 and 5.

3.2. Covered multilayer filter with modified hairpin resonators

The multilayer filter is obtained from the optimized single layer hairpin filter. The hairpin resonator and the modified hairpin resonator are electrically equivalent: the line width and the length of the arms are the same. In the multilayer filter, the modified hairpin resonator is realized with a via that connects the arms. The length of the via and the via pad should correspond to the line that connects the arms of a hairpin resonator in the single layer structure. The coupling gaps between the arms of adjacent modified hairpin resonators are the same as in the single layer realization.

In the multilayer filter, there are arms, on the same side of multilayer structure, which should not be coupled. The distance between these arms (D_0 in Figure 5) should provide a negligible coupling, but is limited by the via design and requirements for miniaturization. The optimal values of D_0 are D_{01}=1.9mm, D_{02}=1.72mm, and D_{03}=1.3mm . The configuration of the proposed multilayer bandpass filter is shown in Figure 9.

Frequency response of the covered hairpin filter and covered multilayer filter is shown in Figure 10. The curves are generated by circuit simulation [15] and verify the equivalence between the two filter realizations.

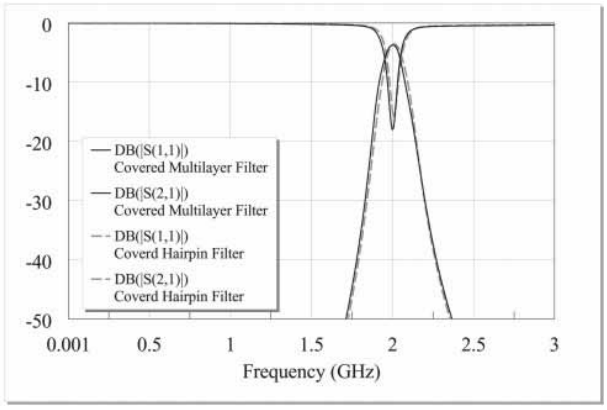

Figure 10: Scattering parameters of the equivalent circuit model of the single layer and the multilayer filter housed in a metallic box.

3.3. Experimental results

The fabricated multilayer filter has a footprint of $0.257\lambda_g$ x $0.072\lambda_g$, 24.86mm x 7.01mm (not including the feed lines and guard zone), where λ_g is the guided wavelength of a 50Ω line on the substrate at the center frequency. Thus, we can conclude that the proposed design achieves a size reduction of 50%, as compared to the conventional covered hairpin filters implemented on a single layer at the same band.

The structure is housed in a metallic box and the distance between both metallic covers (top and bottom) and dielectric is h_u=0.85mm, Figure 9d. The covers are realized with FR-4 laminate of 0.85mm thickness with t=18μm copper cladding on one side. With milling process [16] we removed almost all FR-4 substrate without digging into the copper foil. After milling, we have found that a thin dielectric layer of thickness h_{FR4}=0.4mm remained. This imperfection has been added in the final 3D EM model of the multilayer filter [17].

The filter dimensions are checked after fabrication in order to find the deviation from the designed values. It is found that the maximum deviation is 5μm.

The photograph of the fabricated filter is shown in Figure 11. The filter is measured using an Agilent E5062A network analyzer. The filter enclosure minimizes "leakage" of the energy from the electromagnetic field and hence reduces conducted emissions.

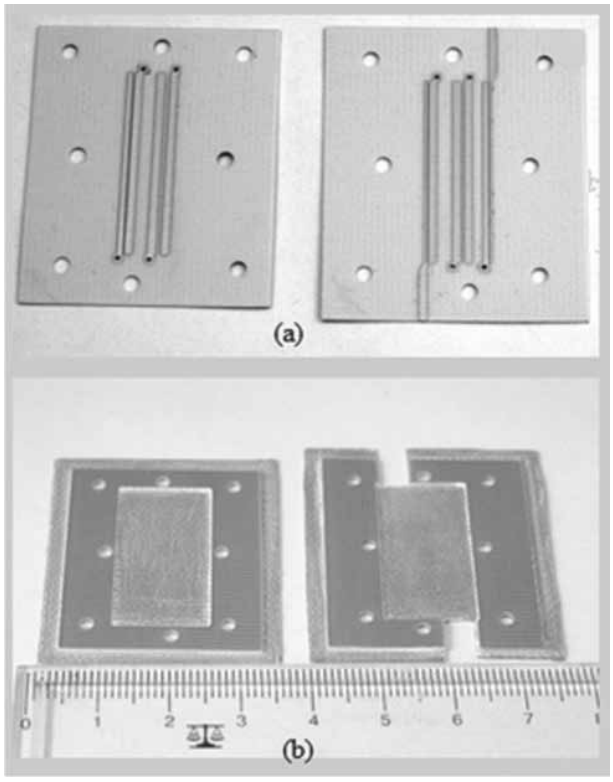

Figure 11: Photograph of the filter: (a) conductor lines – top/bottom view, (b) metallic top/bottom cover.

The simulated and measured response of the proposed filter is shown in Figure 12. Measured results have validated the theoretical analysis well. The filter has an insertion loss of 3.26dB at the central frequency (1.89GHz)

due to the conductor and dielectric losses. The conductor losses dominate. The center frequency is shifted by 110MHz for several reasons: (1) the tolerance of ε_r of RO4003C substrate [9], (2) parasitic dielectric layer on the covers, and (3) the fabrication tolerances.

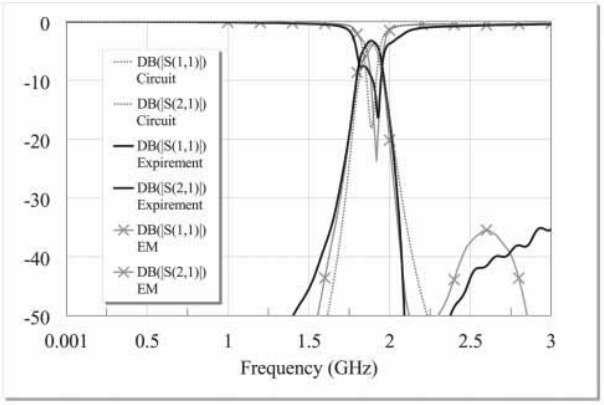

Figure 12: Scattering parameters of the covered multilayer filter with modified hairpin resonators: circuit simulation, EM simulation, and experiment.

4. Conclusion

We have studied realizations of a compact multilayer bandpass filter that has been deduced from the corresponding covered hairpin filter. A novel realization of the multilayer bandpass filter has been presented and it is based on the modified hairpin resonator realized on a double-sided microstrip structure. The benefit of the proposed multilayer filter is a reduction of the footprint by 50% without changing the performance of the original hairpin filter.

In this paper, we have presented the new method to reduce the size of a hairpin filter without deteriorating the filter performance. First, we have designed the optimal single layer hairpin filter with a top metallic cover. Secondly, the hairpin resonators have been replaced by equivalent modified hairpin resonators which were printed in two layers.

Design methodology has been presented and validated by EM simulation. The multilayer filter has been fabricated, measured, and the experimental results are in good agreement with the theoretical and simulation results.

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